NANOSCALE VACUUM ELECTRONIC DEVICES

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High-speed electronic devices rely on short carrier transport times, which are usually achieved by decreasing the channel length and/or increasing the carrier velocity. Ideally, the carriers enter into a ballistic transport regime in which they are not scattered. However, it is difficult to achieve ballistic transport in a solid-state medium because the high electric fields used to increase the carrier velocity also increase scattering. Vacuum is an ideal medium for ballistic transport, but vacuum electronic devices commonly suffer from low emission currents and high operating voltages. We have developed a low-voltage field-effect transistor with a vertical vacuum channel (channel length of ~20 nm) etched into a metal–oxide–semiconductor substrate. We measure a transconductance of 20 nS μm^{-1}, an on/off ratio of 500 and a turn-on gate voltage of 0.5 V under ambient conditions. Coulombic repulsion in the two-dimensional electron system at the interface between the oxide and the metal or the semiconductor reduces the energy barrier to electron emission, leading to a high emission current density (~1×10^5 A cm^{-2}) under a bias of only 1 V. The emission of two-dimensional electron systems into vacuum channels could enable a new class of low-power, high-speed transistors.

Harboring a two-dimensional electronic system, graphene can be highly conductive in in-plane transport while being transmissive to impinging electrons. Based on these in- and out-of-plane interaction properties, a suspended graphene membrane is promising as an ideal gate (grid) to control electron transport in nanoscale vacuum electronic devices. We have measured capture and transmission efficiencies of very low energy (< 3 eV) electrons impinging upon a suspended

graphene anode that is placed on top of a nanoscale void channel formed in a SiO_2/Si substrate. Electron capture efficiency of 0.1 % (transmission efficiency of 99.9 %) is observed at 1 V bias. Presence of suspended graphene is also found to significantly enhance electron emission at cathode beyond the level of Child-Langmuir's space-charge-limited emission.

Photocarrier multiplication, the process of generating two or more electron-hole pairs from a single absorbed photon, can occur in semiconductor quantum dots or nanocrystals. Translating this carrier-level performance into a device-level improvement in sensing or converting photon energy, however, remains challenging. We have developed a graphene/SiO_2/Si photodetector with a nanoscale void channel that demonstrates internal quantum efficiency of 115-175% measured with photocurrent in UV-Vis range. The self-induced electric field in 2D electron gas of a graphene/oxide/Si structure enables photocarrier multiplication.

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PREFACE

First and foremost I would like to express the deepest appreciation to my advisor, Professor Hong Koo Kim for his excellent guidance, caring and patience. He has the attitude and substance of a genius: he continually and convincingly conveyed a spirit of adventure in regard to research and life. His mentorship was paramount in providing a well-rounded experience consistent with my long-term career goals. He encouraged me to not only grow as a scientist but also as an instructor and an independent thinker. For everything you have done for me, Dr. Kim, I thank you. Without his guidance and persistent help this dissertation would not have been possible.

I would also like to thank Dr. Yun Suk Jung and Dr. Dongxiao Li for their assistance and guidance for the past several years, helping me to develop my experimental background. Additionally, I am very grateful for the friendship of all of the members of research group, especially Myungji Kim, with whom I worked closely and puzzled over many of the same problems. She also provided for some much needed humor and entertainment in what could have otherwise been a somewhat stressful in laboratory environment.

I would like to thank the Department of Electrical and computer engineering at university of Pittsburgh, especially those members of my doctoral committee for their input, valuable discussions and accessibility. I also would like to thank Royal Thai Scholarships for providing me invaluable opportunity to further my education abroad to enrich and broaden my skill, knowledge and experience.

Finally, and most importantly, I would like to thank my family for their faith in me. For my parents who raised me with unwavering love, supporting me and encouraging me with their best wishes and quiet patience. For the presence of my best friend, Nongnooch Roongpiboonsopit, who endured and provided me unending love, encouragement and support.

Above all, I owe it all to God for granting me the wisdom, plan, health and strength enabling me to its completion.

1.0 INTRODUCTION

Following the Moore's law the number of transistors placed on an integrated circuit has doubled every two years over the past forty years. Each doubling of transistor density is enabled by shrinking the transistor size, resulting in better performance of chips, for example, faster and more energy efficient computers. As the transistor size approaches the bottom nanometer scale, however, it is increasingly difficult and expensive to extend the Moore's law. The common requirement in developing high speed electronic devices is to reduce the carrier transport time, and this has been achieved by decreasing the channel length and/or by increasing the carrier velocity [1]. The carrier velocity has also been greatly enhanced in terms of its mobility in the case of steady-state transport regime, or alternatively by shifting towards the high-field ballistic regime of operation in the non-equilibrium transport case.

Achieving a ballistic transport of charge carriers in solid-state medium requires a careful design of materials and structure, because high electric field applied across a channel often incurs numerous conflicting situations with a requisite scattering free transport in the medium [2]. Vacuum would serve as ideal medium for ballistic transport of electrons, but vacuum electronic devices commonly suffer from low emission current and high operating voltage.

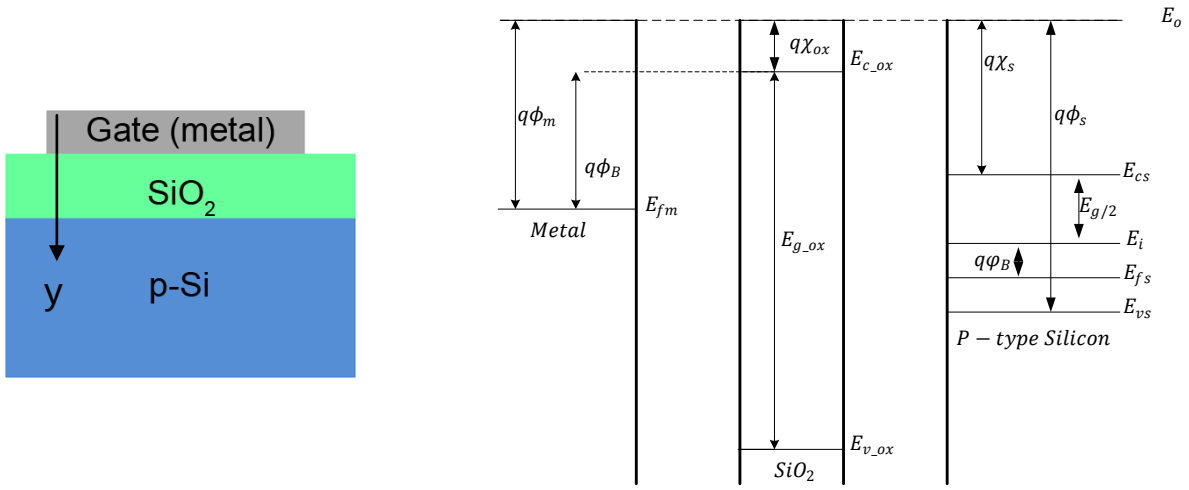
In this thesis we propose to use nanoscale vacuum as a medium for scattering free transport of electrons in air ambient. We demonstrate that a nanoscale void channel (~20 nm length) vertically etched into a Si metal-oxide-semiconductor substrate can be utilized as a

conduit for ballistic electrons. Coulombic repulsion in a two-dimensional electron system [3] induced in cathode (Al or Si) is found to significantly reduce barrier height at the edge, enabling thresholdless emission of electrons. A field-effect-transistor, in which a gate layer controls electron emission from cathode, demonstrates a transconductance of 20 nS/μm and an on/off-current ratio of 500.

Regarding the nanoscale void channel formation we have explored two different approaches: localized oxide breakdown by electric pulses (Chapter 2) and focused ion beam (FIB) etching techniques (Chapters 3 and 4). Both methods enable formation of nanovoid channels in a MOS structure, as demonstrated with the Child-Langmuir's space charge limited current flow in the void channels. In this chapter, the fundamentals of MOS capacitor structure and electron emission/transport properties are reviewed [1, 40].

1.1 MOS CAPACITOR STRUCTURE

Figure 1 shows a typical MOS capacitor formed on p-type silicon substrates with silicon dioxide thermally grown on the substrate. The energy band diagram of the MOS structure can be sketched as follows:



(a) (b)

Figure 1 (a) The MOS capacitor structure, (b) Energy band diagram of the MOS structure

For the sake of simplicity, it is assumed that there is neither interface trap nor any kind of oxide charge inside the insulator and silicon oxide is perfect insulator whose resistivity is infinite. It implies that any leakage current passing through the insulator is negligible. As indicated on the figure 1b, $q\phi_m$ is the work function of the metal gate, $q\phi_s$ is the Fermi level of silicon, $q\chi_{ox}$ is the electron affinity of the oxide, $q\chi_s$ is that of silicon, and E_g is the energy gap of silicon. The energy gap of the oxide is quoted in the literature to be between 8 and 9 electron volt. The work function is the energy required to extract an electron from the Fermi level to the

vacuum level. The work function of material is assumed to be 4.5 eV for tungsten (W) and 4.1 eV for Al. However, in thermal equilibrium, when three materials with different work functions come closer to form MOS capacitor shown in figure 2, a band bending occurs with the flat band voltage expressed as follows.

$$V_{FB} = \phi_m - \phi_s \tag{1.1}$$

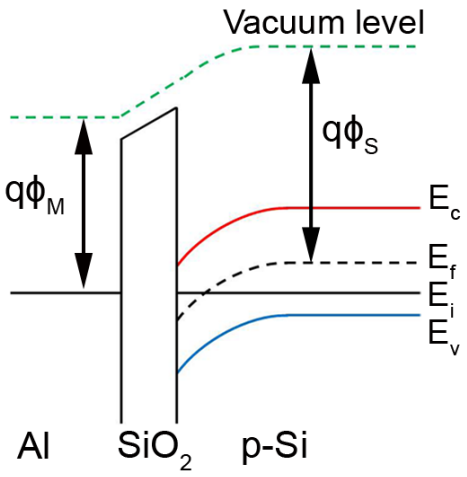


Figure 2 Energy band diagram of MOS capacitor at thermal equilibrium

1.1.1 Electric field, surface charge density and surface charge potential inside MOS capacitor

Figure 3 shows the energy band diagram with charge distributions across the MOS structure.

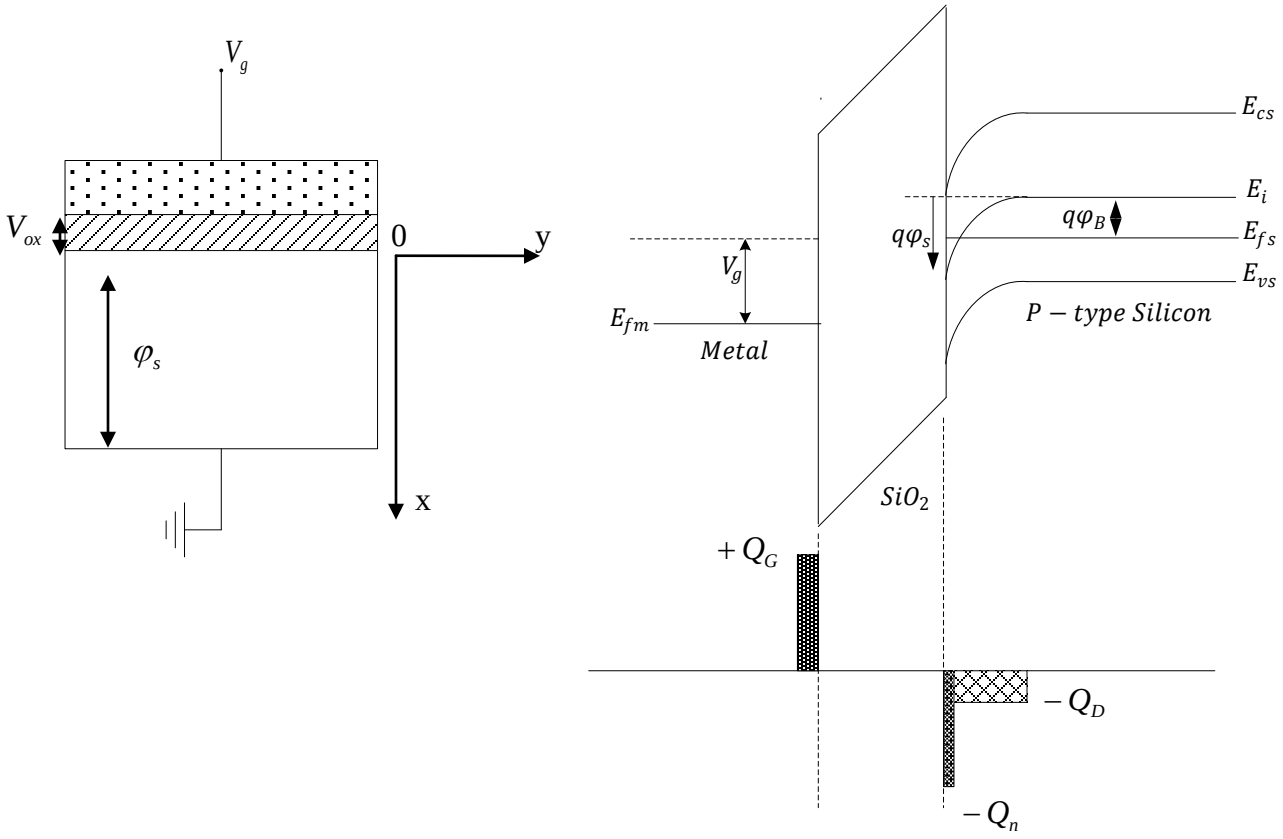


Figure 3 The energy band diagram with charge distributions across the MOS structure: (a) The MOS structure and bias voltage, (b) The energy band diagram with charge distributions

The electron and hole concentrations as a function of potential (φ) can be defined by

$$n_p(x) = n_{po} e^{\beta\varphi} \tag{1.2}$$

$$p_p(x) = p_{po} e^{-\beta\varphi} \tag{1.3}$$

The gate voltage can be calculated by

$$V_g = V_{FB} + V_{oxide} + \varphi_s + V_{SB} \tag{1.4}$$

In this experiment, V_{SB} = 0. Thus, the voltage drop across the oxide layer is estimated to be

$$V_{oxide} = V_g - V_{FB} - \varphi_s \tag{1.5}$$

The electric field inside the oxide layer can be expressed as

$$E_{oxide} = \frac{V_{ox}}{t_{ox}} = \frac{Vg - \varphi_s}{t_{ox}} \tag{1.6}$$

From the Gauss's law, the amount of charge at the oxide/semiconductor interface is determined to be

$$E_{oxide}\varepsilon_{ox} = \varepsilon_s E_s = Q_s \tag{1.7}$$

Here the oxide capacitance is

$$C_{oxide} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{1.8}$$

Determining the actual electric field across the oxide is not straightforward since the electric potential is a function of surface potential and the surface potential is a function of gate voltage as well. To find the surface potential, electric field and surface charge density, Poisson's equation is used

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} \tag{1.9}$$

$$\rho(x) = q(N_D{}^+ - n_p - N_A{}^- + p_p) \tag{1.10}$$

From the charge neutrality condition inside the bulk semiconductor and an assumption of complete ionization,

$$N_D^{+} = n_{po}, N_A^{-} = p_{po} \tag{1.11}$$

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{q(n_{po} - n_p - p_{po} + p_p)}{\varepsilon_s} \tag{1.12}$$

$$\frac{d^2\varphi}{dx^2} = -\frac{q[p_{po}(e^{-\beta\varphi} - 1) - n_{po}(e^{\beta\varphi} - 1)]}{\varepsilon_s} \tag{1.13}$$

Integrating Equation (1.13) from the bulk toward to the surface in conjunction with the boundary condition that $\varphi = 0, \frac{d^2\varphi}{dx^2} = 0$

$$\left(\frac{d\varphi}{dx}\right)^2 = \left(\frac{2}{\beta}\right)^2 \frac{qp_{po}\beta}{2\varepsilon_s\left[(e^{-\beta\varphi} + \beta\varphi - 1) + \frac{n_{po}}{p_{po}}(e^{-\beta\varphi} - \beta\varphi - 1)\right]} \tag{1.14}$$

The electric field is $E = -\left(\frac{d\varphi}{dx}\right)$, and the electric field (E_s) at the semiconductor/oxide interface can be expressed as a function of surface potential:

$$E_s = \frac{\sqrt{2}}{\beta L_D\left[(e^{-\beta\varphi_s} + \beta\varphi_s - 1) + \frac{n_{po}}{p_{po}}(e^{-\beta\varphi_s} - \beta\varphi_s - 1)\right]} \tag{1.15}$$

where $L_D = \sqrt{\frac{\varepsilon_s}{qp_{po}\beta}}$ is extrinsic Debye length for hole.

Gauss's law is used to calculate the total space charge per unit area (Q_s) at the silicon and oxide interface.

$$\oint E_s.ds = \frac{Q_s}{\varepsilon_s} \tag{1.16}$$

$$\left|Q_s\right| = \varepsilon_s E_s = \frac{\sqrt{2}\varepsilon_s}{\beta L_D}\left[(e^{-\beta\varphi_s} + \beta\varphi_s - 1) + \frac{n_{po}}{p_{po}}(e^{\beta\varphi_s} - \beta\varphi_s - 1)\right]^{1/2} \tag{1.17}$$

$$\left|Q_s\right| = \left|Q_n\right| + \left|Q_D\right| \tag{1.18}$$

Q_n is the electron charges per unit area in the inversion region and Q_D is the depletion region charge density. It should be noted that in most literature, according to the variation of $\left|Q_s\right|$ as a function of the surface potential, φ_s, the four regions of operation of a MOS capacitor structure can be separated into accumulation ($\varphi_s < 0$, Q_s is positive), flat band (φ_s and $Q_s = 0$) , depletion ($0 < \varphi_s < \varphi_B$, Q_s is negative) and inversion ($\varphi_s > \varphi_B$ (weak), $2\varphi_B$ (strong), Q_s is negative)

The threshold voltage is then determined as follows

$$Q_s(\varphi_s = 2\varphi_B) = Q_{D\max} = -\sqrt{2\varepsilon_s qN_A(2\varphi_B)} \tag{1.19}$$

$$V_{TH} = V_{g(\varphi_S = 2\varphi_B)} = V_{FB} + V_{oxide} + 2\varphi_B \tag{1.20}$$

$$V_{TH} = V_{FB} + \left|\frac{Q_{D\max}}{C_{oxide}}\right| + 2\varphi_B \tag{1.21}$$

For example, in the electrically-induced formation of highly-localized ballistic nanoscale leakage channels experiment, two types of electrodes were mainly used as gate electrode: tungsten (W) and gold (Au). The work function of W or Au is 4.5 eV or 4.7 eV, respectively. The work function of the p-type Si substrate used in this experiment can be calculated as 4.9eV (n_i =

$1.55\times10^{10}cm^{-3}$, T = 300K, $N_A = 1.32\times10^{15}cm^{-3}$). Thus, flat band voltage (V_{FB}) is around -0.5V (tungsten), -0.3V (gold). With ε_o = 8.85×10^{-12}F/m, $\varepsilon_s = 11.9\varepsilon_o$, $\varepsilon_{ox} = 3.9\varepsilon_o$, the variation of space charge density in the p-type Si with tungsten and gold electrode as a function of the surface potential (φ_s) and gate voltage (V_g) can be plotted as shown in figure 4-5. The electric field across oxide as a function of the gate voltage is shown in figure 6-7.

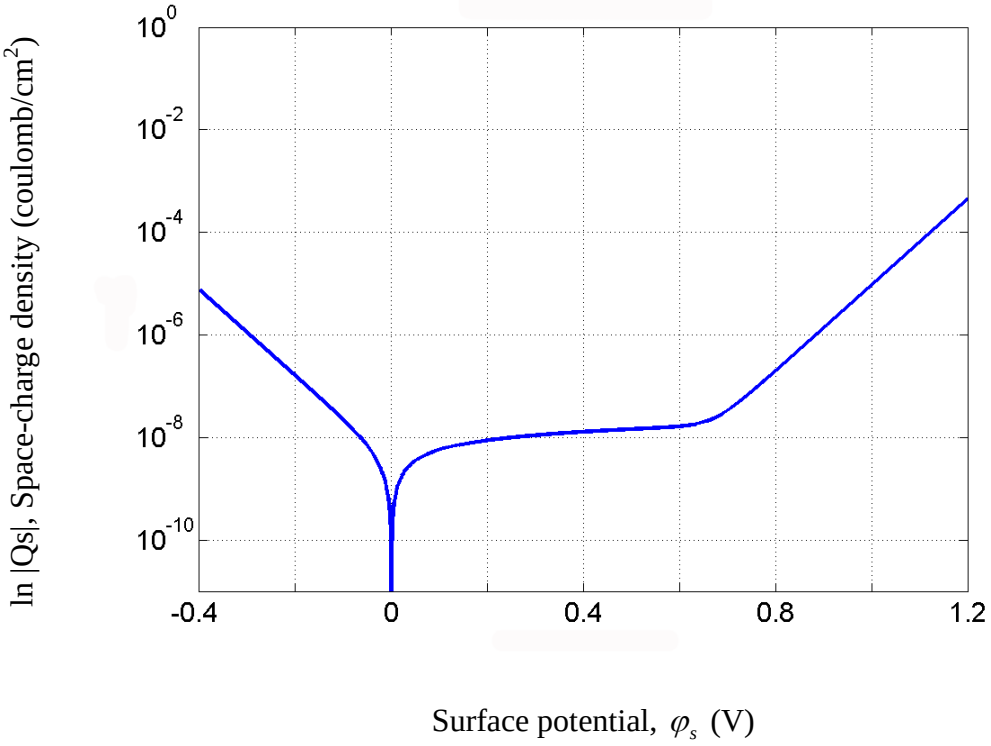


Figure 4 The space charge density in the semiconductor as a function of the surface potential (φ_s): calculated for a p-type silicon with $N_A = 1.32\times10^{15}cm^{-3}$ at room temperature

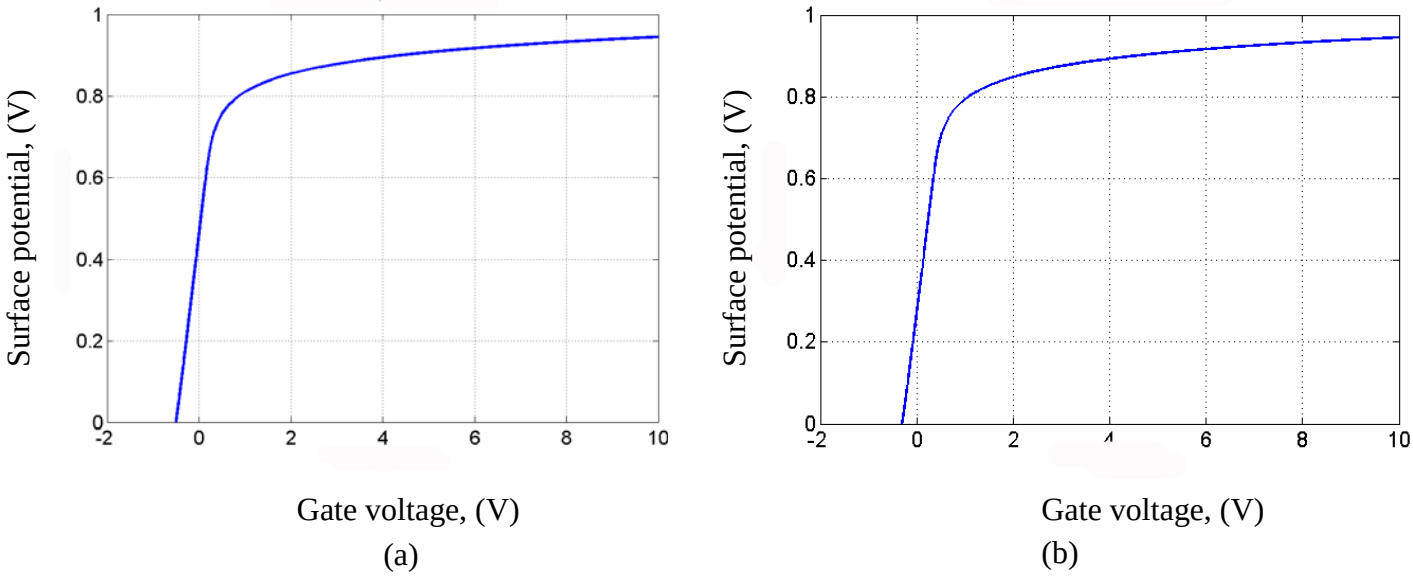
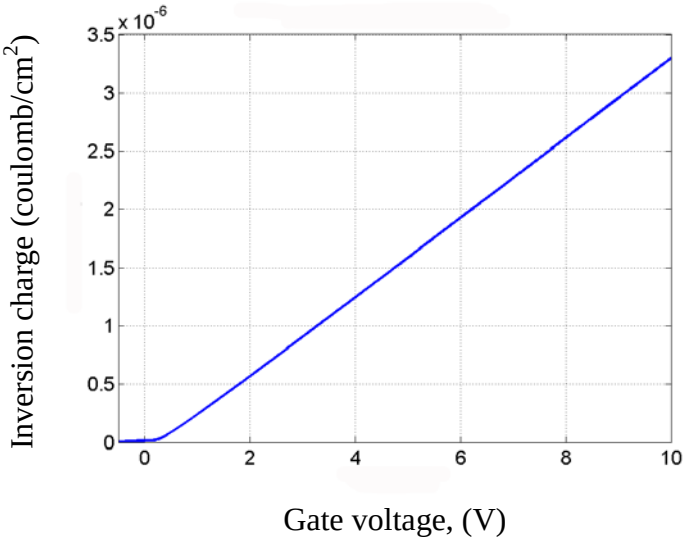
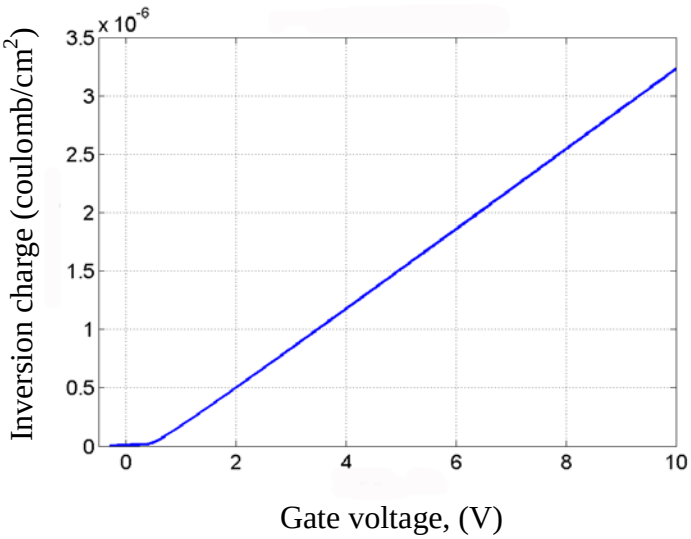


Figure 5 The surface potential of the semiconductor as a function of the gate voltage for (a) Tungsten electrode, (b) Gold electrode

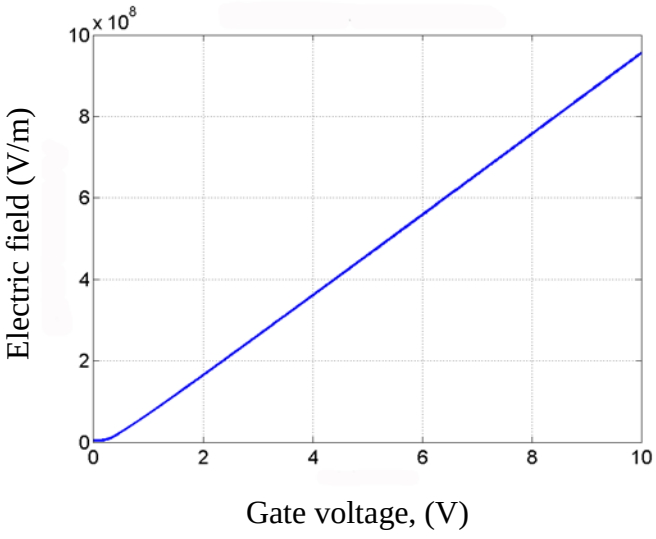


(a)

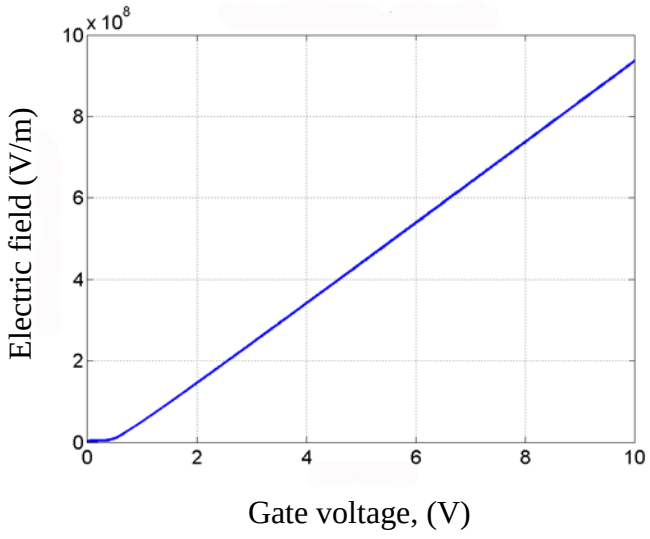


(b)

Figure 6 The inversion charge as a function of the gate voltage for (a) Tungsten electrode, (b) gold electrode



(a)



(b)

Figure 7 The electric field across oxide as a function of the gate voltage for (a) Tungsten electrode, (b) gold electrode

1.2 ELECTRON EMISSION AND TRANSPORT

To understand the electrical properties of the device structures developed in this work, we review first electron emission and transport mechanisms: thermionic and tunneling emission, and ballistic transport [1, 40].

1.2.1 Thermionic electron emission

Electrons confined in metal can gain enough thermal energy (kT) and escape from the metal. This is called "thermionic emission" as demonstrated in vacuum tube filaments. The thermionic emission theory assumes that electrons, with energy larger than the top of the barrier, moving toward to the barrier will cross the barrier. The actual shape of the barrier is hereby ignored. The driving force of this process is the thermal energy which provides a non-zero density of carriers at energies larger than the confining barrier. The current density associated with this process is obtained from:

$$J_x = \int qn(E)v_x(E)dE \tag{1.22}$$

where q is the electronic charge, $n(E)$ is the density of electrons per unit energy and per unit volume and $v_x(E)$ is the velocity of the electrons with which they approach the barrier. The integral is to be taken over all electron energies large enough energy to surmount the barrier and must include only electrons moving towards the barrier. The electron density is obtained by multiplying the density of states function with the Fermi function yielding:

$$n(E)d(E) = f(E)g_c(E)dE = \frac{8\pi\sqrt{2}}{h^3}m^{3/2} * \frac{\sqrt{E}dE}{1+\exp(\frac{E-E_F}{kT})} \tag{1.23}$$

The energy can be written as a function of the electron velocity using:

$$E = \frac{mv^2}{2} \rightarrow \sqrt{E}dE = \frac{m^{3/2}}{\sqrt{2}}v^2dv \tag{1.24}$$

which yields:

$$n(E)d(E) = \frac{8\pi\sqrt{2}}{h^3}m^{3/2} * \frac{\sqrt{E}dE}{1+\exp(\frac{E-E_F}{kT})} \cong \frac{2m^3}{h^3}e^{-\frac{(E-E_F)}{kT}}4\pi v^2dv \tag{1.25}$$

where the Fermi function is approximated by the Maxwell-Boltzmann distribution function. This is based on the assumption that the Fermi energy is at least *3kT* below the top of the barrier as typical case. The energy can be further expressed as a function of the velocity components in the *x*, *y* and *z* direction:

$$E = \frac{mv^2}{2} = \frac{m}{2}(v_x{}^2 + v_y{}^2 + v_z{}^2) \tag{1.26}$$

so that the integral can be written as a product of three integrals, one for each velocity component. The intergral over v_y and v_z extends from minus to plus infinity, while the integral over v_x start from the minimum velocity in the positive x direction needed to overcome the barrier, $v_{x,\min}$, to infinity, yielding:

$$J_x = \frac{2qm^3}{h^3} e^{E_F/kT} \int_{v_{x,\min}}^{\infty} v_x e^{-\frac{mv_x^2}{2kT}} dv_x \int_{-\infty}^{\infty} e^{-\frac{mv_y^2}{2kT}} dv_y \int_{-\infty}^{\infty} e^{-\frac{mv_z^2}{2kT}} dv_z \tag{1.27}$$

The integrals over v_y and v_z can be solved using the following definite integral:

$$\int_{-\infty}^{\infty} e^{-t^2} dt = \sqrt{\pi} \tag{1.28}$$

while the minimum velocity in the x direction required to overcome the barrier is obtained by setting the kinetic energy equal to the barrier height:

$$E_{\min} = q\Phi_B + E_F = \frac{mv_x^2}{2} \tag{1.29}$$

which yields:

$$J_x = \frac{2qm^3}{h^3} e^{-\frac{q\Phi_B}{kT}} \frac{kT}{m} \sqrt{\frac{2\pi kT}{m}} \sqrt{\frac{2\pi kT}{m}} = \frac{4\pi qmk^2}{h^3} T^2 e^{-\frac{q\Phi_B}{kT}} \tag{1.30}$$

This can be rewritten as:

$$J_x = A_R T^2 e^{-\frac{q\Phi_B}{kT}} \tag{1.31}$$

where A_R is referred to as being the Richardson constant and is given by:

$$A_R = \frac{4\pi q m k^2}{h^3} \tag{1.32}$$

The expression for the current due to thermionic emission can also be written as a function of the average velocity with which the electrons at the interface approach the barrier. This velocity is referred to as the Richardson velocity given by:

$$v_R = \sqrt{\frac{kT}{2\pi m}} \tag{1.33}$$

So that the current density becomes:

$$J_n = q v_R N_c \exp(-\frac{\Phi_B}{V_t})\left[\exp(\frac{V_a}{V_t}) - 1\right] \tag{1.34}$$

1.2.2 Field Emission - Fowler-Nordheim tunneling

Field emission is an alternative emission mechanism that can extract electrons out of the potential barrier. For sufficient electric fields, significant numbers of electrons can tunnel through the energy barrier and escape to the vacuum level. This effect is called field emission. For metal, with typical work function and a flat surface, the threshold field is typically around 10^5 - 10^8 V/ cm [20]. It works even at room temperature and is barely temperature dependent. This is a preferred mechanism, compared to thermionic emission, for certain applications because no heating of cathode is required and the emission current is almost solely controlled by external field.

The field emission current from a metal surface is determined by the Fowler–Nordheim (F–N) equation: the process whereby electrons tunnel through a barrier in the presence of a high electric field. This quantum mechanical tunneling process is an important mechanism for thin barriers as those in metal/semiconductor junctions on highly-doped semiconductors or in MOS structure. From the time independent Schrödinger equation and assuming the triangular potential, the tunnel probability, i.e. the probability that one electron having energy *Ex* along the x-axis goes through the potential barrier can be expressed:

$$-\frac{\hbar^2}{2m^*}\frac{d^2\Psi}{dx^2}+V(x)\Psi=E\Psi \tag{1.35}$$

which can be rewritten as

$$\frac{d^2\Psi}{dx^2}=\frac{2m^*(V-E)}{\hbar^2}\Psi \tag{1.36}$$

Assuming that *V(x)-E* is independent of position in a section between *x* and *x+dx* this equation can be solved yielding:

$$\Psi(x+dx)=\Psi(x)\exp(-kdx);k=\frac{\sqrt{2m^*[V(x)-E]}}{\hbar} \tag{1.37}$$

The minus sign is chosen since we assume the particle to move from left to right. For a slowly varying potential the amplitude of the wave function at $x = L$ can be related to the wave function at $x = 0$:

$$\Psi(L) = \Psi(0)\exp\left[-\int_0^L \frac{\sqrt{2m^*}\left[V(x)-E\right]}{\hbar}dx\right] \tag{1.38}$$

This equation is referred to as the *WKB* approximation. From this the tunneling probability, Θ, can be calculated for a triangular barrier for which $V(x)\text{-}E = q\phi_B(1-\frac{x}{L})$

$$\Theta = \frac{\Psi(L)\Psi^*(L)}{\Psi(0)\Psi^*(0)} = \exp\left[-2\int_0^L \frac{\sqrt{2m^*}}{\hbar}\sqrt{q\phi_B(1-\frac{x}{L})}dx\right] \tag{1.39}$$

Form $\int_0^L \sqrt{1-\frac{x}{L}dx} = \frac{2L}{3}$, the tunneling probability then become

$$\Theta = \exp\left[-\frac{4}{3}\frac{\sqrt{2qm^*}}{\hbar}\frac{\phi_B{}^{3/2}}{qF}\right] \tag{1.40}$$

where F is the electric field. As The typical final formula of the tunneling current density is

$$J_{FN} = \frac{4q\pi m(k_BT)^2}{h^3C^2}\Theta\left[\frac{C\pi}{\sin(C\pi)}\right] \tag{1.41}$$

where the tunneling probability Θ and the constant C are, respectively

$$\Theta = \exp\left[-\frac{4}{3}\frac{\sqrt{2qm^*}}{\hbar}\frac{\phi_B{}^{3/2}}{qF}\right] \tag{1.42}$$

and

$$C = k_B T \sqrt{\frac{8\pi^2 m}{h^2}} \int_0^L \frac{1}{\sqrt{q\phi(x) - E_f}} dx \tag{1.43}$$

To determine the constant C for the FN conduction regime, by taking into account that $q\phi(x) - qF.L = 0$, the integral $\int_0^L \frac{1}{\sqrt{q\phi(x) - E_f}} dx$ is equal:

$$\frac{2(q\phi)^{1/2}}{qF} \tag{1.44}$$

The constant C becomes: $C = k_B T \sqrt{\frac{8\pi^2 m}{h^2}} \frac{2(q\phi)^{1/2}}{qF}$

Substituting the expressions for Θ and C into the current density (equation 1.20), the F-N current density is, then, obtained:

$$J_{FN} = \frac{4q\pi m(k_B T)^2}{h^3 \left[k_B T \sqrt{\frac{8\pi^2 m}{h^2}} \frac{2(q\phi)^{1/2}}{qF} \right]^2} \exp\left[-\frac{4}{3} \frac{\sqrt{2qm^*}}{\hbar} \frac{\phi_B{}^{3/2}}{qF} \right] \left[\frac{C\pi}{\sin(C\pi)} \right] \tag{1.45}$$

If $T \rightarrow 0$ (low temperatures) then $C \rightarrow 0$ and the term $\frac{C\pi}{\sin(C\pi)} \rightarrow 1$. Hence the classical expression of F-N current density is

$$J = AF^2 e^{\left[-\frac{B}{F}\right]} \tag{1.46}$$

Where $A = \frac{q^2}{8\pi h\phi}$ and $B = -\frac{4}{3}\sqrt{\frac{8\pi^2 m}{h^2}}\frac{(q\phi)^{3/2}}{q}$

The tunneling current therefore depends exponentially on the barrier height to the *3/2* power.

1.2.3 Ballistic Transport

If the dimensions of a conductive path are considerably larger than the mean free path, the conductance is given by Ohm's law G = S/L, where conductivity, S is a material parameter independent of the sample dimensions. However, Ohm's law fails if the length, L of the conductive path is smaller than the conductivity mean free path. The electron transport can be considered as ballistic inside the conductor. A ballistic transport is expected when a charge carrier drifts under electric field without involving a scattering process. In air ambient, the mean free collision path length is estimated to be 65 nm. In particular, a device whose channel length is designed to be shorter than this mean free collision length, the carriers can travel to destination without collision. The ballistic transport current can then be the dominant mechanism of charge transport. This phenomenon has been conventionally explained by the Langmuir-Child's law using the theory of carrier transport mechanism in vacuum diodes model in which space charges build up near the anode side. Here we first review the derivations of the mean free collision path length in air ambient and the Child-Langmuir's formula

1.2.4 Mean free path in air ambient

The simple approximation of ideal gas law can be employed to calculate the mean free path of electrons.

$$PV = NKT \tag{1.47}$$

where P is absolute pressure (1 atm), V is volume (m^3), N is the number of gas molecules, k is Boltzmann's constant (1.38E-23 m^2 kg s^{-2} K^{-1}), T is absolute temperature of gas (at room temperature, T = 300 K). The key assumptions involved are that there are a very large number of tiny particles compared to the size of distance between particles, and carriers are always moving rapidly in a straight line. Referring to the Maxwell velocity distribution and the assumption that a force is exerted to particles only during collisions, the particle velocity can be expressed as

$$Vrms = \sqrt{\frac{3kT}{m}} \tag{1.48}$$

The kinetic theory is utilized to estimate the average distance between collisions for a gas molecule. If the molecules have diameter, d, then the effective cross-section for collision can be modeled by using a circle of diameter, $2d$, to represent a molecule's effective collision area. The molecule can travel, before it collides with another molecule, to distance

$$\lambda = \frac{1}{\sqrt{2}\pi d^2 n} \tag{1.49}$$

where λ is mean free path of carrier, d is diameter of a molecule, V is the volume occupied by the gas molecule, and gas density, n, can be expressed as term N/V. The $\sqrt{2}$ factor was

introduced for an average relative velocity of the molecules involved in the system. The density is solved by using the ideal gas law,

$$n = \frac{P}{kT} \tag{1.50}$$

Thus, the mean free path of particle in a given ambient can be determined as a function of pressure and temperature as follows

$$\lambda = \frac{kT}{\sqrt{2}\pi d^2 P} \tag{1.51}$$

As an exercise the mean free path for an oxygen molecule in atmospheric pressure at room temperature can be calculated as follows. With Boltzmann's constant (k = 1.38 × 10^{-23} J/K), the temperature (T = 300 K), pressure (760 Torr or 101325 Pascal (kg/ (m·s^2)), and the diameter of an oxygen molecule (~3.6 Angstroms),

$$\lambda = \frac{kT}{\sqrt{2}\pi d^2 P} = \frac{(1.38E-23)(300)}{\sqrt{2}\pi(3.7E-10)^2(101325)} = 67nm$$

1.2.5 Collisionless transport - vacuum diode model

For the sake of simplicity, a vacuum diode model will be used in deriving the relationship between current density and applied voltage, V_o in ballistic regime [11, 12, 41]. Imagine two parallel plate electrodes placed in vacuum. One is connected to positive potential, V_o while the other one is connected to ground as shown in Figure 8.

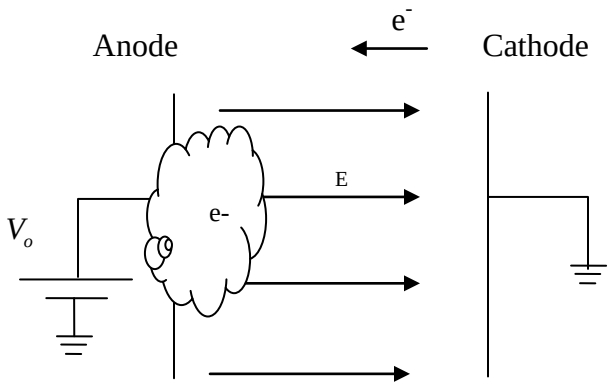


Figure 8 The Space charge limited current in vacuum diode model

The velocity of electrons traveling between the two electrodes is expressed as

$$J = \rho v \tag{1.52}$$

From the Poisson's equation the electric potential and the charge density are related as follows.

$$\frac{d^2V}{dx^2} = \frac{-\rho}{\varepsilon_o} \tag{1.53}$$

The kinetic energy of an electron is related to the electric potential.

$$\frac{1}{2}mv^2 = qV \ ;$$

From $\rho = \frac{J}{v}$; and $v = \sqrt{\frac{2qV}{m}}$

Thus, $$\frac{d^2V}{dx^2} = \frac{J}{\varepsilon_o}\sqrt{\frac{m}{2qV}} \tag{1.54}$$

Multiplying both sides of the equation with $\frac{2dV}{dx}$

$$\frac{2dV}{dx}\frac{d^2V}{dx^2} = \frac{J}{\varepsilon_o}\sqrt{\frac{m}{2qV}}\frac{2dV}{dx} \tag{1.55}$$

Since the potential V is a function of position, rearranging the equation,

$$\frac{d}{dx}\left(\frac{dV}{dx}\right)^2 = \frac{4J}{\varepsilon_o}\sqrt{\frac{m}{2q}}\frac{dV^{1/2}(x)}{dx} \tag{1.56}$$

Integrating both sides over x yields

$$\left(\frac{dV}{dx}\right)^2 = \frac{4J}{\varepsilon_o}V^{1/2}(x)\sqrt{\frac{m}{2q}} \tag{1.57}$$

Integrating again from $V = 0$ to V_o , $x = 0$ to $x = L$, we obtain the expression for the space-charge-limited current flow in vacuum.

$$J = \frac{4\varepsilon_o}{9L^2}\sqrt{\frac{2q}{m}}V_o^{\frac{3}{2}} \tag{1.58}$$

2.0 ELECTRICALLY-INDUCED FORMATION OF HIGHLY-LOCALIZED BALLISTIC NANOSCALE LEAKAGE CHANNELS IN THE OXIDE LAYER OF A METAL-OXIDE-SEMICONDUCTOR (MOS) STRUCTURE

2.1 INTRODUCTION

Applying high electric field across a solid-state channel often incurs numerous conflicting situations with the required scattering-free transport through the medium. A ballistic transport of charge carriers in solid-state medium requires careful design of materials and structure such that it can provide maximum suppression of various scattering processes. Vacuum would serve as an ideal medium for high field ballistic transport of carriers without such complications. Vacuum electronics, however, has been perceived somehow less appealing than conventional solid-state electronics, and its full potential has not been thoroughly investigated.

In this chapter a beneficial aspect of nanoscale vacuum electronic structure was investigated in transporting electrons but actually operates in air ambient. The mean free collision path in air is ~50 nm. A device whose channel length is significantly smaller than this mean free path would essentially see the air ambient the same medium as vacuum. We have explored the possibility of achieving a new method of electrically-induced formation of highly-localized nanoscale leakage channels in the oxide layer of a metal-oxide-semiconductor (MOS) structure. Nanoscale void channels were formed in the oxide layer of a MOS structure by pulsed

operation in a breakdown regime (field strength ~ 10^8 V/cm) to initially forms localized leakage channels in the oxide layer. Electron transport through the channels is found to be ballistic (kinetic energy up to ~15 eV) with high current density (~10^8 A/cm^2). In the initial pre-breakdown stage, a direct or Fowler-Nordheim tunneling process is expected to be the dominant mechanism of carrier transport through the oxide layer. The latter process corresponds to the tunneling of electrons from the vicinity of the silicon side Fermi level through the triangular barrier in the forbidden band into the oxide conduction band. As more defects (vacancy defects) form over repeated application of an electrical pulse, the transport mechanism will eventually switch to a ballistic space-charge-limited current in the void channels. The performed I-V characteristic demonstrated the nanoscale void channels allow ballistic transport of electrons following the well-defined space-charge-limited current governed by the Child-Langmuir's law. The electron transport properties were analyzed assuming a simple two-dimensional model of the void channel. By solving the Poisson equation, the Coulombic repulsion of electrons limits the electrons injection into the channel. The space-charge-limited current varies proportional to the three halves power of the applied voltage and inversely to the square of the electrode distance, known as the Child–Langmuir law. Due to the well-established of oxide and interface properties of Si and highly reproducible, the nanochannel arrays demonstrated the reproducibility of nanochannel formation and the current scalability.

2.2 DIELECTRIC BREAKDOWN PROCESS

2.2.1 Introduction

Although SiO_2 has many extraordinary properties, it is possibly not perfect and can suffer from degradation caused by any stress factors, such as a high oxide field. Oxide degradation of MOS transistors, thus, has been the subject of numerous studies over the past decades since there is a strong correlation between the device degradation due to formation of interface traps and the substrate current known as time dependent dielectric breakdown (TDDB) appears to be a root of failure in the integrated circuit. Dielectric breakdown is a wear out phenomenon of SiO_2 as the stress across oxide of MOS, especially, in the thin insulating layer. The defects produced in the volume of the oxide film by driving force such as the applied voltage or the resulting of substrate tunneling electrons will accumulate with time and eventually reach a critical density known as charge to breakdown, triggering a sudden loss of dielectric properties. A surge of current produces a large localized rise in temperature, leading to permanent structural damage in the silicon oxide film [48, 49]. Unlike the traditional MOS operation, by using the benefit of metamorphism of on-purposely damaging oxide to create the nanochannel and operate in vertical direction, we report electrically-induced formation of highly-localized nanoscale leakage channels in the oxide layer of a metal-oxide-semiconductor (MOS) structure under pulsed drive allowing ballistic transport of injected electrons.

2.2.2 Charge-to-Breakdown and Trap Generation Process in Oxides

Charge to breakdown (QBD) is the process used to determine the quality and reliability of gate oxide in MOS device structure known as time dependent dielectric breakdown (TDBD) measurement. It demonstrates the total accumulated charge passing through the dielectric layer just before failure. The evolution of breakdown mechanisms have been investigated widely by both constant voltage stress (CVS) and constant current stress (CCS) method [52]. When a device is under stress either by voltage or current, charges are injected into the gate oxide by Fowler-Nordheim tunneling [52, 53] resulting in oxide damage such as traps, trapped charges or interface states. The breakdown process will occur as a result of the charges directly passing through the path formed by traps or trapped charges in the oxide. In addition, the major cause of the MOSFET degradation is the Si/SiO_2 interface state that generated when the injected charges passing through the oxide during stress.

For the breakdown phenomenon generated by constant-voltage stress CVS, This phenomenon could be attributed to the electrons trapped in oxide, the breakdown would occur when the stress induced traps form a path in the oxide, where the charges pass through. Because the electric field in oxide is high in the beginning of stress, the injection charges are very much inducing higher trapped charge generation rate, then, trapped charges quickly move to the front. When charges are trapped in oxide, they move forward due to the electrical field. The distributions of trapped charges are exponentially increased [52]. The breakdown occurs when the trapped charges move forward and reach charge to breakdown. Unlike CVS, when a device is stressed with CCS, the charges are injected into the oxide, and some of them are trapped in the oxide with a constant trapped charge generation rate. After stressing for a time, the charges are trapped to position, and they create some new traps by impact ionization [52]. The stress current

and trapped charge generation rate are all constant, resulting in a constant speed of tunneling front of trapped charge. When a trap reaches the other side and forms a path, the breakdown phenomenon would be occurred.

2.3 DEVICE REQUIREMENTS

Here, we demonstrate the device structure requirements for electrically-induced formation of highly-localized nanoscale leakage channels can be met in a silicon metal-oxide-semiconductor (MOS) structure under a breakdown regime operation with high voltage pulse (*i.e.,* with applied electric field greater than the oxide breakdown field) in order to induce nanochannel formation. A Si MOS structure is designed to have oxide thickness < 20 nm. In an ideal MOS capacitor structure, the amount of leakage current through the oxide layer is expected to be negligible. At sufficiently high electric field across oxide, however, charge carriers start to flow incurring physical breakdown of oxide. Once the total charges injected into oxide reach a 'charge-to-breakdown' level, a large leakage current develops. The breakdown process is known to involve hot electron (2-9 eV) injection and induces formation of leakage paths consisting of nanoscale defects [54-56]. The charge-to-breakdown is known to depend on oxide and interfacial quality as well as applied field. The oxide and interface properties of Si are well established and highly reproducible, and the material can serve as a model system in studying the high field operation.

2.3.1 Device fabrication

The MOS capacitor structure fabricated in this work is comprised of metal top electrode/ 10nm SiO_2/ p-type silicon. On top of a p-Si wafer [(100)-oriented; with 525±15 μm thickness, 1.32E15 cm^{-3} Boron doping concentration; 10±5 Ohm-cm resistivity], a 10 nm thick silicon oxide was thermally grown at 850 ˚C in oxygen ambient. The thickness of oxide layers was measured with a surface profiler (KLA/Tencor Alpha-Step IQ) on steps formed by lithography and etching. This oxide thickness (10 nm) determines the length of a void channel that will be formed in the oxide layer. Note that in order to achieve a ballistic transport in the channel region, the channel length must be smaller than the mean free collision path length. After the oxide layer growth, a broad-area Ohmic contact was prepared on the backside of the substrate by depositing a 150-nm-thick Al (Alfa Aesar, 5N purity) followed by annealing at 350 ˚C in N_2 ambient. Finally, one sample set will be deposited by an array of Ag or Al (10-15 nm thickness; 0.73 mm diameter) as a top electrode via thermal evaporation method (Fig 9). These typical MOS devices were serving as general purpose of MOS measurement such as capacitance and atomic luminescence [57]. Another sample set was mainly utilized in the main chapter by introducing nanochannels and nanochannels array that will be discussed in the following section.

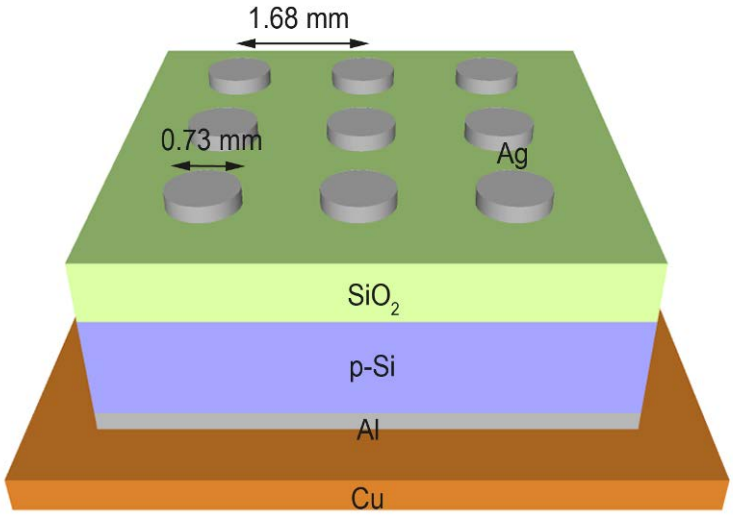


Figure 9 The typical MOS capacitor structure serving as general purpose of MOS measurement such as capacitance and atomic luminescence

2.3.2 MOS capacitor fabrication process flow

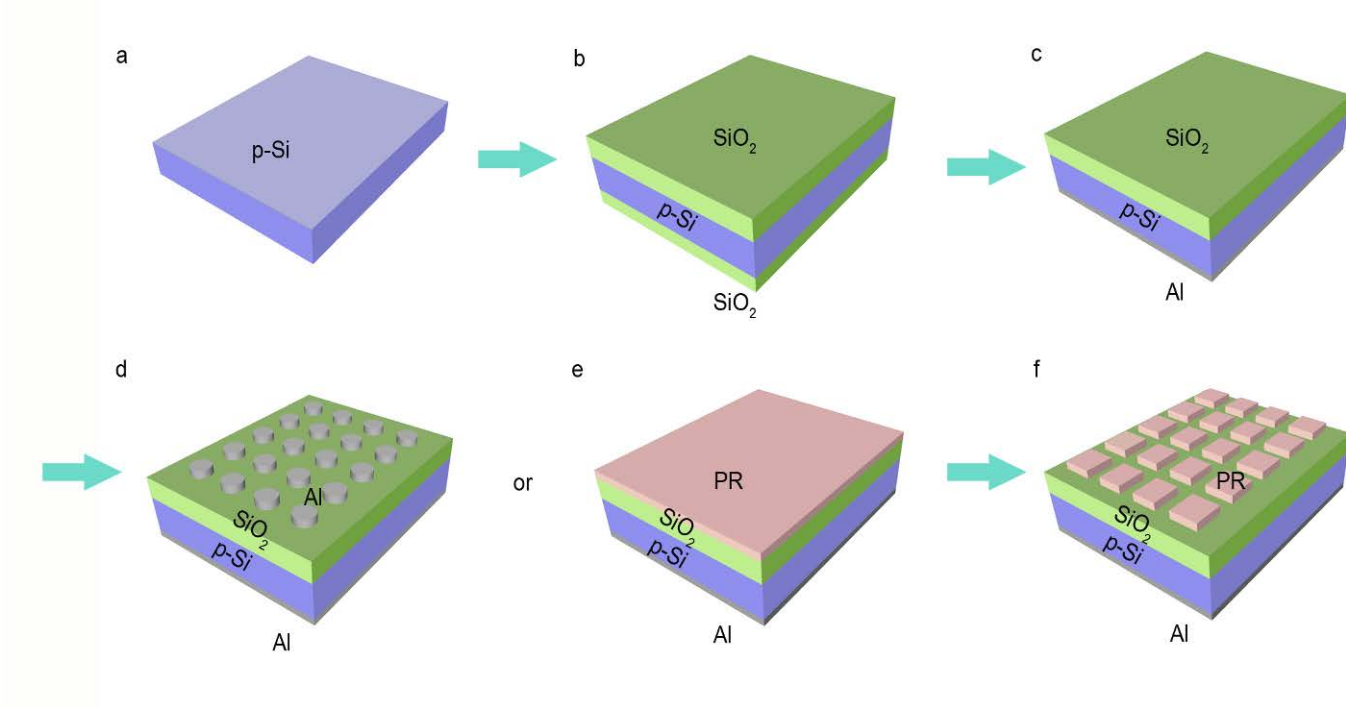


Figure 10 The MOS capacitor fabrication process flow: (a) p-Si substrate (1E15 cm^{-3}) after RCA cleanning, (b) 10 nm silicon dioxide dry oxidation grown on p-Si, (c) Al deposited on back side electrode forming ohmic contact, (d) Top electrode deposited as top electrode forming MOS capacitor for basic experiment, (e) and (f) patterned photoresist for ballistic transport experiment (photo-resist was patterned to located the position of probe tip(gate electrode) where the nanochannel formation was expected to form under tip location

2.3.3 Wafer cleaning process

The silicon wafers were initially cleaned by RCA cleaning process (Fig 10a). The RCA cleaning has two steps, one for removal of organic contamination and the other for removal of ionic contaminants (Fig 11).

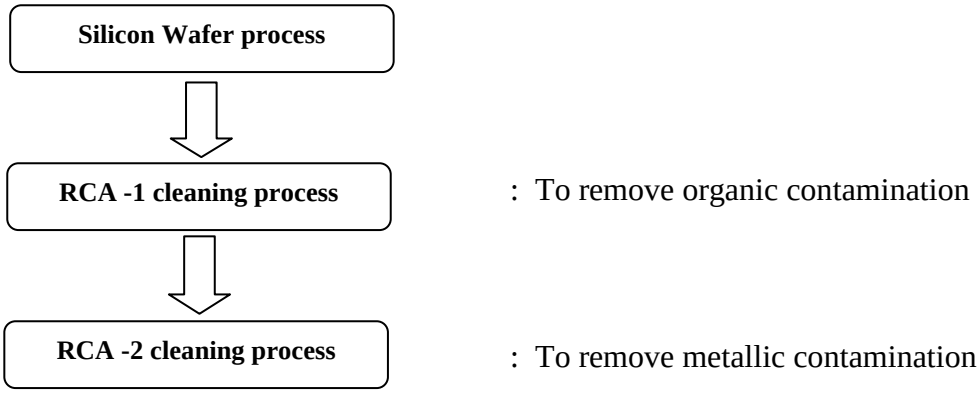


Figure 11 The RCA cleaning process diagram

The wafers were first prepared by soaking them into de-ionized (DI) water, then in trichloroethylene (TCE) for 5 min. After that, samples were cleaned in two solvents in sequence by ultrasonication: acetone for 5 min, methanol for 5 min and then rinsed in DI water. Subsequenly, specimens were etched in a 1:1:5 ratio (volume) solution of NH_4OH (ammonium hydroxide), H_2O_2 (hydrogen peroxide) and H_2O (water) for 10 min. This process is known to produce thin oxide (~10 Angstrom thickness) on the silicon surface. Subsequently, samples were treated with a 1:1:6 solutions of $HCl + H_2O_2 + H_2O$ in order to remove any residual contaminants

along with the oxide layer. Finally the wafers were rinsed in DI water and then blow-dried with nitrogen.

2.3.4 Oxidation process

To form an oxide with target thickness of ~10 nm (Fig 10b), an oxide growth was performed by using a thermal oxidation furnace (Thermo MB-71). Oxidation at 850 °C for 16 min in air produced 10-nm-thick SiO_2. The oxide thickness was measured by employing both surface profiler (alpha step) and C-V measurements.

2.3.5 Bottom electrode for Ohmic contact

The backside of silicon wafer was deposited with a 150 nm thick Al by thermal evaporation. Before Al deposition, the grown oxide on the backside was removed by BHF (H_2O: HF = 4:1) etchant, while the SiO_2 on the front side was protected by a photoresist layer. After Al layer deposition, the front side protective photoresist layer was removed. Then, the specimen was annealed in a furnace at 350 ºC for 30 min in N_2 ambient to form ohmic contact (Fig. 10c).

To verify Ohmic contact formation, contact resistance was measured from aluminum dots (0.73 mm diameter; 1.68 mm spacing between dots) deposited on top surface of silicon wafer. After annealing, I-V characteristic was measured for varying distances between dots. Contact resistance was calculated by transfer length method (TLM). Formation of Ohmic contact between Al and Si was confirmed.

2.3.6 Top electrode deposition

Top electrodes (Ag or Al) were prepared by performing thermal evaporation in conjunction with use of a shadow mask (0.73 mm-diameter holes and 1.68 mm center-to-center spacing between dots) (Fig 12). The deposition chamber was vacuum-pumped down below $1x10^{-5}$ Torr level. Applying high current (150 ~ 200 A) through the tungsten boat, the source material inside the boat was heated above the melting point of the metal source. The metal was deposited at the deposition rate of 3~4 Å/sec.

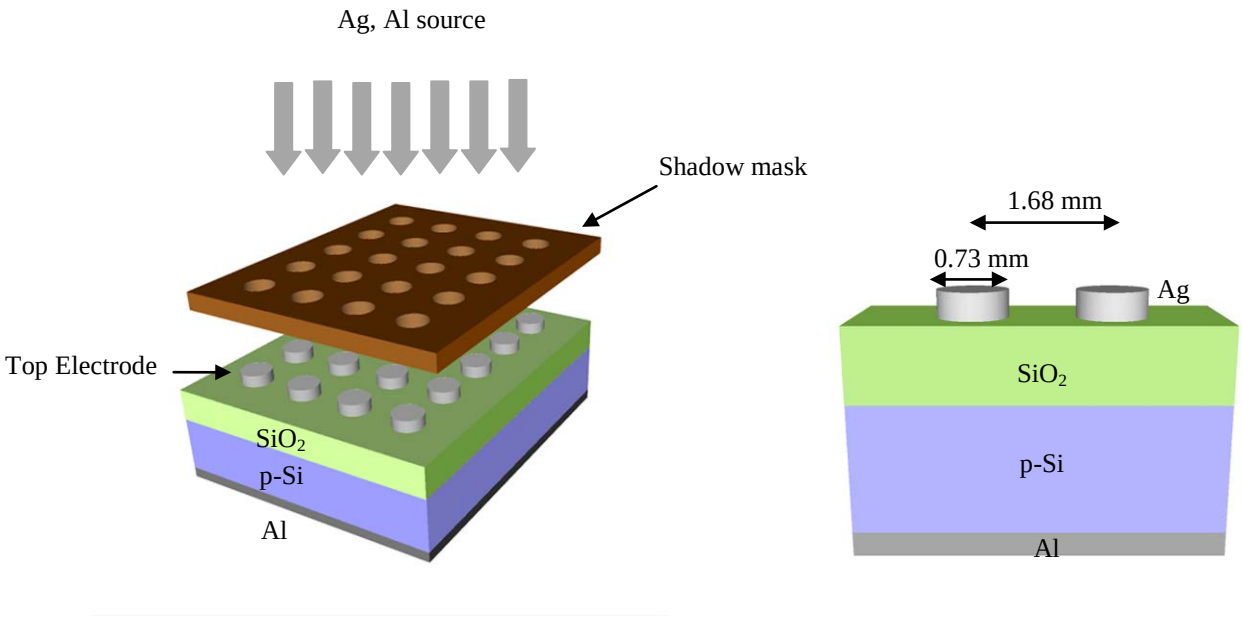


Figure 12 (a) Top electrode deposition by thermal evaporation, (b) Cross-section of MOS capacitor

While the relatively large area electrode (0.73 mm diameter) MOS samples well-served the purpose of some basic property measurement, another set of sample structure/configuration was employed for nanochannel formation and transport measurement (Fig. 10f). A sharp-tip (~1 micron radius of tip part) tungsten probe was placed on top of the oxide surface as describing in the following sessions. This configuration basically forms a MOS structure with the top electrode being tungsten and the dimension being in micron order, much smaller than the millimeter-size shadow mask electrodes.

2.4 NANOCHANNEL

2.4.1 Nanochannel formation and characterization

In order to induce the hard breakdown phenomena confined in the designated spot/area, a sharp-tip tungsten probe (1 μm radius tip size) was utilized as a top electrode for applying high pulse voltage [pulse generator (HP214B)] and this allows us to confine the electrical characterization within small area. Photoresist was patterned as shown in figure 10f to locate the position of tip where the nanochannel formation was expected to form under probe tip. Positive voltage pulses (25-100 V amplitude and 0.01 - 10 ms pulse width) were applied to the gate electrode (tungsten probe), driving the MOS to form an inversion channel (electron channel) in the Si substrate. The pulse amplitude was set such that the electric field in the gate oxide is to be significantly higher than the oxide breakdown field strength: for example, the electric field in oxide at 100 V is ~$1x10^8$ V/cm and this is significantly greater than the oxide breakdown field strength, 10^7 V/cm [40, 58]. The result is that MOS is suddenly driven to form an inversion layer in the silicon

substrate and electrons can be injected into oxide. This process is expected to form current paths or leakage channels in oxide. Without moving the probe the specimen was characterized by semiconductor parameter analyzer (HP4145B) for current-versus-voltage (*I*-*V*) characteristic (Fig 13).

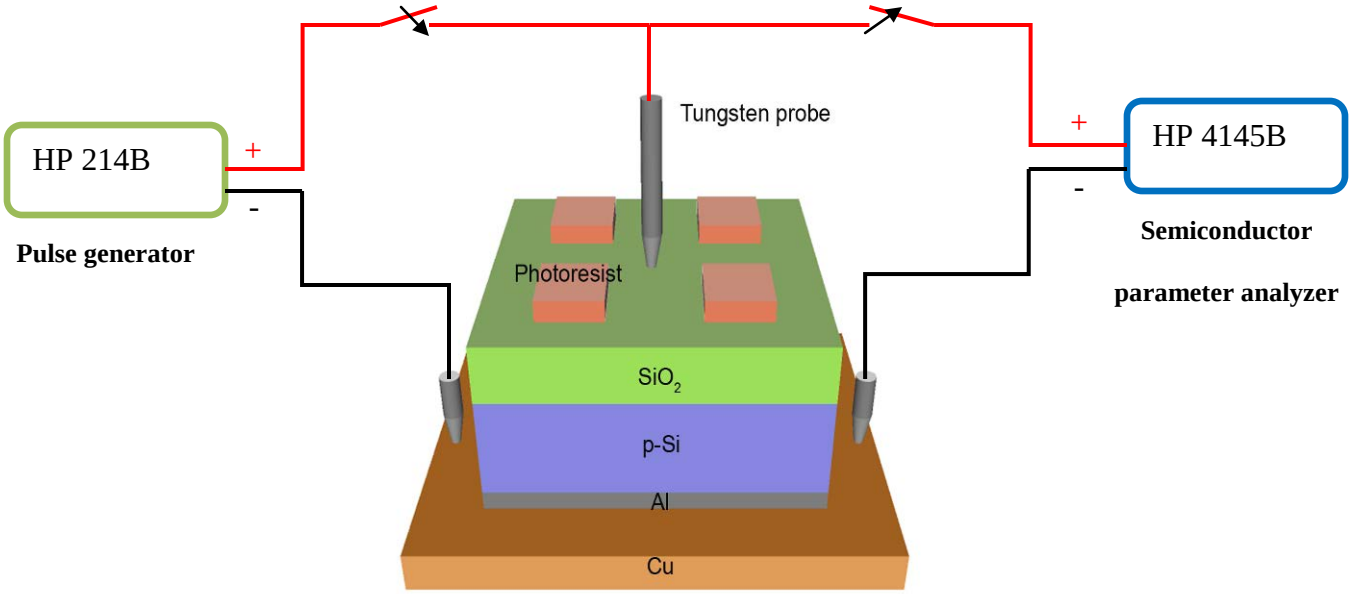


Figure 13 Nanochannel formation by high voltage pulse and characterization: a tungsten probe is connected to either semiconductor parameter analyzer (HP4145B) or pulse generator (HP214B). A sharp-tip tungsten probe (1 μm radius tip size) is used as electrode to create nano-void channels in the oxide layer of a MOS.

2.4.2 Result and discussion

Fig. 14 shows the evolution of current-versus-voltage (*I-V*) characteristic of the MOS structure over repeated application of a pulse (50 V amplitude and 1 ms width): the *I-V* characteristic of leakage current was measured before and after pulse application. The leakage current on a fresh sample (before pulse drive) shows tunneling-limited current at ~10^{-10} A (Fowler-Nordheim or direct tunneling) [35, 37]. The leakage current jumps up to ~10^{-6} A level after the pulse. This indicates some local conduction paths formed between cathode and anode (Fig 14b) [36, 38]. However, the local conduction path is not stable and the relatively high conductance state cannot be maintained if the applied pulse is not of enough strength. The switching between the low and high conductivity states can be interpreted as opening or closure of conduction channels between the electrodes [39].

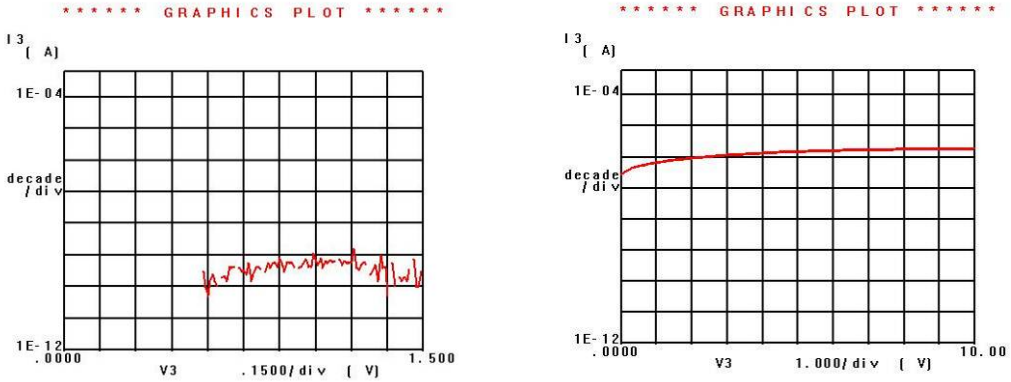


Figure 14 Nanochannel I-V characteristics: (lef) Before applying a pulse (right) After applying a pulse

2.5 BALLISTIC TRANSPORT IN NANOVOID CHANNELS

A ballistic transport is expected when a charge carrier drifts under electric field without involving a scattering process. In air ambient, the mean free collision path length is estimated to be ≈ 65 nm. For a device whose channel length is designed to be shorter than this mean free collision length, the carriers can travel to destination without collision. The ballistic transport current can then be the dominant mechanism of charge transport. This highly localized leakage channels formed in the oxide, which allow ballistic injection of kinetic electrons. This phenomenon has been conventionally explained by the Langmuir-Child's law using the theory of carrier transport mechanism in vacuum diodes model in which space charges build up near the anode side.

2.5.1 Experiment

In order to understand the mechanisms of current transport through the oxide layer that has experienced the high voltage pulses, the *I-V* characteristic of a Si MOS was examined for application of each high-voltage pulse (25 - 100 V amplitude and 1 – 10 ms width) (Fig 15). After application of a voltage pulse, the current level abruptly increased to the level of 10^{-6} A. Then, the current finally settled down at around the level of 10^{-3} - 10^{-4} A after several times of pulse application.

2.5.2 Result and discussion

Figure 15c shows a log-log scale I-V plot of a void channel created by a voltage pulse (50-75 V and 1 ms). The plot shows the three halves power relationship ($I \sim V^{3/2}$), known as the Child-Langmuir space-charge-limited current in a narrow gap between two parallel electrodes [45, 46]. This demonstrates collisionless transport of electrons through the leakage paths formed in the oxide layer and the leakage paths are basically void channels

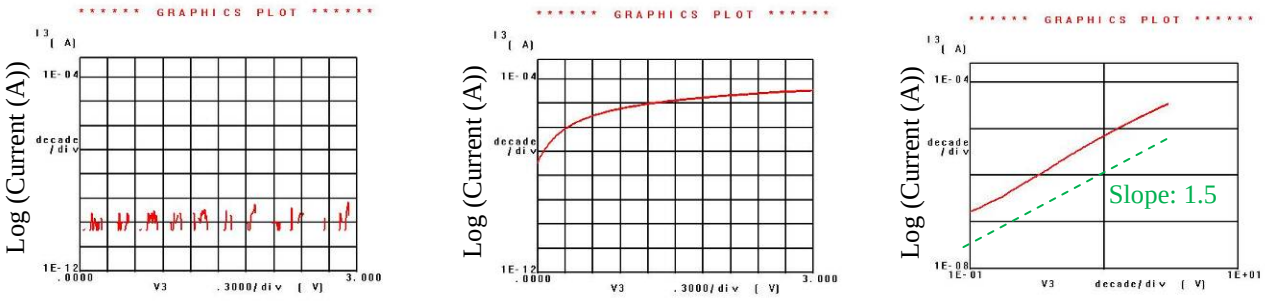


Figure 15 The evolution of nanochannel leakage current: (a) The leakage current of MOS before pulse application, (b) V (linear) – I (log) characteristic of a nano-void channel with upto 3V bias voltage, (c) The log-log scale plot of I-V shown in (b)

The space charge limited current is expressed as

$$J_{CL} = \frac{4\varepsilon_o}{9L^2}\sqrt{\frac{2q}{m}}V_o^{\frac{3}{2}}$$

with the following parameter values: ε_o = 8.854×10^{-12} F/m, m_e =9.31×10^{-31} kg, t_{ox} = 10 nm, q= 1.6×10^{-19} C

$$J_{CL} = \frac{4\varepsilon_o}{9t_{ox}^2}\sqrt{\frac{2e}{m_e}}V_o^{\frac{3}{2}} = (2.33E10)V_o^{\frac{3}{2}}$$

Assuming the channel length of 10 nm (same as the oxide thickness), the diameter of the nano-void channel is estimated to be 3-4 nm for the case of figure 16a. In the case of figure 16b the channel diameter is estimated to be ~28 nm.

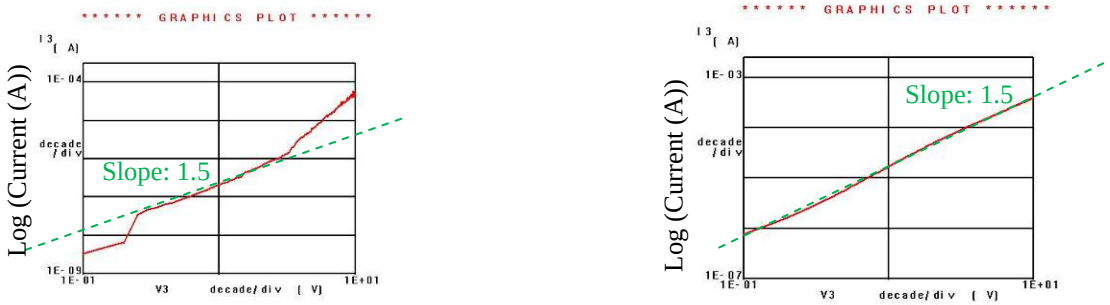


Figure 16 The log-log scale plot of I-V characteristic of a nano-void channel created by (a) 50 V, 1 ms pulse , or (b) 75 V, 1 ms pulse

The channel diameter varies, apparently depending on the pulse condition (total energy dissipation). This space-charge-limited current formula assumes ballistic transport of electrons across the gap with negligible barrier height for carrier injection. The monotonic increase of leakage current suggests formation of an increasing number of leakage channels, where the barrier height for electron injection at the SiO_2/Si interface is believed to be significantly reduced. This allows for injection and transport of a large amount of kinetic electrons through the channels. Additionally, a conductive atomic force microscopy (C-AFM) was employed to measure the leakage current distribution over the oxide surface. It can be concluded that one or two nanochannels formed within the probe contacted area as explained in previous chapter. Overall this measurement confirms the formation of nanoscale void channels in which electrons travel ballistically governed by the Child-Langmuir's law of space-charge-limited current flow. This transport is collisionless, therefore, electrons can be accelerated to a very high velocity inside the channel.

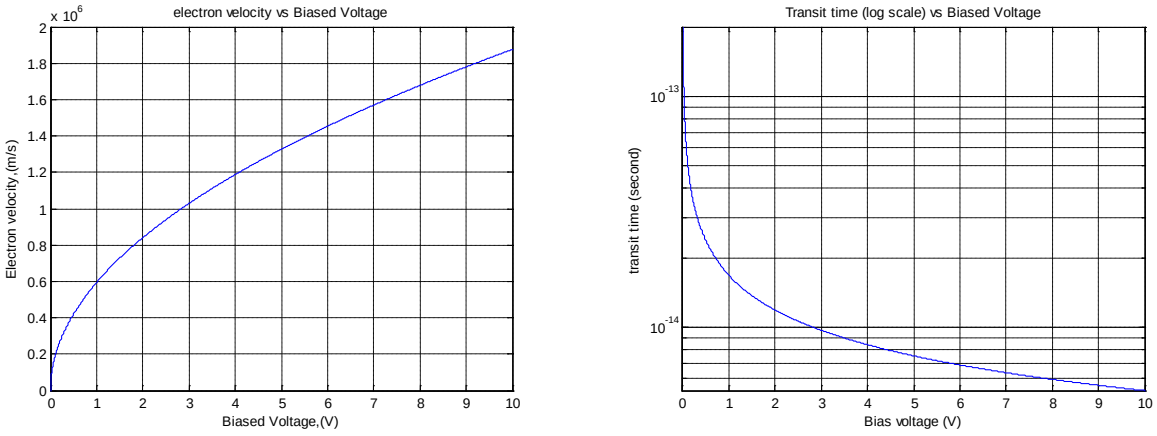
Terminal velocity of electron and transit time can be calculated as follows. From the conservation of energy,

$$\frac{1}{2}mv^2 = qV$$

$$v = \sqrt{\frac{2qV}{m}}$$

$$\tau = \frac{L}{v} = \frac{L}{\sqrt{\frac{2qV}{m}}} \ .$$

The electron velocity and transit time are plotted as a function of bias voltage (figure 17).



(a) (b)

Figure 17 (a) Electron velocity and (b) Transit time (log scale) as a function of bias voltage

2.5.3 Conclusion

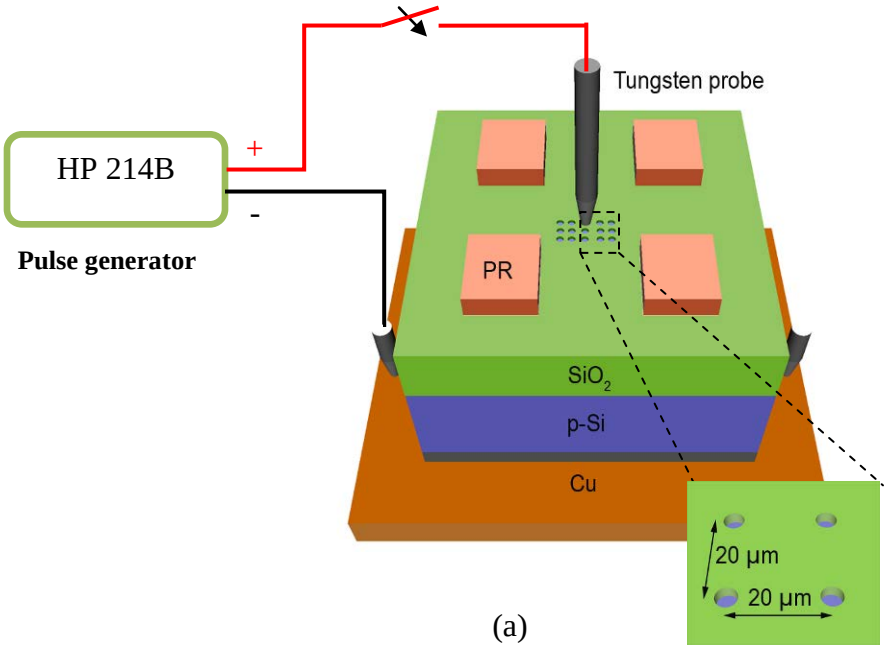
We extracted the effective channel diameter by assuming that the channel length is equal to the oxide thickness. In ballistic transport at nanoscale, electrons can reach very high drift velocity at low voltage and in short transit time. Thus-formed nanochannels are found to serve as a conduit for ballistic transport of electrons. Due to the high velocity, the resulting current density is also very high. This characteristic charge transport would be very useful in developing high-speed, low-power-consuming devices and circuits [44]. In the deep-down nanoscale regime (channel diameter and/or length < 2-3 nm), the quantum confinement and tunneling effects may become important. Note the de Broglie wavelength of a ballistic electron is ~0.5 nm at V = 1 V. In this regime the quantum effects need to be taken into account [41, 42]. With channel length or diameter > ~10 nm, the classical Child-Langmuir's law for nonrelativistic electron flow is considered to be valid. In the case of moderately-high field strength (10^7 V/cm) in 5 to 10 nm-thick SiO_2, the tail of energy distribution of electrons in the oxide is known to extend up to 7-8 eV (53, 54). In the case of leakage channels formed in oxide, the ballistic nature of electron transport appears to be significantly enhanced, enabling the attainment of high kinetic energy (up to ~16 eV) under the strong electric field (~10^8 V/cm). The exact nature of the nanochannels is not fully established yet and is a subject of research. The space-charge-limited current behavior with clear $V^{3/2}$ dependence suggests that the leakage channels are basically void channels formed by nanoscale percolation of vacancy defects in oxide.

2.6 NANOCHANNEL ARRAY

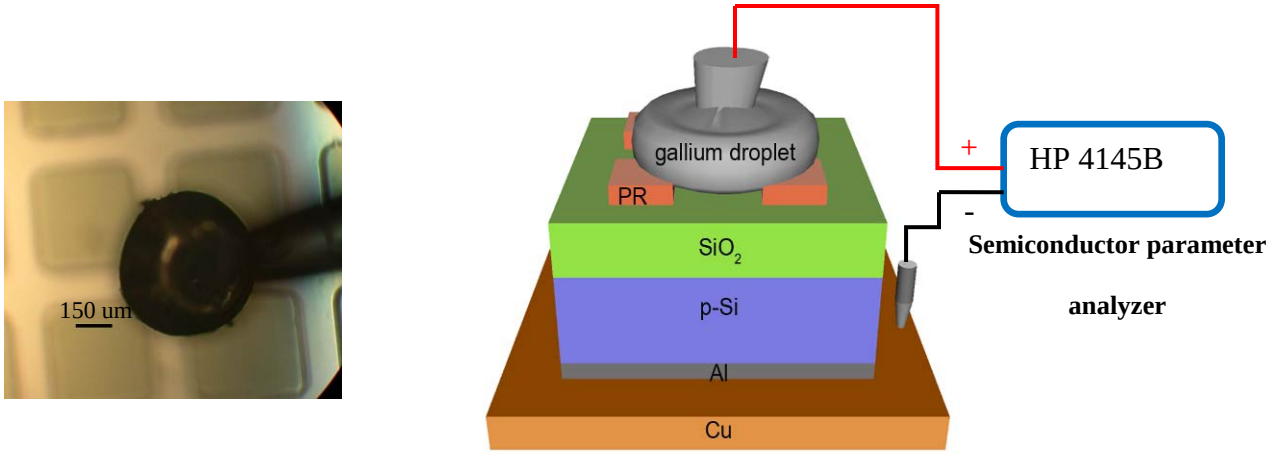
In the previous section we described the process and characteristic of the electrically-induced formation of highly-localized nanoscale void channels in the oxide layer of a metal-oxide-semiconductor (MOS) structure. The nano-void channels demonstrate a well-defined space-charge-limited current flow governed by the Child-Langmuir's law. In this chapter we further discuss the reproducibility and scalability of the current. Another experiment was performed on the same MOS structure with an array of nanochannels formed by use of a sharp-tip tungsten probe for voltage pulse application (Fig 18a). The thus-formed nanochannels were characterized by employing a liquid-gallium-drop-tipped tungsten probe. This gallium probe method is found to offer great flexibility in locating the array area and covering it with good physical contact. The 1, 4, 9 or 22 nanochannels array were formed and characterized for their electron transport properties**.**

2.6.1 Experiment

Gallium has a melting point at 303 K and it can be in the liquid phase at room temperature. When a gallium droplet attached to a probe is brought into contact with the oxide surface that contains locally defined nano-void channels, the gallium surface can serve as a top electrode for the nanochannels defined underneath (Fig. 18b).



(a)



(b)

Figure 18 Nanochannels array formation and characterization: (a) Electrical pulses (HP214B) are applied across the oxide by tungsten probe tip (1 um radius). (b) A gallium droplet utilized as a top electrode (left), I-V characterization by using gallium as a top electrode (right)

2.6.2 Result and discussion

Figure 19 shows I-V curves of four individual nanochannels formed on the same oxide layer under the same pulse condition. Some channels show clear $V^{3/2}$ dependence, whereas other channels show V^2 dependence. The latter one corresponds to the Mott-Gurney's space-charge-limited current. This V^2 law is for the case that the charge carriers experience collisions during transport and a constant mobility is assumed [43, 46]. The Mott-Gurney (MG) model can be expressed by

$$J_{MG} = \left(\frac{9\varepsilon}{8d^3\mu} \right) V^2$$

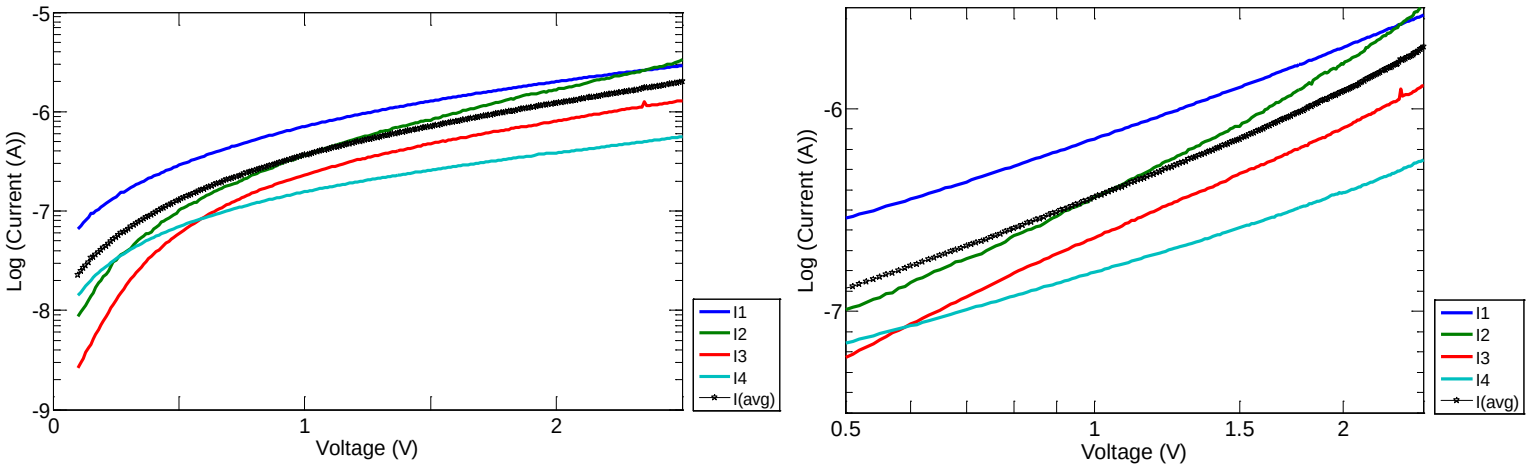


Figure 19 The space-charge-limited current through individual nanochannels formed in the oxide layer: (a) Log-linear scale plots of I-V characteristic (b) Log-log scale plots of I-V characteristic. The slope of 1.5 in the log-log scale plot indicates ballistic transport in the nanochannel.

Figure 19 reveals a statistical distribution of a single channel *I-V* characteristic. Although there is a certain degree of fluctuation observed, the average *I-V* characteristic (black line) well matches the Child-Langmuir's $V^{3/2}$ law. The different slope and current level indicate different degree of channel formation and dimension. A slope close to 1.5 indicates complete opening of the void channel, whereas a slope close to 2 would indicate a partially blocked leakage channel.

For the same slope value, a larger current at a given voltage would indicate effectively larger channel diameter. Figure 21 shows the evolution of nanochannel characteristic measured during I-V scan or after repeated application of voltage pulses. Sometimes a sudden jump-up of current level was observed during *I-V* scan. This is attributed to widening of the channel diameter or formation of additional formation or opening of channels. See figure 20a: in the voltage range (0.2 V-0.3 V) the I-V characteristic well matches the Child-Langmiur model with estimated channel diameter of 2 nm. At ~0.5 V, the current jumps up and the effective diameter is estimated to be 4 nm. Eventually, after repeated *I-V* scans, the nanochanel *I-V* characteristic becomes stable. This suggests that DC scan at medium voltage level can be employed as a refining process in nanochannel formation. In the very low voltage range (0 - 0.2 V), the *I-V* curve shows an ohmic behavior (Fig. 20b). This indicates that the space charges injected are less than thermal carriers that exist in the oxide adjacent to the channel region. For $V > 0.4$ V, the slope gradually increases to 1.5. The $V^{3/2}$ voltage-dependence is a characteristic of the Child-Langmuir space-charge-limited current in a narrow gap between two parallel electrodes [39, 40]. Assuming free-space permittivity for ε and free-space electron mass for m^*, the space-charge-limited current formula produces an injection current at $V = 1$ V and $d = 10$ nm the total effective size of nanochannel is around 3-4 nm.

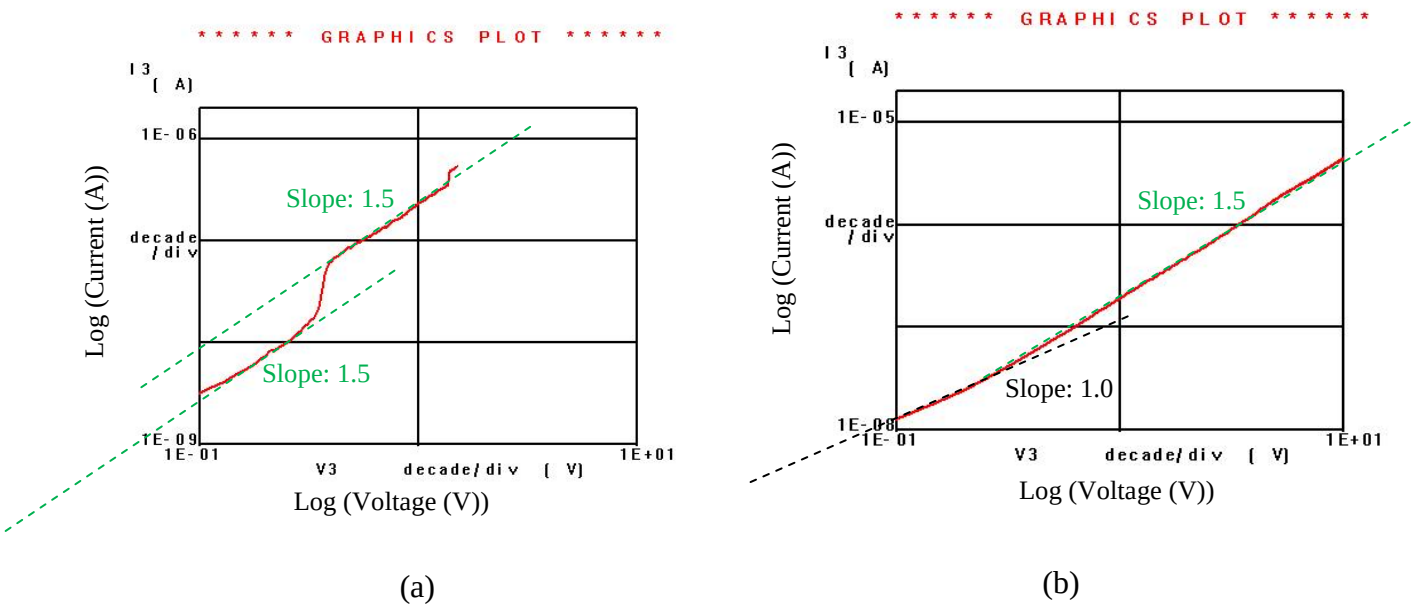
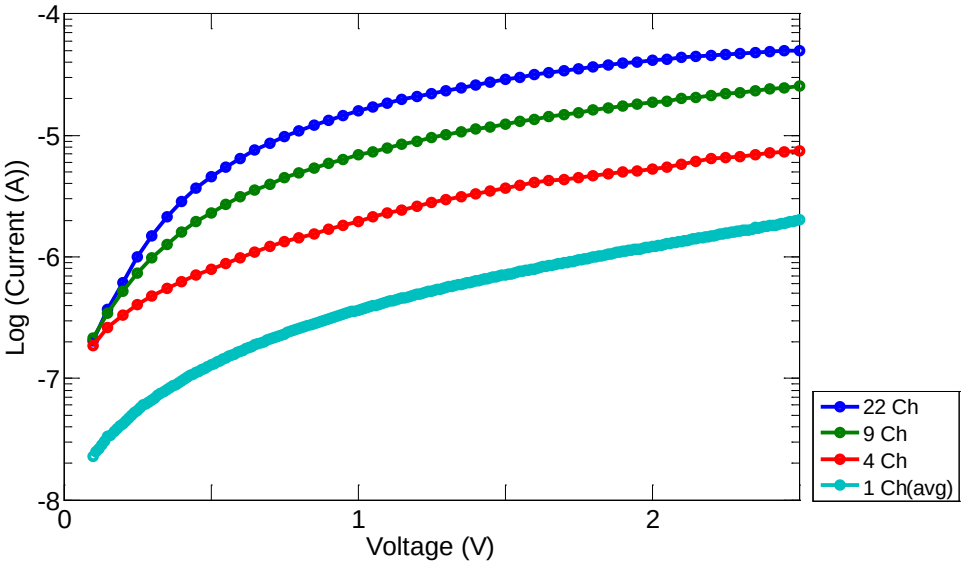
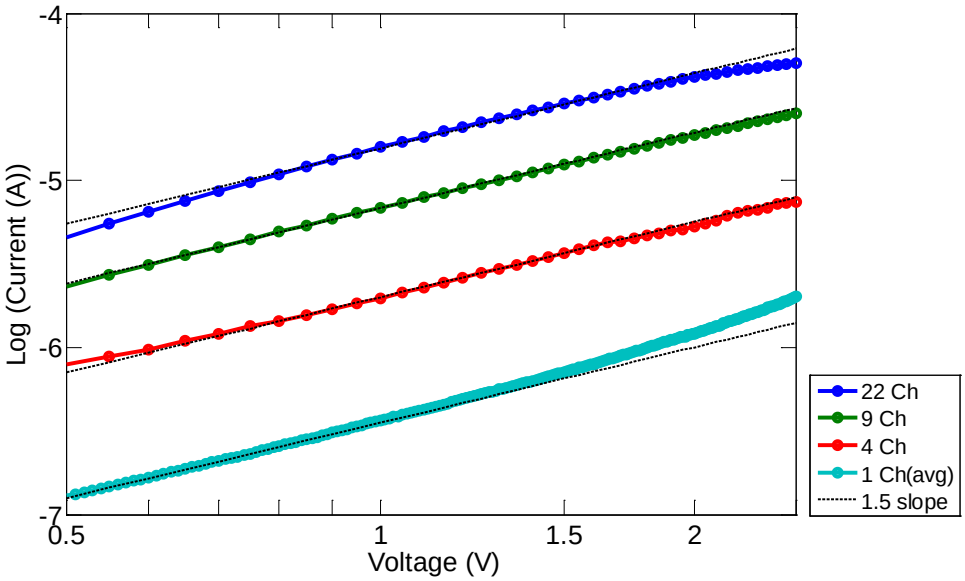


Figure 20 The evolution of nanochannel during DC voltage scan: (a) Log-log scale plots of I-V characteristic showing a step increase of current. (b) Log-Log scale of I-V characteristic showing a gradual change of slope from 1 to 1.5.

Nanochannel arrays comprising 1, 4, 9 or 22 channels were created on MOS structure with 20 micron channel spacing. The post breakdown *I-V* characteristic was measured by using a gallium-tipped probe as a top electrode for the nano-void channels. Fig 21 shows the Log-Linear scale of I-V and Log-log scale of I-V. The *I-V* curves show that in the voltage range 0.5-2.5 V, they fit well the Child-Langmuir model. At 1 V, the single channel current is 0.37 µA, 4 channels are 2 µA, 9 channels are 6.88 µA, and 22 channels are 15.81 µA. This demonstrates good scalability of current by channel number.



(a)



(b)

Figure 21 The space-charge-limited current through 22, 9, 4 and 1 nanochannel arrays formed in the oxide layer: (a) Log-linear scale plots of I-V characteristic, (b) Log-log scale plots of *I-V*

A space-charge-limited current flow is demonstrated through nano-void channels formed in the oxide layer of a MOS structure. In the one dimensional free space medium, the current transport in the collisionless regime can be described by the Child-Langmuir's law. On the other hand, if the collision becomes significant in carrier transport, the corresponding SCL current can be described by the Mott-Gurney's law. Although nanochannels initially show an evolutionary characteristic, i.e., fluctuation of current level and/or transition between different transport mechanisms (CL, MG or Ohmic), very stable and reproducible CL characteristic can be achieved by repeating I-V scan at intermediate voltage level.

3.0 A NANOSCALE VOID CHANNEL FORMED BY FOCUSED ION BEAM (FIB) ETCHING IN A SI METAL-OXIDE-SEMICONDUCTOR STRUCTURE

3.1 INTRODUCTION

The metal-oxide-semiconductor (MOS) capacitor structure forms the backbone of modern silicon electronics [1]. The enabling nature of MOS structure stems from the fact that an electron (or hole) channel can be induced and modulated at the Si/SiO_2 interface by applying proper voltage to the capacitor. The charge carriers in the channel region, whether in inversion or accumulation regime, usually form a quasi-two-dimensional (2D) system that is narrowly confined (~2 nm width) in a potential well developed in Si [3,4]. Besides the potential well in Si, the metal side also develops band bending, harboring charges of opposite polarity in confined space (< 1 nm) across the oxide layer [5, 6].

Now consider a MOS capacitor structure whose lateral extent is finite, e.g., terminated by cleaved edges. An interesting situation can develop with the two dimensional electron system (2DES) induced in the capacitor: electrons near the edge would experience Coulombic repulsion (to the in-plane lateral direction) from accumulated charges, and this may significantly reduce the barrier height for emission into air side [7, 9]. A 2DES is a system of charged fermions interacting with a Coulombic potential, to which a uniform background is commonly added for charge neutrality [3, 10]. Coulombic interactions become dominant over the kinetic energy in the

low density regime. However, the Coulomb energy in a neutral 2DES with electron density of 10^{11}- 10^{12} cm^{-2} is typically on the order 10 meV, not sufficient to make a significant change of emission barrier. In the case that the charge neutrality is maintained by relatively remote charges (*e.g.,* opposite polarity charges induced across the oxide layer of MOS capacitor), strong Coulombic repulsion is expected in the local area around the edge of 2DES, and this can significantly alter the electrostatic potential there. In this study, we have investigated emission and transport properties of electrons from the edges of MOS capacitor under various bias conditions and explored the potential to develop low-voltage, high emission-current density, nanoscale vacuum electronic devices.

3.2 FABRICATION OF A SILICON MOS CAPACITOR STRUCTURE WITH A VERTICAL NANO-VOID CHANNEL

Nanoscale void-channels were fabricated by performing focused-ion-beam (FIB) etching of a Si MOS structure [20-nm Al / 23-nm SiO2 / p- (or n-) Si substrate] (Fig. 22a). Square wells (0.5x0.5 μm^2, 1x1 μm^2, and 2x2 μm^2) were etched to 1 μm or 2 μm depth. In this vertically-etched well structure, the channel length between anode and cathode was precisely determined by the oxide layer thickness, and was designed to be smaller than the mean free path of air (~60 nm).

3.2.1 Fabrication process flow of Si MOS capacitor structure with a nanoscale void channel

A metal-oxide-semiconductor (MOS) capacitor structure was formed by growing a 23 nm thick thermal oxide layer on p-type Si (B-doped, 10 Ω-cm resistivity) or n-type Si (P-doped, 5 Ω-cm resistivity) wafers [(100)-oriented; 525 μm thickness]. The bottom electrode was prepared by depositing a 150-nm-thick Al layer (5N purity) by thermal evaporation, followed by Ohmic contact annealing at 350 ^{o}C (Fig 22a). A stripe pattern of Al electrode (20 nm thickness; 40-60 μm width; 1 mm length) was prepared on top of the oxide layer by thermal evaporation in conjunction with a photolithography and lift-off process (Fig. 22b, c). After formation of the conventional MOS capacitor structure, the MOS wafers were further processed to develop nanoscale void vertical channels by employing a focused-ion-beam (FIB)-etching technique (Fig. 22d) or a mechanical cleaving method. The FIB etching process was performed with Seiko Dual Beam System (SMI-3050SE). A Ga ion beam (30 keV; 94 pA) was used with 0.5 μs dwell time in creating square wells (cross-section: 0.5x0.5 μm^2, 1x1 μm^2, or 2x2 μm^2; etch depth: 1μm or 2 μm) in Si MOS wafers.

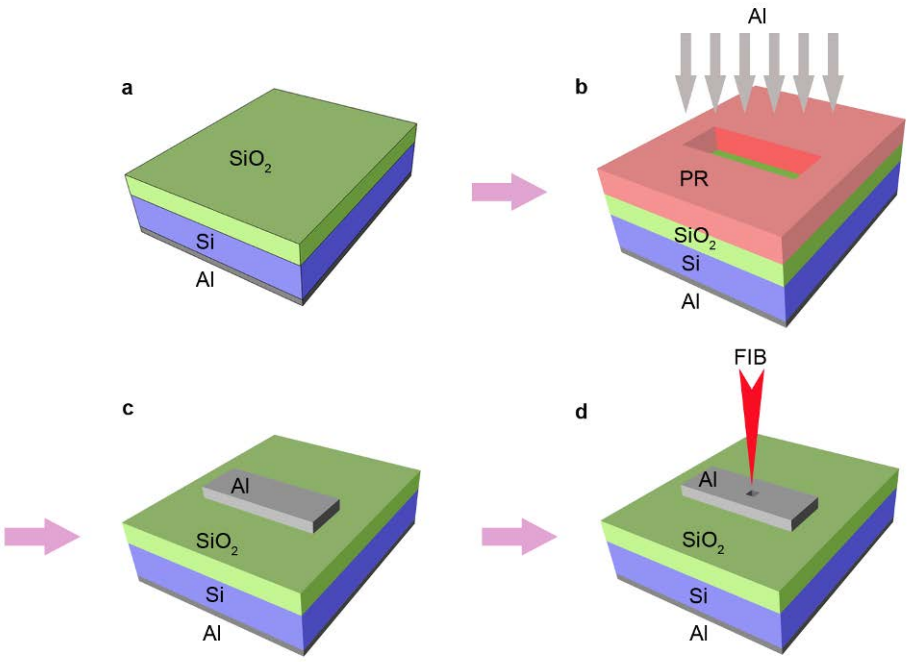


Figure 22 The fabrication process flow of a Si MOS capacitor with a nanoscale void vertical channel

3.3 TWO TERMINAL CHARACTERIZATION OF NANOSCALE VOID-CHANNEL

3.3.1 Two terminal I-V characteristic of FIB-etched nanoscale void-channel

The channel transport properties were characterized by measuring the current-versus-voltage (I-V) characteristics (Fig. 23). The two-terminal *I-V* characteristics show a rectifying behavior with a forward slope of ~1.5 and a reverse slope of 0.5-1.0 in the log-log scale plots (Fig. 23c to e). In the p-Si (n-MOS) case, the channel reveals a forward characteristic when the Al gate is negatively biased. This implies that electron emission from the metal side is more efficient than from the Si side at the same bias voltage of opposite polarity. With a 0.5x0.5x1.0 μm^3 well-formed on p-Si, for example, a channel current of 43 nA is observed at +1 V bias, whereas 6 nA is obtained at -1 V bias (Fig. 23c). Comparison of the three different well-size samples (perimeter of 2, 4, or 8 μm) reveals that the channel current is proportional to the perimeter of well, not to the area of well. This result suggests that electron emission occurs at the edge surface (periphery) on the vertical sidewalls of a well. The samples with different etch depth (1 or 2 μm) show the same level of current (Fig. 23d), a result consistent with that the channel length is effectively determined by the oxide layer thickness. In the n-Si (p-MOS) case, a forward characteristic is observed when the substrate is negatively biased, implying that electron emission from Si is more efficient than the other way, e.g., 60 nA at +1 V versus 3 nA at -1 V for the 0.5x0.5x1.0 μm^3 well sample (Fig. 23e).

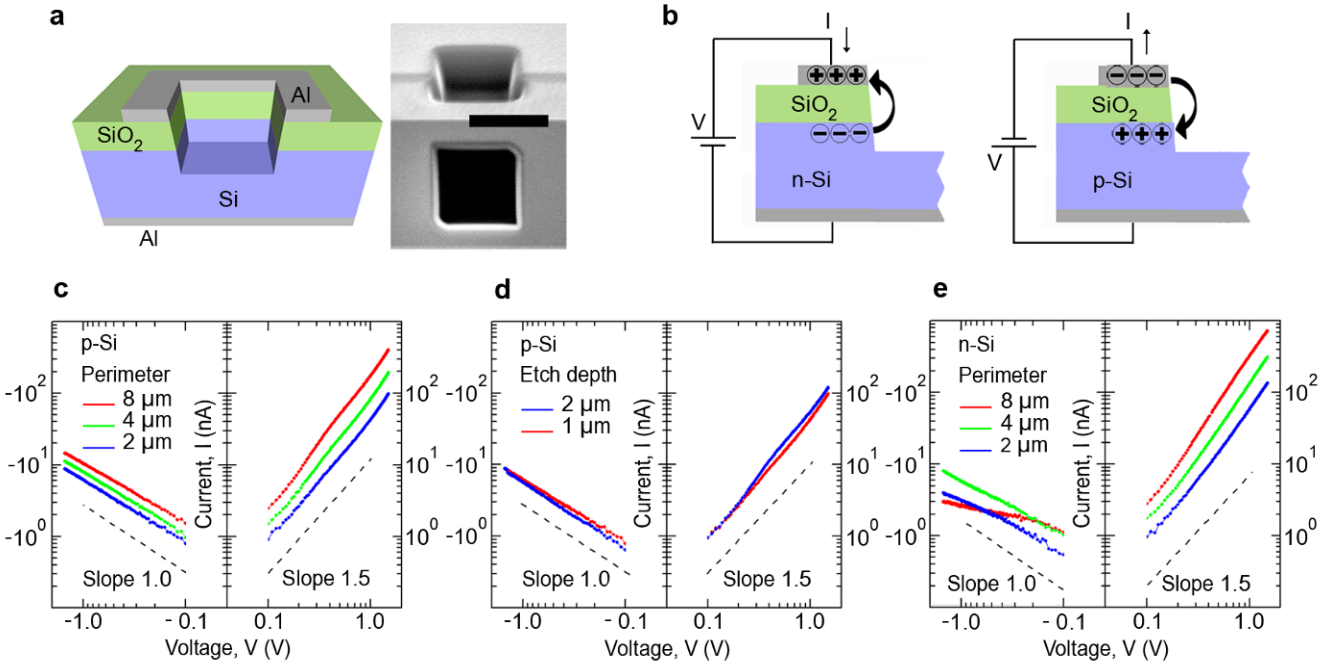


Figure 23 Ballistic transport of electrons in nano-void channels in Si MOS. (a) Schematic drawing of a nano-void channel fabricated by focused-ion-beam etching (left). SEM images of a square well (1x1 μm2) etched to 1 μm depth (right). Scale bar, 1 μm. (b) Schematics of electron emission and transport in nano-void channels: n-Si (left) and p-Si (right) substrate samples under forward bias. Note electron emission from the edge of 2DES formed in cathode (Si: left; Al: right). (c) to (e), Measured I-V characteristics of nano-void channels: (c), square wells (with perimeter of 2, 4, or 8 μm) formed on p-Si; (d) a 2-μm-perimeter well formed on p-Si with different etch depths (1 or 2 μm). (e), Square wells (with perimeter of 2, 4, or 8 μm) formed on n-Si; the dashed lines indicate the slope of 1.5 (forward) or 1.0 (reverse).

The forward characteristic with a slope of 1.5, that is, the $V^{3/2}$ voltage-dependence corresponds to the Child-Langmuir's space-charge-limited (SCL) current flow in vacuum [11, 12]:

$$J = \frac{4\varepsilon_o}{9L^2}\sqrt{\frac{2q}{m}}V_o^{\frac{3}{2}} \tag{3.1}$$

Where the permittivity of gap medium, m* is the effective mass of electron, d is the gap size, and V is the applied voltage. [Note that this 1D version of Child-Langmuir law is applicable to a planar gap, where the current scales with electrode area. When the current injection is confined to an edge-shaped area, that is, the current scales with the perimeter, the gap dependence of SCL current is changed to ~(1/d): $J \sim V^{3/2}/d$] [1, 13]. This space-charge-limited current flow assumes a scattering-free ballistic transport of electrons across the gap with a negligible barrier height for carrier injection.

3.3.2 I-V characteristic of nanoscale void vertical channel prepared by cleaving a MOS capacitor structure

In order to make sure that the observed $V^{3/2}$ dependence is from the electron transport through the air (nanoscale vacuum), not from a surface conduction that might be enabled by possible etch residue or deposit on oxide surface, the same vertical channel structure was fabricated by cleaving a MOS wafer. The cleaved samples clearly demonstrate the same rectifying *I-V* characteristic (forward slope of 1.5 and reverse slope of ~1) as the FIB samples (Fig. 24). The leakage current through the oxide layer was also characterized by performing I-V measurement

prior to FIB etching. The oxide leakage was measured to be ~20 pA at 2 V bias, far smaller than the channel current level described above.

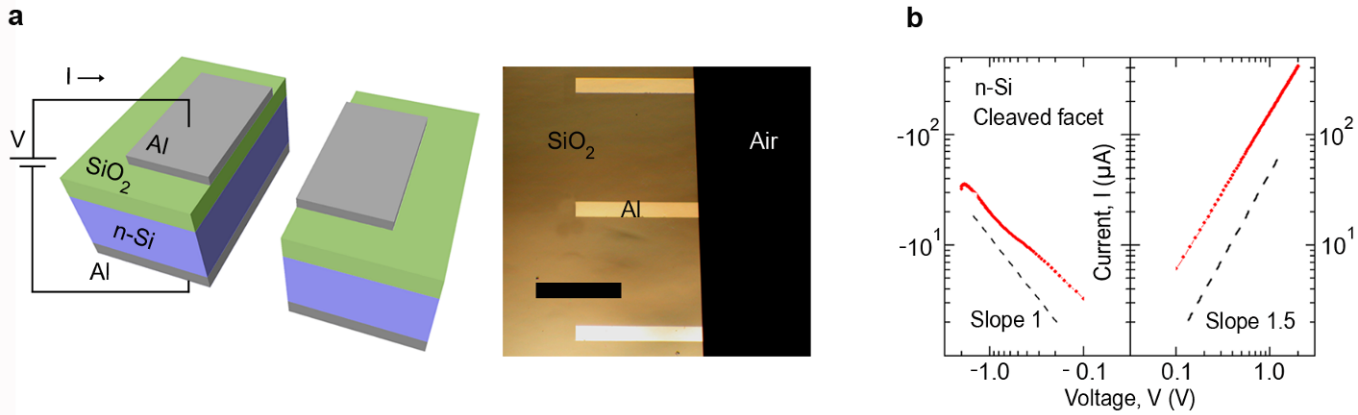


Figure 24 Vertical channel structure was fabricated by cleaving a MOS wafer (a) A schematic of a nanoscale void vertical channel prepared by cleaving a MOS capacitor structure. An Al electrode pad (stripe) was first deposited on an oxidized Si substrate. The MOS wafer was then mechanically cleaved into two pieces with each cleaved facet comprising cross-sections of MOS layers (left). An optical micrograph of a top view of a cleaved sample containing three stripes of Al electrode (right: scale bar, 300 μm). The capacitor area is defined by the top electrode (a rectangular stripe with 40 μm width). (b) I-V characteristic of a nano-void vertical that was developed on the cleaved facet of a MOS capacitor formed in n-Si substrate. The cleaved samples clearly demonstrate the same rectifying I-V characteristic (forward slope of 1.5 and reverse slope of 0.5-1.0) as the FIB samples (Fig. 23e).

3.4 RESULT AND DISCUSSION

Fig. 25 shows the energy band diagrams of MOS structures under forward bias of 1 V. In the n-Si case, the flat band voltage is -0.32 V, and the MOS is accumulation biased by the amount of 1.32 V (Fig. 25d). The electron accumulation in Si is estimated to be $1x10^{12}$ cm^{-2} at this bias voltage and the same amount of charges of opposite polarity are expected to be induced in the metal side across the oxide layer (see Fig. 25). The accumulation electrons form a 2DES, and this layer serves as a reservoir of electrons that would be readily available for emission through the edge under forward bias. From the charge neutrality point of view, approximately 74 % of the total accumulation electrons in Si are balanced by adjacent polarization charges induced at the Si/SiO_2 interface. This implies the 'net' accumulation electrons that are balanced by 'remote' charges across the oxide layer account for 26 % of total accumulation, which corresponds to the ratio, $\varepsilon_o / \varepsilon_{SiO_2}$. The mean spacing of electrons in this 'net' charged 2DES is given as $2(\pi n)^{-1/2}$, and is estimated to be ~20 nm, comparable to the separation of 2D systems of opposite charges, that is, the oxide layer thickness (23 nm). The Coulomb potential around the edge is then expected to be significantly altered, enabling virtually barrierless emission of electrons into air, thereby the Child-Langmuir's space-charge-limited current flow in the nano-void channel.

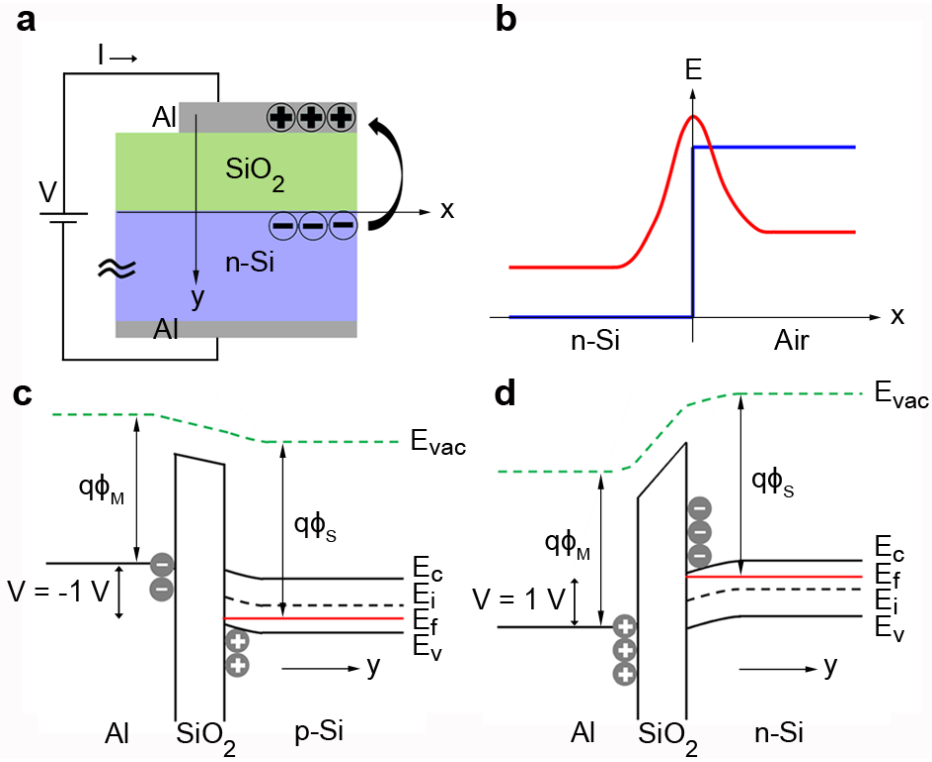


Figure 25 Energy band diagrams of nano-void channel during forward bias. (a) 2D electron or hole systems induced across the oxide layer. (b) Schematic illustration of electron potential (red) and energy barrier (blue) profiles on the plane of the 2DES layer at the Si/SiO2 interface. (c) A schematic drawing of energy band diagram of p-Si sample at 1 V forward bias. (d) A schematic drawing of energy band diagram of n-Si sample at 1 V forward bias. The 2DES induced in cathode (Al for p-Si; Si for n-Si substrate) serves as a reservoir of electrons that are readily available for emission through the edge under forward bias.

In the p-Si case, the flat band voltage is -0.90 V, and the MOS at 1-V forward bias is accumulation biased by the amount of 0.10 V (Fig. 25c). The hole accumulation in Si is estimated to be $5x10^{10}$ cm^{-2}, and the same amount of electrons are induced in the metal side. 26 % of the accumulation electrons are balanced by remote holes, and the mean spacing of electrons in the net charged 2DES is estimated to be ~100 nm. This 2DES in metal serves as a reservoir of electrons for emission under forward bias. Field penetration into metal is less than that in Si, and the 2DES in metal is more narrowly confined (< 1 nm) than that in Si (2-3 nm). Electrons are injected into air from the cathode (Al) edges with negligible barrier height. The overall voltage dependence of anode current is then governed by the channel transport properties, which demonstrates the Child-Langmuir's $V^{3/2}$ dependence (Fig. 23c, d). In reverse bias, part of the bias voltage goes to depletion region formation in Si, therefore the void-channel section receives less voltage than the accumulation case. This explains the reduced slope (0.5–1.0) in reverse bias. In the n-Si case, the forward bias (slope of 1.5) corresponds to the case of electron emission from the accumulation layer formed in Si, and the top metal gate serves as an anode. In reverse bias, part of the voltage goes to the depletion region in Si, and the *I-V* characteristic demonstrates a reduced slope (0.5-1.0), similar to the p- Si case (Fig. 23e).

3.5 CHARGE DENSITY CALCULATION

In a MOS capacitor structure, the space charge density in the semiconductor side can be determined by solving the Poisson equation, and is expressed as follows for the case of n-MOS [40]:

$$\left|Q_s\right| = \varepsilon_s E_s = \frac{\sqrt{2}\varepsilon_s}{\beta L_D}\left[(e^{-\beta\varphi_s} + \beta\varphi_s - 1) + \frac{n_{po}}{p_{po}}(e^{-\beta\varphi_s} - \beta\varphi_s - 1)\right]^{1/2} \tag{3.2}$$

where ε_s is the permittivity of semiconductor, and E_s is the electric field at the interface with the oxide layer. φ_s is the band bending at the semiconductor/oxide interface, called the surface potential. $\beta = q/kT$, and L_D is the extrinsic Debye length for holes, given as. n_{po} and p_{po} are the equilibrium densities of electrons and holes, respectively. The applied capacitor voltage (V) appears across mainly three places (neglecting the band bending in the metal side): across the band bending region in semiconductor (φ_s), across the oxide layer (V_{ox}), and the flat band voltage (V_{FB}).

$$V = \varphi_s + V_{ox} + V_{FB} \tag{3.3}$$

The voltage drop across the oxide layer (V_{ox}) is related to the space charge (Q_s) and oxide capacitance ($C_{ox} = \varepsilon_{ox}/ d$) as follows.

$$V_{ox} = Q_s/C_{ox} \tag{3.4}$$

Solving the above equations (3.1)-(3.3) simultaneously, the space charge density *Qs* can be calculated as a function of applied voltage *V*. Fig. 26 shows *Qs* for *V* in the range of 0 to -1.5 V for a Si n-MOS with $N_A = 1.32\times10^{15}$ cm^{-2}. At *V* = -1 V, the MOS is in the accumulation regime, and the space charge (hole) density is calculated to be $5x10^{10}$ cm^{-2}. At this bias voltage, the surface potential φ_s is -0.05 V and the voltage drop across the oxide layer V_{ox} is -0.05 V. Fig. 27 shows the case of a Si p-MOS with $N_D = 1.0\times10^{15}$ cm^{-2}. At V = 1 V, the MOS is in the accumulation regime, and the space charge density is calculated to be $1x10^{12}$ cm^{-2}. The same amount of electrons is accumulated in the metal side. At this bias voltage, the surface potential φ_s is 0.21 V and the voltage drop across the oxide layer V_{ox} is 1.11 V. In this calculation, the following numbers were assumed: the work function of Al, 4.1 eV; electron affinity of Si, 4.15 eV; electron affinity of SiO_2, 0.95 eV; dielectric constant of SiO_2, 3.9; dielectric constant of Si, 11.8 [61].

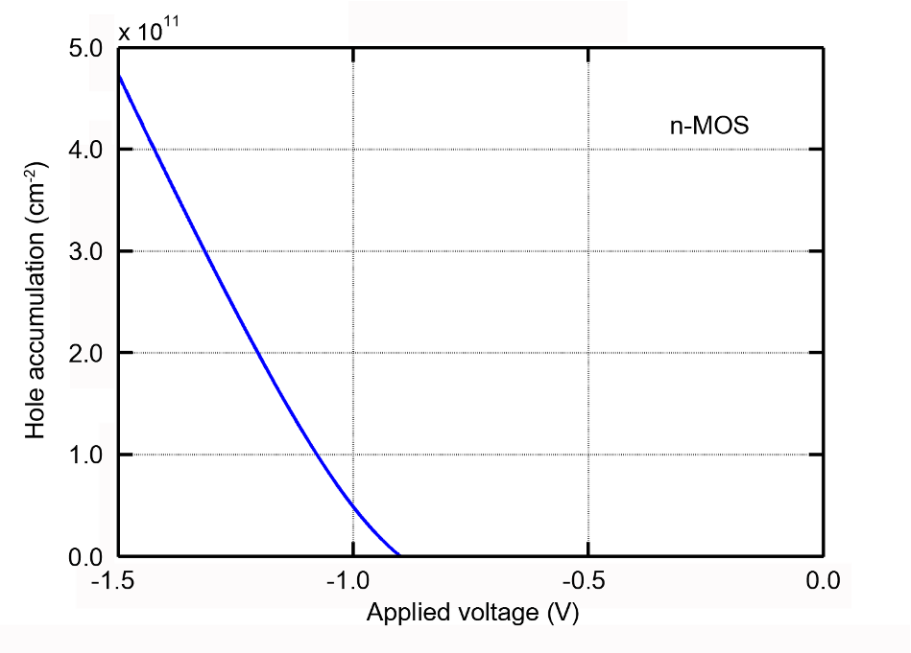


Figure 26 Hole accumulation as a function of applied voltage for p-Si (n- MOS)

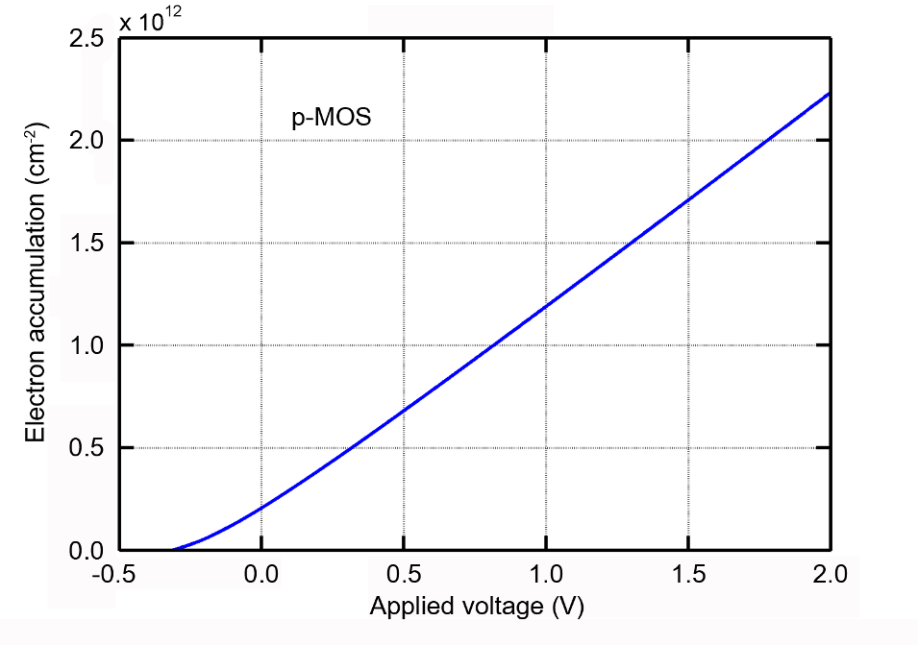


Figure 27 Electron accumulation as a function of applied voltage for n-Si (p- MOS)

3.6 ELECTRON CAPTURE EFFICIENCY EXPERIMENT

In the nano-void channel structure, electrons emitted from the cathode edges are expected to travel along the wall side and arrive at the open-ended anode with a ballistic speed. Considering this channel/electrode configuration and geometry, all electrons emitted from the cathode might not be collected by the anode, and the measured current may represent a small fraction of total emission. In order to estimate the collection efficiency, the total electron emission from cathode was measured for a 0.5x0.5x1 μm^3 well sample formed on n-Si substrate (Fig. 28). The channel aperture (Al electrode with a square opening) was covered with a Ga droplet electrode so that all emitted electrons be captured without loss (the work function of Ga is 4.3 eV, close to Al's 4.1 eV). Thus- measured channel current is found to be two orders of magnitude greater than that without a cover (i.e., 12 μA versus 60 nA at +1 V forward bias). This implies that ~0.5 % of emitted electrons are collected at the anode in open-aperture configuration, or stated equivalently that the total emission current is 12 μA at +1 V bias.

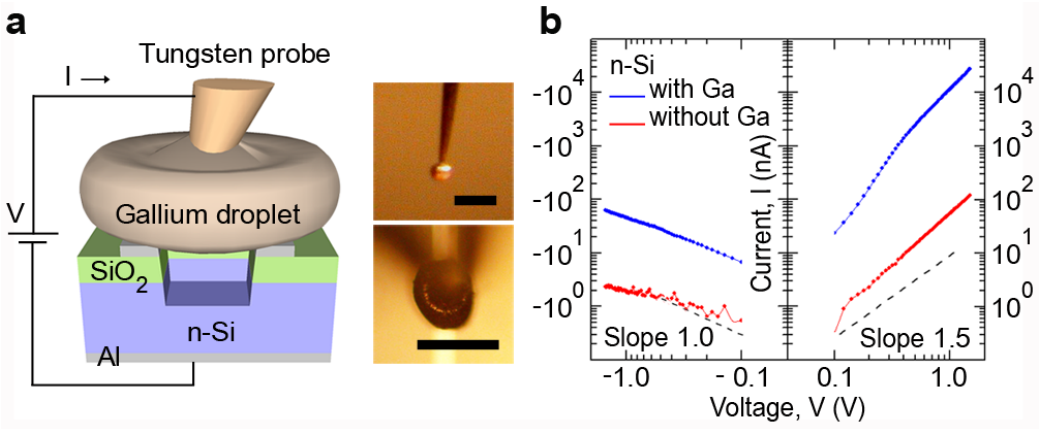


Figure 28 Measurement of electron capture efficiency at the top anode edges of a nanovoid-channel sample formed on n-Si substrate. (a) (left) Schematic drawing of channel top (Al electrode with a square opening) covered with a Ga droplet electrode, (right) Optical micrograph of a Ga droplet pressed by a tungsten probe. Scale bar, 400 μm (top) and 200 μm (bottom). (b) The channel current measured with and without a Ga cover: a 0.5x0.5x1 μm2 well sample formed on n-Si substrate. Thus-measured channel current is found to be two orders of magnitude greater than that without a cover.

Assuming uniform injection of electrons from the cathode emission area [perimeter (2 μm) x thickness of 2DES layer (~1 nm, in Si)] and referring to the 1D version of Child-Langmuir law as an approximate guide, the SCL current density is estimated to be on the order of 10^5 A/cm^2 at low bias voltage (~1 V). This channel current density is orders of magnitude greater than those of conventional emission models [14-17]. Various geometries of cold cathode for enhanced emission have been reported in literature [18, 19], including the one with vertically stacked metal films separated by insulating layers, similar to the work described in the present study. In most cases of previous work, however, detailed designs of their electrode geometry and configuration are different in that external applied field is to have significant strength of normal component on cathode surface, unlike the case of the vertical structure reported in the present work, where external field has zero normal component at the emitter surface (vertical sidewall). The resulting *I-V* characteristics of conventional structures consistently demonstrate Fowler-Nordheim (*FN*), not SCL.

3.7 TESTING OF AGING AND ENDURANCE OF CATHODE EMISSION

Native oxide forms on metals and Si surfaces in air, and it has been reported that oxide formation on cathode surface significantly reduces the emission current [23, 24]. In order to test the effect of native oxide formation, the I-V characteristics of the void-channel diode structure were measured after 10 months of time lapse (in air ambient) and the result was compared with those measured right after fabrication (first measurement usually performed within 24 hours after FIB etching). The forward current of a p-Si substrate sample (cathode, Al) reveals a small decrease (23 % at 1.5 V) after 10 months, whereas the n-Si substrate sample (cathode, n-Si) shows a slight increase (20 % at 1.5 V) over the same period (Fig. 29).

Although the amount of change is relatively small, the different behavior of Al and Si cathodes may be associated with the beneficial role of oxide formation in passivating the surface states on Si. Detailed mechanisms are unclear at this point and are a subject of further study. The vertical void-channel structures tested in this study did not show any instability problem, such as the one associated with ‘forming process’ in conventional cold cathodes [19]. The endurance of the cathode emission process in the diode structures (both n-Si and p-Si substrate samples) was also tested by performing repeated scans (anode-cathode voltage of -1.5 to +1.5 V; scan time, 15 s). No measurable change in *I-V* characteristics was observed after 1200 scans (total 5 hours of continuous scanning) (Fig. 30).

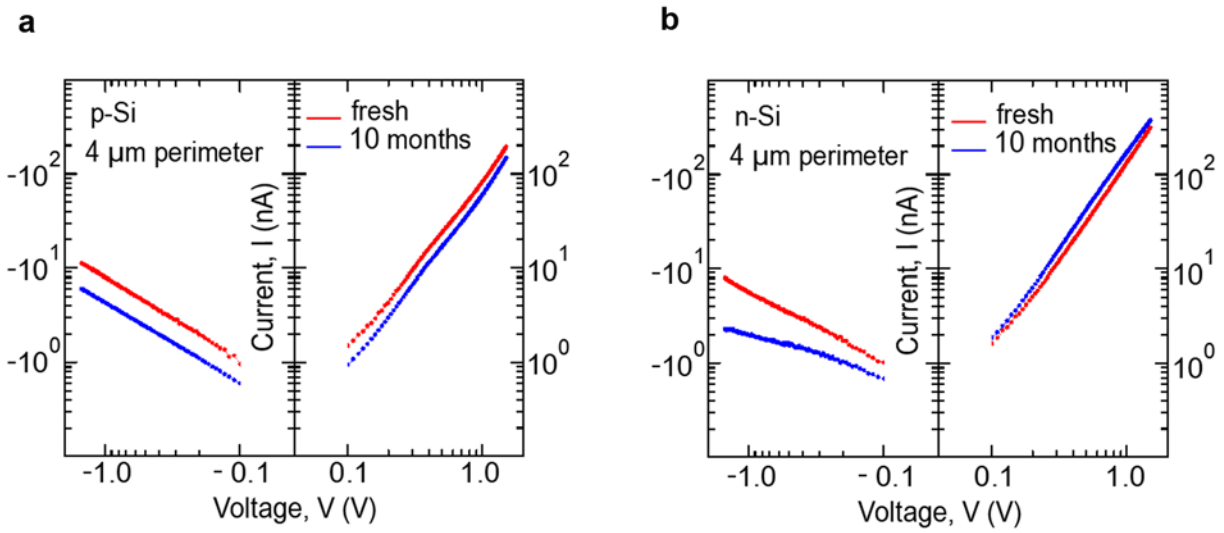


Figure 29 The I-V characteristics of diode structure measured before and after 10 months of time lapse in air ambient.

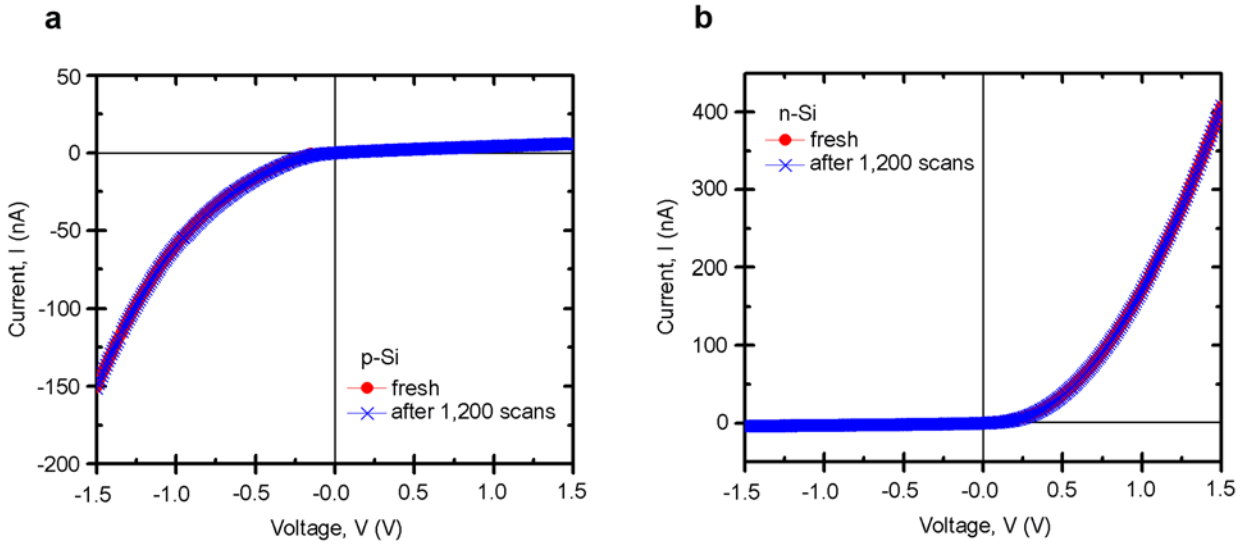


Figure 30 The I-V characteristics of diode structure measured before and after 1200 continuous scans (total 5 hours of scan time)

3.8 CONCLUSION

The electron flow through a metal-nanogap structure usually involves a two-step process: field emission from metal surface, commonly described by the Fowler-Nordheim theory, and subsequent transport through the gap, governed by the Child-Langmuir's space-charge-limited current flow. The Child-Langmuir law assumes zero field (normal component) at cathode surface, whereas the FN emission requires a surface normal field of significant strength (typically ~10 V/nm order for metals with work function of 4-5 eV) in order to enable tunneling emission through the potential barrier at cathode. As more electrons are injected into the gap, the space charge field builds up reducing the field on cathode surface, thereby decreasing the Fowler- Nordheim emission. The overall current flow at steady state is then a balancing act of the two processes, being usually governed by the field emission in a low voltage range and by the space charge effect at higher voltages [20-22].

In the present work, the SCL regime begins to appear at very low voltage (~0.5 V), whereas the FN regime is absent in the voltage range tested (< 2 V). This observation is consistent with the earlier reports that the barrier height for electrons at cathode edges is very low [7-9]. In the 2DES with net accumulation charges, electron emission from cathode edges is virtually thresholdless, enabling very low voltage operation (similar to the negative electron affinity effect) of channel transport with high current density. Similarly, electrons approaching the anode edges will experience Coulombic attraction from the 2D hole system formed there, and this will help capturing electrons into the anode.

4.0 METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR WITH A VACUUM CHANNEL

4.1 INTRODUCTION

Based on the promising two-terminal characteristics, we further developed the nanochannel structure into a nanoscale vacuum field-effect-transistor (FET) device. A thin layer of indium-tin oxide (ITO) was introduced into the MOS capacitor structure as a gate electrode, overall forming a vertically-stacked 5-layer structure: 20-nm Al / 30- nm SiO_2 / 20-nm ITO / 23-nm SiO_2 / p-Si substrate (Fig. 33a, b). Nano-void-channels of square cross-section (0.5x0.5 μm^2, 1x1 μm^2, and 2x2 μm^2) were formed by FIB etching of the stacked layers. Here the ITO gate layer is designed to control formation of an electron inversion layer in the p-Si substrate [21-25]. A band bending occurs at zero bias, and an inversion layer readily develops in p-Si even at low gate voltage (Fig. 33c). In the ITO layer, no significant band bending occurs that can help capture of electrons into the gate layer. In conventional field-effect transistors, the gate voltage controls the transport process via modulating the channel conductance. Similarly in vacuum tubes, the grid voltage modulates the electron transport to anode. By contrast the nano-void-channel FET described in the present work directly modulates electron emission by use of an ITO gate in MOS capacitor structure. With use of an electron inversion layer induced in cathode (p-Si) as an emission source, a normally OFF mode of operation (i.e., enhancement mode FET) is possible.

4.2 NANOSCALE VACUUM FIELD-EFFECT TRANSISTOR (FET) FABRICATION

A nano-void-channel FET structure was fabricated on p-Si substrate [B-doped, 10 Ω-cm resistivity; (100)-oriented; 525 μm thickness]. First a 23-nm-thick SiO2 layer was grown by thermal oxidation (Fig. 31a). After Ohmic contact metallization (150-nm-thick Al) on the bottom side, a 20-nm-thick indium-tin-oxide (ITO) layer was deposited on top of the thermal oxide layer on the front side. The ITO layer was deposited by radio frequency (RF) magnetron sputtering of an ITO target (In_2O_3/SnO_2, 90/10 wt %; 4N purity; Kurt J. Lesker) in Ar ambient gas without intentional heating of substrate. Subsequently, a stripe pattern (40-60 μm width; 2-3 mm length) of ITO was developed by performing photolithography and chemical etching (1 HCl + 5 H_2O). This ITO electrode serves as a gate of the FET device (Fig. 31b, c). A 30-nm-thick SiO_2 layer was blanket deposited on top of the ITO by RF sputtering of a SiO_2 target in Ar ambient without substrate heating (Fig. 31d). Finally, on top of the sputter-deposited silicon oxide, a 20-nm-thick Al top electrode (60 μm width; 1 mm length) was deposited by thermal evaporation and a lift-off process (Fig. 31e, f). The Al stripe was aligned perpendicular to the ITO stripe. Overall the vertically-stacked layer structure at the cross is comprised of: 20-nm Al / 30-nm SiO_2 / 20-nm ITO / 23-nm SiO2 / p-Si substrate. Here the Al Ohmic contact on p-Si substrate serves as a source (cathode) electrode and the top Al electrode as a drain (anode). Finally, a nano-void-channel was formed in the cross area by performing FIB etching (Ga ion beam: 30 keV; 94 pA; 0.5-μs dwell time) of a square well. The square well was etched to 2 μm depth. The channel length of this FET is determined by the spacing between the top Al electrode (anode) and p-Si substrate (cathode), which is 73 nm in this particular design.

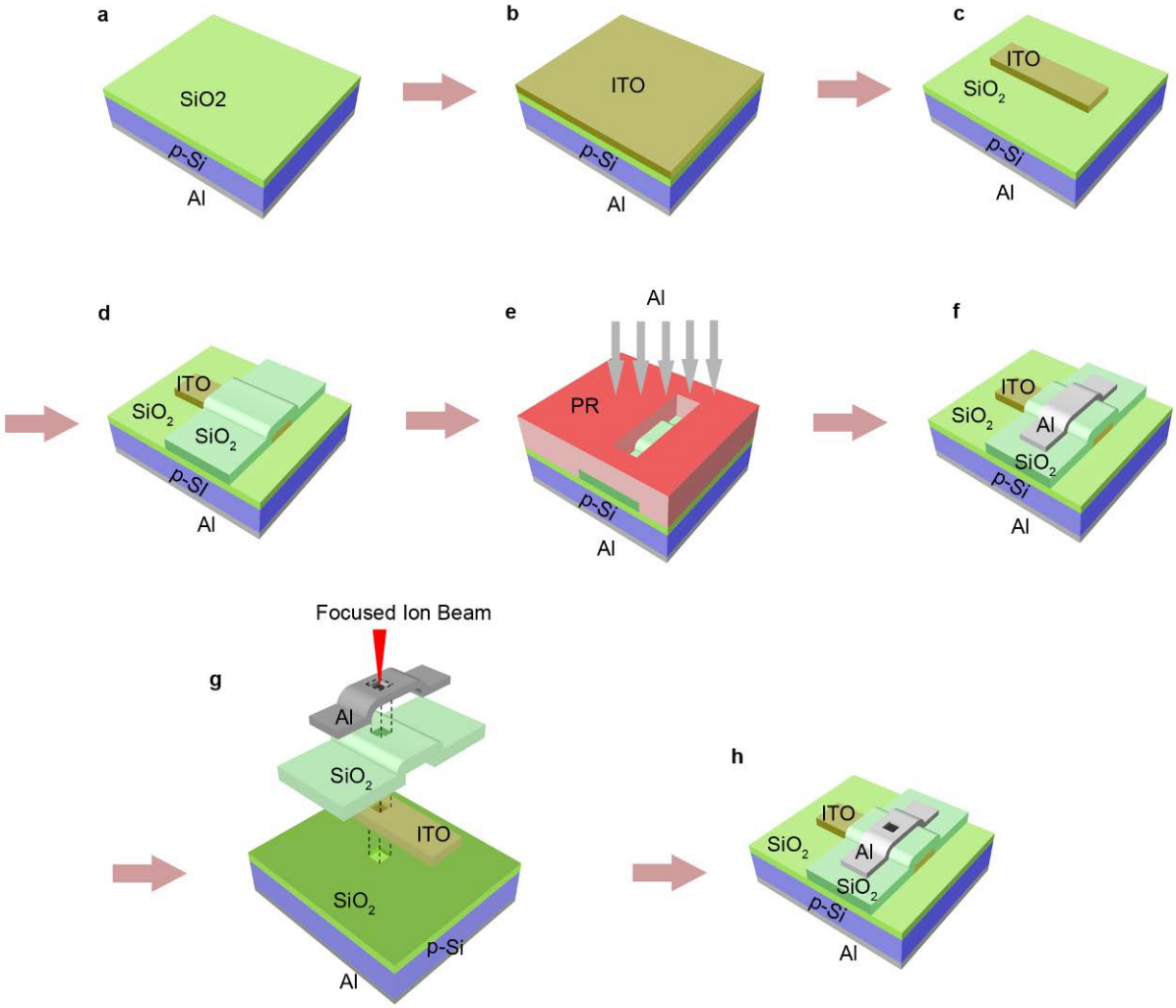


Figure 31 The fabrication process flow of nanoscale void channel FET in Si MOS

4.3 CHARACTERIZATION OF NANOSCALE VOID CHANNEL FET

The fabricated FET structure was tested with the p-Si substrate as cathode (source), the Al electrode as anode (drain), and the ITO electrode as gate (Fig. 32b). The three-terminal I-V curves measured in the common cathode mode reveal a clear, well- defined field-effect transistor characteristic (Fig. 32d, e).

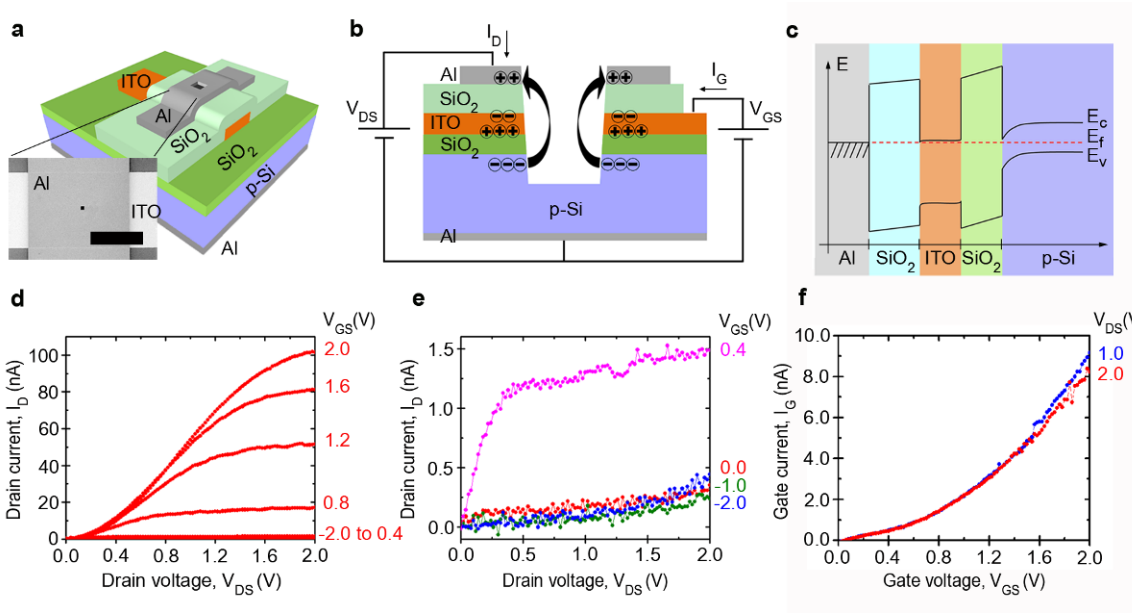


Figure 32 Nano-void channel FET. A Device structure formed on Si MOS substrate (inset: a plan-view SEM image of a nanochannel fabricated by FIB; scale bar, 30 μm). A thin layer of ITO was introduced into the MOS capacitor structure as a gate electrode, overall forming a vertically-stacked 5-layer structure: 20-nm Al / 30-nm SiO_2 / 20-nm ITO / 20-nm SiO_2 / p-Si substrate. A nano-void-channel of square cross-section (0.5x0.5 μm^2, 1x1 μm^2, and 2x2 μm^2) was formed by FIB etching of the stacked layers. b, Operation of a nano-vacuum FET. The ITO gate layer is designed to control electron inversion layer formation in the p-Si substrate. c, A schematic drawing of energy band diagram at zero bias. d, I-V characteristics of a nanochannel FET (1x1 μm^2) measured in common source (cathode) mode. For VGS > 0.4 V, the channel current is ON. e, ID versus VDS measured at VGS < 0.5 V. f, IG versus VGS measured at VDS = 1 V or 2 V.

4.4 RESULT AND DISCUSSION

The nano-void channel demonstrates a turn-on threshold voltage of ~0.5 V. At below threshold (V_{GS} < 0.5 V) the channel current remains off even at V_{DS} of ~2 V, indicating that the 2DES layer induced in the ITO layer provides a good shielding effect on the electrostatic field applied by the drain-source voltage [21-25]. At above threshold (V_{GS} > 0.5 V) the channel current turns on and reveals $V^{3/2}$ dependence on the drain-source voltage for V_{DS} < V_{GS}. This indicates that electrons emitted from the inversion layer in p-Si are accelerated by the electric field developed between anode and cathode edges, and travel ballistically in the nano-void channel region. The slope of 1.5 also indicates that the channel current is space-charge limited. As V_{DS} approaches VGS, the increase of channel current gradually tapers down. For V_{DS} > V_{GS}, the channel current remains flat, whose level is solely determined by V_{GS}. Overall the channel current is governed by two control parameters: gate voltage (V_{GS}) that sets the maximum level of electron inversion charge density in cathode, and anode voltage (V_{DS}) that drives electrons in the void channel with a given level of electron supply available at cathode. At positive bias on the gate comparable to the anode (for example, V_{GS} = 2 V and V_{DS} = 2 V), the gate current (IG) is measured to be ~8 nA (Fig. 32f). This corresponds to 8 % of the anode current measured at the same bias (I_D = 100 nA at V_{GS} = 2 V and V_{DS} = 2 V) (Fig.32d). This indicates that the gate electrode (ITO) is not as efficient as the anode (Al) in capturing electrons, while it is evident that the gate layer provides a good control of electron emission at cathode edge via modulating induction/depletion of a 2DES layer at the Si/SiO_2 interface. This apparently conflicting behavior may suggest that the electron flow is very close to the gate and/or there is no lateral (horizontal) field of sufficient strength that can attract passing electrons into the gate, although the underlying mechanisms remain to be determined.

The transconductance, g_m of the nano-void-channel FET device is measured to be 20 nS/μm without correction for anode collection efficiency. When the anode electrode is designed to capture all emitted/transported electrons, the device transconductance is expected to increase by two orders of magnitude, reaching 2 μS/μm level. This number is comparable to those of FETs made on graphene layers [30-32], and yet significantly smaller than those of Si MOSFETs (~1000 μS/μm) [33, 34]. One way to further increase transconductance would be to increase the total edge length on a given foot print of device, e.g., designing the edges into serpentine or interdigitated patterns. Our nano-void-channel FETs show an on/off-current ratio of ~500 at VDS = 2 V. This is compared to much smaller ratios (typically ~2) of graphene FETs. In high frequency operation, the switching speed is expected to be governed by the effective delay time of anode current, expressed as $\tau = C/g_m$ [1]. In the vertical void-channel FET structure, the device capacitance (C) would scale with gate electrode area (A). The device transconductance (gm) scales with edge length (L): for the case of 100 % anode collection efficiency and 23 nm oxide thickness for both gate-cathode and gate-anode capacitors, g_m is expected to reach the level of 2 (μS/μm) x L (μm). For an ideal case, edge length L is to be maximized for minimum electrode area A. An array of closely-spaced slit-shaped aperture wells (instead of having a single square well) would be considered close to ideal. Imagine, for example, an FET with a 1 μm^2 x 1 μm^2 top electrode that fully covers an array of 10 slit wells (100 nm width; 1 μm length; 100 nm slit spacing; 1 μm etch depth) formed within the electrode area: gm is estimated to be 20 μS, and C is to be 15 fF. This would result in τ of 80 ps. The low voltage, stable, high-speed operation of nano-void-channel FETs in room-temperature air-ambient would offer an interesting potential for nanoelectronic devices that are compatible with and yet can complement conventional Si CMOS electronics.

5.0 VERY LOW ENERGY (< 3 EV) ELECTRON PERMEABILITY OF SUSPENDED GRAPHENE

5.1 INTRODUCTION

Harboring a two-dimensional electron system, graphene can be highly conductive in in-plane transport while being transmissive to impinging electrons. Based on these in- and out-of-plane interaction properties, a suspended graphene membrane is promising as an ideal gate (grid) to control electron transport in nanoscale vacuum electronic devices. We report measurement of capture and transmission efficiencies of very low energy (< 3 eV) electrons impinging upon a suspended graphene anode that is placed on top of a nanoscale void channel formed in a SiO_2/Si substrate. Electron capture efficiency of 0.1 % (transmission efficiency of 99.9 %) is observed at 1 V bias. Presence of suspended graphene is also found to significantly enhance electron emission at cathode beyond the level of Child-Langmuir's space-charge-limited emission.

Graphene possesses many fascinating properties originating from the manifold potential for interactions at electronic, atomic, or molecular levels [62, 63]. Being a monolayer carbon lattice, graphene is transmissive to impinging electrons while being impermeable to atoms and molecules [64]. At electron energy < ~10 eV the de Broglie wavelength becomes greater than the lattice atomic spacing and crystalline diffraction is less likely to occur. Below 5-10 eV, the dominant scattering mechanism is expected to involve inelastic interactions such as electron

excitations or electron-phonon interactions [65-66]. The damage threshold of graphene is known to be > 15 eV, corresponding to incident electron energy > 80 keV [68, 69]. Considering the relatively large threshold, electrons of very low energy (< 3 eV) are expected to induce no damage to graphene. In this study we characterize the capture and transmission interactions of very low energy electrons with suspended graphene and explore the potential to use graphene as an electron-permeable grid layer in low-voltage nanoscale vacuum electronic devices [70-73].

In generating a constant flux of very low energy electrons we are exploiting the phenomenon that a two-dimensional electron gas (2DEG) induced at the SiO_2/Si interface of a metal-oxide-semiconductor (MOS) structure can easily emit into air (void channel) at low voltage (~1 V) [73]. This low-voltage emission, enabled by Coulombic repulsion of electrons in 2DEG, has the effect of negative electron affinity, and demonstrates high current density emission (~10^5 A/cm^2). The emitted electrons ballistically travel in the nano-void channel. The channel length (i.e., the thickness of oxide layer) is designed to be smaller than the mean free path of electrons in air (~60 nm). Therefore, emitted electrons should travel scattering-free in the ambient (air) channel, as if in a vacuum. The transit time is estimated to be 10-100 fs for 10-20 nm-thick SiO_2 at 1-10 V bias.

5.2 GRAPHENE TRANSFER PROCESS AND DEVICE FABRICATION

5.2.1 Graphene transfer process

To form suspended graphene membranes over trenches or FIB channel of SiO_2/Si substrate, we started with monolayer graphene (purchasedfrom Advanced Chemicals, grown on 25 μm copper foil by chemical vapor deposition) (Fig. 33A). The Cu foil (~0.3×0.5 cm^2) with single layer graphene was spin-coated with PMMA (MicroChem Corp. 950 PMMA A7, 4% in anisole) followed by selective etching of the copper. The Cu substrate was etched down to the underlying graphene/PMMA by a ferric chloride solution (COPPER ETCH TYPE CE-100) about 30 minutes (Figs. 33B and C). The graphene/PMMA stack film was floated on the surface of the etchant, and a clean glass substrate was then submerged into the solution to lift the floating film and transfer into deionized water container for ~10 min. The process was repeated at least 3 times in order to remove etchant residue. A target substrate (SiO_2/Si wafer) was then immersed into the DI water and lifted the graphene/ PMMA film from water while the film was positioned by a needle (Fig. 33D). Consequently, the graphene/ PMMA film was placed onthe substrate. Next, the unwashed PMMA was thermally annealed at ~70˚C for 2 hours to remove water, and strengthen the adhesion between the graphene and the substrate [112]. Finally, the PMMA was gently removed inacetone follow by rinse in methanol and DI water. The sample was heated at ~70˚C for ~2 hour to remove any trapped moisture and to enhance adhesion/ flattness of graphene (Fig. 33E)

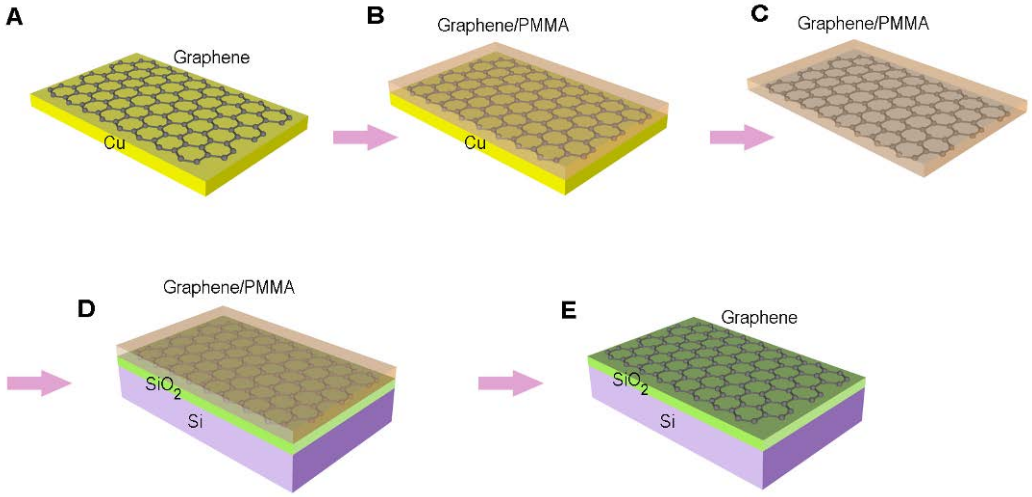


Figure 33 Schematic illustration of graphene wet transfer processes. (A) Graphene/Cu foil, (B) Graphene / Cu foil/ PMMA stack layer, (C) Graphene/PMMA stack film, (D) Graphene/ PMMA stack film transferred to SiO_2 / Si substrate, (E) Graphene / SiO_2 / Si layer

5.2.2 Fabrication process flow of a nano-void channel (500 nm x 500 nm cross-section; 1 μm depth) by focused-ion-beam (FIB) etching

A metal-oxide-semiconductor (MOS) capacitor structure was formed by growing a ~20 nm thick thermal oxide layer on n-type Si (P-doped, 5 Ω-cm resistivity) wafers [(100)-oriented; 525 μm thickness]. The bottom electrode was prepared by depositing a 150-nm-thick Al layer (5N purity) by thermal evaporation, followed by Ohmic contact annealing at 350 ^{o}C (Fig 34A). A stripe pattern of Al electrode (20 nm thickness; 40-60 μm width; 1 mm length) was prepared on top of the oxide layer by thermal evaporation in conjunction with a photolithography and lift-off process (Figs 34B and C). After formation of the conventional MOS capacitor structure, the MOS wafers were further processed to develop nanoscale void vertical channels by employing a focused-ion-beam (FIB)-etching technique (Fig. 34D) or a mechanical cleaving method. The FIB etching process was performed with Seiko Dual Beam System (SMI-3050SE). A Ga ion beam (30 keV; 94 pA) was used with 0.5 μs dwell time in creating square wells (cross-section: 0.5x0.5 μm^2) in Si MOS wafers. The Al electrode was further removed by photolithography process in conjunction with aluminum etchant (HCl: HNO_3:H_2O = 1:1:1) (Fig. 34E).

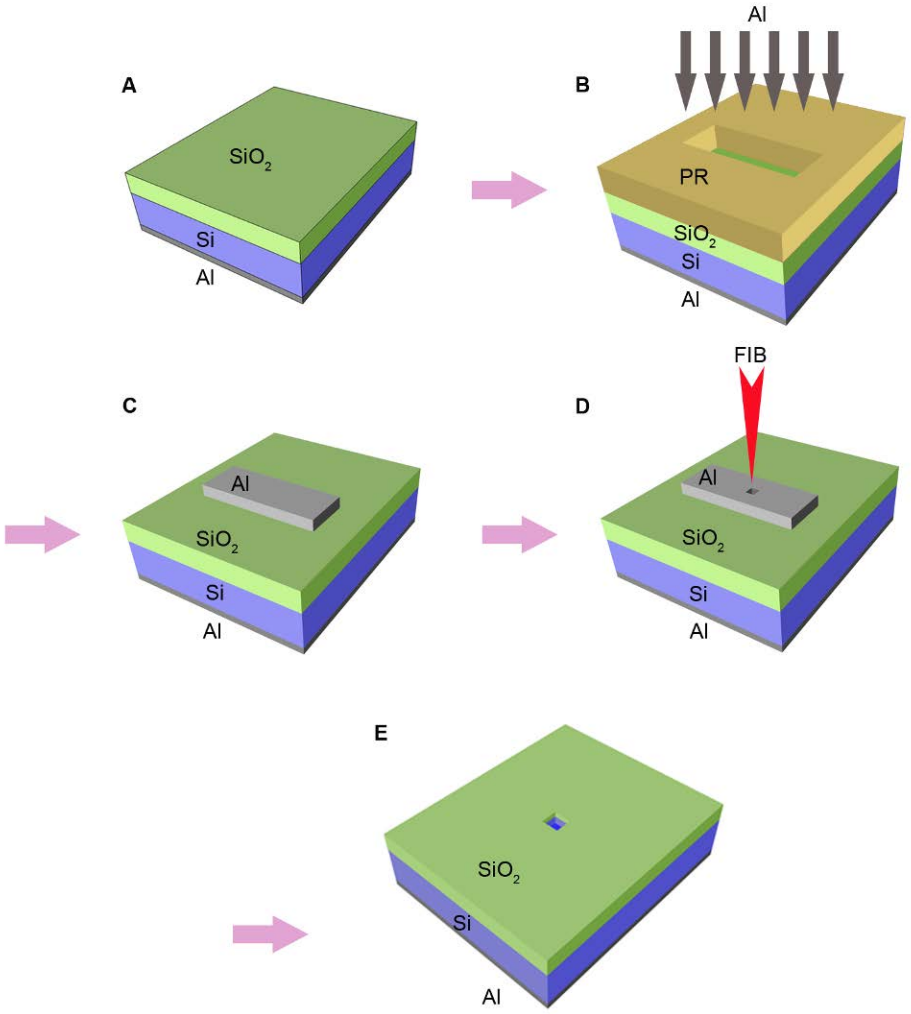


Figure 34 The fabrication process flow of a nano-void channel (500 nm x 500 nm cross-section; 1 μm depth) that was focused-ion-beam (FIB) etched into a SiO2 (23 nm thickness)/n-Si (5 Ω-cm resistivity) substrate

5.2.3 Fabrication of a suspended graphene on SiO_2/n-Si trench structure

A single or multiple trenches void-channel structure was fabricated on n-Si [B-doped, 10 Ω-cm resistivity; (100)-oriented; 525 μm thickness]. First, ~20-nm-thick SiO_2 layer was thermally grown on top of Si substrate (Fig. 35A). Next, a 50-nm-thick Cr film was deposited as an etch mask on top of the silicon dioxide by thermal evaporation (Fig. 35B). Subsequently, opening narrow strips pattern (~4-60 μm width; 8-10 mm length) was formed by photolithography (~2-μm-thick photoresist) in conjunction with an inductively coupled plasma reactive ion etching (ICP-RIE) system (Unaxis 790 ICP-RIE). The Cl_2/O_2 (Cl_2:O_2 = 15 sccm: 10 sccm) gas mixture was used to open an aperture on the Cr strip mask on SiO_2/Si substrate. Next, CF_4/O_2 (CF_4: O_2 = 37 sccm: 9 sccm) ambient gas was further processed in order to etch SiO_2/Si stack layer down to 500 -1000 nm depth (Figs 35C and D). After that, the remaining photoresist was removed by acetone followed by methanol and DI water rinse. The Cr mask was removed by Cr etchant (NaOH: $K_3Fe(CN)_6$: DI H_2O = 2g : 6g : 22ml). Al (~150-nm-thick) was deposited onto the back side of the Si substrate by thermal evaporation followed by annealing process at 350˚C to form an Ohmic contact (Figs 35D and E). Finally, a monolayer graphene was transferred on top of the trench of SiO_2/Si stack layer as described previously. Overall the vertically-stacked layer structure at the cross is comprised of: monolayer graphene / ~20-nm SiO_2 / n-Si substrate (Fig. 36F). Here the Al Ohmic contact on n-Si substrate serves as a source cathode electrode, and the top graphene as anode electrode.

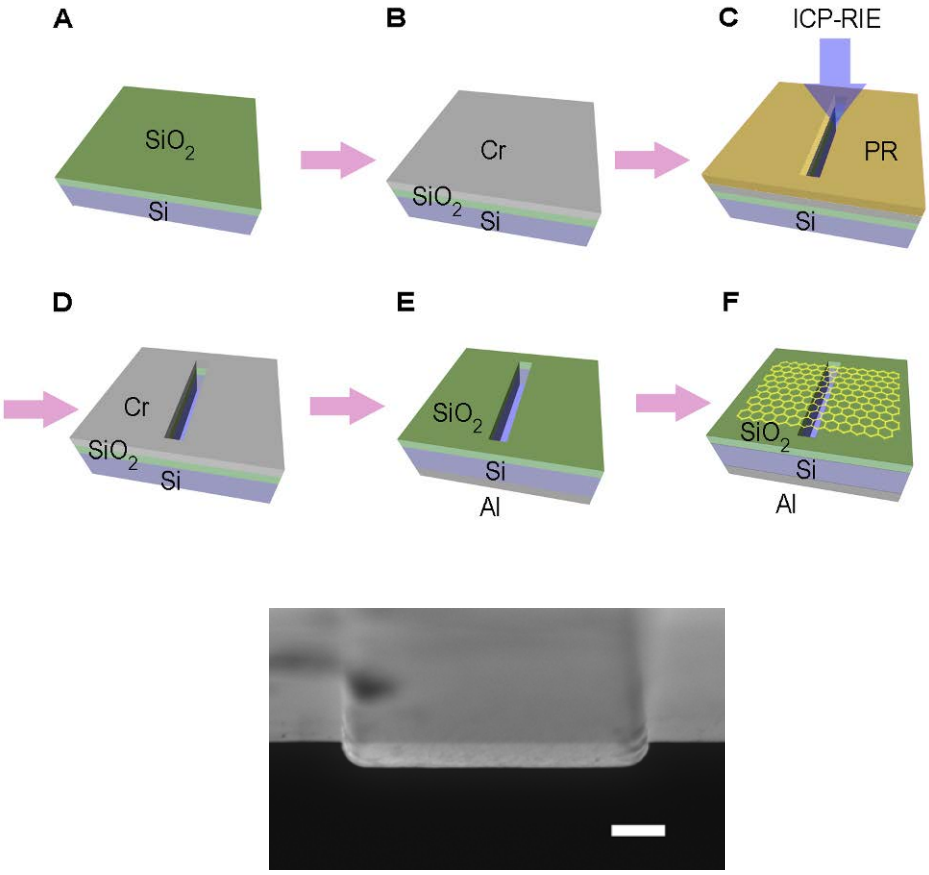


Figure 35 Fabrication of a graphene/SiO_2/Si structure with a nano-void channel. Process flow (top): Thermal oxidation of Si substrate (A); Deposition of a Cr layer (B); Window opening in the Cr layer by photolithography and RIE (C); Trench etching into SiO_2/Si substrate and removal of Cr mask by RIE (D); Al Ohmic contact metallization on the back side of Si substrate (E); Transfer of graphene onto the nano-channel-etched SiO_2/Si substrate (F). SEM image (bottom): A thus-fabricated sample was cleaved, and a cross-section image clearly reveals a monolayer graphene that is suspended flat on the trench-etched SiO2/Si substrate. Trench width, 5 μm; trench depth, 500 nm; SiO_2 thickness, 23 nm. Scale bar, 1 μm.

5.3 THE ELECTRONIC BAND STRUCTURE OF A GRAPHENE-OXIDE-SEMICONDUCTOR AND CHARGE DENSITY CALCULATION

In this study, we have investigated the electronic properties of graphene-oxide-semiconductor (GOS) structure. Graphene properties can be greatly influenced by supporting substrate or metal contact [80]. Graphene shows zero band gap and an ambipolar behavior, i.e., the Fermi level can be symmetrically shifted for both electron and hole doping [82]. This is directly related to the band structure of graphene-oxide-semiconductor since the electronic band alignment is determined by their relative work function. Previous studies reveal that the free standing intrinsic (undoped) work function of graphene is ~4.56 eV [84]. Due to the presence of carriers at the SiO_2/graphene in graphene-oxide-silicon structures, the application of a gate voltage V_G leads to the variation of carrier concentration and thus a shift of Fermi level in graphene, which can be characterized by the following relation [81]:

$$\Delta E_F = \hbar \mid \nu_F \mid \sqrt{\pi . n_s} \tag{5.1}$$

where $\mid \nu_F \mid$ is Fermi velocity = 1.1×10^8 cm/s.

The applied capacitor voltage (V) appears across mainly three places (neglecting the band bending in the metal side): across the band bending region in semiconductor (φ_s), across the oxide layer (V_{ox}), and the flat band voltage (V_{FB}).

$$V_g = V_{FB} + \mid V_{oxide} \mid + \mid \varphi_s \mid \tag{5.2}$$

The flat band voltage of graphene-oxide-semiconductor structure varies depending on the work function of graphene. Thus, the well-known MOS equation (5.2) can be expressed as

$$V_g = [(\phi_{graphene} \pm \Delta E_F) - \phi_s] + |V_{oxide}| + |\varphi_s| \tag{5.3}$$

In a MOS capacitor structure, the space charge density in the semiconductor side can be determined by solving the Poisson equation, and is expressed as follows for the case of p-MOS [93].

$$Q_s = \varepsilon_s E_s = \frac{\sqrt{2}\varepsilon_s}{\beta L_D}\left[(e^{-\beta\varphi_s} + \beta\varphi_s - 1) + \frac{p_{no}}{n_{no}}(e^{\beta\varphi_s} - \beta\varphi_s - 1)\right]^{1/2} \tag{5.4}$$

Where ε_s is the permittivity of semiconductor, and E_s is the electric field at the interface with the oxide layer. φ_s is the band bending at the semiconductor/oxide interface, called the surface potential. $\beta = q/kT$, and L_D is the extrinsic Debye length for electrons, given as $L_D = \sqrt{\frac{\varepsilon_s}{qn_{no}\beta}}$. n_{no} and p_{no} are the equilibrium densities of electrons and holes, respectively.

The voltage drop across the oxide layer (V_{ox}) is related to the space charge (Q_s) and oxide capacitance ($C_{ox} = \varepsilon_{ox}/d$) as follows.

$$V_{ox} = Qs/C_{ox} \tag{5.5}$$

The surface charge of n-Si in accumulation is negative charge

$$V_G = V_{FB} - \frac{Q_S}{C_{oxide}} + |\varphi_S| \tag{5.6}$$

$$V_G = [(\phi_{graphene} \pm \Delta E_F) - \phi_s] - \frac{Q_S}{C_{oxide}} + |\varphi_S| \tag{5.7}$$

Solving the above equations (5.4)-(5.7) simultaneously, the accumulation space charge density Qs can be calculated as a function of applied voltage, *V*. In this calculation, the following numbers were assumed: the work function of Al, 4.1 eV; electron affinity of Si, 4.15 eV; electron affinity of SiO_2, 0.95 eV; dielectric constant of SiO_2, 3.9; dielectric constant of Si, 11.8 [61]. When a Ga droplet is placed on graphene, the graphene's Fermi level is expected to decrease slightly, from 4.56 eV to 4.43 eV.

Table 1. Summary table of accumulation electron density of graphene/oxide/n-Si at 0.1-1.0V forward bias

Top electrode on oxide/n-Si	Work function	At 0.1 V forward bias		At 0.3 V forward bias	
		Forward current	Accumulation electron density	Forward current	Accumulation electron density
Gallium	4.3 eV	≈ 7 nA	≈6×10^{10} cm^{-2}	≈76 nA	≈2×10^{11} cm^{-2}
Graphene/Ga	4.43 eV ± ΔE_F	≈ 655 pA	Depletion/Inversion	≈17.3 nA	≈7.57×10^{10} cm^{-2}
Graphene	4.56 eV ± ΔE_F	≈ 28 pA	Depletion/Inversion	≈ 57 pA	≈1.5×10^{10} cm^{-2}

Top electrode on oxide/n-Si	Work function	At 0.4 V forward bias		At 1.0 V forward bias	
		Forward current	Accumulation electron density	Forward current	Accumulation electron density
Gallium	4.3 eV	≈ 148 nA	≈3×10^{11} cm^{-2}	≈ 1.2 µA	≈8.7×10^{11} cm^{-2}
Graphene/Ga	4.43 eV ± ΔE_F	≈53 nA	≈1.38×10^{11} cm^{-2}-	≈ 1.4 µA	≈6.36×10^{11} cm^{-2}
Graphene	4.56 eV ± ΔE_F	≈ 119 pA	≈5.88×10^{10} cm^{-2}	≈1.3 nA	≈5.2×10^{11} cm^{-2}

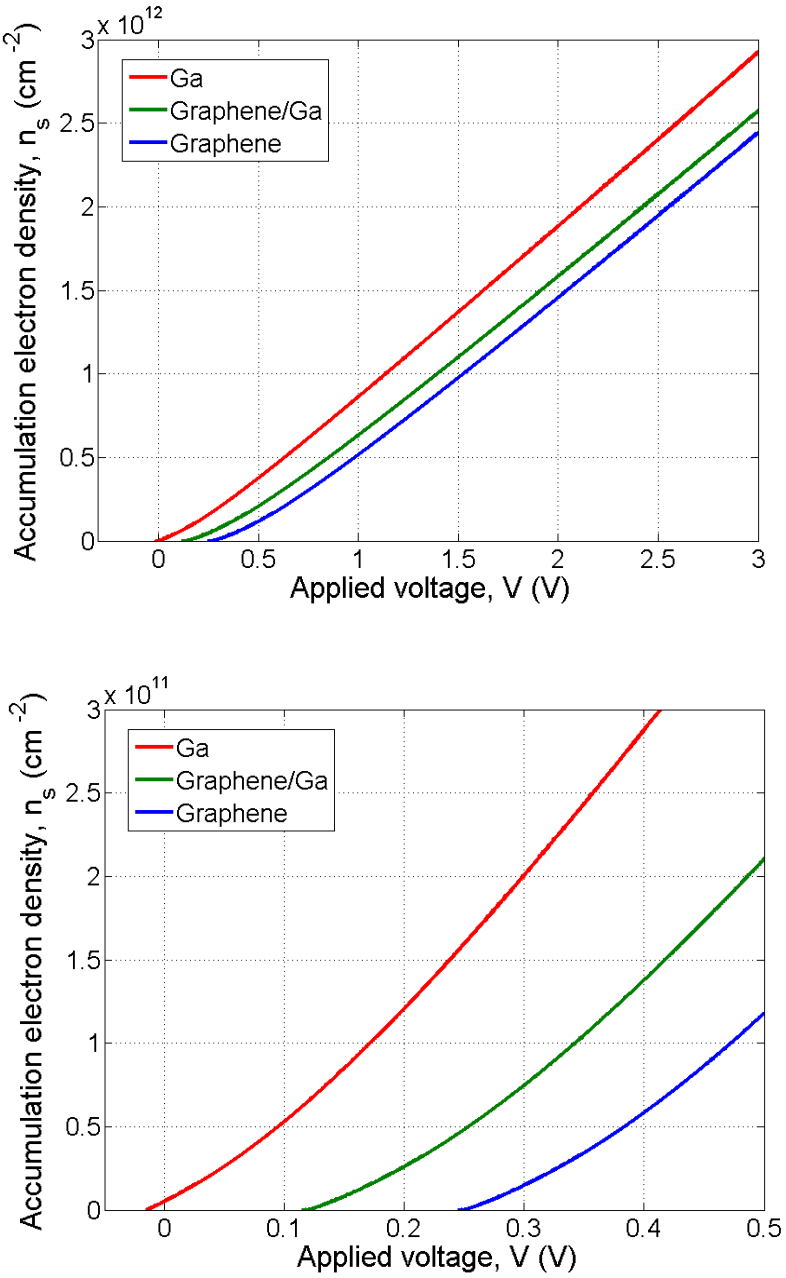


Figure 36 The accumulation electron density (ns = Qs/q) calculated as a function of applied bias voltage V for 0 – 3V (top) and 0 – 0.5V (bottom). Three different cases are shown for top electrode: graphene (blue); graphene/Ga (green); Ga (red). SiO_2 thickness, 23 nm; ND = 1.0×10^{15} cm^{-2}

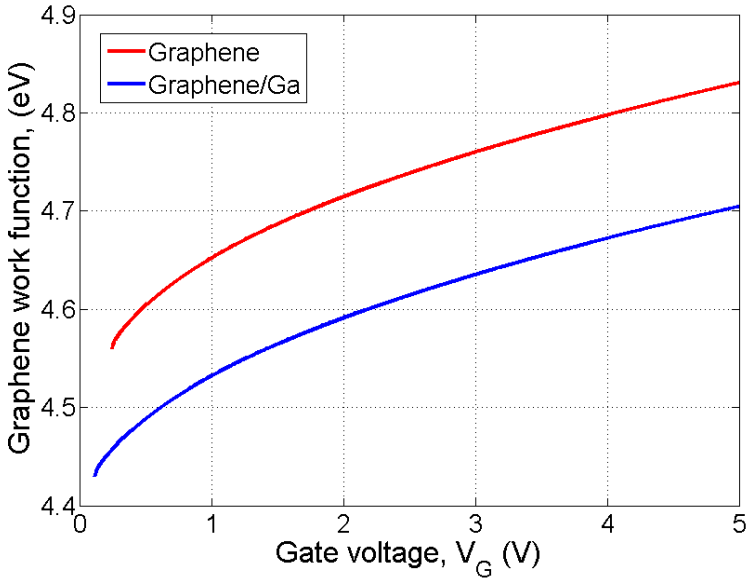


Figure 37 The application of a gate voltage VG leads to the variation of carrier concentration and thus the shift of Fermi level in graphene

5.4 RESULT AND DISCUSSION

5.4.1 Graphene-oxide-n-Si characteristic

A graphene membrane was placed on top of a nano-void channel (500 nm x 500 nm cross-section; 1 μm depth) that was focused-ion-beam (FIB) etched into a SiO_2 (23 nm thickness)/n-Si (5 Ω-cm resistivity) substrate (Fig. 38A&B). A graphene/oxide(or air)/Si (GOS) structure, instead of MOS, was formed by introducing a monolayer graphene as a counter-electrode to the 2DEG layer at the SiO_2/Si interface. Here in the two-terminal mode of operation, the graphene serves as an anode while the n-Si substrate serves as a cathode. Under forward bias (i.e., graphene electrode positively biased with respect to n-Si substrate) a quasi-2DEG (accumulation) develops in the Si side while a 2D hole system (2DHS) forms in the graphene side (Fig. 38C). Due to the Coulombic repulsion of electrons around the aperture edge, the 2DEG in Si emits into air and travels up toward the edge of 2DHS at graphene/SiO_2 interface (Fig. 38B).

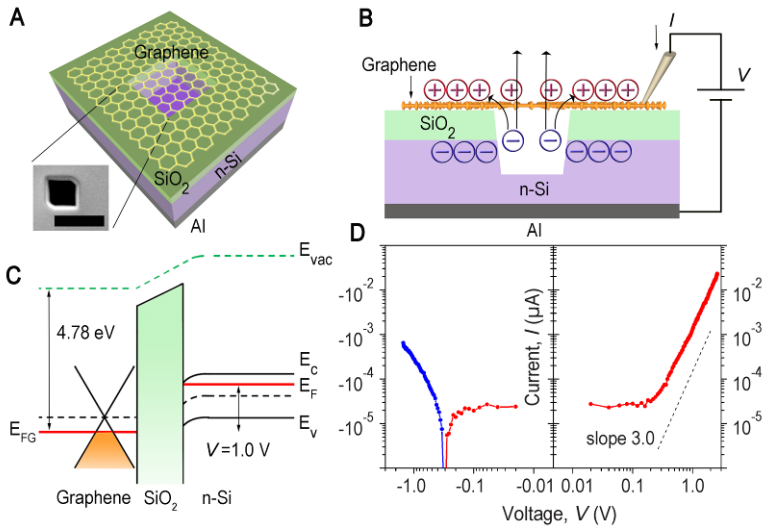


Figure 38 Transport of very low energy (< 3 eV) electrons in a nano-void channel covered with a suspended graphene. (A) Schematic of a graphene/SiO_2/Si structure with a nano-void channel and plan-view SEM image (inset) of a square well (500x500 nm^2) etched into 1 μm depth by FIB. SiO_2 thickness, 23 nm. Scale bar, 1 μm. (B) Schematic of electron emission from the 2DEG at SiO_2/n-Si interface and capture/transmission at the graphene anode. (C) Schematic energy band diagram of a graphene/SiO_2/n-Si structure at 1 V bias. (D) Measured *I*-*V* characteristic of a nano-void channel (500-nm square well) covered with a monolayer graphene. The forward *I*-*V* shows V^3 dependence (red, $V > 0.4$ V) indicating electron-space-charge compensation by holes induced in suspended graphene.

Fig. 38D shows a measurement result of the channel-current-versus-voltage *(I-V)* characteristic. The forward *I-V* characteristic reveals the V^3 dependence for $V > 0.3$ V. Note that the flat band voltage of this GOS structure is 0.25 V, and an electron accumulation layer begins to develop at around this voltage. At 1 V bias, the channel current is measured to be 1.3 nA. The V^3 regime is called the double injection or injected plasma regime [74]. This corresponds to another type of space-charge-limited emission, differing from the Child-Langmuir's $V^{1.5}$ dependence or the Mott-Gurney's $V^{2.0}$ [75-78]: the V^3 regime involves bipolar space charges (electrons and holes) injected into a void channel, whereas the latter ones are mostly governed by unipolar space charges (electrons).

Presence of a free-standing graphene layer in a nano-void channel, therefore the availability of a 2D hole system in the aperture region is expected to affect the space charge field in the channel. In response to electron injection from cathode, for example, the graphene anode brings positive space charges into the void channel by inducing a 2D hole system in the free-standing cover. This has the effect of neutralizing electron space charges. With a reduced space charge field on cathode surface, electron emission becomes easier, resulting in higher channel current with stronger voltage dependence (i.e., V^3 instead of $V^{1.5}$ or $V^{2.0}$).

Besides altering the behavior of space-charge-limited emission under forward bias, a free-standing graphene appears to affect the reverse characteristic as well (Fig. 38D). At around -0.3 V the current level drops to zero, switching the polarity from reverse (blue) to forward (red). Note that bias voltage was swept in the positive direction from -1.5 V to +1.5 V. The early reversal of current flow suggests a discharge of graphene anode around this bias. As the Fermi level is reduced toward the Dirac point, the carrier density of graphene monotonically decreases [79]. Electrons then evacuate from the graphene at reduced bias, and this exiting (discharging)

electron flow has an effect of compensating the reverse leakage (charging) current (Fig. 39). At some bias point the two current components cancel each other, causing a zero-current crossing (i.e., a dip in *I*-*V*).

5.4.2 Discharge-induced reversal of graphene anode current

In order to substantiate this observation (discharge-induced reversal of graphene anode current) we fabricated another graphene/SiO_2/n-Si structure without a nano-void channel. Fig 39 shows and *I*-*V* characteristic obtained by scanning in two different directions. For the positive scan direction (from -1.5 V to +1.5V), a positive surge of current was observed at *V*= -0.62 V to 0.14 V. By integrating the surge current over the corresponding time interval (3.04s), the amount of electrons discharge-transferred out of graphene is calculated to be 1.21×10^{10}. This corresponds to a carrier density of 1.21×10^{11} cm^{-2} when averaged over the entire graphene sheet (2 mm* 5mm = 10 mm^2). The observed carrier density shows a reasonable agreement with that calculated for graphene at the same bias voltage. When scanned in the negative direction (freom +1.5V to -1.5V), the same sample reveals a negative surge of current in positive bias and no surge in reverse bias. In the negative scan the discharging process involves holes and is governed by the same mechanism that the carrier density diminishes for reduced Fermi levels. Overall this result supports the observation that graphene's discharging process can have a canceling effect on the current component transported through a nano-void channel, causing a voltage shift of zero-crossing point in *I*-*V* measurement.

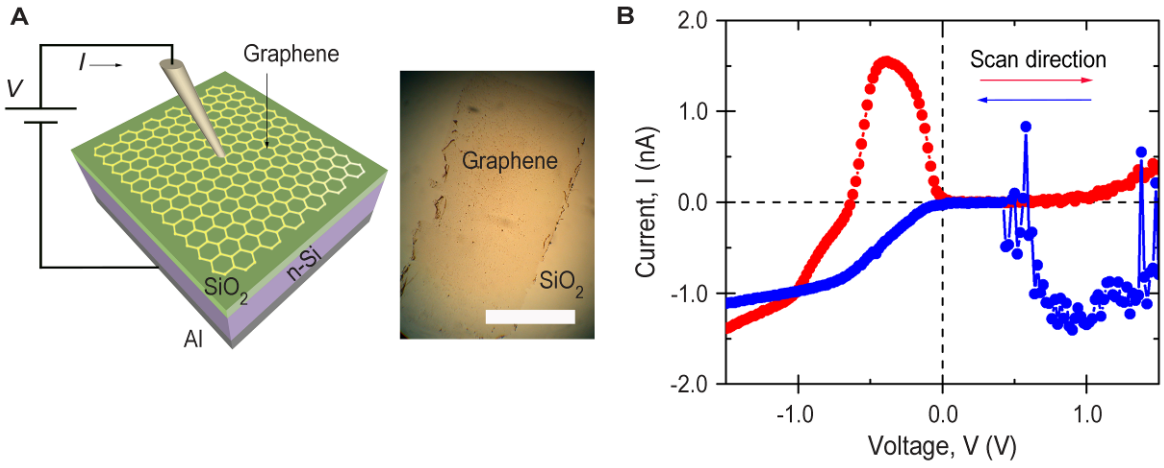


Figure 39 Graphene discharge and current reversal. (A) A schematic of a graphene/SiO^2/n-Si structure without a nano-void channel and I-V measurement (left). An optical micrograph of a sample showing a monolayer graphene placed on SiO^2/Si substrate (right). Scale bar, 2 mm. (B) I-V characteristics measured by scanning in two different directions: from -1.5 V to +1.5 V (red); from +1.5 V to -1.5 V (blue). The voltage step was 0.02 V, and the total scan time was 12 s. As the bias voltage is reduced toward zero, the graphene discharges its carriers, revealing a reversal of current flow. From the time interval (3 s) of current reversal (red: -0.6V to 0V with peak current of +1.5 nA), a total discharge amount is estimated to be $1.2x10^{10}$ electrons. When averaged over the graphene area (0.1 cm^2), this corresponds to a carrier density of 1.2x1011 cm^{-2}

5.4.3 Electron capture efficiency of suspended graphene anode

In order to estimate the total electron emission from cathode, the graphene anode was covered by placing a Ga droplet in the aperture area (Fig. 40A). Note that the Ga droplet size is designed to be much larger than the channel diameter (i.e., 500 μm versus 500 nm) so that incident electrons are fully blocked by the Ga-covered graphene anode. The forward *I-V* characteristic clearly reveals the V^3 dependence for $V > 0.1$ V. By placing Ga on top, graphene's work function is expected to decrease slightly by ~0.2 eV [80]. This will then reduce the flat band voltage to ~0.12 V, as seen in the earlier on-set of steeply rising channel current (Fig. 40, red). The V^3 regime of the Ga-covered graphene sample shifted up almost parallel to that of the sample without Ga. This indicates that the graphene layer underneath Ga still plays the same role of compensating the effect of electron space charges as in the case of the graphene-only sample via inducing holes in the suspended area. At 1 V bias, the channel current with graphene/Ga is now measured to be 1.4 μA, 1.1×10^3 times increase from the current without Ga (1.3 nA). When assuming all incident electrons are blocked and captured by the graphene/Ga anode, the total electron emission from cathode equals the measured anode current (1.4 μA) [81]. Further assuming that the emission current of the graphene/Ga sample remains the same as that of the graphene-only sample, the electron capture efficiency of suspended graphene anode is estimated to be 0.1 % at 1 V bias.

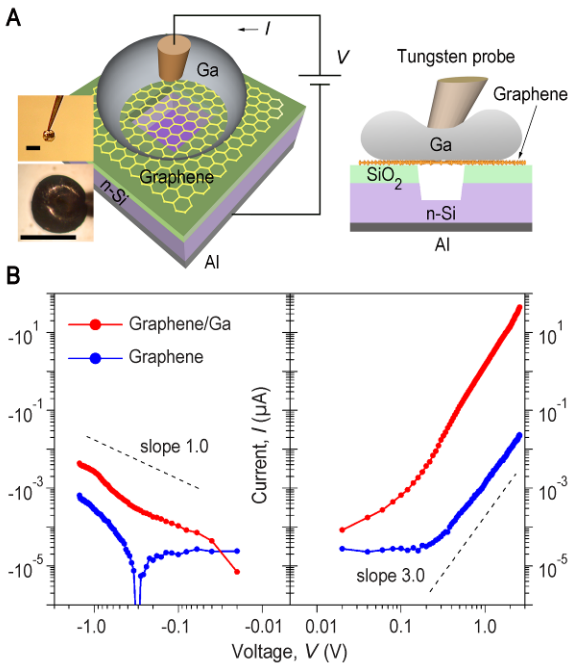


Figure 40 Electron capture efficiency of a suspended graphene anode. (A) Schematic of electron emission measurement. A Ga droplet is placed on top of the graphene anode covering the entire aperture area (inset: optical micrograph of a Ga droplet attached to a tungsten probe). Scale bars, 500 μm. (B) Measured I-V characteristics: with a Ga cover on graphene (red) and without Ga (i.e., graphene only) (blue). The channel current increased by 1100 times (from 1.3 nA to 1.4 μA at 1 V bias) after Ga cover, implying that the electron capture efficiency at a suspended graphene anode is ~0.1 %.

The 1.4 μA channel current of the graphene/Ga sample at +1 V corresponds to an injection rate of ~10^{13} electrons/s at cathode and the same rate of electron capture at Ga-covered graphene anode. The electron transit time in a nano-void channel is estimated to be ~100 fs at 1 V bias for 23 nm channel length [74]. This implies that on average one electron is in transit inside the void channel. In other words, an average amount of electron space charge is to be of single electron level. A similar amount of hole charges are expected to be induced on the suspended graphene area (500 nm x 500 nm). The resulting space-charge density in graphene is then estimated to be maximum ~4 holes/μm^2, corresponding to ~$4x10^8$ holes/cm^2. The induction of holes at this level of density is expected to shift the graphene's Fermi level by no more than 0.1 eV at 1 V bias [82-84]. Overall the result demonstrates the graphene's enabling nature of enhancing cathode emission by inducing hole space charges thereby compensating the electron space charge effect.

Note that the zero-current crossing point in reverse bias (i.e., the dip at -0.3 V in the graphene-only sample) now shifted close to 0 V (~-0.01 V) with the graphene/Ga sample (Fig. 40B, red). This is explained by that the Ga-covered-graphene has a reduced work function (Fermi level), shifting the discharging of graphene to occur at lower bias. For a given bias voltage, the Fermi level shift might have affected the band bending on Si side, altering the density of 2DEG at SiO_2/Si, therefore cathode emission. In order to further investigate these possible effects of anode work function change (i.e., graphene Fermi level shift) on emission and capture at 2DES edges, an additional sample structure was prepared and characterized.

5.4.4 The effects of graphene Fermi level shift on 2DEG emission and capture

Without involving graphene a Ga droplet was directly placed on top of a nano-void-channel-etched SiO_2/n-Si substrate, and the resulting *I-V* characteristic was compared with that of the sample with graphene/Ga (Fig. 41). Again the Ga droplet size was designed to be significantly greater than the channel diameter (500 μm versus 500 nm) so that incident electrons are fully captured. The forward *I-V* characteristic reveals the V^2 dependence for $V > 0.1$ V (Fig. 41, red). At low bias (V < 0.8 V) the sample with Ga-only (red) shows larger current than the sample with graphene/Ga (blue). This is explained by the fact that the work function of Ga (4.3 eV) is smaller than that of the graphene under Ga (estimated to be 4.43 eV) [80], and therefore accumulation electrons build up more readily at low voltage for the Ga-only sample case. At 0.4 V, for example, the 2DEG density is calculated to be 3.0×10^{11} cm^{-2} or 1.4×10^{11} cm^{-2} for the Ga-only or the graphene/Ga sample, respectively. The ratio of the two electron densities (2.1) well corresponds to the ratio of channel currents at the same bias (148 nA versus 53 nA). As bias voltage is increased over the flat band voltage, accumulation electrons build up fast, ensuing electron emission at cathode and space charge build-up in the void channel. In the graphene/Ga sample case, hole space charges are induced in the suspended graphene area and the double injection regime emerges, as evidenced by a steep rise of channel current at $V > 0.2$ V (Fig. 41, blue). Note that the V^3 regime of the graphene/Ga sample surpasses the V^2 regime current of the Ga-only sample at 0.8 V. This comparison clarifies the roles played by graphene at different bias regimes: in low bias the presence of graphene affects 2DEG density therefore channel current via altering the anode work function, whereas in large bias the graphene influences cathode emission by inducing hole space charges that mitigate the effect of electron space charges.

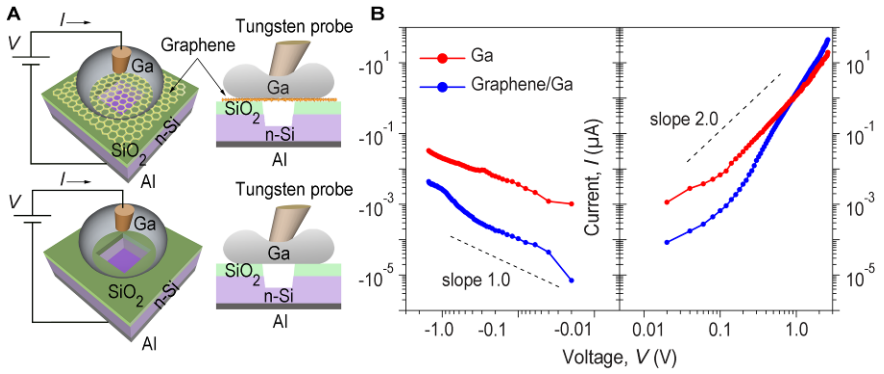


Figure 41 Enhancement of electron emission by a suspended graphene anode. (A) Schematic of nano-void channels covered with a Ga droplet as a top cover: with a graphene layer placed underneath a Ga cover (top) or without graphene (bottom). (B) Measured I-V characteristics: The nano-channel covered with graphene/Ga cover (blue) shows the Fowler-Nordheim tunneling emission, and the channel current surpasses the space-charge-limited current of the sample without graphene (red) at $V > 0.8$ V.

Taking the graphene's Fermi level shift into account, our earlier estimate of electron capture efficiency of suspended graphene anode is now refined as follows. When a Ga droplet is placed on graphene, the graphene's Fermi level is expected to decrease slightly, from 4.56 eV to 4.43 eV. At low bias this can make a significant increase of 2DEG density, e.g., at +0.4 V from $5.9x10^{10}$ cm^{-2} to $1.4x10^{11}$ cm^{-2} after placing Ga. At large bias, however, this effect becomes insignificant, e.g., at +1.0 V bias the 2DEG density increases from $5.2x10^{11}$ cm^{-2} to $6.4x10^{11}$ cm^{-2}, only 1.2 times increase (Fig. 36). The cathode emission of the Ga-covered graphene sample is then estimated to have increased by the same ratio. This suggests that the earlier estimate of cathode emission in the sample without Ga was only slightly overestimated by the same factor (1.2). The electron capture efficiency of a suspended graphene electrode is now confirmed to be in the same range as before, i.e., at 0.1 % at 1 V bias.

5.4.5 The nature of electron capture at a suspended graphene anode

Lastly we elucidate the nature of electron capture at a suspended graphene anode. Here an outstanding question is whether electron capture occurs over the entire area of suspended graphene or only at the channel edges. Previously we reported that in a nano-void-channel MOS with an open apertured anode the 2DEG emission at cathode is proportional to the perimeter of channel edges, not the area of channel cross-section, and also that injected electrons are captured at the edges of 2D hole system at anode [73]. When a suspended graphene is used as an anode, a new question arises as to whether capture occurs in a fashion highly localized (at the edges) or more uniformly distributed (across the suspended area). In order to answer this question the following samples were prepared and compared. Trench and twin-well structures were fabricated by photolithography and inductively-coupled-plasma reactive ion etching (ICP-RIE). The

channel perimeter to area ratio was varied in a wide range by employing different channel widths (5 μm or 60 μm) (Fig. 42A): Sample 1 with three 5-μm-width trenches (15 mm perimeter, $3.8x10^4$ μm^2 area) (blue); Sample 2 with one 60-μm-width trench (5 mm, $1.5x10^5$ μm^2) (green); and Sample 3 with twin-wells of 50 μm x 25 μm (0.3 mm, $2.5x10^3$ μm^2) (red). The measured channel currents were normalized by channel perimeter (Fig. 42B).

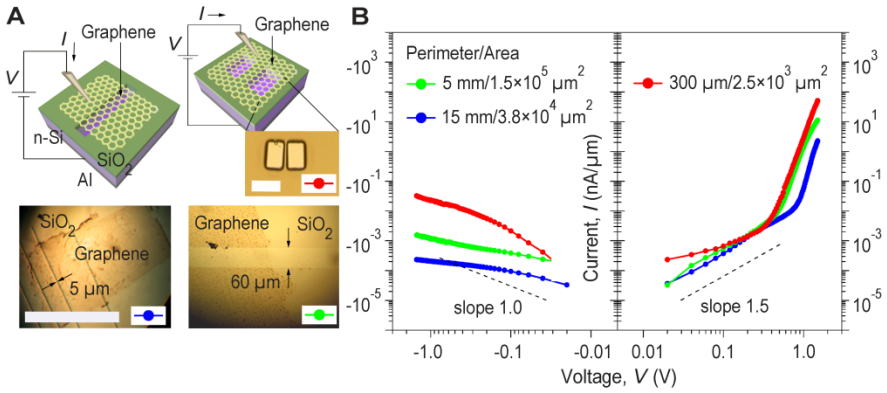


Figure 42 Channel-perimeter dependence of electron capture at graphene anode. (A) Schematic of trench-etched void-channels covered with a graphene and optical micrographs of 5 μm width trenches (bottom left) or 60 μm width trench (bottom right), or a twin-well (inset). Scale bars, 3mm (bottom) and 50 μm (inset). (B) Measured I-V characteristics of trench-etched structures with different perimeter/area ratios. The channel currents normalized by perimeter show a good overlap, indicating that electron capture at graphene anode occurs near/at channel edges, not over the area of graphene.

In all three samples, the channel current reveals a space-charge limited effect ($V^{1.5}$ regime) in low bias, followed by a steep rise at V > 0.4 or 0.8 V. Here the fast rising regime corresponds to the Fowler-Nordheim (FN) tunneling emission of electrons at cathode [85] (Fig. 43).

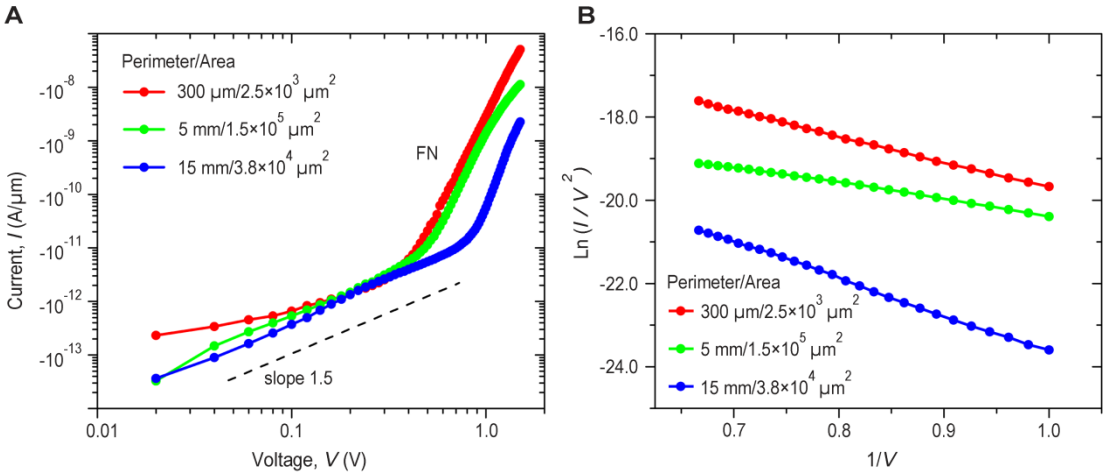


Figure 43 Measured I-V characteristics of a graphene/SiO_2(23 nm)/n-Si with vertically-etched trenches of various different channel perimeter and area. (A) The forward I-V characteristics reveal a space-charge-limited current regime ($V^{1.5}$) at low voltage (< 0.4V or 0.8V) and the Fowler-Nordheim regime at higher voltage. The current is normalized by channel perimeter. The perimeter-normalized currents of three samples closely overlap, indicating that the electron capture at graphene anode is also perimeter dependent, not area-dependent. (B) The FN plots of the I-V characteristics at higher voltage (~1V) demonstrate the Fowler-Nordheim tunneling emission of electrons from the cathode.

Observation of FN emission at large bias implies that the space charge field of electrons at cathode surface is now better (more fully) compensated by hole charges induced in graphene. Note that the degree of space charge neutralization depends on the availability of hole charges in the graphene cover. The near-perfect cancellation of electron space charge field in the three samples can be ascribed to the use of wider channel width (5 μm or 60 μm as opposed to 500 nm), which allows more hole charges than before (the 500-nm FIB sample discussed above). The channel current is primarily determined by two factors, emission of 2DEG at cathode and capture of incident electrons at anode. Cathode emission is perimeter-dependent, as reported before [73]. Anode capture would be either perimeter-dependent (if captured at edges) or area-dependent (if captured over the suspended area), with capture efficiency at graphene edges expected to be much greater than that of free-standing graphene. The perimeter-normalized current of the $V^{1.5}$ regime reveals the same level for the three samples, independent of area (Fig. 42B). This strong perimeter dependence indicates that in low bias electron capture occurs at graphene edges. In large bias, the FN regime currents of Samples 2 & 3 (Fig. 42B, green & red) also show a good overlap, despite a difference in their area/perimeter ratios (i.e., 1.5×10^5 μm^2/5 mm versus 2.5×10^3 μm^2/0.3 mm). This confirms strong perimeter dependence of electron capture at large bias as well. In Sample 1 (5-μm width channels) the FN regime emerges at higher voltage (> 0.8 V) (Fig. 42B, blue). This is ascribed to that the relatively small channel width allows a smaller amount of hole space charges compared to the 60-μm width samples and therefore requires higher voltage to attain the same level of space charge field cancellation. Overall this comparison elucidates that electron capture occurs highly localized to channel edges of graphene.

6.0 PHOTOCARRIER SELF-INDUCED-FIELD IMPACT MULTIPLICATION IN 2D ELECTRON GAS OF A GRAPHENE/OXIDE/SI PHOTODETECTOR WITH A NANOSCALE VOID CHANNEL

6.1 INTRODUCTION

Photocarrier multiplication, the process of generating two or more electron-hole pairs from a single absorbed photon, can occur in semiconductor quantum dots or nanocrystals [86-93]. Translating this carrier-level performance into a device-level improvement in sensing or converting photon energies, however, remains challenging. Here we report a graphene/SiO_2/Si photodetector with a nanoscale void channel that demonstrates internal quantum efficiency of 115-175% as measured with photocurrent in the UV-Vis range. Photocarriers generated in Si are separated by the depletion field developed in the region under the reverse-biased graphene electrode: minority carriers drift to the oxide interface forming an inversion layer of quasi-2D electron system (2DES), while majority carriers are driven away to the substrate inducing a current flow around the external circuitry. The 2D electron gas (2DEG) at SiO_2/Si constantly emits into the nano-void channel [l04], enabling continuous separation of photogenerated carriers. The loss of photoelectrons into air results in accumulation of holes in Si, which in turn induces a strong buildup ($> 10^{13}$ cm^{-2}) of 2DEG at SiO_2/Si as a balancing act of maintaining charge neutrality in the host materials. The electric field in the inversion layer rises above 10^6

V/cm, allowing the carriers there to gain a significant amount of kinetic energy within a mean-free scattering length (6-8 nm). A step-like increase of photocurrent with internal quantum efficiency greater than 100 % is observed for incident photon energy > ~1.9 eV. This spectral dependence indicates a field-assisted energy gain of ~0.3 eV, which supplements the excess energy of photocarriers (> 0.8 eV) satisfying the impact excitation threshold (1.1 eV over the bandgap energy) [95]. The photocarrier multiplication by self-induced electric field in a 2D inversion layer offers an interesting approach to achieving photon energy conversion with quantum efficiency exceeding 100 % for a broad spectral range.

When a strong electric field is applied inside a semiconductor, charge carriers gain enough energy so that they can excite electron-hole pairs by impact ionization. This excitation process in bulk semiconductor requires high field strength, therefore large bias voltage, and usually results in a cascade of impact ionization or so-called avalanche multiplication of carriers leading to a catastrophic damage [97]. Ideally an impact-ionization event must occur within a minimum travel distance before a carrier dissipates its gained energy to the lattice. Considering the phonon mean free path in Si (6-8 nm), however, a prohibitively large field (~10^6 V/cm) would be needed to induce impact ionization [97]. In the case of exciting with above-bandgap photons, photocarriers can be ‘hot’ as generated, possessing kinetic energies equal to the excess energy [98, 99]. This implies that the minimum energy gain required for impact ionization (therefore, threshold field strength) can be significantly reduced depending on incident photon energy. In this study we have investigated photocarrier multiplication in a 2D electron gas layer induced in a graphene/oxide/Si structure. The structure exploits both the hot carrier effect of photoexcitation and the field-assisted energy gain in the 2DEG layer.

6.2 DEVICE STRUCTURE

A graphene/oxide/Si (GOS) structure with a nanoscale void channel was fabricated by employing photolithography, plasma etching, and graphene transfer processes. In brief, a vertically etched trench structure (5 μm or 60 μm width, 500 nm depth) was formed by plasma reactive ion etching (RIE) of a 23-nm-thick-SiO_2-covered (100) Si substrate (p- or n-type doped with resistivity of 5-10 Ω-cm). A monolayer graphene (purchased from ACS Material: CVD grown on 25-μm-thick Cu foil) was then transferred to the trench-etched substrate.

6.3 RESULT AND DISCCUSSION

6.3.1 Dark/photo I-V characteristic of graphene-oxide-silicon (GOS) structure with a nanoscale void channel

First, the dark current-versus-voltage (*I-V*) characteristic was analyzed in order to understand the emission and transport properties of the quasi-two-dimensional electron gas (2DEG) accommodated at the materials interface in the Si or graphene side. In the case of an n-Si substrate sample under forward bias (i.e., graphene anode positively biased with respect to n-Si cathode), a 2DEG develops in the Si side while a 2D hole system (2DHS) forms in the graphene side. Due to the Coulombic repulsion of electrons around the aperture edge, the 2DEG in Si emits into air and travels up toward the edge of 2DHS at graphene/SiO_2 interface [94]

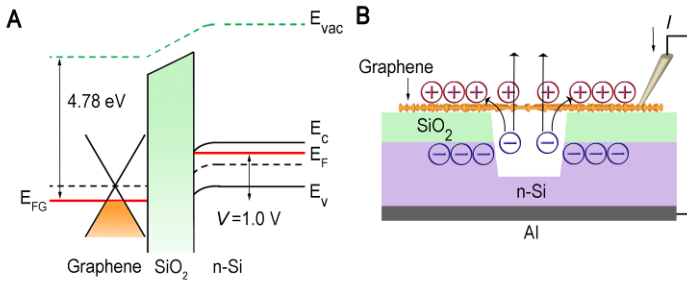


Figure 44 A graphene/SiO_2/Si structure with a nano-void channel. (A) Energy band diagram of a n-Si substrate sample under dark, forward bias (i.e., graphene anode positively biased with respect to n-Si cathode). (B) A 2DEG develops in the Si side while a 2D hole system (2DHS) forms in the graphene side.

The measured forward *I-V* clearly reveals two distinctly different regimes (Fig. 45c, blue: V > 0): space-charge-limited (SCL) emission of 2DEG in the low voltage range (< 0.6 V) and Fowler-Nordheim (FN) tunneling emission in the higher voltage range (> 1.0 V) [100]. The SCL regime with a slope of 1.5 (i.e., voltage dependence of $V^{1.5}$) extends down to ~0.02 V, being consistent with the Child-Langmuir's assumption of zero field strength at emitter surface [101, 102]. The emergence of FN regime at higher voltage is explained as follows. As electron injection increases, the suspended graphene induces hole charges. This has the effect of neutralizing space charges in the void channel. As a result, cathode emission of 2DEG, which has been limited by the injected electrons' space-charge field, now becomes easier and greater in its flux [103]. In the case of a p-Si sample under forward bias (Fig. 45e, blue: $V < 0$), a 2DEG develops in the graphene side while a 2DHS forms in the Si side. Owing to Coulombic repulsion of electrons near the edge, the 2DEG emits into air and travels down to the edge of 2DHS in Si. In reverse bias, most of initial voltage goes to depletion region formation in Si, therefore the *I-V* characteristic shows a slope smaller than 1.5 (Fig. 45c, blue: $V < 0$ for n-Si; Fig. 45e, blue: $V > 0$ for p-Si).

The photo *I-V* characteristic of a p-Si sample was measured under illumination with a 633-nm-wavelength laser light (Fig. 45a). In reverse bias, that is, with the graphene electrode positively biased with respect to p-Si substrate, and for 0.1 mW input power, the photocurrent rises initially slowly (for $V < 0.4$ V), then steeply (for $0.5 < V < 1.2$ V), and finally saturates at 46 μA for $V > 1.5$ V (Fig. 45e, red). This corresponds to responsivity of 0.46 A/W and internal quantum efficiency (IQE) of ~135% (Fig. 45f). In forward bias, a negligible increase of current was observed under illumination.

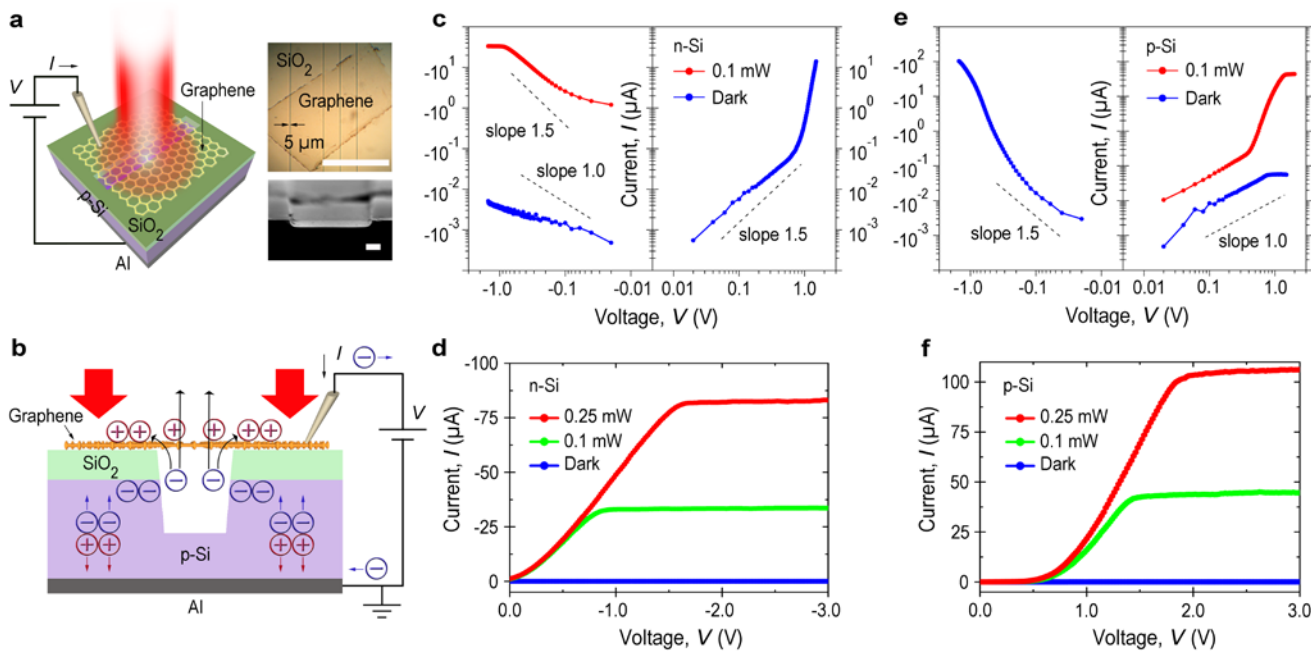


Figure 45 Photodetector operation of a graphene-oxide-silicon (GOS) structure with a nanoscale void channel (a, b), the dark/photo current-versus-voltage (*I*-*V*) characteristic of n-Si (c, d), p-Si (e, f)

The absorption length in Si is 3.0 μm at 633 nm wavelength. Since a monolayer graphene absorbs only 2.3 % of incident light, most photons are absorbed in/near the depletion region (1.0 μm width at 3-5 V reverse bias) [104]. The depletion field in the region covered by a graphene electrode provides a lateral confinement of photogenerated 2DEG within the electrode-covered area. Minority carriers generated outside the graphene electrode (and within the minority carrier diffusion length in Si from the edge: 200 μm for electron and 100 μm for hole) [105] can diffuse into the area under the electrode and get confined at SiO_2/Si.

Similar to the forward bias case, Coulombic repulsion among electrons enables low-voltage emission of photogenerated 2DEG into air. Emitted electrons travel ballistically in the nano-void channel. Some of them are captured/collected at the edge of 2DHS induced in the graphene side, while majority pass through the suspended graphene (Fig. 45b). Majority carriers generated in the depletion region drift to the substrate side, inducing an external current flow. At steady state the saturation photocurrent is balanced by the photocarrier generation rate in Si. Overall the photocurrent is conducted by majority carriers [94, 104]. In the case of n-Si sample, a similar photo *I-V* characteristic is observed (Fig. 45c, red and Fig. 45d). The photocurrent rises with a slope of ~1.5 for low bias ($V < 0.8$ V), then reaches the saturation level at 34 μA for $V >$ 0.8 V. This corresponds to a responsivity of 0.34 A/W and internal quantum efficiency of 100 % at ~0.1 mW.

The pre-saturation I-V characteristics of the two samples, however, significantly differ (Fig. 45c, e). The ratio of the photo- to dark-currents (i.e., on/off ratio) of n-Si sample, for example, is far greater than that of p-Si (e.g., ~5000 versus ~10 at 0.3 V). This can be ascribed to their differing flat band voltages (0.21 V for n-Si versus -0.31V V for p-Si samples) and that in the former sample a strong built-in field develops at low bias readily separating electron-hole

pairs generated in the depletion region. The photocurrent rise in n-Si shows a voltage dependence of $V^{1.5}$ suggesting that the electron transport in air channel is governed by Child-Langmuir's SCL current. In contrast, the p-Si sample shows initially a linear rise ($V^{1.0}$ dependence) followed by a steep rise for 0.5 V < V < 1.0 V. This fast rise regime corresponds to the FN emission observed with the dark, forward *I-V* of n-Si sample, in which the suspended graphene provides space charge holes that compensate the electron space-charge field effect on cathode (2DEG) emission. A similar effect is expected in the photo, reverse *I-V* of p-Si sample (Fig. 45b): photogenerated 2DEG emits into air channel and the suspended graphene provides holes enhancing cathode emission therefore inducing the fast rise FN regime.

6.4 SPECTRAL DEPENDENCE OF PHOTOCURRENT RESPONSIVITY OF GRAPHENE/SIO_2/P- (OR N-) SI STRUCTURE WITH NANO-VOID CHANNELS

The spectral dependence of photocurrent responsivity of the graphene/SiO_2/p- (or n-) Si structure with nano-void channels was characterized in the UV-Vis-IR range at input power of ~0.1 mW (Fig. 46). It is important to note that both samples show a step-like increase of responsivity/quantum efficiency at ~650 nm: from ~105% to ~115% for p-Si and from ~94% to ~100% for n-Si sample. The observation that the quantum efficiency jumps up surpassing 100 % level for photon energy greater than ~1.9 eV indicates a threshold behavior associated with carrier multiplication [95, 106]

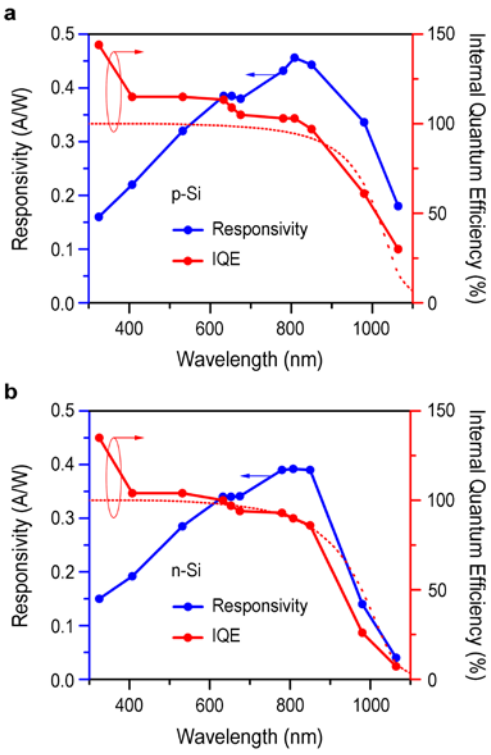


Figure 46 The spectral dependence of photocurrent responsivity of the graphene/SiO2/p- (or n-) Si structure with nano-void channels was characterized in the UV-Vis-IR range at input power of ~0.1 mW (IQE simulation: red dot calculated by minority carrier diffusion length in Si from the edge: 200 μm for electron and 100 μm for hole)

6.5 BAND BENDING AND ELECTRIC FIELD DISTRIBUTION IN THE GRAPHENE/SIO_2/SI STRUCTURE AND CALCULATION OF THE IMPACT IONIZATION/CARRIER MULTIPLICATION UNDER ILLUMINATION

In order to substantiate this finding and to elucidate the underlying mechanisms we have analyzed the band bending and electric field distribution in the graphene/SiO_2/Si structure and calculated the impact ionization/carrier multiplication under illumination of 633-nm wavelength light (Fig. 47). At steady state the 2DEG at SiO_2/Si constantly emit into air, leaving photogenerated holes behind in Si. Being majority carriers, photoholes quickly spread across bulk Si in the time scale of dielectric relaxation and induce an external current along the circuitry. It is important to note that despite the constant loss of photoelectrons into air the host material system (graphene/SiO_2/Si) maintains charge neutrality: electrons are supplied to the system through the ground terminal. The photohole charges in Si are balanced by the photoelectron inversion charges at SiO_2/Si, therefore the net charge in Si does not increase even after illumination. Compared to the dark case at the same bias (5 V), the 2DHS in the graphene side slightly decreased (from 4.51 $x10^{12}$ cm^{-2} to 4.48 $x10^{12}$ cm^{-2}), although the 2DEG at SiO_2/Si significantly increased under illumination (from 4.39$x10^{12}$ cm^{-2} to 1.08$x10^{13}$ cm^{-2}). The voltage drop across the oxide layer V_{ox} decreased (from 4.19 V to 4.15 V), enabling more band bending in Si (surface potential, from 0.89 V to 0.93 V), consistent with the increase of 2DEG at SiO_2/Si under illumination. Note that the band bending in bulk Si remains negligible even with presence of photohole charges there. This is because the photohole concentration in bulk Si is far below the background level (~1.2$x10^{14}$ cm^{-3} versus ~1.32$x10^{15}$ cm^{-3}). Without emission of 2DEG into air, photocarriers would continue to build up in Si until the depletion region collapses. Without depletion field there would be no more separation of photocarriers and therefore no photocurrent.

Therefore the presence of a nano-void channel through which photoelectrons constantly emit into air is essential for photocurrent flow.

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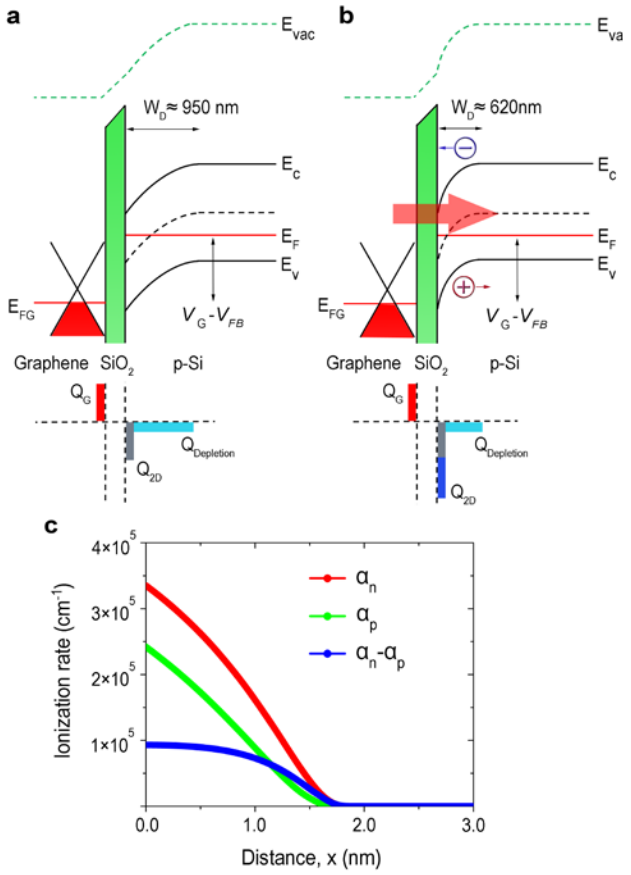


Figure 47 Band bending, space charge distribution, and impact ionization rates of a graphene/SiO_2/Si structure: under dark condition (a), under illumination (b) and calculated the impact ionization/carrier multiplication under illumination (c) at input power of ~0.1 mW, 633 nm wavelength .

6.5.1 Dark, reverse, quasi-static operation calculation of GOS structure

6.5.1.1 Surface charge density $|Q_s|$ as a function of surface potential φ_s can be obtained from

$$|Q_s| = \varepsilon_s E_s = \frac{\sqrt{2}\varepsilon_s}{\beta L_D}\left[(e^{-\beta\varphi_s} + \beta\varphi_s - 1) + \frac{n_{po}}{p_{po}}(e^{\beta\varphi_s} - \beta\varphi_s - 1)\right]^{1/2}$$

where $L_D = \sqrt{\frac{\varepsilon_s}{qp_{po}\beta}}$ is extrinsic Debye length for hole.

$$L_D = \sqrt{\frac{\varepsilon_s}{qp_{po}\beta}} = \sqrt{\frac{(11.8\times 8.854E-14)}{(1.6\times 10^{-19}\times N_a \times 38.62)}} = \frac{411.192}{\sqrt{N_a}}cm$$

$$\frac{\sqrt{2}\varepsilon_s}{\beta L_D} = \frac{\sqrt{2}\times(11.8\times 8.854E-14)}{38.61\times L_D} = \frac{3.8258E-14}{L_D}$$

$$\frac{n_{po}}{p_{po}} = \left(\frac{n_i}{N_A}\right)^2 = \left(\frac{1.0\times 10^{10} m^{-3}}{N_a}\right)^2$$

Thus

$$|Q_s| = \varepsilon_s E_s = \frac{3.8258E-14}{L_D}\left[(e^{-38.62\varphi_s} + 38.62\varphi_s - 1) + \frac{n_{po}}{p_{po}}(e^{38.62\varphi_s} - 38.62\varphi_s - 1)\right]^{1/2}$$

Thus, by assuming φ_s from 0 to 1 V (depletion and inversion operation region) we can obtain $|Q_s|$ as a function of φ_s

Depletion charge $Q_D \approx \sqrt{2\varepsilon_s qN_A(2\varphi_s)}$, *Deplete width*, $W = \sqrt{\left(\frac{\varphi_s \times 2\varepsilon_{Si}}{qN_A}\right)} = 3613.81\sqrt{\left(\frac{\varphi_s}{N_A}\right)}$

6.5.1.2 Gate voltage, V_G as a function of surface potential φ_s can be obtained from

$$V_G = V_{FB} + V_{oxide} + \varphi_s$$

$$V_G = V_{FB} + \left|\frac{Q_S}{C_{oxide}}\right| + \varphi_S = (\phi_m - \phi_s) + \left|\frac{Q_S}{C_{oxide}}\right| + \varphi_S ; \phi_m = \phi_{graphene}$$

The Fermi energy in graphene changes as

$$\Delta E_F = \hbar \,|\nu_F|\sqrt{\pi . n_s}$$

Where $|\nu_F|$ is Fermi velocity = 1.1E8 cm/s

Thus, $V_G = (\phi_{G\_\text{int}rinsic} + \Delta E_F) - \phi_s + \left|\frac{Q_S}{C_{oxide}}\right| + \varphi_S ; \phi_m = \phi_{graphene}$

Similar to n-Si, $V_G = (\phi_{G\_\text{int}rinsic} - \Delta E_F) - \phi_s + \left|\frac{Q_S}{C_{oxide}}\right| - \varphi_S ; \phi_m = \phi_{graphene}$

Table 2. Summary of initial parameters for impact multiplication calculation

ni	1.0×10^{10} cm^{-3}
N_A	1.32×10^{15} cm^{-3}
N_D	1.0×10^{15} cm^{-3}
Oxide thickness	20 nm
V_{FB}	ϕ_{ms}
graphene work function	$4.56eV \pm \Delta E_F$
p-Si work function	4.91 eV
n-Si work function	4.315 eV

6.5.2 Band bending and charge/electric field distribution in the graphene/SiO_2/Si structure under illumination at input power of ~0.1 mW, 633 nm wavelength.

The photo electron/hole pairs generated in silicon substrate, specifically at 0.1 mW of HeNe laser 633 nm on Graphene/oxide/p-Si with trench.

Light is fully absorbed in Si ~ 98%, input power is ~ 10^{-4} W,

Photon energy is 1.24/0.633 = 1.96 eV.

The Generation rate, R = 10-4 W/ 1.96 eV ≈ 3.2×10^{14} s^{-1}

At ~ 1mm^2 area light spot (0.01 cm^2), the photogeneration rate is 3.2×10^{16} s^{-1} cm^{-2}

At 100% electron generation and 300 μs life time of electron and 100 μs for hole, Number of photo carrier is

$N_e = R \times T_e \approx 3.2\times10^{16} \times 300\ \mu s \approx 9.6\times10^{12}$ cm^{-2} in p-Si

With the transmittance 67%, $N_e = 0.67\times9.6\times10^{12}$ cm^{-2} = 6.43×10^{12} cm^{-2}

$N_h = R \times T_h \approx 3.2\times10^{16} \times 100\ \mu s \approx 3.2\times10^{12}$ cm^{-2} in n-si

With the transmittance 67%, $N_e = 0.67\times3.2\times10^{12}$ / cm^2 = 2.14×10^{12} cm^{-2}

Thus, the photo electrons ~ 6.43×10^{12} cm^{-2} contributes charge ~ 1.03×10^{-6} coul/cm^2 at SiO_2/Si interface of p-si.

6.5.2.1 The charge and potential distribution at 5 V reverse bias of p-Si under dark condition

From $$Q_{Si/SiO_2}(\varphi_s) = \varepsilon_s E_s = \frac{\sqrt{2}\varepsilon_s}{\beta L_D}\left[(e^{-\beta\varphi_s} + \beta\varphi_s - 1) + \frac{n_{po}}{p_{po}}(e^{\beta\varphi_s} - \beta\varphi_s - 1)\right]^{1/2}$$

2DES Charge at interface $Q_{2D} \approx Q_{Si/SiO_2} \approx 7\times10^{-7}\, coul/cm^2; \varphi_s \approx 0.89V$

and $$V_G = V_{FB} + V_{oxide} + \varphi_s$$

$$V_G = V_{FB} + \frac{Q_{Si(net\,charge)}}{C_{oxide}} + \varphi_s$$

Thus, $Q_{Si/SiO2} \approx 7.23\times10^{-7}\, coul/cm^2$, $Q_{2D(dark\ inversion)} \approx 7.03\times10^{-7}\ coul/cm^2$,

$Q_{Depletion} \approx 2\times10^{-8}\ coul/cm^2$

At V_G = 5V, $V_{oxide} = 4.19V$, $\varphi_s = 0.89V$, $V_{FB} = -0.08V$, Depletion width ≈ 950 nm

At dark condition/ static steady state $Q_{Si/SiO_2}(\varphi_s) = Q_{2D(dark\ inversion)} + Q_{Depletion}$

Charges in graphene are equal to net charges in Silicon or charge at in the interface

$$Q_{Si(net\,charge)} = Q_{Si/SiO2} = Q_{Graphene}$$

The local electric field at the interface is equal to

$$E_{field(Si/SiO2)} = \frac{Q_{2D(Si/SiO2)}}{\varepsilon_s} = \frac{7.23\times10^{-7}}{11.8\times8.85\times10^{-14}} \approx 6.9\times10^{5}\ \text{V/cm}$$

6.5.2.2 The charge and potential distribution at 5 V reverse bias of p-Si under illumination condition at incident power ~0.1 mW, 633 nm wavelength, 300 μs minority electron life time, 0.67 transmittance

At input power of ~0.1 mW, the photo electrons ~ 6.43×10^{12} cm^{-2} contribute charge ~ 1.03×10^{-6} coul/cm^2 at SiO_2/Si interface. Photocarriers generated in/near the depletion region in Si are separated by the depletion field: minority carriers drift to the oxide interface forming a 2D hole inversion layer while majority carriers (electrons) are driven to the substrate side inducing an external current.

$$Q_{2D(photo\,\text{electron})} = Q_{2D(photohole)} = 1.03\times10^{-6}\,coul/cm^2$$

Photocarriers generated in Si are separated by the depletion field developed in the region under the reverse-biased graphene electrode: minority carriers drift to the oxide interface forming an inversion layer of quasi-2D electronic system (2DES). The total 2D electron gas (2DEG) at SiO_2/Si, thus, will increase as

$$Q_{2D(Si/SiO2)} = Q_{2D(dark\ inversion)} + Q_{2D(photo\,\text{electron})}$$

$$Q_{2D(Si/SiO2)} = 7.03\times10^{-7} + 1.03\times10^{-6} = 1.73\times10^{-6}\,coul/cm^2,$$

From $$Q_{Si/SiO_2}(\varphi_s) = \varepsilon_s E_s = \frac{\sqrt{2}\varepsilon_s}{\beta L_D}\left[(e^{-\beta\varphi_s} + \beta\varphi_s - 1) + \frac{n_{po}}{p_{po}}(e^{\beta\varphi_s} - \beta\varphi_s - 1)\right]^{1/2}$$

To have charge $Q_{2D} \approx 1.7\times10^{-6}\,coul/cm^2$ at the interface the surface potential need to be increase to $, \varphi_s \approx 0.93V$

The photocarrier 2DEG induced at the oxide interface is estimated to be 1.07x10^{13} cm^{-2}. The electric field in the inversion layer reaches a peak value of

$$E_{field(Si/SiO2)} = \frac{Q_{2D(Si/SiO2)}}{\varepsilon_s} = \frac{1.73\times10^{-6}}{11.8\times8.85\times10^{-14}} \approx 1.66\times10^{6} V/cm$$

at the interface with a full-width half-maximum (FWHM) of 2 nm

Being majority carriers, photoholes quickly spread across bulk Si ~525 μm thickness in the time scale of dielectric relaxation and induce an external current along the circuitry. The photohole charges in Si are balanced by the photoelectron inversion charges at SiO_2/Si, therefore the net charge in Si does not increase even after illumination. The total (net) charge in Silicon (equal to charge in the graphene side) can be considered as

$$Q_{Graphene} = Q_{Si(net\ charge)} = Q_{2D(dark\ inversion)} + Q_{Depletion} + \cancel{Q_{2D(photo\ electron)}} - \cancel{Q_{2D(photohole)}}$$

$$Q_{Graphene} = Q_{Si(net\ charge)} = Q_{2D(dark\ inversion)} + Q_{Depletion}$$

Find the amount of net charge in graphene $Q_{Graphene}$ or silicon $Q_{Si(net\ charge)}$ by using the following equation as

$$V_G = V_{FB} + V_{oxide} + \varphi_s$$

$$V_G = V_{FB} + \frac{Q_{Si(net\ charge)}}{C_{oxide}} + \varphi_s$$

At 0.1 mw with 5V reverse bias, $Q_{2D} \approx 1.73\times10^{-6} coul/cm^2, \varphi_s \approx 0.93V$

$$V_G = 5V,\ V_{oxide} = 4.15V,\ \varphi_s = 0.93V,\ V_{FB} = -0.08V,$$

$$Q_{Si(net\ charge)} = \frac{V_{oxide}\times\varepsilon_{oxide}}{t_{oxide}} = \frac{4.15V\times3.9\times8.85\times10^{-14}}{20\times10^{-7}} = 7.16\times10^{-7} coul/cm^2$$

The net charge in silicon or graphene will be reduced with the negligible amount during photo application. The amount of net charge in Silicon that needs to be reduced is

$$\Delta Q_{Si(net\ charge)} = Q_{Si(net\ charge)} dark - Q_{Si(net\ charge)} photo$$

$$\Delta Q_{Si(net\ charge)} = 7.23\times10^{-7} - 7.16\times10^{-7} = 7\times10^{-9}\, coul/cm^2$$

However, if we assume only depletion charge was adjusted during photo application; the depletion charge during photo application can be found as

$$Q_{Depletion}\, photo \approx Q_{Depletion}\, dark - \Delta Q_{Si(net\ charge)} \approx 2\times10^{-8} - 7\times10^{-9} \approx 1.3\times10^{-8}$$

Therefore, we can estimate the new depletion width form

$$Q_{Depletion} \approx qN_A W_D\,;\ W_D \approx 620 \text{ nm}$$

Note that the band bending in bulk Si remains negligible even with presence of photohole charges there. This is because the photohole concentration in bulk Si ~$1.2\text{x}10^{14}$ cm^{-3} is far below the background level ~$1.32\text{x}10^{15}$ cm^{-3}

6.5.3 Impact ionization in 2DES

6.5.3.1 Impact ionization in silicon

The ionization rate α is defined as the number of electron-hole pairs generated by a carrier per unit distance travelled. It is different for electrons ($\alpha_{n,}$) and for holes (α_p). In general, the ionization rates depend on the probability for the carriers to reach the local electrical field to gain at least the threshold energy for ionization. An empirical expression model of local avalanche generation model in which the ionization rate depends only on the local electrical field was used [113].

$$\alpha_{n,p} = A_{n,p} \exp(-b_{n,p} / \mathrm{E})$$

with: For electrons $A_n = 7.03 \times 10^5 \ cm^{-1}$

$b_n = 1.231 \times 10^6 \ V \ cm^{-1}$

$or \ 1.75 \times 10^5 \le E \le 6.0 \times 10^5 \ V \ cm^{-1}$

For holes $A_n = 1.582 \times 10^6 \ cm^{-1}$

$b_n = 2.036 \times 10^6 \ V \ cm^{-1}$

$for \ 1.75 \times 10^5 \le E \le 4.0 \times 10^5 \ V \ cm^{-1}$

And $A_n = 6.71 \times 10^5 \ cm^{-1}$

$b_n = 1.693 \times 10^6 \ V \ cm^{-1}$

$for \ 4.0 \times 10^5 \le E \le 6.0 \times 10^5 \ V \ cm^{-1}$

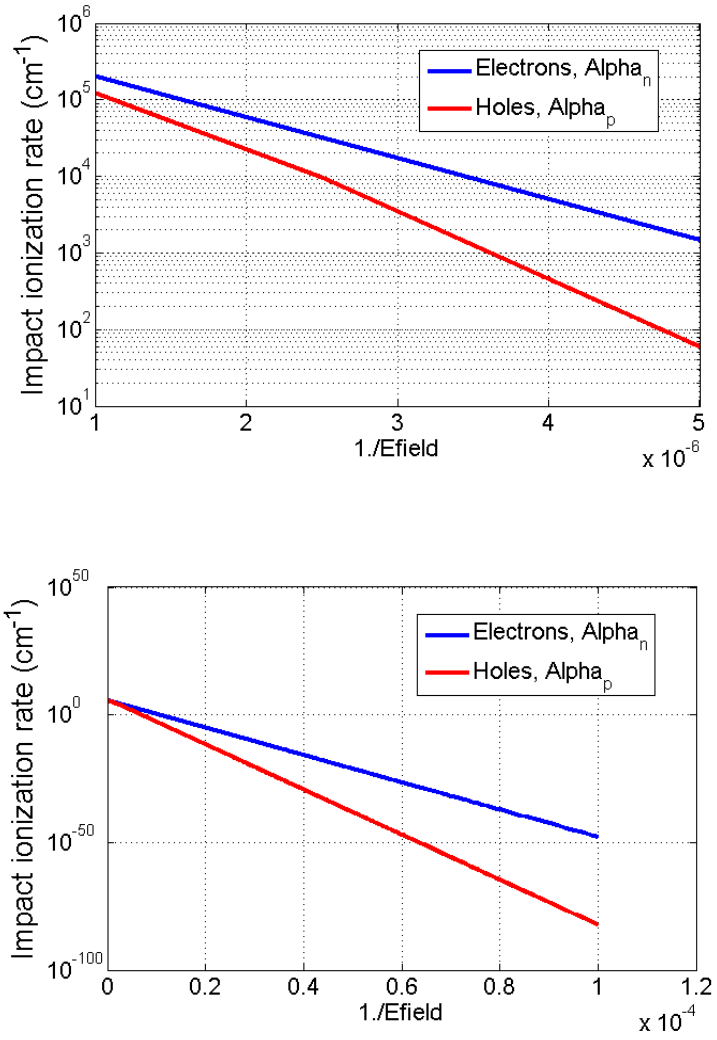


Figure 48 Ionization rates of electron and hole in function of the reciprocal of the electric field. (a) 2: Ionization rates electron- and hole for intermediate-high electric field range ($2 \times 10^5 \leq E \leq 1x\ 106$ V cm^{-1}) (b) Ionization rates of electron and hole for low-high electric field range ($1 \times 10^4 \leq E \leq 2x\ 10^6$ V cm^{-1})

The ionization rate and the multiplication factor together with their interrelationship are defined [109]. For electrons, as incident carriers initiating the multiplication process:

$$1-\frac{1}{M_n}=\int_0^W \alpha_n e^{-\int_0^x (\alpha_n-\alpha_p)dx'} dx$$

For holes, as incident carriers:

$$1-\frac{1}{M_p}=\int_0^W \alpha_p e^{\int_0^x (\alpha_n-\alpha_p)dx'} dx$$

6.5.3.2 Calculation of impact ionization/carrier multiplication under illumination

In this work, the ionization coefficients and multiplication factor cannot be obtained analytically when the electrical field is not constant *i.e.*, the electrical field as a function of distance. In addition, the electron and hole ionization coefficients are always appearing together in the equation even when the injected current is of only one type. The numerical calculation of the integral can be simplified by using curve fitting method.

The photocarrier 2DEG induced at the oxide interface is estimated to be 1.08×10^{13} cm^{-2}. The electric field in the inversion layer reaches a peak value of 1.66×10^{6} V/cm at the interface. Since the strong electric field is narrowly confined in the inversion layer (~2 nm), carrier multiplication occurs in the highly localized area. This implies that most of photocarriers contributing to a photocurrent can experience carrier multiplication in the inversion layer.

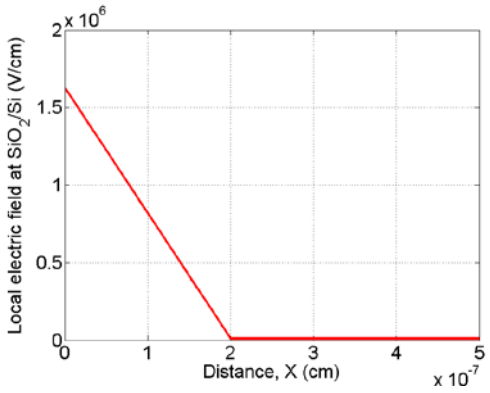
The depletion charge was reduced since the depletion width was shrunk to ~ 620 nm. The depletion maximum electric field, $E_{depletion}$ is ~ $\frac{Q_D}{\varepsilon_{si}} \approx \frac{qN_A W_D}{\varepsilon_{si}}$

$$\approx \frac{1.6 \times 10^{-19} \times 1.32 \times 10^{15} \times 620 \times 10^{-7}}{11.8 \times 8.854 \times 10^{-14}} \approx 1.24 \times 10^{4} V / cm$$

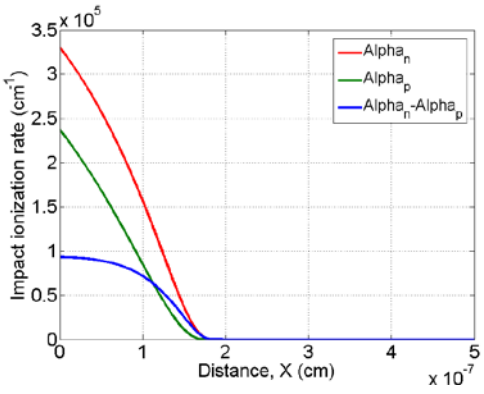
Therefore, The local electric field at interface is ~ 1.66×10^{6} V/cm, and then sharply decreases to depletion maximum electric field ~ 1.24×10^{4} in ~ 2 nm inversion width. (Fig 49a)

GOS-p-si photo-detector at 5V operation, 633 nm 0.1 mW, 0.67 transmittance, 300 µs minority carrier life time

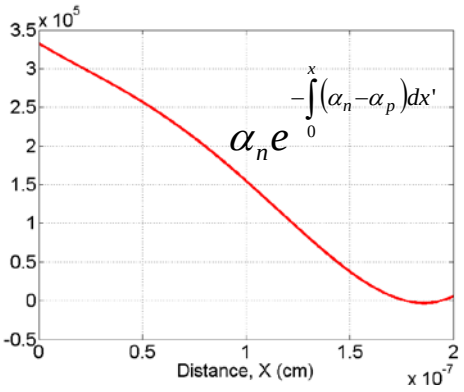
a



b



c



$$\int_0^W \alpha_n e^{-\int_0^x (\alpha_n - \alpha_p)dx'} dx = 0.031$$

$$M_n = \left[\frac{1}{1 - \int_0^W \alpha_n e^{-\int_0^x (\alpha_n - \alpha_p)dx'} dx} \right] = \left[\frac{1}{1 - 0.031} \right] = 1.032$$

Figure 49 (a) The electrical field as a function of distance. (b) The electron and hole ionization coefficients (c) The numerical calculation of the integral can be simplified by using curve fitting method.

Table 3. GOS-p-si photo-detector at 5Vreverse bias operation, 633 nm, 0.67 transmittance

Power	**dark**	**0.1 mW**	**0.75 mW**	**1.0 mW**	**unit**
Electron carrier life time	**-**	**300 µs**	**300 µs**	**300 µs**	µs
photo carrier charges	-	1.03×10^{-6}	7.7×10^{-6}	1.03×10^{-5}	coul/cm^2
$Q_{2D(Si/SiO2)}$	$\approx 7.23\times10^{-7}$	1.73×10^{-6}	8.4×10^{-6}	1.1×10^{-5}	coul/cm^2
Local $E_{field(Si/SiO2)}$	6.9×10^{5}	1.66×10^{6}	8.04×10^{6}	1.05×10^{7}	V/m
Depletion width	$\approx$ 950 nm	620	0	N/A	nm
Multiplication factor of **2 nm** inversion layer	**-**	**1.032**	**1.10**	**1.11**	**-**

Table 4. GOS-n-si photo-detector at 5V reverse bias operation, 633 nm, 0.67 transmittance

Power	**dark**	**0.1 mW**	**1.0 mW**	unit
hole minority carrier life time	**-**	**100 µs**	**100 µs**	µs
photo carrier charges	-	3.424×10^{-7}	3.424×10^{-6}	coul/cm^2
$Q_{2D(Si/SiO2)}$	$\approx 7.07\times10^{-7}$	1.05×10^{-6}	4.13×10^{-6}	coul/cm^2
Local $E_{field(Si/SiO2)}$	6.8×10^{5}	1.01×10^{6}	4×10^{6}	V/m
Multiplication factor of **2 nm** inversion layer	**-**	**$\approx$ 1.01**	**$\approx$ 1.053**	-

Table 5 Summary table of GOS-p-si photo-detector at 5V operation, 633 nm 0.1, 0.5 mW, 0.67 transmittance, 300 us minority carrier life time

Status	Dark	0.1 mW	0.75 mW	unit
Electron life time		**300 us**	**300 us**	
(photo) electrons	-	6.42×10^{12}	4.81×10^{13}	cm^{-2}
(photo) electron charges	-	-1.03×10^{-6}	7.7×10^{-6}	$coul/cm^2$
(photo) holes	-	6.42×10^{12}	4.81×10^{13}	cm^{-2}
(photo) hole charges	-	1.03×10^{-6}	7.7×10^{-6}	$coul/cm^2$
V_G	5	5	5	V
V_{FB}	~ -0.08	~ -0.08	~ -0.08	V
V_{oxide}	~ 4.19	~ 4.15	~ 4.07	V
Surface potential, Vsi or (φ_S)	~ 0.89	~ 0.93	~ 1.01	V
Electrons at SiO_2/Si, n_{2D}	$\approx 4.39\times10^{12}$	1.08×10^{13}	5.25×10^{13}	cm^{-2}
Electrons charge at SiO2/Si, qn_{2D} or $Q_{2D(Si/SiO2)}$	$\approx 7.03\times10^{-7}$	1.73×10^{-6}	8.4×10^{-6}	$coul/cm^2$
$E_{field(Si/SiO2)}$	6.9E5	1.66×10^{6}	8.04×10^{6}	V/m
net charge in Silicon, Q_{Si}	$\approx 7.23\times10^{-7}$	$\approx 7.16\times10^{-7}$	$\approx 7.03\times10^{-7}$	$coul/cm^2$
2DHS in the graphene side	4.51×10^{12}	4.48×10^{12}	4.4×10^{12}	
$Q_{Si(dark)} - Q_{Si(photo)}$	-	$\approx 7\times10^{-9}$	$\approx 2\times10^{-8}$	$coul/cm^2$
Depletion charge	$\approx 2\times10^{-8}$	$\approx 1.3\times10^{-8}$	~0	$coul/cm^2$
Depletion width	≈ 950	≈ 620	≈ 0	nm
Multiplication factor 2 nm inv layer	-	≈ 1.032	≈ 1.10	

6.5.4 Conclusion

The saturation photocurrent corresponds to the photocarrier generation rate in Si, expressed as $qηPin/hν$, where q is the electron charge, η is the external quantum efficiency, Pin is the power incident to graphene electrode, and hν is the photon energy. Assuming a minority carrier (electron) lifetime of 300 μs [107] and photogeneration rate of ~$2.14x10^{16}$ $cm^{-2}s^{-1}$ for 0.1 mW at 633 nm wavelength in p-Si, the photocarrier 2DEG induced at the oxide interface is estimated to be $1.08x10^{13}$ cm^{-2}. The electric field in the inversion layer reaches a peak value of $1.66x10^{6}$ V/cm at the interface with a full-width half-maximum (FWHM) of 2 nm [108]. In the case of n-Si sample under the same illumination condition, the photogenerated 2DHS is estimated to be ~$6.6×10^{12}$ cm^{-2}. The peak value and FHWM of field distribution in the inversion layer are calculated to be ~$1.01x10^{6}$ V/cm and 2 nm, respectively.

The impact ionization rates and carrier multiplication factors [109] were then calculated from the field distributions (Fig. 47). The carrier multiplication is estimated to be 1.03 for p-Si and 1.01 for n-Si at 0.1 mW input power of 633 nm light. Since the strong electric field is narrowly confined in the inversion layer (< 2-3 nm), carrier multiplication occurs in the highly localized area. This implies that most of photocarriers contributing to a photocurrent can experience carrier multiplication in the inversion layer. In the UV-visible range (< 700 nm) the internal quantum efficiency without a carrier multiplication effect is calculated to be 97-99.9%. When taking into account this impact ionization effect in the inversion layer, the responsivity is multiplied by the carrier multiplication factor, and the IQE is increased by the same factor (1.03 for p-Si and 1.01 for n-Si). The measurement results in the visible range (400-650 nm) show a reasonable agreement with this model calculation (Fig. 46). In the shorter wavelength range (< 400 nm), the measured responsivity and quantum efficiency values show significantly larger

numbers (IQE at 325 nm approaching 144% in p-Si and 135% in n-Si). The enhanced efficiency at UV is ascribed to the carrier multiplication process involving the direct bandgap transitions (Γ-point transition at 3.4 eV) [98, 99].

6.6 THE POWER DEPENDENCE OF CARRIER MULTIPLICATION FACTOR IN THE 2D INVERSION LAYER

According to the model discussed above the carrier multiplication factor should depend on peak field strength in the 2D inversion layer. In other words, the multiplication factor is expected to increase when the light intensity is increased. At 1.0 mW input power, for example, a model calculation estimates that the maximum field increases to1.05×10^7 V/cm for p-Si and 4×10^6 V/cm for n-Si, and the multiplication factor becomes 1.11 or 1.05, respectively. In order to test this model prediction, we measured the power dependence for input power in the range of 0.1 mW to 1.5 mW at 633 nm wavelength. The internal quantum efficiency rises to 132% for 0.1 mW - 0.5 mW and then gradually saturates at 175 % for 1.0 mW or higher. The measurement result shows a reasonable agreement with model calculation. At ~0.8mW or beyond, the depletion width is reduced to zero. Photoelectrons and holes, however, remain separated, since newly generated photoelectrons constantly exit the system. This enables a continuous operation of photocarrier separation and photocurrent flow at steady state. This is contrasting to the case of the sample without a nano-void channel (i.e., without constant emission of 2DEG into air). In the latter case the photoelectrons and holes would recombine when the depletion region diminishes to zero, and the photocurrent flow would eventually discontinue [96, 110, 111].

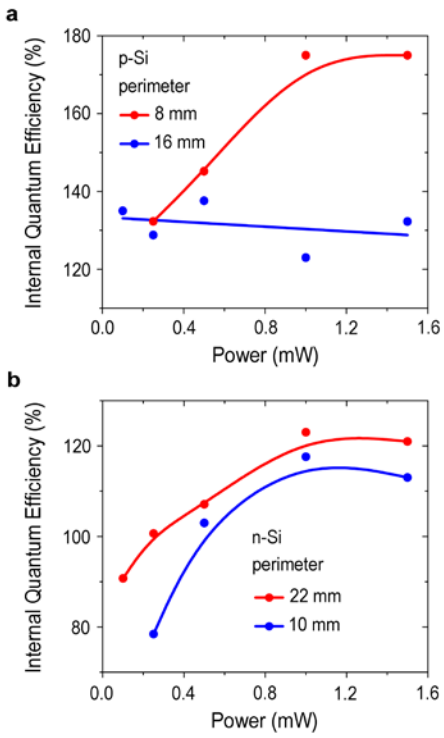


Figure 50 The power dependence of internal quantum efficiency of p-Si (a), n-Si (b)

Lastly we consider the dependence of photo *I-V* characteristic on void-channel perimeter. For a given input power, the saturation photocurrent is independent of channel perimeter. The saturation voltage, however, decreases for larger perimeter. This is because the 2DEG emission is through edges, therefore the channel current is proportional to the total edge length (channel perimeter). Being governed by a space-charge-limited emission process, the total emission can reach the saturation level at lower voltage for larger perimeter. The average density of 2DEG is expected to decrease as the channel perimeter is increased. This effect is then expected to reduce the multiplication factor therefore responsivity and quantum efficiency. In order to test this perimeter dependence, samples with widely varying perimeters were prepared (Fig. 50). For p-Si, the longer perimeter sample shows lower quantum efficiency compared to the smaller perimeter sample (~130 % versus ~170 %). For n-Si case no such dependence was observed. The different perimeter dependence can be explained by that in p-Si the emission of 2DEG is enhanced by the space charge cancellation effect of hole charges on the suspended grapheme. In n-Si case, however, there is no such enhancement and therefore no strong dependence on perimeter.

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