DIRECT DC SOLAR INTEGRATION

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The output characteristic of a photovoltaic (PV) module varies as the environmental conditions of the module's operation change. Changes in operating temperature and incident sunlight dynamically change the maximum power available from a PV module, as well as the output voltage. The output voltage of the PV generating system must be regulated, in order to ensure proper power quality for connection to an electrical load, building electric power system, or the electric grid.

PV modules are typically connected in series strings and parallel arrays to create PV generating systems. Non-uniform environmental conditions create voltage mismatches throughout PV generating systems. A mismatch between module voltages can severely reduce the amount of power available from the overall generating system. These system losses can be eliminated by regulating the output voltage of each module.

This dissertation proposes a power electronic device that fulfills two objectives: extracting maximum power from the single PV module, and regulating the output voltage to ensure a constant value. This dissertation reviews the analytical design of such a system, and validates this design in simulation, utilizing MATLAB/SIMULINK and ANSYS Simplorer.

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1.0 INTRODUCTION

This dissertation describes the design of a distributed power electronics device used for integrating photovoltaic (PV) generation into DC electrical systems. The operation of this distributed converter is analogous to the functions performed by a micro-inverter, for integrating PV generation into an AC electrical system.

A micro-inverter eliminates the need to connect PV modules in series and parallel to create strings and arrays. Instead, all modules can be connected in parallel at the point of common coupling with the AC network [1]. The micro-inverter performs maximum power point tracking (MPPT) on each individual module, and regulates the output voltage from each module [1]. These two features act to minimize the effects of partial shading on the system performance, and to eliminate the mismatch losses in the system [1]. The use of micro-inverters results in PV generating systems with higher utilization, and lower system losses.

The benefits of micro-inverters have been realized, through this work, for systems utilizing DC electrical distribution infrastructure. The designed power electronics system, henceforth referred to as a micro-converter, performs the tasks of MPPT and voltage regulation, producing a DC output, as opposed to an AC sine wave.

This design is accomplished through the cascaded connection of two power electronic sub-systems: a boost converter that performs MPPT, and a Cuk converter that performs voltage

regulation. Cascaded converter systems often suffer from interactions which can lead to system instability. In this work, the stability of the cascaded system is considered

The system is designed and analyzed analytically through the application of power electronics theory, AC equivalent circuit modeling, and linear control theory. The analytical model of the circuit predicts stable operation over the expected operating range of the system. The stability of the system is validated through simulation, using the MATLAB/SIMULINK software environment, in combination with Ansys/Simplorer. Simulation results show that the physical circuit behaves in accordance with the predictions made by the mathematical model.

2.0 BACKGROUND AND SIGNIFICANCE

The United States Department of Energy (DOE) Sunshot program was formulated with the goal of making unsubsidized solar generation economically competitive in the country's electrical supply [2]. When the program was first formulated, the installed cost of utility-scale photovoltaic (PV) generation was $8/W. In order to become cost competitive, the price of solar must drop to $1/W installed [3]. Figure 1 demonstrates the cost reductions required in order for this to be achieved.

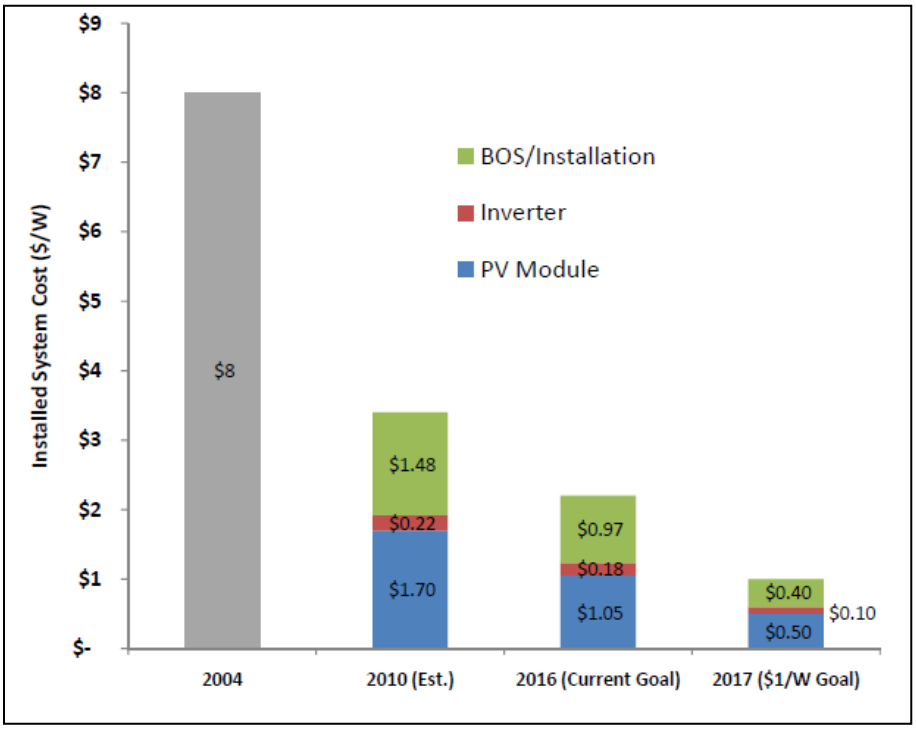

Figure 1: DOE Sunshot Goals [3]

Since 2008, the market price for solar panels has declined significantly, from a starting price near $4/W, to an end price near $1.00/W at the end of 2012 [4]. Figure 2 shows the overall trend.

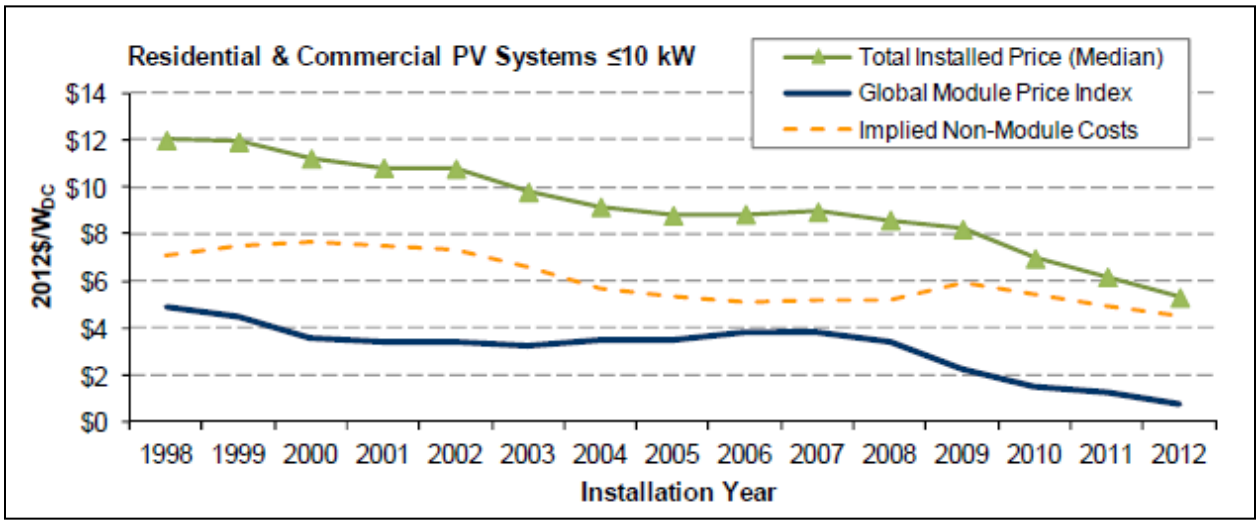

Figure 2: Global PV Module and Installed Price Trends [4]

The drop in panel prices has been so significant as to cause a shift in the cost reduction efforts related to PV technology. Figure 3 shows the installed cost for solar, in every market sector, during the last quarter of 2011, and again during the last quarter of 2012. As shown, at the end of 2012, the majority of the costs for PV installations was attributed to the balance-of-system costs, due to the sharp reduction in the price of panels.

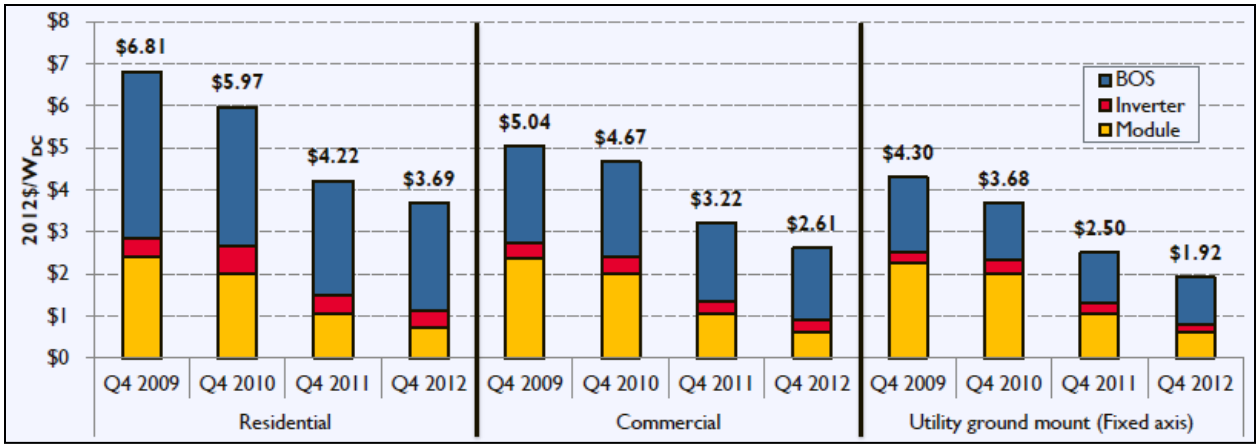

Figure 3: Installed Cost by Sector [4]

Table 1 shows a breakdown of the hardware costs for a PV installation in 2011. At that time, the PV panels accounted for roughly 2/3 of the installed hardware costs [4]. Holding all other hardware costs constant, and adjusting for the market price of PV panels ($0.7/W as of October 2013), PV panels account for only 39% of the system hardware costs [5].

Table 1: PV Hardware Costs [4]

Material Category	Component costs[13] (per $W_{P\,DC}$)	Installation labor allocation requirements			
		Units/system	Units	Electrical (hr/unit)	General (hr/unit)
Module	$2.05[14]	914	Modules	0.43	
Inverter	$0.37	1	Inverters	16.0	16.0
Wiring	$0.02	6,164[15]	Linear ft	0.08	
Other electrical[16]	$0. 74	1	Electrical subsystem	111	
Mounting hardware	$0.06	914	Modules		
Stage project	$0.00	1	None		36.6
	$3.21				
Total Installation Labor Requirements (hr/system):				1,010.1	52.6

In this dissertation, I present a method for further reducing the hardware costs associated with PV installations. Figure 4 shows the hardware involved in a residential or commercial PV installation. Comparing the 'Other electrical' category from Table 1 to the picture in Figure 4, one can see that the remaining hardware consists primarily of protection equipment for the AC and DC stages of the system (the mounting equipment is not shown). By eliminating the AC stage of the PV integration process, roughly half of the 'Other electrical' and wiring costs become obsolete. Furthermore, the cost of the inverter disappears as well. Integrating PV generation directly into a DC distribution network immediately eliminates nearly 40% of the hardware costs associated with PV integration.

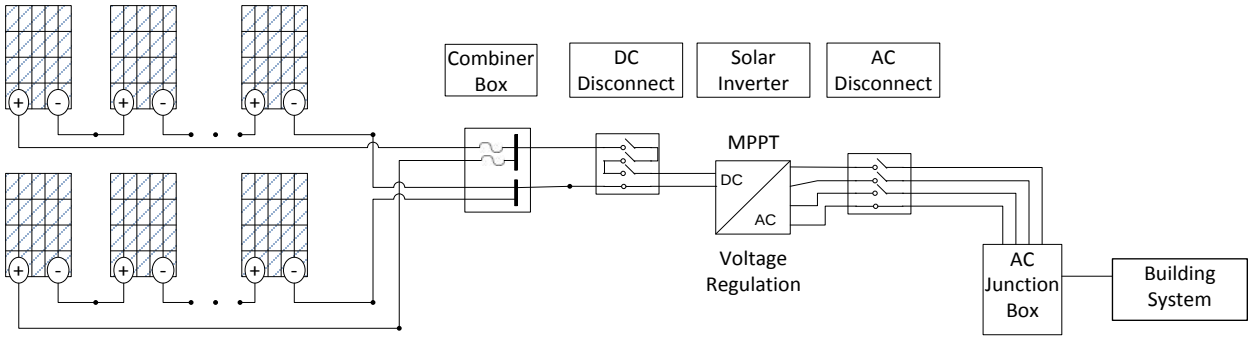

Figure 4: Equipment for Solar Installation

In place of the obsolesced equipment, I recommend utilizing the introduced micro-converter. Additional protection equipment, like a DC circuit breaker, may be recommended or mandated by electrical code. The combined cost of the DC equipment still presents a significant savings potential, compared to the equipment used in the standard AC system.

2.1 APPLICATION CONTEXT: DATACENTERS

Datacenters are physical facilities that house information technology (IT) equipment [6]. The main function of the datacenter is to provide reliable power, security, cooling, and network connectivity to computer equipment [7]. Compared to the electrical loads which have traditionally dominated the electric grid, IT equipment is more sensitive to fluctuations in the electric power supply [8]. Given the sensitivity of the equipment, datacenter facilities have strict requirements for their design and operation [6]. Many studies have shown the merits of using DC distribution within data centers, to improve reliability, efficiency, capital costs, and the utilization of space [8][9][10].

Since 2006, almost 30 DC data center projects have been built worldwide, ranging in size from 10 kW to 1 MW. Table 1 summarizes the known projects that have been built to date.

Table 2: Data Center Projects to Date [Unpublished]

	DC DATACENTER PROJECT LISTING				
	SYSTEM / PROJECT	POWER RATING(kW)	Voltage (V)	Year	LOCATION
1	Gnesta Municipality	9	350/380	2006	Gnesta, Sweden
2	Elicom	4.5	350	2006	Toreboda, Sweden
3	NTT NEDO Project	20	380	2007	Sendai, Japan
4	NTT University Microgrid	50	380	2007	Aichi, Japan
5	France Telecom	31.5	350/380	2007	Lannion, France
6	Ericsson	4.5		2008	Stockholm, Sweden
7	Soderhamm Teknikpark	6	350/380	2008	Soderhamn, Sweden
8	NTT Data Corp.	100	380	2009	Tokyo, Japan
9	NTT Lab.	100	380	2009	Tokyo, Japan
10	NTT Facilities	100	380	2009	Tokyo, Japan
11	Compare Test Lab	4.5		2009	Hammaro Karlstad, Sweden
12	Korea Telecom		300/380	2009	Seoul, Korea
13	UCSD	20	380	2009	San Diego, California
14	Syracuse University	150	380	2009	Syracuse, New York
15	Swedish Energy Agency	18	350	2010	Eskilstuna, Sweden
16	Compare Test Lab	500	350	2010	Hammaro Karlstad, Sweden
17	Duke Energy	30	380	2010	Charlotte, North Carolina
18	NTT East	100	380	2010	Tokyo, Japan
19	NTT	100	380	2011	Atsuigy City, Japan
20	Intel		400		
21	Validus		550		
22	China Telecom		240/380		
23	China Mobile		380		
24	ABB - Green	1000	380	2012	Zurich, Switzerland

DC data centers provide a context for direct DC solar integration. This idea has been proposed by others in the past [11]. Figure 5 shows one suggested architecture.

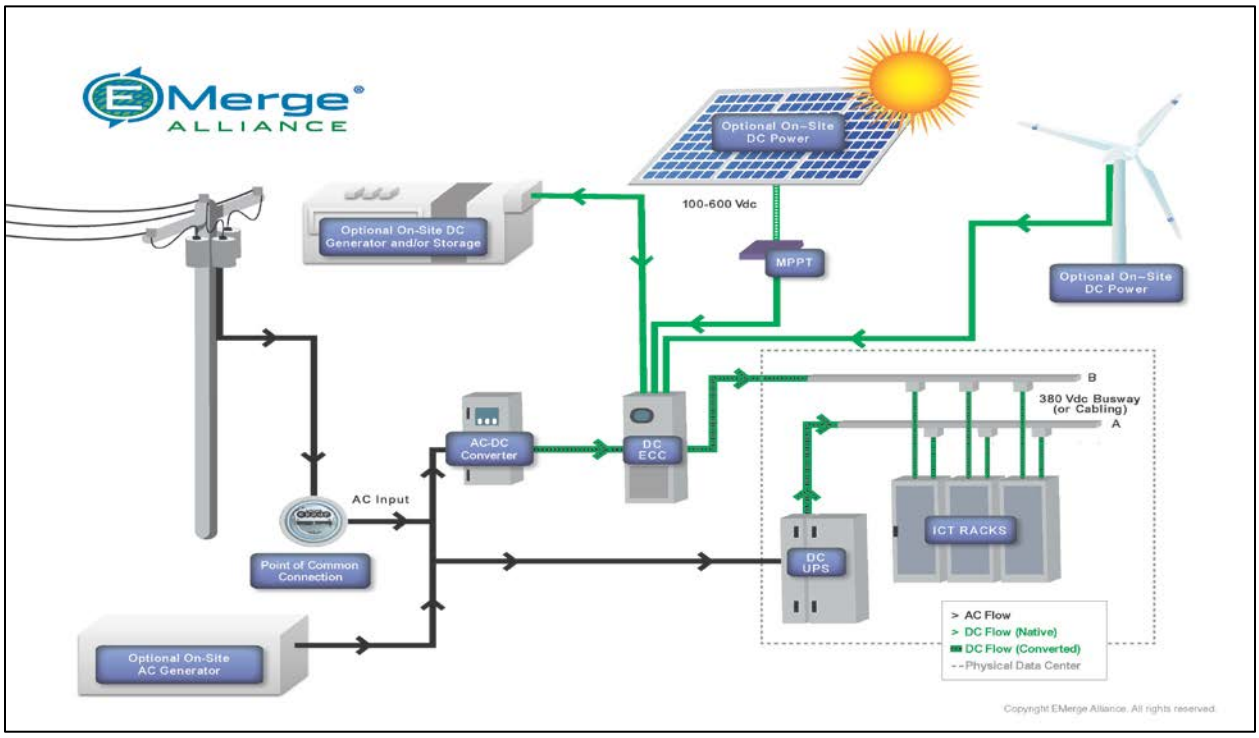

Figure 5: Concept for DC Solar Integration [8]

Although data centers are highlighted as an application area in this dissertation, there are many more possibilities. The 380V DC standard is rapidly emerging as a relevant architecture for telecom sites, for independent micro grids, and for military applications [12][13][14].

3.0 PROBLEM STATEMENT

This dissertation addresses the problem of effectively integrating PV generation into a DC electrical distribution network. Before determining an appropriate technical approach, the objectives of PV integration must be described. This section describes the two main objectives of PV integration, namely, maintaining a constant interconnection voltage, and extracting the maximum amount of available power from the installed PV modules. This section also describes some of the difficulties involved in performing these tasks, which include the effects of partial shading, and mismatch losses. This section describes the tasks which need to be accomplished, and the difficulties which need to be eliminated, in order to effectively integrate PV generation into a DC electrical network.

3.1 REGULATION OF THE INTERCONNECTION VOLTAGE

In mature electrical networks, like the US electric grid, power quality is well defined [15]. Electricity suppliers are expected to supply a constant voltage supply to their customers (in most cases, a constant RMS value for an AC supply), with minimal fluctuations in the supply voltage magnitude. The output voltage of a PV module can change, given the environmental conditions of the module's operation. The output voltage must be regulated to ensure proper power quality at the point of interconnection with the larger electrical system.

Figure 6 and Figure 7 show the way in which a PV module I-V characteristic changes with environmental conditions. When the operating temperature, or solar insolation level, of the module vary, the open circuit voltage and short circuit current change in magnitude. Despite these changes, the interconnection voltage (output voltage of the aggregated PV generation system) must remain constant.

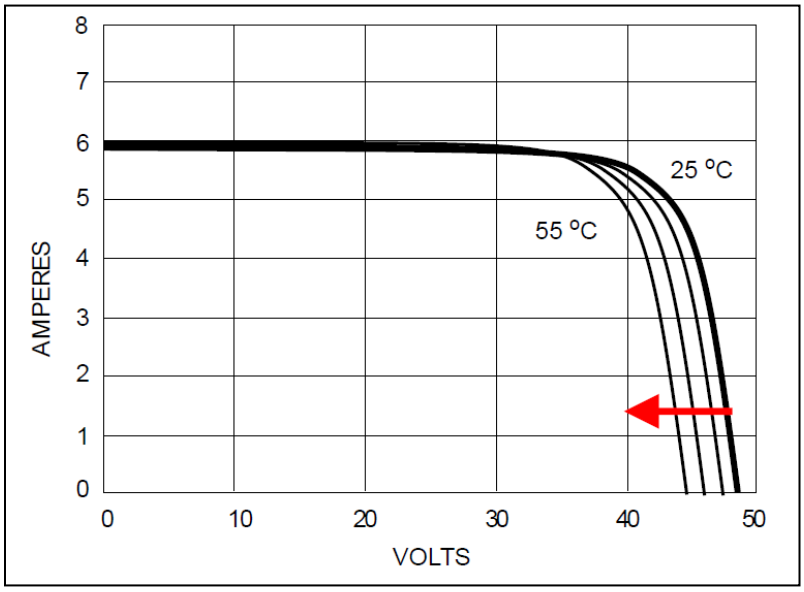

Figure 6: Module I-V Characteristic as a Function of Temperature [16]

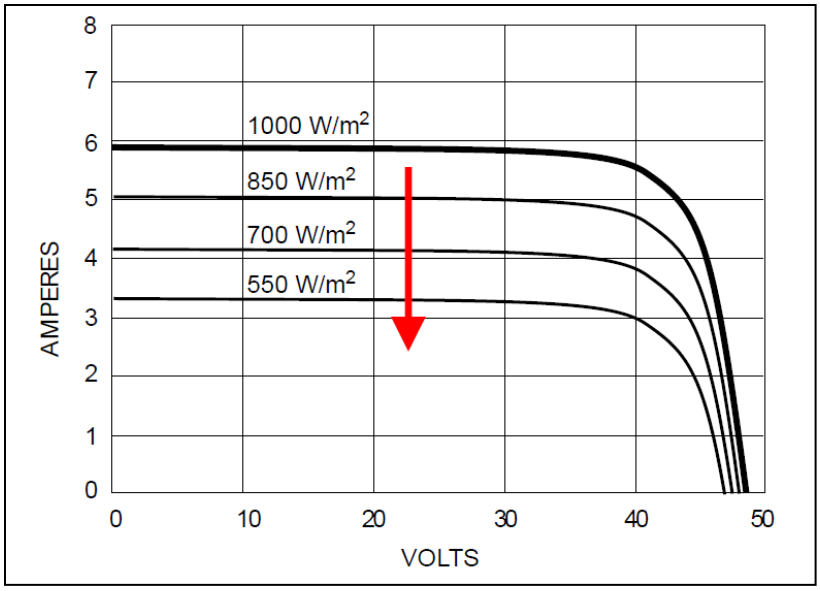

Figure 7: Module I-V Characteristic as a Function of Insolation [16]

3.2 OPTIMIZING POWER EXTRACTION

As environmental conditions change, and the I-V characteristic of the PV module changes, the power available from the module changes as well. Figure 8 and Figure 9 show the way in which the P-V characteristic of a PV module changes with temperature and insolation, respectively.

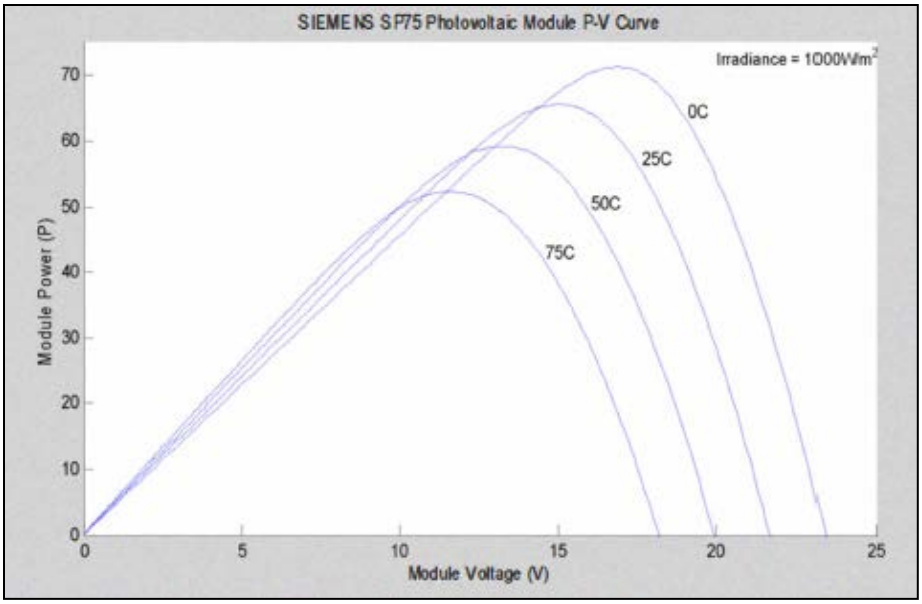

Figure 8: Module P-V Characteristic as a Function of Insolation [17]

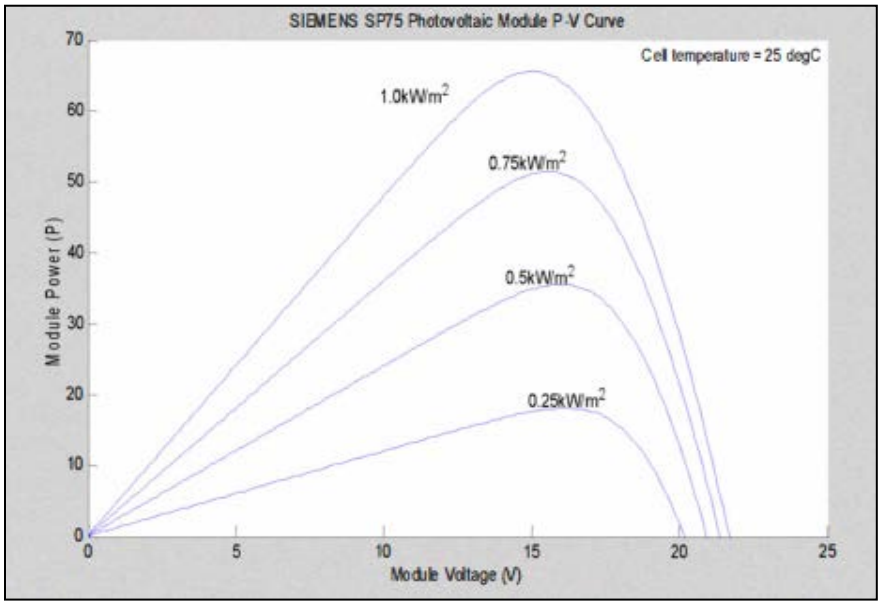

Figure 9: Module P-V Characteristic as a Function of Temperature [17]

Note that these power characteristics are parabolic in nature. Given specific environmental conditions (operating temperature and insolation), there is always one unique operating point

(module output voltage and current) that produces the most power from the PV module. This unique point is referred to as the maximum power point (MPP).

When a constant impedance load is connected to a PV module, or array of modules, the system assumes a particular operating point, dictated by the intersection of the constant impedance load line, and the system I-V characteristic. An example I-V characteristic with a load line is shown in Figure 10.

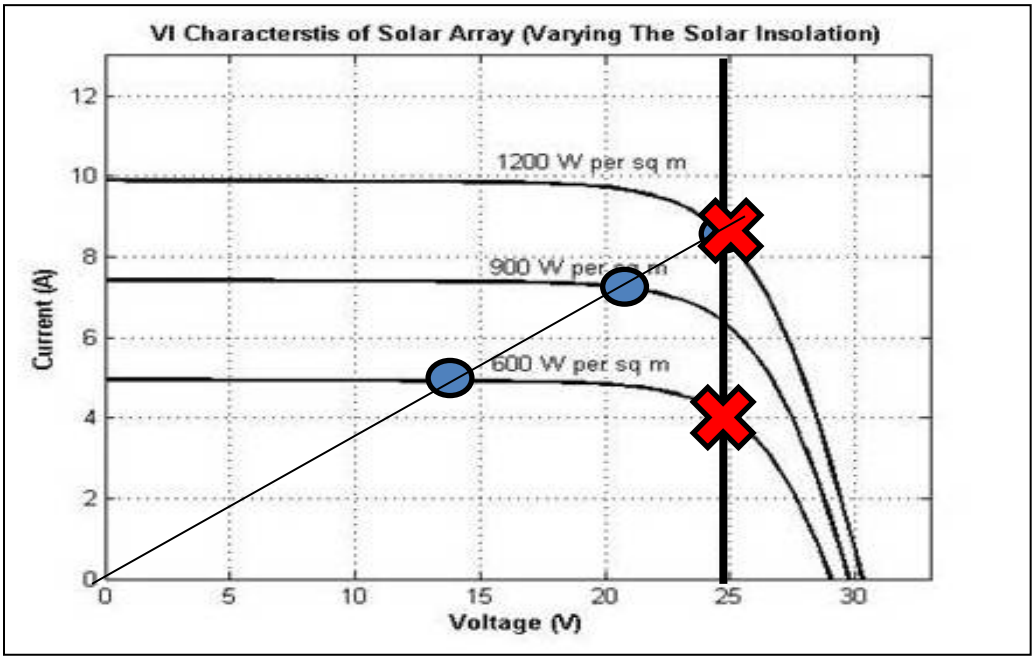

Figure 10: Illustration of MPPT

In Figure 10, the vertical black line represents the voltage corresponding to the maximum power point of the array. The blue circles represent the natural operating points of the system. At various levels of solar intensity, the system voltage and current will change. If the system originally operates at 1200 W/sq-m of light intensity, the load will operate at the MPP of the PV module. If the light intensity suddenly drops to 600 W/sq-m (do to a passing cloud, for instance),

the system voltage will drop to near 15 V, and the current to 5 amps. The large red X indicates that the module has the potential to produce 4 amps at 25 V, 25% more power than the production at its natural operating point. In practice, PV modules and loads are buffered by feedback-controlled power electronic systems that maintain the system operating at the MPP. This active regulation at the MPP is referred to as maximum power point tracking (MPPT). Figure 11 demonstrates the concept of a MPPT system.

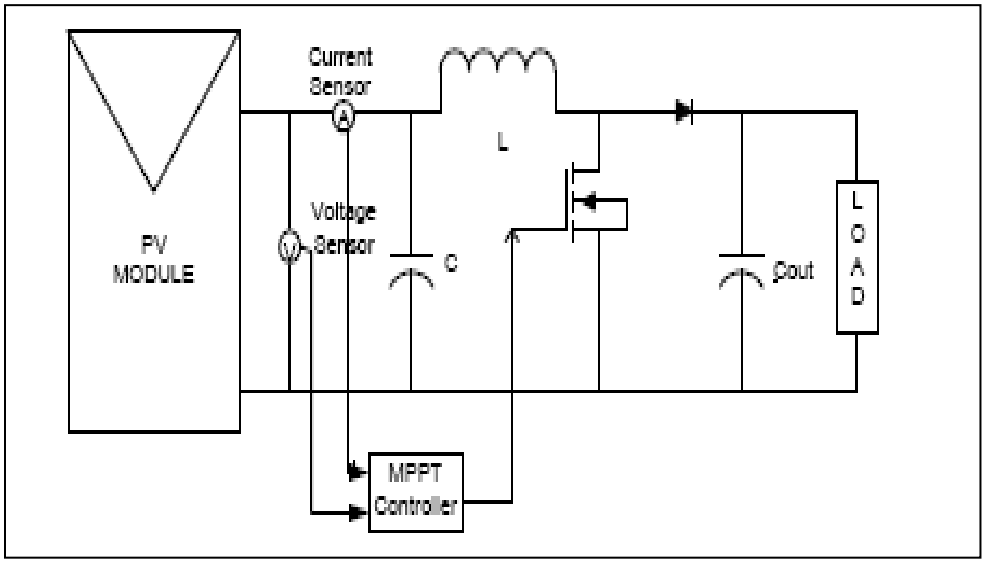

Figure 11: MPPT Hardware Implementation [16]

3.3 PARTIAL SHADING

Maximum power point tracking becomes more complicated under partial shading conditions. Partial shading describes a time period in which a portion of a PV module experiences diminished illumination, compared to other sections of the same module. This can be the result of clouds slowly passing by, or nearby obstructions such as trees and buildings. Regardless of the

cause, partial shading can have profound effects on the amount of power produced from a PV generation system.

A 2013 study by the National Renewable Energy Laboratory (NREL) sought to quantify the effects of partial shading of PV system power production [18]. The example system used by NREL is shown in Figure 12 below.

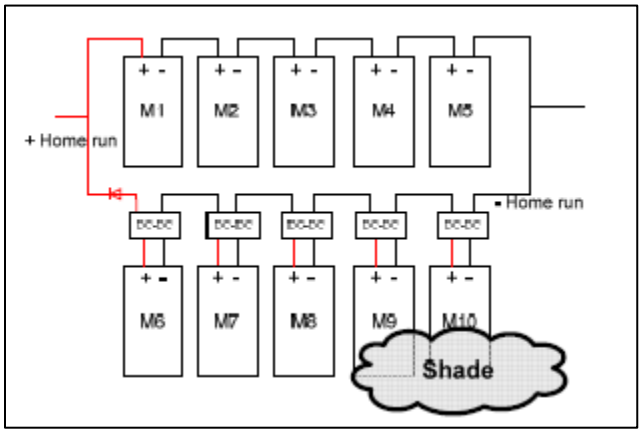

Figure 12: NREL Partial Shading Study System Diagram [18]

The study showed that shading a panel by as little as twenty percent was enough to reduce the power output of the module by 40 percent [18]. Figure 13 shows the shading versus power reduction characteristic.

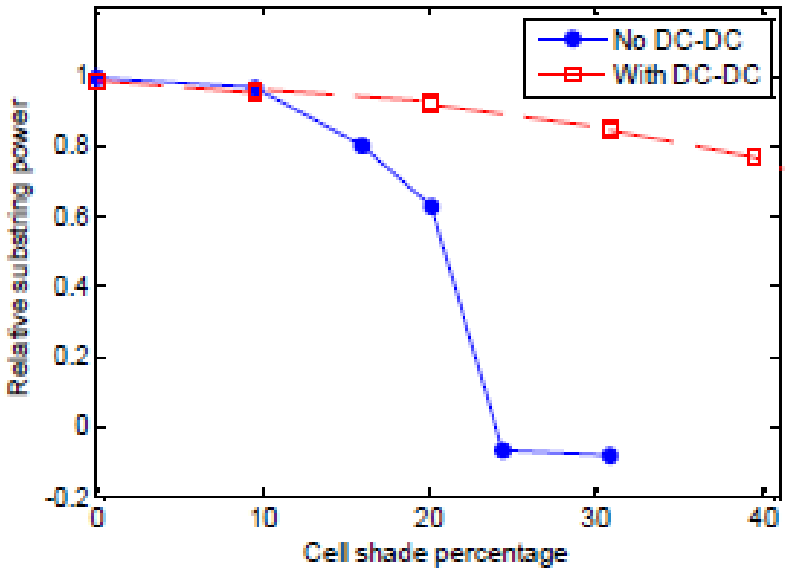

Figure 13: Effect of Cell Shading on Power Production Reduction [18]

Solar panel manufacturers are familiar with this and have included bypass diodes in the PV modules that they sell. Typically, commercial modules contain up to 72 solar cells, wired in series [18]. Panel manufacturers tend to group these cells in sub-modules consisting of 12 – 24 cells, paralleled by a bypass diode [18]. Commercial modules may contain one, two, or three bypass diodes [18].

Bypass diodes effectively partition a PV module into distinct, separate sub-modules [19]. Under partial shading conditions, one sub-module can continue to produce power, while the other module is bypassed through the paralleling diode [19]. This changes the nature of the P-V characteristic, while the module is partially shaded. Figure 14 below shows the effect that partial shading has on a module with two bypass diodes. In effect, two P-V characteristics are produced, corresponding to the two sub-modules.

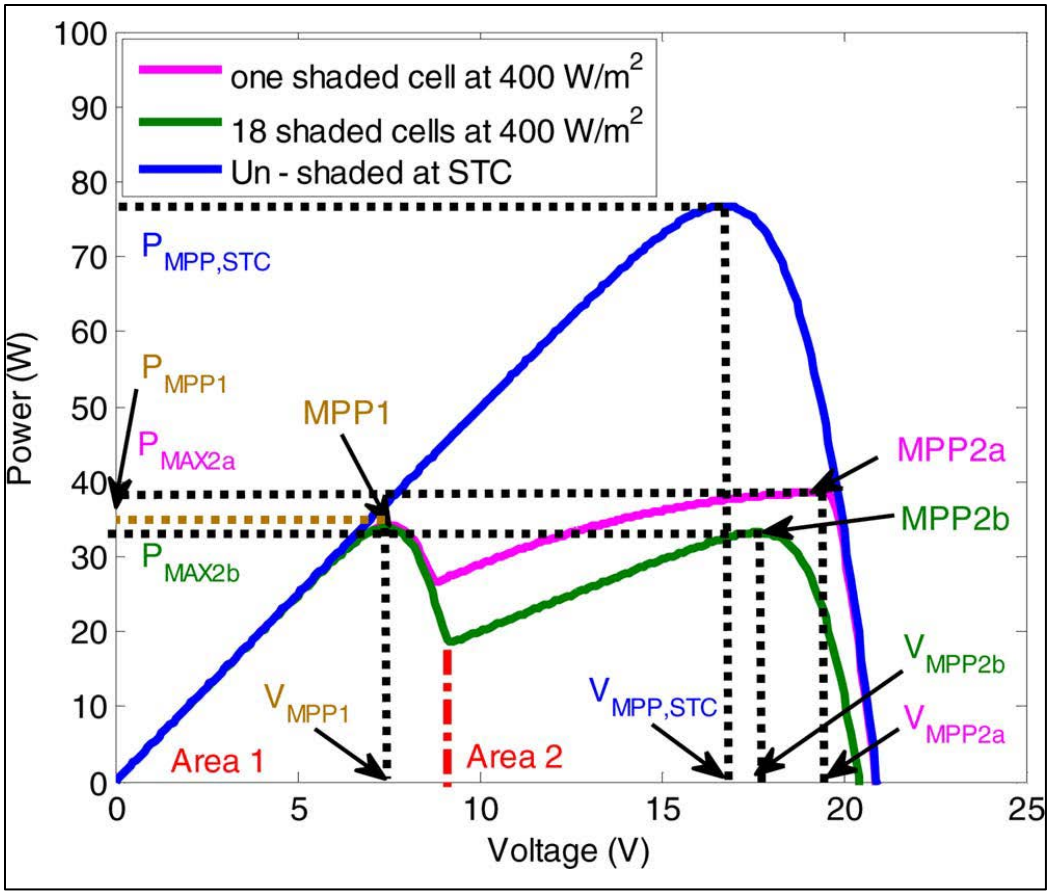

Figure 14: P-V Characteristic Under Partial Shading With Bypass Diodes [19]

Under partial shading conditions, the P-V characteristic changes shape, resulting in a local and global maximum power point. Measurements have shown the global MPP to be on the order of 13% percent higher than the local MPP [19]. However, the voltage reduction required in order to operate at the MPP tends to be on the order of 45% percent [19]. Many MPPT algorithms result in operation at the local MPP, instead of the global [19].

3.4 MISMATCH LOSSES

PV modules are connected in series (strings) in order to raise the output voltage of the system to the level required for interconnection (either with the building EPS, in the case of a DC power system; or with the PV inverter, in the case of an AC power system). PV strings are then connected in parallel to form arrays, in order to increase the total current injected into the system, and thus, the produced power. The total power injected into the system is the product of the voltage and current at the point of interconnection.

Referring to the diagram in Figure 12, one can see that the voltage of each string must be identical at the point of interconnection. Consider the case that one panel in the first string becomes partially shaded. The voltage output of the panel will be reduced, and the total voltage of string one will reduce by the same amount. Since the string voltages must match, string two will be forced to change its operating point, until a voltage equilibrium is found between the two strings [19]. At the new equilibrium point, all panels have adjusted their operating points, deviating from their respective MPPs, all because of the partial shading on one panel [19]. It has been shown that shading one panel in row one by 33 % can reduce the power output of row two by 3 to 9 %, due to the mismatch in string voltages [19].

3.5 SUMMARY OF PV INTERCONNECTION ISSUES

In real PV systems, issues like partial shading and mismatch losses are interrelated. In the case of a single panel becoming partially shaded, the drop in voltage can cause mismatch losses between parallel strings. So there is a balance between the power and voltage of a single module, and the

power and voltage of a large array. It is not always straightforward to determine the optimal operating point. Therefore, the goal of effective interconnection can become complicated, as the optimal operating voltage, and the ability to extract maximum power from the system, can be set at odds with each other.

The effects of partial shading can be minimized by performing MPPT on each individual module. In this way, the reduced illumination of one panel does not produce a reduction in the power produced by another module. Each individual panel can be regulated to extract its maximum power, independent of the operation of the other panels in the system.

Furthermore, the effects of voltage mismatch can be eliminated by ensuring that the output voltage of each module is regulated to a constant value, regardless of the environmental conditions. If all modules always operate at a constant and equal voltage, mismatch becomes impossible.

4.0 DESIGN CONSIDERATIONS

A number of design considerations must be balanced, in creating a solution for DC solar integration. Most notably, suitable power electronic circuit topologies must be chose, and appropriate controls must be designed. This section will discuss the chosen topologies, while the control strategies are addressed in later chapters.

4.1 POWER ELECTRONIC CONVERTER TOPOLOGIES

MPPT algorithms can be implemented in a variety of power electronic circuit topologies. Buck, boost, and buck-boost topologies have all been demonstrated [20]. However, it has been shown that the boost converter operates at the highest efficiency, and with a large input voltage range [21] Other advantages include a simple, single switch architecture, which reduces component count, leading to more cost effective hardware implementation. The boost converter has been demonstrated as a logical choice for implementing MPPT algorithms in power electronic systems.

MPPT algorithms regulate the terminal voltage of the PV module. Given an input voltage to the boost stage, and a varying duty cycle, the output voltage of the boost converter will change, as the boost converter performs the task of regulation. The voltage swings on the output of the boost stage must be regulated for proper interconnection into a DC system. Depending on

the module output voltage, the magnitude of the voltage swings introduced by the MPPT algorithm, and the interconnection voltage, the regulator may need to increase, or decrease the output voltage. Therefore, it is beneficial to perform the voltage regulation task with a power electronics converter that can either buck or boost its input voltage. Candidate converters include the buck-boost converter, Cuk converter, and SEPIC converter, amongst others.

To perform the task of regulation, a Cuk converter was chosen. The Cuk converter has a buck-boost voltage conversion ratio, but with an inverted output polarity. This inverted output ensures easy integration into -48 V DC telecom systems. For systems requiring a positive output voltage, the wiring is reversed when connecting the PV modules to the boost converter. Cuk converters have been utilized for PV integration in a number of scenarios previously [22][23][24][25][26].

5.0 ANALYTICAL FRAMEWORK

The cascaded converter system is shown in Figure 15 below. The PV module is represented by an equivalent circuit network. The shown system models a 72 cell panel, configured with three bypass diodes. An isolation capacitor separates the PV module from the converter system. The buck converter and Cuk converter are cascaded, followed by an equivalent load resistance. This chapter details the design of the converter sub-systems.

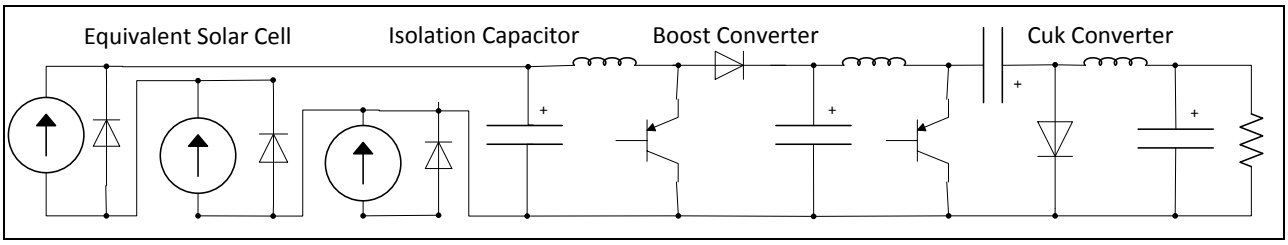

Figure 15: System Circuit Representation

Figure 16 shows a modified version of the circuit, wherein the PV module is lumped into one equivalent cell.

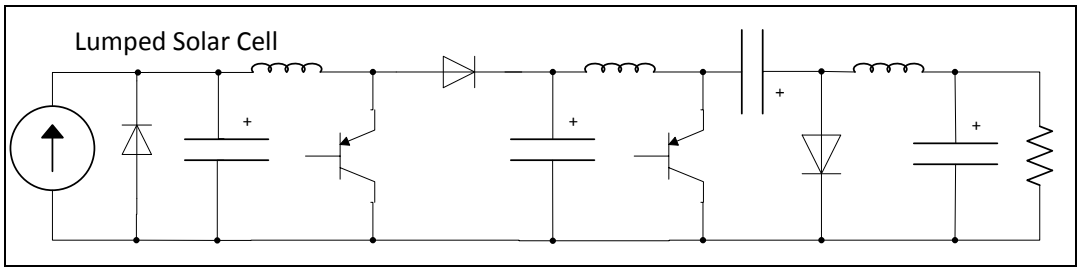

Figure 16: System With Lumped PV Model

The 72 cell model is necessary when quantifying the effects of partial shading on the system's operation. However, for steady-state modeling, an equivalent behavioral model offers sufficient detail. Figure 17 shows an equivalent model which replaces the input current source, bypass diode, and isolation capacitor with a voltage source. Under steady-state conditions, the input terminal of the system can be accurately represented using an equivalent voltage source, whose voltage is equivalent to the terminal voltage of the PV module. This equivalent circuit model is used in developing the analytical framework for the converter's operation.

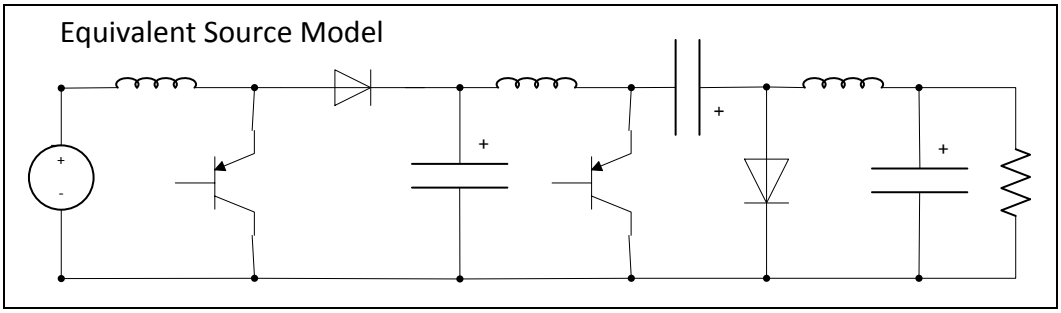

Figure 17: System With Equivalent Source Model

5.1 AVERAGED CIRCUIT ANALYSIS

This section presents a DC steady-state analysis of the converter system. The system has two independent switching devices, resulting in four switching states. Figure 18 shows the equivalent circuit diagrams for each of the four converter states.

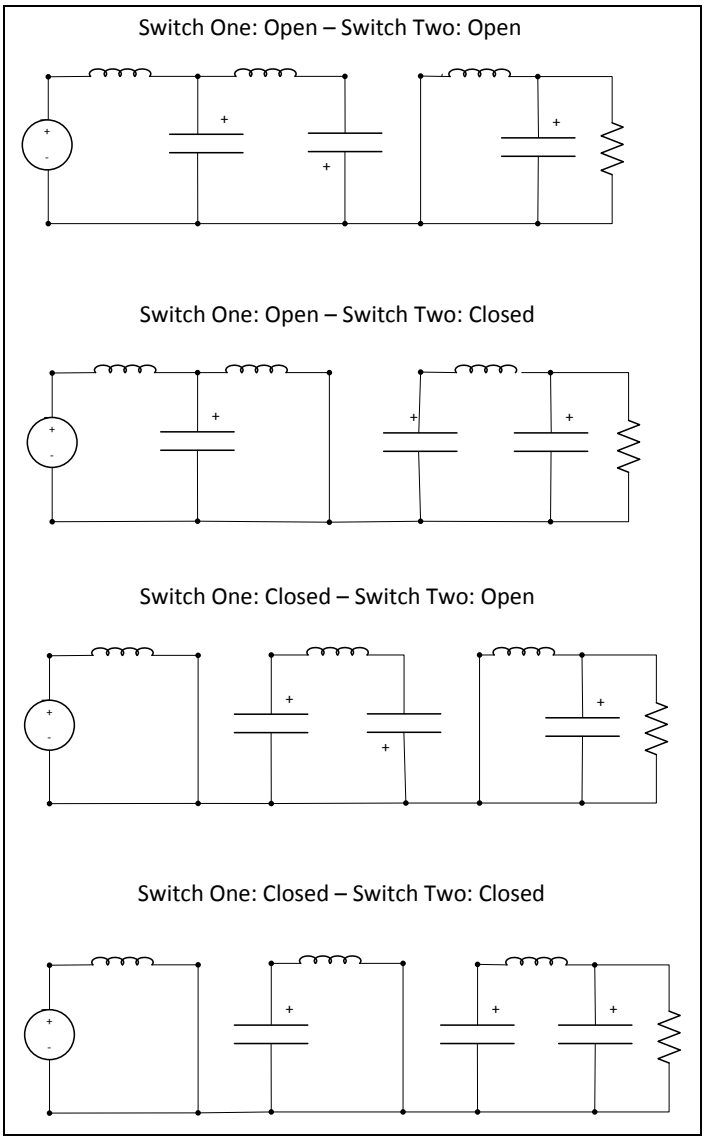

Figure 18: Converter Switching States

Based on the given diagrams, the following equations can be written for the dynamic components in the circuit during each switching state. Note that this system has three inductors and three capacitors. The description of the converter is segmented into three stages: the boost stage (containing the boost inductor and boost capacitor), the regulator stage (containing the regulator inductor and regulator capacitor), and the output stage (containing the output filter inductor and output filter capacitor). The dynamic equations are shown below:

State One - Switch One Off, Switch Two Off:

$$V_{LB} = (d_1' * d_2') * \left(V_g - V_{CB}\right) \tag{1}$$

$$V_{LR} = (d_1' * d_2') * (V_{CB} - V_{CR}) \tag{2}$$

$$V_{LO} = (d_1' * d_2') * (V_o) \tag{3}$$

$$I_{CB} = (d_1' * d_2') * (i_{LB} - i_{LR}) \tag{4}$$

$$I_{CR} = (d_1' * d_2') * (i_{LR}) \tag{5}$$

$$I_{CO} = (d_1' * d_2') * \left(i_{LO} - \frac{V_o}{R}\right) \tag{6}$$

State Two - Switch One Off, Switch Two On:

$$V_{LB} = (d_1' * d_2) * \left(V_g - V_{CB}\right) \tag{7}$$

$$V_{LR} = (d_1' * d_2) * (V_{CB}) \tag{8}$$

$$V_{LB} = (d_1' * d_2) * \left(V_g - V_{CB}\right) \tag{9}$$

$$I_{CB} = (d_1' * d_2) * (i_{LB} - i_{LR}) \tag{10}$$

$$I_{CR} = (d_1' * d_2) * (-i_{LO}) \tag{11}$$

$$I_{CO} = (d_1' * d_2) * \left(i_{LO} - \frac{V_o}{R}\right) \tag{12}$$

State Three - Switch One On, Switch Two Off:

$$V_{LB} = (d_1 * d_2') * (V_g) \tag{13}$$

$$V_{LR} = (d_1 * d_2') * (V_{CB} - V_{CR}) \tag{14}$$

$$V_{LO} = (d_1 * d_2') * (V_o) \tag{15}$$

$$I_{CB} = (d_1 * d_2') * (-i_{LR}) \tag{16}$$

$$I_{CR} = (d_1 * d_2') * (i_{LR}) \tag{17}$$

$$I_{CO} = (d_1 * d_2') * \left(i_{LO} - \frac{V_o}{R}\right) \tag{18}$$

State Four - Switch One On, Switch Two On:

$$V_{LB} = (d_1 * d_2) * (V_g) \tag{19}$$

$$V_{LR} = (d_1 * d_2) * (V_{CB}) \tag{20}$$

$$V_{LO} = (d_1 * d_2) * (V_{CR} + V_o) \tag{21}$$

$$I_{CB} = (d_1 * d_2) * (-i_{LR}) \tag{22}$$

$$I_{CR} = (d_1 * d_2) * (-i_{LO}) \tag{23}$$

$$I_{CO} = (d_1 * d_2) * \left(i_{LO} - \frac{V_o}{R}\right) \tag{24}$$

In the equations above, the value of each component is represented as a function of the duty cycles of both switches. However, the value of each component is only dependent on the duty cycle of one switch. Figure 19 demonstrates the relationship between the switching states, and the value of each component.

I_{CR}	0	1	S2
0	i_{LR}	$-i_{LO}$	
1	i_{LR}	$-i_{LO}$	
S1			

Figure 19: Karnaugh Map Showing Component Value Dependency

From the figure, it can be deduced that the average value of the regulator capacitor current can be expressed as:

$$I_{CR} = d_2' i_{LR} + d_2 i_{LO} \tag{25}$$

Using the same method, the average values of each element, over one switching period, can be defined. It is assumed that the two switches have the same switching period, although their duty cycles are independent. The equations are shown below.

$$\langle V_{LB} \rangle = \langle d_1' \rangle * \left(\langle V_g \rangle - \langle V_{CB} \rangle \right) + \langle d_1 \rangle * \langle V_g \rangle \tag{26}$$

$$\langle V_{LR} \rangle = \langle d_2' \rangle * (\langle V_{CB} \rangle - \langle V_{CR} \rangle) + \langle d_2 \rangle * \langle V_{CB} \rangle \tag{27}$$

$$\langle V_{LO} \rangle = \langle d_2' \rangle * \langle V_o \rangle + \langle d_2 \rangle * (\langle V_{CR} \rangle + \langle V_o \rangle) \tag{28}$$

$$\langle I_{CB} \rangle = \langle d_1' \rangle * (\langle I_{LB} \rangle - \langle I_{LR} \rangle) + \langle d_1 \rangle * -\langle I_{LR} \rangle \tag{29}$$

$$\langle I_{CR} \rangle = \langle d_2' \rangle * \langle I_{LR} \rangle + \langle d_2 \rangle * -\langle I_{LO} \rangle \tag{30}$$

$$\langle I_{CO} \rangle = \left(\langle I_{LO} \rangle - \frac{\langle V_o \rangle}{R} \right) \tag{31}$$

5.2 EQUIVALENT CIRCUIT MODEL

An AC equivalent circuit model can be derived by perturbing the system and then linearizing around an operating point. The average circuit values are replaced by their steady-state (DC) values, plus a small signal AC variation. Small signal implies that the magnitude of the AC variations are smaller than the DC quantities for each variable. The following substitutions are made to the DC circuit equations from the prior section:

$$\langle I_{LB} \rangle = (I_{LB} + \hat{\imath}_{LB}) \tag{32}$$

$$\langle I_{LR} \rangle = (I_{LR} + \hat{\imath}_{LR}) \tag{33}$$

$$\langle I_{LO} \rangle = (I_{LO} + \hat{\imath}_{LO}) \tag{34}$$

$$\langle V_{CB} \rangle = (V_{CB} + \hat{v}_{CB}) \tag{35}$$

$$\langle V_{CR} \rangle = (V_{CR} + \hat{v}_{CR}) \tag{35}$$

$$\langle V_{CO} \rangle = (V_{CO} + \hat{v}_{CO}) \tag{36}$$

$$\langle V_{LB} \rangle = (V_{LB} + \hat{v}_{LB}) = L * [\frac{d}{dt}(I_{LB}) + \frac{d}{dt}(\hat{\imath}_{LB})] \tag{37}$$

$$\langle V_{LR} \rangle = (V_{LR} + \hat{v}_{LR}) = L * [\frac{d}{dt}(I_{LR}) + \frac{d}{dt}(\hat{\imath}_{LR})] \tag{38}$$

$$\langle V_{LO} \rangle = (V_{LO} + \hat{v}_{LO}) = L * [\frac{d}{dt}(I_{LO}) + \frac{d}{dt}(\hat{\imath}_{LO})] \tag{39}$$

$$\langle I_{CB} \rangle = (I_{CB} + \hat{\imath}_{CB}) = C * [\frac{d}{dt}(V_{CB}) + \frac{d}{dt}(\hat{v}_{CB})] \tag{40}$$

$$\langle I_{CR} \rangle = (I_{CR} + \hat{\imath}_{CR}) = C * [\frac{d}{dt}(V_{CR}) + \frac{d}{dt}(\hat{v}_{CR})] \tag{41}$$

$$\langle I_{CO} \rangle = (I_{CO} + \hat{\imath}_{CO}) = C * [\frac{d}{dt}(V_{CO}) + \frac{d}{dt}(\hat{v}_{CO})] \tag{42}$$

$$\langle V_g \rangle = (V_g + \hat{v}_g) \tag{43}$$

$$\langle V_o \rangle = (V_o + \hat{v}_o) \tag{44}$$

$$\langle d_1 \rangle = (D_1 + \hat{d}_1) \tag{45}$$

$$\langle d_1' \rangle = ({D_1}' - \hat{d}_1) \tag{46}$$

$$\langle d_2 \rangle = (D_2 + \hat{d}_2) \tag{47}$$

$$\langle d_2' \rangle = ({D_2}' - \hat{d}_2) \tag{48}$$

Perturbation of the system results in the following circuit equations:

$$L * [\frac{d}{dt}(I_{LB}) + \frac{d}{dt}(\hat{\imath}_{LB})] = ({D_1}' - \hat{d}_1) * \big((V_g + \hat{v}_g) - (V_{CB} + \hat{v}_{CB})\big) + (D_1 + \hat{d}_1) * (V_g + \hat{v}_g) \tag{49}$$

$$L * [\frac{d}{dt}(I_{LR}) + \frac{d}{dt}(\hat{\imath}_{LR})] = ({D_2}' - \hat{d}_2) * (V_{CB} + \hat{v}_{CB}) - (V_{CR} + \hat{v}_{CR}) + (D_2 + \hat{d}_2) * (V_{CB} + \hat{v}_{CB}) \tag{50}$$

$$L * [\frac{d}{dt}(I_{LO}) + \frac{d}{dt}(\hat{\imath}_{LO})] = ({D_2}' - \hat{d}_2) * (V_o + \hat{v}_o) + (D_2 + \hat{d}_2) * (V_{CR} + \hat{v}_{CR}) + (V_o + \hat{v}_o) \tag{51}$$

$$C * [\frac{d}{dt}(V_{CB}) + \frac{d}{dt}(\hat{v}_{CB})] = ({D_1}' - \hat{d}_1) * (I_{LB} + \hat{\imath}_{LB}) - (I_{LR} + \hat{\imath}_{LR}) + (D_1 + \hat{d}_1) * -(I_{LR} + \hat{\imath}_{LR}) \tag{52}$$

$$C * [\frac{d}{dt}(V_{CR}) + \frac{d}{dt}(\hat{v}_{CR})] = ({D_2}' - \hat{d}_2) * (I_{LR} + \hat{\imath}_{LR}) + (D_2 + \hat{d}_2) * -(I_{LO} + \hat{\imath}_{LO}) \tag{53}$$

$$C * [\frac{d}{dt}(V_{CO}) + \frac{d}{dt}(\hat{v}_{CO})] = \left((I_{LO} + \hat{\imath}_{LO}) - \frac{(V_o + \hat{v}_o)}{R}\right) \tag{54}$$

By factoring, grouping the DC terms, grouping the 1st order AC terms, and eliminating the higher order terms, insights into the circuit behavior can be found. The following equations describe the DC circuit behavior.

$$L\frac{d}{dt}(I_{LB}) = V_g - {D_1}' * V_{CB} \tag{55}$$

$$L\frac{d}{dt}(I_{LR}) = V_{CB} - D_2{}' * V_{CR} \tag{56}$$

$$L\frac{d}{dt}(I_{LO}) = V_o + D_2 * V_{CR} \tag{57}$$

$$C * \frac{d}{dt}(V_{CB}) = D_1{}' * I_{LB} - I_{LR} \tag{58}$$

$$C * \frac{d}{dt}(V_{CR}) = D_2{}' * I_{LR} - D_2 * I_{LO} \tag{59}$$

$$C * \frac{d}{dt}(V_{CO}) = I_{LO} - \frac{V_o}{R} \tag{60}$$

Note that the left-hand side of the prior equations all equal zero in the steady-state. From these equations, the following DC conversion ratios can be deduced:

$$\frac{V_{CB}}{V_g} = \frac{1}{D_1'} \tag{61}$$

$$\frac{V_{CR}}{V_{CB}} = \frac{1}{D_2'} \tag{62}$$

$$\frac{V_O}{V_{CR}} = -D_2 \tag{63}$$

The following equations represent the AC behavior of the circuit.

$$L\frac{d}{dt}(\hat{\imath}_{LB}) = \hat{v}_g + V_{CB} * \hat{d}_1 - D_1{}' * \hat{v}_{CB} \tag{64}$$

$$L\frac{d}{dt}(\hat{\imath}_{LR}) = \hat{v}_{CB} + V_{CR} * \hat{d}_2 - D_2{}' * \hat{v}_{CR} \tag{65}$$

$$L\frac{d}{dt}(\hat{\imath}_{LO}) = \hat{v}_o + V_{CR} * \hat{d}_2 + D_2 * \hat{v}_{CR} \tag{66}$$

$$C\frac{d}{dt}(\hat{v}_{CB}) = -\hat{\imath}_{LR} - I_{LB} * \hat{d}_1 + D_1{}' * \hat{\imath}_{LB} \tag{67}$$

$$C\frac{d}{dt}(\hat{v}_{CR}) = -D_2 * \hat{\imath}_{LO} - I_{LR} * \hat{d}_2 - I_{LO} * \hat{d}_2 + D_2{}' * \hat{\imath}_{LR} \tag{68}$$

$$C * \frac{d}{dt}(\hat{v}_{CO}) = \hat{\imath}_{LO} - \frac{\hat{v}_o}{R} \tag{69}$$

Each of these equations represents either a voltage loop containing an inductor, or a current node containing a capacitor. From these six equations, the following behavioral circuit model can be constructed:

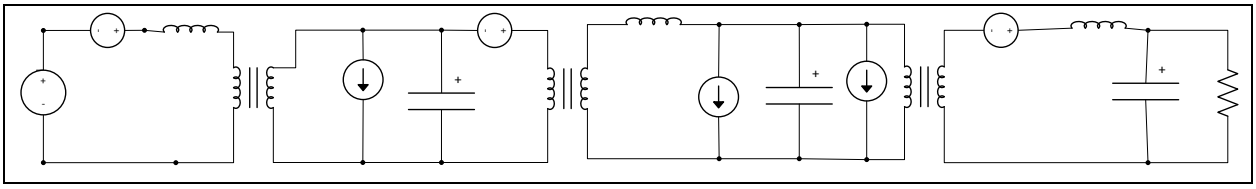

Figure 20: Equivalent AC Circuit

From inspection, the following current relationships can be deduced:

$$I_{LB} = \frac{V_{CB}}{D_1' * R_{Bin}} \tag{67}$$

$$I_{LR} = \frac{V_{CR}}{R_{Bin}} \tag{68}$$

$$I_{LO} = \frac{V_{CO}}{R_{Load}} \tag{69}$$

5.3 CANONICAL FORM REPRESENTATION

The AC equivalent circuit model contains three DC transformers, and three sets of inductors and capacitors. The circuit can be re-arranged to form three cascaded circuits, each in the canonical form shown in Figure 22.

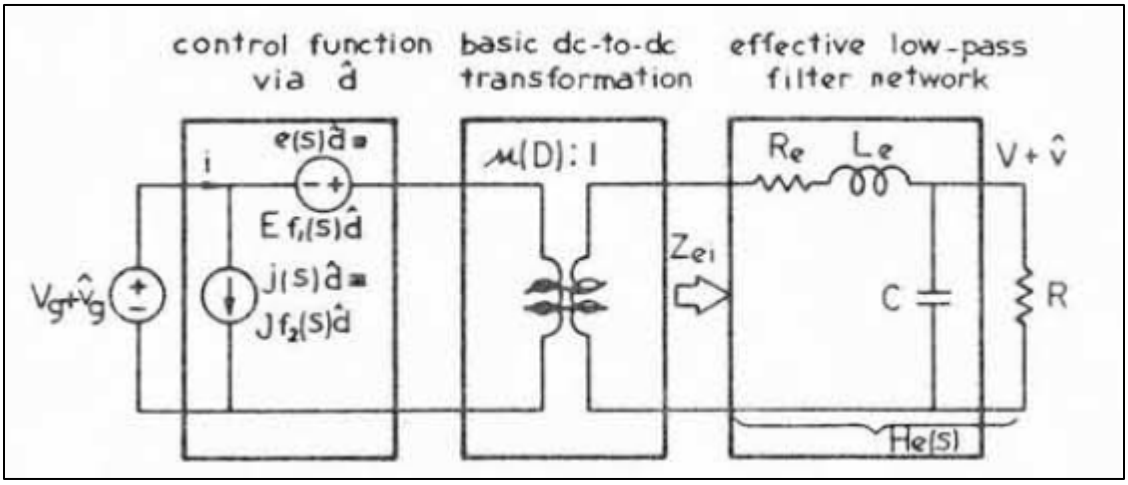

Figure 21: Converter Canonical Form [27]

Again, these three sections of the circuit are referred to as the boost stage, the regulator stage, and the output stage. The equivalent circuit, shown in cascaded canonical form, is shown in Figure 22 below.

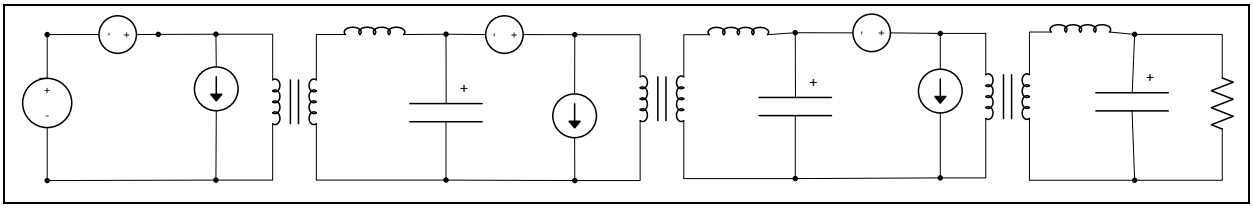

Figure 22: Circuit in Cascaded Canonical Form

The following chart shows the values of all of the circuit components, and the way that each component value changes when transforming the circuit into canonical form. Figure 23 shows the circuit arrangement during the five steps in the transformation process.

Table 3: Component Values During Canonical Form Transformations

	1	2	3	4	5
Vg	Vg	Vg	Vg	Vg	Vg
LB	L_B	$\frac{L_B}{{N_1}^2}$	$\frac{L_B}{{N_1}^2}$	$\frac{L_B}{{N_1}^2}$	$\frac{L_B}{{N_1}^2}$
VEB	$V_{CB} * \hat{d}_1$	$V_{CB} * \hat{d}_1$	$V_{CB} * \hat{d}_1$	$V_{CB} * \hat{d}_1$	$\hat{d}_1 * (V_{CB} + s * I_{LB} * \frac{L_B}{N_1})$
VEBW	-	-	$s * I_{LB} * \hat{d}_1 * \frac{L_B}{{N_1}^2}$	$s * I_{LB} * \hat{d}_1 * \frac{L_B}{N_1}$	-
CB	C_B	C_B	C_B	C_B	C_B
IJB	$I_{LB} * \hat{d}_1$	$I_{LB} * \hat{d}_1$	$I_{LB} * \hat{d}_1$	$\frac{I_{LB} * \hat{d}_1}{N_1}$	$\frac{I_{LB} * \hat{d}_1}{N_1}$
LR	L_R	L_R	L_R	L_R	L_R
VER	$V_{CR} * \hat{d}_2$	$V_{CR} * \hat{d}_2$	$V_{CR} * \hat{d}_2$	$V_{CR} * \hat{d}_2$	$\hat{d}_2 * (V_{CR} + s * L_R * I_{LR} * N_2)$
VERW	-	-	$s * L_R * I_{LR} * \hat{d}_2$	$s * L_R * I_{LR} * \hat{d}_2 * N_2$	-
CR	C_R	C_R	C_R	C_R	C_R
IJR	$I_{LR} * \hat{d}_2$	$I_{LR} * \hat{d}_2$	$I_{LR} * \hat{d}_2$	$\frac{I_{LR} * \hat{d}_2}{N_2}$	$\frac{I_{LR} * \hat{d}_2}{N_2}$
LO	L_O	L_O	L_O	L_O	L_O
VEO	$V_{CR} * \hat{d}_2$	$N_3 * V_{CR} * \hat{d}_2$	$N_3 * V_{CR} * \hat{d}_2$	$N_3 * V_{CR} * \hat{d}_2$	$N_3 * V_{CR} * \hat{d}_2$
CO	C_O	C_O	C_O	C_O	C_O
IJO	$I_{LO} * \hat{d}_2$	$I_{LO} * \hat{d}_2$	$I_{LO} * \hat{d}_2$	$I_{LO} * \hat{d}_2$	$I_{LO} * \hat{d}_2$

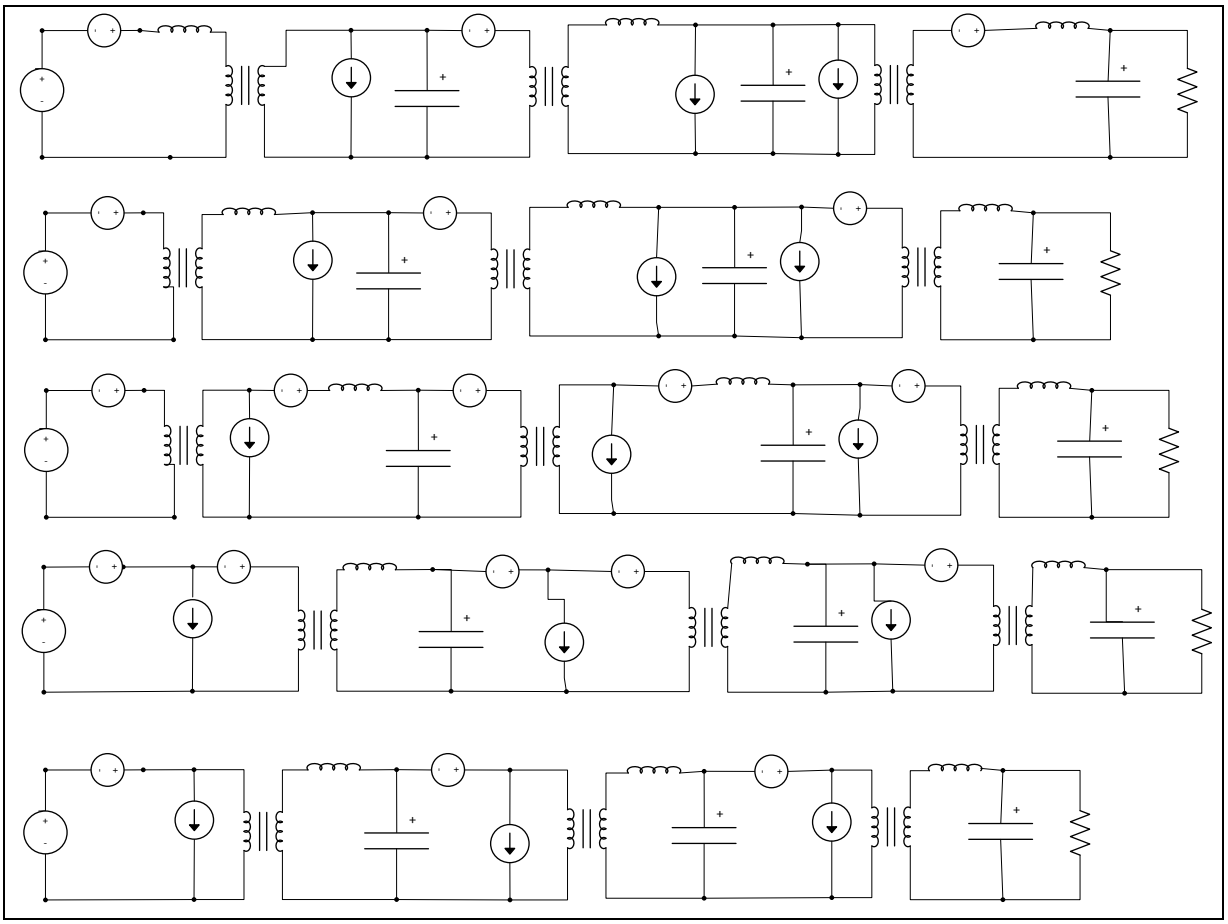

Figure 23: Circuit Transformation into Canonical Form

When each stage of the cascaded system is written in canonical form, and when the appropriate DC current equations are substituted, the canonical circuit parameters can be expressed as:

Table 4: Canonical Circuit Parameters

Sub-System	N	M(D)	Le	e(s)	j
Boost	D_1':1	$\frac{1}{D_1'}$	$\frac{L_B}{D_1'^{\,2}}$	$\hat{d}_1 * V_{CB} * (1 + s * \frac{L_B}{D_1'^{\,2} * R_{Bin}})$	$\hat{d}_1 * \frac{I_{LB}}{D_1'}$
Regulator	D_2':1	$\frac{1}{D_2'}$	L_R	$\hat{d}_2 * V_{CR} * (1 + s * \frac{L_R * D_2'}{R_{Bin}})$	$\hat{d}_2 * \frac{I_{LR}}{D_2'}$
Output	$1:-D_2$	$-D_2$	L_O	$-\hat{d}_2 * (\frac{V_{CR}}{D_2})$	$\hat{d}_2 * I_{LO}$

5.4 SUB-SYSTEM OPEN LOOP TRANSFER FUNCTIONS

As described in [27], the line-to-output transfer function and control-to-output transfer function for the canonical form circuit can be expressed as:

$$G_{VG} = M(D) * H_e(s) \tag{70}$$

$$G_{VD} = \frac{e(s)}{\hat{d}(s)} * G_{VG} \tag{71}$$

As described in [28], $H_e(s)$ for each sub-section is of the form:

$$H_e(s) = \frac{1}{1 + s * \frac{L_e}{R} + s^2 * L_e C} \tag{72}$$

For each converter, the transfer functions take the following forms:

$$G_{VG} = G_{g0} * \frac{1}{(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2})} \tag{72}$$

$$G_{VD} = G_{d0} * \frac{(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2})} \tag{73}$$

The parameters for each converter subsystem are listed in Table 5, where R_{Bin} refers to the input impedance seen across the terminals of the boost stage output capacitor, and R_{Rin} refers to the

input impedance seen across the terminals of the regulator stage output capacitor. R_{Load} refers to the equivalent resistance of the load attached to the cascaded system.

Table 5: Transfer Function Parameters

Sub-System	G_{g0}	G_{d0}	ω_1	ω_2	ω_z	ω_0	Q
Boost	$\frac{1}{D_1'}$	$\frac{V_{CB}}{D_1'}$	$\frac{D_1'^2 * R_{Bin}}{L_B}$	$\frac{1}{R_{Bin} * C_B}$	$\frac{D_1'^2 * R_{Bin}}{L_B}$	$\frac{D_1'}{\sqrt{L_B * C_B}}$	$D_1' * R_{Bin}\sqrt{\frac{C_B}{L_B}}$
Regulator	$\frac{1}{D_2'}$	$\frac{V_{CR}}{D_2'}$	$\frac{R_{Rin}}{L_R}$	$\frac{1}{R_{Rin} * C_R}$	$\frac{R_{Rin}}{L_R * D_2'}$	$\frac{1}{\sqrt{L_R * C_R}}$	$R_{Rin}\sqrt{\frac{C_R}{L_R}}$
Output	$-D_2$	$-V_{CR}$	$\frac{R_{Load}}{L_O}$	$\frac{1}{R_{Load} * C_O}$	∞	$\frac{1}{\sqrt{L_O * C_O}}$	$R_{Load}\sqrt{\frac{C_O}{L_O}}$

Note that every steady-state duty cycle, resistance, capacitance, and inductance represents a positive, real-valued quantity. Therefore, the roots of each transfer function lie in the left-hand side plane, and each open-loop converter sub-system is shown to have stable operation.

As derived in [28], for each converter sub-system, the output impedance takes the form:

$$Z_o = \frac{1}{\frac{1}{R} + \frac{1}{sL_e} + sC} \tag{74}$$

For the boost stage, $R = R_{Bin}$, and $C = C_B$. For the regulator stage, $R = R_{Rin}$, and $C = C_R$. For the output stage, $R = R_{Load}$, and $C = C_o$. The values forL_e are identical to those found in Table 4. The R_{Bin} and R_{Rin} values represent the effective input impedances from the subsequent sub-systems. These values are defined as follows.

$$R_{Rin} = Z_{in,output\ stage} = sL_o + \frac{1}{\frac{1}{R_{Load}} + sC_o} \tag{75}$$

$$R_{Bin} = Z_{in,regulator\ stage} = sL_R + \frac{1}{\frac{1}{R_{Rin}} + sC_R} \tag{76}$$

5.4.1 Summary of Boost Stage Equations

The following is a summary of the equations related to the boost stage of the converter system.

$$H_{eB}(s) = \frac{1}{1 + s * \frac{L_B}{D_1'^2 * R_{LoadBoost}} + s^2 * \frac{L_B}{D_1'^2} * C_B} \tag{77}$$

$$G_{VGB} = \frac{1}{D_1'} * \frac{1}{1 + s * \frac{L_B}{D_1'^2 * R_{LoadBoost}} + s^2 * \frac{L_B}{D_1'^2} * C_B} \tag{78}$$

$$G_{VDB} = V_{CB} * (1 + s * \frac{L_B}{D_1'^2 * R_{Bin}}) * \frac{1}{D_1'} * \frac{1}{1 + s * \frac{L_B}{D_1'^2 * R_{LoadBoost}} + s^2 * \frac{L_B}{D_1'^2} * C_B} \tag{79}$$

The poles are given as:

$$\omega_1 \approx \frac{R}{L} = \frac{R_{LoadBoost}}{L_{eB}} = \frac{D_1'^2 * R_{LoadBoost}}{L_B} \tag{80}$$

$$\omega_2 \approx \frac{1}{RC} = \frac{1}{R_{LoadBoost} * C_B} \tag{81}$$

$$\omega_z \approx \frac{1}{RC} = \frac{D_1'^2 * R_{LoadBoost}}{L_B} \tag{82}$$

5.4.2 Summary of Regulator Stage Equations

The following is a summary of the equations related to the regulator stage of the converter system.

$$H_{eB}(s) = \frac{1}{1 + s * \frac{L_B}{D_1'^2 * R_{LoadBoost}} + s^2 * \frac{L_B}{D_1'^2} * C_B} \tag{83}$$

$$G_{VGR} = \frac{1}{D_2'} * \frac{1}{1 + s * \frac{L_R}{R_{LoadRegulator}} + s^2 * L_R * C_R} \tag{84}$$

$$G_{VDR} = V_{CR} * (1 + s * \frac{L_R * D_2'}{R_{Bin}}) * \frac{1}{D_2'} * \frac{1}{1 + s * \frac{L_R}{R_{LoadRegulator}} + s^2 * L_R * C_R} \tag{85}$$

The poles are given as:

$$\omega_1 \approx \frac{R}{L} = \frac{R_{LoadRegulator}}{L_R} \tag{86}$$

$$\omega_2 \approx \frac{1}{RC} = \frac{1}{R_{LoadRegulator} * C_R} \tag{87}$$

$$\omega_z \approx \frac{1}{RC} = \frac{R_{Bin}}{L_R * D_2'} \tag{88}$$

5.4.3 Summary of Output Stage Equations

The following is a summary of the equations related to the output stage of the converter system.

$$H_{eO}(s) = \frac{1}{1 + s * \frac{L_O}{R_{Load}} + s^2 * L_O * C_O} \tag{89}$$

$$G_{VGO} = -D_2 * \frac{1}{1 + s * \frac{L_O}{R_{Load}} + s^2 * L_O * C_O} \tag{90}$$

$$G_{VDB} = (\frac{V_{CR}}{D_2}) * -D_2 * \frac{1}{1 + s * \frac{L_O}{R_{Load}} + s^2 * L_O * C_O} \tag{91}$$

The poles are given as:

$$\omega_1 \approx \frac{R}{L} = \frac{R_{Load}}{L_O} \tag{92}$$

$$\omega_2 \approx \frac{1}{RC} = \frac{1}{R_{LoadRegulator} * C_R} \tag{93}$$

5.5 CASCADED CONVERTER STABILITY

Although the operation of each sub-system can be shown to be stable, even under closed loop operation, the cascading of the two sub-systems can introduce instability. The Middlebrook criterion is sufficient to ensure that the cascaded system remains stable. A cascaded system can be represented by the diagram in Figure 24 [29].

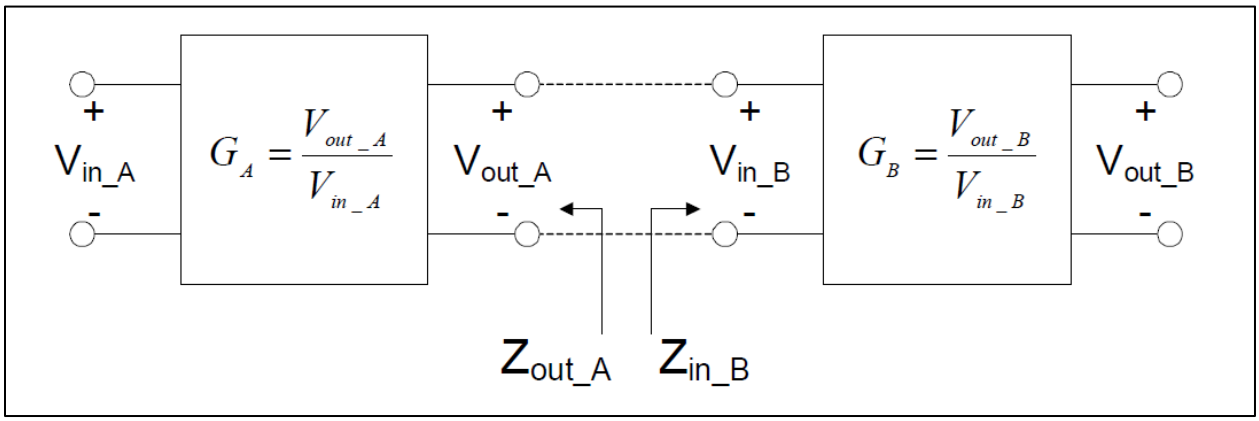

Figure 24: Cascaded Converter Impedances [29]

In the system shown, the total input-output transfer function can be expressed as:

$$G_{AB} = G_A * G_B * \frac{z_{in_B}}{z_{in_B} + z_{out_A}} = G_A * G_B * \frac{1}{1 + T_{MLG}} \tag{107}$$

Where T_{MLG}, the minor loop gain is defined as:.

$$T_{MLG} = \frac{z_{out_A}}{z_{in_B}} \tag{108}$$

The Middlebrook Criterion ensures that the system exhibits stable behavior, if the following condition is met:

$$\|T_{MLG}\| = \left\|\frac{Z_{out_A}}{Z_{in_B}}\right\| \ll 1 \tag{109}$$

6.0 SYSTEM DESIGN

In this chapter, component sizes are specified for each stage in the system. The stability criteria are evaluated based on the design. MATLAB/SIMULINK is used to validate the stability of the open loop transfer functions and cascaded converters.

6.1 SYSTEM OPERATING POINT

In this section, the general system operating parameters are described. This includes the input and output voltages, the power ratings, the devices modeled, and the switching frequency. The following parameters define the system steady-state operating point.

Table 6: Steady-State Circuit Values

Name	Symbol	Value
Input Voltage	Vg	34
Switching Frequency	f	100000
Load Power Consumption	Pload	150
Resistance of Load	Rload	20

6.2 FILTER SIZING

The inductor and capacitor values were chosen in order to minimize the output voltage ripple, and the inductor current ripple throughout the circuit. The ripple equations are shown below, as derived in [28]. Component values are also listed below.

Each inductor was sized to limit the current ripple through the inductor to 10% of the steady-state value. The equations used are as follows:

$$LB = \frac{V_g * D_{Boost}}{2 * f * \Delta I_{LB}} \tag{110}$$

$$LR = \frac{V_{mid} * D_{Cuk}}{2 * f * \Delta I_{LR}} \tag{111}$$

$$LO = \frac{V_{mid} * D_{Boost}}{2 * f * \Delta I_{LO}} \tag{112}$$

Each capacitor was sized to limit the voltage ripple through the capacitor to 5% of the steady-state value. The equations used are as follows:

$$CB = \frac{V_g * {D_{Boost}}^2}{2 * f * D'_{Boost} * R_{B,equiv} * \Delta V_{CB}} \tag{113}$$

$$CR = \frac{V_{mid} * {D_{Cuk}}^2}{2 * f * D'_{Cuk} * R_{R,equiv} * \Delta V_{CR}} \tag{114}$$

$$CO = \frac{\Delta I_{LO}}{8 * f * \Delta V_{CO}} \tag{115}$$

$$Ciso = \frac{P_{mpp}}{2 * \pi * V_{mpp} * \Delta V_{mpp}} \tag{116}$$

The filter component sizes are given below.

Table 7: Reactive Component Sizes

Name	Symbol	Value
Boost Stage Inductor	LB	2.91E-04
Boost Stage Capacitor	CB	9.91E-06
Regulator Stage Inductor	LR	5.66E-04
Regulator Stage Capacitor	CR	6.43E-06
Output Stage Inductor	LO	3.54E-04
Output Stage Capacitor	CO	1.09E-06

6.3 OPEN LOOP TRANSFER FUNCTIONS

In this section, the open loop transfer functions are evaluated using MATLAB. Pole locations, phase and gain margins, and impedance ratios are evaluated.

6.3.1 Pole Values:

The following figures show the locations of the poles and zeros for the transfer functions defined in the previous chapter. As shown, all poles lie in the left-hand plane, meaning the open-loop transfer functions are stable. However, the control-to-output transfer functions for both the boost and Cuk converters exhibit a right-hand-plane pole, which can have a destabilizing effect in some applications.

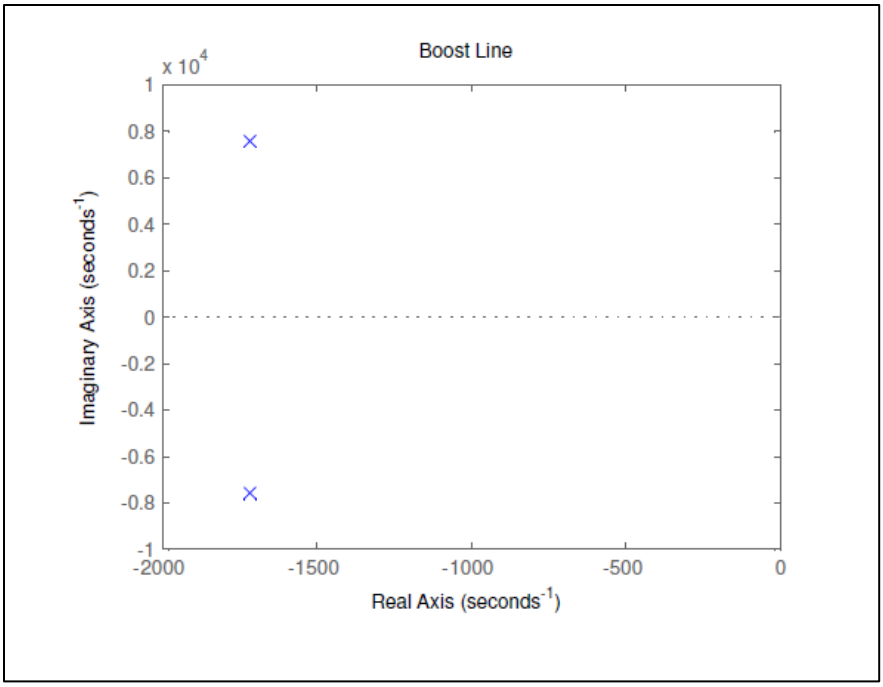

Figure 25: Boost Converter: Line Voltage to Output Voltage Transfer Function

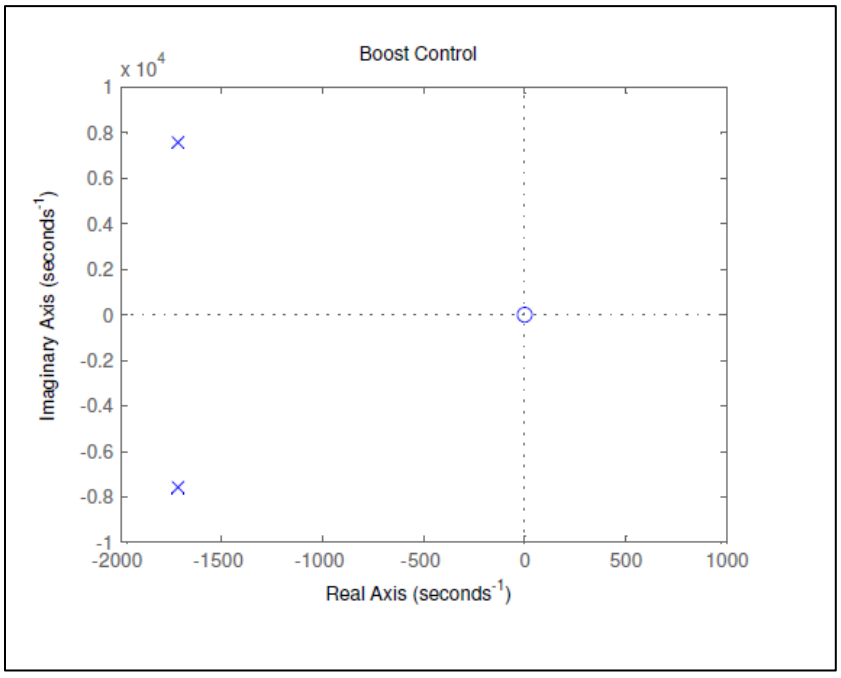

Figure 26: Boost Converter: Control to Output Voltage Transfer Function

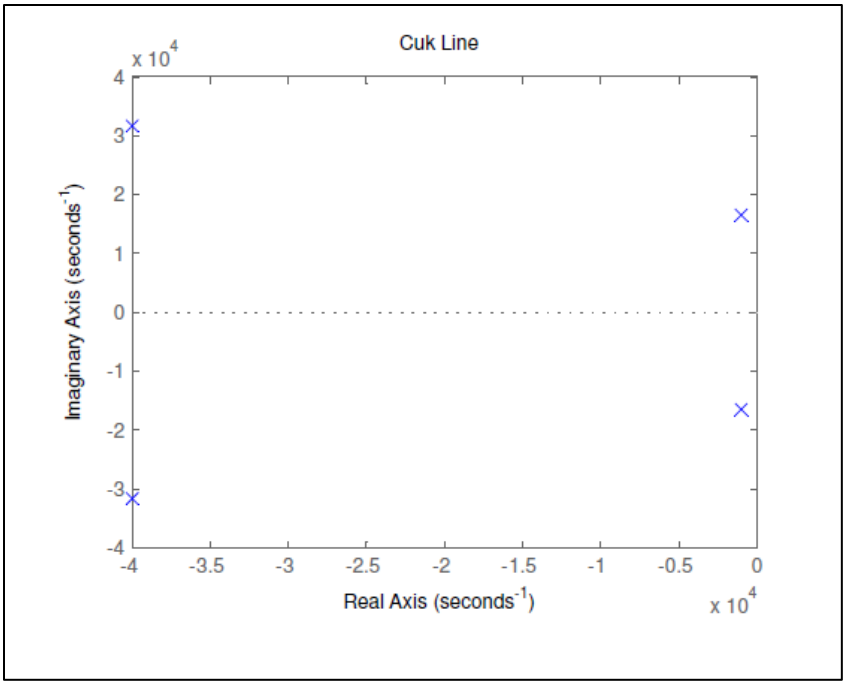

Figure 27: Cuk Converter: Line Voltage to Output Voltage Transfer Function

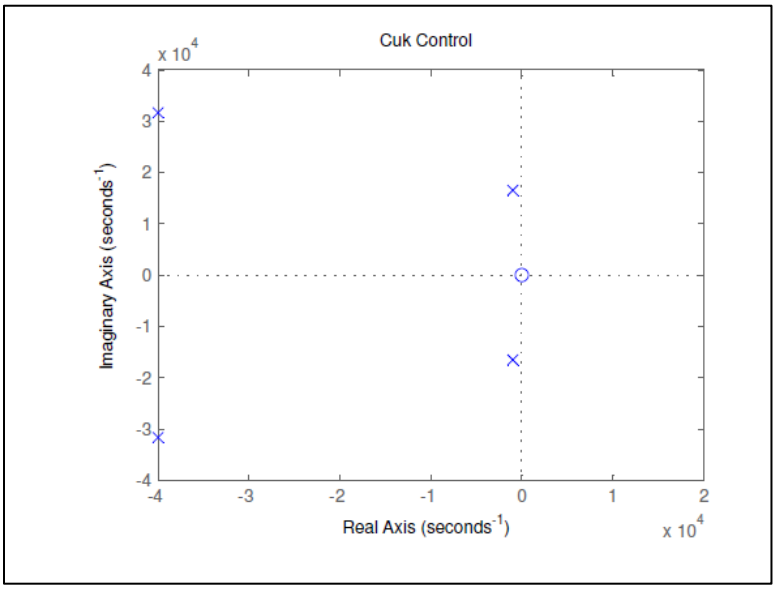

Figure 28: Cuk Converter: Control to Output Voltage Transfer Function

6.3.2 Impedance Ratios:

The minor loop gains were calculated to determine whether converter interactions affected the stability of the system. The minor loop gain was evaluated for the boost and regulator stage interfaces, and for the regulator and output stage interfaces. The minor loop gains are defined as:

$$T_{MLG,BR} = \frac{z_{out,Boost}}{z_{in,Reg}} \tag{117}$$

$$T_{MLG,RO} = \frac{z_{out,Reg}}{z_{in,Out}} \tag{118}$$

Using the parameter values given in this chapter, and the definitions provided in Table 4, the following MATLAB script was used to evaluate the converter input and output impedances, as well as their ratios

.

```
%% Script
ZoB=1/((1/(s*LeB))+(s*CB));
ZinO=(s*LO)+(1/((1/Rload)+(s*CO)));
ZinR=(s*LR)+(1/((1/ZinO)+(s*CR)));
ZoR=1/((1/ZoB)+(1/(s*LeR))+(s*CR));
ratioOne=abs(ZoB)/abs(ZinR);
ratioTwo=abs(ZoR)/abs(ZinO);
%% end script
```

The output of the script is provided below:

%% MATLAB output

ratioOne = 4.5206e-004

ratioTwo = 4.4052e-004

%% end MATLAB output

Note that in each case, the impedance ratio is orders of magnitude less than one, guaranteeing that control interactions will affect the performance of the cascaded system.

6.4 CONTROLLER DESIGN

In order to verify correct system operation, yet simplify the design and simulation, dynamic feedforward controllers were used in the system analysis. Using this method, the reference values for key parameters were dynamically adjusted, and the converter duty cycles were adjusted accordingly. This is not a true feedback control system, but serves the purpose of this analysis. The design of a true feedback system would involve the design of compensator circuits to account for the right-hand plane poles in the converter transfer functions. This work is left for future consideration, while the present work establishes the validity of the converters functionality. The method for calculating the duty cycle needed for operation at the maximum power point is discussed in the section on software simulation.

For the task of voltage regulation in the Cuk converter stage, a simple mathematical relationship can be derived from the converter's voltage conversion ratio, which is repeated below:

$$\frac{V_o}{V_{CB}} = \frac{D_2}{D_2'} \tag{119}$$

Rearranging terms:

$$D_2 = \frac{V_o}{V_o - V_{CB}} \tag{120}$$

As the MPPT controller operates in the boost stage, the midpoint voltage (the voltage across the boost capacitor, which serves as the input voltage to the Cuk stage) will fluctuate. By actively measuring the midpoint voltage, and maintaining a fixed reference for the desired output voltage, the required duty cycle can easily be calculated and updated.

7.0 SOFTWARE VALIDATION

Ansys Simplorer was used to verify the circuit behavior. This chapter describes the simulation setups used, and the results of these analyses. Figure 29 shows the PV module and converter system, as implemented in Simplorer. To the left, a model of the PV module is implemented. In the center, a boost converter with its PWM control, and to the right, a Cuk converter with its PWM control. All components used in the model were available from the Simplorer libraries.

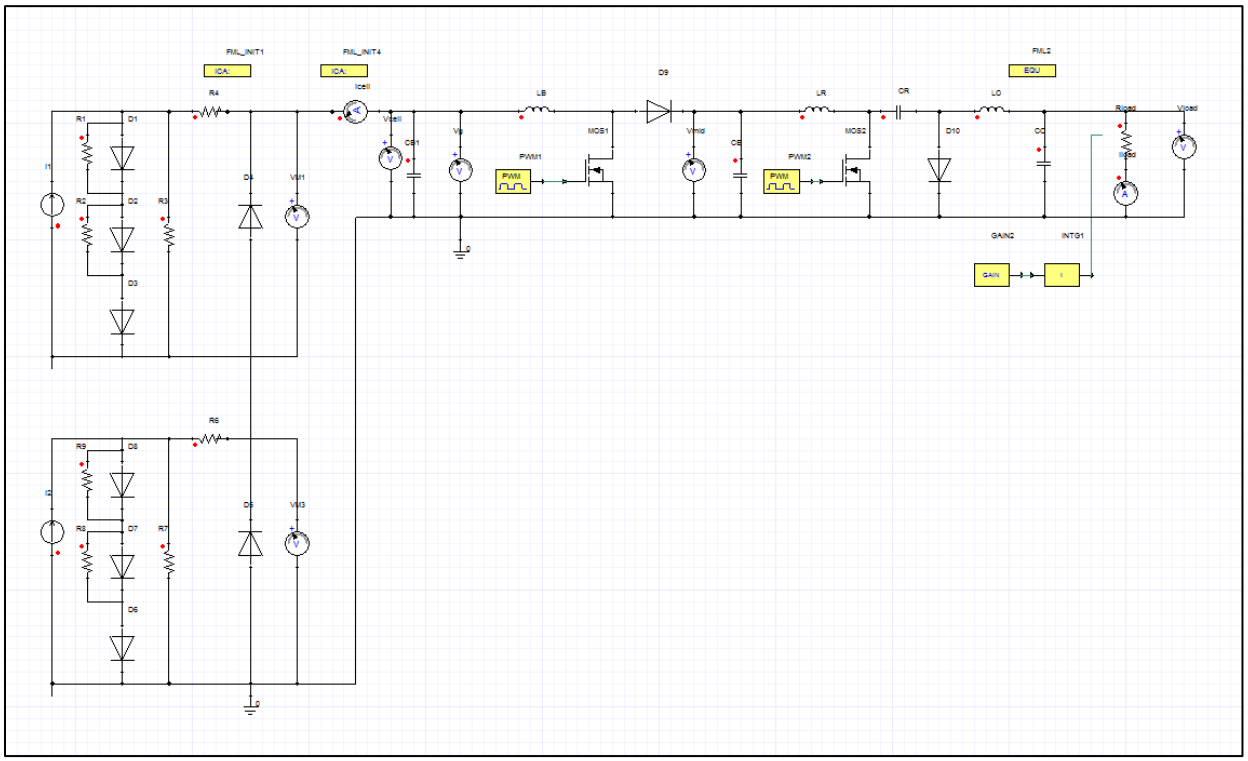

Figure 29: Simplorer Circuit Diagram

7.1 PV MODULE MODELING

PV modules can be modeled in a variety of ways, each being suitable for power system studies. PV modules can be modeled by equivalent equations that produce continuous I-V curves. Alternatively, piecewise-linear curves have been proposed in the literature. The choice between either modeling method involves a tradeoff between model accuracy and simulation time.

7.1.1 Continuous Curve Modeling

A continuous time PV module was implemented in MATLAB/Simulink using the method described in the following reference [30]. The reference implements the I-V characteristics by solving a transcendental equation for the photo-generated PV cell current. This equation must be solved at each time step. This requirement slows the computation process, increasing the simulation run time. The code for the PV model was implemented in C-code. The script can be found in the referenced paper.

To increase simulation speed, the code was translated from C into the MATLAB scripting language, yielding a quicker simulation time. The PV module, written in the MATLAB scripting language, can be found in Appendix A. A resistive load was varied across the terminals of the PV module, and the terminal voltage and source current were measured at every instance of load. Figure 30 shows the model implemented in Simulink. A counter was used to increment the resistor value at each time step.

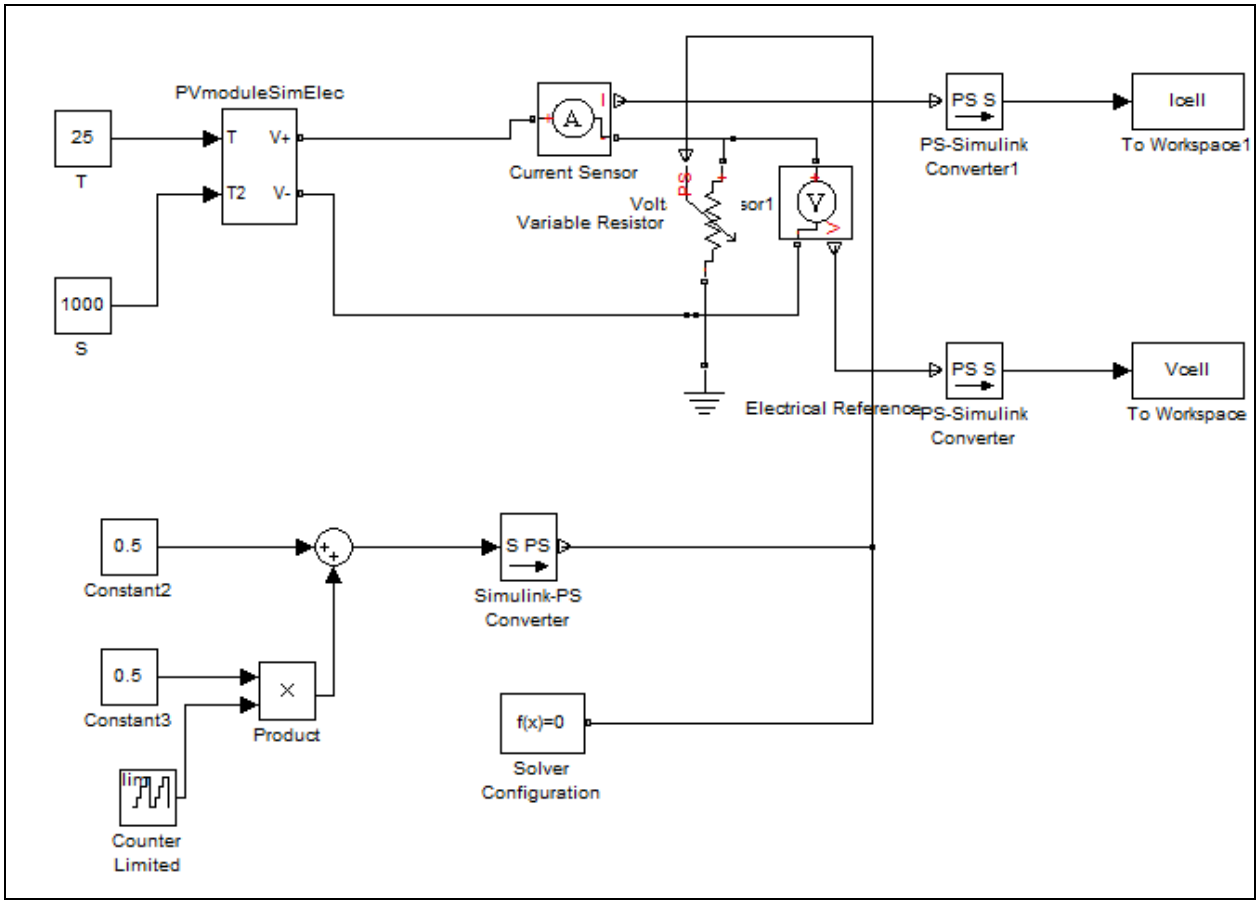

Figure 30: Simulink Model for PV Module

The voltage and current measurements at each time step were used to generate the I-V and P-V characteristics for the module. Figure 31 shows the resulting I-V characteristic. The x-axis shows voltage in volts, while the y-axis displays the module current in amps. Figure 32 shows the resulting P-V characteristic. Again, the x-axis shows the voltage in volts, while the y-axis shows the module power in watts.

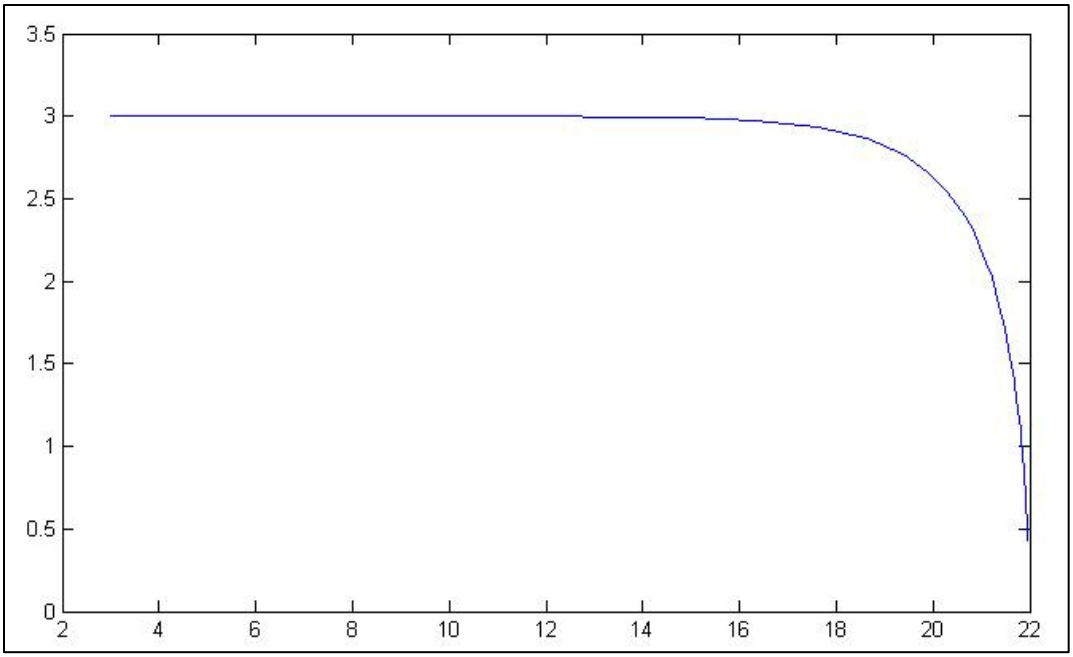

Figure 31: Module I-V Curve Modeled in Simulink

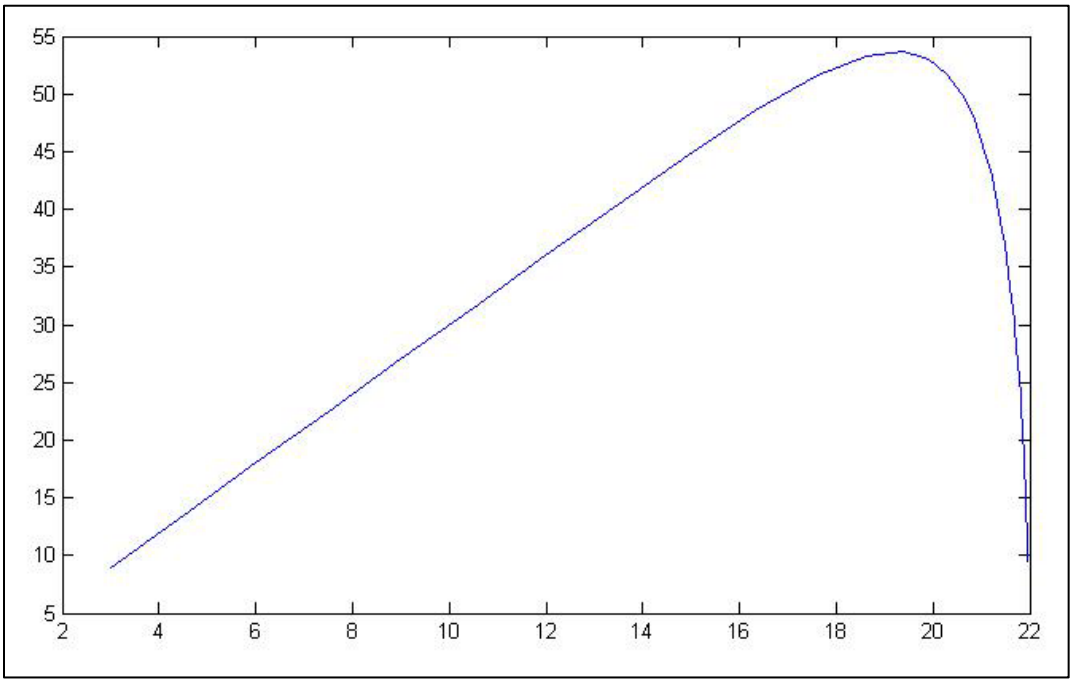

Figure 32: Module P-V Curve Modeled in Simulink

Figure 33 shows the PV module connected to a boost converter model. The boost converter switches at 100 kHz, requiring a small time step to accurately capture the circuit dynamics. Simultaneously, the continuous-time PV module requires a numerical solution to the voltage and current equations at each time step, which is a computationally intensive procedure. The combination of high computational load and small simulation step size results in long simulation run times, making the proposed simulation model impractical. A piecewise-linear PV module simulation model was used in place of the continuous-time model.

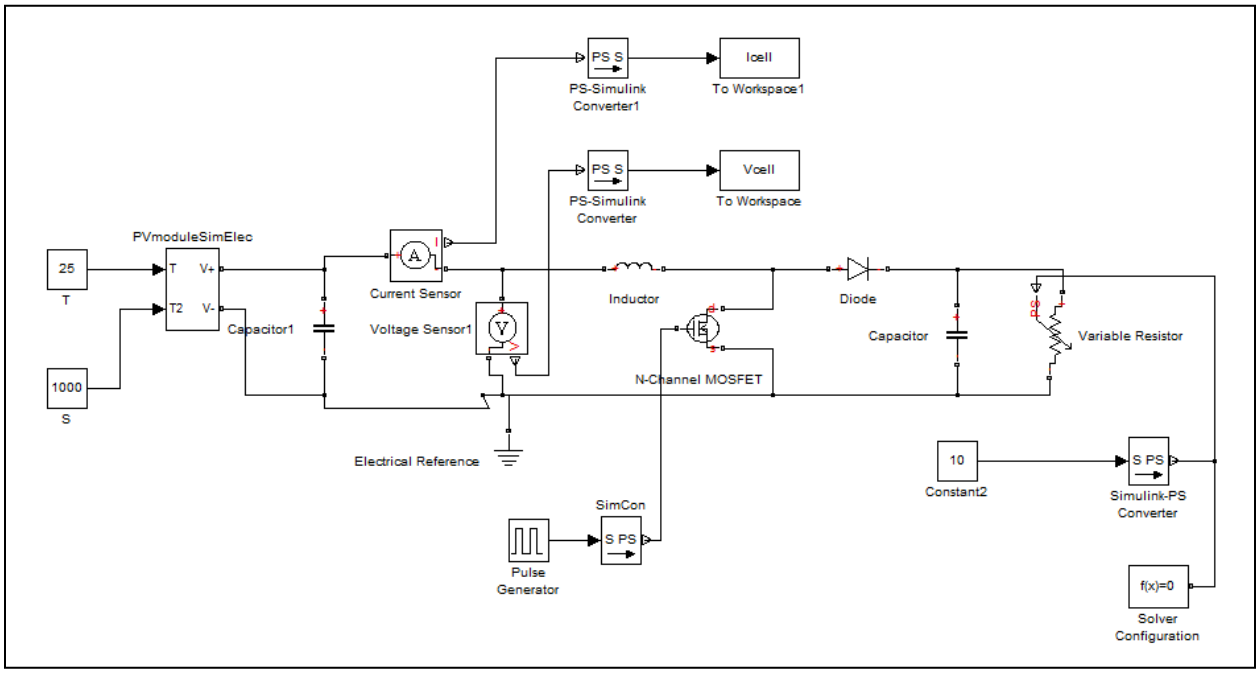

Figure 33: PV Module With Boost Converter in Simulink

7.1.2 Piecewise-Linear PV Module Simulation Model

The equivalent circuit of the PV model is modeled after the methodology referenced here [31]. This approach develops a piecewise-linear approximation to the module's I-V characteristic. This method is employed due to ease-of-implementation, and to overcome the limitations described in the previous section. As noted, alternative modeling approaches involve solving transcendental equations at every time step of the simulation, to accurately recreate continuous-time I-V curves. This approach drastically increases simulation time and for some power system studies, the resulting level of accuracy is unnecessary [31].

The framework for modeling the PV modules was amended from the reference, in order to accurately reflect the effects of partial shading on PV modules with bypass diodes. The entire model given in the reference was duplicated to create two sub-modules. These sub-modules were each placed in parallel to a bypass diode, and the two sub-modules were then connected in series. The circuit parameters provided in the reference were adjusted so that each sub-module produced the rated short circuit current, but only half of the open-circuit voltage of the full array. A MATLAB script was used to solve for the circuit parameters. This script is shown in Appendix A.

The PV module that was modeled in this work, is the BP 2150S. The operating characteristics of this module are given in Table 8.

Table 8: PV Module Parameters

Typical Electrical Characteristics[1]	BP 2140S	BP 2150S
Maximum Power (P_{max})[4]	140W	150W
Voltage at P_{max} (V_{mp})	34.0V	34.0V
Current at P_{max} (I_{mp})	4.16A	4.45A
Warranted minimum P_{max}	130W	140W
Short-circuit current (I_{sc})	4.48A	4.75A
Open-circuit voltage (V_{oc})	42.8V	42.8V
Temperature coefficient of I_{sc}	(0.065±0.015)%/°C	
Temperature coefficient of V_{oc}	-(160±20)mV/°C	
Temperature coefficient of power	-(0.5±0.05)%/°C	
NOCT[3]	47±2°C	
Maximum system voltage[2]	600V	

The following figures show the software model of the PV module, as well as its I-V characteristic, as calculated during the simulation. Note that the critical points provided on the datasheet; including the open-circuit voltage, short-circuit current, and the voltage and current at maximum power; are all identical to the parameters on the I-V characteristic of Figure 31.

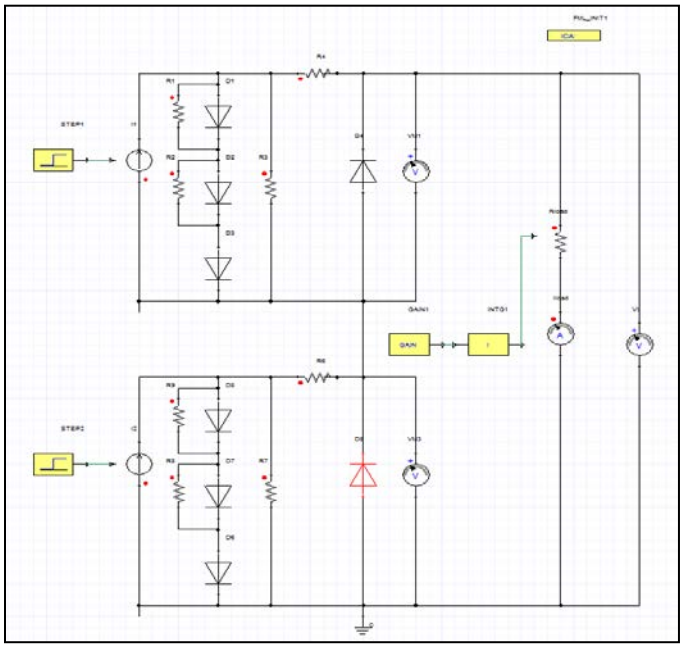

Figure 34: PV Model With Two Sub-Modules and Bypass Diodes

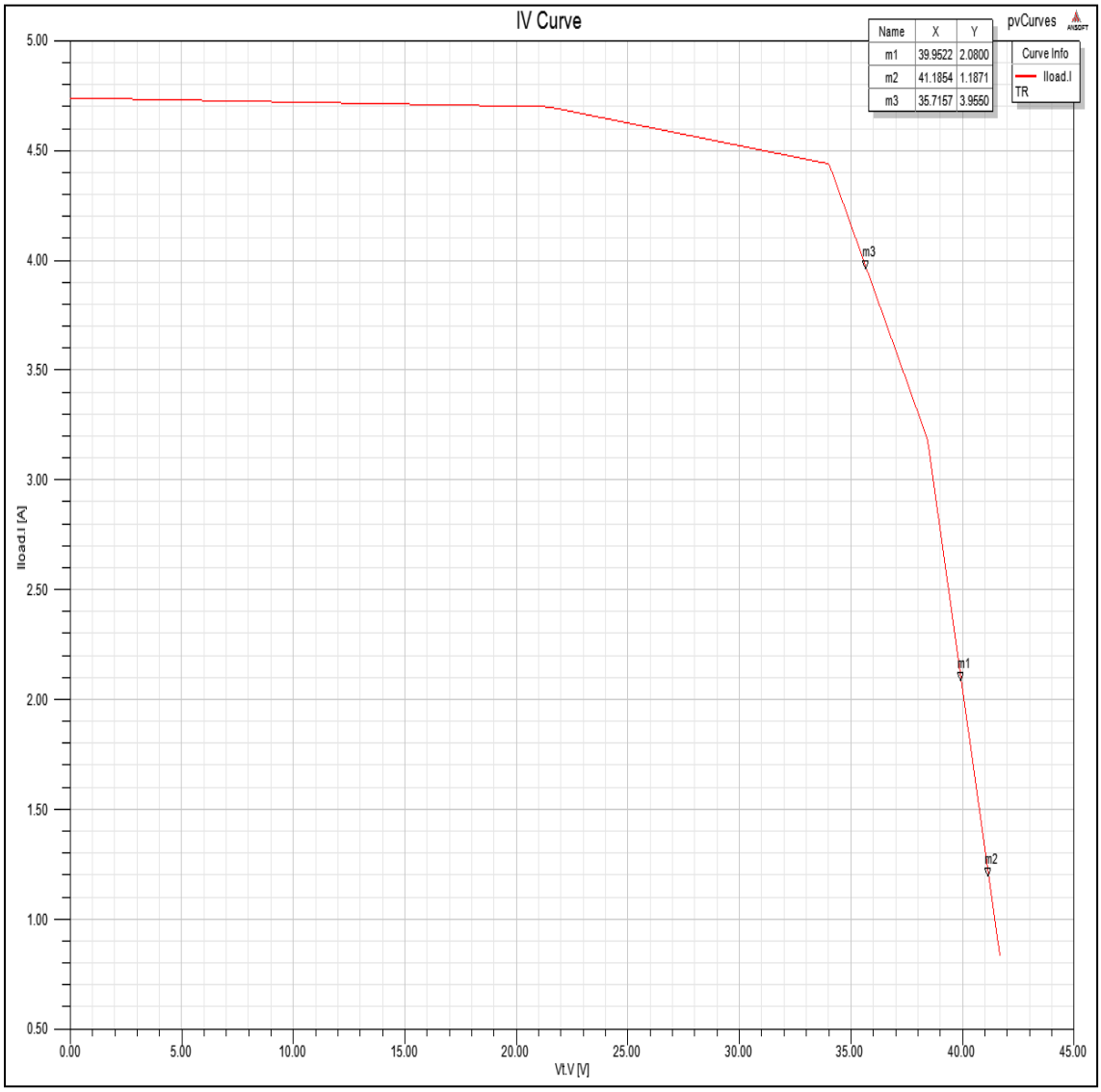

Figure 35: Modeled I-V Characteristic

Figure 32 shows the P-V characteristic of the module, as calculated during the simulation. Figure 33 shows the P-V characteristic when the second sub-module is partially shaded by 50%. Note that Figure 33 bears the same shape as the partial shading example provided in Figure 14.

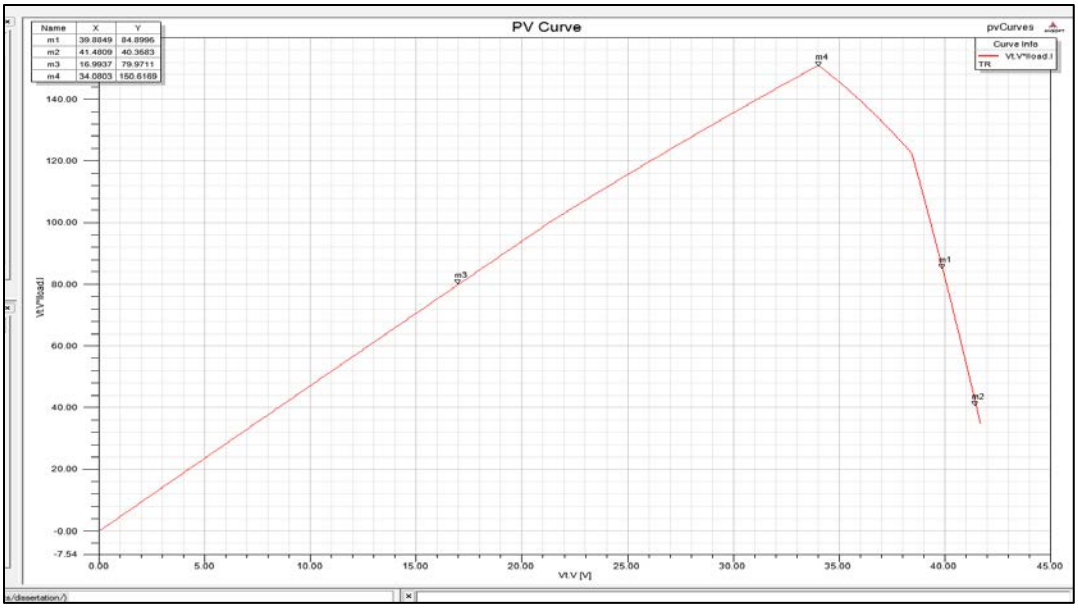

Figure 36: P-V Characteristic Under Full Illumination

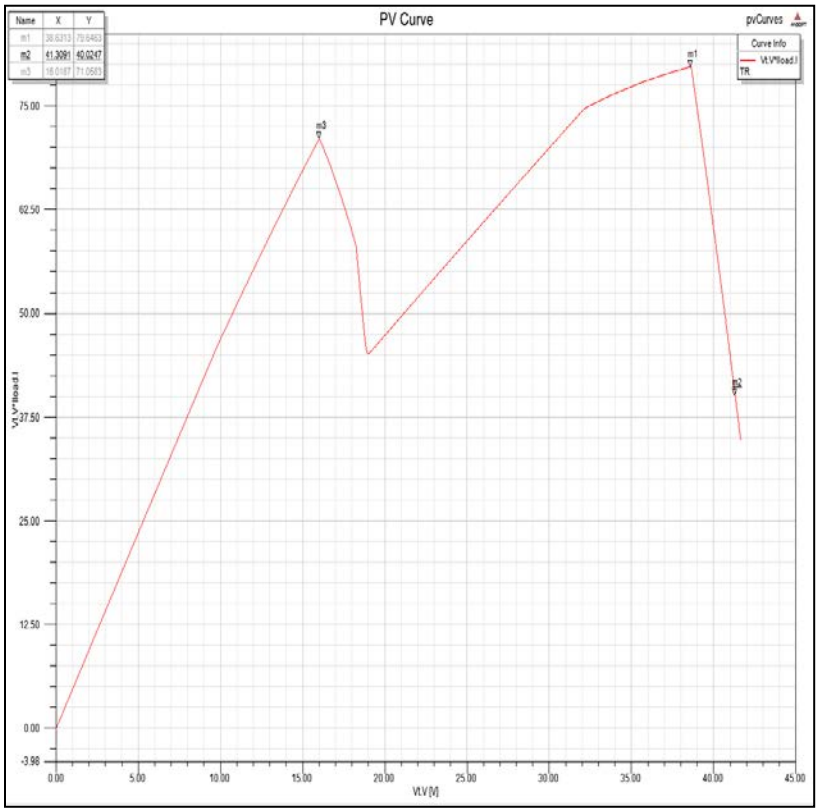

Figure 37: P-V Characteristic Under Partial Shading Conditions

7.1.3 PV Model Choice and MPPT Strategy

The two most commonly implemented MPPT algorithms are referred to as “Perturb and Observe” (P&O) and “Incremental Conductance” [17]. Essentially, both of these methods are gradient based search algorithms. Each algorithm effectively computes the rate of change of a measured or calculated circuit quantity. When using a piecewise-linear approximation for the PV module I-V characteristic in simulation, the instantaneous derivative of the current and voltage will always be zero, except at the points of discontinuity, where two line segments meet. At these points, numerical integration will produce very large magnitude non-zero values. Either way, the calculated rates of change will not be accurate reflections of the true circuit quantities. As the number of line segments in the approximation becomes large, the simulation values more closely match the expected circuit values. But for the piecewise-linear model used, with only four line segments representing the I-V characteristic, a gradient-based search method will not accurately reflect the desired control action within the converter system.

For this reason, the dynamic feed-forward approach was used with the boost converter section for operating the system at the maximum power point. For a given level of insolation, and a desired output voltage, the required boost converter duty cycle is calculated and the PWM generator is assigned this value. This method is equivalent to using a look-up table to implement the controller. This approach simplifies the control design, verifies the system operation, and allows for reduced simulation runtime and design complexity.

7.1.4 Load Variation During the Simulation

Along with variations in the converter duty cycles, the converter operating points are established by varying the load resistance across the Cuk stage terminals. It would seem as though a straightforward comparison of operating states would involve a design that uses converters at differing operating points to service an identical load. However, variations in load resistance values are representative of actual operating dynamics for load circuits.

Furthermore, the variation in load mimics the behavior of an infinite bus. For large building systems, or integration into a DC grid, the network to which the micro-converter system connects can be modeled as an infinite bus. An infinite bus has the ability to absorb all of the power instantaneously produced by the PV module. This is equivalent to saying that the load impedance value (the input impedance from the DC electrical network) changes to match the resistance at maximum power for the micro-converter system. So in the subsequent section, during the simulation testing of the converter system, both the converter duty cycles, and the load resistance change, during the verification of the system operating points.

7.2 ANALYSIS UNDER FULL ILLUMINATION

The goal of the simulation study was to verify that the converter system could simultaneously operate at the maximum power point of the PV module, while maintaining a constant output voltage. There are many MPPT algorithms that have been proposed for PV integration. In this study, the choice of algorithm was irrelevant. It was only required that the boost converter

parameters be set to allow the PV module to operate at its MPP. For the sake of this study, the required duty cycle was calculated and fed to the converter via feed forward control.

Three parameters were specified to establish the operating point of the system, namely, the boost converter duty cycle (DB), the Cuk converter duty cycle (DCUK), and the load resistance (Rload). The value of DB was arbitrarily chosen to 0.55.

The value of DCUK was chosen using the expression given in equation (120). To evaluate this expression, the midpoint voltage must be known, when the system operates at the maximum power point. To obtain the value of the midpoint voltage, the PV module and boost converter were connected in series, with a variable resistance load attached to the terminals of the boost converter. With DB fixed, the load resistance was varied over a wide range. Analyzing the power produced by the panel over the course of the simulation, it was identified that one unique resistive load value, 48 ohms, corresponded to operation at the MPP. Moreover, the voltage across this resister was 82 V when the system operated at the maximum power point.

With a midpoint voltage of 82V, DCUK was evaluated at a value of 0.368. This duty cycle ensures that the Cuk converter produced a -48 V output, while the boost converter ensured operation at the MPP. The following figures show the power delivered by the PV module, and the voltages at the PV module terminals, the circuit midpoint, and the load. Note that there is a delay in the control operation of the Cuk converter, which is apparent in the initial values of the measured parameters. Note that there is less than 5% error between the expected and calculated value of every output parameter in the circuit.

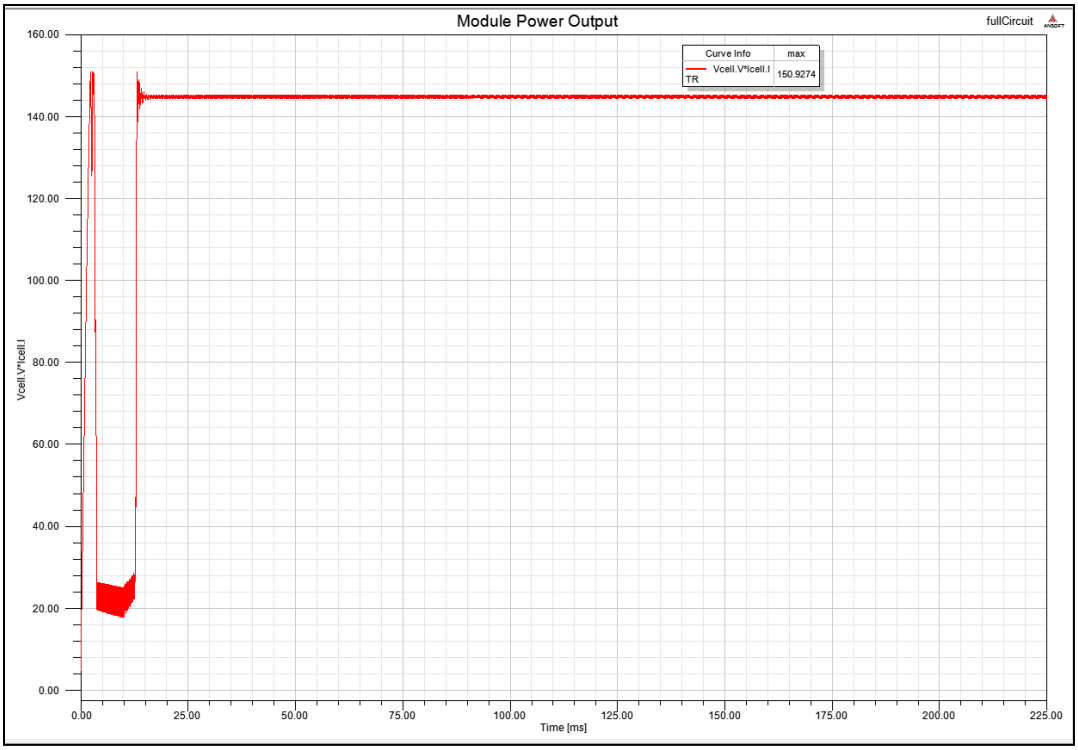

Figure 38: Power Provided by the PV Module

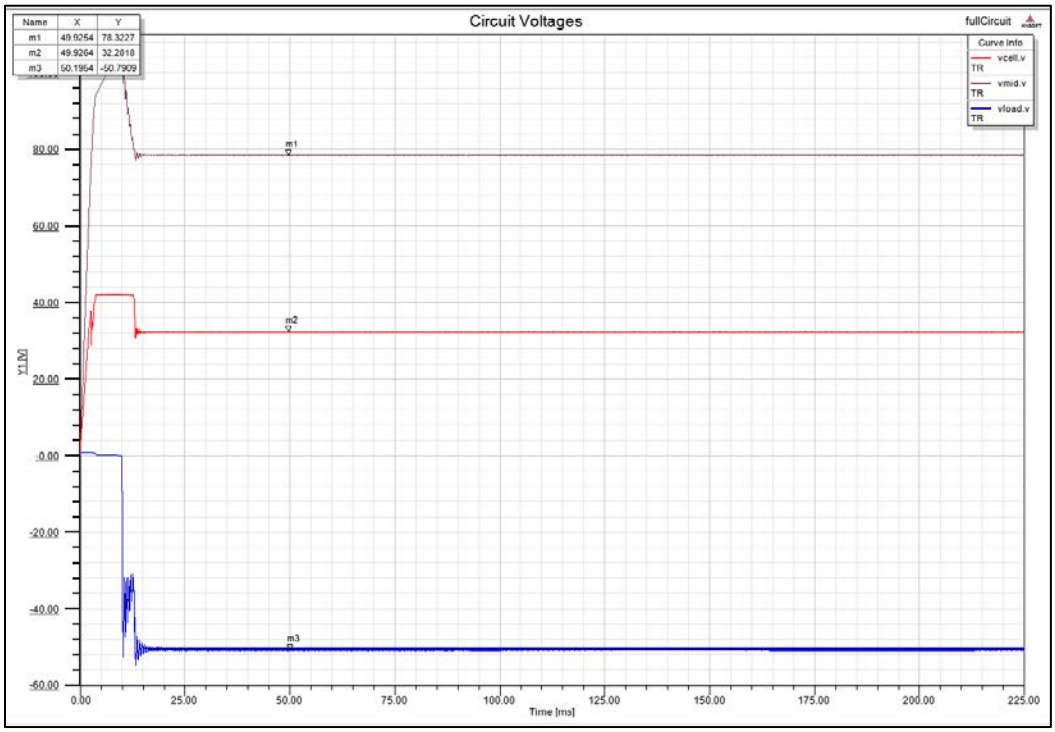

Figure 39: Circuit Voltages During Simulation

7.3 ANALYSIS UNDER PARTIAL SHADING

For the analysis under partial shading conditions, a similar procedure was followed, but with the second PV sub-module half shaded. Under partial shading conditions, the load resistance value is increased to 40 Ohms to maintain optimal operating conditions. The simulation shows that under partial shading conditions, it is possible to operate the module at its maximum power point, while maintaining a constant output voltage. The following figures show the power delivered by the PV module, and the voltages at the PV module terminals, the circuit midpoint, and the load.

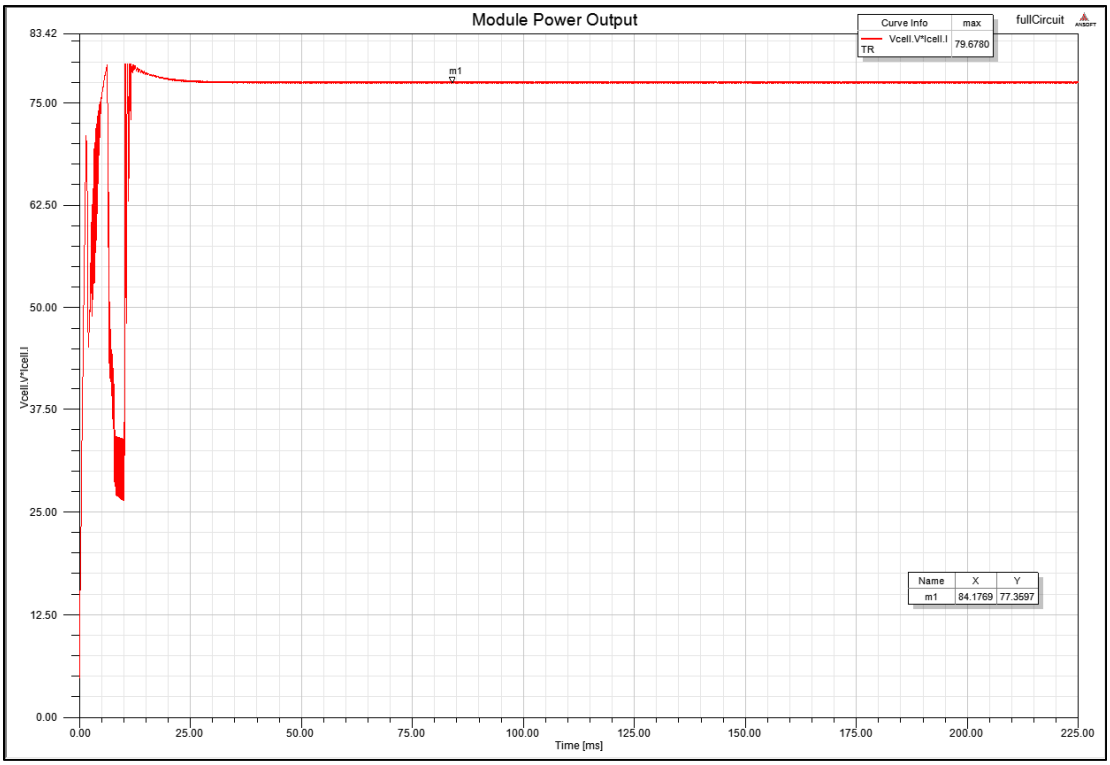

Figure 40: Module Power Output Under Partial Shading Conditions

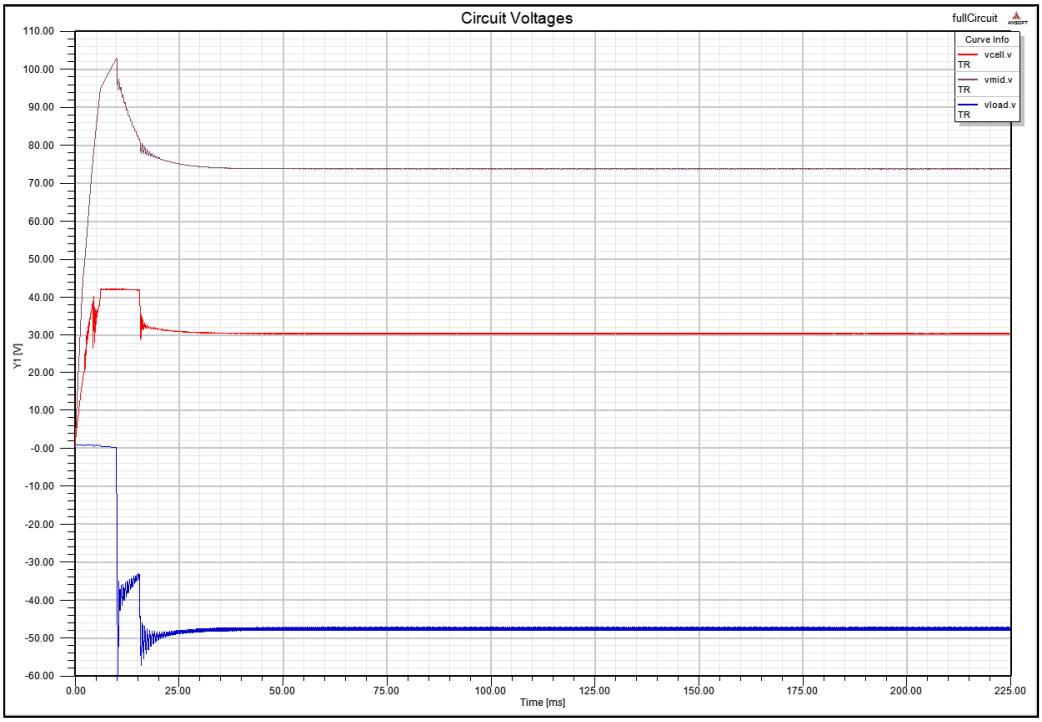

Figure 41: Circuit Voltages Under Partial Shading Conditions

8.0 SUMMARY AND EXTENSIONS

This dissertation confirms the validity of a design approach for creating a micro-converter system. This system of cascaded power electronic converters can be used to effectively integrate PV generation into DC systems. This dissertation established that the micro-converter system can be used to extract maximum power, and regulate the interconnection voltage, under conditions of full illumination and partial shading.

To extend upon the work described herein, and create a product with commercial potential, a robust feedback control system must be implemented for the converter system. An MPPT algorithm must be implemented in the boost stage, and a voltage feedback loop must be implemented in the Cuk stage. Given the right-hand plane pole present in the Cuk converter line-to-output transfer function, a simple PI compensator will not suffice to stabilize the converter system.

The Cuk converter was chosen, in part, because of its excellent filtering capabilities provided from input and output filters, and from the use of the capacitor for energy transfer. The end result is a converter with non-pulsating input current from the PV module, and low voltage ripple in the output voltage. A transformer isolated Cuk converter would offer an additional degree of system protection, while providing for a higher voltage conversion ratio, via the transformer turns ratio.

Furthermore, the concept must be demonstrated in hardware. Alternative converter topologies may be considered, to provide a balance between physical size, heat management, efficiency, and cost. In addition, different operating points may be considered. Of particular interest would be a micro-converter with a regulated 380 V DC output, for use in data center facilities.

It is hoped that developments in DC integration technologies will allow for growth in the area of DC facility design. Better DC integration technology can provide more attractive ROIs for PV systems, making PV affordable in new commercial, industrial, and even residential developments, using DC distribution technology. Through a micro-inverter device, DC facilities with PV generation can offer greater ease-of-implementation, compared to traditional AC installations. And with localized MPPT, and no mis-match losses, DC integrated PV can offer high system utilization, and near ideal system efficiency.

APPENDIX A

PV PARAMETER EVALUATION

PV module implemented as a MATLAB FUNCTION:

```
function Iout = fcn(V, T, S)
%% variable declarations
Isc0=3;
Voc0=22;
Impp0=2.77;
Vmpp0=17.98;
a=0.0004;
b=-0.0033;
c=0.066;
%Rs=0.085;
Sref=1000;
Tref=25;
%% derived parameters
```

```
Rs=(Vmpp0+((Impp0*(Voc0-Vmpp0))/((Isc0-Impp0)*log(1-
(Impp0/Isc0)))))/(Impp0+((Impp0+(Impp0^2))/((Isc0-Impp0)*log(1-(Impp0/Isc0)))));
dT=T-Tref;
Isc=Isc0*(S/Sref)*(1+(a*dT));
Voc=Voc0*(1+b*dT+c*log(S/Sref));
k=(1-Impp0/Isc0)^(Voc0/(Vmpp0-Voc0+Rs*Impp0));
Iref=1.5;
DIref=1.5;
V1=Voc-Rs*Iref*Isc/Isc0+Voc0*log(1-Iref/Isc0)/log(k);
%% numerical solution for Iref
n=0;
for n=0:1:50
   DIref=DIref/2;
   if V1<V
      Iref=Iref-DIref;
   elseif V1>V
      Iref=Iref+DIref;
   else
      n=100;
   end
   V1=Voc-Rs*Iref*Isc/Isc0+Voc0*log(1-Iref/Isc0)/log(k);
end
Iout=Iref*Isc/Isc0;
```

APPENDIX B

PIECEWISE LINEAR PV MODEL

MATLAB script for evaluating parameters of the piecewise-linear PV module:

```
%% Beginning of MATLAB script
%% declarations
clear all;
clc;
syms Rmid Rtop A B N1 N2 D1 D2 Rs Rsh R2 R3
%% input parameters
% from Sandia Database
% BP SolarBP2150s
Voc=42.8;
Vsc=0;
Vmpp=34
% half module for partial shading
Voc=Voc/2;
Vsc=Vsc/2;
```

```
Vmpp=Vmpp/2

% comment the above if modeling a full module

Isc=4.75

Impp=4.45

Ioc=0;

Ix=4.71;

Ixx=3.2;

Rmpp=Vmpp/Impp

Pmpp=Vmpp*Impp

%% resister values

Rsh = ((0.5*Voc)-Vsc)/(Isc-Ix)

Rs = (Voc-(0.5*(Voc+Vmpp)))/(Ixx-Ioc)

R2 = (Vmpp-0.5*Voc)/(Ix-Impp);

R3 = (0.5*(Voc+Vmpp)-Vmpp)/(Impp-Ixx);

N1 = Rsh*(0.001+((1e6*Rmid)/(1e6+Rmid))+((1e6*Rtop)/(1e6+Rtop)));

D1 = Rsh+((1e6*Rmid)/(1e6+Rmid))+((1e6*Rtop)/(1e6+Rtop));

A = Rs-R2+(N1/D1);

Rmid = solve(A,Rmid);

N2 = Rsh*(0.001+((0.001*Rmid)/(0.001+Rmid))+((1e6*Rtop)/(1e6+Rtop)));

D2 = Rsh+((0.001*Rmid)/(0.001+Rmid))+((1e6*Rtop)/(1e6+Rtop));

B = Rs-R3+(N2/D2);

Rtop = solve(B,Rtop);

Rmid = subs(Rmid);
```

```
Rtop=eval(Rtop);

Rtop=Rtop(2)

Rmid=eval(Rmid);

Rmid=Rmid(2)

%% forward voltages

Vbot = ((0.5*Voc)+Ix*Rs)/(1+(Rtop+Rmid)/1e6)

Vmid = (Vmpp-0.5*Voc+Rs*(Impp-Ix))*(1-(Rtop+0.001)/(Rtop+Rmid+0.001))

Vtop = Voc-Vbot-Vmid

%% end of MATLAB script
```

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