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Effect of grain alignment on interface trap density of thermally oxidized aligned-crystalline silicon films

Woong Choi,[a] Jung-Kun Lee, and Alp T. Findikoglu[b]
Materials Physics and Applications Division, Los Alamos National Laboratory, Los Alamos, New Mexico 87545

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The authors report studies of the effect of grain alignment on interface trap density of thermally oxidized aligned-crystalline silicon (ACSi) films by means of capacitance-voltage (*C-V*) measurements. *C-V* curves were measured on metal-oxide-semiconductor (MOS) capacitors fabricated on ⟨001⟩-oriented ACSi films on polycrystalline substrates. From high-frequency *C-V* curves, the authors calculated a decrease of interface trap density from 2×10^{12} to 1×10^{11} cm^{-2} eV^{-1} as the grain mosaic spread in ACSi films improved from 13.7° to 6.5°. These results demonstrate the effectiveness of grain alignment as a process technique to achieve significantly enhanced performance in small-grained ($\leqslant 1$ μm) polycrystalline Si MOS-type devices. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2424655]

Interface trap density is a critical parameter that affects the electronic properties of oxidized semiconductor surfaces, and thus the performance of various electronic devices, such as metal-oxide-semiconductor (MOS) field effect transistors.[1] For single-crystal Si-based MOS devices, the interface trap density has been known to depend on the oxidation process, substrate orientation, and interface roughness.[2,3] While MOS devices based on polycrystalline Si thin films have been of great interest for applications in thin-film transistors (TFTs),[4] little attention has been given to the relationship between interface trap density and grain alignment in polycrystalline Si films. Recently, we reported a technique that uses biaxially oriented buffer layers to grow ⟨011⟩-oriented Si thin films, called aligned-crystalline Si (ACSi), on flexible polycrystalline metal tapes with controllable grain alignment.[5–7] For the work presented here, we have fabricated MOS capacitors from ⟨001⟩-oriented ACSi films on flexible substrates and investigated the correlation between interface trap densities and grain alignment by using capacitance-voltage (*C-V*) measurements.

The ACSi films were grown on polycrystalline metal tapes (Hastelloy C-276, 100 μm thick) using a buffer layer architecture composed of γ-Al_2O_3, MgO, and Y_2O_3. Details on growth conditions can be found elsewhere.[5] All the layers were deposited by electron-beam evaporation in the following sequence: a Y_2O_3 nucleation layer (5 nm) at room temperature, a biaxially oriented MgO layer (10 nm) using an ion-assist beam of 750 eV Ar^+ at room temperature, a homoepitaxial MgO layer (100–200 nm) at 500 °C, and a γ-Al_2O_3 buffer layer (100–200 nm) at 800 °C. A heavily doped p^+-ACSi bottom electrode layer (1 μm), followed by a lightly doped p-ACSi layer (3 μm), was grown at 710–770 °C using two separate boron-doped Si sources. The doping concentrations of p^+- and p-ACSi layers were measured to be 2×10^{19} and 3×10^{17} cm^{-3}, respectively, by secondary ion mass spectroscopy (SIMS).

The crystallographic properties of the ACSi layers were analyzed by x-ray diffraction (XRD). A θ-2θ XRD scan of the multilayer indicated that the MgO, γ-Al_2O_3, and ACSi layers grew with ⟨001⟩ orientation perpendicular to the substrate surface. For the Si (004) reflection, the full width at half maximum (FWHM) of the rocking curve $\Delta\omega_{004}$ was in the range of 2.0°–4.0° for the series. The fourfold in-plane symmetry of the Si layer was confirmed by XRD ϕ scan of the 022 reflection. The average FWHM $\Delta\phi_{022}$ was distributed between 6.1° and 13.1°. The average grain mosaic spread of each sample was analyzed using the total mosaic spread (TMS) defined as $\mathrm{TMS}=(\Delta\omega_x^2+\Delta\omega_y^2+\Delta\phi_z^2)^{1/2}$, where $\Delta\omega_x$, $\Delta\omega_y$, and $\Delta\phi_z$ are the tilt along x, tilt along y, and rotation along z, respectively.[5] The crystallographic properties were also confirmed by electron backscattering diffraction. XRD analysis indicated compressive stress in ACSi films, which was also observed by Raman spectroscopy. The root mean squared (rms) surface roughness of ACSi films was measured by atomic force microscopy on a 5×5 μm^2 scale.

To form MOS capacitors, silicon oxide layers (~25 nm) were thermally grown at 900 °C for 1 h in a conventional tube furnace using dry O_2. Before oxidation, samples were cleaned with Radio Corporation of America (RCA) cleaning procedure[8] and the native oxide layer was removed with a buffered HF solution. The FWHM of the Raman bandwidth of the thermally oxidized ACSi films was measured to analyze the defect density. MOS capacitors were patterned using standard photolithography and reactive ion etch. The sputtered Al contact electrodes (80×80 μm^2, 200 nm thick) were patterned by a lift-off technique, followed by annealing in forming gas (94% Ar, 6% H_2) at 450 °C for 30 min. The *C-V* characteristics were measured at room temperature with an HP4194A impedance analyzer.

The measurement of the small signal differential capacitance of MOS capacitors as a function of gate voltage has been extensively used to extract the properties of the Si surfaces, oxide layers, and interfaces. Figure 1 shows the MOS capacitance as a function of the applied voltage measured at three different frequencies (1, 10, and 100 kHz). It also shows a schematic cross section of the MOS capacitor. The

[a]Present address: Applied Materials Inc., Sunnyvale, CA 94085; electronic mail: woong_choi@amat.com
[b]Electronic mail: findik@lanl.gov

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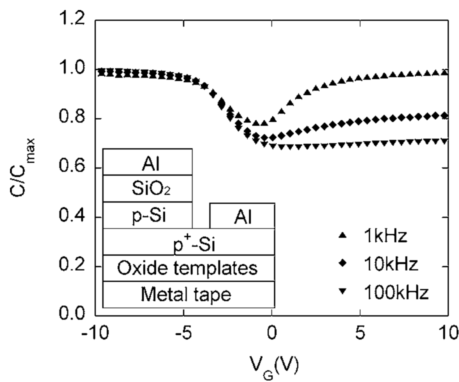

FIG. 1. Normalized capacitance (C/C_{max}) of metal-oxide-semiconductor capacitors as a function of applied gate voltage measured at 1, 10, and 100 kHz. Also shown is a schematic cross section of the MOS capacitor structure.

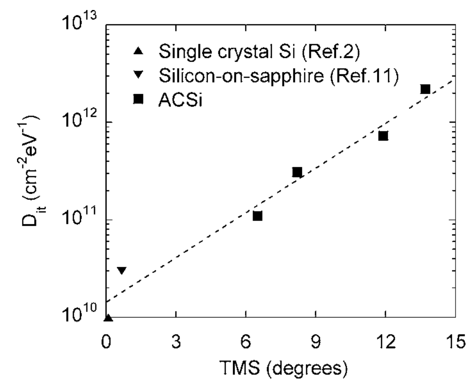

FIG. 3. Interface trap density at midgap (D_{it}) as a function of total mosaic spread. D_{it} data of single crystal Si and silicon-on-sapphire are based on Refs. 2 and 11, respectively. The dashed line is a guide for the eye.

C-V results show well defined regions of accumulation, depletion, and inversion. An accumulation capacitance appears at negative voltages, indicating that the top layer of the ACSi film is *p* type. Figure 1 also shows typical high- and low-frequency curves at 100 and 1 kHz, respectively, with a transition curve at 10 kHz. A hole concentration ($\sim 3 \times 10^{17}$ cm^{-3}) estimated from the *C-V* curve was consistent with the doping concentration measured by SIMS. The thickness of depletion layer (~40 nm) was also estimated from the *C-V* curve and was in good agreement with a known value at $\sim 3 \times 10^{17}$ holes cm^{-3} (Ref. 9).

Figure 2 shows high-frequency (1 MHz) *C-V* curves of MOS capacitors based on ACSi films with TMS values of 6.5°, 8.2°, 11.9°, and 13.7°. As the TMS value increases, the *C-V* curve stretches out further along the voltage axis, indicating higher density of interface traps.[9] Interface traps change their charge state depending on whether they are filled or empty. Because interface trap occupancy varies with gate bias, the stretch-out of *C-V* curves occurs. To determine the correlation between interface traps and TMS in our ACSi films, we calculated the midgap interface trap density (D_{it}) of each ACSi sample by the high-frequency capacitance method.[10] A uniform doping level of 3×10^{17} cm^{-3} in all four ACSi samples, experimentally confirmed by SIMS, was used for this calculation. As shown in Fig. 3, D_{it} of our Si films is reduced from 2×10^2 to 1×10^{11} cm^{-2} eV^{-1} as the TMS of the ACSi film decreases from 13.7° to 6.5°. For single crystal Si, a dry-oxygen-grown SiO_2 layer has a typical D_{it} in the 10^{12} cm^{-2} eV^{-1} range, but forming gas annealing reduces D_{it} to the low 10^{10} cm^{-2} eV^{-1} range.[2] Consistent with the case of single crystal Si, our thermally oxidized ACSi films also showed D_{it} in the 10^{12} cm^{-2} eV^{-1} range before forming gas annealing. However, for a given series of samples, D_{it} could not be reduced below 1×10^{11} cm^{-2} eV^{-1} after forming gas annealing. This may be related to grain boundary traps, but it is difficult to suggest with certainty a microscopic mechanism to describe our results. Combined with D_{it} data of single crystal Si and good-quality silicon-on-sapphire reported in the literature,[2,11] these results indicate that D_{it} decays approximately exponentially as TMS decreases (dashed line).

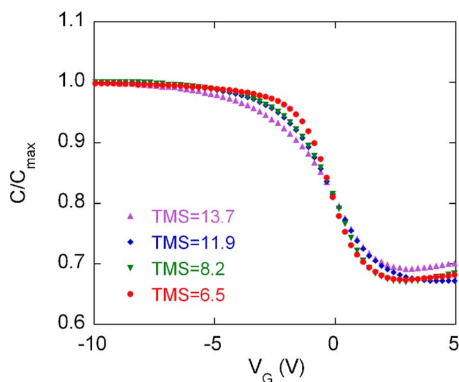

FIG. 2. (Color online) Normalized capacitance (C/C_{max}) of MOS capacitors, based on ACSi films with four different values of grain total mosaic spread (TMS), as a function of applied gate voltage measured at 1 MHz.

Since all the samples were processed under the same conditions, changes in the oxidation process were negligible. As ACSi films showed ⟨001⟩ orientation within a few degrees at the surface normal, changes of D_{it} in such a narrow range of surface orientation are expected to be insignificant.[12] It has also been known that D_{it} increases with increasing interface roughness.[3] However, while the distribution of grain size remained similar, the rms surface roughness of our ACSi films increased monotonically from 13 to 15 nm as the TMS decreased from 13.7° to 6.5°, and thus cannot explain the observed D_{it} dependence.

Interface traps are thought to originate from dangling bonds or metallic impurities at the Si surfaces.[1] Since we used the growth temperatures of the ACSi films as a variable to control grain alignment, we cannot exclude the possibility that changes in growth temperature might influence D_{it} by significantly reducing the density of dangling bonds or defects in the Si film or at its surface. However, based on the following argument, we conclude that the effect of grain alignment on D_{it} is likely to be dominant over direct growth temperature effects. The experimental techniques and models employed in this study do not allow for definitive identification of the density of dangling bonds; they let us estimate the overall trap density due to all types of defects and dangling bonds. However, with forming gas anneal (FGA) studies,[7] we have observed that the dangling bond density is likely to be negligible compared to other types of defects in well-aligned ACSi films because we have not observed any significant change in behavior with FGA in such films. Also, we measured the FWHM of the Raman bandwidth of our ACSi films to compare the defect density within Si grains (Fig. 4). The FWHM of the Raman bandwidth in polycrystalline silicon films increases with increasing defect density of the Si

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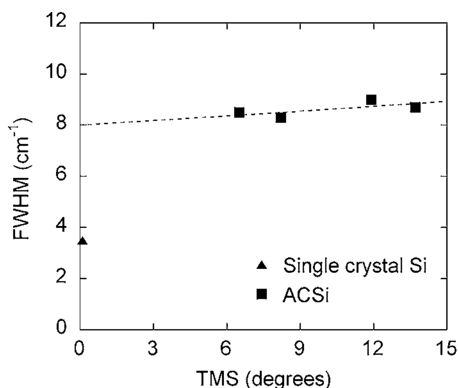

FIG. 4. Full width at half maximum (FWHM) of the Raman bandwidth of ACSi films as a function of total mosaic spread. The FWHM in single crystal Si was also measured as a reference. The dashed line is a guide for the eye.

grains.[13] For our ACSi films, the FWHM of the Raman bandwidth varied less than 10% independent of the growth temperature, indicating that the defect density within the Si grains does not depend significantly on the growth temperature that we have used. For comparison, the FWHM of Raman bandwidth measured on single crystal Si is less than 50% of that on ACSi films.

Microstructural and electrical measurement results in previous publications already indicated that improving the grain alignment of small-grained ($\leqslant 1\ \mu$m) ACSi films produced effectively the same results that increasing grain size does.[5–7] This study showed that the interface trap density also decreases significantly as grain alignment improves. Therefore, ACSi process could be considered as an effective alternative to fabrication methods in TFTs, where a laser annealing method is typically used, such as sequential lateral solidification[14] or selectively enlarging laser crystallization.[15] Currently, no other technology combines the high-performance aspects of single crystal silicon with the low-cost aspects of polycrystalline silicon films, which use inexpensive, non-single-crystalline substrates. As such, the ACSi process could allow the Si industry to lower its costs while maintaining or improving the performance of its products.

In conclusion, we have studied the relationship between grain alignment and interface trap density in MOS capacitors fabricated using ⟨001⟩-oriented ACSi thin films on polycrystalline substrates. Based on the high-frequency capacitance method, we calculated the interface trap density, which decreased from 2×10^{12} to 1×10^{11} cm^{-2} eV^{-1} as the grain mosaic spread decreased from 13.7° to 6.5°. These results indicate that improved grain alignment could lead to significantly reduced interface trap density in polycrystalline Si films, with potentially important implications for TFT applications.

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