MODULAR MULTILEVEL CONVERTER BASED HIGH VOLTAGE DC PROTECTION

by

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B.S. in Electrical Engineering, University of Pittsburgh 2012

Submitted to the Graduate Faculty of

the Swanson School of Engineering in partial fulfillment

of the requirements for the degree of

Master of Science

University of Pittsburgh

2014

UNIVERSITY OF PITTSBURGH

SWANSON SCHOOL OF ENGINEERING

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University of Pittsburgh, 2014

This thesis addresses the protection of a high voltage DC (HVDC) system that utilizes the modular multilevel converter (MMC) topology, a voltage sourced converter (VSC), and incorporates two transmission line sections, a cable and an overhead line. Protection for high voltage AC systems is mature in installation experience. On the other hand there are many avenues of research needs for the protection of the more modern technology, HVDC.

The avenue of system protection focused upon in this work is the system restart sequence post DC side faults. This restart sequence is simply the sequence of events that occur necessarily in order to restart the HVDC system after a specified fault is already isolated and diminished. This avenue of system protection is focused upon but not exclusively. Fault isolation and suppression are also protection topics noted and discussed. Ultimately a fault section identification protection method is required for restart of the HVDC system when there are two transmission line sections. Specific to the HVDC system design presented there is desire for no communication channel between the converter stations of the system. Additionally, recovery of the system to normal operation is preferably as fast as possible in order to maintain power delivery with minimal disturbance. Solutions to these challenges are investigated and proposed.

The first part of this thesis work involves the detailed modeling of the MMC-HVDC system in the PSCAD simulation environment. After providing the validation of the model, both a parameter sensitivity analysis and an in-depth fault case analysis are performed for the overall

examination of protection needs of the HVDC design. The fault analysis evaluation brings to light the means for a unique protection coordination method for the system design during post-fault system restart. The protection method ensures that cable faults, assumed to be permanent faults, are not reclosed upon while for any non-permanent faults attempt of reclose is made. The protection coordination method proposed in this work is unique in that it utilizes a signal characteristic to the HVDC system design to implement protection coordination without the use of a communications channel between converter stations.

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ACKNOWLEDGMENTS

First of all, I want to acknowledge and thank my family for their support and love. I especially thank my beautiful wife, Heidi, for taking care of me, being extremely supportive of my educational efforts and for encouraging me to do the very best that I can to the glory of God. I also thank my parents and siblings for being the best family that anyone could ask for. The childhood that I had with you has prepared me in so many ways for where I am today.

I thank my academic advisor, Dr. Greg Reed, who has made this exceptional educational opportunity a reality. I am also greatly appreciative of the guidance of a few other professors at the University of Pittsburgh, namely Dr. Zhi-Hong Mao, Dr. Bill Stanchina, and Dr. Tom McDermott. At this point I take a moment to mention a great big thank you to Brandon Grainger my colleague, now Dr. Brandon Grainger my professor. You have been a mentor, a brother in Christ, and a friend throughout my graduate career. I also acknowledge all of my fellow graduate colleagues that I have had over these past two years and some. I look forward with anticipation to continuing the collaboration and the good times that I have had with you all. I also thank the industry sponsors of this research for their collaborative effort and guidance.

Lastly I acknowledge and thank both my church family and most importantly my heavenly Father. The faith and grace that God has given me has guided me through each step of my life. He has given me the gift of pursuing an education, an opportunity to be a difference maker, and I seek to be a good steward of the life that He gives.

1.0 INTRODUCTION

As an introduction to the thesis work presented, a background of HVDC transmission technology is given. The reason for researching specifically MMC-HVDC is described. Necessary background of protective relay technology is also covered. For clarification the conditions of the desired MMC-HVDC protection design is defined. Additionally the motivation and the contributions of the work are presented. Lastly, the content of each chapter is briefly explained before delving into the body of the thesis.

1.1 BACKGROUND

High Voltage Direct Current (HVDC) is rapidly becoming a predominant choice over high voltage alternating current (HVAC) for many applications of modern transmission projects due to its desirable benefits [1],[2]. HVDC is defined as a DC transmission system incorporating power electronic based controls and other static controllers to enhance system controllability, control power flows, and improve power transfer capability. HVDC transmission is especially desirable for applications that require long distance power delivery due to significantly higher operational efficiency as compared to HVAC. Another application for which it is specifically desirable to utilize HVDC is subsea cable transmission, also for the reason of more efficiently delivering the power. An example of a subsea application is offshore wind generation,

transmitted to shore by subsea cables [2],[3]. Another example of subsea cabling would be transmission of power from one land mass to another with a channel of water between [4]. Future needs of bulk power transmission and subsea cable applications will be met with HVDC technology. With the increased penetration of wind power on the U.S. both offshore and in the Midwest, there will be increased need for subsea cabling and long distance bulk transmission applications. This thesis work supports these applications by analyzing long distance HVDC transmission specifically including two sections to the HVDC line, a cable section (subsea) and overhead (OH) line section (above ground).

HVDC technology is based off of two different converter designs, the line-commutated converter (LCC) and voltage sourced converter (VSC). The classical LCC-based HVDC technology, also known as classic HVDC, is based upon thyristor-based technology. LCC-HVDC is a mature technology with robust reliability, low losses, and a successful history. Advances in semiconductor technology has made VSC-based HVDC possible, utilizing primarily the IGBT (insulated gate bipolar transistor). The IGBT is capable of switching frequencies significantly faster than thyristors. Low switching frequencies is a disadvantage of LCC. VSC is now becoming the choice converter design over LCC in HVDC applications [2]. There are a number of VSC-based converters; the topology of study in this work is the modular multilevel converter (MMC) due to its numerous advantages.

The VSC-based modular multilevel converter (MMC) topology is desirable for HVDC applications due to the number of advantages it can offer in comparison to other topologies [2], [5]. The MMC topology, depicted in Figure 1, boasts a number of advantages over traditional VSC multilevel designs including its high modularity in hardware and software, low generation

of harmonics, lower switching frequency of semiconductor devices, easily scalable, and, most importantly, a stronger approximation of a sinusoidal output with increasing submodules [5], [6].

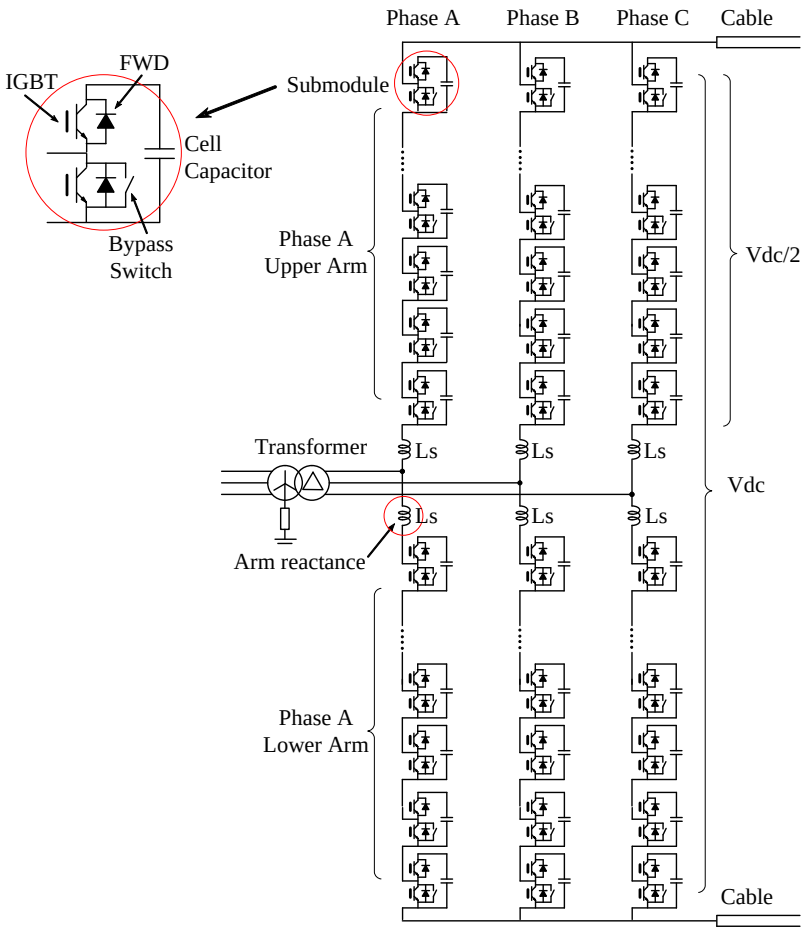

Figure 1: Schematic of the Modular Multilevel Converter Topology

Due to HVDC being choice for future bulk transmission and subsea installations, combined with the advantages of MMC-HVDC in particular, it is desired to minimize or eliminate entirely any hindrances or weaknesses of the technology. There is need of minimizing the weaknesses of MMC-HVDC so that the numerous benefits can be utilized, so that MMC-HVDC can become a viable competitor with the mature technologies.

Extensive literature reviews are provided for the MMC topology, modulation, and control in [1] and [5], controller design in [1] and [7], and protection needs in [6] and [8]. In a HVDC transmission system there is a need to address the protection needs of the MMC-HVDC technology design. Protection for AC systems is a mature technology, but on the other hand DC systems have many opportunities to investigate protection needs. There is a need to research DC side fault scenario events and to propose how to handle these events in terms of protection [8]. Especially with the introduction of VSC-HVDC and an increase of VSC systems being installed, the protection of these systems needs to be spoken to.

In protecting MMC-HVDC from DC side faults, there are two exclusive options of a device to implement: 1) DC circuit breaker technology [9], [10], or 2) traditional AC circuit breaker technology combined with custom relay protection coordination on the DC side [8],[11]. The first method has drawbacks. Primarily, DC circuit breaker technology on a high voltage scale is immature and expensive at the present time [1]. Therefore the second method will be investigated. The MMC-HVDC system analyzed in this work will include AC circuit breaker technology.

There are two primary protection challenges facing the MMC-HVDC system design: 1) fault current must be extinguished quickly so that the converter fault withstand rating is not surpassed as well as so that a system restart sequence can commence as soon as possible, and 2) the fault location must be quickly identified so that the system can restart to normal operation as soon as possible maintaining power transmission. The first challenge is a future work item, outside the scope of this thesis work. The second challenge is the primary problem addressed in this work, and a solution to this problem is proposed in chapters 4 and 5.

To expound upon the second challenge, the need is to attempt reclosing the circuit breakers upon non-permanent faults scenarios on the HVDC line and to not reclose the circuit breakers upon permanent fault scenarios. The HVDC line for the design in this work is made up of two sections, a cable and an OH line section. Fault scenarios that occur in the OH line section are potentially non-permanent faults. AC circuit breaker attempt of reclose is then desired. Fault scenarios that occur in the cable section can be assumed to be permanent. AC circuit breaker reclose is not desired. It is therefore desired to identify the fault section in order to know whether or not to attempt ACCB reclose. In order to maintain transmission operation as often as possible, it is crucial for an HVDC system to feature a system restart sequence that restarts the system as quickly as possible post a fault case scenario. This work will propose a system restart sequence that will incorporate protective relay coordination with ACCBs to implement a fault section identification protection method.

When considering protective relay technology there are a few items to describe before continuing further. Fault section identification has been attempted in multiple ways on various types of systems by use of the following methods: wavelet transform, Kalman filtering, neural network, and vector support machine [12], [13], [14]. These solutions can be marginally effective in achieving section identification, but they are calculation heavy, consuming precious time, in determining the section. Fault location identification, identifying the exact location along the transmission distance, could be applied for the purpose of section identification by use of distance (or impedance) protective relaying or traveling-wave based protective relaying, but again these methods are time consuming even if they are marginally effective. Additionally, location identification performs more work than necessary when simply section identification is desired. The exact location of the fault in terms of distance from a converter station is

unnecessary when the desired information is to know whether the fault is located in the cable or OH line region of the HVDC line. All that is necessary to resolve the specific section identification challenge is to identify which section the fault is located in, the cable or OH line section. This work proposes a solution, novel to the HVDC design specified, that identifies the section without performing time consuming location identification.

Protective relay coordination for transmission systems most often requires a communications channel between the converter stations [15]. This is primarily due to the fact that most transmission relay protection is in the form of line current differential protection which requires a communications channel inherent to the relay function [15]. Communications in protection inherently slows down the process of restarting the transmission system after a fault event. Communications are also expensive especially for transmission and can often be unreliable [16]. For the purpose of faster fault isolation and faster system restart, it is desired to design a protection coordination scheme that does not utilize a communications channel. Examples of noncommunication relay coordination protection design are found in [16]–[19]. These examples all fall into the category of relay protection where detection of local circuit breaker operation is depended upon by the relay protection operations. This desire for noncommunication relay coordination protection is set as one of the conditions on the MMC-HVDC protection design proposed through this thesis work.

More protective relay functionality will be presented in chapter 5, but there is one more detail to be considered in defining the conditions set on the MMC-HVDC protection design, the number of signal samples stored in relay memory. A relay stores a certain number of samples of the fault current or voltage signals at a specific sampling frequency. For example, the relay protection in [14] samples at 1kHz and keeps 10 samples in memory. These specifications

change depending upon the relay being used. For the sake of protection method speed, it is desirable for a relay to make a protective action decision in as few memory samples as needed. Speed is everything when protecting against faults. This condition of minimum relay memory samples is set upon the proposed protective solution applied to the MMC-HVDC design.

The protection needs for an MMC-HVDC system is the premise of this thesis. The specific protection need addressed in this work is fault section identification in order to enable fast protection coordination during system restart. Included as future work, is the quick suppression of MMC circulating fault current, expounded upon in the conclusion of this work. The end result of this thesis is the proposal of a fault section identification protection method.

1.2 MMC-HVDC PROTECTION DESIGN CONDITIONS

Throughout the discussed background, certain conditions were set on the HVDC design being considered. In summary of these conditions, the desired HVDC transmission design includes the MMC topology, a two section transmission line, and AC protection devices (ACCBs) in protecting against DC side fault scenarios. Two desired conditions are to implement the proposed fault section identification protection method without the use of a communications channel and to minimize the number of stored fault signal samples upon which the relay protection coordination design depends. Remember, the motivation is to restart power transmission as quickly as possible for the reliability of power delivery. The full list of the desired MMC-HVDC design conditions to be met are listed here:

- Both cable and overhead line sections making up the HVDC line
- HVDC technology implementing the MMC topology

- Only AC protection devices utilized in protecting against DC side fault scenarios
- Communication-less protection coordination between converter stations for faster fault isolation and system restart
- Minimize required fault signal memory samples upon which the protection coordination design depends

Figure 2 is a diagram of this HVDC system design. Terminal *A* and terminal *B* are depicted in this figure, essentially giving terminology to the AC grid connections located on the left and right of the DC system. Terminal *A* is also termed as the sending end of the system while terminal *B* as the receiving end, since power flow as a reference is defined from terminal *A* to terminal *B*. The various other system components are also labeled in this figure.

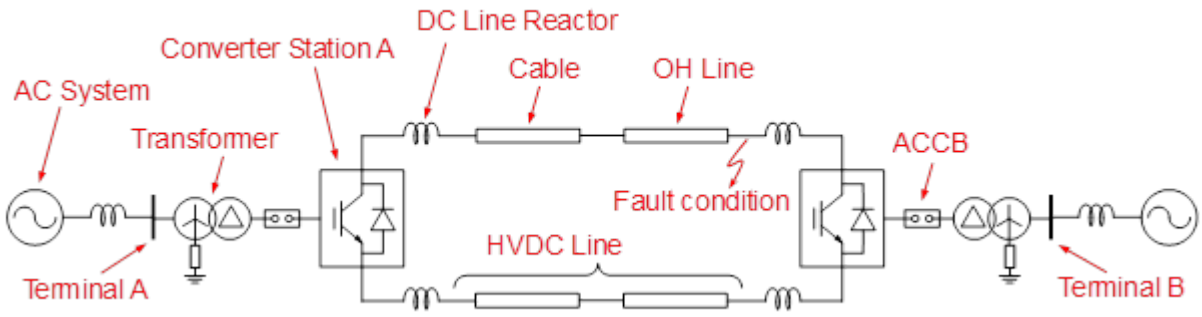

Figure 2: HVDC System Design with Cable and Overhead Line Sections Making up the HVDC Line

1.3 MOTIVATION AND CONTRIBUTIONS

This work is the development of a protection scheme to account for all faults on the DC side of an MMC-HVDC system specifically for a design including both overhead (OH) line and cable sections making up the overall HVDC line. The overall motivation of this work is to equip MMC-HVDC technology to overcome its draw backs and implementation challenges so that its

benefits might be utilized. The primary problem tackled in this work is the challenge of fault section identification in attempt of system restart. The motivation specifically for a fault section identification method is reliability of power delivery. As an end result, a reclose will be attempted for any DC side fault that is potentially non-permanent, and consequently a restart to normal operation is achieved as frequently as possible and as quickly as possible.

Ultimately the contribution of this work is to equip future installations and product lines of MMC-HVDC technology. This work is one more step in supporting the implementation of the beneficial technology. Specific contributions from this work include the trends of MMC-HVDC component sensitivity analysis, awareness of how an MMC-HVDC system responds to a comprehensive list of faults, and a protection coordination scheme uniquely applicable to this promising HVDC system design. There is also considerable significance in the contribution of a fault section identification method incorporated into relay coordination without using a communication channel and without the use of DC circuit breakers. This contribution is ultimately the speed in which the system is restarted after a fault scenario.

1.4 CONTENT ROAD MAP

Now that an MMC-HVDC background has been portrayed along with the protection problem that motivates this work, the process in achieving a solution can be presented. This process is simply organized by chapter. The second chapter describes the detailed modeling of the MMC-HVDC system in the PSCAD environment. Both MMC circuit theory implementation and validation of the model are presented. This is the foundation of the entire work. Validation of the MMC-HVDC model shows that the fault protection analysis will result with expected fault

response dynamics. The third chapter presents a trends analysis of the various system elements and components. A sensitivity analysis is performed upon each primary system parameter to determine its impact on DC fault current. This parametric trends analysis is constructive for fine tuning the selection of system parameters for a fault protection analysis. This analysis is also useful for observing which parameters are critical in the design of MMC and of HVDC systems. The fourth chapter presents the fault protection analysis performed and presents the primary results that were found to be useful in support of the protection method design to be achieved. A signal, characteristic to the HVDC design, was identified through analysis of the results and proved useful for the implementation of a fault section identification protection method. This signal is proven to be an expected system dynamic through circuit analysis. The fifth chapter presents the proposal of the fault section identification method. This chapter presents the overall protection coordination design to be applied to the desired HVDC design with all design conditions met. A summary of conclusions are then given along with a description of future work to be performed.

2.0 MMC-HVDC SYSTEM MODELING

Through this second chapter, the theory and modeling of the monopolar HVDC system within the PSCAD/EMTDC simulation environment is presented and validated. The converter station topology is based upon the Modular Multilevel Converter (MMC) arrangement. All system parameters utilized within this chapter's validation model are provided. Various details of the modeling are documented in this section including a circuit synthesis of the MMC converter, MMC capacitor initialization and balancing procedures, controller implementation (DC and AC voltage, current, and power regulators). The method for tuning the controllers, as well as all references used to aid in the model development are presented. With the theoretical platform established, PSCAD simulation results are provided showing model behavior. Graphical results include a validation of the capacitor balancing algorithm, controller dynamic behavior, and standard system checks that illustrate that the model is performing as expected.

In this work, there are 60 submodules modeled per converter station (10 cells per arm) resulting in 120 total including both converters. This number of cells (submodules) was selected according to modeling experience acquired in the modeling process. The selection was based upon adequately capturing fault current magnitudes and maintaining an IEEE 519 specified level of total harmonic distortion (THD). Various numbers of cells were simulated and 10 cells were chosen in conclusion. The challenge of

For clarity Figure 2 provides a diagram of the HVDC system in its entirety, labeling the portions of the model in order to lay a foundation of understanding of the system model from a high-level view.

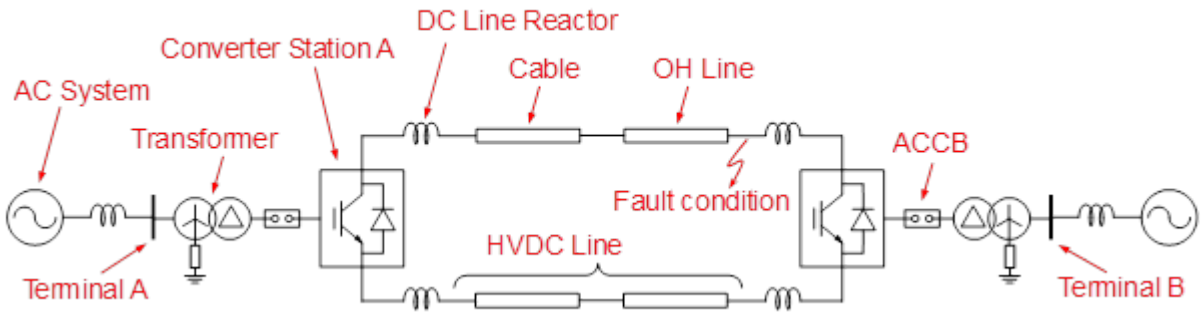

Figure 3: One-Line Diagram of HVDC System

2.1 MODULAR MULTILEVEL CONVERTER MODELING

A detailed model of the MMC-HVDC system was created in the PSCAD/EMTDC simulation environment tool. A detailed model was created, as opposed to the option of an approximate or average model, for the purpose of observing the dynamics generated by the switching states of the submodules inherent to the modular multilevel converter design. When faults occur on an MMC-HVDC system, the energy dissipation from the submodule capacitors needs to be modeled as closely as possible. It is desired to observe the circulating currents typical for an MMC topology upon a fault scenario. This requires that we model the converter in detail including an algorithm for capacitor energy balancing to replicate an actual system as close as possible. With these items being necessary for the accurate simulation of faults on the HVDC system, a detailed

model was created. The level of detail was limited by the fact that device physics were not modeled. This was deemed unnecessary for the purposes of this work. In the end, the peak fault current magnitudes observed on the system are a primary concern to be modeled accurately. Energy dissipation of the submodule capacitance is modeled as closely as possible to measure peak current magnitudes accurately, but device physics does not significantly weigh into these measurements.

2.1.1 System Parameters

It is important to begin by defining the parameters that were used in the model and describing the reasoning behind these parameters. The parameters defined for this initial test system were gathered by a combination of student research and discussions with industry contacts. With all sources considered Table 1 lists the parameters decided upon for the initial validation model. Note that this parameter list is preliminary. Further analysis documented in the next chapter aids the exact selection of each parameter value based upon a trends analysis.

Table 1: HVDC System Parameters for Validation Model Development

Rated AC RMS Voltage	500 kV
Rated DC Voltage	± 500 kV
Short Circuit Capacity	25000 MVA
Rated Power of Converter	1000 MW
Nominal Frequency	60 Hz
Submodule Capacitance	300 uF (10 cell/arm system)
Transformer Reactance	0.25 p.u.
DC Line	0.0 H
Transformer MVA Rating	1050 MVA
Transformer Turns Ratio	1:1
Arm Reactance	10% at bottom of lower arms
Line Length	1000 km

These system parameters have had a history of revisions. Only the final set of validation model parameters are provided here. Calculations, values and explanations are provided here for the model development parameters.

AC System

The rated 500 kV voltage was selected due to typical high voltage transmission rating in the U.S. market. The frequency of 60 Hz is selected also because it is standard for a U.S. market. A short circuit current range was selected according to typical U.S. market ratings based off of discussions with industry personnel.

$$I_{SC} = 11kA - 63kA$$

The short circuit capacity of the system was calculated with the following calculations. Observe and note that the short circuit current of 63 kA dictates the worst case scenario corresponding to a short circuit capacity of 55,000 MVA.

$$S_{SC} = I_{SC} V_{rated}^{new} \sqrt{3} = (11kA)(500kV)\sqrt{3} = 9{,}500MVA$$

$$S_{SC} = I_{SC} V_{rated}^{new} \sqrt{3} = (63kA)(500kV)\sqrt{3} = 55{,}000MVA$$

Transformer

The transformer connection type (Y-Δ) was selected based off of typical transmission line installations. The rated capacity (1050 MVA) was selected based off of a typical 500 kV transformer. The reactance value for the transformer was selected based off of a typical 500 kV transformer installation.

Advised from industry contacts, an X/R ratio of 100 was applied to the transformer impedance and resistance. While holding to an X/R ratio of 100 and keeping the transformer reactance selected, we obtain a corresponding transformer resistance value. This resistance value is calculated as shown here.

$$\frac{X_{p.u.}}{R_{p.u.}} = 100$$

$$R_{p.u.}^{new*} = \frac{0.25\,p.u.}{100} = 0.0025\,p.u.$$

This per unit transformer resistance was inserted into our model.

Converter

The rated AC voltage is 500 kV according to the system rating selected. The rated DC voltage is ±500 kV, equivalent to 1000 kV. The measured voltage difference from the positive to the negative terminals on the DC side of the converter is 1000 kV.

$$V_{DC} = 500kV - (-500kV) = 1000kV$$

The power rating of 1000 MW was selected, and the rated converter current was calculated accordingly.

$$I_{converter}^{new} = \frac{P}{V} = \frac{1000MW}{500kV} = 1000A$$

DC Line Reactor

There is a potential need for a DC line reactance in the system, but for the purpose of the initial validation model no DC line reactance was used. The DC line reactor is not implemented in the initial model being described in this chapter. This parameter was being neglected until the model functioned appropriately. DC line reactance and resistance was applied for the various fault analysis cases presented in the next chapters of this work.

DC Line

In the end there is need for both a cable and an overhead (OH) line model to simulate the multi-section DC line totaling at a 1000 km line. A 1000 km DC cable was employed for initial testing of the model. This cable implementation was based on the availability of reliable

references for DC cables. With industry advisement, a ± 320 kV rated cable model (electro-geometric model) was imported into PSCAD for the purposes of validating the simulation model. Because the desired design is rated for ± 500 kV, another electro-geometric based cable model that meets that specification was found, based on [20]. A PSCAD graphic of the cable model with material radii is provided in Figure 4 based off of this reference.

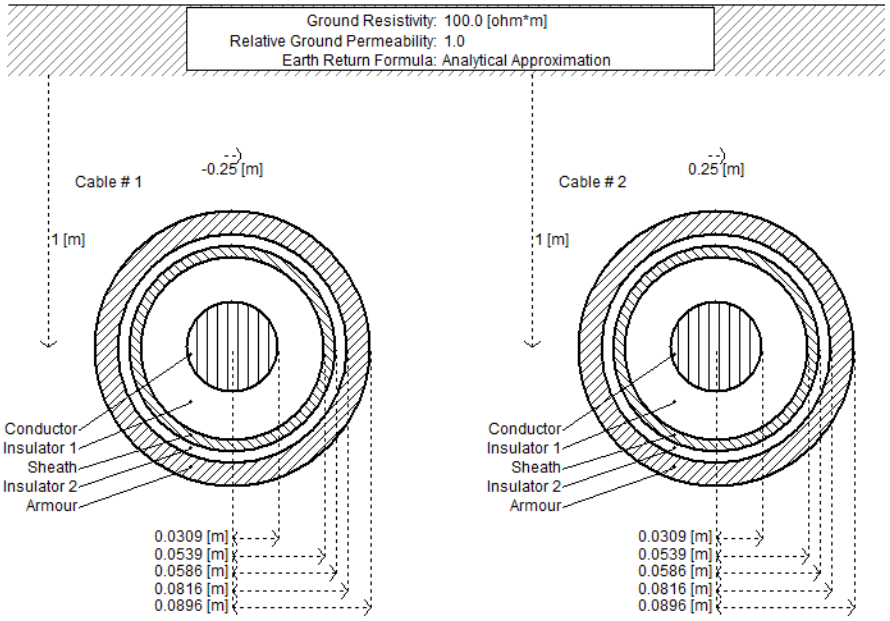

Figure 4: PSCAD Cable Model between Converters Rated for +/- 500 kV DC

The overhead line PSCAD model was based off of data gathered from literature as well as textbook references [20], [21]. The OH line model is based off of an actual ± 500 kV DC OH line located in Gochang County in South Korea [20]. Conductor data was collected from the second edition of Power System Analysis and Design by Glover and Sarma [21]. Cardinal conductor data was implemented. The details GMR (geometric-mean radius) of 0.0122834 meters and the DC resistance of 0.06083 ohms/mi at 25 degrees Celsius were selected according

to these sources. A PSCAD graphic of this OH line model with specific structure dimensions and associated details displayed [20] is provided in Figure 5.

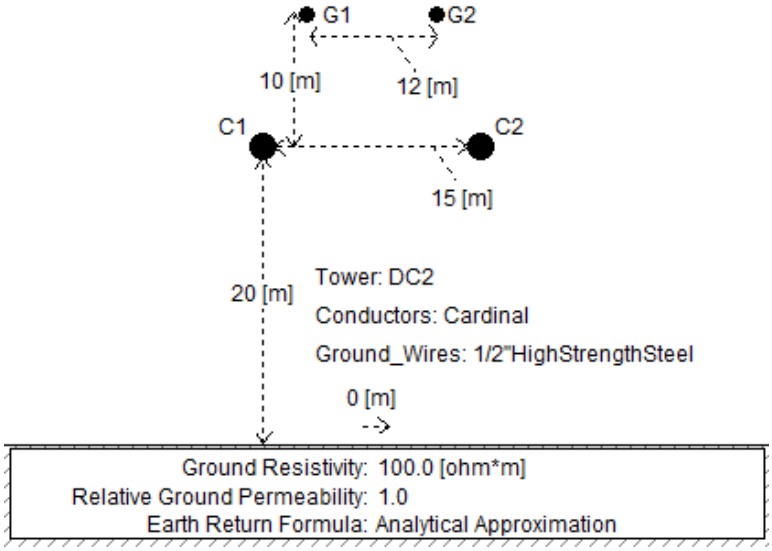

Figure 5: PSCAD Overhead Line Model Rated for +/- 500 kV DC

The end result of the model incorporates 500 km of this OH line model and 500 km of the cable model described. This combination of models was ultimately used in any PSCAD simulation associated with the proposal of the section identification method or with the parametric trends analysis. But for the initial validation model presented in this chapter, 1000 km of the cable model is implemented.

MMC Configuration

The IGBT and diode drop voltages are not applicable for system validation purposes or for the purposes of this work. These intrinsic details do not need to be captured in a "system" model of the converter stations. For an actual system, hundreds of submodules would exist and consequently the cell capacitance would be quite small. However, rather than modelling

hundreds of cells per arm as would be fitting for a 500 kV, 1000 MW system, only ten were used for modeling purposes. To properly scale the capacitance to the system, the value from the 6 cell model presented in [7] was chosen as a starting point. From here a conversion was employed to properly size the capacitors for this model.

$$C_{ref} = 2500\mu F$$

$$C_{new} = C_{ref} \cdot \frac{N_{new}}{N_{ref}} \cdot \frac{S_{new}}{S_{ref}} \cdot \left(\frac{V_{DCref}}{V_{DCnew}} \right)^2 = 2500\mu F \cdot \frac{10}{6} \cdot \frac{1000MVA}{50MVA} \cdot \left(\frac{60kV}{1000kV} \right)^2 = 300\mu F$$

Thus a capacitance value of 300µF is used for each submodule capacitance in the model.

2.1.2 MMC Circuit Synthesis and Capacitor Initialization

The modular multilevel converter (MMC) topology design for the HVDC converter station is shown in Figure 6. The topology boasts a number of advantages over traditional multilevel designs including its high modularity in hardware and software, low generation of harmonics, lower switching frequency of semiconductor devices, easily scalable, and, most importantly, a stronger approximation of a sinusoidal output with increasing submodules [3].

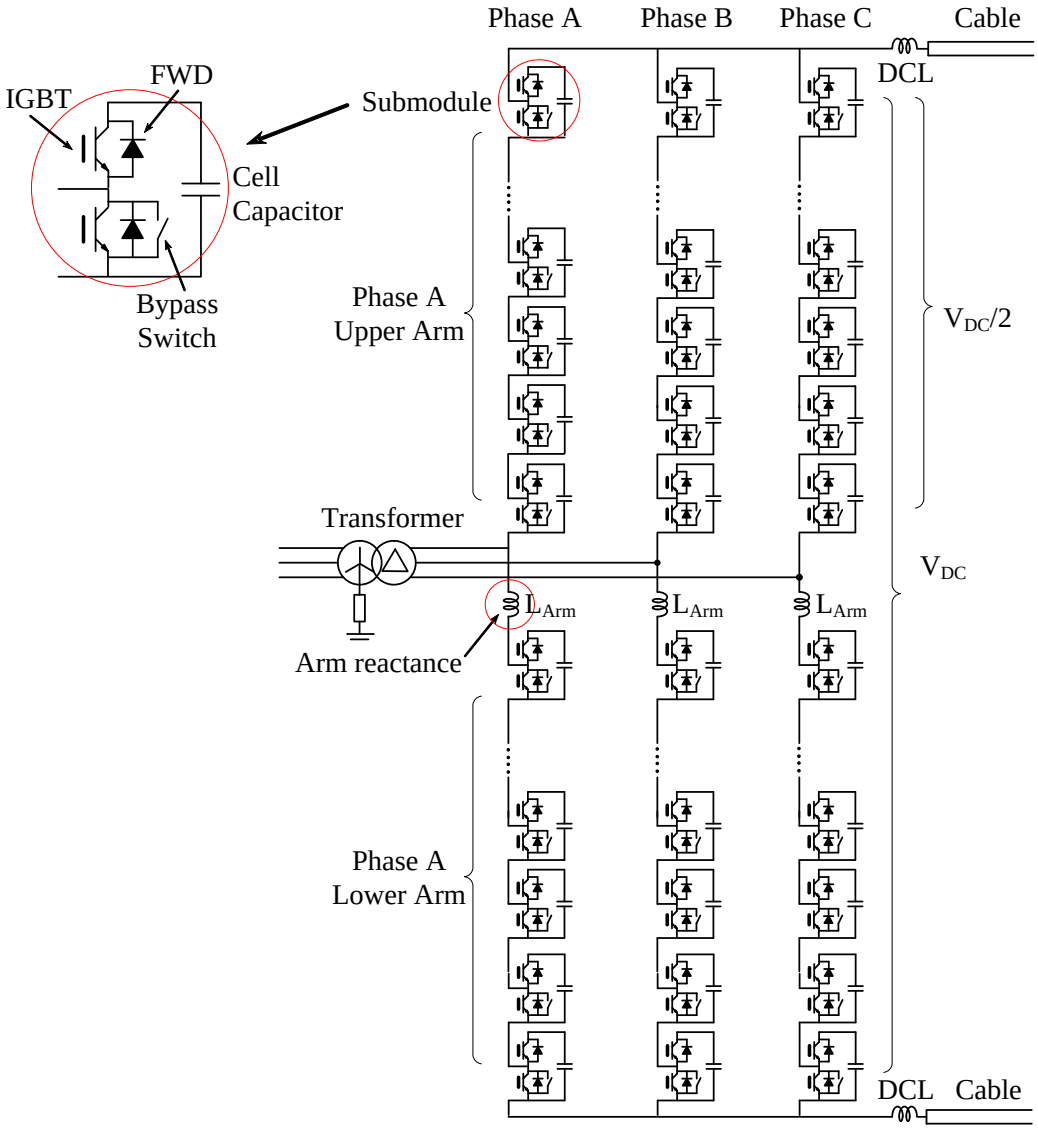

Figure 6: Modular Multilevel Converter Schematic

The MMC in Figure 6 can consist of *n* series-connected half-bridge submodules on each of the six arms, two arms per phase. Figure 6 shows an example with *n* series-connected submodules. For the validated model presented in this report, the number of submodules, or *n*, is 10. For the entire two converter configuration, there are 120 submodules, 60 submodules per converter. On each phase arm, inductances, L_{Arm}, are placed to provide current control and limit fault currents [7]. The bypass switch in parallel with each submodule is typically a press-pack

thyristor used to protect the endangered freewheeling diodes in the case of a fault. A single thyristor is usually enough if the aim is to protect the diode from overcurrent. Recently, research teams have proposed a double thyristor switch to allow the MMC to more quickly clear the fault current and restart power transmission after nonpermanent faults on overhead lines [6]. These discussions will be continued in following sections of this work.

Each MMC submodule consists of a half bridge cell where its output voltage is either equal to its capacitor voltage or zero depending on the switching states (two states). The two switches per submodule are complimentary in nature. The submodule voltage V_{sm} takes on the value of 0 volts or the voltage on the capacitor depending upon which switch is ON and which is OFF. Figure 7 demonstrates this submodule operation. The operation directly depends upon the binary input to the IGBT switches (S1 and S2) specific to each submodule. When $V_{sm} = V_C$ the submodule as a whole is considered ON. When $V_{sm} = 0$ the submodule is considered OFF.

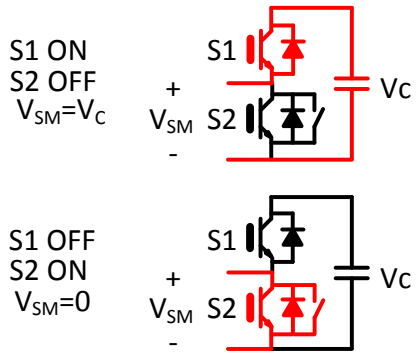

Figure 7: Submodule Operation

From the perspective provided by Figure 6 and Figure 7, equation (1) can be easily determined based on Kirchoff's voltage law for each phase, *j*. Note that for equation (1), *S* takes on the value of 0 or 1 depending on the switching state of S1 in the submodule. A subscript of

"upper" or "lower" signifies submodule position in the arm, above or below the AC midpoint of the converter. Located adjacent to this midpoint, variable L_S is the inductance of the arm reactor, [7]. This inductance L_S is clearly marked in Figure 6 on each of the six converter arms.

$$\begin{aligned} V_{dc} &= V_{upper,j} + V_{lower,j} \\ &= \sum_{i=1}^{6}\left(S_{upper,i}V_{capacitor,i}\right) + \sum_{i=1}^{6}\left(S_{lower,i}V_{capacitor,i}\right) + L_s\left(\frac{d}{dt}i_{upper} + \frac{d}{dt}i_{lower}\right) \end{aligned} \tag{1}$$

The number of levels in the AC output of the converter is a function of the number of modules in series per arm. The modulation strategy utilized for our study to synthesize an eleven-level (n+1) waveform at the ac-side of the converter is a standard phase disposition sinusoidal pulse width modulation technique (PD-PWM). To extend the linear operating range of the PWM strategy and increase the fundamental component of the AC-side line voltage of the MMC, third harmonic injection principles are utilized, [22]. Third harmonic injection is further discussed within the control section of this chapter.

In general for one converter station designed with the MMC topology, there are a total of 2n capacitors per phase in the upper and lower arms. At any instant, only n capacitors can be turned ON in the circuit. Mathematically in terms of switching functions, equation (2) must always hold true for each phase, j.

$$\sum_{i=1}^{n} S_{upper,i} + S_{lower,i} = n \tag{2}$$

Understanding this constraint offers the opportunity to illustratively describe how the output voltage waveform is built using eleven (n+1) levels with Figure 9. Notice that this constraint is ultimately what makes it possible to convert from AC to DC. While the output AC voltage changes by levels of submodule capacitance voltage to create a sinusoidal output at the

AC terminal, the DC terminal maintains a constant voltage because of the fact that only *n* submodules are ON at any given instant. This concept is clearly visualized with Figure 8 (based upon a 6 submodule system [$n = 6$] for a theoretical example).

When considering a theoretical example system with 6 submodules (n = 6), the system is considered a 7 voltage level system (n + 1). To achieve Level 7 all upper switches of one arm must be turned ON ($V_{sm} = V_C$) while all lower switches of the same arm must be turned OFF ($V_{sm} = 0$). To achieve Level 6, the first 5 upper switches closest to the arm reactor must be turned ON and one lower switch closest to the arm reactor must be turned ON with all other switches OFF. Figure 8 provides a visual aid of these voltage level changes on the Phase *A* branch of the MMC. This pattern continues until the approximate sinusoidal waveform is established based upon 7 levels. Further detail of the switch synthesis can be found in [7].

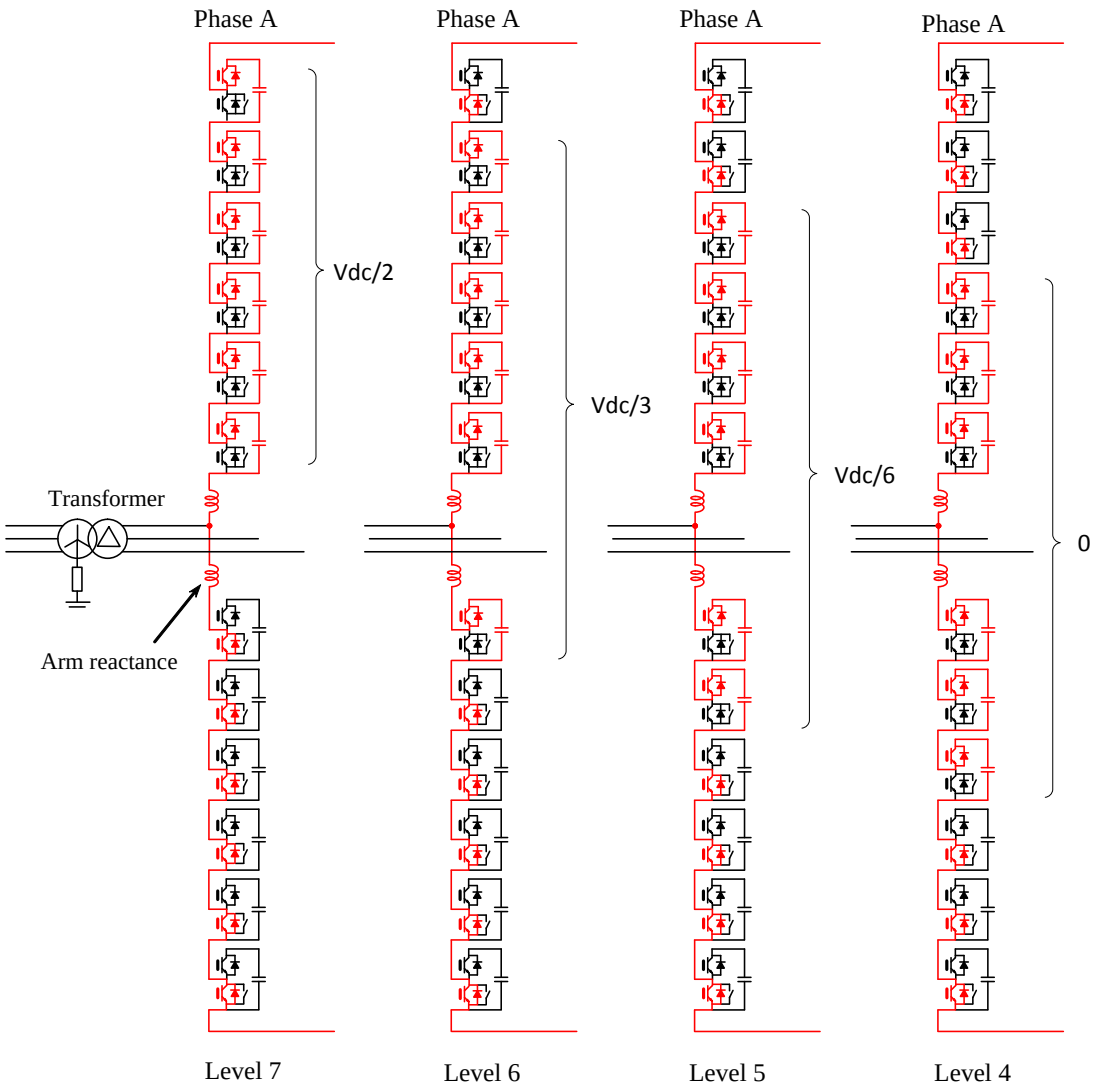

Figure 8: Demonstration of the Controllable Voltage Levels of the Multilevel Converter Based upon a Six Cell System (*n* = 6)

This approximate sinusoidal waveform based upon 7 levels is the AC line-to-neutral voltage. The line-to-neutral voltage specifically defines the multilevel converter capability (*n* + 1 levels). With 7 submodules per arm, the converter presented in this example from Figure 8 is a 7 level converters because *n* is equal to six. With 10 submodules per arm, the converters presented in this validation model are 11 level converters. While the line-to-neutral voltage is

defined by having n + 1 levels, the AC line-to-line voltage waveform is defined by having $2n$ – 1 levels. Thus for the modeled system with 10 cells:

$$n+1=10+1=11 \text{ levels}$$

$$2n-1=2(10)-1=19 \text{ levels}$$

Figure 9 shows the MMC line-to-neutral AC voltage output from the PSCAD model. The line-to-neutral voltage has 9 voltage levels when we would obtain 11 according to our equations above. These 9 voltage levels are as expected though because we have lost the highest and lowest levels (as indicated in Figure 9 where levels 1 and 11 are nonexistent in the plot) corresponding to an m (modulation index) being equivalent to approximately 0.83 at the time. With an m of 1.0, all 11 voltage levels would be seen. Model validation is further developed in Section 3.

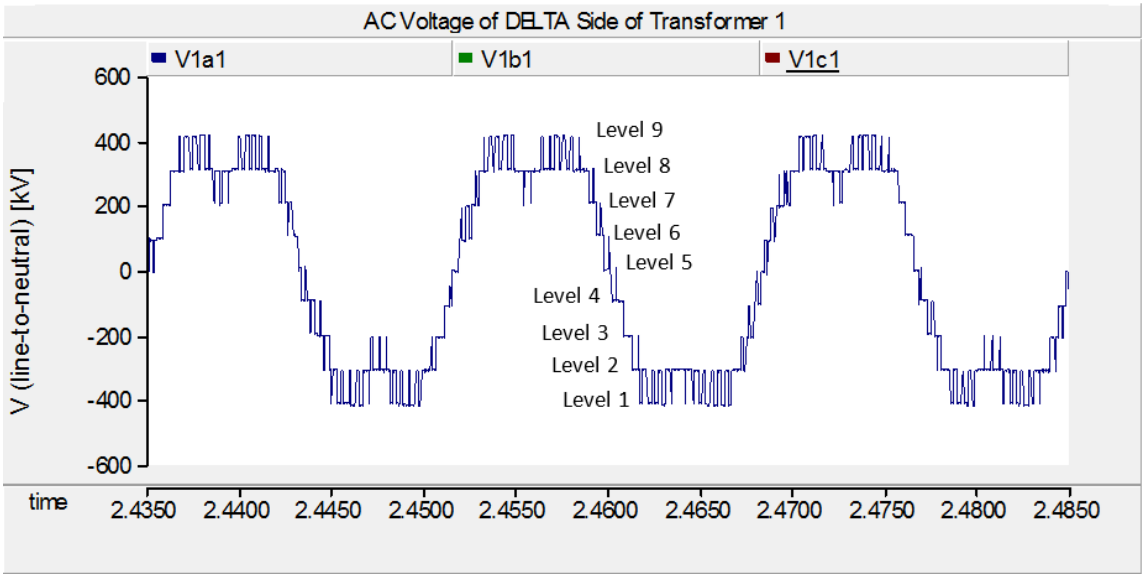

Figure 9: Line-To-Neutral AC Voltage Output of MMC Converter

While modeling the described system, a challenge arose due to initialization of the model in the PSCAD environment. Starting from zero voltage on the system, where all cell capacitors started from an uncharged state, the system model could not establish expected steady-state behavior. The model was incapable of charging up the voltage from a cold start. Therefore a modeling strategy was needed to initialize a specified voltage on all cell capacitors. The strategy implemented was to start the system with DC sources inserted in parallel to each submodule capacitor charging the capacitor until each capacitor was charged to a specified voltage.

Figure 10 shows a PSCAD view of the entire MMC converter, as well as a close up of one submodule to provide a visual of the switched in parallel DC source per submodule. These DC sources are initially included in the circuit and disconnected by switching logic at 0.10 seconds, a time at which all submodule capacitors are ensured to be fully charged to the specified voltage.

Upon a complete charge of all capacitors, the DC sources would be switched out of the circuit then allowing the appropriately charged capacitors to take over the system operation in a stable voltage state. Without this capacitor charging initialization strategy the system was not capable of starting in a stable enough state to operate correctly. Once this initialization strategy was implemented, the process of accurately modeling the system could proceed.

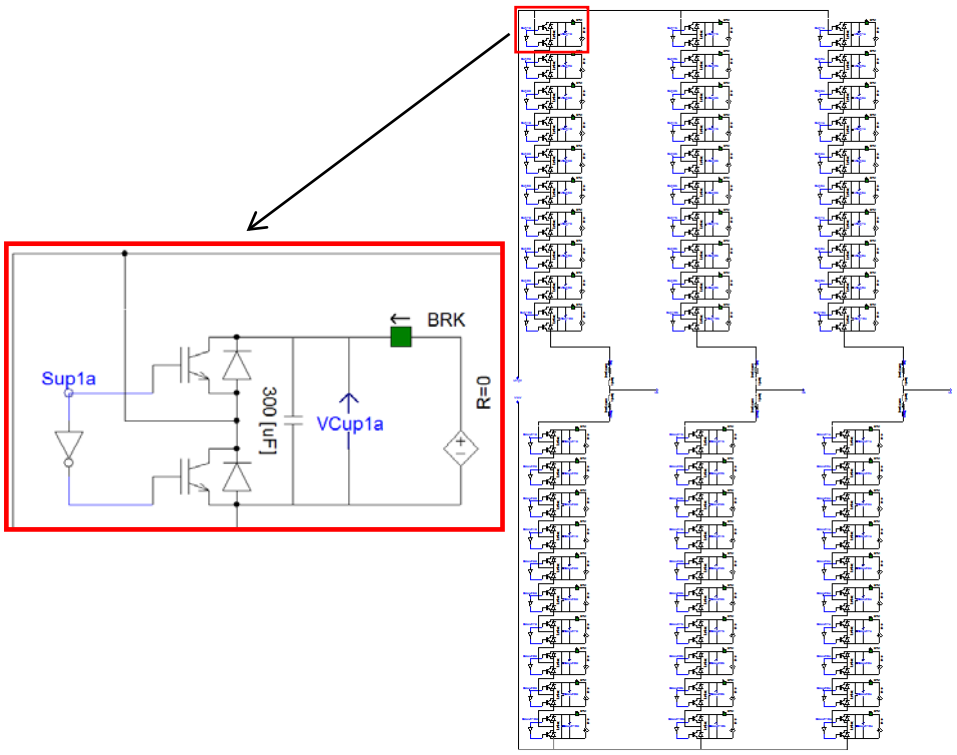

Figure 10: Demonstration of Voltage Initialization within the PSCAD Environment (not final PSCAD model)

The specified initializing voltage chosen for this model validation was 100 kV per submodule capacitor. At steady-state, each submodule capacitor will be charged to 100 kV in order that 10 capacitor voltages add up in series to a total voltage of 1000 kV at all times. Remember that *n* capacitors out of 2*n* capacitors per phase will at all times be turned ON. These *n* capacitor voltages (*n*=10 for this model validation) add up to the necessary 1000 kV.

$$V_{C,ref} = \frac{V_{DC}}{N_{Cells}} = \frac{1000kV}{10} = 100kV$$

Validation of the PSCAD HVDC system model is provided at the end of this chapter. Voltage initialization and voltage control illustrations will be provided with corresponding PSCAD diagrams. It will be displayed that each submodule capacitance is charged to 100 kV by

the parallel DC sources, and then at 0.1 seconds the system will begin switching normally with DC sources switched out.

2.1.3 Capacitor Balancing Algorithm

A problem that arises if left unaddressed is a voltage imbalance between the various capacitors in a given arm. This is due to the different rates at which the capacitors are switched, resulting in more charge being stored in the capacitors that are switched the least frequently. To remedy this problem an algorithm was implemented based on that demonstrated in [7], which relies on selection of cells based on capacitor voltage and the direction of current flow. The capacitor balancing algorithm can be separated into three distinct steps: determination of the number of conducting cell capacitors per arm, sorting of cells based on capacitor voltage, and selection of the conducting cells based on current direction. These steps are described here:

1. Calculate the number of ON cells in upper and lower arms based on the value of the voltage reference compared to ten carriers.
2. Sort the cells in each arm based on ascending voltage magnitudes.
3. If the current in an arm is positive, select ON cells based on ascending capacitor voltage. If the current in an arm is negative, select ON cells based on descending capacitor voltage.

In a given phase of the converter, there must be exactly ten cell capacitors conducting at any given moment in time. As discussed previously, this can be represented by the following equation (3).

$$\sum_{i=1}^{n} S_{upper,i} + S_{lower,i} = 10 = n \tag{3}$$

In order to determine the total number of upper and lower cells that must be on, a comparative algorithm was used. This algorithm compared a third harmonic injected sinusoidal waveform to a series of ten triangular carrier waveforms which evenly divided the magnitude of the reference.

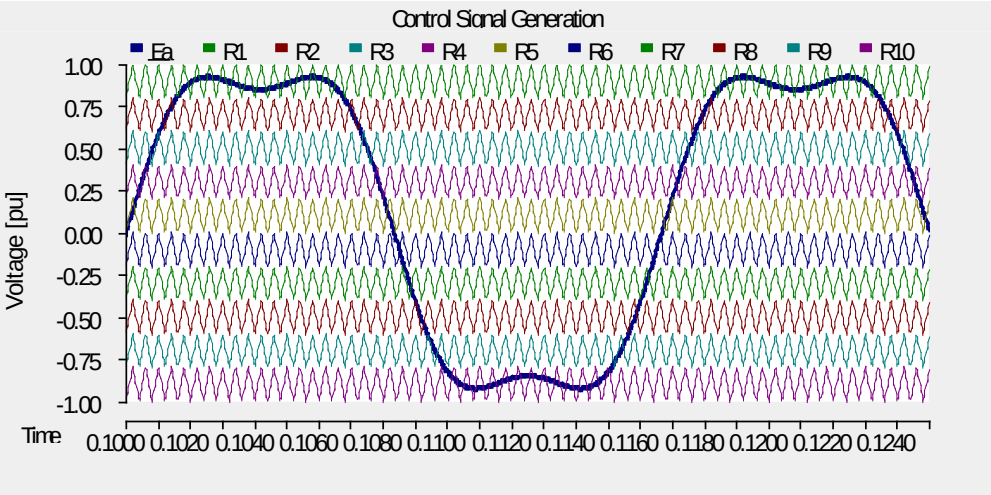

Figure 11: Reference and Carrier Waveforms for Switching Algorithm

Each carrier signal was tied to a comparator. The output of each comparator was equal to 1 when the reference voltage was greater than its corresponding carrier signal and otherwise equal to 0. The outputs of all of the comparators for a given phase were summed, which was equivalent to the total number of necessary ON cells for the upper branch of that phase or Nup_a. The same was done for the inverse of the comparator outputs, yielding the total number of necessary ON cells for the lower branch of the same phase or $Ndown_a$. This system is shown in Figure 12.

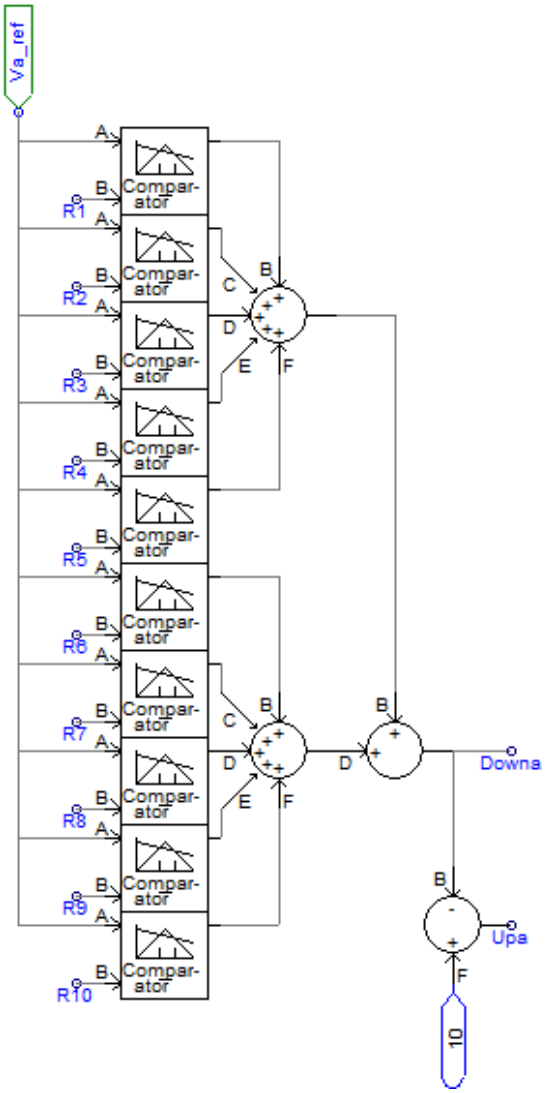

Figure 12: Calculation of the Number of ON Cells in the Upper and Lower Arms of Phase A

The next step was to sort the cells in the upper and lower arms of a given phase in order of ascending capacitor voltage. The sorting algorithm chosen was a standard bubble sort, which was chosen for its simplicity in terms of implementation in the PSCAD environment. The bubble sort functions by comparing each capacitor voltage to the next one and pushing the higher voltage towards the top of the array. This process is repeated until the voltages are in ascending order. However, rather than outputting the array of capacitor voltages, the function block that was implemented instead outputs the indices of the corresponding switches. Thus, if cell 5 in the

upper arm had the highest capacitor voltage, the last element of the output array would be 5. This sorted array was sent as output.

The final step of the voltage balancing method was the selection algorithm. This module had 3 inputs: the number of cells ON in the given arm, the measured current flowing in the arm, and the sorted array of cell indices from the capacitor voltage sorting algorithm. If the current flowing in the arm was positive, the module selected the number of cells specified in ascending order. If the current flowing in the arm was negative, the module selected the number of cells specified in descending order. The module then output the necessary signals to switch the associated IGBT selections. Figure 13 is an image of these sorting and selection modules.

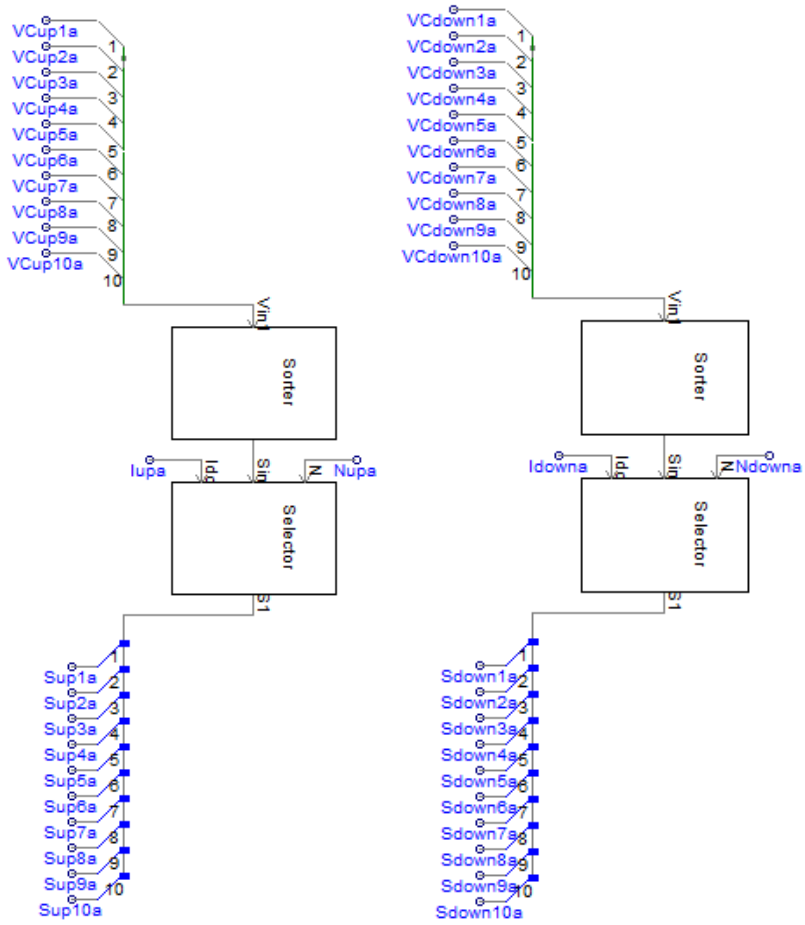

Figure 13: Sorting and Selection Modules for the Upper and Lower Arms of Phase A

2.1.4 Controller Design and Tuning

Next a description of the control structure implemented into PSCAD for each converter is provided. This section covers all control associated topics of the control modeling implementation. These topics include Park's transformation, the current controller, controller performance tuning, determining current controller gains, AC voltage regulation, DC voltage regulation, and power regulation.

Park's Transformation

For each converter station, standard PI controllers were implemented into our PSCAD/EMTDC model to regulate current, the DC output voltage, and the AC regulator. First, the Park's transformation utilized is displayed in (4a) and (4b). Note that *K* is the transformation matrix and variable *f* can be either current or voltage. Figure 14 shows generic Park Transformation blocks to more simply picture what is going on. The line-to-ground voltage measurements and current measurements for the DQ transformation are taken on the primary side (AC side, Y-side) of the transformer interfacing the MMC converter.

$$f_{dq0} = Kf_{abc} \tag{4a}$$

$$K = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{4b}$$

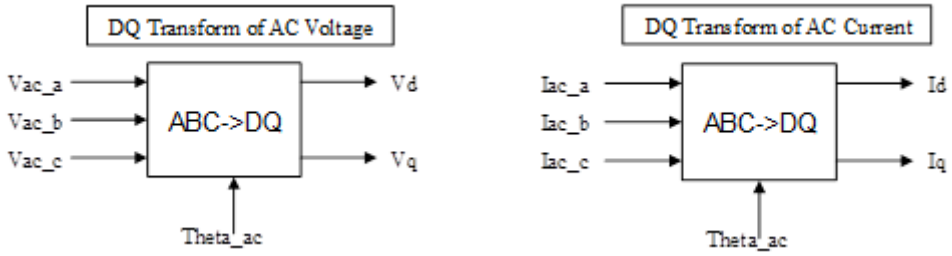

Figure 14: Generic Park Transformation Blocks for Voltage and Current

The Park's transformation implementation into PSCAD performed on both the current and voltage measurements are found in Figure 15 and Figure 16, respectively. Prior to the software performing the Park's transformation computations, logic is used to convert the current and voltage measurements into per unit. In the top left of each figure, one will see three inputs connected by three green bars. This is where per unit values enter into the dedicated area of the file for converting to *d* and *q* quantities.

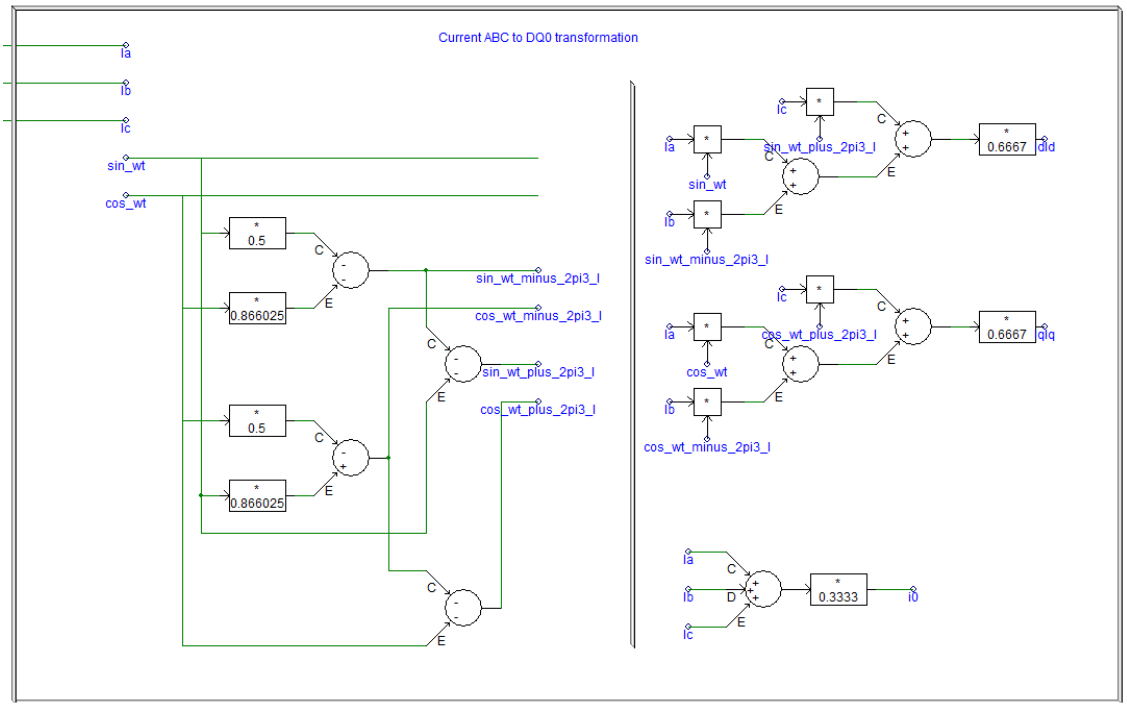

Figure 15: Current ABC to dq0 Transformation Implementation in PSCAD

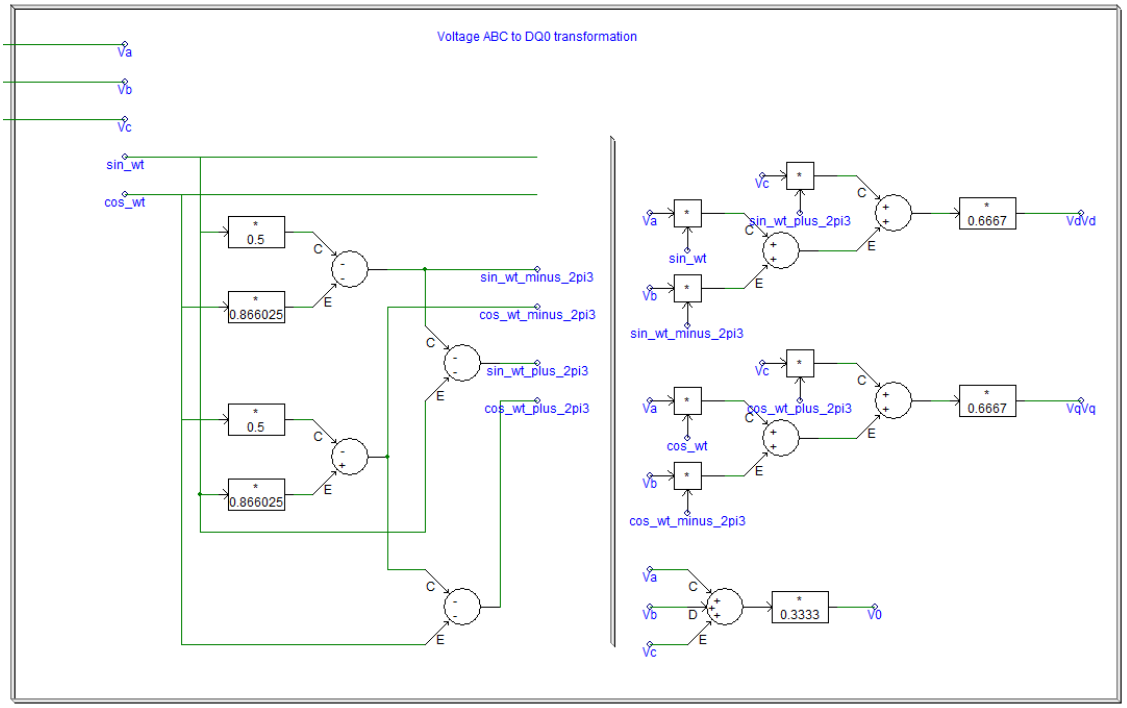

Figure 16: Voltage ABC to dq0 Transformation Implementation in PSCAD

Current Controller

The AC current regulator for each HVDC converter station is found in Figure 17. The section surrounded with a blue outline is the current controller and the section with a green outline sets up the reference signals for the pulse width modulator. The standard relationships, based off of Kirchoff's voltage law, governing the current controller are listed as (5a) and (5b) for the *d*-axis and *q*-axis, respectively [23]. Note that k_P and k_I are the PI controller gains and X_{Tx} is the transformer reactance. $V_{d,meas}$, $V_{q,meas.}$, $I_{d,meas.}$, $I_{q,meas.}$ are the variables computed from Figure 16, the results of Park's transformation. The error amplified by the PI controller that receives the difference between the measured DC voltage value and reference DC voltage value determines the direct axis current reference, $I_{d,ref}$. Similarly, the error amplified by the PI controller that receives the difference between the measured AC voltage value and reference AC voltage value determines the quadrature axis current reference, $I_{q,ref}$. These latter PI controllers corresponding to the DC voltage regulator and AC voltage regulator will be described in upcoming material.

$$V_{\mathrm{d,ref}} = V_{d,meas} + X_{Tx} I_{q,meas} - \left[k_p \left(I_{d,ref} - I_{d,meas} \right) + k_I \int \left(I_{d,ref} - I_{d,meas} \right) dt \right] \quad (5a)$$

$$V_{\mathrm{q,ref}} = V_{q,meas} - X_{Tx} I_{d,meas} - \left[k_p \left(I_{q,ref} - I_{q,meas} \right) + k_I \int \left(I_{q,ref} - I_{q,meas} \right) dt \right] \quad (5b)$$

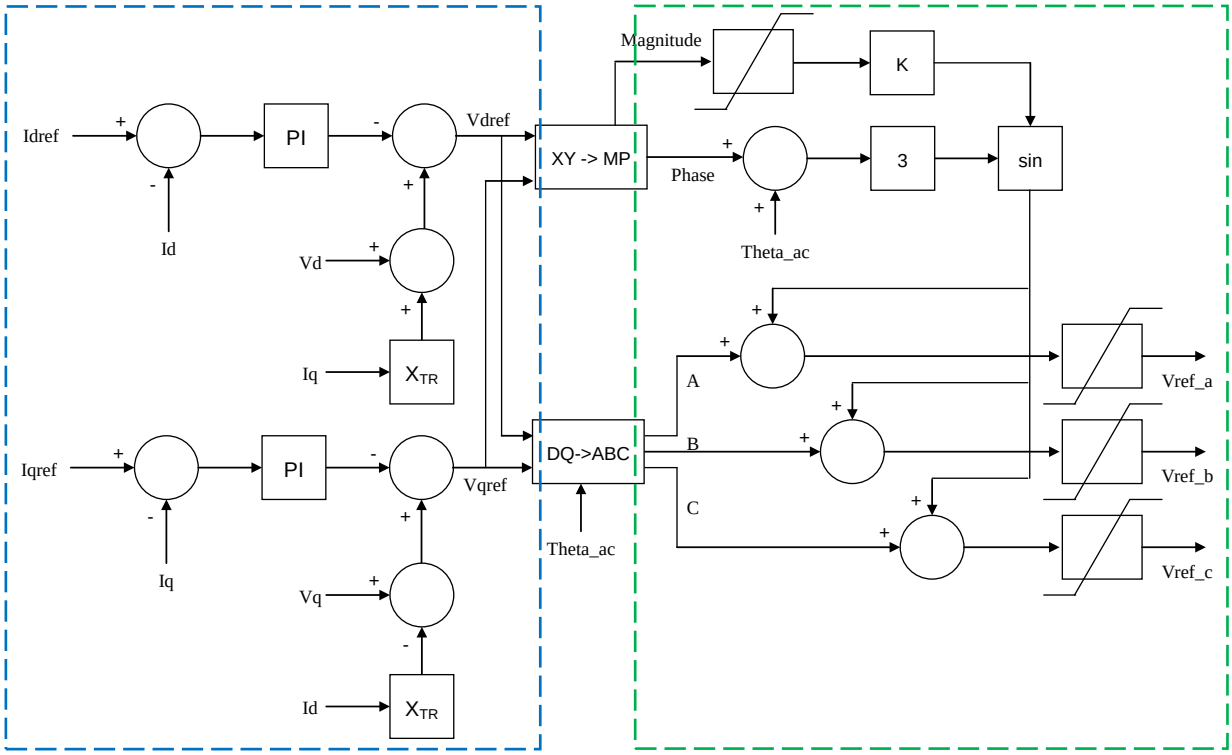

Figure 17: AC Current Regulator Block Diagram

To obtain the desired DC rated voltage of the system, it may be required to increase the fundamental line-to-line voltage by adding a third harmonic component to the three-phase sinusoidal modulating wave without causing overmodulation [22]. This technique is illustrated in Figure 18. Essentially, the peak *fundamental* component can be higher than the peak triangular carrier wave, which boosts the fundamental voltage. At the same time, the *modulated* wave can be kept lower than the carrier signal avoiding problems caused by overmodulation. This technique is referred to as third harmonic injection. The reference signal generated is a combination of the three-phase sinusoidal modulated wave signal generated by the current controller based upon $V_{d,ref}$ and $V_{q,ref}$ and a third harmonic signal. The latter describes the purpose of the section outlined in green of Figure 17. Figure 19 and Figure 20 are the current controller and third harmonic injection implementations in PSCAD, respectively.

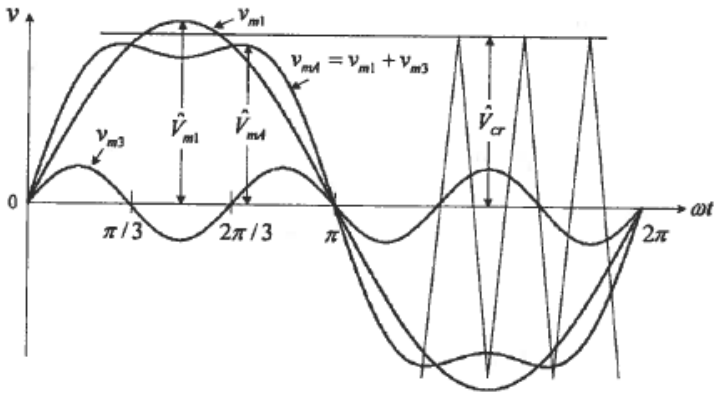

Figure 18: **Illustration of Modulated Case with Third Harmonic Injection** [22]

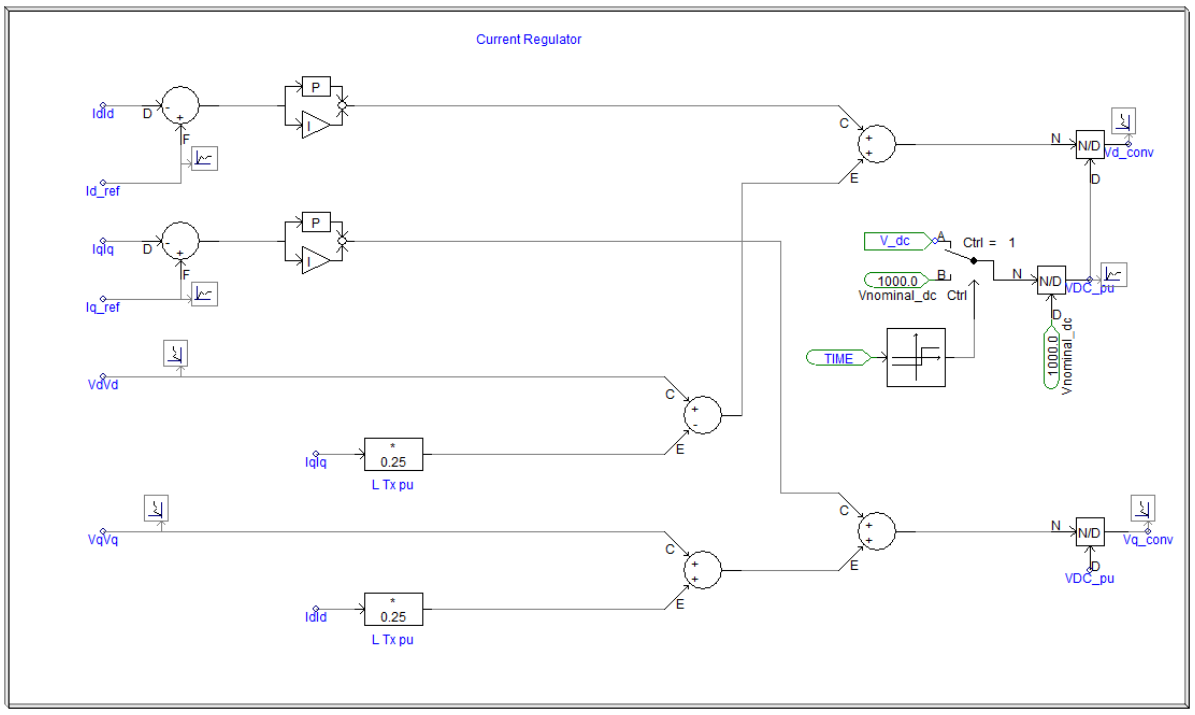

Figure 19: Current Controller Implementation in PSCAD

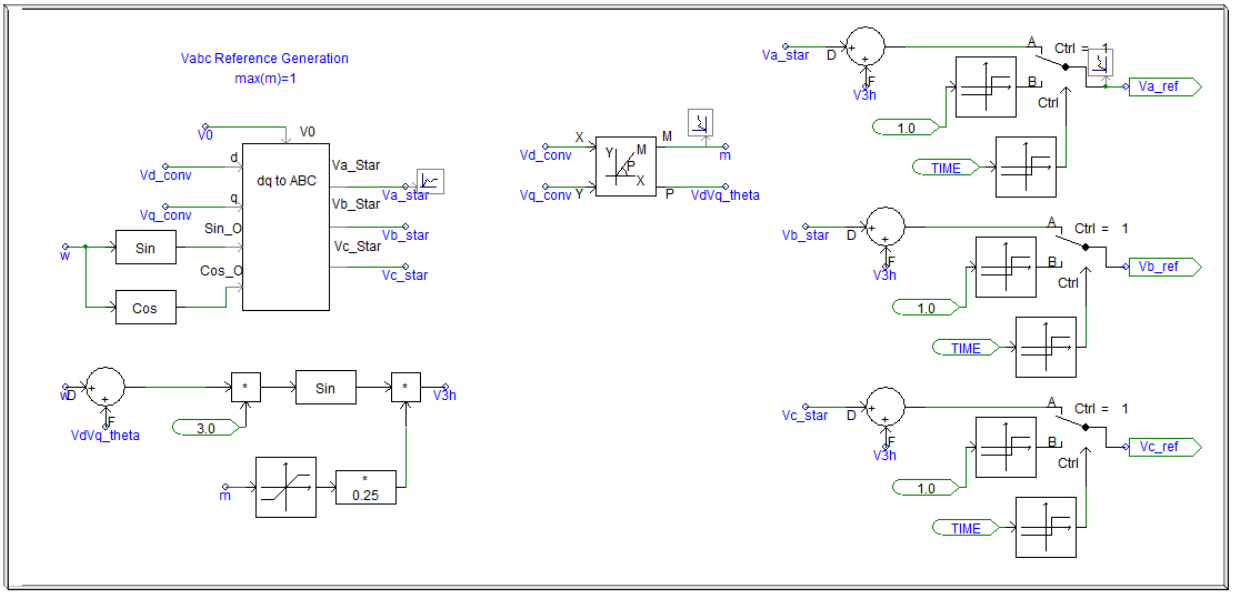

Figure 20: Third Harmonic Injection and Generated Reference Signals in PSCAD

Tuning Controller Performance [23], [24]

A simplified equivalent circuit on the AC side of the back-to-back HVDC system is found in Figure 21. The positive sequence relationships of the MMC, in terms of their synchronous *dq*-frame components can be expressed by (7a) and (7b), respectively [23].

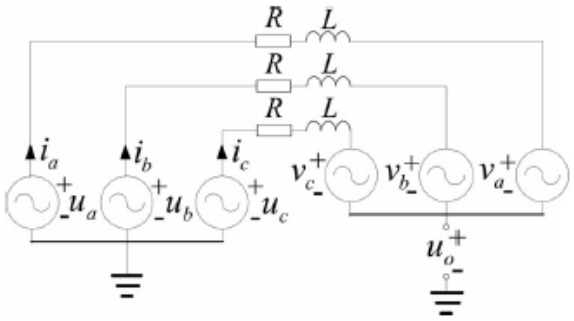

Figure 21: Simplified Equivalent Circuit on AC Side

$$\frac{di_d}{dt} = -\frac{R}{L}i_d + \omega i_q + \frac{1}{L}u_d - \frac{1}{L}V_d \tag{7a}$$

$$\frac{di_q}{dt} = -\frac{R}{L}i_q - \omega i_d + \frac{1}{L}u_q - \frac{1}{L}V_q \tag{7b}$$

Substituting (5a) into (7a), one will arrive at (8). Equation (8) represents a first order system with open-loop transfer function described by (9).

$$L\frac{di_d}{dt} + Ri_d = \left[k_p\left(I_{d,ref} - I_{d,meas}\right) + k_I\int\left(I_{d,ref} - I_{d,meas}\right)dt\right] \tag{8}$$

$$l(s) = \frac{k_p + k_i/s}{Ls + R} \tag{9}$$

If the two gains are selected by (10), the open-loop and closed-loop transfer function simplify to (11) and (12), respectively.

$$k_p = \frac{L}{\tau} \quad k_I = \frac{R}{\tau} \tag{10}$$

$$l(s) = \frac{1}{\tau s} \tag{11}$$

$$G(s) = \frac{1}{\tau s + 1} \tag{12}$$

Determining Current Controller Gains

Utilizing a value of 1 millisecond for τ and per unit values for L and R, the following gains were determined:

$$L = \frac{X_{Tx}}{\omega} = \frac{0.25\,p.u.}{377} = 0.000663$$

$$\frac{X_{Tx}}{R_{Tx}} = 100 \rightarrow R = \frac{0.25\,p.u.}{100} = 0.0025\,p.u.$$

$$k_p = \frac{L}{\tau} = \frac{0.000663\,p.u.}{1ms} = 0.663 \quad k_I = \frac{R}{\tau} = \frac{0.0025\,p.u.}{1ms} = 2.5 \xrightarrow{inverted} 0.4s$$

The per unit values utilized for L and R were the per unit values previously specified for the transformer inductance and resistance. Arm inductance and arm resistance were neglected in these gain parameter calculations since the transformer impedance is dominant.

AC Voltage Regulator, DC Voltage Regulator, and Power Regulator

The last components associated with the controllers in the model include the AC voltage regulator, the DC voltage regulator, and the power regulator. The AC regulator utilized in the PSCAD implementation is provided in Figure 22. The tag labeled *Va_in* is a voltage measurement from the system not in per unit. Note that √(3/2) is equivalent to 1.225. There is also switch logic that sets the voltage reference at certain points in the simulation. The first reference point, B, is set until the capacitors in the MMC are initialized. As stated earlier in this report, this loop sets the quadrature axis current reference for the current controller.

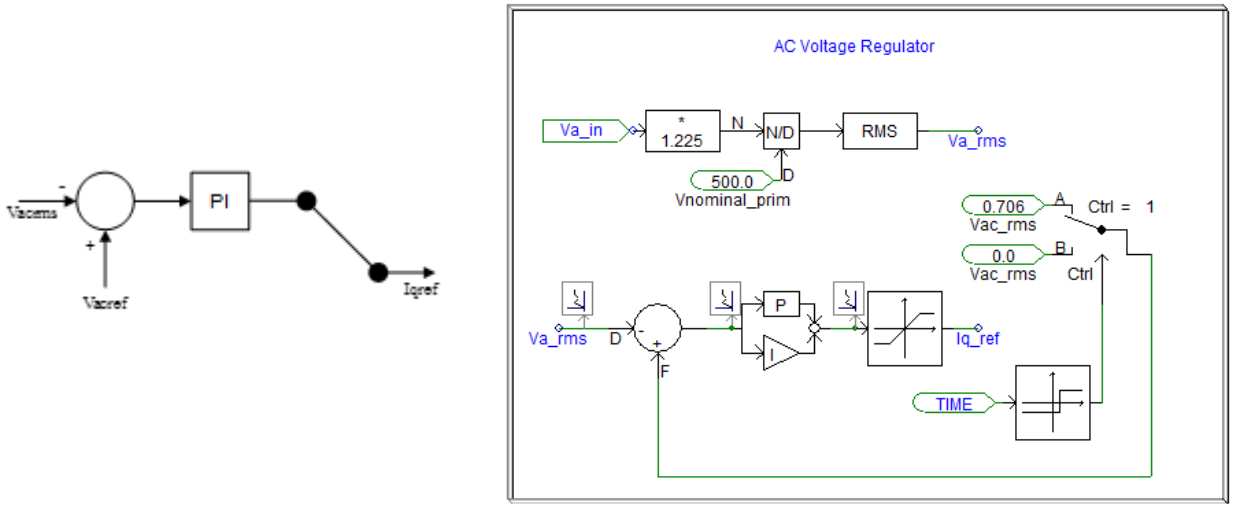

Figure 22: AC Voltage Regulator and PSCAD Implementation

The DC regulator utilized and the PSCAD implementation is provided in Figure 23. As stated earlier in this report, this loop sets the direct axis current reference for the current controller. The PI controller was tuned iteratively corresponding to the response time of the system and the capacitance of each arm. This resulted in $k_p = 10$ and $k_I = 200$.

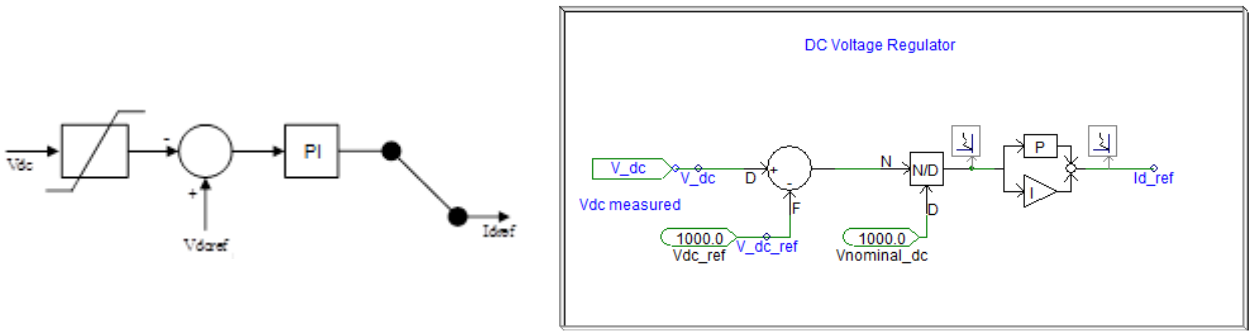

Figure 23: DC Voltage Regulator Diagram and PSCAD Implementation

In the monopolar HVDC system, one converter acts as the sending end (A) and the other as the receiving end (B) at any given time. The converter controlled by the DC voltage regulator can be seen as the sending end. The receiving end must then be controlled by a real power regulator, ensuring proper power transfer through the system. The real power regulator can be seen in Figure 24. Switch logic is used here to require full power flow only after steady state voltage is achieved in simulation, initially set to *B* and switched to *A* at 3 seconds of run time.

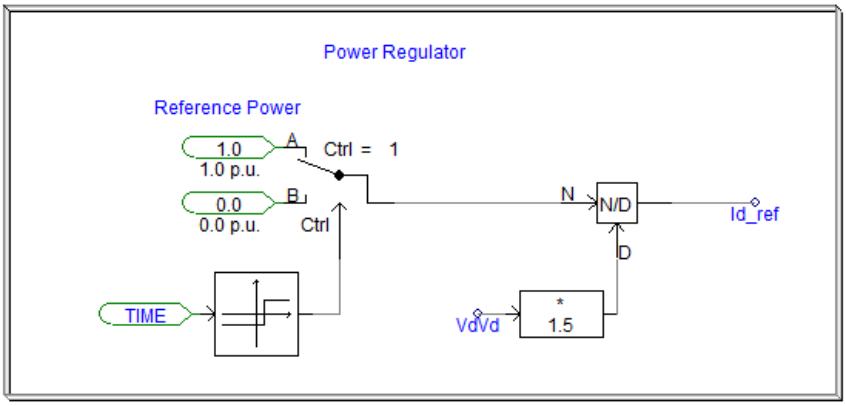

Figure 24: Real Power Regulator

DC voltage regulator is implemented in terminal *A* converter control while the power regulator is implemented in terminal *B* converter control. Each of these controllers function to set the direct axis current reference for the controller.

2.2 HVDC SYSTEM MODEL VALIDATION

The purpose of this section is to validate the PSCAD HVDC system model by showing simulation results and assessing that they are as expected. Figure 25 shows a top level view of the entire monopolar HVDC system model in the PSCAD environment. Note that all measurement points used for plotting results are shown in this figure.

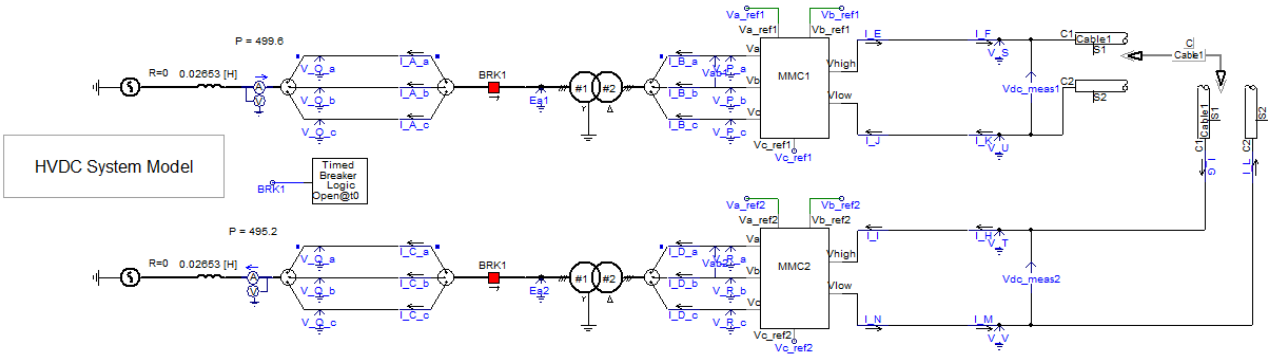

Figure 25: Top Level View of PSCAD HVDC System Model

First, the validation simulation process is here described for the purpose of having a lens through which to view and analyze the validation results. At the start of the validation simulation, the system voltage is first initialized and shown to reach steady state. This was achieved by allowing 0.1 seconds to pass before beginning converter operation. During that time, a DC voltage source of 100 kV is applied to each converter submodule capacitance to initially charge these capacitors. These DC sources are disconnected from each submodule capacitance after 0.1 seconds has passed, and the converter is simultaneously connected to the system. At this point system power flow is not yet required. In converter *B* control, the power reference is initially set at 0.0 p.u. to ensure achieving steady state voltage before requiring power flow. Note that at the start of converter operation (post capacitance charging), a large transient occurs in PSCAD results due to converter connection with the system. For one example of this transient, reference Figure 26, the plot of demanded and actual DC voltage at the terminal *A* MMC. This transient should be viewed as a computational occurrence, not as a true circuit phenomenon. This transient can be seen to reach steady state in the converter approximately at or before 1 seconds of run time. With ample time after steady state operation has been achieved, power flow is then demanded of the system at 2 seconds time. This power flow demand is achieved in simulation by

changing the power regulator control reference from 0.0 p.u. to 1.0 p.u. Next, in order to demonstrate proper response from the system due to demand changes, the DC voltage is stepped from 1000 kV to 1050 kV at 3 seconds, achieved by changing the voltage regulator reference from 1000 kV to 1050 kV. Proper functionality of voltage regulation is thus demonstrated. By use of this validation simulation process, the goal of this section is achieved by demonstrating both system and control level functionality at steady state and after the step input.

The DC voltage over the course of simulation can be seen in Figure 26. It is clear that after the initial transient, the DC voltage settles near the demanded 1000 kV value. No more than 10% fluctuation in the voltage is permissible. In steady state, the overshoot can be calculated as:

$$Overshoot = \frac{V_{actual} - V_{demanded}}{V_{demanded}} \cdot 100\% = \frac{1006kV - 1000kV}{1000kV} \cdot 100\% = 0.6\%$$

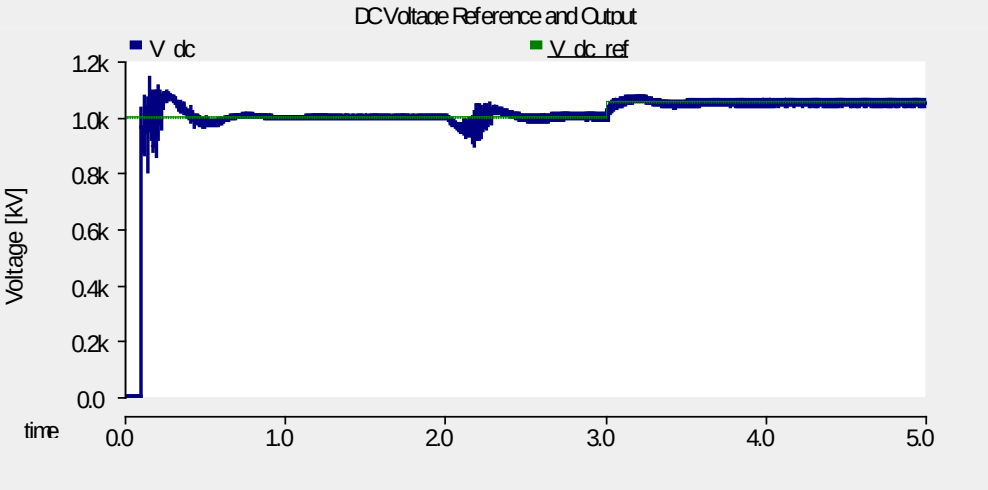

Figure 26: Demanded and Actual DC Voltage on MMC A

As shown in Figure 23, the step change in the DC voltage drives a corresponding change in the reference point for the direct axis current, I_{d_ref}, via the outer PI control loop. The inner

loop control for the *d*-axis current then responds accordingly as demonstrated in Figure 27. Both the power demand input to the system at 2 seconds as well as the voltage step input at 3 seconds can be clearly seen, both with a rapid response from the controller. While there is noise on this signal and many others within the system, it is negligible and preferable to filtering to maintain a faster response.

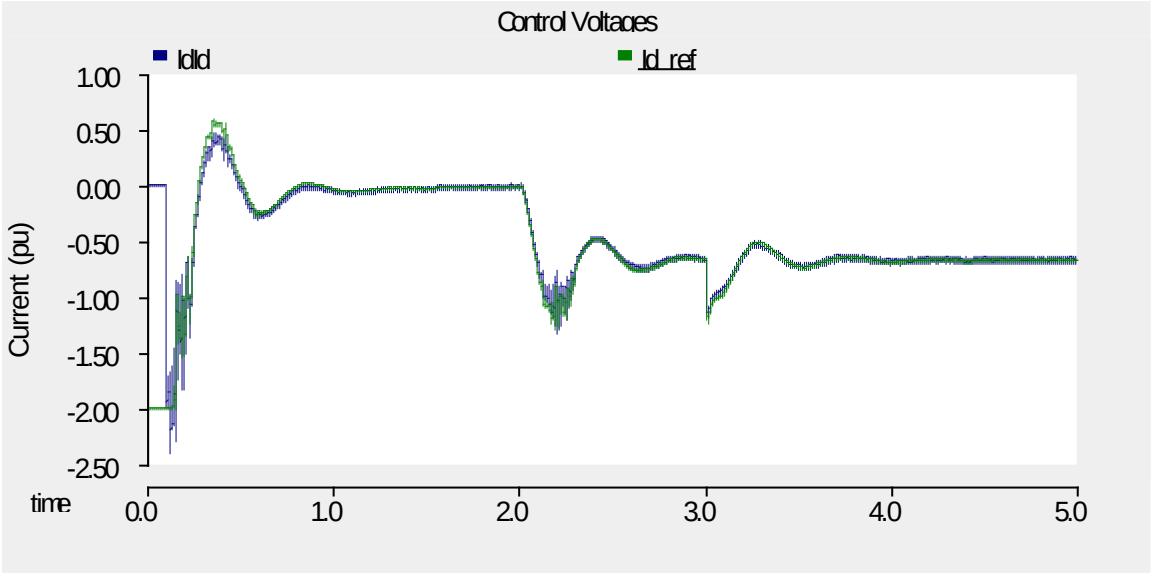

Figure 27: *d*-Axis Current Controller Response

Figure 28 gives the current controller response for the *q*-axis controller. This control signal is also driving towards the reference established by the AC current regulator. The *q*-axis current is satisfactorily regulating to the reference.

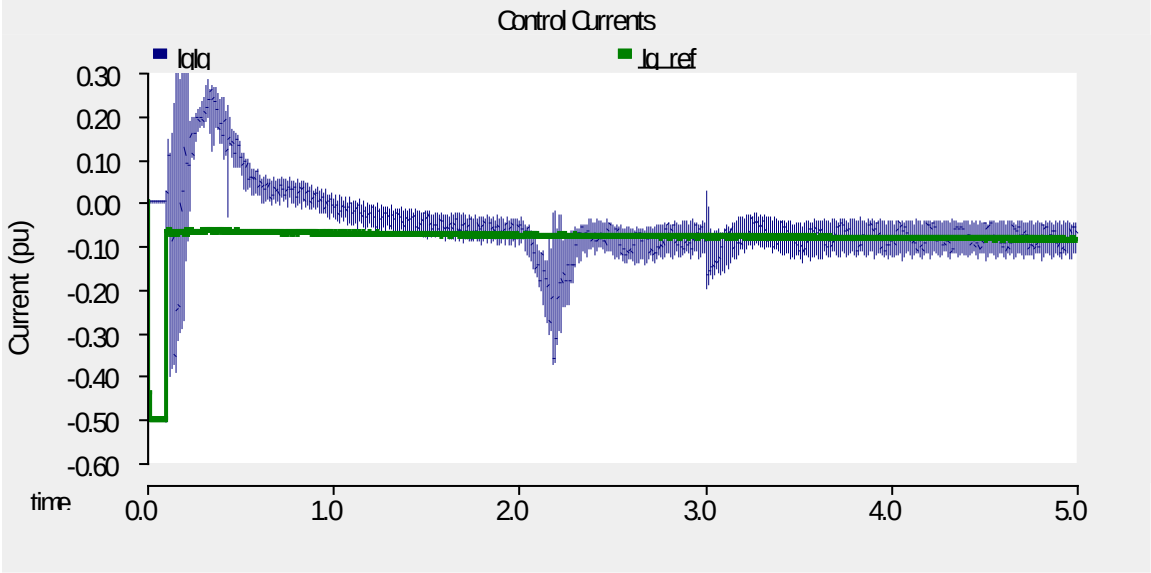

Figure 28: *q*-Axis Current Controller Response

The signals that establish the reference signal for the pulse width modulator, referred to as the reference *d* and *q*-axis voltage control responses, are shown in Figure 29.

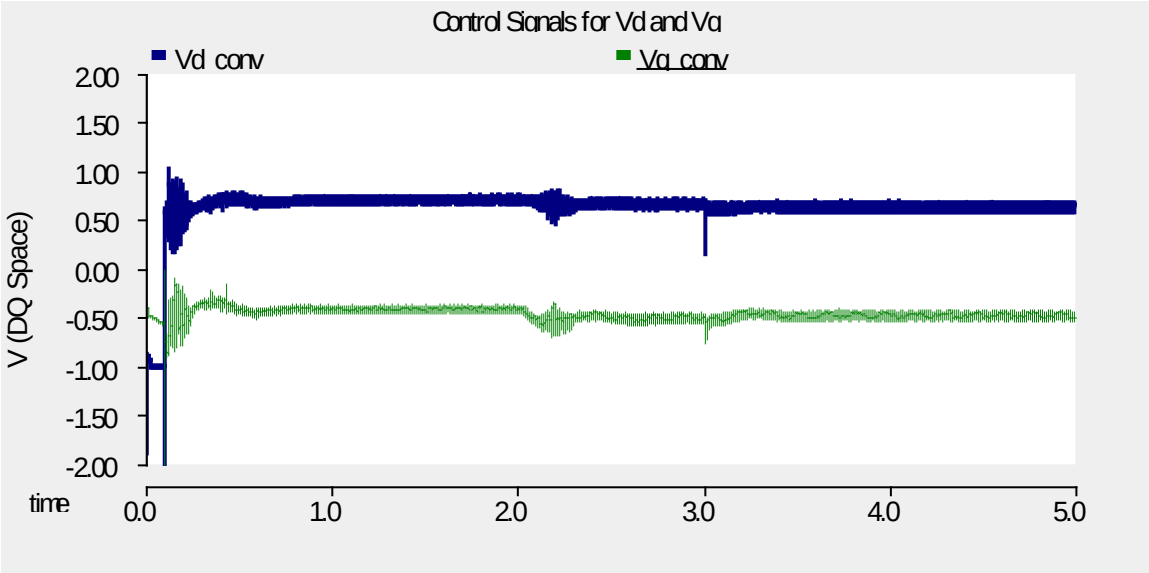

Figure 29: *d* and *q*-Axis Voltages Establishing Reference Voltage for PWM Modulator

The modulation index (*m*) is displayed in Figure 30. Note that the modulation index operates within the linear range if its value falls between 0 and 1. Also, *m* is a function of the reference *d* and *q*-axis voltage signals shown in Figure 29. The correlation between these signals and the modulation index is clear upon observation. The 2 second and 3 second simulation events are clearly observed in each of these signals, responding in the same way. Once the system reaches steady state with power flow at approximately 2.5 seconds, the modulation index reaches an average value of 0.83 as expected. The modulation index is observed to decrease when the voltage is stepped from 1000 kV to 1050 kV at 3 seconds. This is as expected, because the system is rated for 1000 kV. Running the system at 1050 kV, higher than system ratings, will cause operation to fall farther from ideal rated operation (*m*=1.0).

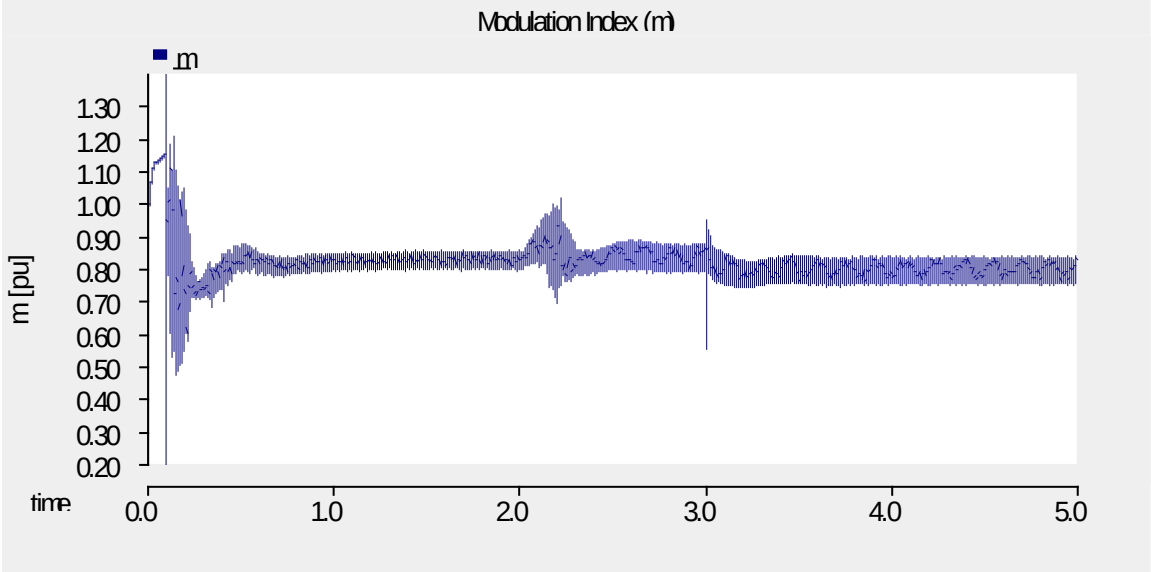

Figure 30: Modulation Index

The *d* and *q*-axis control voltages, along with *m*, are then used to form the reference AC voltage waveform with third harmonic injection. This control signal is the output of the

controller that drives the comparators in the converter itself, and is displayed in Figure 31. This figure displays the AC control signal reference waveform during steady state with power flow. This signal is compared with the carrier waveforms to determine the number of submodules to switch, as previously shown in Figure 11.

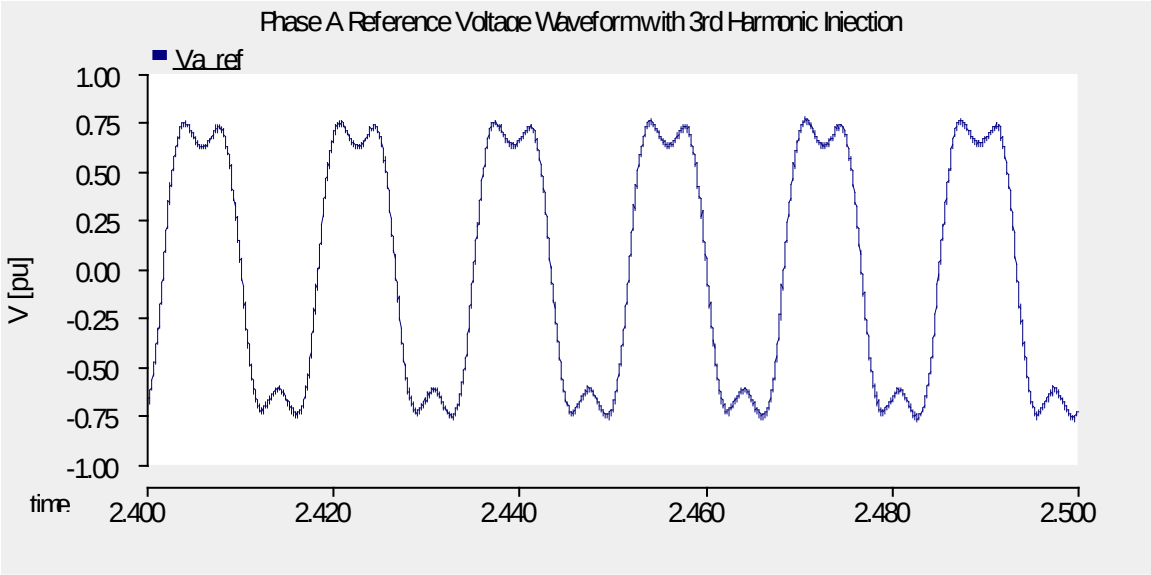

Figure 31: Third Harmonic Injected AC Control Signal Waveform

The sequenced switching of submodules according to the control reference waveform above yields fluctuating voltages on the capacitors in the converter. According to desired specifications, the ΔV (ripple voltage) of the capacitors was limited to no more than a steady state ± 10% ΔV. The capacitor voltage for the full duration of simulation is shown in Figure 32 and the steady state operation is shown in Figure 33.

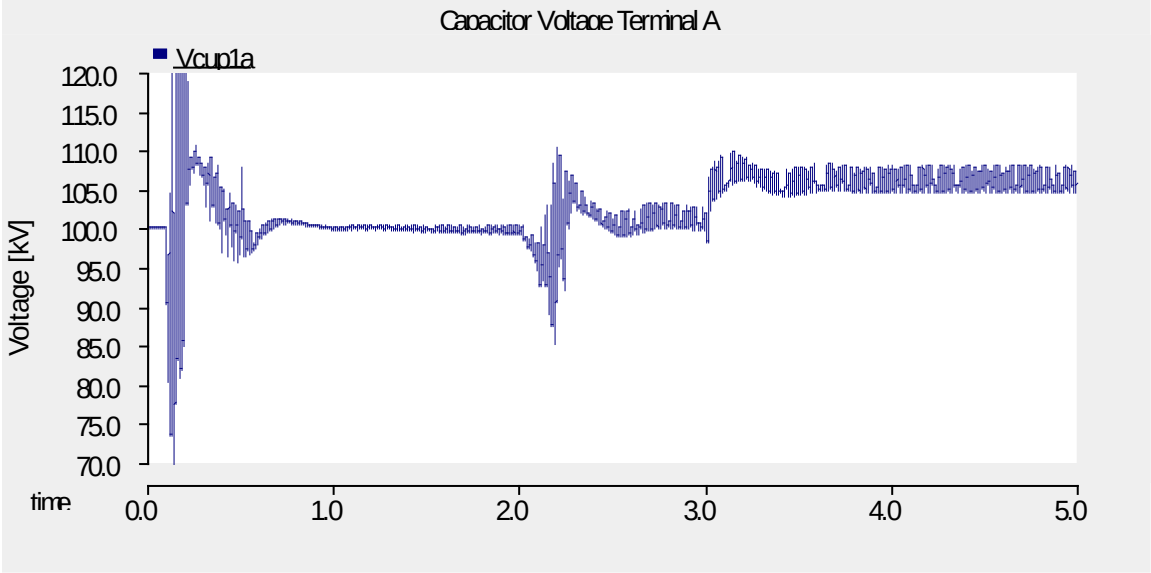

Figure 32: Capacitor Voltage for Full Duration

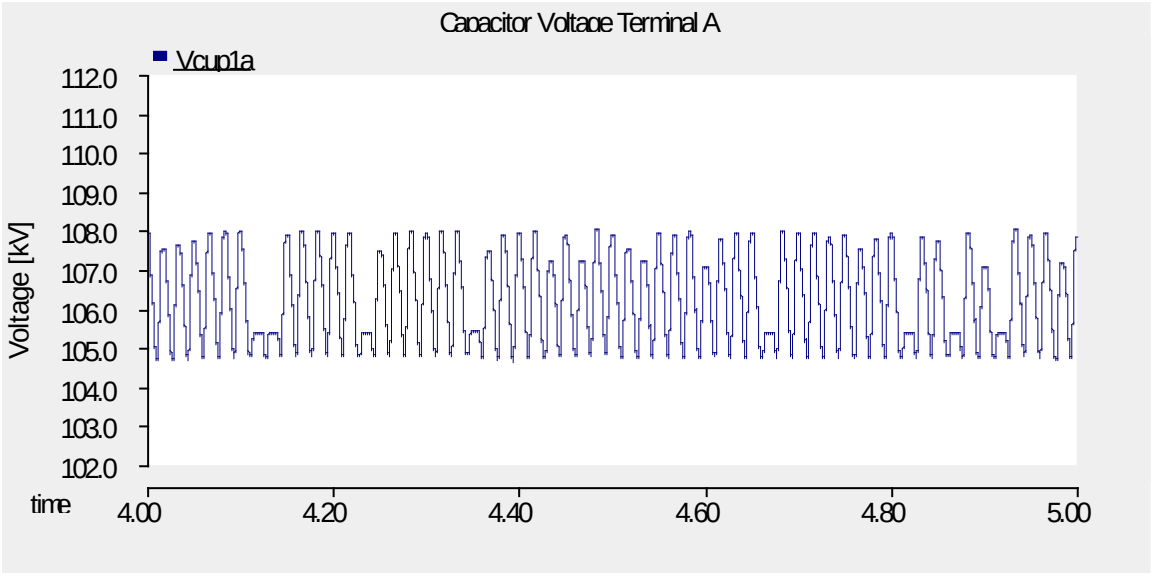

Figure 33: Steady State Capacitor Voltage

The calculation of the voltage fluctuation is shown below. It is found to be 3.15%, which is well below the 10% specified limit.

$$\Delta V_{cap} = \frac{V_{\max} - V_{avg}}{V_{avg}} = \frac{108kV - 104.7kV}{104.7kV}(100) = 3.15\%$$

By switching the capacitors according to the control output reference waveform of Figure 31 and the capacitor balancing algorithm previously presented, the line-to-neutral AC voltage waveform shown in Figure 34 is the AC output of the converter, with a peak of 408 kV. The line-to-line AC voltage is expected to be 500 kV (line-to-line RMS), as seen in Figure 35. The following calculation validates the simulation finding:

$$V_{LL}^{RMS} = \frac{\sqrt{3}}{\sqrt{2}} V_{LN}^{peak} \longrightarrow 500kV = \frac{\sqrt{3}}{\sqrt{2}} 408kV$$

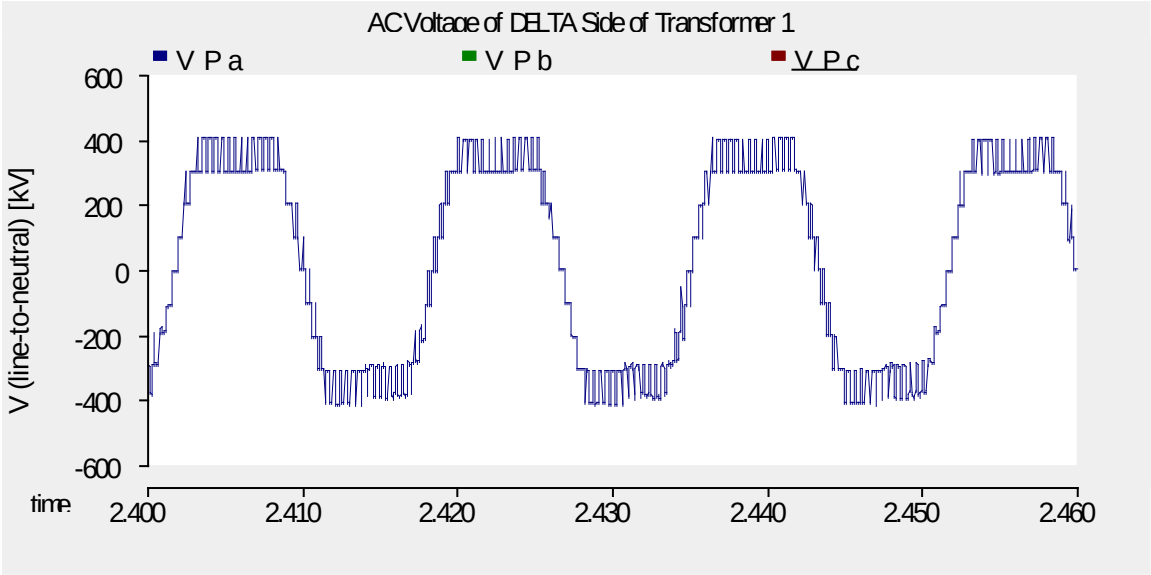

Figure 34: Line-to-Neutral AC Voltage Created by the Converter

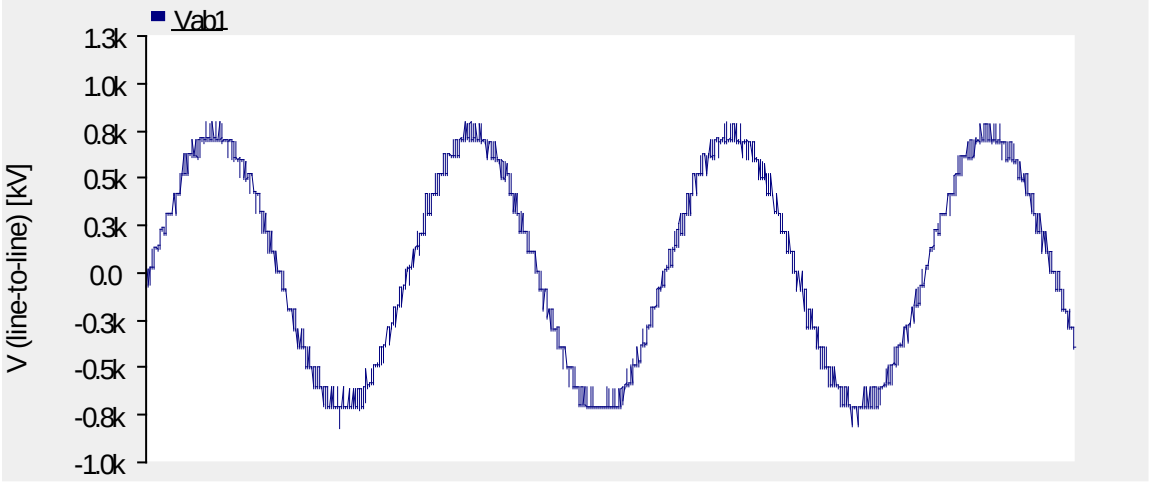

Figure 35: Line-to-Line AC Voltage Created by the Converter

This waveform is a strong illustration that shows that the HVDC system model is functioning satisfactorily – all circuitry, capacitor balancing algorithm, and system controls. A clearer comparison of this waveform with the control signal that governs it, as well as the line-to-neutral voltage on the grid side of the transformer is presented in Figure 36. Note that the slight phase shift between the AC voltages on the converter side and the grid side is expected due to the Y-Δ transformer (30 degree phase shift). Additionally, it is important to note the effect of the transformer inductance in terms of filtering most of the harmonics generated by the converter.

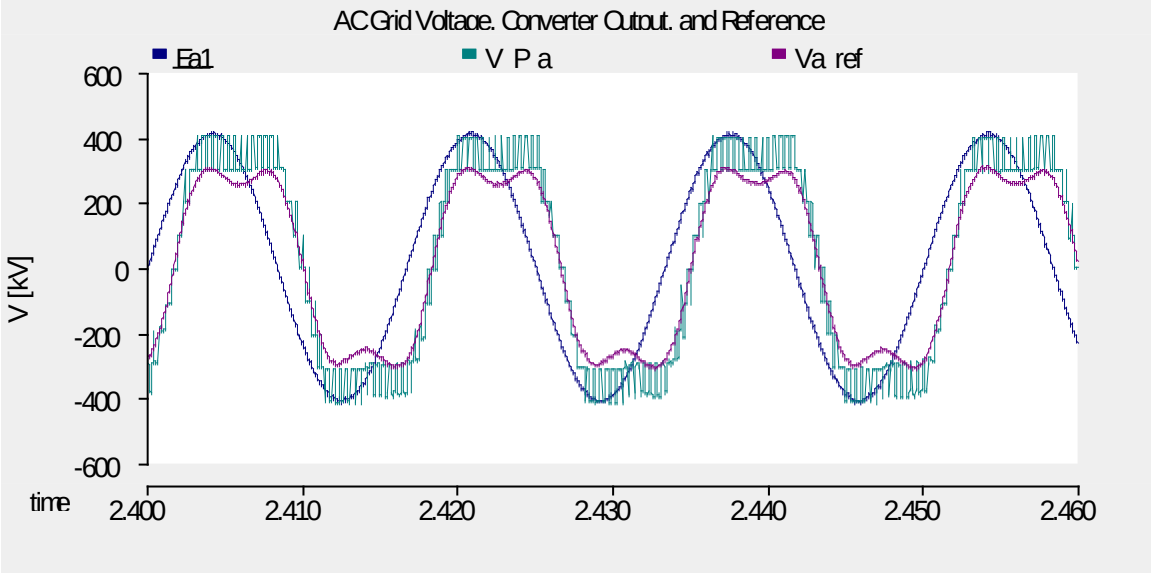

Figure 36: Grid Side Voltage, Converter Side Voltage, and Reference Waveform

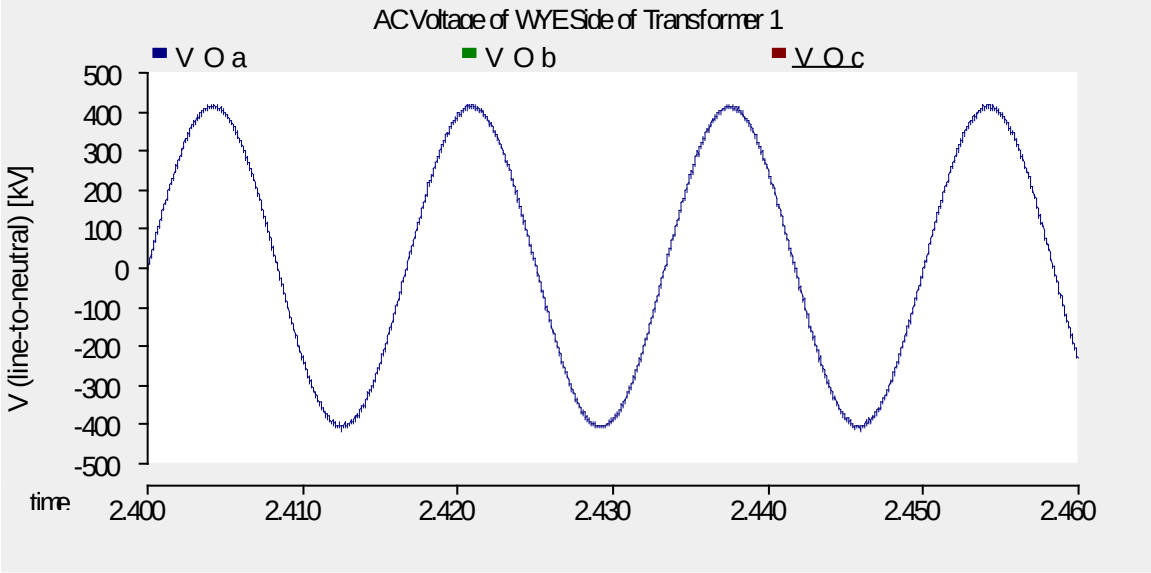

Figure 37: Grid Side of Transformer Line-to-Neutral AC Voltage

The grid side AC voltage can be seen isolated in Figure 37, and as is clearly apparent, is very smooth and free of harmonics. According to IEEE 519, to which a transmission converter must adhere, the total harmonic distortion (THD) at the point of interconnection can be no more

than 1.5% [25]. Analyzing the grid side AC voltage waveform, once the system reached steady state with power flow, it was found that the THD for this converter is less than 0.01%. This analysis was performed using the fast Fourier transform and THD calculation components in PSCAD, and verifies that the converter model designed meets the IEEE 519 specified criteria. Thus, 10 cells per arm is adequate for model simplification of the modular multilevel converter.

The final portion of this validation analysis presents the power flow characteristics of the converter. The DC power demand was required to be 1000 MW at 2 seconds, after a steady state voltage was achieved at approximately 1 second according to Figure 26. Steady state power flow is achieved at approximately 2.5 seconds according to Figure 38. Upon the event of stepping the voltage regulator reference at 3 seconds, steady state power flow is regained approximately half a second later. As discussed previously, the DC power flow was controlled by a power regulator at the receiving end converter. The resulting DC power flow can be seen in Figure 38.

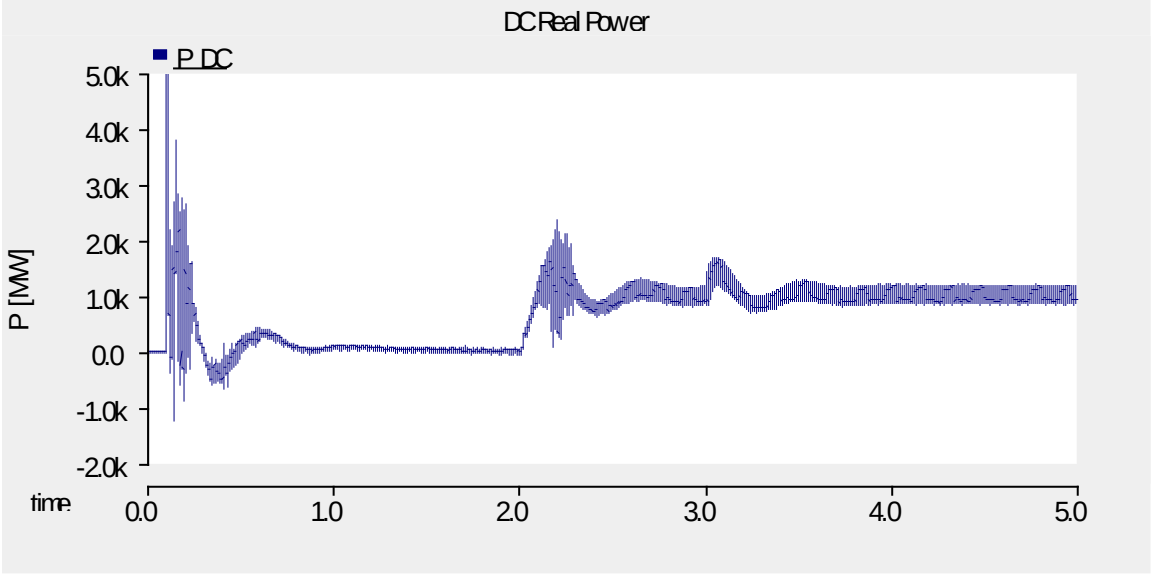

Figure 38: DC Power Transfer

2.3 CONCLUSION

Throughout this chapter, emphasis is placed upon the modeling the monopolar HVDC system within the PSCAD simulation environment. The converter station topology is based upon the modular multilevel converter (MMC) arrangement. Additionally, all system parameters utilized within the PSCAD validation model are provided.

Various details of the computer modeling are documented including a thorough circuit synthesis of the MMC converter topology, MMC capacitor initialization and balancing procedures, controller implementation (DC voltage, AC voltage, power and current regulators) and the method for tuning the controllers. With the theoretical platform established, PSCAD simulation results are presented in order to show that the system is performing as expected.

After the validation presented in this chapter there are further refinements made to the model for the DC fault analysis in the next chapter. These modifications include an addition of a frequency dependent overhead line model placed in series with the cable model already implemented in the model, as well as the various model adjustments associated per differing fault case. The next chapter presents the performance of a DC fault analysis for the purpose of evaluating system trends based off of varied component ratings.

3.0 PARAMETER TRENDS RESULTING FROM SENSITIVITY ANALYSIS

With a validated MMC-HVDC model, the next step was to probe the system with fault case scenarios for the purpose of observing the impact that the various system parameters have on the peak line current during a fault. This parameter impact analysis has a high amount of value for the purpose of determining what parameter values are implemented for the ultimate system protection analysis. Yes, we have a validated model, but the parameters selected for the initial model validation might not be parameters desired for analysis of the HVDC system protection. Not until each parameter has been purposefully chosen for the model can we proceed to probe the system with various fault types and locations for the purpose of determining protection needs. From the trends analysis presented in this section each parameter value will be chosen based upon its impact upon the DC line fault current. As discussed in the background of this work, these line currents are what the ultimate protection design is protecting against.

Each parameter will be chosen according to either the highest peak current or the lowest peak current, depending upon the nature of the parameter. For example, the HVDC line configuration will be chosen for protection analysis based upon the highest peak current observed, because for this parameter we want to evaluate the worst case scenario that would be seen in installation. But for the DC line reactance (DCL) sensitivity analysis, the lowest peak current observed will dictate which DCL is chosen for protection analysis, because the selection depends upon which value performs the DCL function best – DC line current suppression. Note

that all simulated faults for this section, both L-G and L-L, are located at the sending end of the DC line, at the junction of the terminal *A* converter station and the DC cable. This fault location is the worst case scenario in terms of protecting converter *A* devices from fault current. The only trend that includes fault locations at the midpoint and receiving end of the DC line in addition to the sending end location is the HVDC line configuration trend. A sensitivity analysis was performed for each primary system parameter. Table 2 shows each of the parameters for which a sensitivity analysis was performed and provides the range of parameter sensitivity that was analyzed.

Table 2: Parameters Simulated with Associated Sensitivity Ranges for Trends Analysis

Parameter:	Sensitivity Range:
DCL Impedance	0, 10, 50, 100 *mH*
Transformer Reactance	10, 15, 25, 30 %
Asymmetric Arm Reactor Impedance	5, 10, 15, 30 %
Symmetric Arm Reactor Impedance	5, 10, 15 %
BPS Operation Speed	5, 6, 7, 8, 9, 11, 12, 15 *ms*
AC Short-Circuit Capacity	9.5, 25, 55 *GVA*
DC Line Length	800, 1000, 1200 *km*
DC Line Configuration	OH line (sending) Cable (receiving), Cable (sending) OH line (receiving)

Each of these sensitivity ranges were simulated for both line-to-line and line-to-ground faults, almost exclusively located at the sending end of the DC line. The validation model parameters from the HVDC MMC system modeling section were used for the base cases, Cases 1-1-1 and 1-1-2, for this trends analysis as shown in Table 3.

Table 3: Validation Model Parameters, Used as the Base Cases of Trends Analysis

	DCL	Transformer reactance	Arm inductance	BPS speed	AC short circuit capacity	DC length	Fault case
	(mH)	(%)	(%)	(ms)	(GVA)	(km)	
Case1-1-1	0	25	10.0	10	25	1,000	L-L
Case1-1-2	0	25	10.0	NA	25	1,000	L-G

With each primary parameter being varied per case run, the peak DC fault current was observed and recorded (at terminal of converter *A*). Each parameter value was selected based upon what caused the desired outcome of peak DC fault current for the HVDC protection analysis. This HVDC protection analysis is presented in chapter four.

3.1 TREND OF DC LINE REACTANCE

Table 4 lists the cases associated with a sensitivity analysis of the DC line reactance (DCL).

Table 4: Case List Showing Variance of DC Line Reactance

	DCL	Transformer reactance	Arm inductance	BPS speed	AC short circuit capacity	DC length	Fault case
	(mH)	(%)	(%)	(ms)	(GVA)	(km)	
Case1-1-1	0	25	10.0	10	25	1,000	L-L
Case1-1-2	0	25	10.0	NA	25	1,000	L-G
Case1-2-1	**10**	25	10.0	10	25	1,000	L-L
Case1-2-2	**10**	25	10.0	NA	25	1,000	L-G
Case1-2-3	50	25	10.0	10	25	1,000	L-L
Case1-2-4	50	25	10.0	NA	25	1,000	L-G
Case1-2-5	100	25	10.0	10	25	1,000	L-L
Case1-2-6	100	25	10.0	NA	25	1,000	L-G

The DC line reactors are located in the converter stations at the sending and receiving end of both the positive and negative terminal DC lines. This location is displayed in Figure 3, the one line diagram of the HVDC system provided earlier in this document.

The system function of the DCL twofold: 1) limiting the DC line fault current for protection and 2) smoothing out harmonics and noise for a clean converter output signal. With this functional purpose, the lower the peak DC line fault current the better the DCL is performing its function. This reasoning plays into the selection of the DCL for the system protection analysis. For an HVDC installation, the DCL will be selected partially based upon this same criteria, component performance. The selection will also depend upon unimpeded power flow. We expect that the higher the DCL value, the lower the peak DC currents will be, but we cannot simply select an extremely high impedance due to increased power loss. Considering these factors a DCL parameter will be appropriately selected for the HVDC protection analysis.

Figure 39 shows the impacts of a varied DC line reactance on the peak DC current of the system. One apparent observation is that L-L faults cause much higher currents. This is expected according to the nature of L-L faults. When comparing DCL values for L-L fault currents, the significance drawn from the results is that the higher the DCL impedance, the lower the DC line current. This is expected based upon the function of the DCL aforementioned. When comparing DCL values for L-G fault currents, there is not much significance to be drawn from the results. Accordingly the DCL selection is essentially determined upon the L-L fault currents measured.

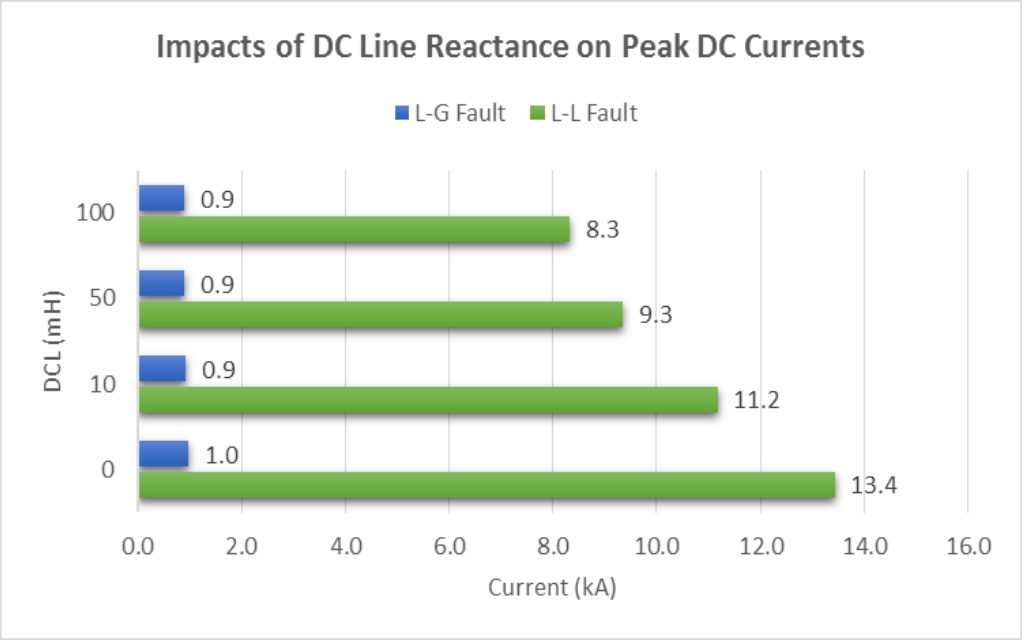

Figure 39: Impacts of DC Line Reactance on Peak DC Currents

The other factor that plays into selecting the DCL value is how much the power flow is impeded. Ultimately unimpeded power flow is desired, but for the sake of protecting components from fault currents a DCL is still necessary. Therefore a tradeoff between unimpeded power flow and suppression of fault current was used to select 10 mH (with 0.02 Ω) for the DCL parameter for the HVDC protection analysis.

When speaking of protecting components against fault currents, the high voltage IGBT modules connected in series in each arm of the converter are of highest concern. In the MMC converter design, each of the three phases will each see a current that is one third of the total peak DC line current. For the 10 mH case in Figure 39, the 11.2 kA of current will be divided into 3.733 kA per arm. Each IGBT will see 3.733 kA for this case. The Mitsubishi CM1200HG-90R is an example IGBT applicable to the HVDC system ratings of this work. According to the data sheet of this device [26], the IGBT has a maximum current rating of 2400 A during a

transient event (Note: it is advisable that any device only ever experiences 75% of its maximum rating). Bypass switches are placed in parallel to each submodule in the MMC design for the protection of each of these IGBTs. The role of the bypass switch in the MMC is discussed in more detail during chapter 2: MMC HVDC system modeling. The bypass switches utilized for high voltage cases are generally press pack thyristors, which are capable of high current/high power applications. One example of such a thyristor switch is the Mitsubishi FT1500AU-240 [27] which is capable of handling 34 kA for a transient peak current over a half cycle's time (1500 A average on-state current). It is desirable that the peak DC fault current is maintained below 15 *kA* for our given application. This is the value that we will compare against when observing the peak DC fault currents within this trend analysis section. This 15 kA keeps the peak fault current below 50% of the maximum peak current handling capability of the applicable example thyristors for the bypass switch (34 *kA*), and this allows for peak currents to exist for longer than a half cycle and still be safely protected against. This large margin is set for extreme conservative protection necessary due to the severe magnitude of HVDC fault scenarios. With this conservative fault current handling capability of a press pack thyristors for a bypass switch, the peak DC fault currents observed in Figure 39 (13.4 kA worst case) are not of great enough of concern to require a larger DCL than the 10 mH selected (11.2 kA peak current). The 10 mH DCL selection is still necessary to include in the system design for smoothing of the converter output signals as well as providing some amount of fault current suppression. These results also show that the DCL reactance is not the dominant reactance on the system.

3.2 TREND OF TRANSFORMER REACTANCE

Table 5 lists the cases associated with a sensitivity analysis of the transformer reactance.

Table 5: Case List Showing Variance of Transformer Reactance

	DCL	Transformer reactance	Arm inductance	BPS speed	AC short circuit capacity	DC length	Fault case
	(mH)	(%)	(%)	(ms)	(GVA)	(km)	
Case1-3-1	0	10	10.0	10	25	1,000	L-L
Case1-3-2	0	10	10.0	NA	25	1,000	L-G
Case1-3-3	0	15	10.0	10	25	1,000	L-L
Case1-3-4	0	15	10.0	NA	25	1,000	L-G
Case1-1-1	0	**25**	10.0	10	25	1,000	L-L
Case1-1-2	0	**25**	10.0	NA	25	1,000	L-G
Case1-3-5	0	30	10.0	10	25	1,000	L-L
Case1-3-6	0	30	10.0	NA	25	1,000	L-G

The transformers on the system are located at grid side of the converter stations both at the sending and receiving ends (terminal *A* and terminal *B*). These locations are clearly displayed in Figure 3, the one line diagram of the entire HVDC system provided earlier in this document.

The selection of the transformer reactance for a protection analysis simulation ultimately depends upon realistic values for actual installations of transformers rated for 500 *kV* high voltage. The analysis of the impacts of transformer reactance variance on peak DC line current is valuable to note the magnitude of impact that a variance of transformer reactance can have on system performance. Figure 40 shows the impacts of a varied transformer reactance per simulation on the peak DC line current.

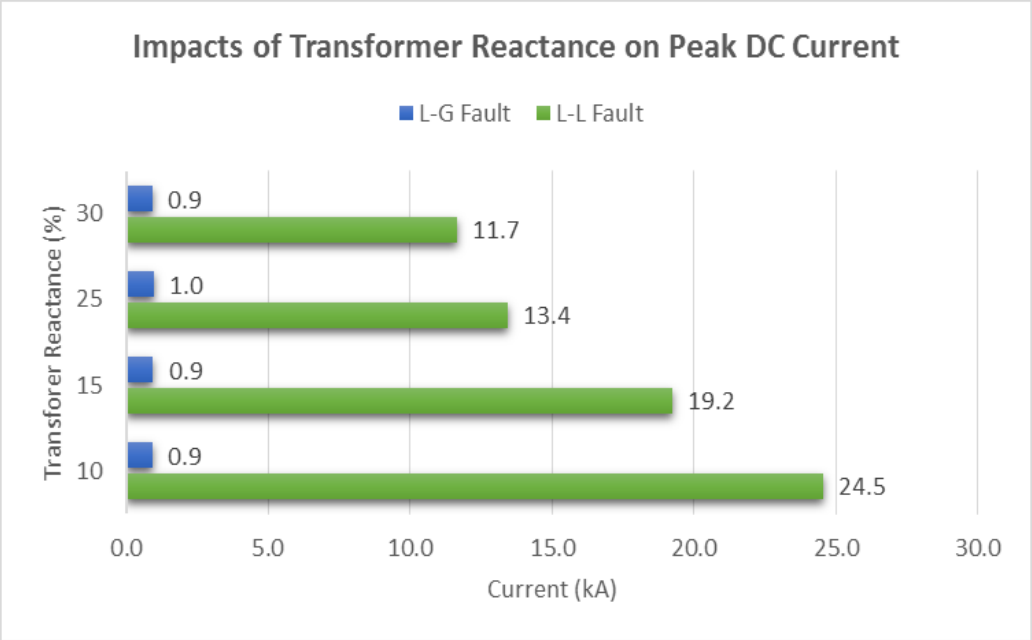

Figure 40: Impacts of Transformer Reactance on Peak DC Currents

One apparent observation is that L-L faults cause much higher currents, which is expected according to the nature of L-L faults. When comparing transformer reactance values for L-L fault currents, the significance drawn from the results is that the higher the transformer reactance, the lower the DC line current. This is expected of impedance on the system of any notable magnitude. When comparing transformer reactance values for L-G fault currents, there is essentially no variance in current, and therefore hardly any significance to be drawn from the results for L-G faults. Accordingly the impact of transformer reactance variance is primarily seen in L-L fault cases. It is apparent that the transformer reactance has a large impact upon the peak DC line fault current, much more impact when compared to the DCL and the arm reactance on the system. Over the DCL and the arm reactance combined, the transformer is the most dominant impedance on the HVDC system and consequently of the three has the most impact upon the peak DC fault current.

The transformer reactance range of 0.10 p.u. up to 0.30 p.u. (10% - 30%) dictates a range of variance in the DC line fault current from 24.5 kA down to 11.7 kA. This large range in peak fault current quantifies the dominance of the transformer reactance in the system as compared to the DC line reactance (DCL) and the converter arm reactance.

The magnitude of 0.25 p.u. was ultimately selected as the transformer reactance for the HVDC protection analysis. This was the same value implemented in the model validation in chapter 2. Consultation was obtained from personnel from Mitsubishi Electric that a 0.25 p.u. transformer reactance should be selected based off of experience of transformer installations at the 500kV voltage level. Also as advised by Mitsubishi Electric personnel an X/R ratio of 100 was maintained. With the 0.25 p.u. transformer reactance selection for the protection analysis, transformer winding (copper) losses of R = 0.0025 p.u. was implemented corresponding to an X/R ratio of 100 being maintained.

3.3 TREND OF ASYMMETRICAL ARM REACTANCE

The comparison of the next two trends is of notable interest – the comparison of asymmetrical and symmetrical arm reactance. Asymmetrical arm reactance implies arm reactors placed only on the lower three converter arms, while symmetrical arm reactance implies arm reactors placed on both the upper three phase arms and the lower three phase arms. Reference Figure 41 to visualize these two differing configurations of arm reactance in the context of the modular multilevel converter topology.

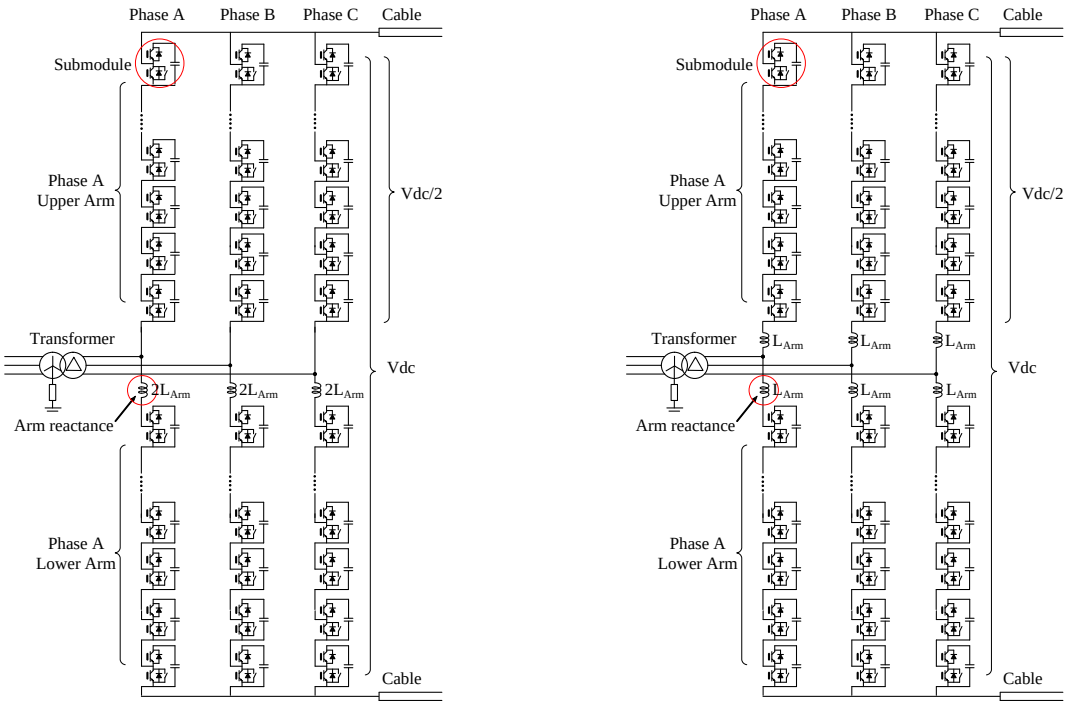

Figure 41: Comparison of Asymmetric (Left) and Symmetric (Right) Arm Reactance

The comparison of these arm reactance circuit configurations is of notable interest because it determines whether asymmetrical or symmetrical arm reactance should generally be used in the MMC topology design to best perform the aforementioned function. Consequently this also determines which will be used in the final system protection analysis in this work.

The function of converter arm reactance is twofold: 1) limiting the DC line fault current for the protection of the converter devices and 2) smoothing out harmonics and noise for a clean converter output signal. These system functions are essentially identical to that of the DCL, but simply located in a different location on the system. Lower peak DC line fault current is desirable based off of the function of the arm reactance – limiting the DC fault current. Lower peak DC line fault current is expected with increased arm reactance. This plays into the selection of the DCL for the system protection analysis.

Table 6 lists the cases associated with a sensitivity analysis of asymmetrical arm reactance in the converter. Note that Cases 1-1-1 and 1-1-2 are the base cases (validation model).

Table 6: Case List Showing Variance of Asymmetrical Arm Reactance

	DCL	Transformer reactance	Arm inductance	BPS speed	AC short circuit capacity	DC length	Fault case
	(mH)	(%)	(%)	(ms)	(GVA)	(km)	
Case1-4-1	0	25	5 lower	10	25	1,000	L-L
Case1-4-2	0	25	5 lower	NA	25	1,000	L-G
Case1-1-1	0	25	**10 lower**	10	25	1,000	L-L
Case1-1-2	0	25	**10 lower**	NA	25	1,000	L-G
Case1-4-3	0	25	15 lower	10	25	1,000	L-L
Case1-4-4	0	25	15 lower	NA	25	1,000	L-G
Case1-4-5	0	25	30 lower	10	25	1,000	L-L
Case1-4-6	0	25	30 lower	NA	25	1,000	L-G

Figure 42 shows the impacts of a varied asymmetrical arm reactance on the peak DC current. These are the results obtained from running all of the cases listed in Table 6. The peak currents are expected to decrease as arm reactance increases. This is relatively the case for the results presented in Figure 42, with the exception of the 30% asymmetrical arm reactance case for which peak DC current increases with an increase of arm reactance. This inconsistency can easily be explained with the fact that all peak DC currents are approximately equivalent. The increase of peak DC current for an increase of arm reactance is in fact a minimal increase if any. With this observation it is accurate to infer that variance of asymmetrical arm reactance does not have a large impact upon peak DC current. But the parameter is still necessary to the converter design for the protection of devices. From Figure 42, 10% seems to be an appropriate asymmetric selection based off the fact that any larger reactance is unnecessary to achieve the

same results. This 10% ($X_{Arm,p.u.} = 0.10$) correlates to an impedance value calculated from the base system impedance as shown below:

$$Z_{Base} = \frac{V^2}{S_{MVA}} = \frac{(500kV)^2}{1050MVA} = 238.1\Omega$$

For 10% arm reactance with 5% margin ($X_{Arm,p.u.} = 0.105$):

$$L_{Arm} = X_{Arm,p.u.} \frac{Z_{Base}}{2\pi f} = 0.105 \frac{238.1\Omega}{377} = 66.31mH$$

This 66.31 mH is the asymmetrical arm reactance that would be implemented for the protection analysis if the asymmetric configuration is found to be more effective than the symmetric configuration. The arm reactance value selected for the protection analysis ultimately depends upon this comparison of asymmetric and symmetric impacts.

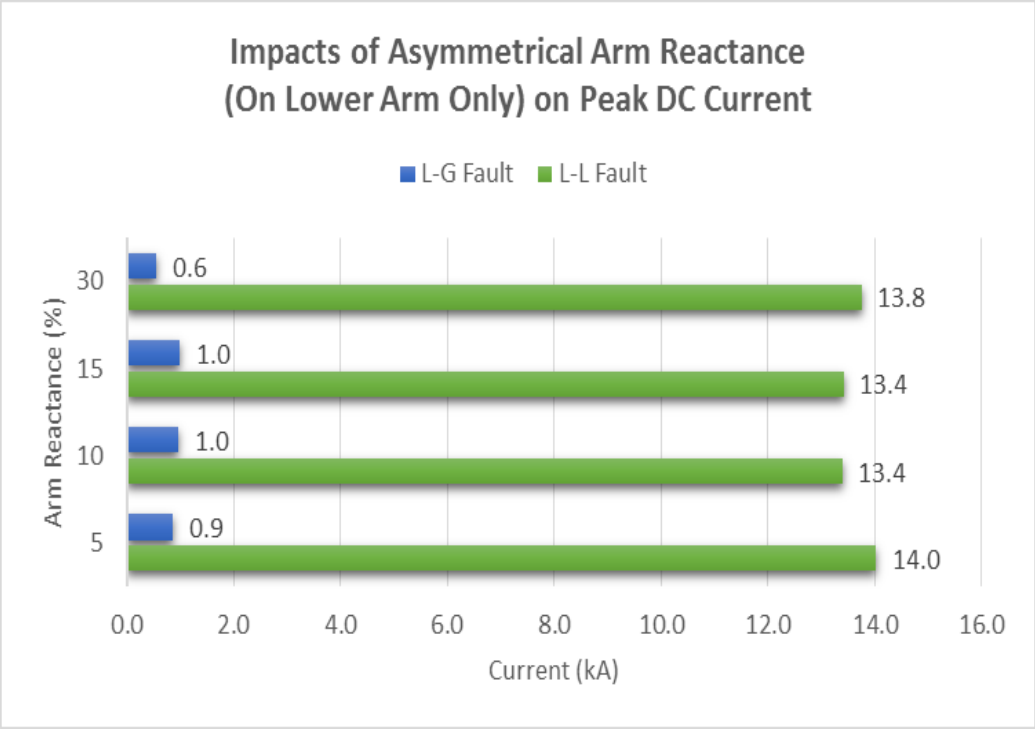

Figure 42: Impacts of Asymmetrical Arm Reactance on Peak DC Current

3.4 TRENDS OF SYMMETRICAL ARM REACTANCE

Installing symmetrical arm reactance essentially indicates that whatever value would have been installed asymmetrically on the lower arms (previous parameter trend analyzed) is now divided into two halves and installed on both the upper and lower converter arms. Therefore the 10% asymmetric case can be compared to the 5% symmetrical case due to being the same amount of reactance in the converter system. The asymmetric case lumps all arm reactance on the lower converter arms, while the symmetric case divides the lumped amount of arm reactance between the upper and lower arms. This comparison is clarified in Figure 41 with the notation $2L_{Arm}$ and L_{Arm} corresponding to asymmetric and symmetric arm reactance respectively.

Table 7 lists the cases associated with a sensitivity analysis of the symmetrical arm reactance. Figure 43 shows the impacts of symmetrical arm reactance on the peak DC current.

Table 7: Case List Showing Variance of Symmetrical Arm Reactance

	DCL	Transformer reactance	Arm inductance	BPS speed	AC short circuit capacity	DC length	Fault case
	(mH)	(%)	(%)	(ms)	(GVA)	(km)	
Case1-6-1	0	25	5 up and low	10	25	1,000	L-L
Case1-6-2	0	25	5 up and low	NA	25	1,000	L-G
Case1-6-3	0	25	10 up and low	10	25	1,000	L-L
Case1-6-4	0	25	10 up and low	NA	25	1,000	L-G

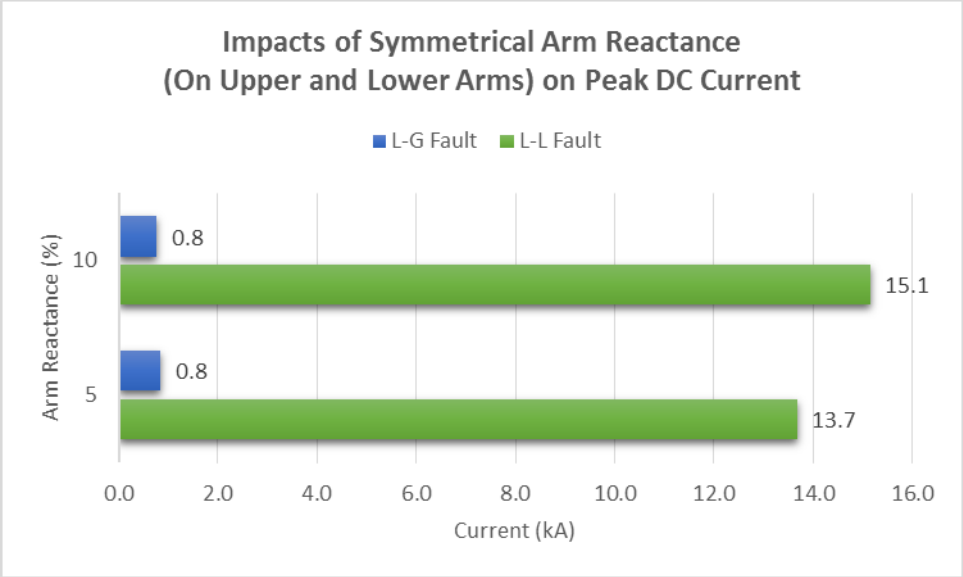

Figure 43: Impacts of Symmetrical Arm Reactance on Peak DC Currents

Upon comparison of asymmetric and symmetric configurations, these results from Figure 43 compared to Figure 42 show that the asymmetric configuration is more effective than the symmetric configuration. The 10% asymmetric can be compared to the 5% symmetric which provides 13.4 *kA* compared to 13.7 *kA* respectively. The asymmetric configuration is more effective due to better performing the arm reactance function, limiting peak DC fault current. Additionally, the 10% symmetric case shown in Figure 43 results with 15.1 *kA* which is higher peak DC fault current than any asymmetric case run. Even the 30% asymmetric case which is comparable to 15% symmetric (more reactance than the 10% symmetric) results in 13.8 *kA* which is less than 15.1 *kA*. For the protection analysis, the asymmetric configuration will be utilized. Correspondingly, the 66.31 *mH* arm inductance calculated in the last section will be implemented for the protection analysis.

In the end, the combination of DC line reactance, transformer reactance, and asymmetric arm reactance parameter values that was implemented for the protection analysis were:

- DC line reactance: 10 mH (with 0.02 Ω)
- Transformer reactance: 25% = 0.25 p.u. (with 0.0025 p.u.)
- Asymmetric arm reactance: 10% = 66.31 mH (with 0.056 Ω)

This combination of reactance on the system resulted with the best performance for the protection analysis simulation. The sensitivity analysis process in obtaining this combination of reactance selections is valuable to a generic design of the MMC-HVDC system when considering the best performance in terms of protection. .

3.5 TREND OF BYPASS SWITCH (BPS) SEED

Table 8 lists the cases associated with a sensitivity analysis of the bypass switch speed. Note that these cases only include line-to-line fault cases due to the fact that the bypass switch (BPS) is only switched in as a form of protection for a L-L fault. Only L-L faults generate a circuit dynamic of circulating currents which in turn threaten to damage the freewheeling diodes within the half bridge submodule topology.

Table 8: Case List Showing Variance of Bypass Switch (BPS) Speed

	DCL	Transformer reactance	Arm inductance	BPS speed	AC short circuit capacity	DC length	Fault case
	(mH)	(%)	(%)	(ms)	(GVA)	(km)	
Case1-5-1	0	25	10.0	5	25	1,000	L-L
Case1-5-2	0	25	10.0	6	25	1,000	L-L
Case1-5-3	0	25	10.0	7	25	1,000	L-L
Case1-5-4	0	25	10.0	8	25	1,000	L-L
Case1-5-5	0	25	10.0	9	25	1,000	L-L
Case1-1-1	0	25	10.0	**10**	25	1,000	L-L
Case1-5-6	0	25	10.0	11	25	1,000	L-L
Case1-5-7	0	25	10.0	12	25	1,000	L-L
Case1-5-8	0	25	10.0	15	25	1,000	L-L

The bypass switch (BPS) speed is defined by the amount of time that passes between the occurrence of the fault on the system and the thyristor bypass switch being turned on. This is a significant parameter since the bypass switch is the first layer of protection for the half bridge submodules in the MMC topology. For the system faults being analyzed we can expect the DC line currents to rise quickly and therefore we expect to see significant impacts of the BPS speed upon the peak DC line fault currents. The faster the BPS is switched into the circuit, the peak DC currents are expected to be lower. Figure 44 shows the impacts of a varied bypass switch speed on the peak DC current. These results are as expected. With the BPS speed incrementally varied from 5 ms to 15 ms, we see a range of peak DC line fault currents from 9.5 *kA* to 15.2 *kA* respectively. The BPS speed has significant impact upon the peak DC line fault currents.

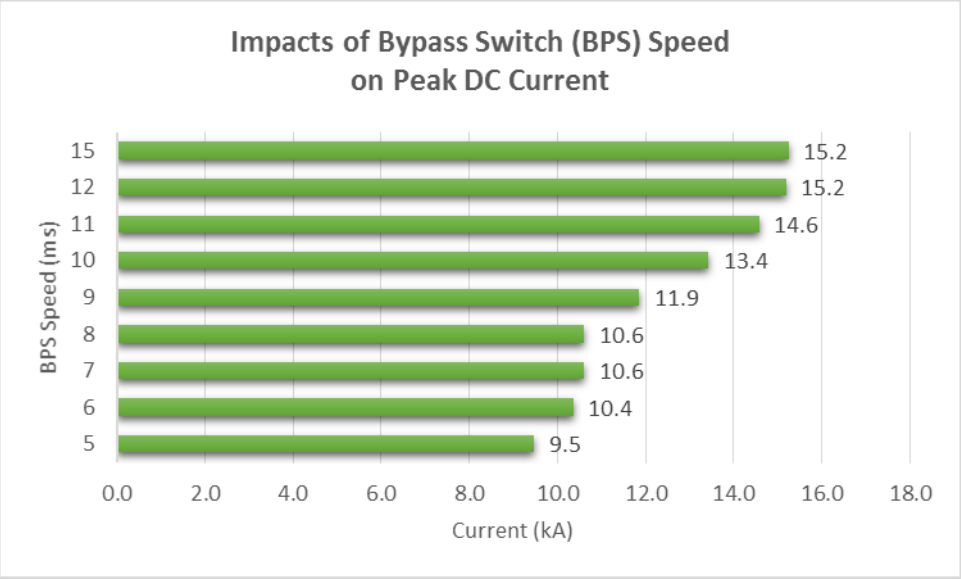

Figure 44: Impacts of Bypass Switch Speed on Peak DC Current

From previous discussion, a conservative limitation of 15 *kA* for the peak DC line fault current is desired for the sake of device protection. Time delay for power electronics varies depending upon the system design. For the HVDC protection analysis, it is desirable to analyze the worst case scenario within the protection limitations set for the HVDC system design. This worst case scenario within the set limit of 15 *kA* corresponds to the 11 ms case in Figure 44 at 14.6 *kA*. Because this value is too close to the limitation for comfort, the BPS speed of 10 ms, corresponding to 13.4 *kA*, was therefore selected for the protection analysis.

3.6 TRENDS OF SHORT CIRCUIT STRENGTH

A short circuit strength is defined by the system impedance and the amount of rotational inertia on the system [28]. System rotational inertia originates from induction machine power generation. The short circuit strength of the HVDC system model being analyzed is dictated by

the system impedance associated with the equivalent AC grids on either end of the HVDC transmission system. For example if the HVDC line were to be interconnecting an isolated wind farm, this would be an AC grid of weak short circuit strength due to the lack of inherent inertia generated from a wind farm. This is a critical parameter to analyze for an HVDC system due to HVDC becoming a choice technology for applications such as weak wind farm grids among others [2], [5], [6]. The weaker the system, the higher the system impedance. Therefore what is expected from this trend analysis is that the peak DC line fault current would have lower peaks for a weaker system due to the increase of system impedance limiting the AC grid current feeding the DC side fault. Correspondingly higher peak DC line fault currents are expected for a stronger short circuit strength because of less AC grid system impedance.

Table 9 lists the cases for a sensitivity analysis of the system short circuit strength.

Table 9: Case List Showing Variance of Short Circuit Strength

	DCL	Transformer reactance	Arm inductance (lower arm)	BPS speed	AC short circuit capacity	DC length	Fault case
	(mH)	(%)	(%)	(ms)	(GVA)	(km)	
Case1-7-1	0	25	10.0	10	9.5	1,000	L-L
Case1-7-2	0	25	10.0	NA	9.5	1,000	L-G
Case1-1-1	0	25	10.0	10	**25**	1,000	L-L
Case1-1-2	0	25	10.0	NA	**25**	1,000	L-G
Case1-7-3	0	25	10.0	10	55	1,000	L-L
Case1-7-4	0	25	10.0	NA	55	1,000	L-G

These short circuit strength values originate from the minimum and maximum short circuit currents that the system is rated for – 11 *kA* and 63 *kA* corresponding to 9,500 *MVA* and 55,000 *MVA* respectively. The rated short circuit strength corresponds to 25,000 *MVA*.

This trend is valuable to observe in order to note how the system will handle the same DC line fault under different system strengths, minimum and maximum short circuit strengths. Figure 45 shows the trending impacts of the varied short circuit strength on the peak DC current.

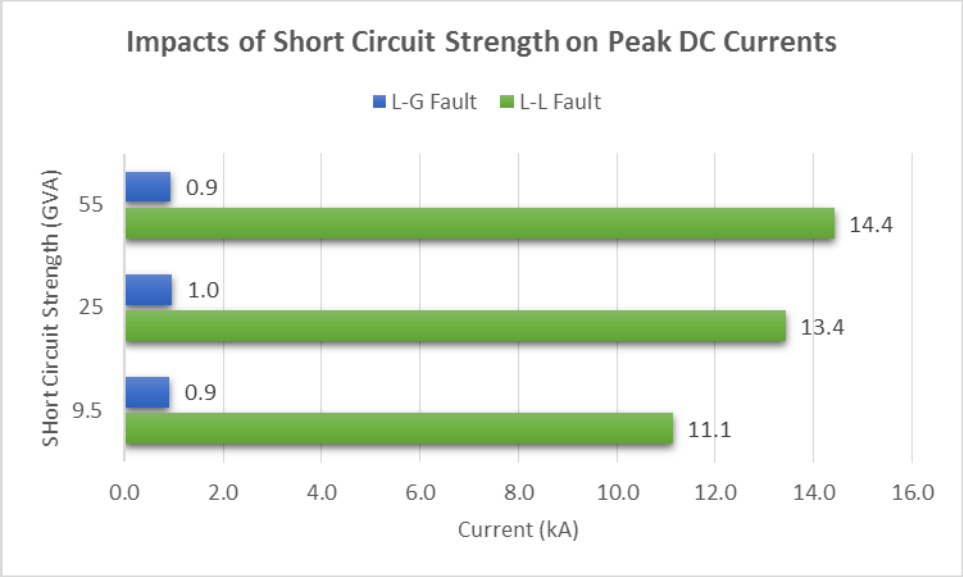

Figure 45: Impacts of Short Circuit Strength on Peak DC Currents

From these results we can see that at both the minimum and maximum operating system strengths the peak DC line fault currents are within the set 15 *kA* protection limitation. Therefore at least for the base parameters, the system protection will be able to handle the worst fault case with the set range of short circuit strength. It is also clear that with an increase in system short circuit strength there is an increase in peak DC line fault current. These results are as expected from our previous discussion.

3.7 TREND OF DC LINE LENGTH

When analyzing the impact of the length of the DC line upon the peak DC line fault current, each of the simulated lengths were divided equally between cable and overhead (OH) line. For example when 800 km was simulated, 400 km of the line was cable while the other 400 km was OH line. Table 10 lists the cases associated with a sensitivity analysis of the DC line length.

Table 10: Case List Showing Variance of DC Line Length

	DCL	Transformer reactance	Arm inductance	BPS speed	AC short circuit capacity	DC length	Fault case
	(mH)	(%)	(%)	(ms)	(GVA)	(km)	
Case1-8-1	0	25	10.0	10	25	800	L-L
Case1-8-2	0	25	10.0	NA	25	800	L-G
Case1-1-1	0	25	10.0	10	25	**1,000**	L-L
Case1-1-2	0	25	10.0	NA	25	**1,000**	L-G
Case1-8-3	0	25	10.0	10	25	1,200	L-L
Case1-8-4	0	25	10.0	NA	25	1,200	L-G

Figure 46 shows the impacts of a varied DC line length on the peak DC current.

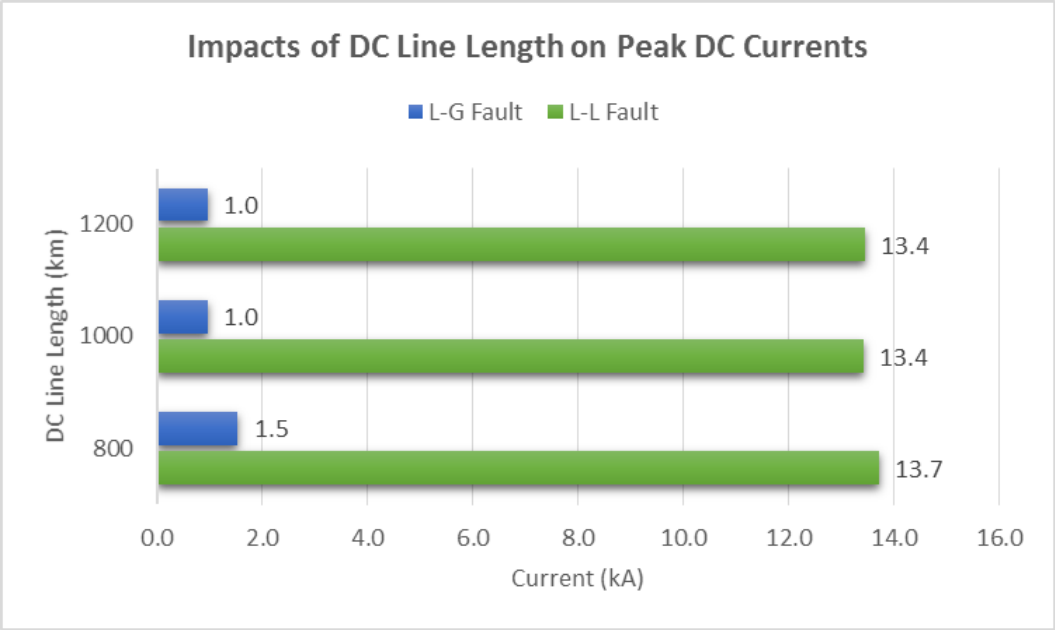

Figure 46: Impacts of DC Line Length on Peak DC Currents

These results show that with a shorter the line length the peak DC line fault current increases but only minimally. Both L-G and L-L fault cases are consistent with this result. For the 1200 km case, beyond 1000 km, the peak fault currents do not decrease but remain the same in magnitude. With this reasoning it is safe to perform the protection analysis with a 1000 km DC line. In the end we are investigating long distance transmission applications of HVDC.

3.8 TREND OF HVDC LINE CONFIGURATION

Table 11 lists the cases associated with a sensitivity analysis of the HVDC line configuration.

Table 11: Case List Showing Variance of HVDC Line Configuration

	Tx X	Arm inductance	BPS speed	AC short circuit capacity	Fault case	DC Line Configuration
	(%)	(%)	(ms)	(GVA)		(500 km each section)
Case1-9-1	25	10.0	10	25	L-L	Cable only (1000 km)
Case1-9-2	25	10.0	NA	25	L-G	Cable only (1000 km)
Case1-9-3	25	10.0	10	25	L-L	Cable (Sending) OHL (Receiving)
Case1-9-4	25	10.0	10	25	L-L	Cable (Sending) OHL (Receiving)
Case1-9-5	25	10.0	10	25	L-L	Cable (Sending) OHL (Receiving)
Case1-9-6	25	10.0	NA	25	L-G	Cable (Sending) OHL (Receiving)
Case1-9-7	25	10.0	NA	25	L-G	Cable (Sending) OHL (Receiving)
Case1-9-8	25	10.0	NA	25	L-G	Cable (Sending) OHL (Receiving)
Case1-9-9	25	10.0	10	25	L-L	OHL (Sending) Cable (Receiving)
Case1-9-10	25	10.0	10	25	L-L	OHL (Sending) Cable (Receiving)
Case1-9-11	25	10.0	10	25	L-L	OHL (Sending) Cable (Receiving)
Case1-9-12	25	10.0	NA	25	L-G	OHL (Sending) Cable (Receiving)
Case1-9-13	25	10.0	NA	25	L-G	OHL (Sending) Cable (Receiving)
Case1-9-14	25	10.0	NA	25	L-G	OHL (Sending) Cable (Receiving)

The line configuration is defined as what makes up the DC line, whether it is only cable for all 1000 *km* or a combination of cable and overhead (OH) line in a specific order. The specific order can be cable on the terminal *A* half of the system and OH line on the terminal *B* half, or vice versa as expressed in Table 11. In this trend analysis, a worst case scenario in terms of peak DC line current determined the selection for the protection analysis. A line configuration that resulted in worst case peak DC line currents was desired for a protection analysis. Figure 47 shows the impacts of a varied line configuration on the peak DC current.

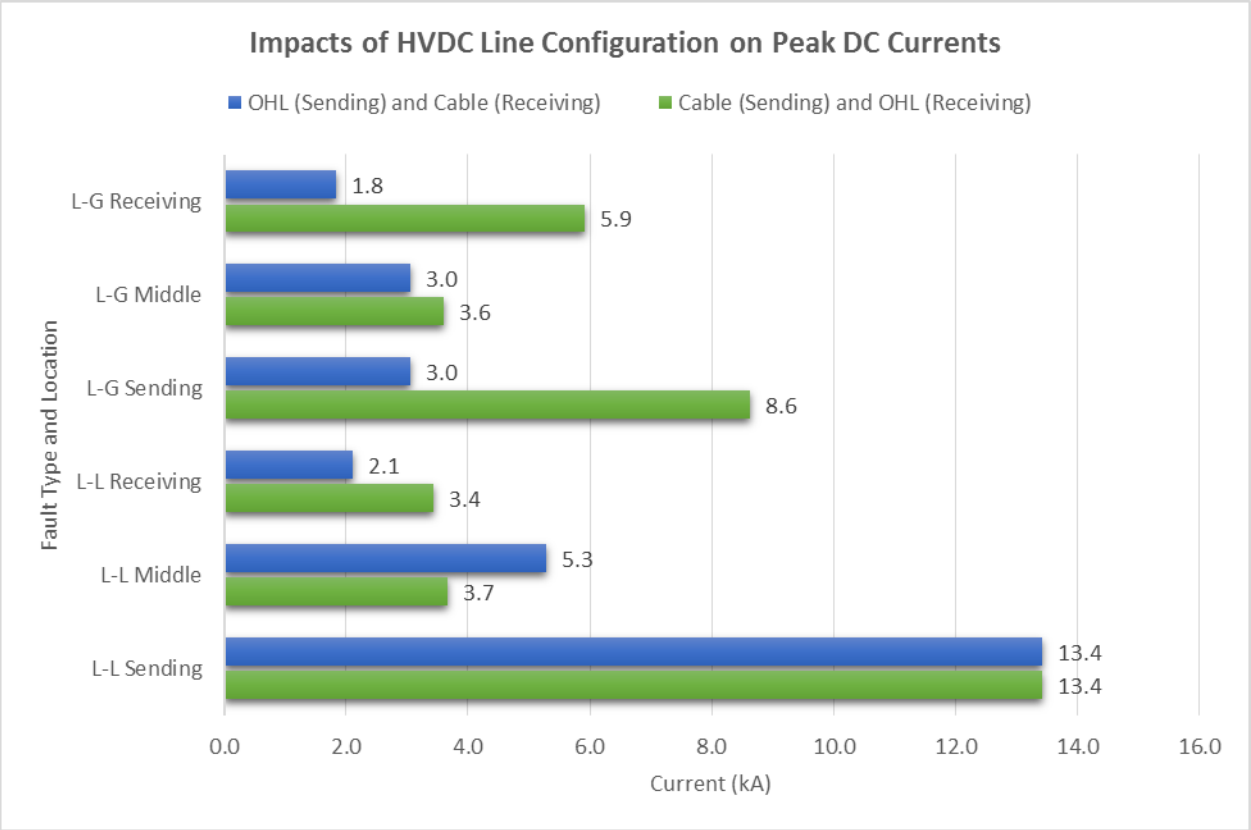

Figure 47: Impacts of HVDC Line Configuration on Peak DC Currents

This trend analysis is somewhat different than the rest due to introducing multiple fault locations, sending end, midpoint, and receiving end of the HVDC line. With the exception of the L-L fault located at the midpoint of the line, the HVDC line configuration that resulted with the higher peak DC line fault currents is the cable (sending) and OH line (receiving). This configuration identifies the cable as located on terminal *A* side and the OH line as located on terminal *B* side. It is apparent from Figure 47 that this line configuration is the worst case scenario configuration. Therefore this configuration will be implemented for the protection analysis in order to design protection for the worst case scenario which will in turn be sufficiently conservative for the second configuration.

3.9 CONCLUSION

In conclusion of observing the impact that the various system parameters have on the peak line current during a fault, the parameter values appropriate for a protection analysis have been purposely selected. The validated MMC-HVDC model can now be implemented with the parameters desired for an analysis of the HVDC system protection. Now it is appropriate to probe the system design with various faults of differing type and location to determine a protection design. Table 12 summarizes the parameters that were selected as a result of this trends sensitivity analysis.

Table 12: Parameters Selected from Trends Analysis for Protection Analysis

Parameter:	Protection Analysis Parameters:
DCL Impedance	10 *mH*
Transformer Reactance	25 % = 157.9 *mH*
Asymmetric Arm Reactor Impedance	10 % = 66.31 *mH*
Symmetric Arm Reactor Impedance	NA
BPS Operation Speed	10 *ms*
AC Short-Circuit Capacity	25 *GVA*
DC Line Length	1000 *km*
DC Line Configuration	OH line (sending) Cable (receiving)

4.0 FAULT ANALYSIS AND EVALUATION OF CHARACTERISTIC SIGNAL

This chapter covers the background of the protection implemented into the HVDC model for the purpose of supporting the solutions proposed in this work. Also covered is an explanation of the fault analysis performed to analyze the protection needs of the system and evaluate whether a relay coordination scheme can be implemented into this HVDC system. Lastly this chapter covers the evaluation of an oscillation signal found through the fault analysis.

4.1 SYSTEM PROTECTION BACKGROUND

For the given MMC-HVDC system there is a need to define a protection scheme to appropriately handle DC faults scenarios. The goal of handling a system fault is to isolate it, diminish it and return the system to full power operation in a short period of time. This presents two phases of protection: 1) fault detection and isolation, and 2) system restart sequence.

The appropriate and sufficient design for the first phase of protection is ultimately to implement overcurrent protection. The way in which overcurrent protection works is that when a preset current relay threshold is surpassed in the system current measurements, the associated relay sends a signal to activate a protection sequence. Protection within the MMC converter stations themselves is based upon this type of relay protection where the converter arm currents will have a threshold set at 3.348 kA. When the converter arm currents surpass 3.348 kA, the

protection sequence for the entire HVDC system is activated. In order of operation this protection sequence includes gate block, bypass switch, and AC circuit breaker (ACCB) operations. Figure 48 demonstrates the activation of this protection sequence.

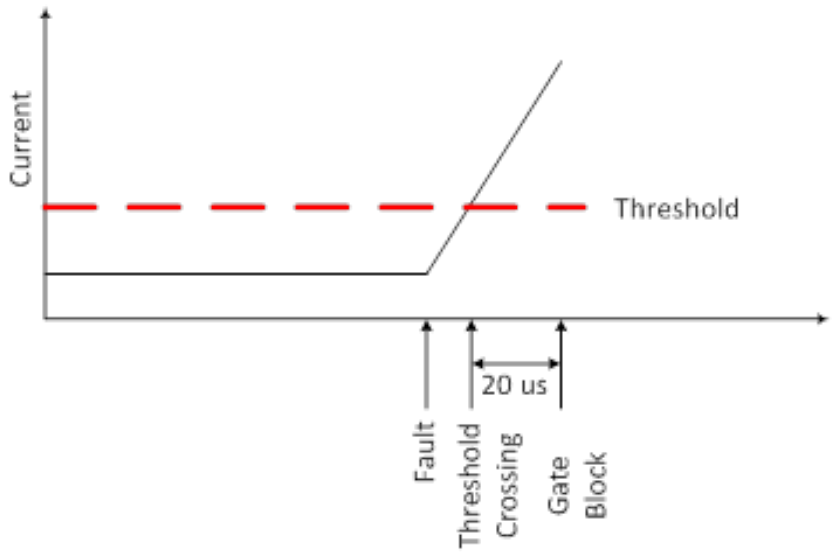

Figure 48: Overcurrent Protection as the Initiation of the System Protection Sequence

Table 13 shows the timing of this sequence of operations. All fault case scenarios that were simulated with active protection followed this timing sequence. The final step in the first phase of protection is the decay of all fault current in the system. Once the ACCB operation has occurred the DC portion of the system is completely isolated from the rest of the grid. Consequently all currents will go to zero, but the speed in which the remaining fault current goes to zero varies significantly. Depending upon the fault type and location this fault current takes approximately 2 seconds or a little longer to decay to zero in simulation.

Table 13: Protection Sequence

Time[s]	Fault	VSC			Remark
		ACCB	BPS	controller	
0	OFF	Close	Open	DCAVR	Steady state, P=1000MW from VSC1 to VSC2
0.1	**ON**	Close	Open	DCAVR	Apply DC fault
0.10002	ON	Close	Open	**GB**	Gate block both VSC1 and VSC2, 20us after fault
0.11	ON	Close	**Close**	GB	Close all BPSs to protect FWD
0.167	ON	**Open**	Close	GB	Open all ACCBs to interrupt fault current from AC system
1	ON	Open	Close	GB	Wait for decaying DC fault current

The second phase of protection involves the restart of the HVDC system once the protection sequence has been followed through until all fault current has decayed to zero. The desire is that the system would be delivering full power flow as soon as possible. This involves a restart sequence beginning with reclosing the circuit breakers, then allowing the voltage to stabilize, and lastly beginning to require power flow again. This restart sequence will only be successful if the fault has been successfully cleared before attempting to reclose the breakers. Therefore if the fault is temporary an automatic restart sequence will be successful.

On the other hand, if the fault is permanent the restart sequence will only be successful after the permanent fault has been manually fixed by a utility repair crew that drives out to the location of the fault. Only after repair of a permanent fault can the restart sequence successfully return the HVDC system to normal operation.

The challenge of section identification arises with the process of reclosing the circuit breakers. Knowing whether the fault is a temporary or permanent fault is desirable. If the fault is temporary the restart sequence is activated. Reclosing is attempted as the start of that sequence. But if the fault is permanent, reclosing the breakers is not attempted until that permanent fault is cleared manually.

The difficulty in the given system is ultimately determining whether a given DC fault is located on the overhead (OH) line or on the cable portion of the entire HVDC line. This process will be termed as section identification. Through our work we have found a characteristic phenomenon specific to this HVDC system that helps to achieve section identification within the protection scheme.

4.2 FAULT PROTECTION ANALYSIS

The protection fault analysis was performed for the purposes first of all, to observe the dynamic response to various faults and second, to determine a characteristic signal existent on all DC fault cases on the system that would be useful in implementing a section identification method. The analysis was organized into four sets of simulation cases as shown below:

1. Without power flow, without protection
2. Without power flow, with protection
3. With power flow, without protection
4. With power flow, with protection

The simulation cases with protection implement the sequence of gate blocking, bypass switch, and circuit breaker operations as described in Table 13. For cases specified without protection, no measures are taken to isolate the fault. The comparison of cases with and without protection enables an evaluation of whether or not the system protection is performing effectively. The simulation cases designated as with power flow simply means that the converter controller regulates a power reference of 1.0 p.u. – an operational state of full power flow is regulated. For the case of without power flow, the controller regulates a power reference of 0.0 p.u. – an

operational state of no power flow is regulated. The comparison of cases with and without power flow enables an evaluation of identifying root causes of dynamics on the system.

Each simulated case was also organized into a numbered system specifying fault location and whether or not protection is implemented as depicted in Table 14. Note that the entirety of cases from Table 14 were simulated both with and without power flow. This is consistent with the overall organization of the protection analysis.

Table 14: Sets of Cases for the Fault Protection Analysis

		Protection Sequence:		Fault Location:		
		With	Without	MMC Station	DC Line	AC Grid
Case No.	3-1-###	•		•		
	3-2-###	•			•	
	3-3-###	•				•
	3-4-###		•	•		
	3-5-###		•		•	
	3-6-###		•			•

This table is a compressed form of the extensive fault protection analysis case list. The expanded form of the fault protection analysis table is included in Appendix *A*. Each set of cases from Table 14 (3-#-###) includes an assortment of fault types and locations as depicted in Figure 49.

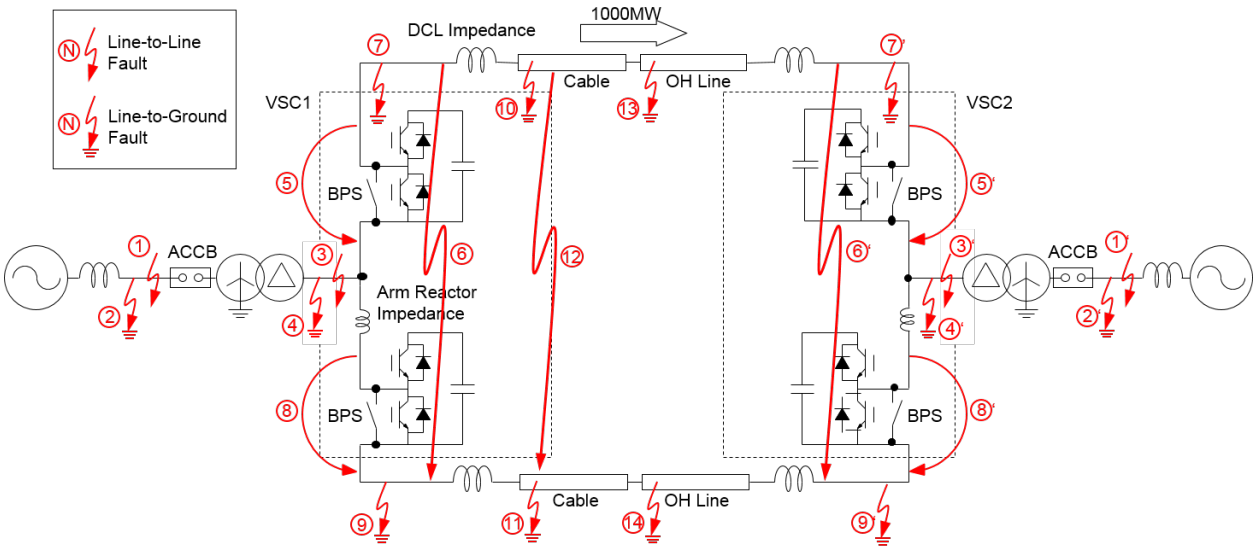

Figure 49: Fault Locations and Types for All Case Scenarios for the Fault Protection Analysis

For each simulation, depicts all of the voltage and current measurement locations that were monitored for the fault protection analysis. The measurement symbols depicted are voltage and current transformers as specified in the legend.

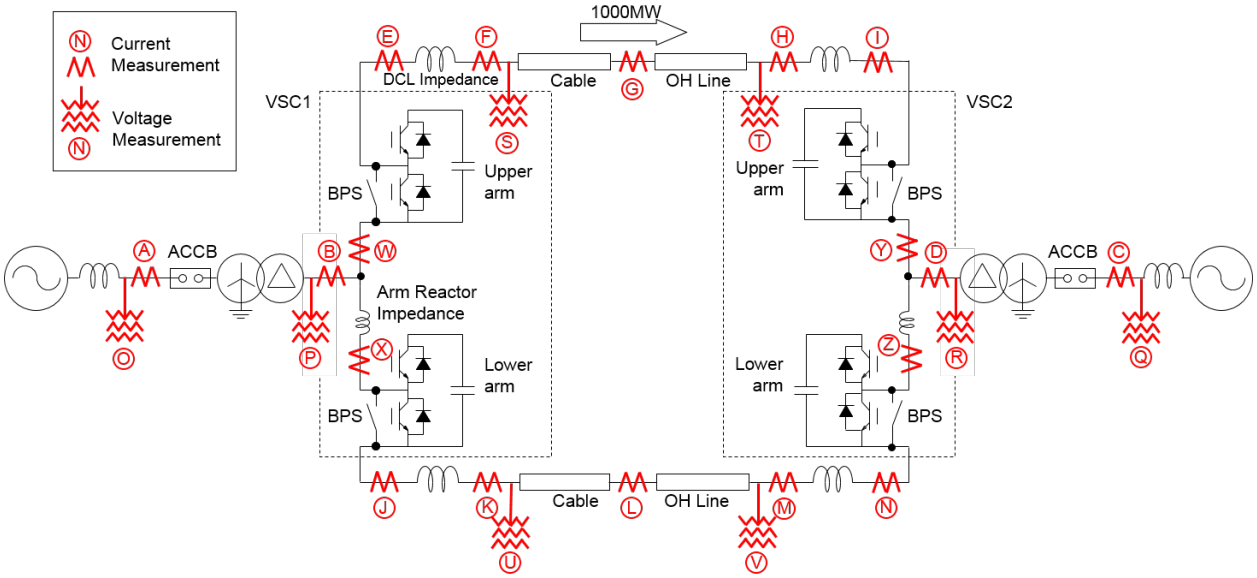

Figure 50: HVDC System Voltage and Current Measurements Monitored for Fault Protection Analysis

For each case, all voltage and current results were analyzed and compared to other case results. The investigations were performed systematically, comparing “with power” to “without power” as well as comparing “with protection” to “without protection” among all fault types and locations. All analysis and comparisons were performed for the purposes of first, to confirm that the system results were as expected and second, but more importantly, to uncover a unique characteristic signal that will enable a section identification protection method with the implementation of protection relays.

4.3 CHARACTERISTIC SIGNAL FOR SECTION IDENTIFICATION

For the purpose of finding a solution to section identification an examination of all signals of the various fault case scenarios was performed. Upon in-depth analysis of the system voltages and currents there was a distinct characteristic that showed up within DC fault case scenarios as compared to any AC fault cases. This characteristic was the presence of an oscillation that shows up on voltage and current measurements specifically after the AC circuit breaker already operated – opening the breakers. The measurements spoken of are the current measurements F, H, K, M and voltage measurements S, T, U, V. Reference Figure 51 to picture where these measurements are located on the HVDC system.

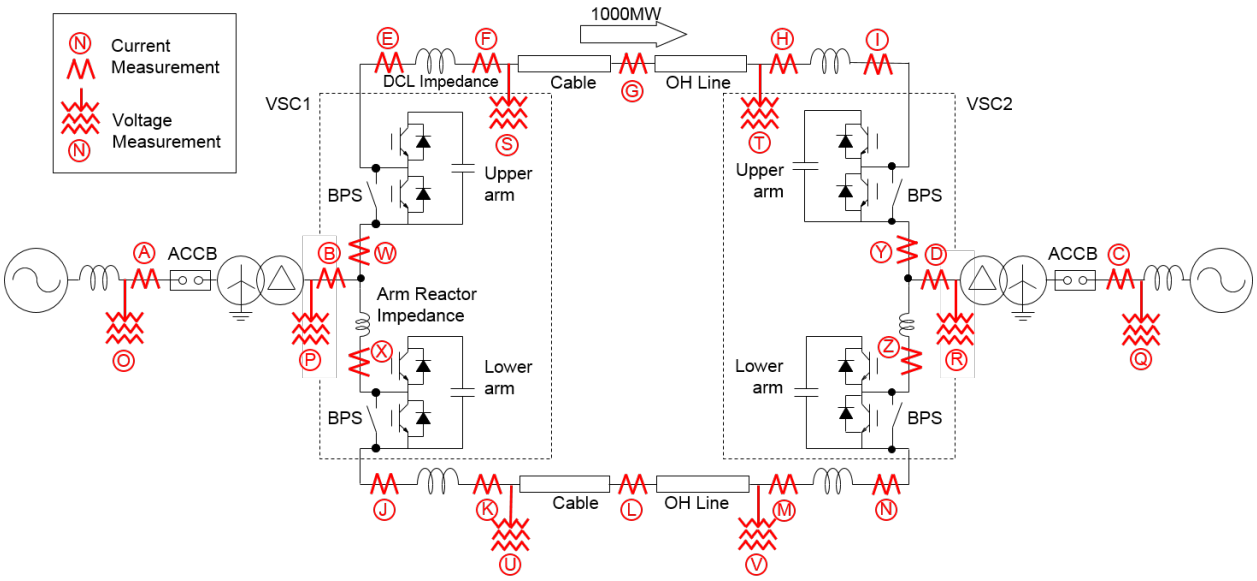

Figure 51: HVDC System Voltage and Current Measurements

When the fault occurs on the DC portion of the system these voltage measurements [S, T, U, V] are expected to go to zero within a time frame of anywhere between instantaneously to approximately 60 milliseconds depending upon how close the measurement is to the point of the fault. This voltage zero will continue through circuit breaker operation. When the breakers open 67 ms after the fault the expectation is that the specified current measurements would all go to zero relatively quickly, depending primarily upon the fault type. Regardless of the speed of current dissipation in the system and regardless of the fault type, the currents are reasonably expected to have magnitudes below approximately 1kA post the ACCB operation.

Contrary to these expectations, there exists oscillations in a select few of the voltages and currents post ACCB operation. Additionally the location of the oscillation depends upon where the corresponding DC fault is located. Taking case 3-1-407 as an example case to analyze the phenomena, Figure 52 and Figure 53 are sample current and voltage measurements.

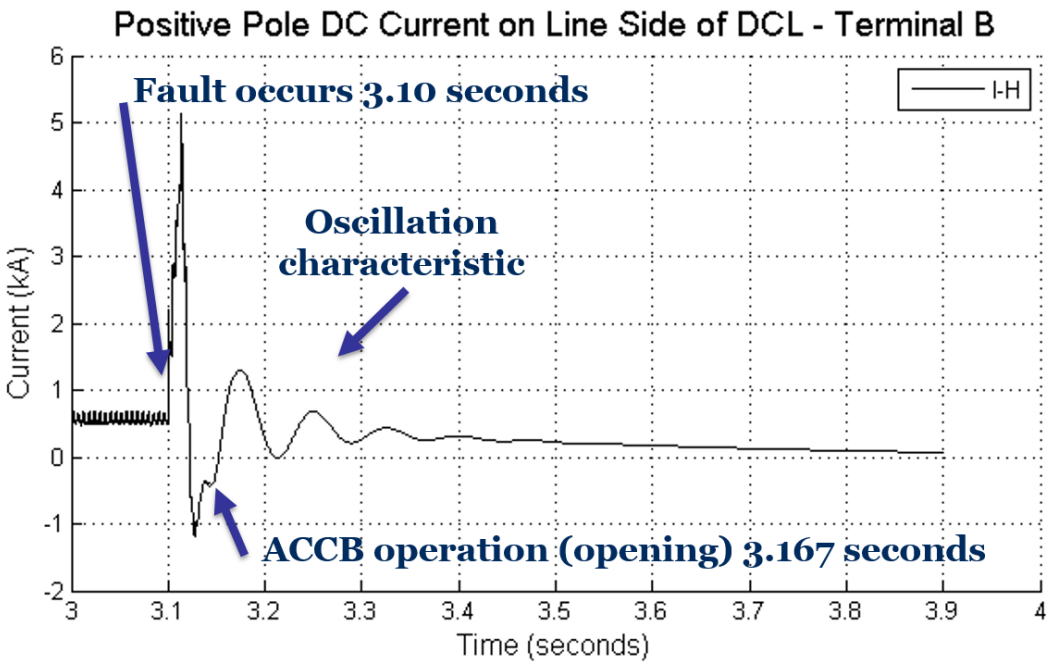

Figure 52: Example of Current Oscillation in Case 3-1-407

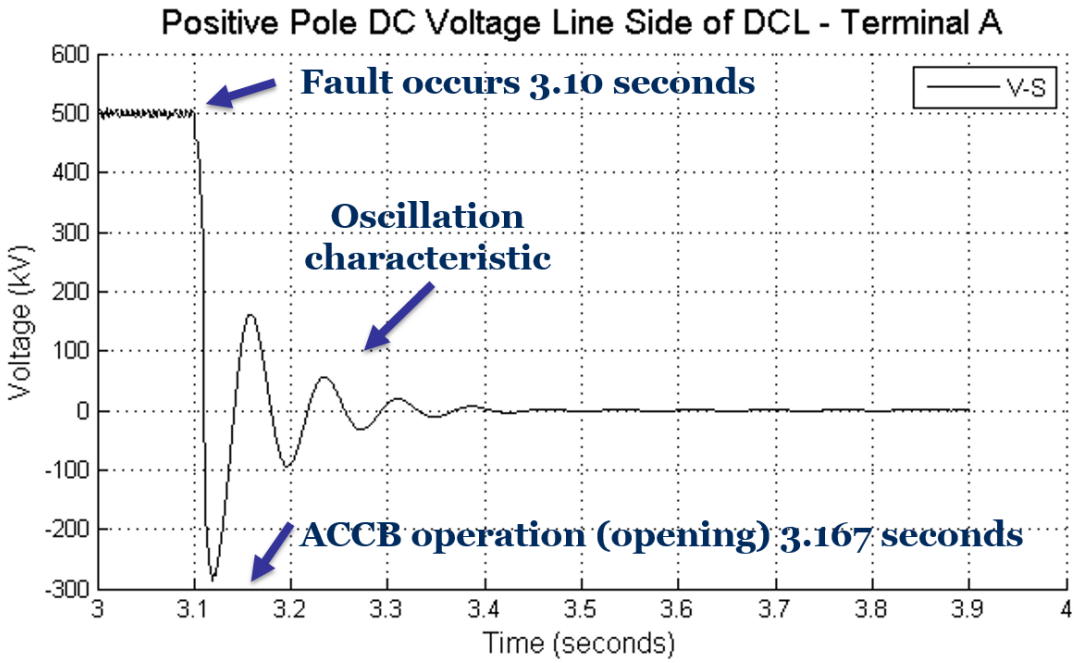

Figure 53: Example of Voltage Oscillation in Case 3-1-407

Case 3-1-407 is simulated with full power demanded as well as the initial protection sequence incorporated. This case includes a line-to-ground fault located on the positive terminal of the HVDC line at the receiving end of the OH line. For reference, the locations for all fault scenarios for all cases are depicted in Figure 54. Case 3-1-407 corresponds to the fault (7').

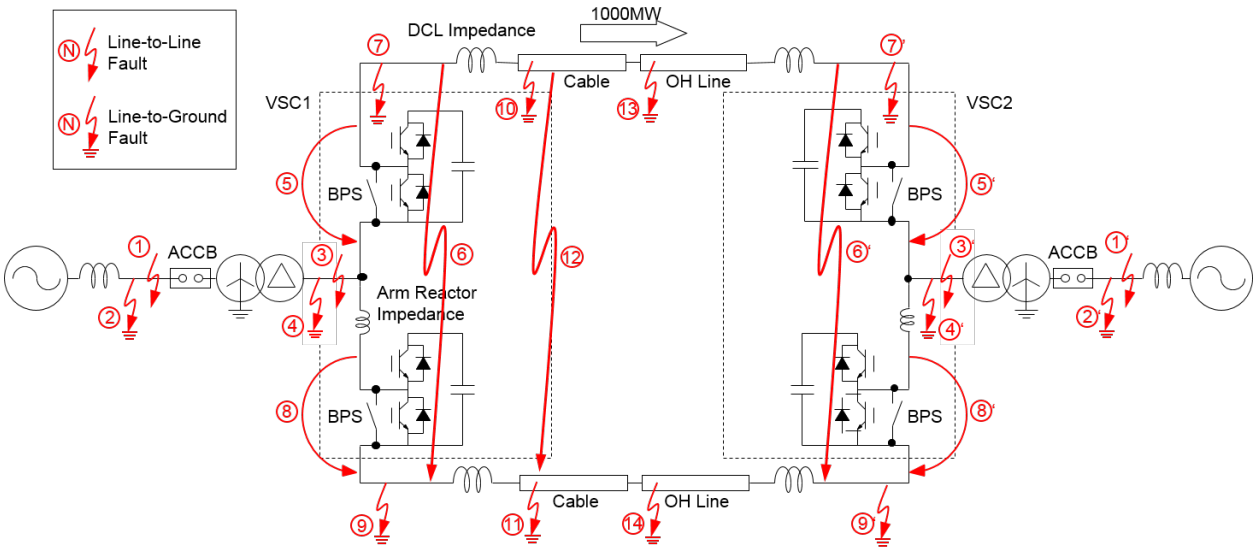

Figure 54: Fault Locations for all Case Scenarios

In determining the oscillation's usefulness the root cause of the phenomena first needed to be found. Upon further analysis the cause of the oscillations post ACCB operation are caused by current flow having passed through the cable in the HVDC system. The following example in Figure 55 demonstrates this root cause of phenomena. With current flowing towards the fault on the HVDC line, it is apparent in the following example that the oscillations exist in the current measurement after passing through cable and not before.

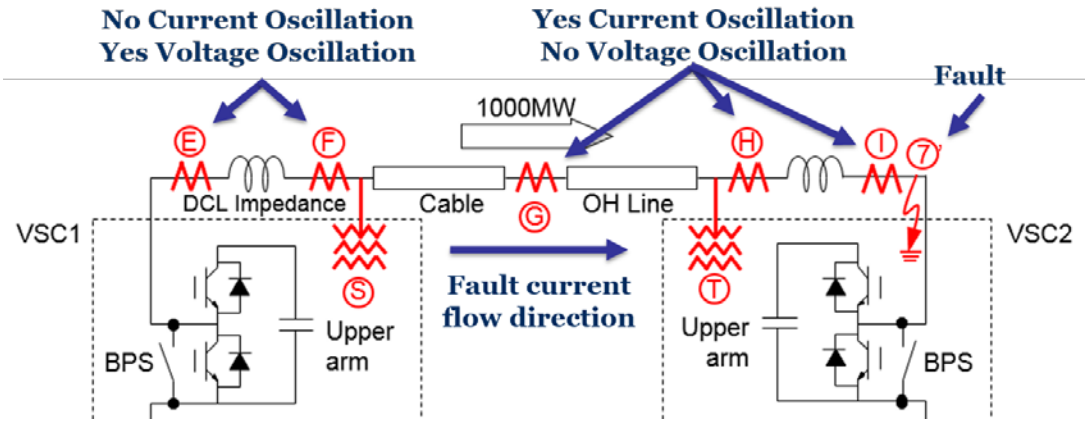

Figure 55: Positive Terminal of Example Case 3-1-407 showing Signal Oscillation Caused by Capacitive Nature of Cable

Corresponding with Figure 55, Figure 56 shows four of the current signals across the positive HVDC terminal. These current signals clearly show that the oscillation characteristic appears in the current immediately after passing through the cable. The oscillation does not exist in current measurement *F* but does exist in current measurement *G*.

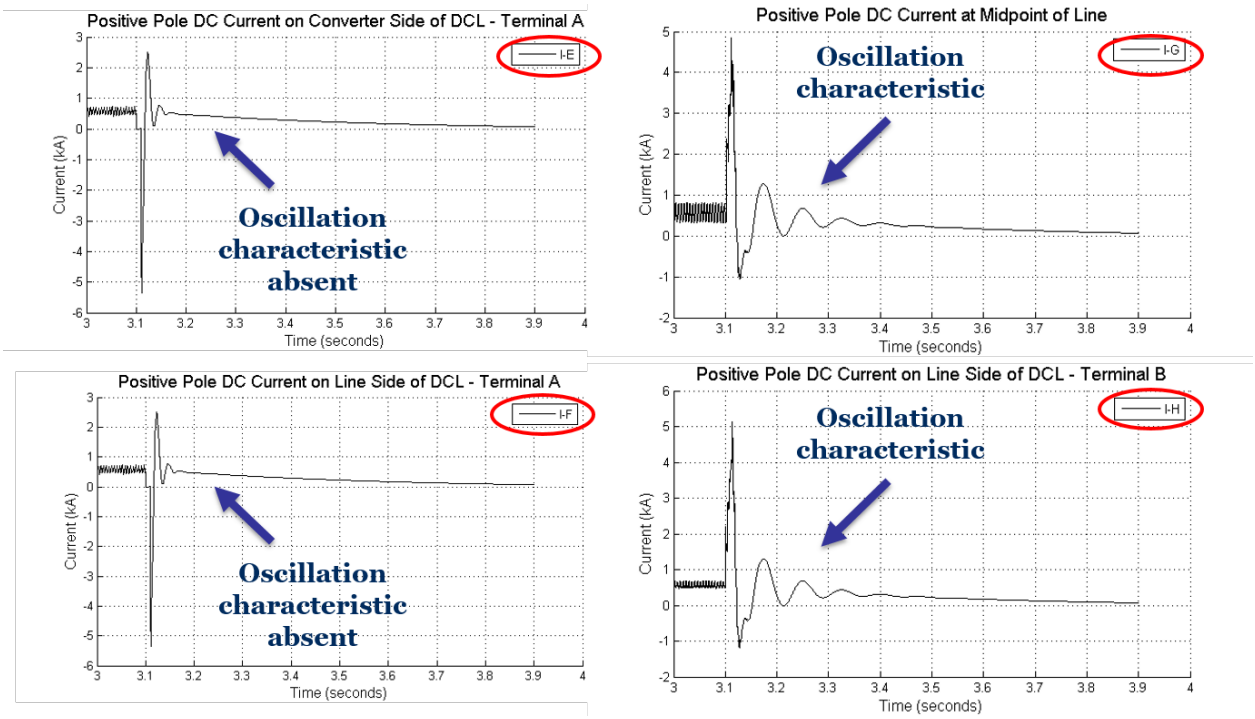

Figure 56: Case 3-1-407 Positive Terminal Currents showing that Signal Oscillation Appears in Current after Passing through Cable

Upon evaluating Figure 56, there is no other option but to conclude that the cable is a root cause of the oscillations. This evaluation is consistent among all other DC fault case scenarios. It seems that the oscillation is somehow triggered by the capacitive nature of the cable. Any oscillations in the voltage signals [S, T, U, V] (i.e. Figure 53) are consequently caused due to the current oscillating.

It is necessary to investigate the origin of the oscillation in order to be able to depend upon it as a part of the section identification protection method. Upon analysis of the oscillations across multiple cases it is apparent that there is a distinct frequency common among them. Figure 57 analyzes this frequency by approximating the period of the signal.

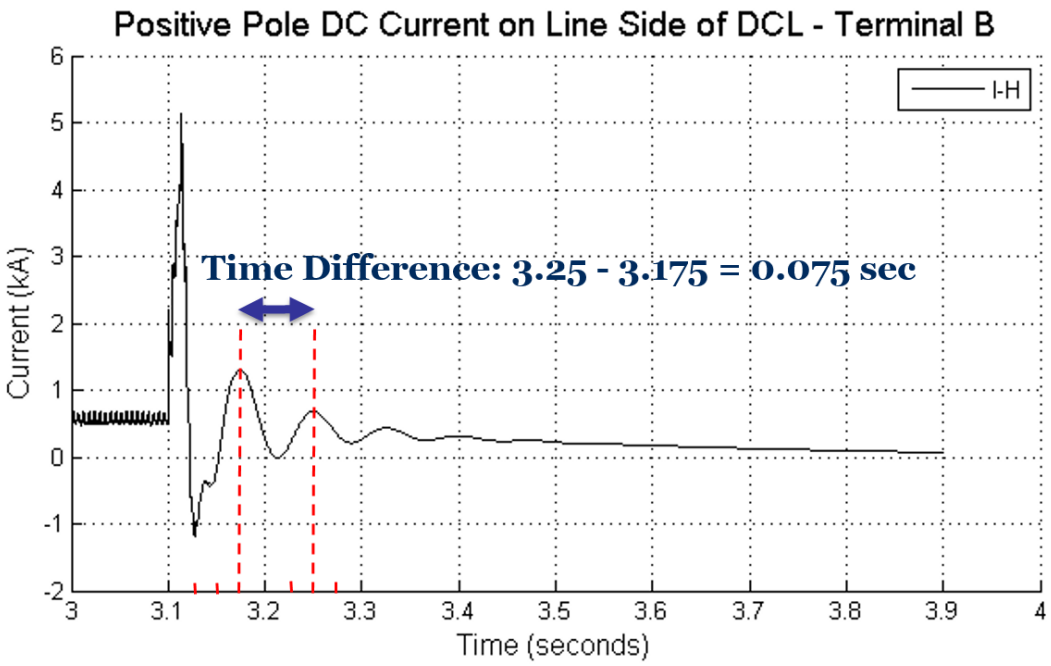

Figure 57: Example of Current Oscillation in Case 3-1-407 with the Period of

The period of the oscillation frequency is approximately 0.075 seconds according to Figure 57 when measuring from one peak to another peak of the oscillation signal. With this approximate period the frequency is calculated as shown here:

$$f_{Oscillation} = \frac{1}{T} \approx \frac{1}{3.25 - 3.175} = \frac{1}{0.075} = 13.33Hz$$

The oscillation consists of a notably low frequency which could be explained by being driven by a large inductance on the system. To determine the ultimate cause of this oscillation it is necessary to analyze the equivalent circuit at the time of its existence with lumped parameter pi-model approximations in place of the distributed cable and OH line models. It is desirable to show that this oscillation consists of an expected frequency according to circuit analysis of the natural frequencies on the equivalent system.

This oscillation occurs after the BPS switches and the ACCBs have all operated. In other words it occurs in the protected, isolated state of the DC system. With this knowledge, Figure 58 depicts the equivalent circuit for the fault case 3-1-407 where the L-G fault is located on the receiving end of the DC line.

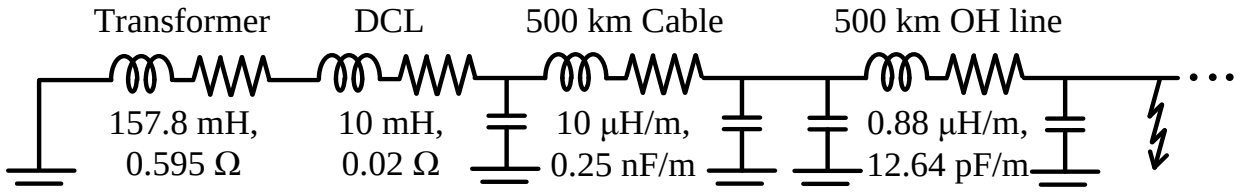

Figure 58: HVDC System Equivalent RLC Circuit for Case 3-1-407 Post ACCB and BPS Operation

The converter arm reactance is not included in this equivalent circuit because arm reactance only exists in the lower converter arms for the fault protection analysis. This fault case currently being analyzed is a line-to-ground fault on the positive terminal of the DC side which means the upper arms, without arm reactance, are in the equivalent circuit.

The oscillation is reasonably expected to be a natural frequency of this equivalent circuit. Also note from Figure 57 that the oscillation dissipates after a few cycles. The oscillation dissipates through the resistances of this circuit shown in Figure 58. The resistance in this circuit can be ignored when determining the resulting natural frequency of the system. In the big picture, the root cause of the oscillation frequency needs to be identified, and resistance does not significantly affect the frequency. Therefore Figure 59 can be analyzed as a simplified version of the initial circuit schematic.

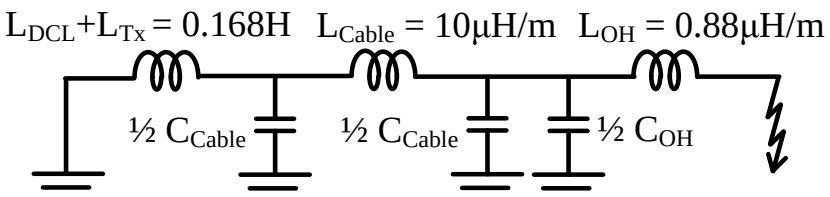

Figure 59: Simplified Equivalent LC Circuit for Case 3-1-407 for Determining Oscillation Frequency

The values associated with each inductance and capacitance in this circuit were determined according to the following calculations and evaluations. The transformer and DC line reactance values are the same values that were determined from the previous section. The transformer calculations from per unit base to inductance were performed as follows.

$$X_{Tx,p.u.} = 0.25\,p.u.$$

$$Z_{Base} = \frac{V^2}{S_{MVA}} = \frac{(500kV)^2}{1050MVA} = 238.1\Omega$$

$$X_{Tx} = X_{Tx,p.u.}Z_{Base} = (0.25\,p.u.)(238.1\Omega) = 59.5\Omega$$

$$L_{Tx} = \frac{X_{Tx}}{2\pi f} = \frac{59.5\Omega}{2\pi(60)} = 157.97mH$$

This transformer inductance is a significant magnitude at least compared to the DC line reactance, as can be seen in Figure 58 for comparison. Utilizing the geometric mean radius (GMR) parameter of the simulated overhead line model, the following inductance and capacitance per meter were determined:

$$L_{OH} = \frac{\mu_0}{\pi}\ln\left(\frac{1}{GMR}\right) = 2*10^{-7}\ln\left(\frac{1}{0.0122834m}\right) = 0.8799\,\mu H/m$$

$$C_{OH} = \frac{2\pi\varepsilon}{\ln\left(\frac{1}{GMR}\right)} = \frac{2\pi\left(8.85*10^{-12}\right)}{\ln\left(\frac{1}{0.0122834}\right)} = 12.6392\,pF/m$$

These approximate calculations were taken from chapter 9 of Greenwood [29]. Next, through a frequency sweep of the frequency dependent cable model, the cable inductance and capacitance per meter were determined. PSCAD generates an output file of the cable model providing reactance (X) and susceptance (B) per meter in matrix form. An output file was created for the cable model for each frequency of the frequency sweep. As an example, the 0.1 Hz output file can be seen in Appendix A. From each output file, corresponding to the various frequencies, the inductance and capacitance per meter were calculated. Shown below are the calculations for the 0.1 Hz case of the frequency sweep, with the inductance and capacitance per meter values taken from the PSCAD cable output file.

$$L_{Cable} = \frac{X}{2\pi f} = \frac{6.36\,{}^{\mu H}\!/_{m}}{2\pi(0.1Hz)} = 10.1\,{}^{\mu H}\!/_{m}$$

$$C_{Cable} = \frac{B}{2\pi f} = \frac{0.157\,{}^{nF}\!/_{m}}{2\pi(0.1Hz)} = 0.25\,{}^{nF}\!/_{m}$$

The PSCAD cable model and corresponding calculations were performed for the following frequencies: 0.01, 0.1, 1, 10, and 60 Hz. The frequency sweep of the frequency dependent cable model generated the results in Table 15.

Table 15: Frequency Sweep of Cable Capacitance and Inductance per Meter for the Frequency Dependent Cable Model in Simulation

Frequency (Hz)	Inductance (μH/m)	Capacitance (nF/m)
0.01	10.4	0.25
0.1	**10.0**	**0.25**
1	7.1	0.25
10	1.9	0.25
60	0.9	0.25

This sweep allowed for a rough estimate of what inductance and capacitance to select for an approximate natural frequency calculation. From these results in Table 15 the following cable inductance and capacitance per meter were chosen for the equivalent lumped parameter circuit.

$$L_{Cable} = 10\mu H / m$$

$$C_{Cable} = 0.25nF / m$$

The selected inductance and capacitance per meter for the frequency dependent model is an approximate assumption for the purpose of the oscillation frequency validation. The inductance per meter selected is less accurate of an assumption than the capacitance per meter since it varies over the frequency sweep, but for the purposes of approximating the frequency of the oscillation the 10 μH/m is a sufficient selection.

Now that the equivalent circuit element values are known, calculating the expected natural frequencies is the next step. The following Laplace domain expression of this type of LC circuit was determined from Greenwood, end of chapter 3 [29].

$$s^4 + s^2\left(\frac{1}{L_1C_1} + \frac{1}{L_2C_2} + \frac{1}{L_2C_1}\right) + \frac{1}{L_1L_2C_1C_2} = 0$$

Where the *L* and *C* parameters correspond to the following calculations to match the equivalent circuit components:

$$L_1 = L_{Tx} + L_{DCL} = 157.97mH + 10mH = 168mH$$

$$L_2 = L_{Cable} = \left(10\,{}^{\mu H}\!\!\diagup\!\!{}_{m}\right)(500km) = 5H$$

$$C_1 = \frac{1}{2}C_{Cable} = \frac{1}{2}\left(0.25\,{}^{nF}\!\!\diagup\!\!{}_{m}\right)(500km) = 62.5\mu F$$

$$C_2 = \frac{1}{2}C_{Cable} + \frac{1}{2}C_{OH} = 62.5\mu F + \frac{1}{2}\left(12.64\,{}^{pF}\!\!\diagup\!\!{}_{m}\right)(500km) = 65.66\mu F$$

Note that C_2 is the parallel combination of the capacitances $½C_{Cable}$ and $½C_{OH}$ as seen in Figure 59. Using the software tool MATLAB, the roots of this fourth order system were determined. These roots are the eigenvalues of the system and correspond to the angular frequencies of the system. These angular frequencies were converter to the natural frequencies, dividing by $2\pi f$. The results are provided:

$f =$

0.0000 +49.9648i
0.0000 -49.9648i
0.0000 + 8.6354i
0.0000 - 8.6354i

Of these two sets of natural frequencies on the imaginary axis, the 8.635 Hz roughly corresponds to the 13.33 Hz oscillation signal observed in the fault analysis results. These frequencies are close enough to validate the cause of the oscillation being the natural frequency of the equivalent circuit in Figure 59.

5.0 FAULT SECTION IDENTIFICATION PROTECTION METHOD

With a stronger comprehension of the cause of the oscillations on the system, it is now possible to explore a section identification protection method that applies this oscillation as a characteristic signal of the HVDC system design. First it is essential to cover the basis of how to approach the development of the section identification. The proposed method needs to meet desired conditions on the design, previously introduced in the introduction of this work. Next, the fault case scenarios that are incompatible with the initially proposed protection method are discussed and accounted for in order to ensure that the section identification method performs successfully for all fault case scenarios. Lastly, details are covered for the practical implementation of this system restart protection method with the utilization of protection relays.

5.1 BASIS FOR PROPOSED NOVEL PROTECTION METHOD

5.1.1 Conditions Met and Oscillation Applied

According to the desired HVDC design presented in the introduction of this work, the desired method of detecting DC fault locations needs to meet the following conditions:

1. Method preferably will not use a communication channel because the detection of a DC fault location needs to operate very quickly in the case of a VSC-based HVDC system

2. Assumption can be made that the sampling interval is 175 μs (3.75 degrees of electrical angle)
3. If past sampling data is needed for detecting the DC fault location, it is desirable that the number of past sampling data is limited to 3 samples
4. Both cable and overhead line sections making up the HVDC line
5. HVDC technology implementing the MMC topology
6. Only AC protection devices utilized in protecting against DC side fault scenarios

Note that conditions 2 and 3 are related, both being relay measurement limitations. Also note that conditions 4, 5 and 6 have already been met from the onset of modeling the MMC-HVDC system. The ultimate goal is to use protective relays that will be triggered by characteristic signals specific to the given HVDC system for a section identification method while satisfying these conditions. The section identification protection method presented in this work successfully meets these conditions. Conditions 1, 2 and 3 will be discussed further, and the characteristic signal to be used by the proposed method is the oscillation signal that appears post ACCB operation consisting of a low frequency.

Upon observation of all case results we found that the existence of oscillation (post ACCB operation) in either voltage or current specifically corresponds to any L-G fault in the OH line section. On the other hand, the absence of oscillations in either voltage or current (post ACCB operation) corresponds to a L-G DC fault in the cable section. As seen in Figure 60, Case 3-1-407 has a L-G OH line fault and oscillations exist. This corresponding fault is located on the positive terminal at the receiving end of the OH line, shown as fault (7)' in Figure 54.

Case 3-1-404 shown in Figure 61 is an example of a L-G cable fault where there are no existing oscillations. This corresponding fault is located on the positive terminal at the sending end of the cable, shown as fault (7) in Figure 54. These observations can be effectively used for a section identification method.

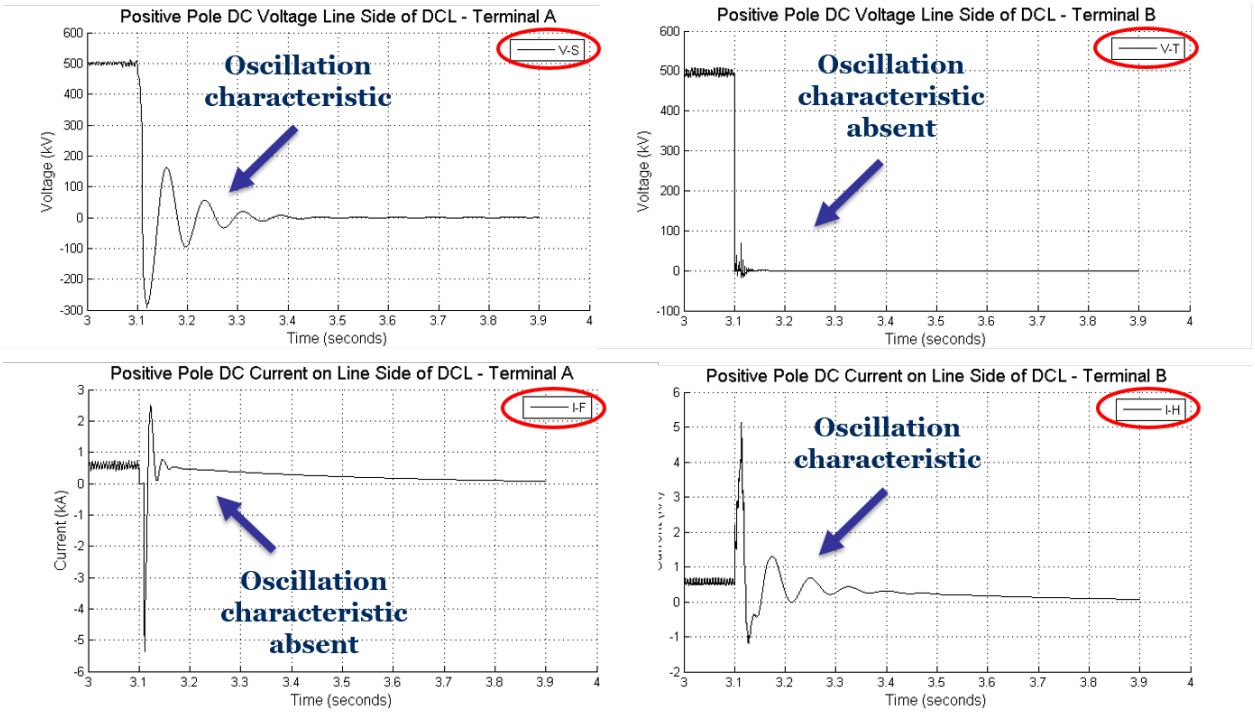

Figure 60: Case 3-1-407 Positive Terminal Voltage and Current Measurements are Consistent with Complementary Distinctive

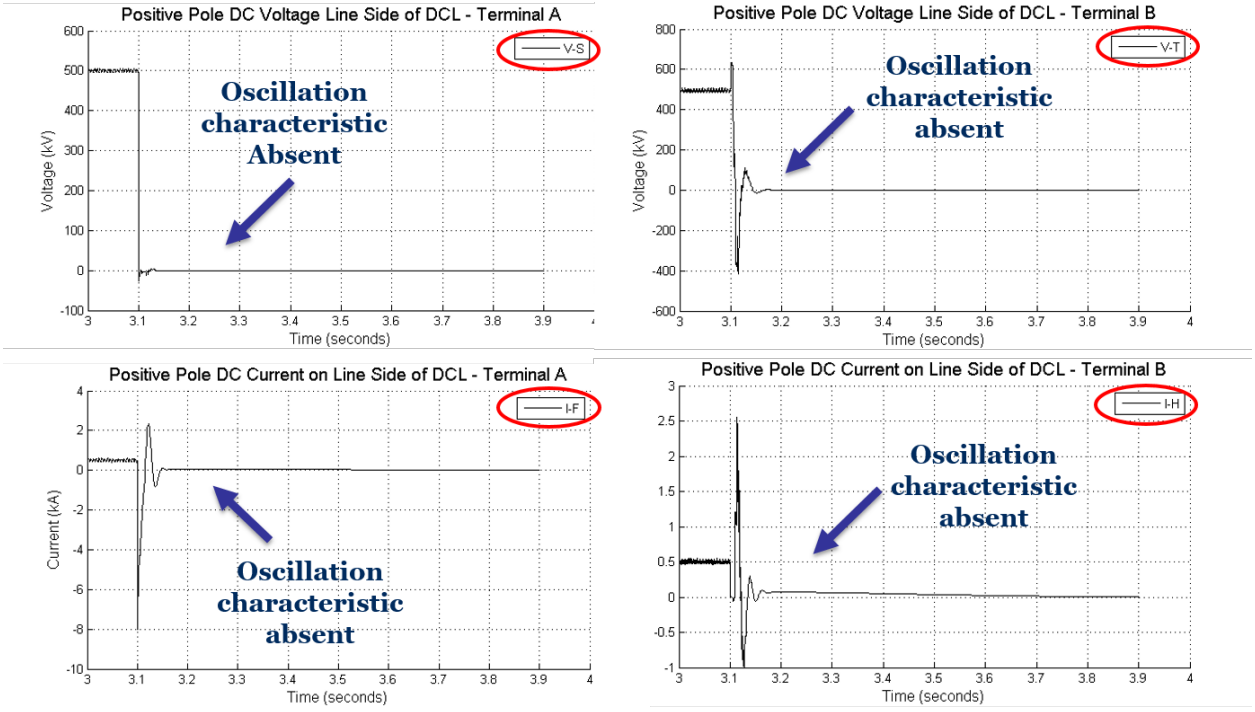

Figure 61: Case 3-1-404 Positive Terminal Voltages and Currents for Line-to-Ground Cable Fault with an absence of any Oscillation

Recall that when there is a cable fault we do not want to initiate a reclose or restart sequence. When there is an OH line fault we do want to initiate an attempt at reclosing the breakers. Based upon observation of all L-G faults, oscillations do not exist post ACCB operation for cable faults while they do for OH line faults. All L-G DC fault cases had oscillation results similar in nature to Case 3-1-407 or to Case 3-1-404 depending upon whether it was an OH line or cable fault respectively. Based upon observation of all L-G DC fault cases through the lens of the oscillation detection method, it is possible to identify the location of all L-G DC faults.

When an oscillation exists after ACCB operation and is detected in either voltage or current, the restart sequence will be initiated because of an OH line section fault location. If no oscillation is detected after ACCB in either voltage or current, the restart sequence will not be initiated because of a cable section fault location. The reason for not restarting is that all cable faults can be assumed to be permanent faults. An attempt of reclose performed on a permanent fault is termed as a false reclose. A false reclose by definition is an unsuccessful reclose. Reclosing on a permanent fault will only result in feeding the fault and potentially damaging system components (i.e. converter, transformer, etc.). It is therefore desirable to eliminate false reclosing as much as possible. Hence there is the desire to identify which section the fault is located in, so that cable faults are never reclosed upon.

Condition (1) No Communication Channel

According to condition (1) the section identification method cannot utilize a communication channel. This is a challenge due to the fact that standard relay protective methods for transmission lines include line current differential protection and impedance/distance protection. Differential protection always requires a communication channel

while distance protection often does [15]. The method being introduced here is a solution that bypasses both of these relay protection designs that require the communications channel and depends upon the overcurrent and overvoltage threshold features of protective relays.

The solution is rooted in an important observation concerning the oscillation phenomena. This observation is that the voltage and current oscillations are complementary in terms of location. When comparing the voltage and the current signals that contain oscillations, the existence occurs exclusively on opposite ends of the overall DC line per type of signal – voltage on the sending end while current on the receiving end. For all DC L-G faults on the OH line, the oscillation exists in the voltage only on the sending end (terminal *A*), while the oscillation simultaneously exists in the current only on the receiving end (terminal *B*). This observation is consistent with Figure 52 (receiving end measurement) and Figure 53 (sending end measurement) from the previous section. In these figures, the current signal *H* and the voltage signal *S* contain oscillations consistently on each specific end of the HVDC line. The voltages and currents along the positive DC terminal (case 3-1-407) shown in Figure 60 are also consistent with this complementary distinctive.

Thanks to this complementary nature of the oscillations in voltage and current measurements, there is no need for a communication channel between relays. There will be either a voltage or current oscillation detected by each relay on each corresponding end of the HVDC line. The overcurrent threshold that should be set for each terminal *B* relay will individually detect the existence or absence of an oscillation post ACCB operation. The overvoltage threshold that should be set for each terminal *A* relay will likewise individually detect the existence or absence of an oscillation post ACCB operation. Reference Figure 55 again and note that the labels communicate the existence of one oscillating signal on each end of

the positive terminal of the line whether it be voltage or current. With protective relays on each end watching for an oscillation or the lack thereof, section identification should be achievable for all DC L-G faults. The placement of relays in the entire HVDC system should align with what is depicted in Figure 62. DC L-G faults will be detected whether or not they are on the positive or negative terminal of the DC line. Figure 62 also shows the appropriate zones of protection for the MMC-HVDC system associated with this work. These zones include Zone 12P and Zone 34N, the positive and negative terminals of the DC line protected by relays 1 through 4; Zone 136A and Zone 247B, the converter stations on terminals *A* and *B*; Zone 56A and Zone 78B, the transformer differential relays on terminals *A* and *B*; and lastly Zone 5A and Zone 8B, corresponding to the extended grid on terminals *A* and *B*. In this work, only Zone 12P and Zone 34N are analyzed in terms of protection since they correspond to described DC protection research.

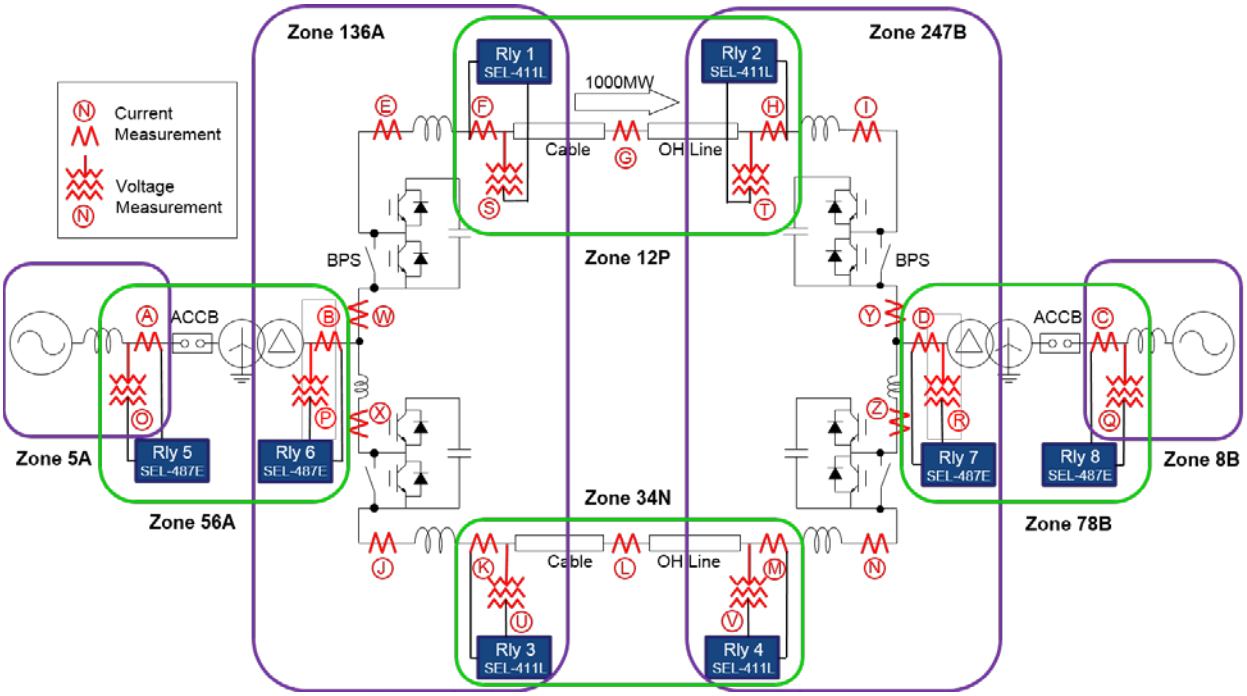

Figure 62: Placement of Protective Relays and Zones of Protection

The overcurrent threshold of each terminal *B* transmission relay should be set at a level that will be passed during any oscillation event. The overvoltage threshold of each terminal *A* relay should be set likewise. These threshold magnitudes require extensive investigation of many fault case scenarios to ensure reliable protection. Outside the scope of this work, the determination of these relay thresholds requires an in-depth sensitivity analysis to be performed. Oscillations caused by L-G faults closer to the junction of cable and OH line will cause oscillations of lower magnitude than L-G faults located at the sending or receiving ends of the entire line. A sensitivity analysis will ensure that the thresholds set will be passed for oscillations located at any point along the line. This remains an item of future work.

An important detail to note is that the relay thresholds will only be actively detecting overvoltages and overcurrents specifically after the circuit breakers have already isolated the fault. This section identification method is a part of the restart sequence for the purpose of deciding whether or not to reclose the circuit breakers. These relay thresholds will effectively detect whether or not the fault on the system is located in the OH line (oscillation detected) or in the cable (no oscillation detected). Relay 1 and relay 3 will send trip signals to the ACCB of terminal *A* while relay 2 and relay 4 will send trip signals to the ACCB of terminal *B*. There will be no need for a communication channel between terminals *A* and *B*. Condition three held to the proposed section identification protection method is satisfied.

5.1.2 Resolving Problematic L-L Faults within Method

Upon further analysis of the oscillation protection method, we found a problem where the so far described method would be unsuccessful in identifying the appropriate section. The problem arises when attempting to identify the location (section) of line-to-line (L-L) faults. Line-to-line

faults on the DC system do not generate oscillations, regardless of whether the fault is located on the OH line or the cable. The oscillations are characteristic of L-G faults. As demonstrated in example case 3-2-104 in Figure 63 (positive terminal) and Figure 64 (negative terminal), we find that oscillations do not exist in L-L cases where they do in L-G cases. What we do find is zero volts at all voltage measurements post ACCB operation, and we find varied currents depending upon the measurement location. Line-to-line faults on an MMC-HVDC system are expected to have extremely high current at or near the location of the fault. Figure 63 shows the positive terminal voltages and currents for a L-L OH line fault located at the middle point of the OH line. Figure 64 shows the negative terminal voltages and currents of the same case. There are no characteristic oscillations as there are for L-G faults on the OH line.

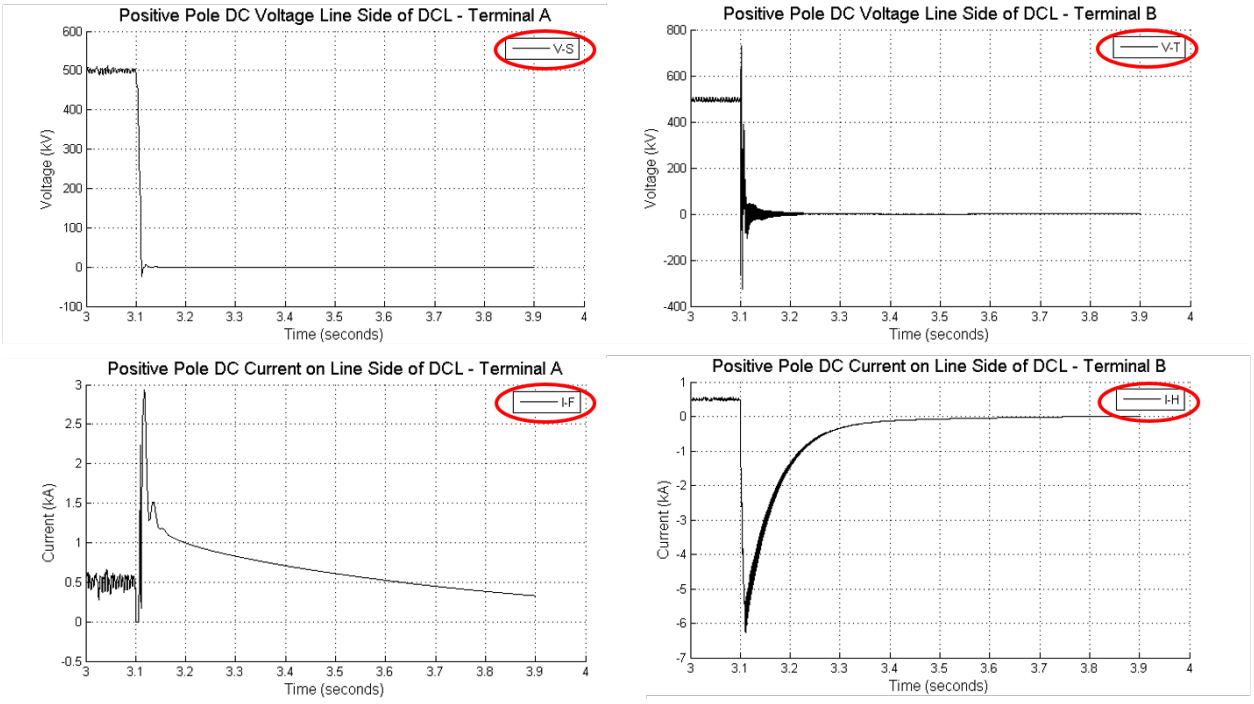

Figure 63: L-L DC Fault at the Midpoint of the OH Line – Positive Terminal Voltages and Currents Shown

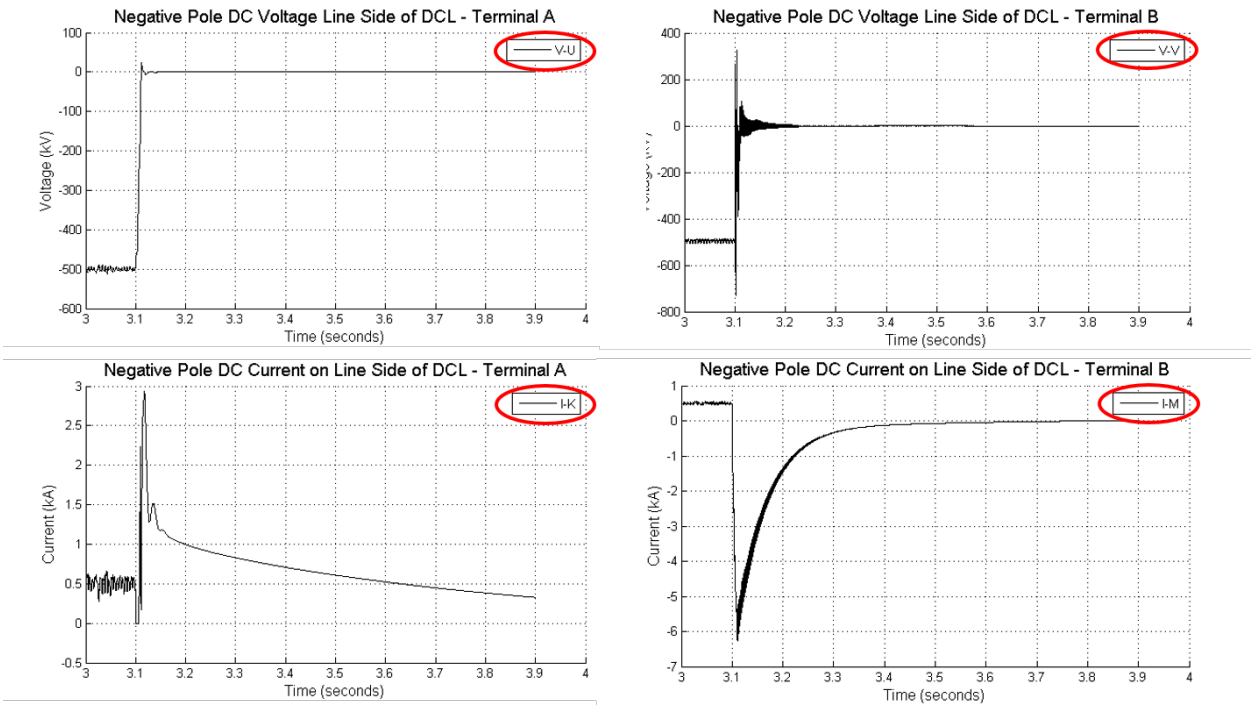

Figure 64: L-L DC Fault at the Midpoint of the OH Line – Negative Terminal Voltages and Currents Shown

We do not see the characteristic voltages and current oscillations, but what we do see is a current transient in measurement *H* (terminal *B*) with a peak current magnitude which is significantly larger compared to previous L-G current oscillations. This peak transient current also appears for L-L faults on the cable. Figure 65 shows the positive terminal voltages and currents for the L-L cable fault case 3-2-104 with the fault located at the sending end of the cable. Figure 66 shows the negative terminal voltages and currents of this same case. The peak transient current in this case appears in measurement *F* and *K* (terminal *A*). These are the measurements specifically measured in the relay closest to the L-L fault location. The reason the peak fault current is higher in case 3-2-104 is because the fault is located directly at the point of measurement, sending end of cable, while in the previous case the fault was located in the middle of the OH line.

Let us first analyze the results of the L-L fault on the OH line when applying the threshold infrastructure of the oscillation method. As seen in Figure 63 and Figure 64 the peak current will pass the oscillation current threshold on terminal *B* and consequently a reclose signal will be sent to the breakers on the terminal *B* side. It will function just as if there was current oscillation on terminal *B*. This action is as desired since it is an OH line fault. With no voltage oscillations on either end, terminal *A* will not send any reclose signals. Being an OH line fault the desired outcome is for both sides of the system to attempt to reclose. At this point of development of the section identification method, terminal *B* will reclose but terminal *A* will not. This is inconsistent with the desired outcomes of a section identification protection method.

Now let us look at the next case and analyze the results of the L-L fault on the cable when applying the threshold infrastructure of the oscillation method. As seen in Figure 65 and Figure 66 the peak current will not pass an oscillation threshold since there is only an oscillation threshold on terminal *B*. There will be no reclose signal sent to the breakers on the terminal *A* side. This action is desired since the L-L fault is in the cable. We do not want to reclose. The current magnitudes on terminal *B* will not pass the oscillation current threshold, because the oscillation threshold will be set around 1 kA. The currents on terminal *B* after 3.167 seconds (when the ACCB operates) are lower than the thresholds will be set. With no voltage on either end of the system after the ACCB operation, there will be no reclose attempt on terminal *B* since the oscillation voltage threshold was not passed. For cable faults, L-G or L-L, the oscillation detection method will succeed in not reclosing

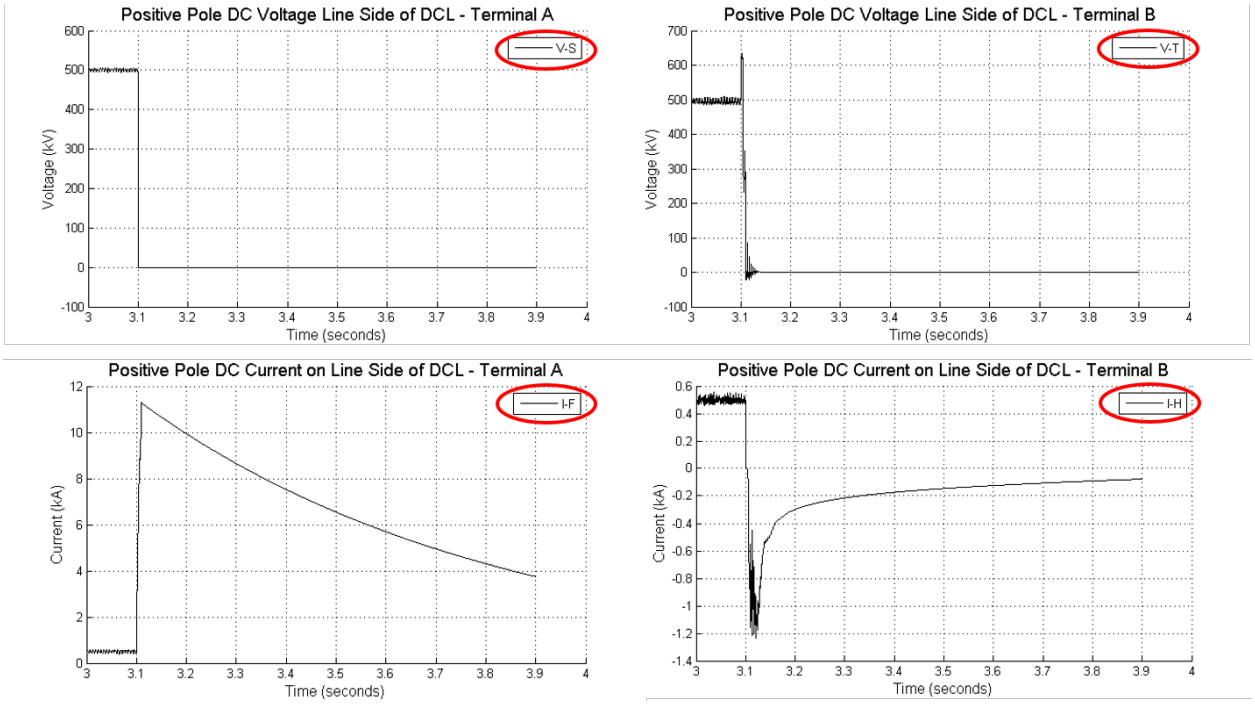

Figure 65: Case 3-2-104 L-L DC fault at the Sending End of the Cable – Positive Terminal Voltages and Currents Shown

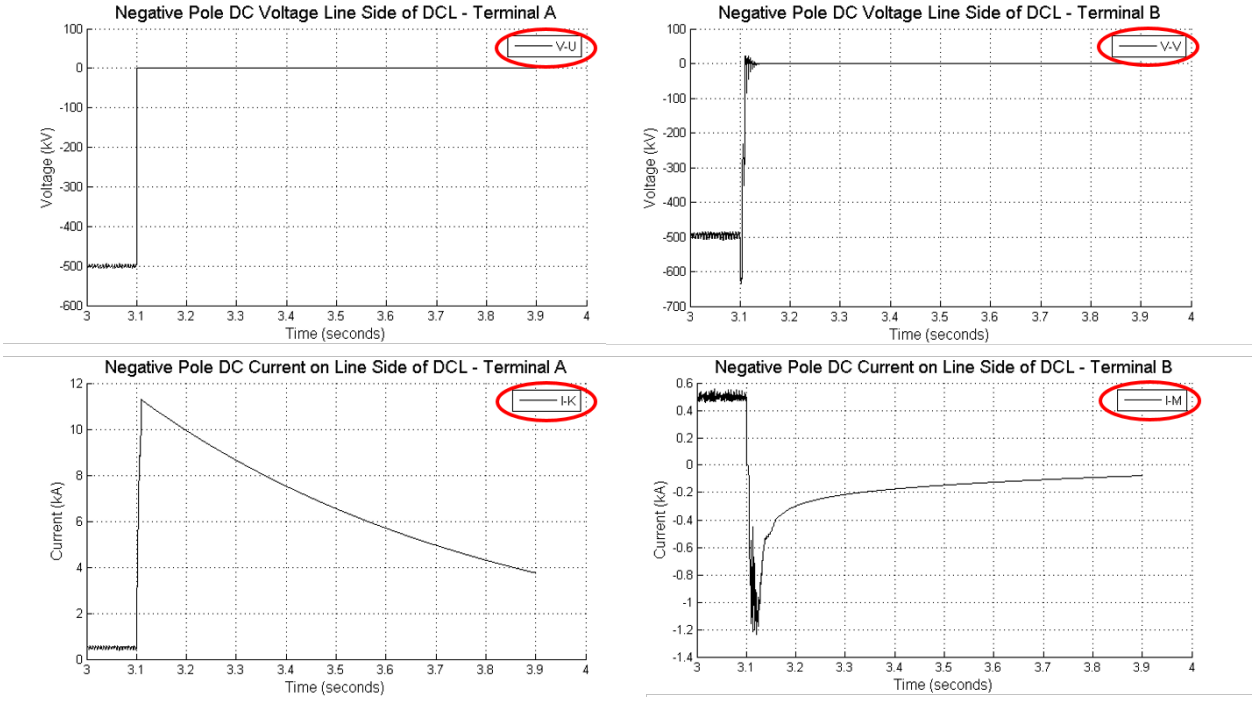

Figure 66: Case 3-2-104 L-L DC fault at the Sending End of the Cable – Negative Terminal Voltages and Currents Shown

Upon analysis of these two cases it is apparent that the one case is not responding according to appropriate section identification. Ultimately there is a challenge in being able to identify whether an OH line L-L fault is in the OH line or in the cable. The oscillation method that has been established so far needs to be modified in order to account for OH line L-L fault cases accurately. One modifications to the method design is bulleted below. This is the solution to making the OH line DC L-L fault cases a consistent addition to the original oscillation method of section identification. This modification is the respective solution to the OH line L-L fault case.

- Second (different time frame) voltage threshold on terminal *A* relay(s) in order to detect a voltage build up as a natural means of communication that does not require a communications channel

In the case of a L-L OH line fault, terminal *B* will be signaled to reclose as described before and is the appropriate action for an OH line fault. The challenge for this case is to have terminal *A* reclose as well for the OH line fault, without using a communication channel. A useful observation is that when terminal *A* has been reclosed by simply following the initial oscillation threshold method, there will be voltage building up on the HVDC line – assuming that the fault was not permanent, and a successful reclose resulted. If the fault is permanent, the breakers will not reclose successfully, and voltage will remain at zero. Upon a successful reclose after a non-permanent fault, the proposed solution is to add a voltage detection threshold on the terminal *A* relay(s) (only one relay with this second voltage threshold is necessary since only one relay is needed to send a reclose signal, but redundancy of both would only ensure higher reliability). Immediately after the initial oscillation voltage threshold at terminal *A* has stopped sensing for its defined oscillation time frame (roughly 150 ms), this second voltage threshold would begin sensing for voltage at a low threshold magnitude. This would allow for terminal *A* to know if terminal *B* has independently reclosed. If there was a successful reclose at terminal *B*

of a non-permanent fault then terminal *A* detects the voltage build up and also attempts to reclose. If it was a permanent fault and voltage remains at zero then terminal *A* correctly stays with its original conclusion to not reclose.

The entirety of the proposed section identification method has now been presented with the appropriate modification to resolve the discrepancy of not being able to differentiate OH line L-L fault location. A critical step in clearly presenting this section identification method is to depict the steps of logic that have been made in the form of a flow chart. Figure 67 and Figure 68 serve the purpose of summarizing the section identification method being proposed. The flow chart in Figure 67 is corresponds to terminal *A* relays while the flow chart in Figure 68 corresponds to terminal *B* relays. When each local relay follows its corresponding flow chart, the section identification protection reclosing method will be executed accurately. For clarification each flow chart per terminal is a decision tree that must be followed by each relay on the HVDC line per corresponding relay location – terminal *A* or *B*.

Following the terminal *A* flow chart in Figure 67, the first evaluation is whether or not the ACCB has been tripped (opened), isolating the DC fault. Once the ACCB has been tripped, each terminal *A* relay evaluates for a set time period (*t1*) whether or not the preset voltage threshold (*Thr_V*) is passed or not. If yes, then the fault is undoubtedly an overhead line fault and ACCB reclose is activated by either terminal *A* relay, the positive or negative pole relay. If no, then the relay must decide whether or not the fault is a L-L overhead line fault. This evaluation was previously described. If so then reclose can be performed. But if not then the fault is undoubtedly a cable fault and ACCB reclose is not desired due to the likelihood of a cable fault being permanent. When *Thr_V* is not passed, deciding whether the fault is L-L OH line or cable is determined by the method modification previously introduced – the terminal *A* voltage

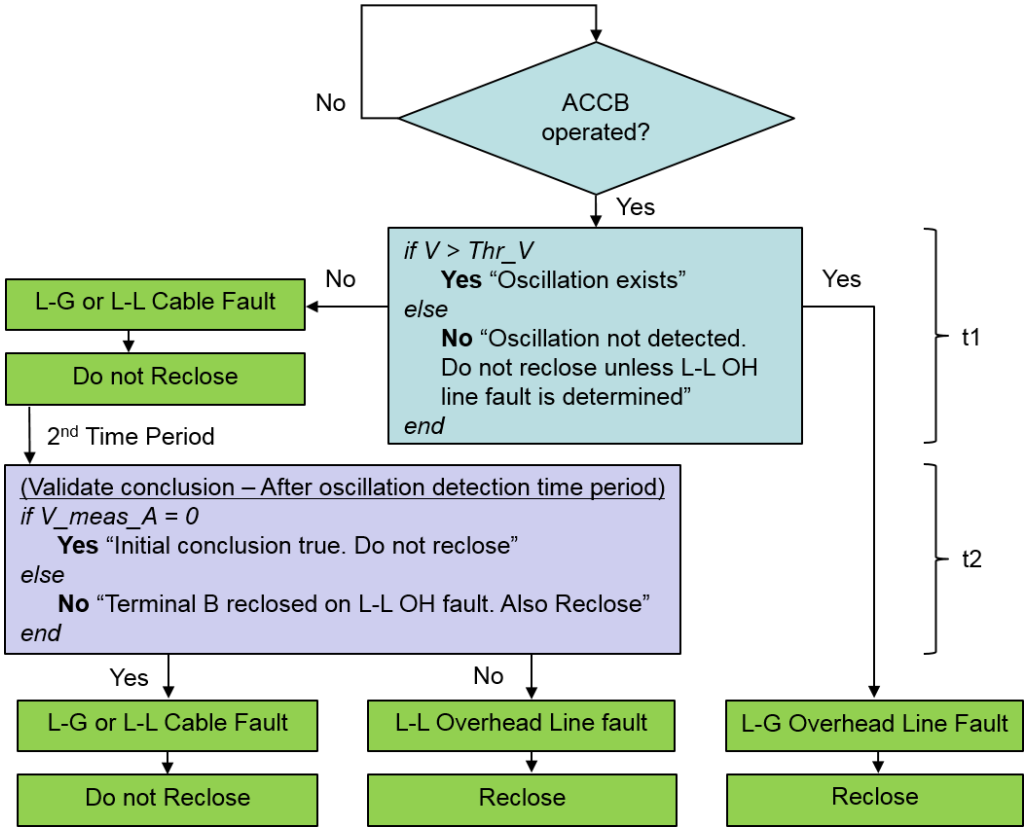

Figure 67: Terminal *A* Relay Flow Chart for the Section Identification Protection Reclosing Scheme

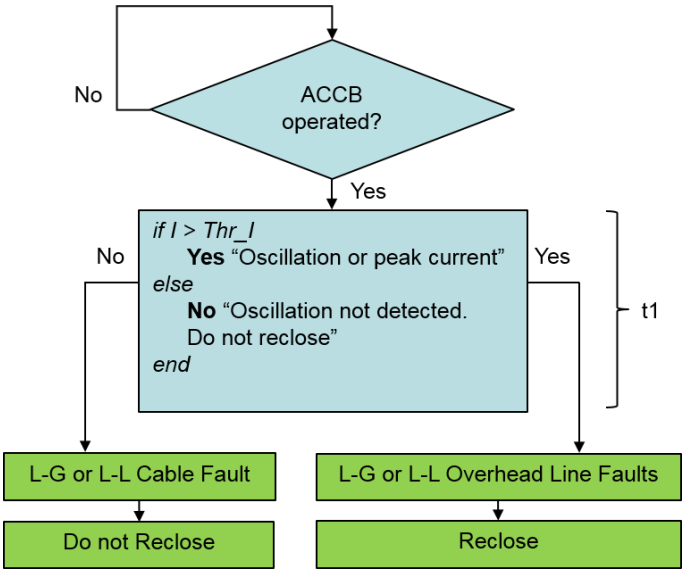

Figure 68: Terminal *B* Relay Flow Chart for the Section Identification Protection Reclosing Scheme

threshold measurement that detects whether or not terminal *B* has reclosed. This voltage threshold measurement is notated as *V_meas_A* on the flow chart. On the flow chart, this voltage measurement is clearly depicted as occurring during a second time period (*t2*). This second time period is critical, because during *t1* the voltage oscillation is sensed and then during t2, immediately after *t1*, *V_meas_A* as natural means of communication senses for a terminal *B* reclose. The duration of the first time period, *t1*, should be approximately 150 ms or more based off of observation of the oscillation signals in the previous figures, Figure 52 and Figure 53. The duration of the second time period, *t2*, can be set to start after terminal *B* has had time to determine a successful reclose or not, and only need continue for as long as is necessary to detect voltage build up on the DC line. If voltage is sensed by *V_meas_A* during *t2*, terminal *A* has successfully reclosed, and the restart sequence will also be activated at terminal *A*. With this result it can be concluded that a L-L fault occurred on the OH line. If voltage is not sensed by the *V_meas_A* threshold during *t2*, terminal *A* did not reclose, and the restart sequence will not be activated at terminal *A*. With this result it can be concluded that either a L-L or L-G cable fault occurred.

Following the terminal *B* flow chart in Figure 68, the first evaluation again is whether or not the ACCB has been tripped, isolating the DC fault. Once the ACCB has been tripped, each terminal *B* relay evaluates for the set time period (*t1*) whether or not the preset current threshold (*Thr_I*) is passed or not. If yes, either a L-G fault oscillation or a L-L fault peak transient current was detected in the OH line, and the restart sequence is started by sending a ACCB reclose signal. If no, either a L-G or L-L fault occurred on the cable resulting with no passing of the *Thr_I* relay threshold. Being a cable fault in this case, the fault is assumed to be permanent and

no circuit breaker reclose is attempted. In total, these two flow charts account for all fault case scenarios resulting with the desired restart action based upon the fault section location.

The next few figures are for the purpose of depicting the protective relay overvoltage and overcurrent thresholds to be set for the section identification method. These plots provide validation of the method. Figure 69 shows an example depiction of a relay voltage threshold being passed during a L-G fault located on the receiving end of the OH line.

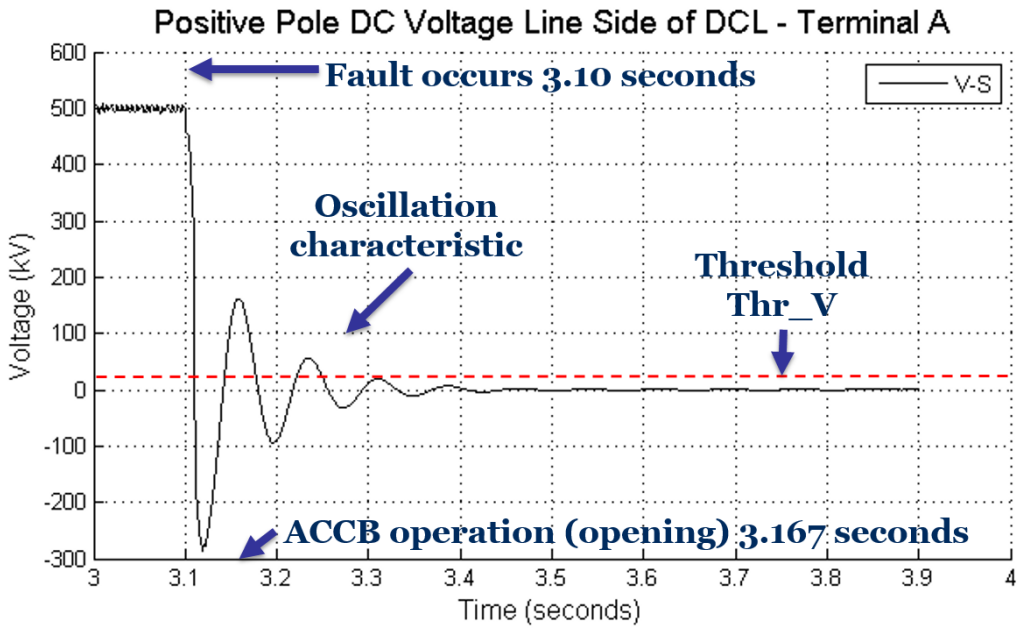

Figure 69: Protective Relay Voltage Threshold applied to a Terminal *A* Relay during a L-G Fault on the Receiving End of the OH Line (Case 3-1-407)

Figure 70 shows a relay voltage threshold being passed during a L-G fault located in the middle of the OH line. As would be expected, the magnitude of this oscillation is lower than the fault located on the receiving end of the OH line - Figure 69. This is due to the fact that the relay measurement is farther from the fault location. The closer the measurement is to the fault

location, the higher the oscillation magnitude. Note that the threshold is set to be passed by both magnitudes.

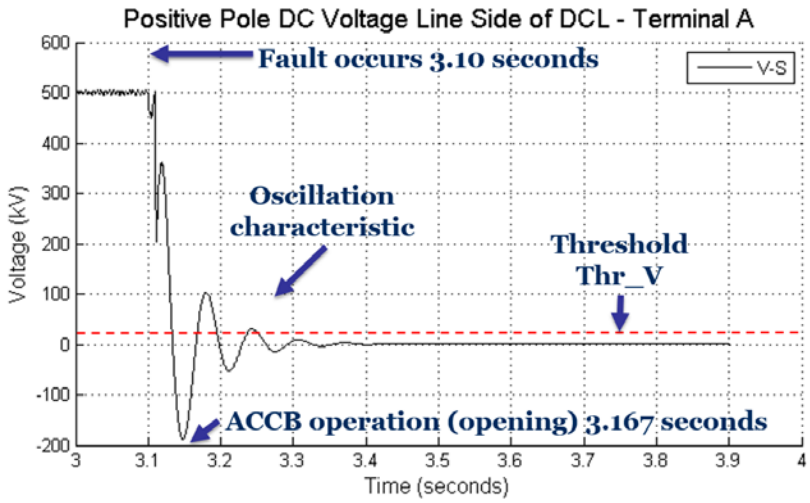

Figure 70: Protective Relay Voltage Threshold applied to a Terminal *A* Relay during a L-G Fault in the Middle of the OH Line

Figure 71 shows a relay current threshold being passed during a L-G fault located on the receiving end of the OH line. This figure as well as Figure 69 are associated with case 3-1-407.

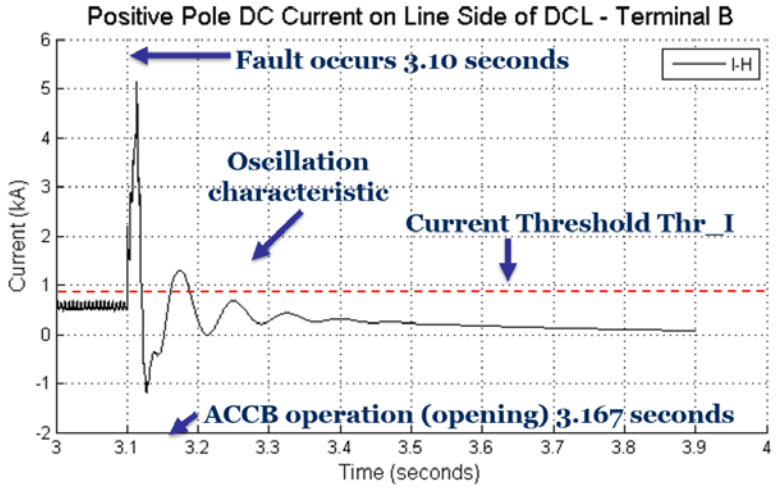

Figure 71: Protective Relay Current Threshold applied to a Terminal *B* Relay during a L-G Fault on the Receiving End of the OH Line (Case 3-1-407)

Figure 72 shows a relay current threshold being passed during a L-L fault located in the middle of the OH line. When comparing this figure with the previous, Figure 71, it is apparent that the same current threshold set on terminal *B* relays functions for both L-G and L-L fault cases in the OH line. One relay threshold is sufficient for detecting both L-G oscillations and L-L OH line peak currents, and both will successfully result with an attempt of reclose for the OH line fault cases.

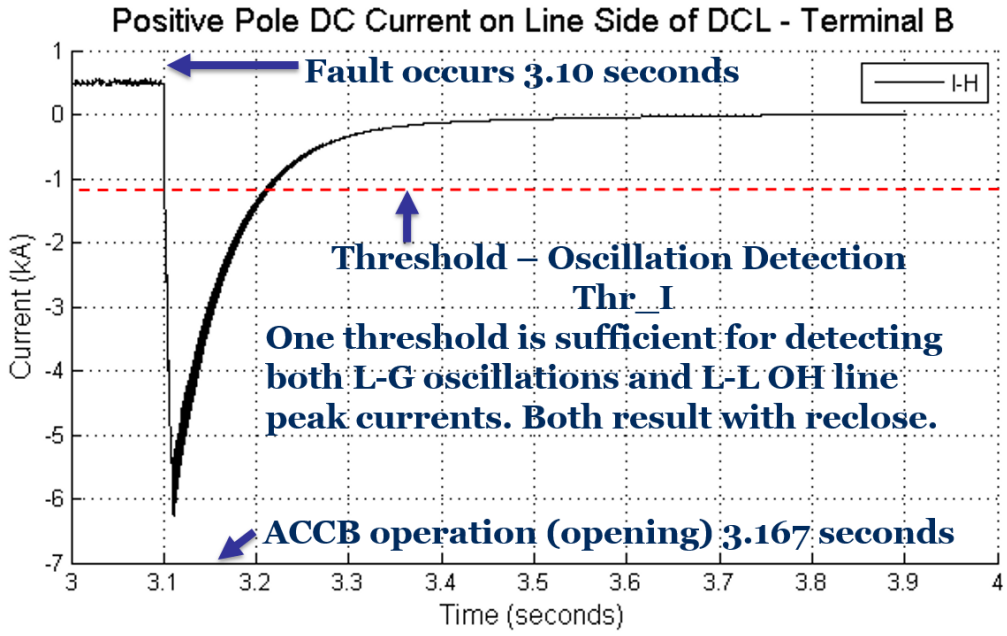

Figure 72: Protective Relay Current Threshold applied to a Terminal *B* Relay during a L-L Fault in the Middle of the OH Line

These figures, Figure 69 through Figure 72, are provided as the cases that will pass the set threshold values as desired and will activate a reclosing sequence, sending an ACCB trip signal.

Table 16 shown below clarifies the coordination of the relays on the DC portion of the system. For the purpose of this table we have defined a relay active operation as a relay that has

sent a trip signal to reclose the breakers. The purpose of this table is simply to further clarify the resulting actions taken based off of the section identification method being proposed.

Table 16: Relay Coordination Table for the DC System relating to Section Identification

Fault No.	Fault Location	Fault Type	Terminal *A* Operations	Terminal *B* Operations
7	DC System Sending End - Positive Terminal	LG	No Oscillation - No Operation	No Oscillation - No Operation
9	DC System Sending End - Negative Terminal	LG	No Oscillation - No Operation	No Oscillation - No Operation
10	DC Cable Sending End - Positive Terminal	LG	No Oscillation - No Operation	No Oscillation - No Operation
11	DC Cable Sending End - Negative Terminal	LG	No Oscillation - No Operation	No Oscillation - No Operation
12	DC Cable Sending End	LL	Rly 1, Rly 3 (Current)	Rly 2, Rly 4 (Voltage build)
7'	DC System Receiving End - Positive Terminals	LG	Rly 1 (Voltage)	Rly 2 (Current)
9'	DC System Receiving End - Negative Terminal	LG	Rly 3 (Voltage)	Rly 4 (Current)

Condition (2) Sampling Rate 175us, and Condition (3) Limit of 3 Past Sampling Points

It is important to quickly reference the other two conditions placed upon the proposed section identification method. The second condition requires that the method functions with a sampling rate of 175 us. When analyzing the oscillations upon which this method depends, a sampling rate of 175 us is definitely sufficient for the relays to detect any oscillation over a set current or voltage threshold. Reference Figure 52 and Figure 53 for confirmation. As for the third condition overcurrent and overvoltage relay functions do not have any need for past sampling points as do other relay protection features. Therefore the proposed method of section identification satisfies the third condition. Condition 2 and condition 3 are both met by the proposed section identification method.

5.2 PROTECTIVE RELAY CONSIDERATIONS

Protective relay technology uses a current transformer or voltage transformer (CT or VT) to use a proportional system current or voltage signal respectively to evaluate what is occurring on the protected system and act accordingly with logic analysis on said signals. The simple logic for overcurrent and overvoltage relay functionality is described previously in this work. There are primarily three functional protective relay systems: 1) line current differential protection, 2) impedance/distance relay protection, and 3) overcurrent/overvoltage relay protection [30]. Line current differential protection is commonly implemented in transmission protection, but this protection cannot be performed without a communication channel [15]. In perspective of the proposed protection method, line current differential protection is not applicable for the reason of desiring to not use a communication channel as discussed earlier in this chapter. Distance relay protection is potentially applicable for a protection method, but is more applicable to a situation where an exact location identification is desired. For the protection method being proposed, we are interested simply in section identification and as quickly as possible. Exact fault location identification is unnecessary until a permanent fault is determined, upon which a utility repair crew would be dispatched for construction. This stage of system protection is outside the scope of this work.

Distance relay protection could have potentially been used for the section identification application but an exact distance location is unnecessary for the proposed section identification protection method and more importantly slower than simple overcurrent and overvoltage protection. The speed comparison between the three described relay functions depends upon the application. For the section identification application of this work, overcurrent and overvoltage methods are faster than distance relay protection for the reason of calculation time for exact

distance determination. Therefore with this knowledge while designing the fault section identification method, overcurrent and overvoltage protection was chosen as preferable for the given design and has been incorporated into the method coupled with the finding of the characteristic oscillation signal – unique to this exact HVDC system design.

There are multiple relays readily available from Schweitzer Engineering Laboratories that can be used to implement the methodology presented into the proposed HVDC protection design. Schweitzer Engineering Laboratories (SEL) dominate the U.S. market for protective relays. Figure 73 is a picture of the SEL 411L which is a relay selected specifically because of its features for the fault section identification protection method.

Figure 73: Protective Relay (SEL 411L) Advanced Line Differential Protection, Automation, and Control System [31]

There are multiple transmission relays offered by SEL that have overvoltage and overcurrent protection, but this new SEL relay is the only one that has traveling wave location identification capability. This feature is desirable for finding the exact location of a permanent fault so that a utility crew can be dispatched time-efficiently to repair transmission. While distance relay functionality can perform this function as previously mentioned, the SEL 411L with traveling

wave location identification capability can locate permanent faults from each terminal separately without the need for a communications channel [31]. Additionally the traveling wave feature can locate the permanent fault faster than distance relays as well as determine the location with more exact precision than distance relays. This SEL relay is merely an example of a readily available protective relay that can aid the implementation of the proposed fault section identification protection method.

5.3 CONCLUSION

The content of this section is the proposed method of section identification for the protective restart sequence of the described MMC-HVDC system being analyzed. Utilization of the oscillation characteristic found unique to this system is a desirable option due to forming a section identification method capable of functioning without a communication channel as well as satisfying the other set conditions mentioned. The conditions are met and the method accounts for all fault types and fault section, resulting with the desired restart action per fault type and location.

6.0 CONCLUSION

In summary, this work presents an HVDC design and evaluates the protection needs of this HVDC design. A detailed model of this HVDC system design is validated and presented. A parametric trends analysis is presented to meet the purpose of selecting appropriate parameters for a protection analysis. A fault protection analysis was performed, and lastly a fault section identification protection method has been proposed that successfully meets the desired design requirements.

The proposed fault section identification method incorporates conventional overcurrent and overvoltage relay protection. This conventional method of protection has limitations specifically when applied to complex networks [19]. Determining what the cause of an overcurrent or overvoltage becomes near impossible with considerably complex power system networks, and consequently making protection decisions of act or restrain becomes impossibly difficult. Since HVDC transmission is truly a simple network or two terminals, the limitations of this conventional protection hardly apply. The simple and robust conventional protection can be implemented as has been done in the method proposal without confusion of fault events.

Additionally, a benefit of implementing conventional overcurrent and overvoltage protection is that the set design condition of minimizing the memory samples of relay protection has been minimized to none. Overcurrent and Overvoltage protection does not require past samples to make current decisions. The system is memory-less. This requires the least amount of

time that a relay protection decision can be made for an overcurrent or overvoltage function. The condition of no communications channel was also successfully achieved with the proposed protection method. This ensures that the protection method is that much faster without any communications delay, making appropriate protection decisions local to each terminal independently.

The proposed protection method accounts for all faults on the DC side of an MMC-HVDC system specifically for a design including both overhead (OH) line and cable sections making up the overall HVDC line. Each DC side fault is identified to be in the cable or in the OH line section and the corresponding restart sequence decision is appropriately made, without any need for communication between relays at each end of the HVDC transmission line.

With the implementation of the method, a reclose will be attempted for any DC side fault that is potentially non-permanent, and consequently a restart to normal operation is achieved as frequently as possible and as quickly as possible. With this fault section identification protection method, the MMC-HVDC technology is further equipped so that its benefits might be utilized on the power grid. The method successfully meets the motivation of enhancing reliability of power delivery.

Ultimately the contribution of this work is to equip future installations and product lines of MMC-HVDC technology. This work is one more step in supporting the implementation of the beneficial technology. Specific contributions from this work include the trends of MMC-HVDC component sensitivity analysis, awareness of how an MMC-HVDC system responds to a comprehensive list of faults, and a protection coordination scheme uniquely applicable to this promising HVDC system design. There is also considerable significance in the contribution of a fault section identification method incorporated into relay coordination without using a

communication channel and without the use of DC circuit breakers. This contribution is ultimately the speed in which the system is restarted after a fault scenario.

6.1 FUTURE WORK

This thesis does in fact stand on its own in addressing MMC-HVDC system restart protection, and yet there is still more work to be done. Another challenge in addressing MMC-HVDC protection is the existence of circulating currents in the MMC topology during line-to-line faults on the DC side. These high currents endanger the elemental devices of the MMC, namely the freewheeling diodes (FWD) and the bypass switches (BPS). The DC line-to-line fault creates a circuit path with these converter devices in the initial stages of fault protection sequence. This protection sequence was presented earlier, in Table 13. The first protection layer is gate blocking, where the IGBTs all turn off. The FWDs still allow for a circulating path with the line-to-line fault. The second protection layer is the bypass switch (BPS), which is in parallel to each submodule for the purpose of protecting the FWDs from the fault current magnitudes. Bypass switches are typically a press packed thyristor which can handle higher currents. With either the FWDs or BPSs in the circuit, a circulating current path is formed with the DC line-to-line fault as shown in Figure 74. For clarity only phase C depicts the current path in this figure, but in reality all phases have the same circulating current path caused by the DC line-to-line fault.

A nonpermanent fault should be cleared quickly in order to restart power transmission as soon as possible. During the DC line-to-line fault on the MMC, the freewheeling diodes (FWD) inherent to the design undesirably function as uncontrolled rectifier bridges allowing a DC fault current to feed the fault (reference Figure 74). During a non-permanent fault there is enough time

for the fault currents to reach a current stress level that will damage the converter's freewheeling diodes [6], [11]. Also, for any application of generation or load on the DC-link, there will be a great need for fault tolerance even beyond the need of protection for converter elements. Ultimately to resolve this problem there is need for a protection method that will suppress or eliminate the circulating currents within a MMC of half bridge submodule topology. With these circulating currents suppressed quickly, the system will be able to return to normal operation through restart sequence that much more quickly.

One weakness of the MMC topology is the circulation of currents in a gate blocking protection scenario [6], [11]. For the half bridge topology of MMC in particular, circulating currents cannot be easily eliminated during a gate blocking attempt [6], [11]. For other converter topologies the gate blocking protection method is a sufficient solution to protect against DC fault scenarios [11]. For example, this is possible with a full-bridge submodule technology, but the half bridge submodule topology is desirable over the full-bridge because the losses are significantly lower [1].

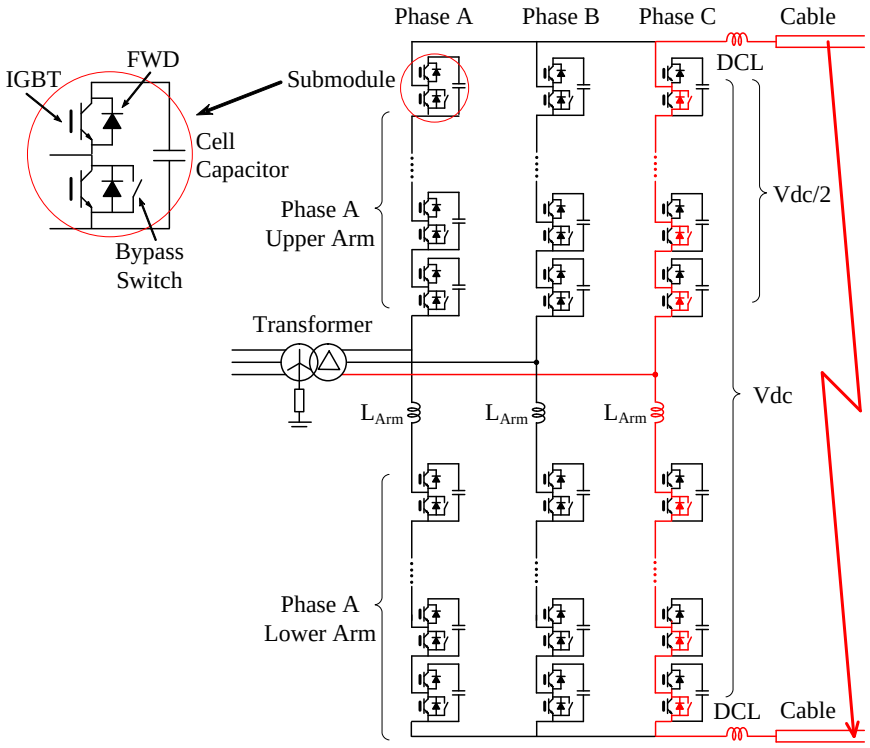

Figure 74: Circulating Current Path Depicted in the Modular Multilevel Converter Topology, Caused by the DC Line-to-Line Fault

The simple solution is to switch resistance somewhere into the circuit to more quickly burn off the circulating current. This is a low hanging fruit solution and is limited by the tradeoff of its effectiveness with the cost. A piece of future work is to design a novel solution to quickly dissipate these slowly decaying circulating fault currents, ultimately for the purpose of protecting the devices of the modular multilevel converter. Conceptual solutions to this problem are currently being proven in simulation and hardware. Expect publications in the near future regarding this topic.

APPENDIX A

PSCAD FREQUENCY DEPENDENT CABLE MODEL OUTPUT DATA

The data provided below corresponds to the PSCAD cable output file in support of proving out the existence of the oscillation frequency characteristic signal discussed at the end of chapter 4.

==========

PSCAD LINE CONSTANTS PROGRAM OUTPUT FILE (*.out)

==========

Display Format: M, N denotes a complex number M + jN

PHASE DOMAIN DATA @ 0.10 Hz:

SERIES IMPEDANCE MATRIX (Z) [**ohms/m**]:
0.622315286E-05, **0.636274522E-05** 0.488890843E-06, 0.625672289E-05
0.488890843E-06, 0.625672289E-05 0.132929884E-03, 0.625497291E-05

SHUNT ADMITTANCE MATRIX (Y) [**mhos/m**]:
0.000000000E+00, **0.157065724E-09** 0.000000000E+00, -.157065724E-09
0.000000000E+00, -.157065724E-09 0.000000000E+00, 0.421000382E-09

LONG-LINE CORRECTED SERIES IMPEDANCE MATRIX [**ohms**]:
0.311153888E+01, **0.318126632E+01** 0.239902977E+00, 0.312601541E+01
0.239902977E+00, 0.312601541E+01 0.664556912E+02, 0.328182224E+01

LONG-LINE CORRECTED SHUNT ADMITTANCE MATRIX [**mhos**]:
0.355076045E-07, **0.785328396E-04** -.927010493E-07, -.785327576E-04
-.927010493E-07, -.785327576E-04 0.246361594E-06, 0.210504409E-03

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