

**A TRANSFORMERLESS PCB BASED
MEDIUM-VOLTAGE MULTILEVEL POWER
CONVERTER WITH A DC CAPACITOR
BALANCING CIRCUIT AND ALGORITHM**

by

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University of Pittsburgh, 2015

This dissertation presents a new method of constructing a transformerless, voltage-sourced, medium-voltage multilevel converter using existing discrete power semiconductor devices and printed circuit board technology. While the approach is general, it is particularly well-suited for medium-voltage converters and motor-drives in the 4.16 kV, 500 - 1000 kW range. A novel way of visualizing the power stage topology is developed which allows simplified mechanical layouts while managing the commutation paths. Using so many discrete devices typically drives cost and complexity of the gate-drive system including its control and isolation; a gate-drive circuit is presented to address this problem. As with most multilevel topologies, the dc-link voltages must be balanced during operation. This is accomplished using an auxiliary circuit made up of the same power stage and an associated control algorithm. Experimental results are presented for a 4.16 kV, 746 kW, five-level power converter prototype. This dissertation also analyzes a new capacitor voltage-balancing converter along with a novel capacitor voltage balancing control algorithm. Analysis of the inverter system provides a new description of capacitor voltage stability as a function of system operating conditions.

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PREFACE

I would like to thank my wife Kristen, my son Miles, and my entire family for fully supporting me over this long journey. This work is dedicated to them. Next, I would like to thank Dr. Gregory Reed, Dr. Zhi-Hong Mao, Dr. Mahmoud El Nokali, Dr. Thomas McDermott, and Dr. William Clark for serving on my committee. A special thanks to Dr. Reed for providing me with invaluable guidance since we first met in 2008. I would like to thank Christopher Lee, Brian Venus, Dr. Shyam Ramamurthy, Dr. Nicholas Benavides, Dr. Daniel Opila, and everyone else at GE Power Conversion that made this research possible. Lastly, I would like to thank Dr. Alfred Permuy for serving as a mentor for me. His brilliant ideas and leadership will stay with me throughout my entire career.

1.0 INTRODUCTION

Medium-voltage motor-drives are a workhorse in the power electronics industry with revenues exceeding \$2.7 billion in 2012, of which applications at or below 3 MW make up 48% [5]. This market segment demands a cost effective, transformerless and bi-directional multilevel converter that minimizes dv/dt and common-mode voltage system stresses while continuing to meet high power quality requirements [6, 7].

Many multilevel converter topologies can be used without a transformer including the neutral-point-clamped (NPC) [8], active neutral-point-clamped (ANPC) [9], neutral-point-piloted (NPP) [10], capacitor-clamped [11], generalized multilevel inverter topology [12], and modular multilevel converter (MMC) [13, 14, 15, 16, 17, 18] topologies. Others topologies like the “cascaded multicell with separate dc sources” [19] use a multi-winding transformer and diode rectifier to maintain the dc voltage levels, with the drawbacks of unidirectional power flow and the transformer cost and size.

Most medium-voltage drives are constructed using packaged “semiconductor modules”. A semiconductor module is a device that contains more than one semiconductor die arranged in a common housing to achieve a specific voltage and current rating from the module [20]. Thus semiconductor module manufacturers address the challenges associated with networking multiple semiconductor devices rather than converter designers.

This dissertation presents a fundamentally different approach to constructing power converters in this medium-voltage, low power class: using the discrete semiconductor devices that comprise 70% of the power semiconductor market [21]. This dissertation uses Transistor Outline (TO) and Diode Outline (DO) 247 package discrete devices [22, 23] in conjunction with widespread printed-circuit board (PCB) technology to leverage economies of scale for significant cost reductions compared to converters built with semiconductor modules. It also

enables the use of standard automated PCB manufacturing and test techniques for the entire converter system. This level of manufacturing and inspection automation is traditionally not possible for converter systems comprised of semiconductor modules.

New developments in three areas enable the construction of converters of this type: the topology arrangement, gate-drive, and dc-link capacitor voltage balancing. The first contribution is a novel way of visualizing and arranging the power stage topology that allows for simplified mechanical layouts while minimizing the commutation loop inductances. This topology “unwrapping” technique enables the separation of a power stage into sub-circuits where all non-zero current commutation events are contained within the sub-circuit. These sub-circuits can then be physically separated to address practical converter design issues.

The gate-drive circuit requires a cost-effective isolation scheme for the large number of semiconductor devices and must be precisely synchronized to allow the use of series-connected devices. Typical methods for isolation use a costly isolated power supply and fiber optic connection for each device instance [24, 25]. Several methods are available for driving series connected devices include using gate side control include synchronization [26, 27] and active voltage control [24, 25, 28], but they are rather complex for large numbers of devices, especially when each device requires individual optical isolation. A magnetically-coupled, current-sourced gate-drive system [29] is presented that significantly reduces the cost and complexity of meeting both requirements.

Transformerless multilevel converter applications typically require a voltage balancing scheme because the instantaneous current distribution causes unequal charging and discharging among the dc-link capacitors. NPC, ANPC, NPP, and capacitor-clamped topologies with four or more levels all have a dc-link capacitor voltage imbalance problem due to unequal current flows in the dc-link capacitors for all desired operating points [11].

Balancing may be achieved by imposing a specific control scheme on all power stages common to the dc-link; however, this requires complex space-vector modulation (SVM) schemes or common-mode injection techniques and puts several operational constraints on the common dc-link power stages [2, 30, 31, 32, 33, 34]. Several active balancing circuits and algorithms have been proposed [1, 2, 3, 4, 35, 36, 37, 38]; however, none of the proposed balancing circuits make use of the same topology used in the converter power stage.

We present an active balancing circuit and algorithm to transfer charge between all dc-link capacitors and allow for a larger operational space for all common dc-link power stages [39]. This circuit is identical to the converter power stage, simplifying manufacturing, test, and maintenance. The balancing algorithm capability is studied in a three-phase induction motor-drive application and experimental results are presented for a 4.16 kV, 746 kW prototype in a back-to-back configuration.

1.1 DISSERTATION ORIGINAL CONTRIBUTIONS

There are several signification and original contributions in the field of power electronics presented in this dissertation. A topology unwrapping scheme for n -level, NPC, ANPC, and NPP topologies [40] is analyzed in Section 4 of this dissertation. The exploitation and supporting analysis of the topology unwrapping scheme to optimize both commutation loops and circuit layout, and to enable a capacitor balancing circuit made up of the same topology as the main power converter stage [39] are original contributions presented in this dissertation.

Another original contribution of this dissertation is a new capacitor balancing algorithm presented for a generalized n -level converter [39]. The control algorithm is presented as the combination of two independent finite state machines in Figure 7.3 and Figure 7.4 and analyzed in Section 7. The original algorithm is robust enough to require no knowledge of the motor drive system operating points. A new capacitor current deviation model based on the front-end and back-end bridge operational spaces is presented in Section 4.3.1 of this dissertation as an original contribution. A capacitor balancing circuit and algorithm capability model was developed through analysis and presented in Figure 8.1 as an original contribution of this dissertation. The original capacitor balancing circuit and algorithm set

points and parameters were processed using a sensitivity analysis to present an optimized circuit and algorithm design. The results of the sensitivity analysis conducted on the original capacitor balancing circuit and algorithm capability model to reveal an optimal capacitor balancing circuit design are presented in Section 8 of this dissertation and these results are additional original contributions of this dissertation.

Another significant contribution presented in this dissertation is an original gate-drive circuit [29]. This gate-drive circuit is analyzed against the requirements of gating large numbers of series connected devices while maintaining proper isolation. The topology unwrapping scheme, optimized balancing circuit and algorithm, and gate-drive circuit were successfully implemented on a PCB and demonstrated in a 746 kW, 4160 V prototype. The implementation and integration of components that include gate-drive isolation, balancing circuit optimization, and heat sink arrangement to support cooling requirements and electrical isolation to form a fully rated, medium-voltage transformerless multilevel motor drive system are original contributions of this dissertation. All of the original concepts presented in this dissertation are supported analytically through a thorough research of the current state-of-the-art presented in literature and proper treatment of the concepts as they are developed in this dissertation.

All original concepts individually and collectively as an original system are validation by the successful demonstration of all systems as they were integrated into a fully rated, fully operational prototype of which the experimental results are presented as original contributions in this dissertation.

Finally, the correction of a significant result published in [41] required for the original capacitor current deviation model is an original contribution of this dissertation.

2.0 VOLTAGE-SOURCED INVERTERS

For many years, the field of power electronics has seen a gradual technology shift from linear power supplies to switching converters for a wide range of applications due to their better efficiency and lighter weight. Power levels encountered in switching converters range from less than a watt in dc-dc converters within battery-operated portable equipment, to tens, hundreds, or thousands of watts in power supplies for everyday appliances, to tens and hundreds of megawatts in variable-speed rotating machine drives to thousands of megawatts in utility scale applications [42, 43, 44].

A voltage-sourced inverter (VSI) is a particular class of switching converters that modulates a dc voltage source, usually a capacitor or battery voltage, to produce an ac voltage source. Figure 2.1 illustrates several different inverters with different numbers of output voltage levels and ideal switches with multiple poles represent the action of the power semiconductor devices. Each of the three circuits shown in Figure 2.1 could represent a single phase of a multiphase inverter. Figure 2.2 illustrates a three-phase inverter comprised of two-level phase legs with phase-to-neutral and phase-to-phase voltage definitions. In practical VSI systems, different topologies of power semiconductor devices such as insulated-gate bipolar transistors (IGBT) or metal oxide semiconductor field-effect transistors (MOSFET) approximate and implement the ideal switches. Designers arrange these basic converter building blocks in various electric and magnetic topologies to create power conversion systems for common consumer, medical, and industrial systems of today.

Table 2.1 summarizes the achievable phase-to-neutral and phase-to-phase voltages for multiphase inverters with varying phase leg output voltage levels.

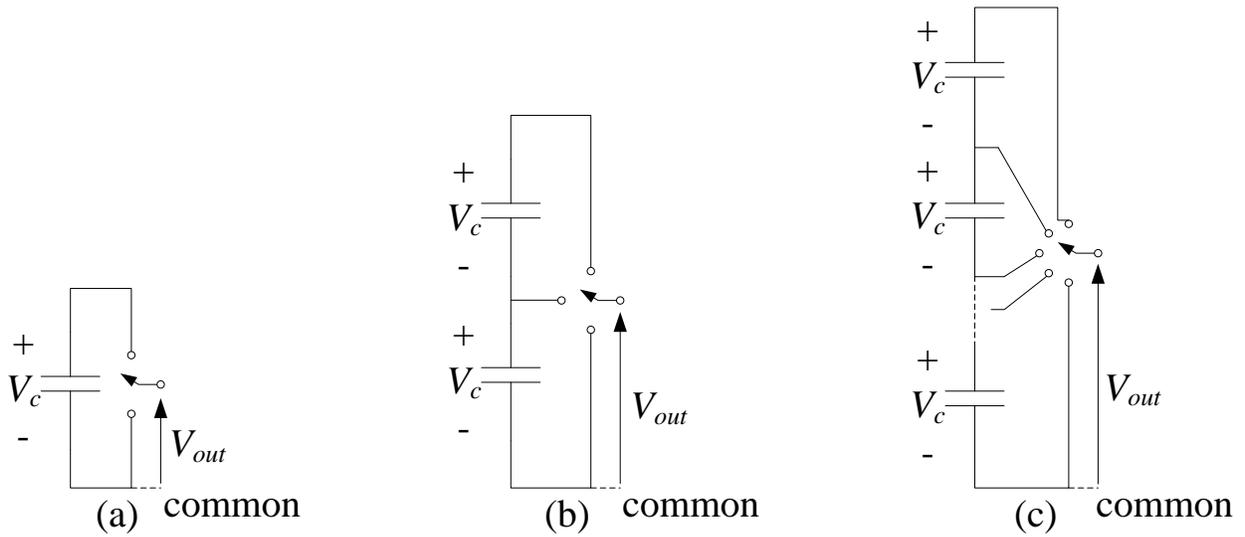


Figure 2.1: Ideal switch model of an inverter with (a) two, (b) three, and (c) n levels with respect to a common point

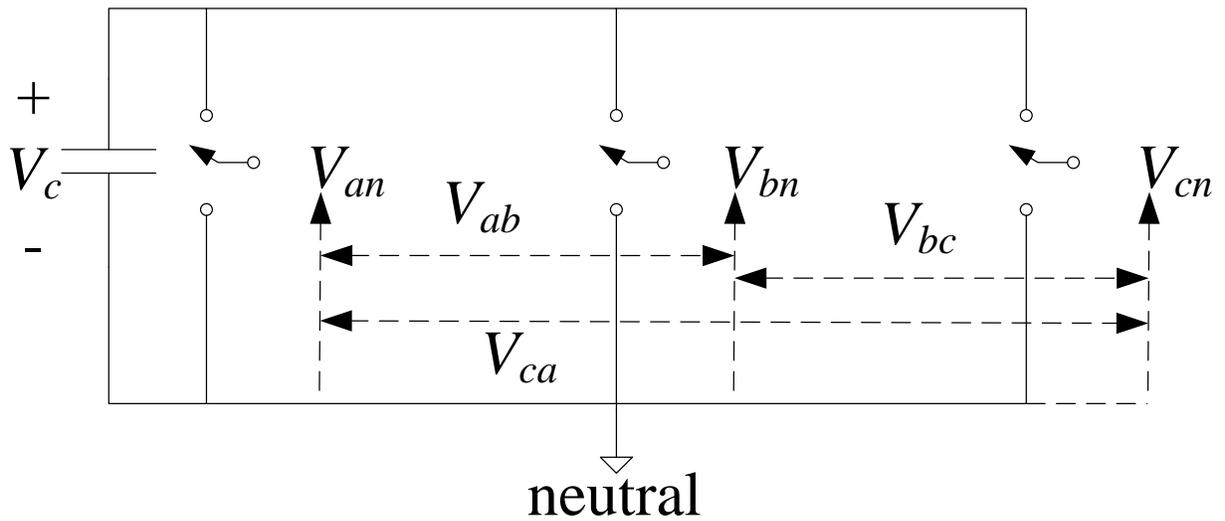


Figure 2.2: Ideal switch model of three-phase two-level inverter

Table 2.1: Inverter voltage combinations by the number of phase to neutral levels.

Number of Levels	$V_{phase-neutral}$	$V_{phase-phase}$
2	$0, V_c$	$-V_c, 0, V_c$
3	$0, V_c, 2V_c$	$-2V_c, -V_c, 0, V_c, 2V_c$
n	$0, V_c, 2V_c, \dots, nV_c$	$-nV_c, -(n-1)V_c, \dots, 0, \dots, (n-1)V_c, nV_c$

For an arbitrary number of phase-to-neutral voltages n , the number of phase-to-phase voltages k is

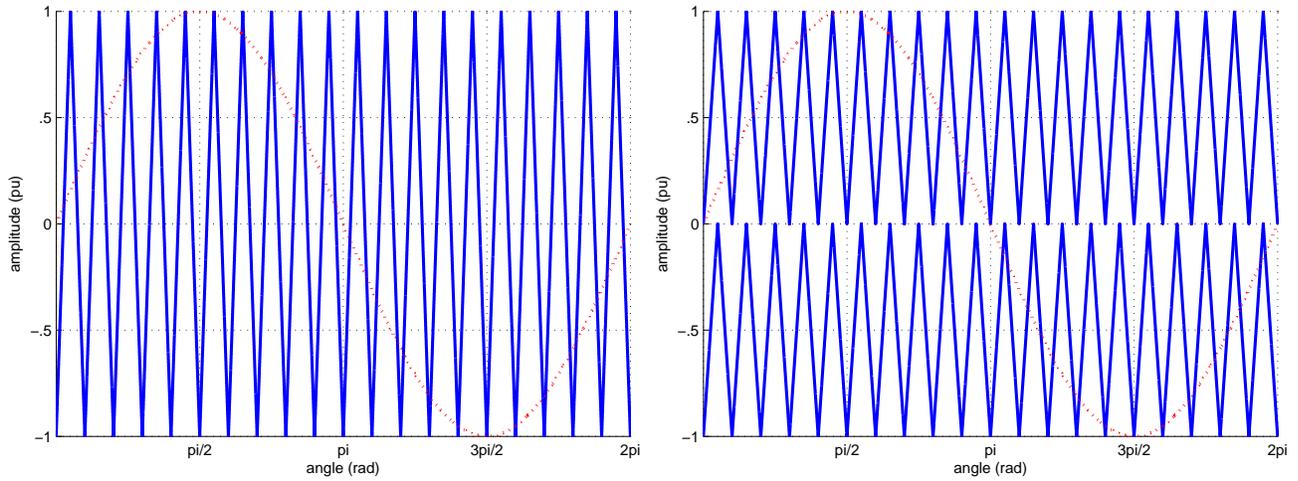
$$k = 2n - 1 \quad (2.1)$$

Several pulse width modulation (PWM) strategies with different design and performance implications exist for power converters [45]. For the purposes of introducing multilevel inverters in this dissertation, naturally sampled sine-triangle modulation is used unless otherwise noted. In VSI sine-triangle modulation, a sinusoidal reference waveform representing the desired output voltage is compared to a triangular carrier waveform. The triangular carrier waveform frequency is generally several times higher than the reference waveform. If the sinusoidal reference waveform is greater than the triangular carrier waveform, the corresponding converter switch is turned on and vice versa if the sinusoidal reference waveform is less than the triangular carrier waveform. Figure 2.3 illustrates sine-triangle modulator strategies for both a two-level and a three-level inverter.

Figure (2.4a) and Figure (2.4b) illustrate the phase-to-neutral output voltage of a single-phase leg of an inverter with two output voltage levels and the phase-to-phase output voltage of a three-phase inverter comprised of two-level phase legs respectively.

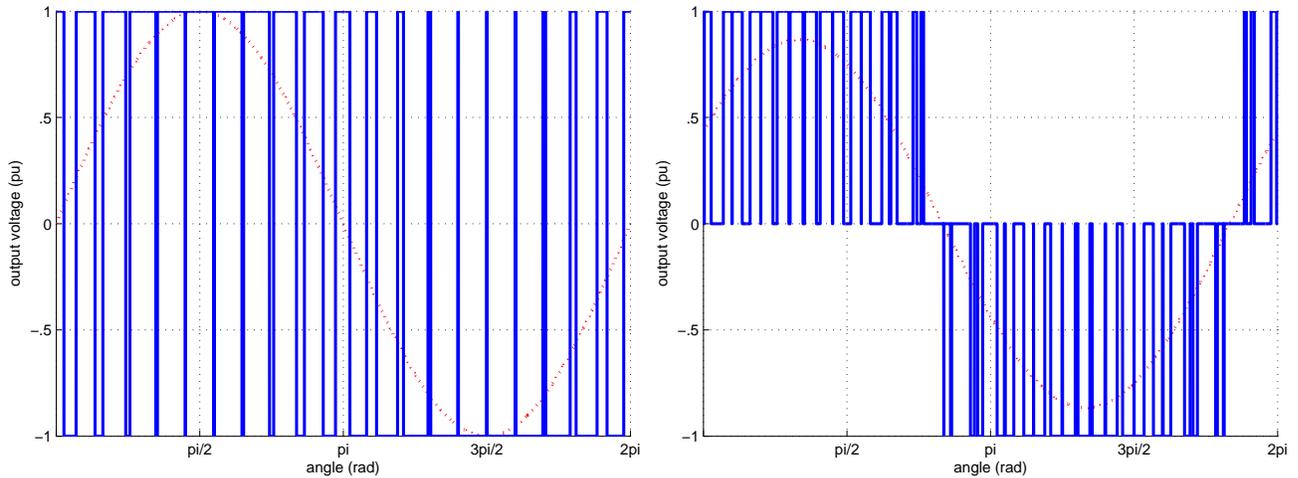
Figure 2.5 illustrates the phase-to-phase output voltage of a three-phase inverter comprised of two-level phase legs.

Figure 2.4 and Figure 2.5 depicted waveforms identify several simple but important concepts. First, as the number of levels of a single-phase leg increases, the unfiltered total



(a) Two-level sine-triangle modulation strategy. (b) Three-level sine-triangle modulation strategy.

Figure 2.3: Sinusoidal reference waveform and triangular carrier waveform for a two-level inverter (2.3a) and a three-level inverter (2.3b).



(a) Phase-neutral output voltage for an inverter with two levels. (b) Phase-to-phase output voltage between two phase legs of a three-phase inverter comprised of two-level inverter phase legs.

Figure 2.4: Phase to neutral output voltage (2.4a) and an phase-to-phase output voltage (2.4b) with all phase legs comprised of two-level inverters.

harmonic distortion (THD) of the output voltage waveform decreases. Output voltage THD is a critical power quality metric used throughout nearly all power electronic applications. Second, as the number of levels of a single-phase leg increases, the output voltage dv/dt decreases. Lower output voltage dv/dt is desirable for many reasons including EMI and voltage insulation system stress mitigation. Not observable from Figure 2.4 and Figure 2.5, common-mode (CM) voltage is another unwanted artifact of PWM VSI systems that is inversely proportional to the number of levels for a given inverter with a fixed control strategy [7]. The CM voltage or neutral point potential variation of PWM VSI exists due to non-zero neutral point current flow coupled with the zero sequence output voltage [46]. This CM voltage is detrimental to standard industrial electric motor drive systems [7]. Theoretically, an inverter with an infinite number of levels produces zero common-mode voltage [11].

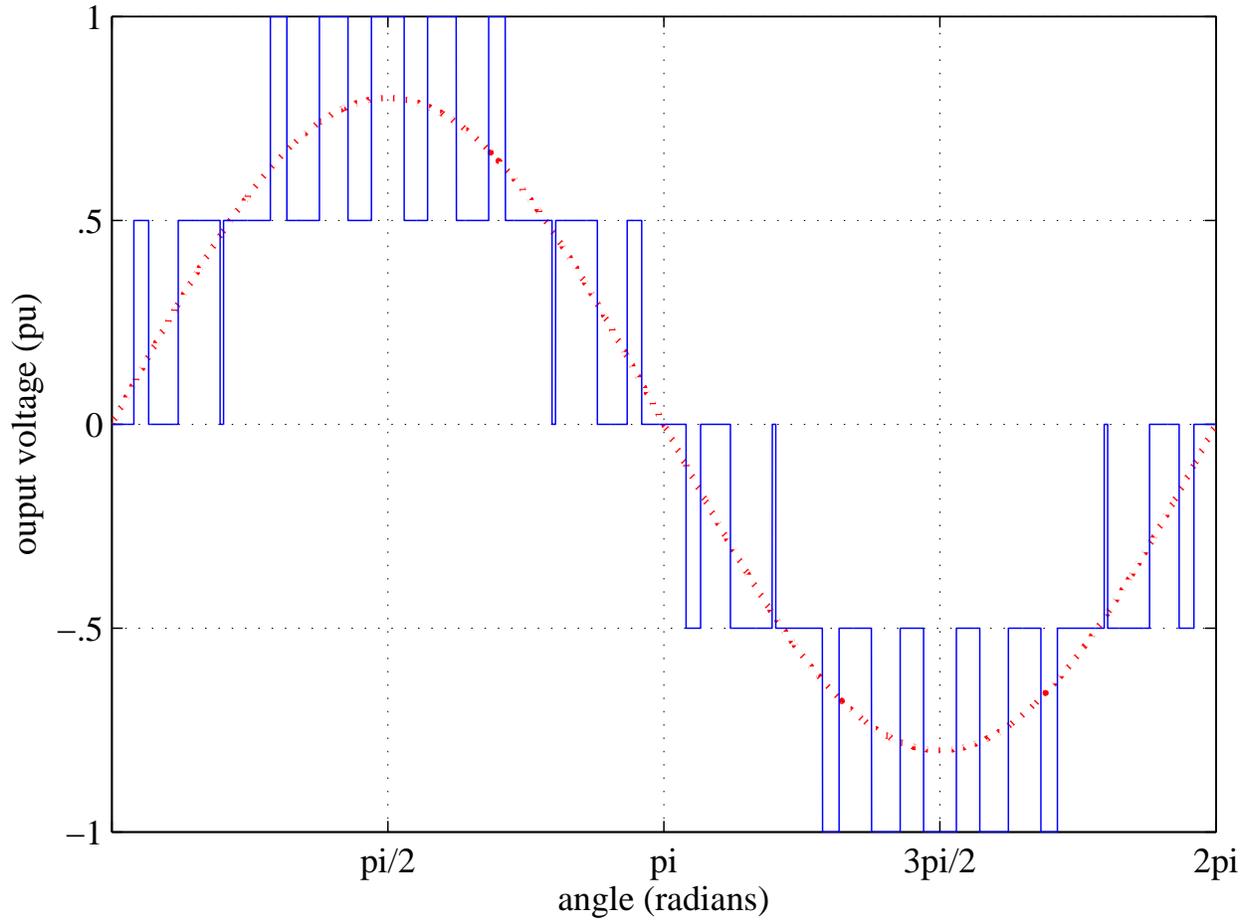


Figure 2.5: Phase-to-phase output voltage between two phase legs of a three-phase inverter comprise three-level inverter phase legs.

3.0 MULTILEVEL INVERTER TOPOLOGIES

Advances in semiconductor technology coupled with the increase in rigor of industrial electronic requirements have driven the need for higher voltage inverters [7] [11]. Medium-voltage high-power industrial applications increasingly use a specific class of inverters for dc-ac conversion known as multilevel inverters ($n = \text{number of levels} > 2$ [11]) due to their low output voltage total harmonic distortion (THD), low output voltage dv/dt , low CM voltage generation, and low input current THD [7]. The current technical literature proposes three major classes of multilevel inverter schemes: capacitor-clamped [7, 11]; cascade multi-cell [11] [47]; and diode-clamped [8]. Each class of multilevel inverter achieves multilevel output voltages by exploiting different electrical properties that are inherent to their electrical topology.

3.1 CAPACITOR-CLAMPED INVERTER

A three-phase, capacitor-clamped inverter is illustrated in Figure 3.1. Each phase leg of this converter is comprised of a single phase, three-level capacitor-clamped inverter. The output voltage of the capacitor-clamped inverter commutates each dc link voltage level through independent capacitors depending on the switch states of the converter. Table 3.1 illustrates the switch states of an individual phase leg of the capacitor-clamped inverter shown in Figure 3.1. Two valid and redundant switch states achieve an output voltage of zero. Switch state 1 from Table 3.1 charges the clamp capacitor while switch state 2 discharges the clamp capacitor. Exploiting these redundant switch states balances the clamp capacitor charge. The existence of a zero level redundant switch state within a single-phase leg is unique to capacitor-clamped converters. Techniques other than common-mode reference

signal injection can be used to keep the clamp capacitors balanced. Until recently, balancing all of the clamp capacitor voltages at the converter startup was considered a complex task; however, dedicated RC pre-charge circuits have been proposed to deal with device voltage overstress during converter start up [48]. Assuming that the voltage rating of each clamp capacitor used is the same as the power switches, an n -level converter will require $\frac{(n-1)(n-2)}{2}$ clamping capacitors per phase leg in addition to $(n - 1)$ main dc link capacitors [7].

Table 3.1: Three-level capacitor-clamped inverter voltage combinations by a single-phase leg switch combinations.

Switch States	S_1	S_2	\underline{S}_1	\underline{S}_2	<i>phase – neutral</i> voltage
0	Off	Off	On	On	$-V_c$
1	On	Off	On	Off	0
2	Off	On	Off	On	0
3	On	On	Off	Off	V_c

3.2 CASCADED MULTI-CELL INVERTER WITH SEPARATE DC SOURCES

Figure 3.2 shows a three-phase cascaded multi-cell inverter with separate dc sources with each phase consisting of a three-level H-bridge. The cascaded multi-cell topologies do not suffer from inherent capacitor charge mismatch because each voltage level is established using separate and galvanically isolated transformer windings; however, the required input transformers add weight and cost to the overall converter design.

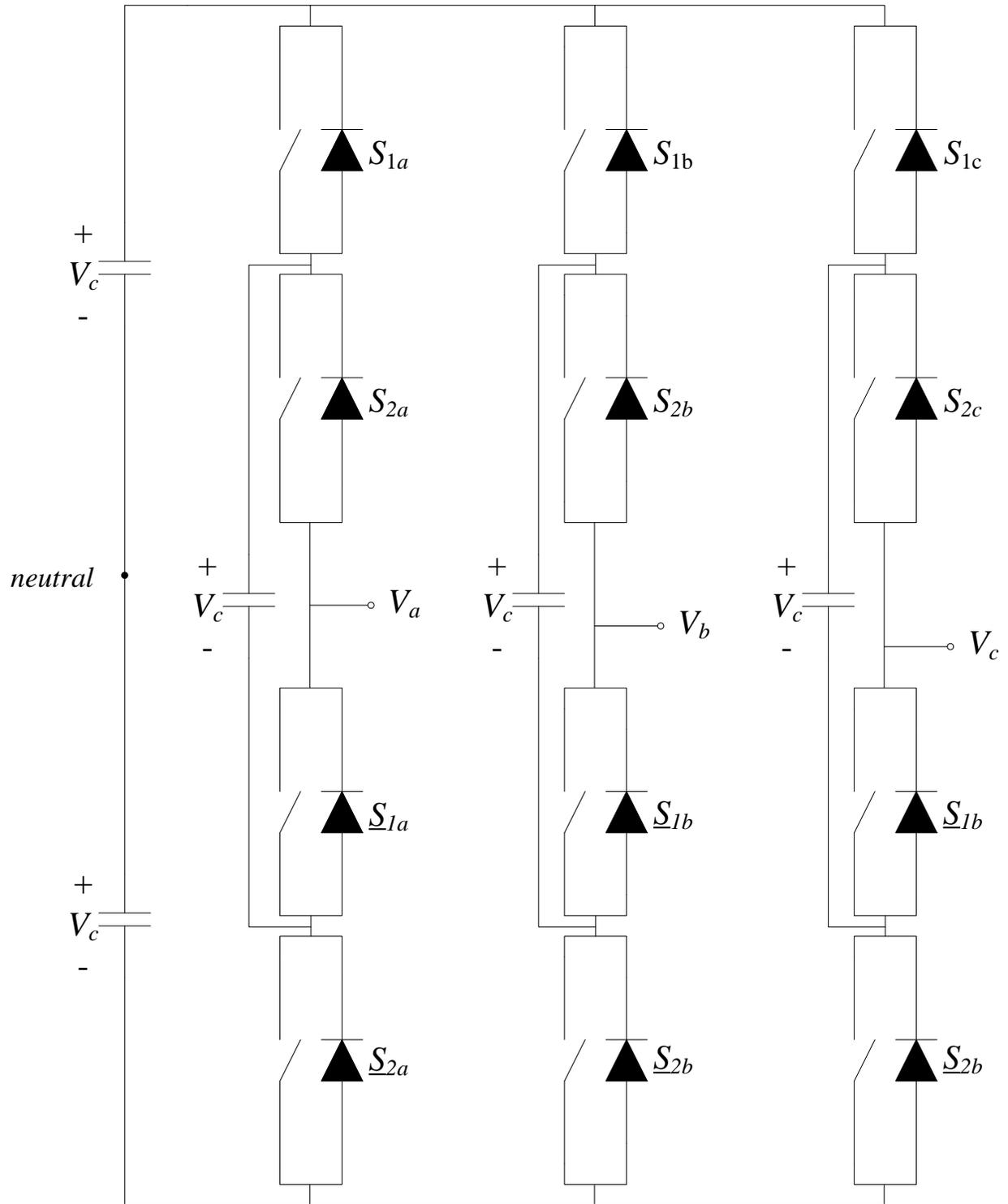


Figure 3.1: Three-phase, multilevel capacitor-clamped inverter with each phase leg comprised of a three-level capacitor-clamped inverter.

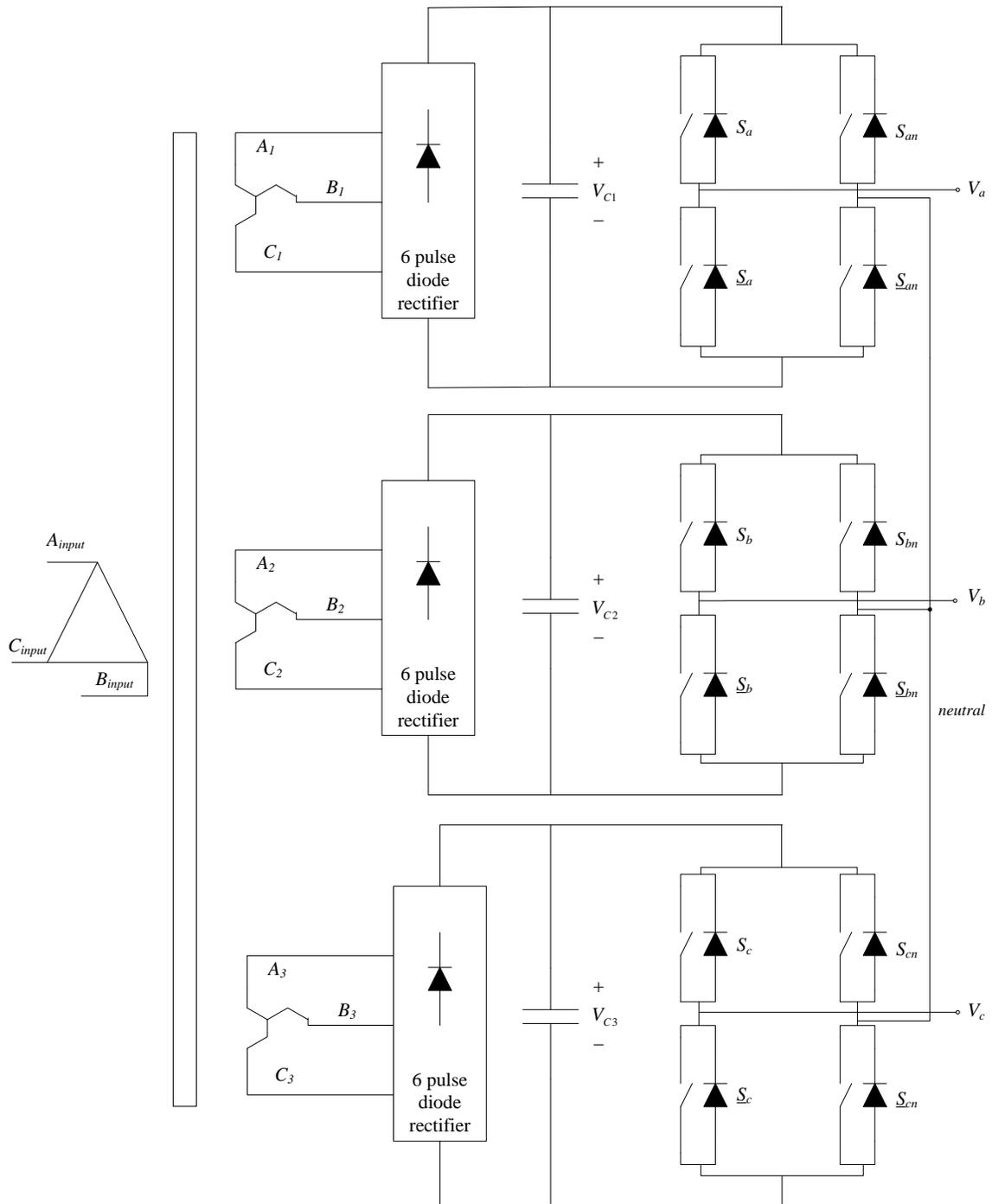


Figure 3.2: Three-phase, cascaded multi-cell inverter with separate DC sources with each phase leg comprised of a three-level H-bridge.

3.3 DIODE-CLAMPED INVERTER

Nabae, Takahashi, and Akagi introduced the neutral-point-clamped or diode-clamped inverter in 1981 as one of the first multilevel voltage sourced inverters [8]. The three-level diode-clamped inverter is shown in Figure 3.3. The inverter is comprised of four active switches and six diodes. The dc link consists of two capacitor banks each sharing the entire dc link voltage evenly. Each semiconductor blocks a single capacitor level V_c worth of voltage during the inverter operation. Table 3.2 summarizes the valid switch states for the corresponding output voltage achieved with respect to neutral.

Paralleling three of the inverters depicted in Figure 3.4 forms a three-phase diode-clamped inverter.

The three-level diode-clamped inverter does not exhibit an average capacitor voltage imbalance problem if all modulator reference waveforms contain no dc offset around the neutral point. The dc link capacitor voltages will vary as a function of the dc link capacitance and reactive power demand. Figure 3.5 illustrates the ideal switch model of back-to-back three-phase diode-clamped inverters sharing common dc link capacitance. Several ac-ac conversion applications use this back-to-back arrangement of two converters.

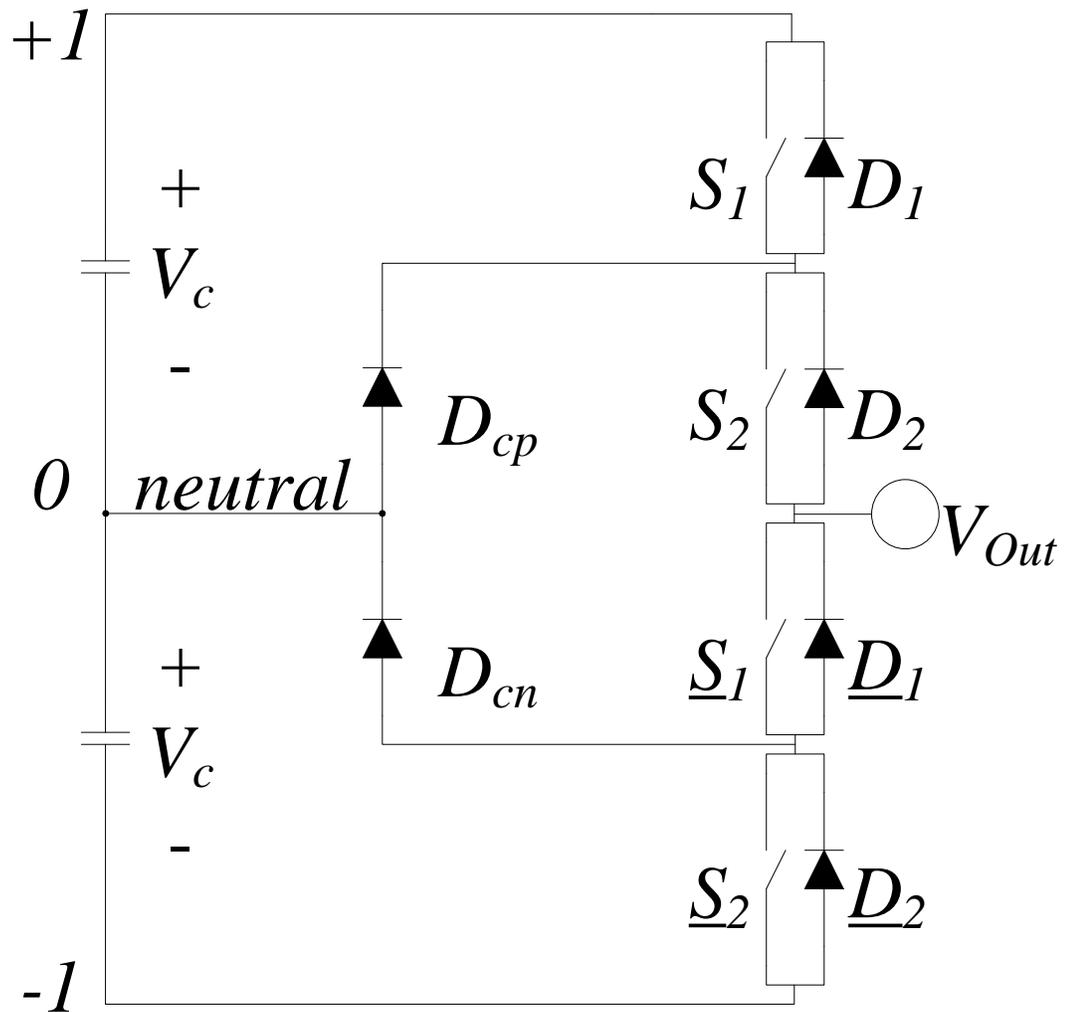


Figure 3.3: Three-level diode-clamped inverter.

Table 3.2: Three-level diode-clamped inverter voltage combinations by a single-phase leg switch combinations.

Switch States	S_1	S_2	\underline{S}_1	\underline{S}_2	<i>phase – neutral voltage</i>
0	Off	Off	On	On	$-V_c$
1	Off	On	On	Off	0
2	On	On	Off	Off	V_c

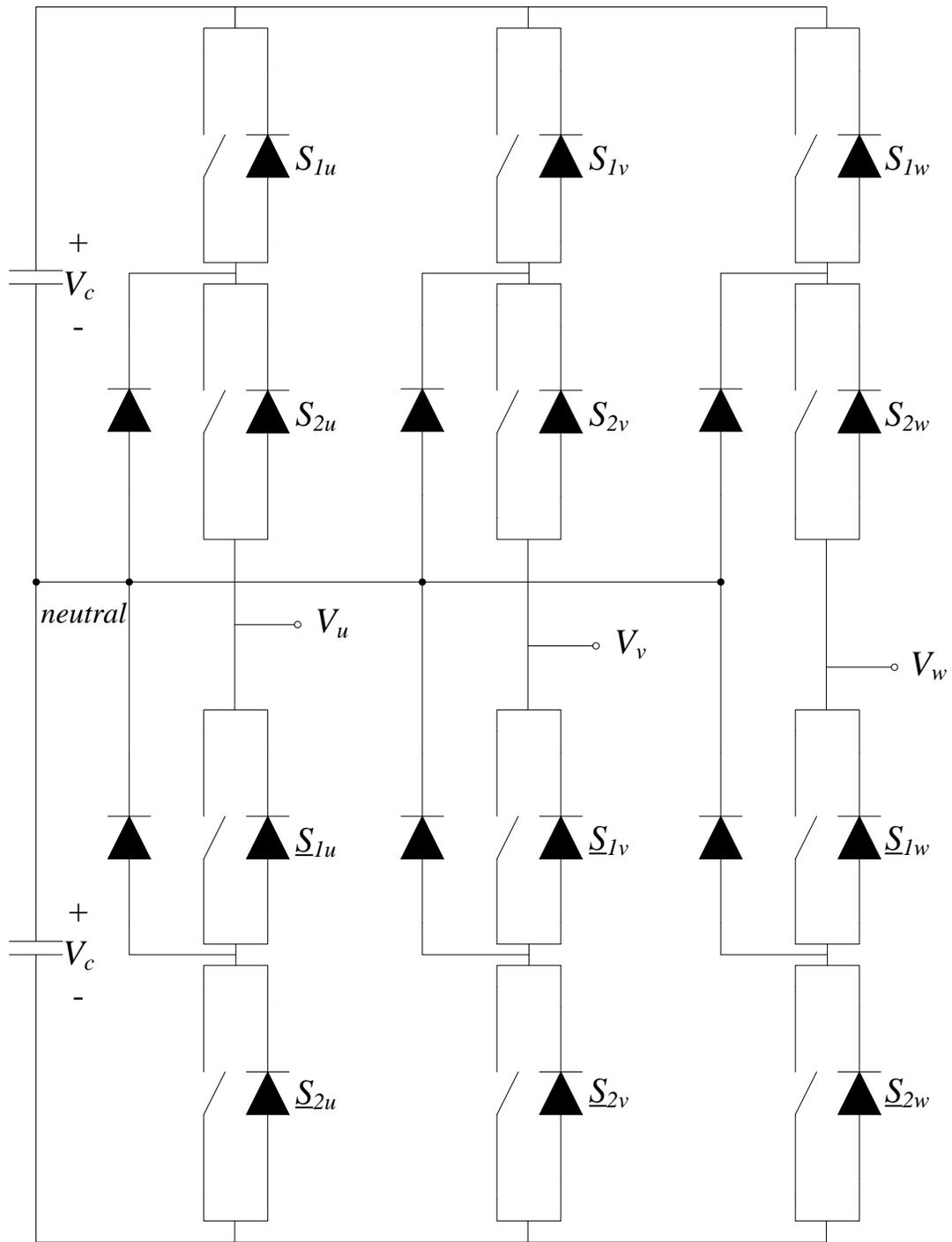


Figure 3.4: Three-phase inverter with each phase leg comprised of a three-level diode clamped inverter.

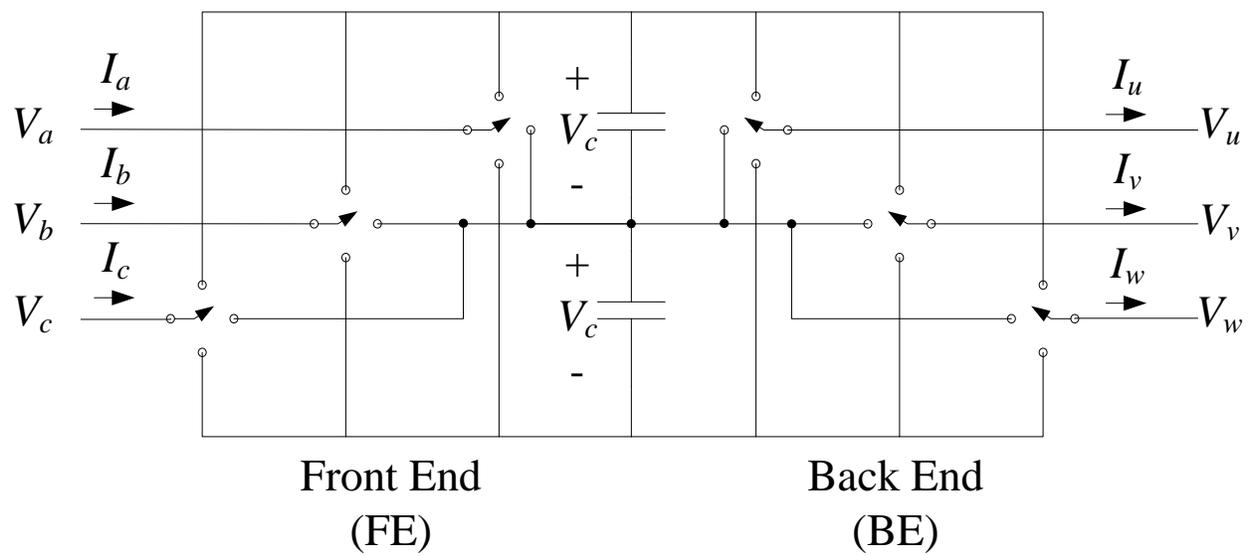


Figure 3.5: Three-phase inverter with each phase leg comprised of a three-level diode clamped inverter.

4.0 CIRCUIT UNWRAPPING FOR N-LEVEL MULTILEVEL CONVERTER

A key enabler for the medium-voltage use of discrete power semiconductor devices soldered to a PCB is an exploitation of the arrangement of the topology [40]. This topology “unwrapping” and mechanical arrangement scheme provides two major advantages: it reduces commutation loop inductance, and it can be exploited to create an active dc-link capacitor balancing circuit using the same power bridge. The unwrapped arrangement is applicable to all NPC topologies including classic NPC [8], ANPC [9], and NPP [10] multilevel converter topologies.

The unwrapping scheme is presented first using the three-level NPP bridge and then the five-level NPP bridge which is the focus of the remainder of the dissertation. The three-level NPC bridge is shown in 4.1 to demonstrate applicability to both topologies.

A pair of traditional and unwrapped configurations are shown for the single-phase, three-level NPC topology in Figure 4.1. All circuit nodes are not preserved when the topology is unwrapped such as the $(Q1, Q2, D1, D2)$ node shown in Figure 4.1a. The unwrapped mechanical arrangement scheme is theoretically applicable to all N -level NPC topologies.

4.0.1 Topology Unwrap for Three-Level NPP Converter

The three-level NPP bridge is illustrated in its usual “wrapped” configuration in Figure 4.2a and shown with commutation loop definitions. With this traditional depiction of the topology, all switches and their corresponding freewheeling diodes are grouped together in an antiparallel arrangement.

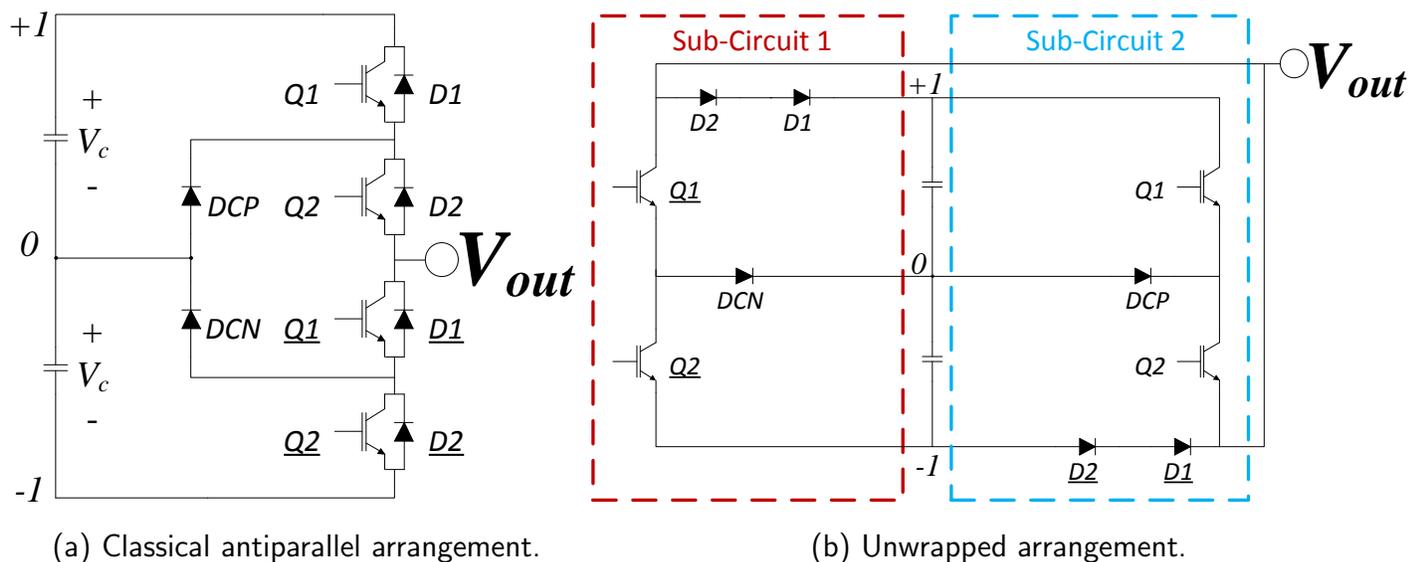


Figure 4.1: Classic and unwrapped three-level NPC topology shown without commutation loops.

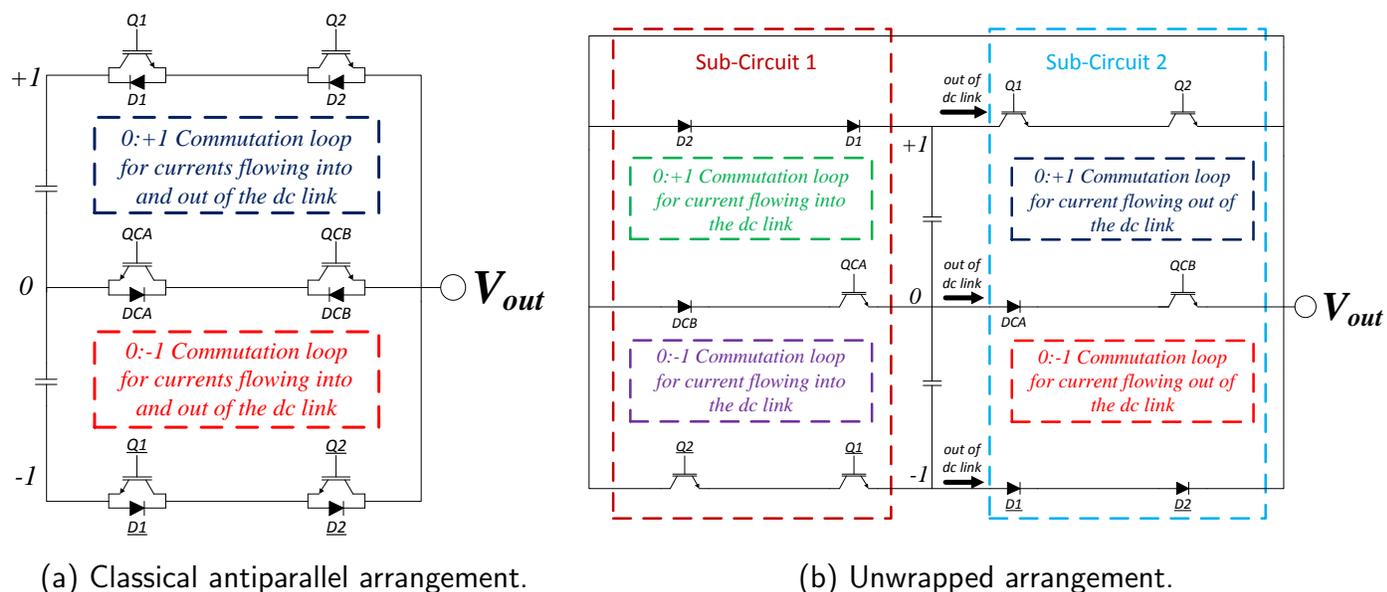


Figure 4.2: Classic and unwrapped three-level NPP topology shown with commutation loops.

It is possible to “unwrap” the circuit by grouping devices into two sub-circuits, with one carrying current into the dc-link and one carrying current out of the dc-link. The output of the two sub-circuits are then connected together to create the output terminal of a single-phase power stage. Figure 4.2b illustrates the single-phase, three-level NPP topology unwrapped into two sub-circuits shown with commutation loop definitions. All circuit nodes are not preserved when the topology is unwrapped such as the (QCA, QCB, DCA, DCB) node shown in Figure 4.2a. However, this does not change the switching behavior because the stage does not require these nodes for operation.

The bridge is operated to move the output node to any one of three states: $+1, 0, -1$. Commutation events considered valid are: moving in either direction between states -1 and 0 , and between states 0 and $+1$. From this analysis, one can see that all non-zero current commutation events occur within a single sub-circuit. Moving between states -1 and $+1$ for both current into and out of the dc-link are possible commutation events that would not leave their respective sub-circuits, but the bridge is typically not operated this way in medium-voltage converters to minimize the dv/dt stress in the system and is therefore not illustrated in Figure 4.2.

4.0.2 Reduced Commutation Inductance

The unwrapping technique allows for reduced commutation inductance compared to the traditional antiparallel arrangement. A power stage layout for the antiparallel arrangement must consider commutation loops with both switches and diodes for events with current flowing into and out of the dc capacitors. In contrast, the commutation loops in the unwrapped design contain only switches *or* diodes, meaning each commutation loop contains half as many devices. Typically each semiconductor die and heat sink pair are the same size for either diodes or switches, so half as many devices implies half the physical space. As loop inductance is primarily a function of the physical area of the loop, separating the loops translates to a much lower total inductance for each of the commutation paths.

The unwrapped mechanical arrangement commutation loop inductances can be minimized by properly arranging the components within sub-circuit 1 and sub-circuit 2 indepen-

dently, with outputs connected together to create a single phase bridge. The adjacency of each commutation loop in the unwrapped version ensures that the voltage between heatsinks is equally distributed across the board, which is not true for traditional ANPC or NPC layouts. This minimizes the distance required between heatsinks to support the voltage isolation requirement, further reducing the inductance. Minimizing the inductance between the two sub-circuit boards is not of great importance because all non-zero current commutation events will occur strictly within one of the two sub-circuit boards.

When using PCB construction at the proposed voltages the designer is limited to a layout with locally small voltage differential around any PCB feature that crosses layers such as through-hole pads or vias. If more than two layers were used, the large creepage and clearance distances required to maintain voltage isolation would make the system impractical. The main voltage isolation method uses in-plane distance across the PCB surface.

Additionally, when the number of levels of the NPC or ANPC topology in antiparallel configuration is increased beyond three, several of the connection paths must cross and managing voltage isolation of these connection paths with a two-layer bus structure becomes difficult due to the creepage and clearance distance requirements. The unwrapped NPC topology with more than three levels removes all connection path crossings and enables a PCB layout with reasonable spacing. This is not an issue with NPP.

4.1 MULTILEVEL DIODE-CLAMPED INVERTER

The diode-clamped inverter is easily extended to a multilevel topology [1]. Figure 4.3 illustrates the five-level NPP bridge shown in classical antiparallel arrangement Figure 4.3a and unwrapped Figure 4.3b with a single device rating per voltage level. This is the topology chosen for implementation and it is the focus of the remainder of this dissertation.

The five-level, back-to-back NPP inverter is shown in Figure 4.4 where IGBTs replace the ideal switches. Table 4.1 summarizes the valid switch states for a single-phase leg and the corresponding output voltage achieved with respect to neutral for the five-level inverter.

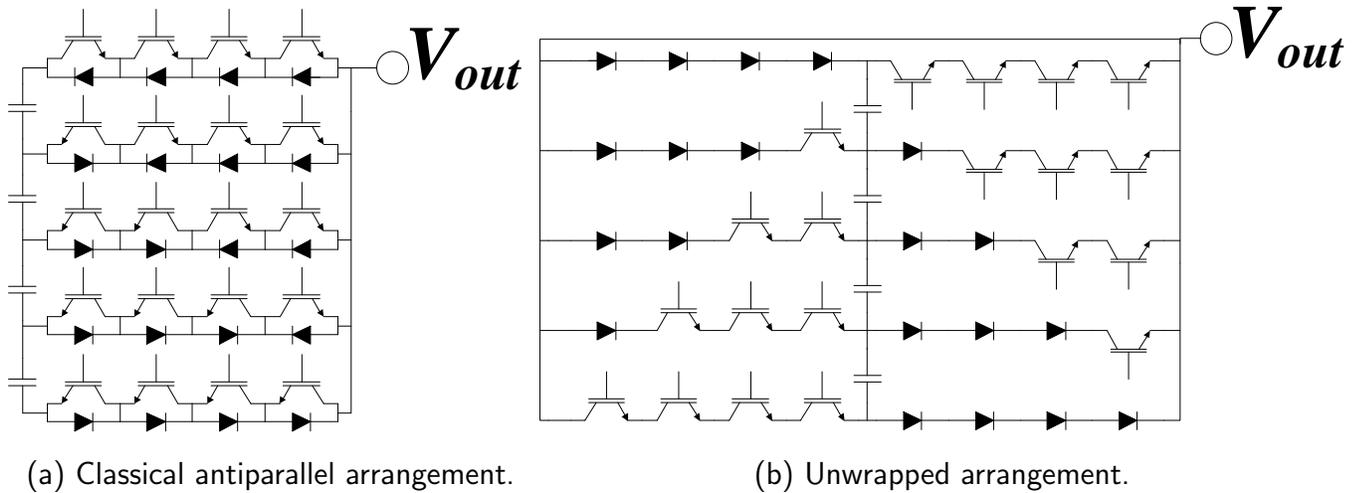


Figure 4.3: Classic and unwrapped five-level NPP topology shown without commutation loops.

The ideal multi-pole switch model of the five-level, back-to-back converter system is depicted in Figure 4.5. An extension of the average capacitor voltage drift analysis from [41] can be made to the back-to-back converter system shown in Figure 4.5. Assuming the carrier frequency is much higher than the modulated reference signal, the instantaneous value of the modulated reference signal approximate the continuous switching functions. This analysis assumes the two sets of converter currents and voltages each form a balanced three-phase set. The modulator reference signals for both the input bridge and output bridge along with the input and output currents are as shown in equations (4.1) through (4.12).

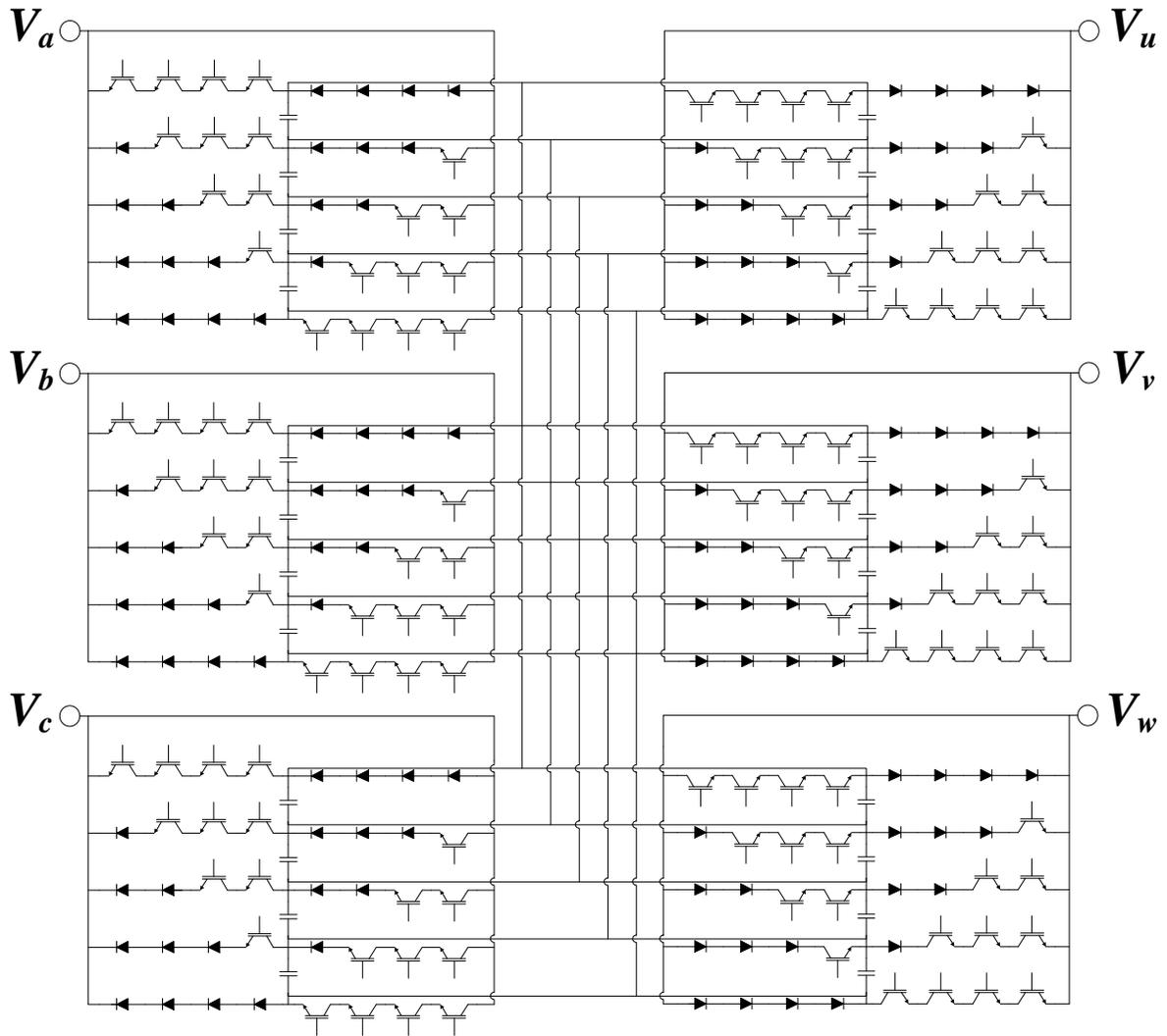


Figure 4.4: IGBT based ac-ac converter system comprised of six independent phase legs (3 input legs and 3 output legs). Each phase leg is comprised of a five-level NPP converter.

Table 4.1: Five-level diode-clamped inverter voltage combinations by a single-phase leg switch combinations.

Switch States	S_1	S_2	S_3	S_4	\underline{S}_1	\underline{S}_2	\underline{S}_3	\underline{S}_4	<i>phase – neutral</i> voltage
0	Off	Off	Off	Off	On	On	On	On	$-(V_{c2} + V_{c1})$
1	Off	Off	Off	On	On	On	On	Off	$-V_{c2}$
2	Off	Off	On	On	On	On	Off	Off	0
3	Off	On	On	On	On	Off	Off	Off	V_{c3}
4	On	On	On	On	Off	Off	Off	Off	$V_{c3} + V_{c4}$

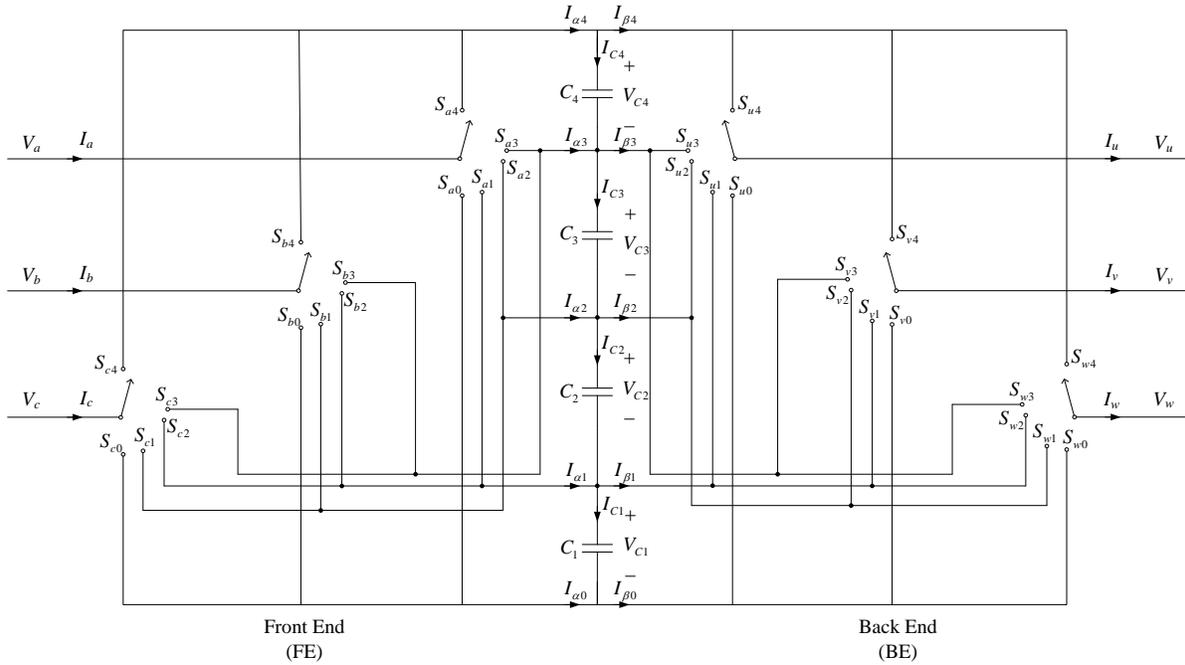


Figure 4.5: Ideal switch model of active front-end / inverter system comprised of six phase legs. Each phase leg is comprised of a single five-level NPC converter.

$$M_a(\omega t) = m_\alpha \sin(\omega t + \alpha) \quad (4.1)$$

$$M_b(\omega t) = m_\alpha \sin\left(\omega t - \frac{2\pi}{3} + \alpha\right) \quad (4.2)$$

$$M_c(\omega t) = m_\alpha \sin\left(\omega t + \frac{2\pi}{3} + \alpha\right) \quad (4.3)$$

$$M_u(\omega t) = m_\beta \sin(\omega t + \beta) \quad (4.4)$$

$$M_v(\omega t) = m_\beta \sin\left(\omega t - \frac{2\pi}{3} + \beta\right) \quad (4.5)$$

$$M_w(\omega t) = m_\beta \sin\left(\omega t + \frac{2\pi}{3} + \beta\right) \quad (4.6)$$

$$I_a(\omega t) = I_{m_\alpha} \sin(\omega t + \theta_{abc} + \alpha) \quad (4.7)$$

$$I_b(\omega t) = I_{m_\alpha} \sin\left(\omega t - \frac{2\pi}{3} + \theta_{abc} + \alpha\right) \quad (4.8)$$

$$I_c(\omega t) = I_{m_\alpha} \sin\left(\omega t + \frac{2\pi}{3} + \theta_{abc} + \alpha\right) \quad (4.9)$$

$$I_u(\omega t) = I_{m_\beta} \sin(\omega t + \theta_{uvw} + \beta) \quad (4.10)$$

$$I_v(\omega t) = I_{m_\beta} \sin\left(\omega t - \frac{2\pi}{3} + \theta_{uvw} + \beta\right) \quad (4.11)$$

$$I_w(\omega t) = I_{m_\beta} \sin\left(\omega t + \frac{2\pi}{3} + \theta_{uvw} + \beta\right) \quad (4.12)$$

The out of-phase disposition sine-triangle modulation strategy depicted in Figure 4.6 is used throughout the average switching waveform analysis [49].

4.2 INSTANTANEOUS CAPACITOR VOLTAGE DEVIATION

Figure 4.7 depicts the equivalent switching waveform and the corresponding average waveform for switch position S_{a4} .

The average waveform for switch position S_{a4} extends for switch positions S_{b4} , S_{c4} , S_{u4} , S_{v4} , and S_{w4} according to the modulation depths and phase angles defined in (4.1) through (4.12). $I_{\alpha 4}$ and $I_{\beta 4}$ can be written in terms of these average waveforms as in (4.13) through (4.14).

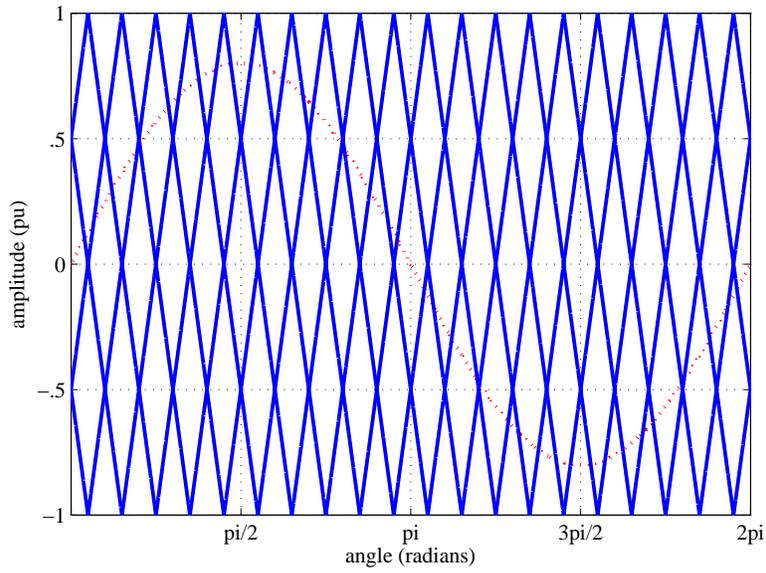


Figure 4.6: Five-level out-of-phase disposition sine-triangle modulation scheme.

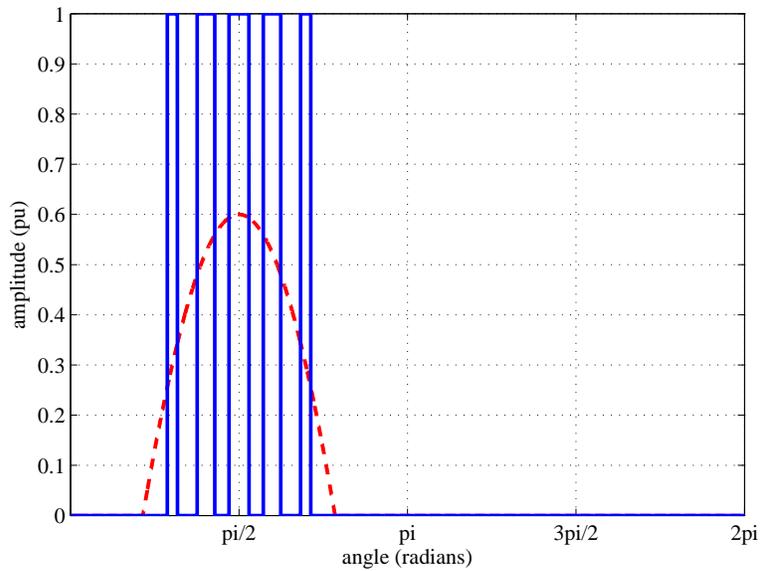


Figure 4.7: Equivalent switching waveforms for switch position 4 for phase a. The average waveform (dashed line) and the switched waveform function (solid line) are shown.

$$I_{\alpha 4} = \widehat{S}_{a4} I_a + \widehat{S}_{b4} I_b + \widehat{S}_{c4} I_c \quad (4.13)$$

$$I_{\beta 4} = \widehat{S}_{u4} I_u + \widehat{S}_{v4} I_v + \widehat{S}_{w4} I_w \quad (4.14)$$

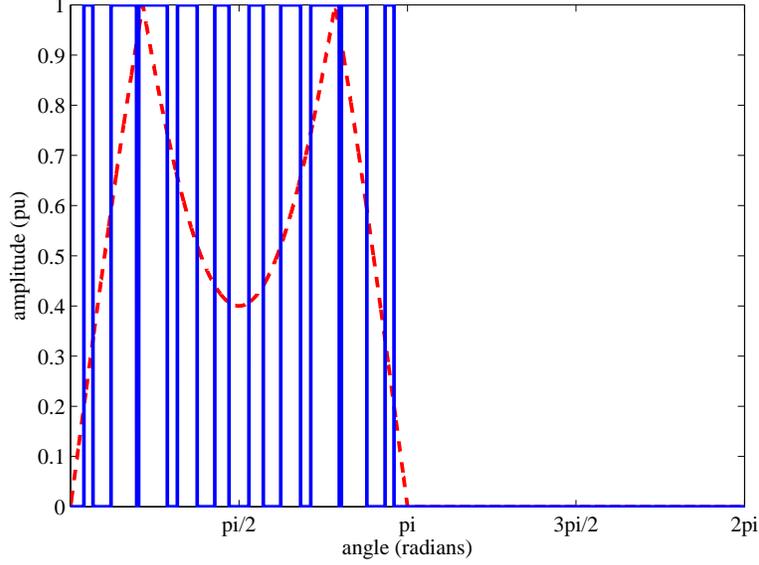


Figure 4.8: Equivalent switching waveforms for switch position 3 for phase a. The average waveform (dashed line) and the switched waveform function (solid line) are shown.

The equivalent switching waveform and the corresponding average waveform for switch position S_{a3} are depicted in Figure 4.8. The average waveform for switch position S_{a3} extends for switch positions S_{b3} , S_{c3} , S_{u3} , S_{v3} , and S_{w3} according to the modulation depths and phase angles defined in (4.1) through (4.12). $I_{\alpha 3}$ and $I_{\beta 3}$ can be written in terms of these average waveforms as in (4.15) through (4.16).

$$I_{\alpha 3} = \widehat{S}_{a3} I_a + \widehat{S}_{b3} I_b + \widehat{S}_{c3} I_c \quad (4.15)$$

$$I_{\beta 3} = \widehat{S}_{u3} I_u + \widehat{S}_{v3} I_v + \widehat{S}_{w3} I_w \quad (4.16)$$

Figure 4.9 depicts the equivalent switching waveform and the corresponding average waveform for switch position S_{a2} . The average waveform for switch position S_{a2} extends for

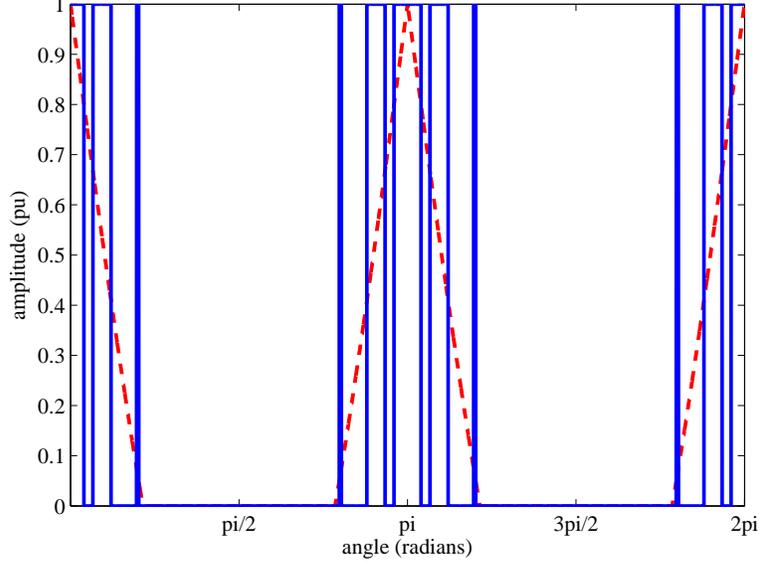


Figure 4.9: Equivalent switching waveforms for switch position 2 for phase a. The average waveform (dashed line) and the switched waveform function (solid line) are shown.

switch positions S_{b2} , S_{c2} , S_{u2} , S_{v2} , and S_{w2} according to the modulation depths and phase angles defined in (4.1) through (4.12). $I_{\alpha 2}$ and $I_{\beta 2}$ can be written in terms of these average waveforms as in (4.17) through (4.18).

$$I_{\alpha 2} = \widehat{S}_{a2}I_a + \widehat{S}_{b2}I_b + \widehat{S}_{c2}I_c \quad (4.17)$$

$$I_{\beta 2} = \widehat{S}_{u2}I_u + \widehat{S}_{v2}I_v + \widehat{S}_{w2}I_w \quad (4.18)$$

The equivalent switching waveform and the corresponding average waveform for switch position S_{a1} are depicted in Figure 4.10. The average waveform for switch position S_{a1} extends for switch positions S_{b1} , S_{c1} , S_{u1} , S_{v1} , and S_{w1} according to the modulation depths and phase angles defined in (4.1) through (4.12). $I_{\alpha 1}$ and $I_{\beta 1}$ can be written in terms of these average waveforms as in(4.19) through (4.20).

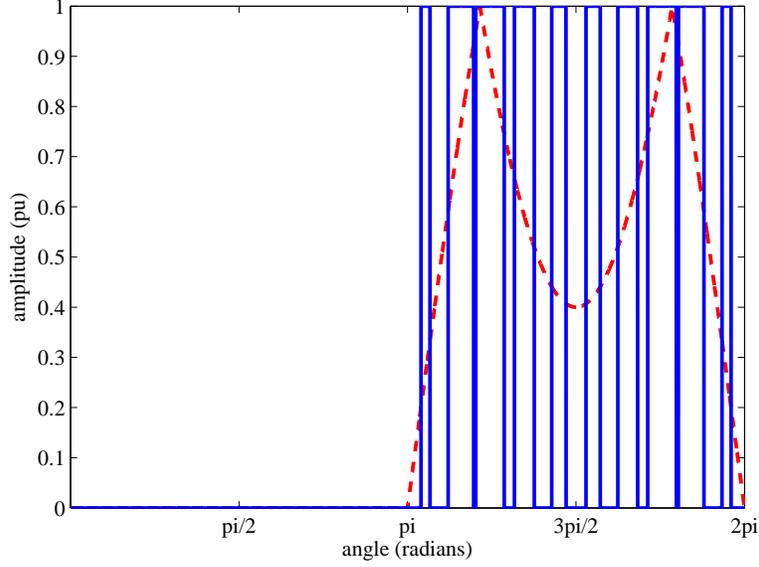


Figure 4.10: Equivalent switching waveforms for switch position 1 for phase a. The average waveform (dashed line) and the switched waveform function (solid line) are shown.

$$I_{\alpha 1} = \widehat{S}_{a1} I_a + \widehat{S}_{b1} I_b + \widehat{S}_{c1} I_c \quad (4.19)$$

$$I_{\beta 1} = \widehat{S}_{u1} I_u + \widehat{S}_{v1} I_v + \widehat{S}_{w1} I_w \quad (4.20)$$

Figure 4.11 depicts the equivalent switching waveform and the corresponding average waveform for switch position S_{a0} . The average waveform for switch position S_{a0} extends for switch positions S_{b0} , S_{c0} , S_{u0} , S_{v0} , and S_{w0} according to the modulation depths and phase angles defined in (4.1) through (4.12). $I_{\alpha 0}$ and $I_{\beta 0}$ can be written in terms of these average waveforms as in (4.21) through (4.22).

$$I_{\alpha 0} = \widehat{S}_{a0} I_a + \widehat{S}_{b0} I_b + \widehat{S}_{c0} I_c \quad (4.21)$$

$$I_{\beta 0} = \widehat{S}_{u0} I_u + \widehat{S}_{v0} I_v + \widehat{S}_{w0} I_w \quad (4.22)$$

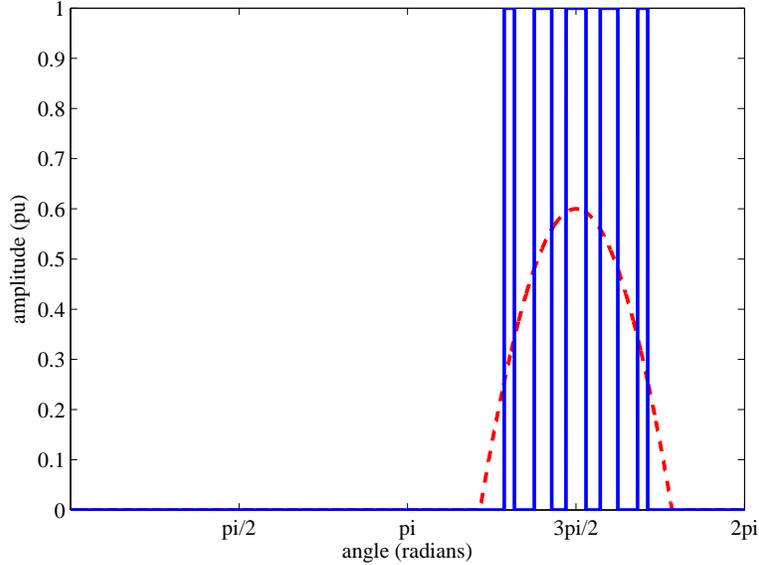


Figure 4.11: Equivalent switching waveforms for switch position 0 for phase a. The average waveform (dashed line) and the switched waveform function (solid line) are shown.

A non-zero instantaneous capacitor current deviation between capacitors 2 and 3 will be present for most operating ranges due to the zero sequence voltage at the output of the VSI [46]; however, no mechanism exists to produce a non-zero average current deviation between capacitors 2 and 3 because the system was defined as a balanced three-phase sinusoidal system with no dc offsets. It is therefore interesting to examine both the instantaneous and average capacitor current deviation between capacitors 3 and 4 and between capacitors 1 and 2 that exists for most system operating points.

The currents defined as functions of the front-end and back-end converter modulation depths and phase angles in (4.13) through (4.22) are used to create a capacitors 3 and 4 and capacitors 1 and 2 current deviation model as shown in Figure 4.12.

A per unitized simulation model was created using the capacitor current deviation model in Figure 4.12 to explore the effects of power factor and voltage angle deviations between the front-end and back-end converters. The simulation model was configured for a 1000hp, 4160V system. The system base units were calculated in (4.26) through (4.26).

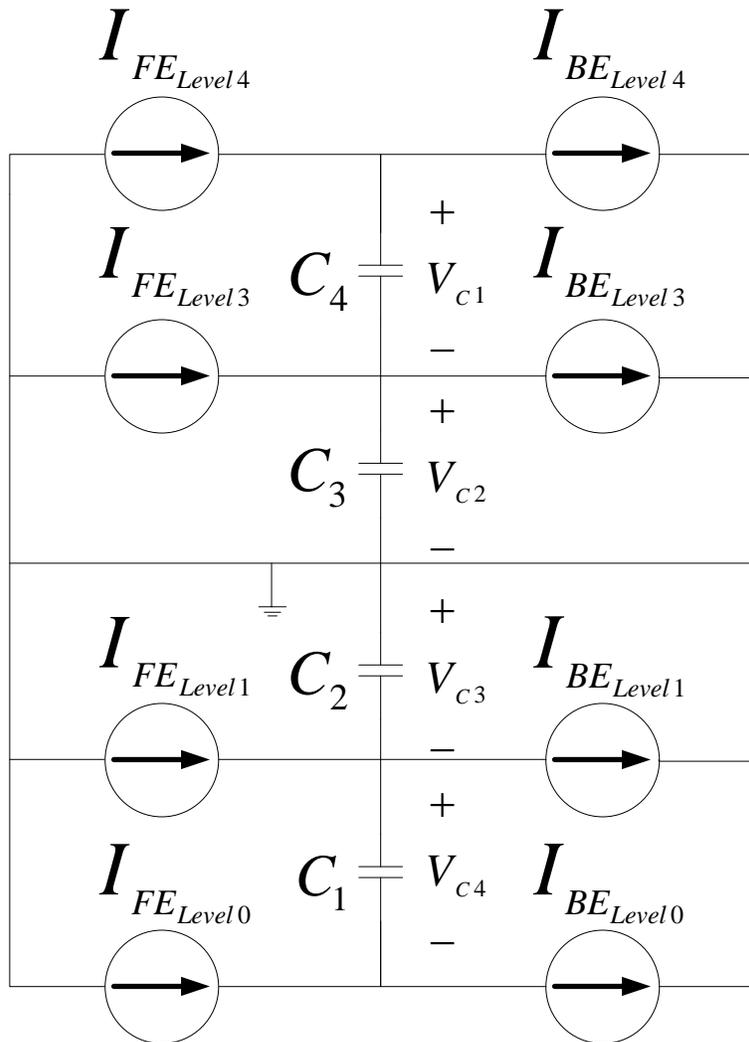


Figure 4.12: Capacitor 3 and 4 and capacitor 1 and 2 current deviation model.

$$V_{base} = \frac{V_{linetoline}}{\sqrt{3}} = \frac{4160V}{\sqrt{3}} = 2401.8V \quad (4.23)$$

$$I_{base} = \frac{S_{base}}{3V_{base}} = \frac{745699.872w}{3(2401.8V)} = 103.4918A \quad (4.24)$$

$$Z_{base} = \frac{V_{base}}{I_{base}} = \frac{2401.8V}{103.4918A} = 23.2076\Omega \quad (4.25)$$

$$C_{base} = \frac{1}{\omega_{base}Z_{base}} = \frac{1}{(2\pi 60Hz)23.2076\Omega} \quad (4.26)$$

With no third harmonic injection, the required dc link voltage with a modulation depth of 1 is [49] given in (4.27) through (4.28).

$$V_{max,rms} = .612V_{dclink}V \quad (4.27)$$

$$V_{dclink} = \frac{4160V}{.612} = 6797.4V \quad (4.28)$$

The voltage per level for a five-level inverter is given in (4.31) through (4.30).

$$V_{level} = \frac{V_{dclink}}{4} = 1694.3V \quad (4.29)$$

$$V_{level,pu} = \frac{V_{level}}{V_{base}} = \frac{1694.3V}{2401.8V} = .7075 \quad (4.30)$$

Typical capacitance per level for a five-level 4160V, 1000hp drive is 1mF. The capacitance per level in per unit is:

$$C_{level,pu} = \frac{1mF}{.11430mF} = 8.749 \quad (4.31)$$

The I_α and I_β currents were calculated for various front-end and back-end modulation depths and power factors to investigate voltage deviations for capacitors 3 and 4 and capacitors 1 and 2. The currents were calculated in Matlab and used as forcing functions in LTspice to calculate the capacitor voltages for several cases. All dc link capacitor voltages were initialized to .7075pu. As a model verification exercise, the front-end and back-end modulation depths, voltage angles, power factors, and current magnitudes were initialized

to the same values. Figure 4.13 illustrates the results of this case. The dc link capacitor voltages remained unchanged because the front-end currents instantaneously equaled the back-end currents on all voltage levels.

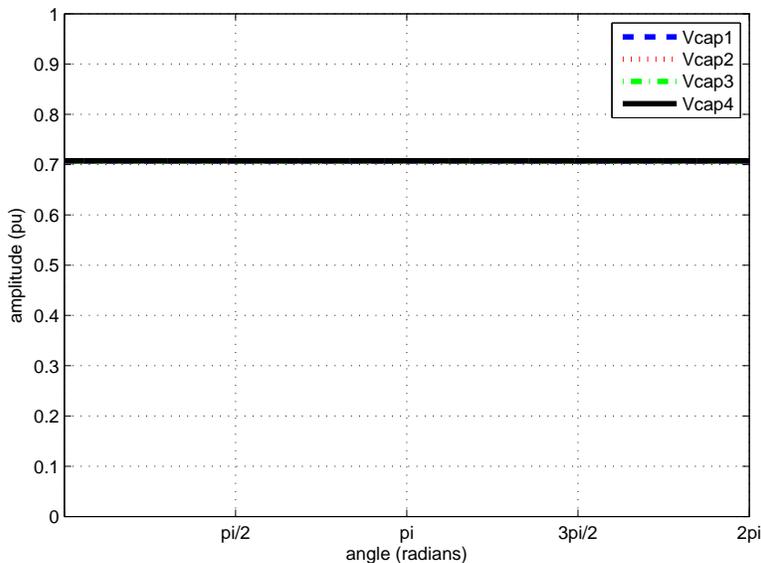


Figure 4.13: Case: front-end modulation depth = 1, back-end modulation depth = 1, front-end voltage angle = $0rad$, back-end voltage angle = $0 rad$, front-end power factor = 1, back-end power factor = 1, front-end current magnitude = $1pu$, back-end current magnitude = $1pu$

Next, a case was formulated to simulate a typical induction motor drive scenario. The front-end and back-end modulation depths were both set to 1. The front-end power factor was set to 1. The back-end power factor was set to .85 to model the induction motor. The front-end current magnitude was set to $1pu$. The active power flowing into and out of the dc link was kept equal by scaling the back-end current by the back-end power factor. The front-end and back-end voltage angles were kept equal at $0rad$. The results of the typical induction motor drive case are illustrated in Figure 4.14.

Several important observations can be made from Figure 4.14. First, there are voltage deviations from nominal for all four capacitors. These voltage deviations are occurring at three times the fundamental frequency. The voltage deviations between capacitors 1 and 2 and capacitors 3 and 4 are equal and πrad radians out of phase. Lastly, there is no

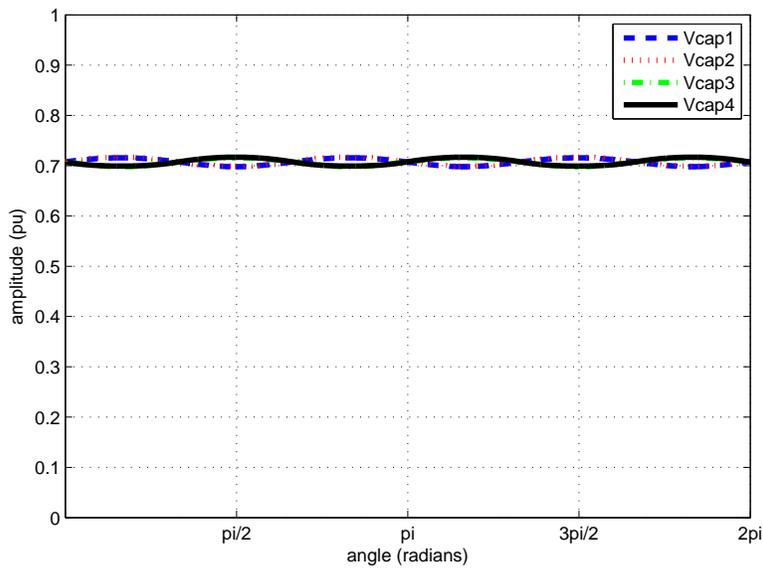


Figure 4.14: Case: front-end modulation depth = 1, back-end modulation depth = 1, front-end voltage angle = $0rad$, back-end voltage angle = $0rad$, front-end power factor = 1, back-end power factor = .85, front-end current magnitude = $1pu$, back-end current magnitude = $\frac{1}{.85pu}$

average current deviation between any of the capacitors. No average current deviation is an important characteristic for the system because it indicates that the dc link will not collapse in this operating state.

The next formulated simulation case investigated the effect of voltage angle difference between the front-end and back-end converters. The front-end and back-end modulation depths were both set to 1. Both the front-end and back-end power factors were set to 1. Both the front and back-end current magnitudes were set to 1 to ensure no mismatch in active power flowing into and out of the dc link. The front-end voltage angle was set to $0rad$ and the back-end voltage angle was set to πrad . Figure 4.15 illustrates the results of this case.

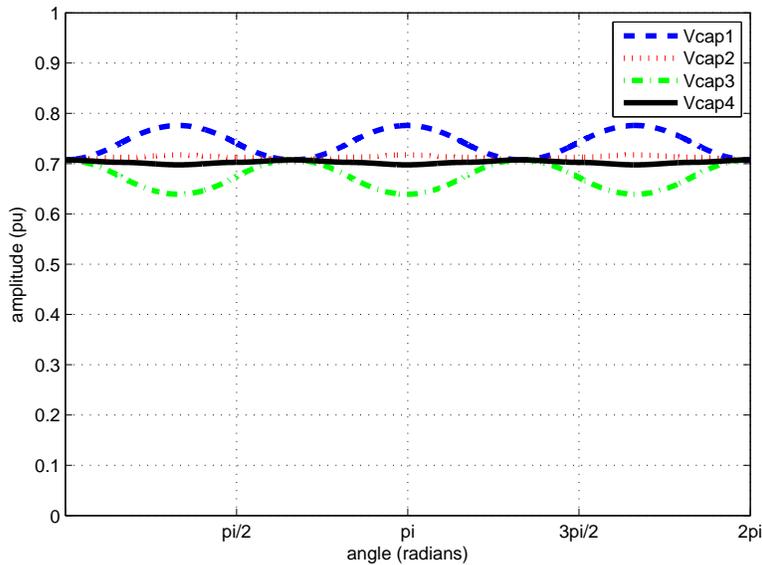


Figure 4.15: Case: front-end modulation depth = 1, back-end modulation depth = 1, front-end voltage angle = $0rad$, back-end voltage angle = πrad , front-end power factor = 1, back-end power factor = 1, front-end current magnitude = $1pu$, back-end current magnitude = $1pu$

Figure 4.15 illustrates several important facts. First, there are clear voltage deviations from nominal for all four capacitors. These voltage deviations for capacitors 1 and 3 are occurring at three times the fundamental frequency, equal in magnitude, and are πrad out of phase with each other. The voltage deviations for capacitors 2 and 4 contain a three times

the fundamental frequency component, but also contain higher order harmonics. The voltage deviations for capacitors 2 and 4 are also equal in magnitude and are πrad out of phase with each other. Lastly, there is no average current deviation between any of the capacitors.

Next, a case was formulated to include parameters from the previous two cases. The front-end and back-end modulation depths were both set to 1. The front-end power factor was set to 1. The back-end power factor was set to .85. The front-end current magnitude was set to $1pu$. The active power flowing into and out of the dc link was kept equal by scaling the back-end current by the back-end power factor. The front-end voltage angle was set to $0rad$, and the back-end voltage angle was set to πrad . Figure 4.16 illustrates the results of this case.

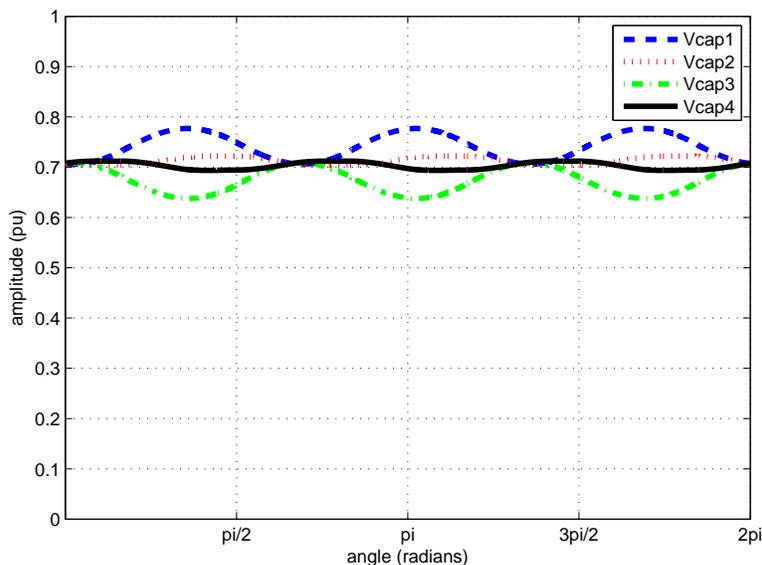


Figure 4.16: Case: front-end modulation depth = 1, back-end modulation depth = 1, front-end voltage angle = $0rad$, back-end voltage angle = πrad , front-end power factor = 1, back-end power factor = .85, front-end current magnitude = $1pu$, back-end current magnitude = $\frac{1}{.85pu}$

Several important observations can be made from Figure 4.16. First, there are voltage deviations from nominal for all four capacitors. These voltage deviations for capacitors 1 and 3 are occurring at three times the fundamental frequency, equal in magnitude and πrad radians out of phase with each other. The voltage deviations for capacitors 2 and 4 contain a

three times the fundamental frequency component, but also contain higher order harmonics. The voltage deviations for capacitors 2 and 4 are also equal in magnitude and out of phase with each other. Lastly, there is no average current deviation between any of the capacitors. A final formulated case investigated the effects of real power mismatch flowing into and out of the dc link. The front-end power factor was set to 1. The back-end power factor was set to .85. The front-end and back-end current magnitudes were both set to 1pu. The active power flowing into and out of the dc link is now unequal. The front-end and back-end voltage angles were set to $0rad$. Figure 4.17 illustrates the results of this case. Capacitor voltages 1 and 3 are unstable due to the real power mismatch at each dc link level.

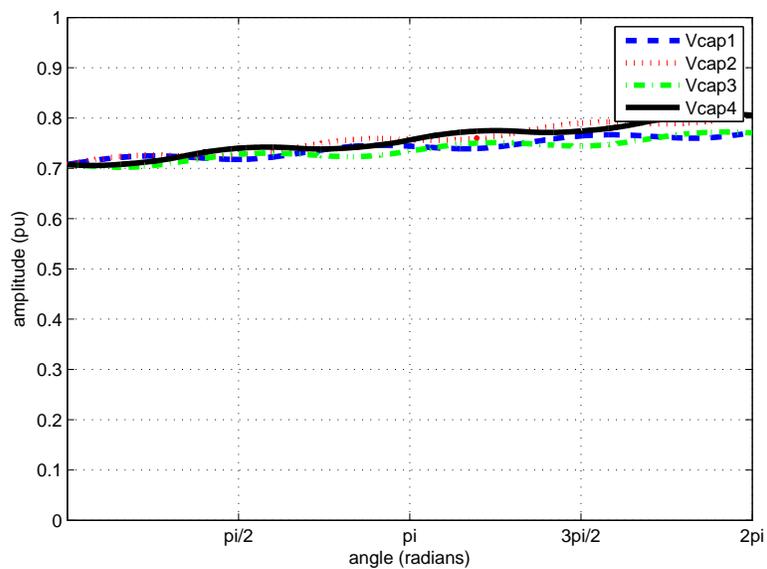


Figure 4.17: Case: front-end modulation depth = 1, back-end modulation depth = 1, front-end voltage angle = $0rad$, back-end voltage angle = $0rad$, front-end power factor = 1, back-end power factor = .85, front-end current magnitude = $1pu$, back-end current magnitude = $1pu$

Additional work is required to quantify all of the phenomena observed through the simulation test cases. It is clear that reactive power mismatch at the dc link causes capacitor voltage deviations from nominal; however, these voltage deviations are stable. It is also clear that front-end to back-end voltage angle difference also causes dc link capacitor voltage deviation; however, these voltage deviations are stable.

4.3 AVERAGE CAPACITOR VOLTAGE DEVIATION

To find the average currents $\bar{I}_{\alpha 4}$ and $\bar{I}_{\beta 4}$, integrate each over one period as follows:

$$\bar{I}_{\alpha 4} = \frac{1}{2\pi} \int_0^{2\pi} \left(\widehat{S}_{a4} I_a + \widehat{S}_{b4} I_b + \widehat{S}_{c4} I_c \right) d\theta \quad (4.32)$$

$$\bar{I}_{\beta 4} = \frac{1}{2\pi} \int_0^{2\pi} \left(\widehat{S}_{u4} I_u + \widehat{S}_{v4} I_v + \widehat{S}_{w4} I_w \right) d\theta \quad (4.33)$$

Using the integration results obtained in [2, 41] with a correction to [41] with the correct multiplier 3/2 for (4.36) & (4.37), and $-3/2$ for (4.40) & (4.41), the average current waveforms can be written as functions of the modulation indices and power angles for each inverter for ideal switch position 4 as follows:

$$\bar{I}_{\alpha 4} = \begin{cases} \frac{3}{4\pi} I_\alpha \cos(\phi_\alpha) \cdot \left(2m_\alpha \pi - 4m_\alpha \arcsin\left(\frac{1}{2m_\alpha}\right) - \sqrt{\frac{4m_\alpha^2 - 1}{m_\alpha^2}} \right) & \text{for } .5 \leq m_\alpha \leq 1 \\ 0 & \text{for } 0 \leq m_\alpha \leq .5 \end{cases} \quad (4.34)$$

$$\bar{I}_{\beta 4} = \begin{cases} \frac{3}{4\pi} I_\beta \cos(\phi_\beta) \cdot \left(2m_\beta \pi - 4m_\beta \arcsin\left(\frac{1}{2m_\beta}\right) - \sqrt{\frac{4m_\beta^2 - 1}{m_\beta^2}} \right) & \text{for } .5 \leq m_\beta \leq 1 \\ 0 & \text{for } 0 \leq m_\beta \leq .5 \end{cases} \quad (4.35)$$

Similarly, the average current waveforms as functions of the modulation indices and power angles for each inverter for ideal switch position 3 can be written as follows:

$$\bar{I}_{\alpha 3} = \begin{cases} \frac{3}{2\pi} I_\alpha \cos(\phi_\alpha) \cdot \left(-m_\alpha \pi + 4m_\alpha \arcsin\left(\frac{1}{2m_\alpha}\right) + \sqrt{\frac{4m_\alpha^2 - 1}{m_\alpha^2}} \right) & \text{for } .5 \leq m_\alpha \leq 1, \\ \frac{3}{2} m_\alpha I_\alpha \cos(\phi_\alpha) & \text{for } 0 \leq m_\alpha \leq .5. \end{cases} \quad (4.36)$$

$$\bar{I}_{\beta 3} = \begin{cases} \frac{3}{2\pi} I_{\beta} \cos(\phi_{\beta}) \cdot \left(-m_{\beta}\pi + 4m_{\beta} \arcsin\left(\frac{1}{2m_{\beta}}\right) + \sqrt{\frac{4m_{\beta}^2 - 1}{m_{\beta}^2}} \right) & \text{for } .5 \leq m_{\beta} \leq 1, \\ \frac{3}{2} m_{\beta} I_{\beta} \cos(\phi_{\beta}) & \text{for } 0 \leq m_{\beta} \leq .5. \end{cases} \quad (4.37)$$

Similarly, the average current waveforms as functions of the modulation indices and power angles for each inverter for ideal switch position 2 can be written as follows:

$$\bar{I}_{\alpha 2} = 0 \quad (4.38)$$

$$\bar{I}_{\beta 2} = 0 \quad (4.39)$$

Similarly, the average current waveforms as functions of the modulation indices and power angles for each inverter for ideal switch position 1 can be written as follows:

$$\bar{I}_{\alpha 1} = \begin{cases} -\frac{3}{2\pi} I_{\alpha} \cos(\phi_{\alpha}) \cdot \left(-m_{\alpha}\pi + 4m_{\alpha} \arcsin\left(\frac{1}{2m_{\alpha}}\right) + \sqrt{\frac{4m_{\alpha}^2 - 1}{m_{\alpha}^2}} \right) & \text{for } .5 \leq m_{\alpha} \leq 1, \\ -\frac{3}{2} m_{\alpha} I_{\alpha} \cos(\phi_{\alpha}) & \text{for } 0 \leq m_{\alpha} \leq .5. \end{cases} \quad (4.40)$$

$$\bar{I}_{\beta 1} = \begin{cases} -\frac{3}{2\pi} I_{\beta} \cos(\phi_{\beta}) \cdot \left(-m_{\beta}\pi + 4m_{\beta} \arcsin\left(\frac{1}{2m_{\beta}}\right) + \sqrt{\frac{4m_{\beta}^2 - 1}{m_{\beta}^2}} \right) & \text{for } .5 \leq m_{\beta} \leq 1, \\ -\frac{3}{2} m_{\beta} I_{\beta} \cos(\phi_{\beta}) & \text{for } 0 \leq m_{\beta} \leq .5. \end{cases} \quad (4.41)$$

Similarly, the average current waveforms as functions of the modulation indices and power angles for each inverter for ideal switch position 0 can be written as follows:

$$\bar{I}_{\alpha 0} = \begin{cases} -\frac{3}{4\pi} I_{\alpha} \cos(\phi_{\alpha}) \cdot \left(2m_{\alpha}\pi - 4m_{\alpha} \arcsin\left(\frac{1}{2m_{\alpha}}\right) - \sqrt{\frac{4m_{\alpha}^2 - 1}{m_{\alpha}^2}} \right) & \text{for } .5 \leq m_{\alpha} \leq 1, \\ 0 & \text{for } 0 \leq m_{\alpha} \leq .5. \end{cases} \quad (4.42)$$

$$\bar{I}_{\beta 0} = \begin{cases} -\frac{3}{4\pi} I_{\beta} \cos(\phi_{\beta}) \cdot \left(2m_{\beta}\pi - 4m_{\beta} \arcsin\left(\frac{1}{2m_{\beta}}\right) - \sqrt{\frac{4m_{\beta}^2 - 1}{m_{\beta}^2}} \right) & \text{for } .5 \leq m_{\beta} \leq 1, \\ 0 & \text{for } 0 \leq m_{\beta} \leq .5. \end{cases} \quad (4.43)$$

It was determined in 4.3 that no mechanism exists to produce a non-zero average current deviation between capacitors 2 and 3 because the system was defined as a balanced three-phase sinusoidal system with no dc offsets. This precept can be used along with the current definitions in 4.5 to write node equations at each of the capacitor terminals as follows:

$$\bar{I}_{\alpha 4} = \bar{I}_{C4} + \bar{I}_{\beta 4} \quad (4.44)$$

$$\bar{I}_{C4} + \bar{I}_{\alpha 4} = \bar{I}_{C3} + \bar{I}_{\beta 3} \quad (4.45)$$

$$\bar{I}_{C2} + \bar{I}_{\alpha 1} = \bar{I}_{C1} + \bar{I}_{\beta 1} \quad (4.46)$$

$$\bar{I}_{\alpha 0} = \bar{I}_{C1} + \bar{I}_{\beta 0} \quad (4.47)$$

Using the derived average current expressions (4.34) - (4.43) and the node equations at each of the capacitor terminals shown in (4.44) - (4.47), a new model can be formulated that describes the average capacitor current deviations as a function of the back-to-back converter operating points; however, more of the converter system details are first required. An input reactor is required to interface the FE bridge and the three-phase electrical grid with input current control. The FE bridge to grid interface is shown in Figure 4.18 with the input reactor impedances.

The balanced three-phase definitions of the modulator reference signals and the input currents of (4.1) - (4.12) can be leveraged to formulate a positive sequence model of the grid to FE bridge interface as shown in Figure 4.19. For the sake of simplicity, it is assumed that mutual impedances between the input reactor phase legs are all equal.

Using the quantities defined in Figure 4.19, a vector diagram can be constructed that defines the vector space as a function of the input current magnitude and angle as shown in Figure 4.20.

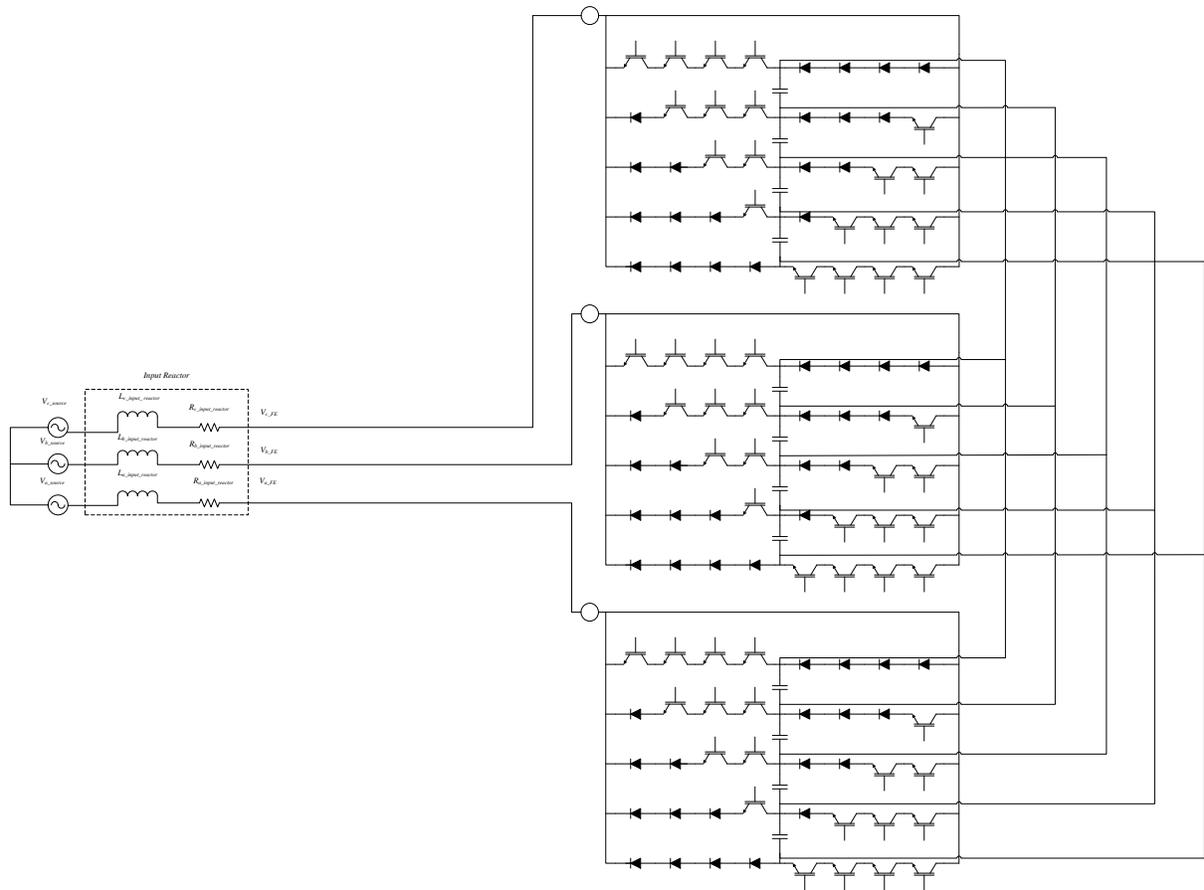


Figure 4.18: FE bridge shown with input reactor and grid voltage

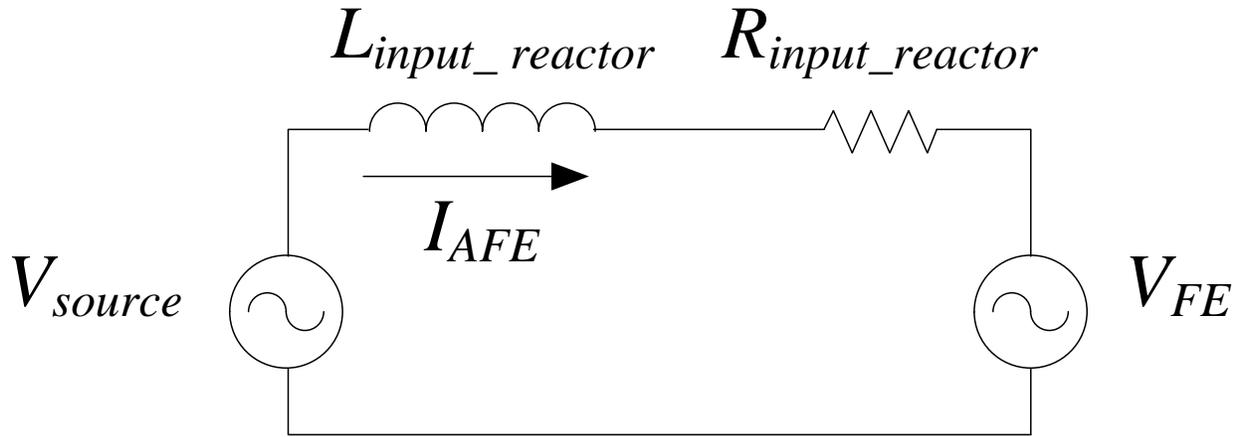


Figure 4.19: Positive Sequence model of FE

A newly derived model uses this vector space definition coupled with the expressions derived in (4.34) through (4.47). The two systems of equations are manipulated and solved simultaneously to map out the two-converter system steady-state operating space for arbitrarily chosen constraints. The model accepts all of the known quantities shown in Figure 4.21 and produces all unknown quantities required to produce an average capacitor current deviation of 0 amps between capacitors 1 and 2 and capacitors 3 and 4. Due to the model symmetry, the average current deviation for capacitors 1 and 2 and capacitors 3 and 4 is always equal.

The model was exercised to study specific steady-state operating spaces subject to various constraints.

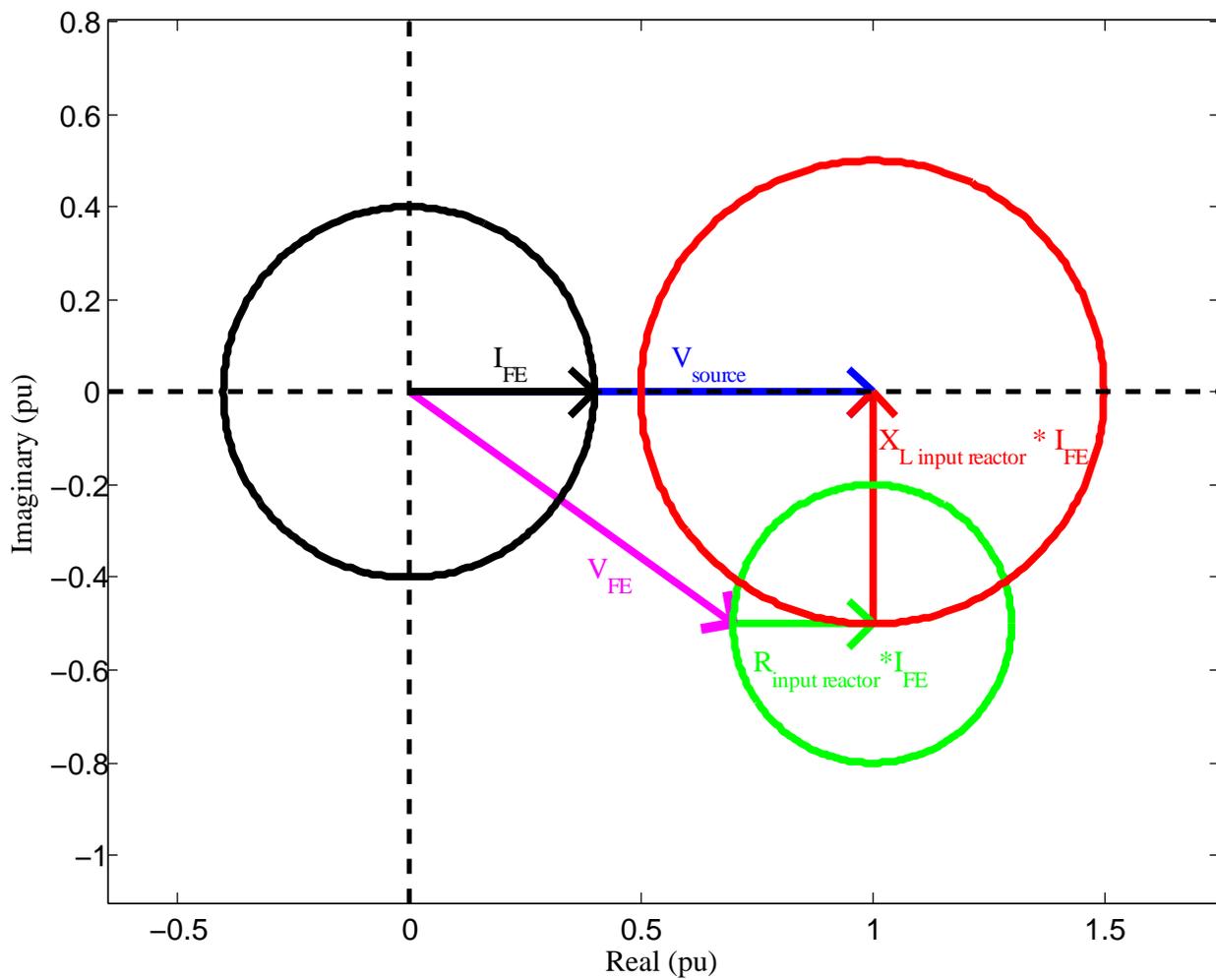


Figure 4.20: Positive Sequence FE vectors

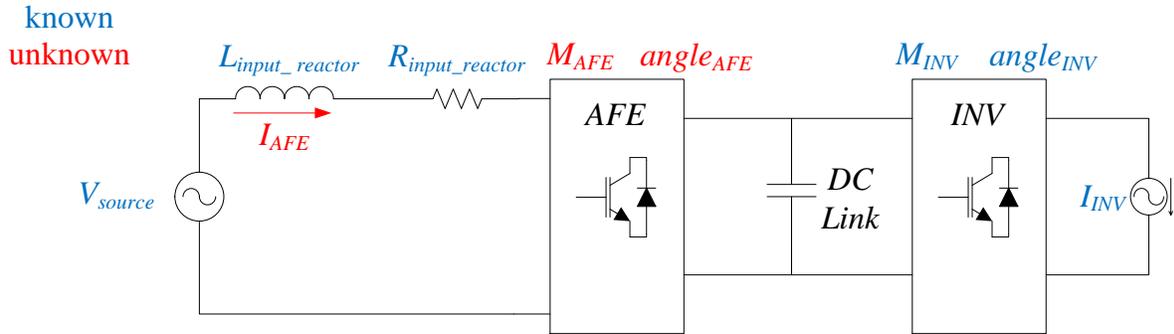


Figure 4.21: Capacitor current deviation model

4.3.1 Induction Motor Drive with Unity Back-End Modulation Depth

Figure 4.22 illustrates the first set of constraints analyzed using the capacitor current deviation model. The constraints model a typical variable frequency drive (VFD) induction motor application. In induction motor drive applications, it is often desired to hold the front-end power factor at a constant value of 1 for all of the induction motor operating space. A back-end power factor of .85 was chosen to model a typical induction motor. Figure 4.22 illustrates the results of this induction motor case.

Figure 4.22 calls for several interesting observations. The results show it is possible to control to zero average capacitor current deviation using only the front-end bridge. The results also show that this control was achieved with a maximum front-end current magnitude of less than 1 pu and a maximum front-end modulation depth of less than or equal to 1 pu. In other words, these achieved results did not violate any safe operating points of the front-end bridge.

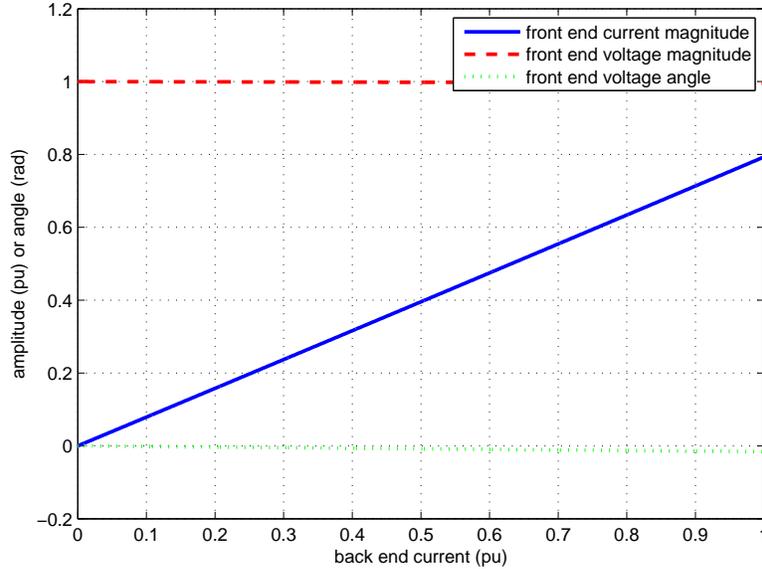


Figure 4.22: FE voltage and current vs. back-end current magnitude to achieve zero capacitor current deviation between all four dc link capacitors

4.3.2 Constant Front-End Power Factor

Figure 4.23 illustrates the second set of constraints analyzed using the capacitor current deviation model. The constraints were chosen to study the effect of sweeping all motoring back-end power factors while constraining the front-end power factor to unity. Figure 4.23 shows the results of the constant front-end power factor case.

4.3.3 Constant Back-End Power Factor

Figure 4.24 illustrates the third set of constraints analyzed using the capacitor current deviation model. The constraints were chosen to study the effect of sweeping all motoring front-end power factors while constraining the back-end power factor to .85. Figure 4.24 illustrate the results of the constant back-end power factor case.

The results illustrated in Figure 4.24 provide crucial insight into the operation of the back-to-back converter system. The front-end bridge was only able to control to zero average

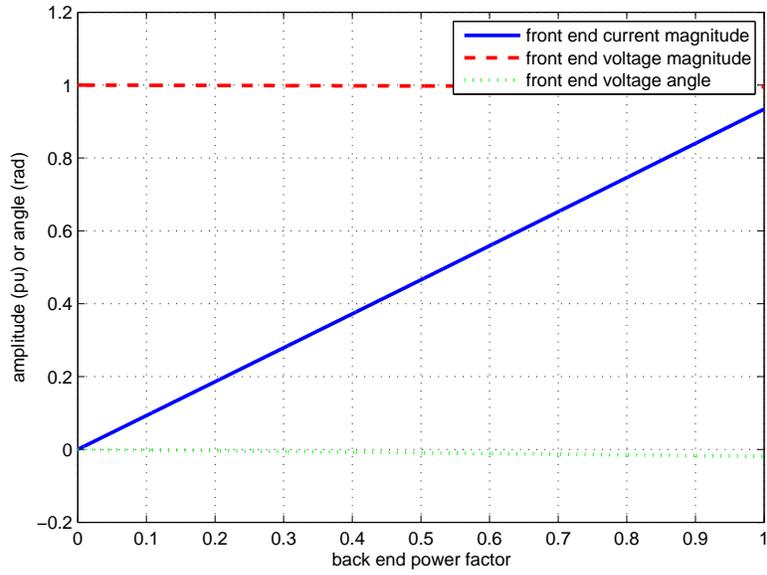


Figure 4.23: FE voltage and current vs. back-end power factor to achieve zero capacitor current deviation between all four dc link capacitors

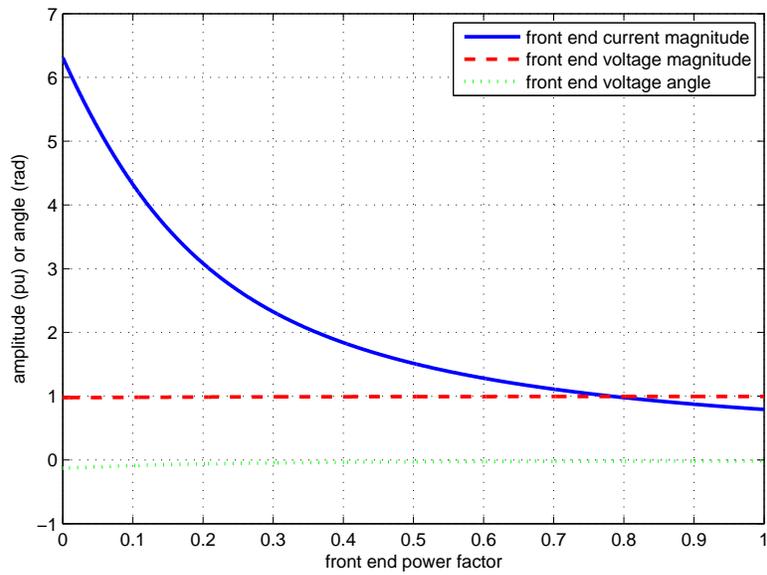


Figure 4.24: FE voltage and current vs. front-end power factor with known back-end operation to achieve zero capacitor current deviation between all four dc link capacitors

capacitor current deviation for low front-end power factors if severe violations in the front-end safe operating areas were made for current. This is because the amount of real power flowing into the system must equal the amount of real power flowing out of the system.

4.3.4 Induction Motor Drive with Variable Modulation Depth

All of the cases studied in 4.3.1 through 4.3.3 assumed a unity modulation depth at the back-end. Because of this, it was possible to control the average current deviation at each dc link capacitor level to zero using only the front-end current controller. Because this converter system is often used for frequency conversion in industrial motor drive applications, it is more interesting to investigate average current deviation at each dc link capacitor for an arbitrary back-end modulation depth and a constant unity power factor at the front-end.

Figure 4.25 illustrates the voltage, current, and power profile for the back-end converter where the converter is being controlled to operate a rotating machine at a constant torque for all back-end modulation depths. In order to model the typical industrial motor drive control strategy, the front-end controller was configured to match back-end real power flow and to keep a constant unity power factor at the front-end for all back-end operating points. The average current deviation was calculated for all constant torque back-end operating points illustrated in Figure 4.25 as a function of back-end frequency. The results of this calculation are illustrated in Figure 4.26. During the calculation, a maximum average current deviation of $43.59A$ was calculated at a back-end frequency of $31.6Hz$ that represents a $.4212pu$ current at the fully rated converter base.

Figure 4.27 illustrates the voltage, current, and power profile for the back-end converter where the converter is being controlled to operate a rotating machine following a typical fan operation profile for all back-end modulation depths. In order to model the typical industrial motor drive control strategy, the front-end controller was configured to match back-end real power flow and to keep a constant unity power factor at the front-end for all fan profile back-end operating points.

The average current deviation was calculated for all fan profile operating points illustrated in 4.27 as a function of back-end frequency. The results of this calculation are illus-

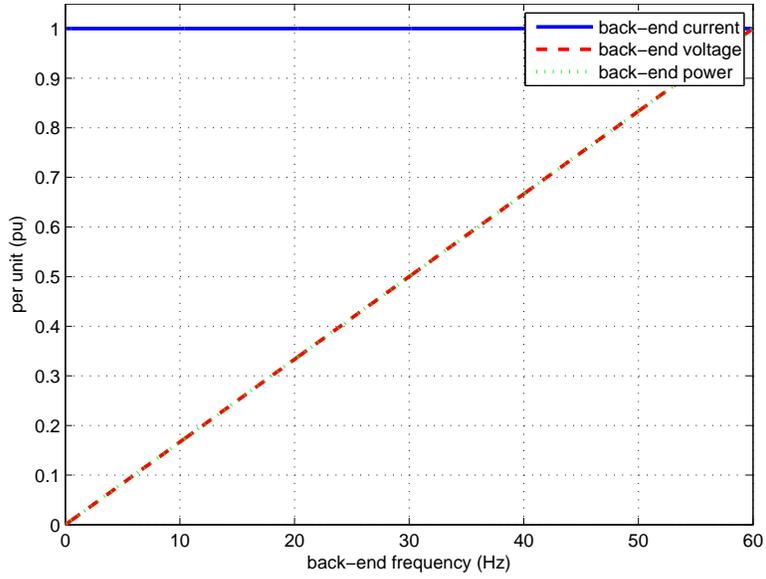


Figure 4.25: BE voltage, current and power vs. BE frequency for a constant torque voltage current BE profile

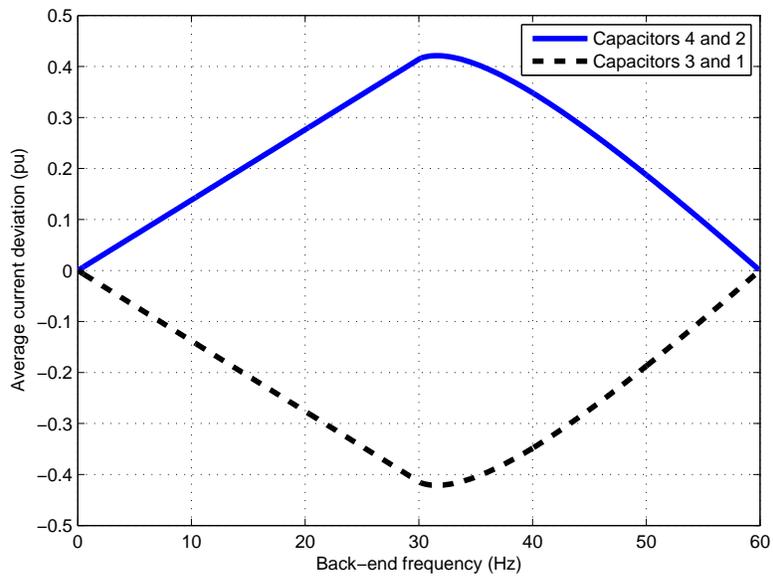


Figure 4.26: Average current deviation vs. BE frequency with BE Modulation Depth = $\frac{\text{BE frequency}}{60}$ and BE current = 1 pu (constant torque profile)

trated in 4.28. During the calculation, a maximum average current deviation of 16.21A was calculated at a back-end frequency of 42.2Hz that represents a .1566pu current at the fully rated converter base.

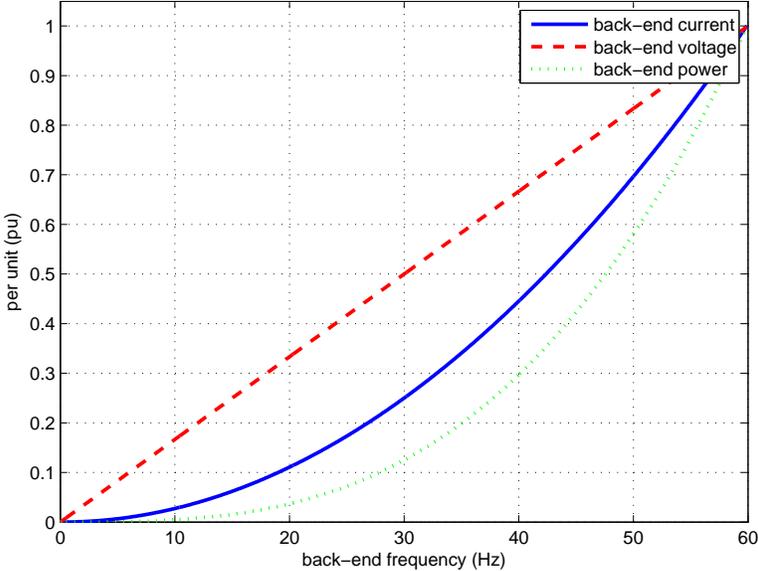


Figure 4.27: BE voltage, current and power vs. BE frequency for a fan/blower BE voltage current profile

The work presented in this section quantified the amount of current deviation observed at the dc link capacitors as an average current deviation. This is a crucial result because the balancing capability of the system can now be modeled and quantified using ideal dc current sources and the mechanisms needed to maintain equal dc link capacitor voltages can now be studied.

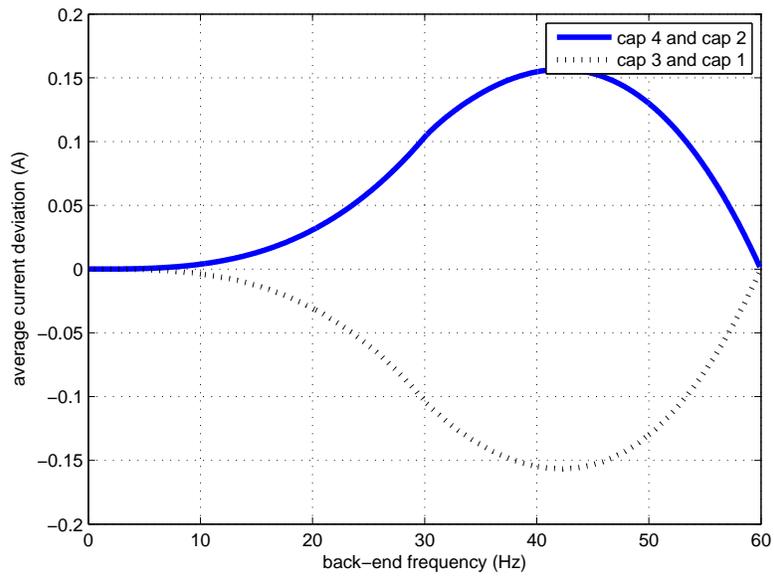


Figure 4.28: Average current deviation vs BE frequency with BE Modulation Depth = $\frac{\text{BE frequency}}{60}$ and BE current = $I_{\text{base}} * (\frac{\text{BE frequency}}{60})^2$ (fan/blower BE voltage current profile)

5.0 SPACE VECTOR MODULATION AND MODIFIED CARRIER BASED PWM

Researchers have offered other mechanisms for controlling average capacitor current deviation. The first mechanism is the use of a modified modulation strategy integrated with a capacitor balancing algorithm [2, 31]. The modified modulation approach exploits the fact that redundant switch states exist for each given phase-to-phase voltage vector. Capacitor balancing decision making is then added to the modulator to choose from a set of redundant switch states that achieves the desired phase-to-phase output voltage while correcting dc link capacitor voltage imbalance. A similar capacitor balancing algorithm can be integrated with both traditional carrier based PWM and space vector modulation (SVM) by intelligently injecting common mode signals into the modulator reference waveform. The injected common mode signal does not change the phase-to-phase output voltage if the saturation limits of the output stage maintain status (no modulation depth greater than unity); however, the injected common mode signal will effectively change which dc link capacitor serves the load current at any given time. Limitations exist when modified modulation strategies are used to maintain capacitor voltage balancing. The inverter system must commute across more than one level to achieve the appropriate output voltages while correcting capacitor voltages using redundant switch states. These level skipping commutation events increase switching losses and increase resonant voltage overshoots in the circuit. More work is required to investigate the modified modulation strategies to achieve capacitor voltage balancing in dynamic scenarios and with varying ranges of input bridge to output bridge power factors to determine the stable operating ranges of these techniques. More work is also required to investigate the viability of applying modified modulation strategies to eliminate the voltage ripple due to power factor mismatch between the input and output bridges.

6.0 CAPACITOR BALANCING CIRCUITS AND ALGORITHMS FOR DIODE FRONT-END CONVERTER SYSTEMS

Separate and independent auxiliary circuits have been proposed to balance dc link capacitor voltages due to average dc link capacitor current deviation in multilevel converters with diode front-ends [1] [2] [3] [4]. In [1], two separate buck-boost converters linking the top two capacitors and bottom two capacitors respectively for a five-level NPC converter system are proposed to correct average capacitor current deviation. Figure 6.1 identifies the proposed balancing circuit.

Drawbacks exist in the balancing scheme proposed in [1] including non-bidirectional capacitor current correction capabilities, no common mode current injection capabilities, and design deviation between the capacitor voltage correction circuit and five-level NPC power stage designs.

In [2], a separate bidirectional balancing circuit proposes to correct dc link voltage imbalance in a five-level NPC converter system. Figure 6.2 is the proposed balancing circuit.

The circuit shown proposed by [2] has several drawbacks. A separate balancing circuit and balancing reactor are required for the top two capacitors and the bottom two capacitors. This implies that dc link capacitor voltage balancing actuation only exists between the top two capacitors and bottom two capacitors respectively. This scheme will work under ideal conditions with no severe common mode current injection requirements; however, the separate balancing circuits do not provide a means of correcting voltage imbalance that exists between the group consisting of the top two capacitors and the group consisting of the bottom two capacitors. The standard 5-level NPC power stage cannot easily construct the proposed balancing circuit. Because of this, separate designs for the 5-level NPC power stage and the auxiliary capacitor balancing circuits would need to be maintained.

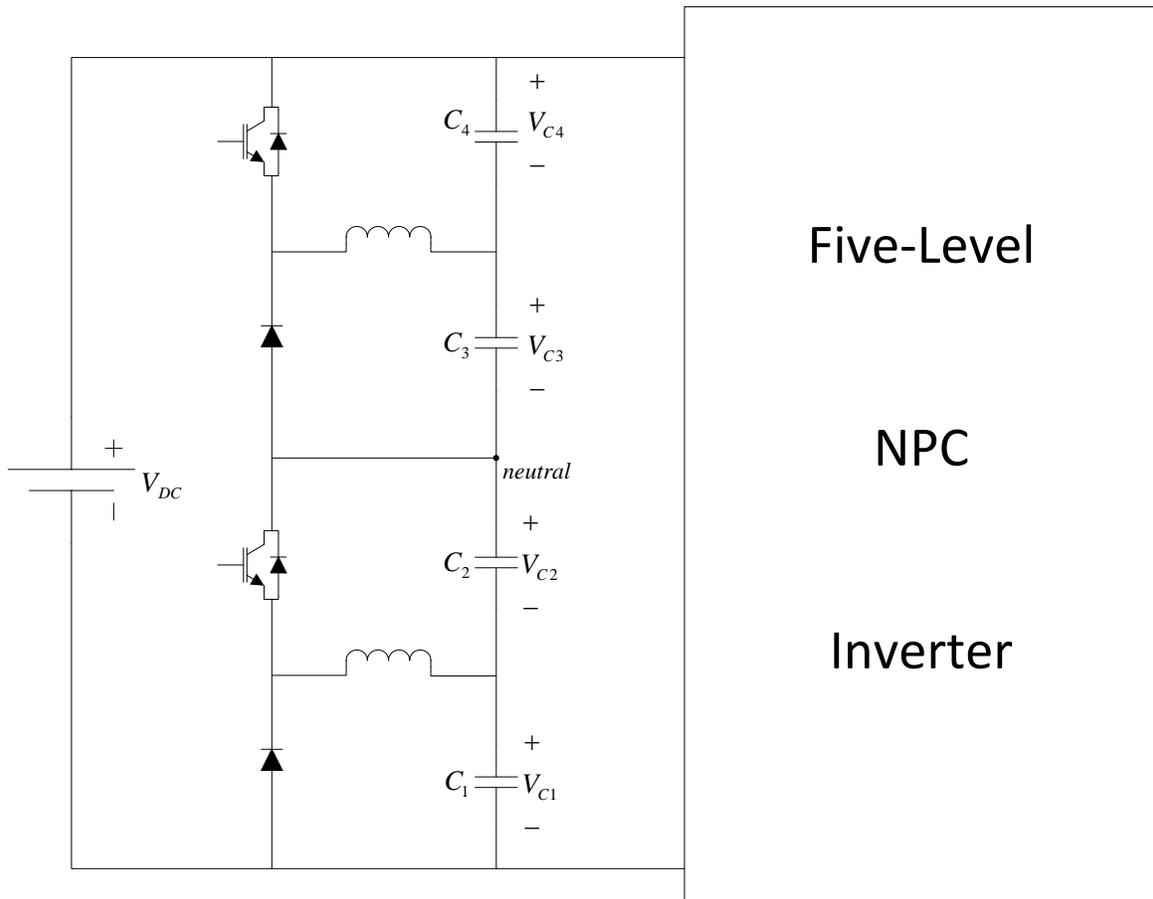


Figure 6.1: Separate buck-boost converters linking the top two capacitors and bottom two capacitors for average dc link capacitor current deviation correction proposed in [1]

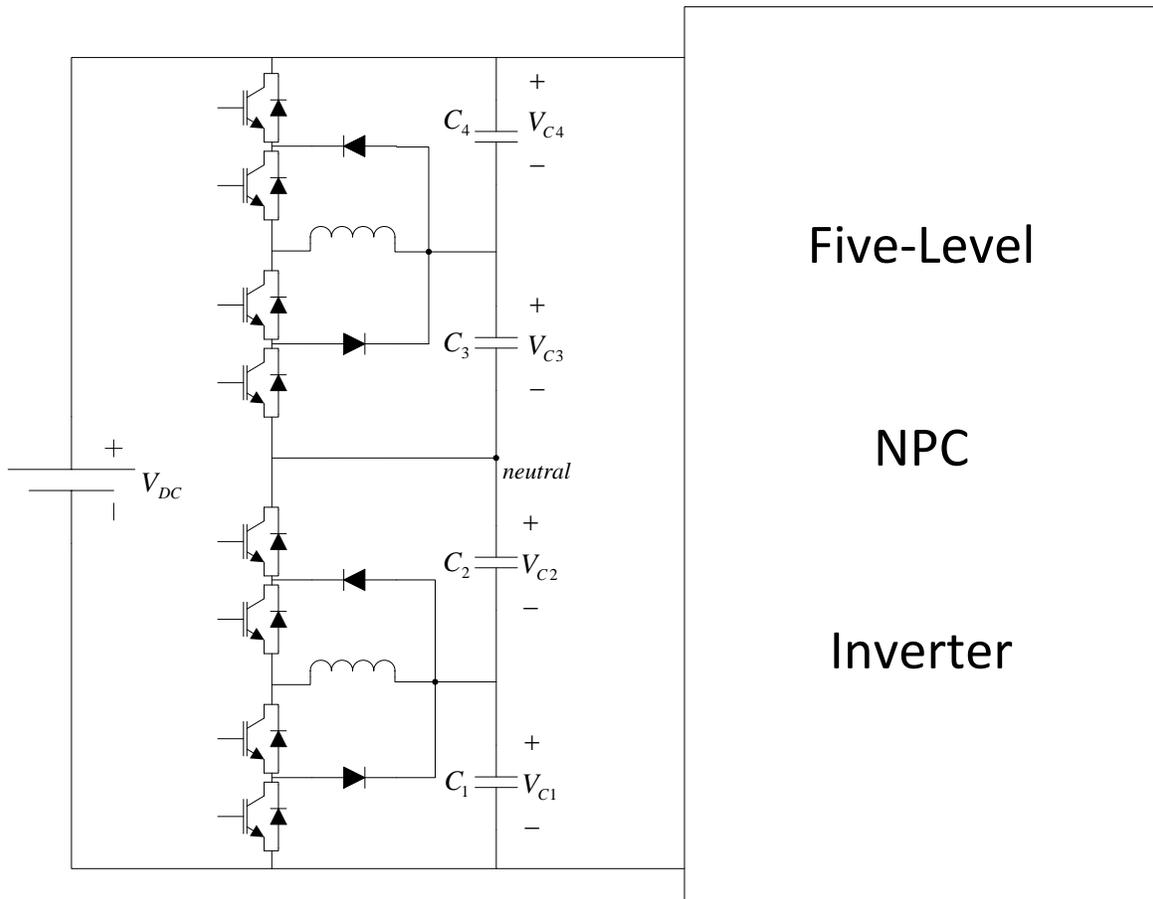


Figure 6.2: Auxiliary dc link capacitor balancing circuit for only the top two capacitor levels proposed in [2]

In [3], a bidirectional dc link capacitor balancing circuit proposes to balance a five-level NPC inverter system that makes use of a coupled-reactor. Figure 6.3 shows the balancing circuit.

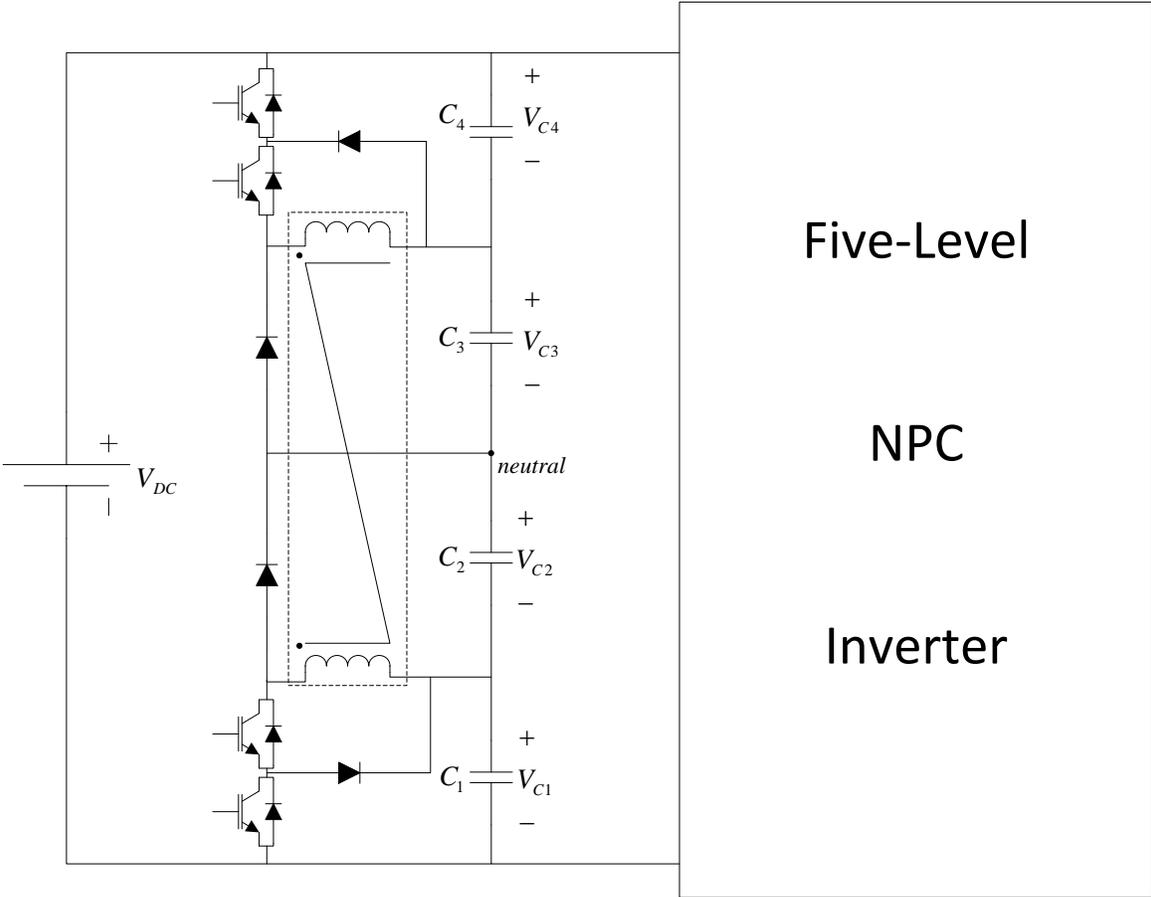


Figure 6.3: Capacitor balancing circuit with coupled reactor proposed in [3]

The balancing circuit proposed in [3] has several advantages including bi-directional correction capabilities and midpoint voltage control capabilities; however, the balancing circuit topology still deviates from the five-level NPC power stage. In [4], a flying-capacitor based chopper circuit is proposed to balance the dc link voltage levels of a five-level NPC inverter system. Figure 6.4 reveals the flying capacitor based balancing circuit.

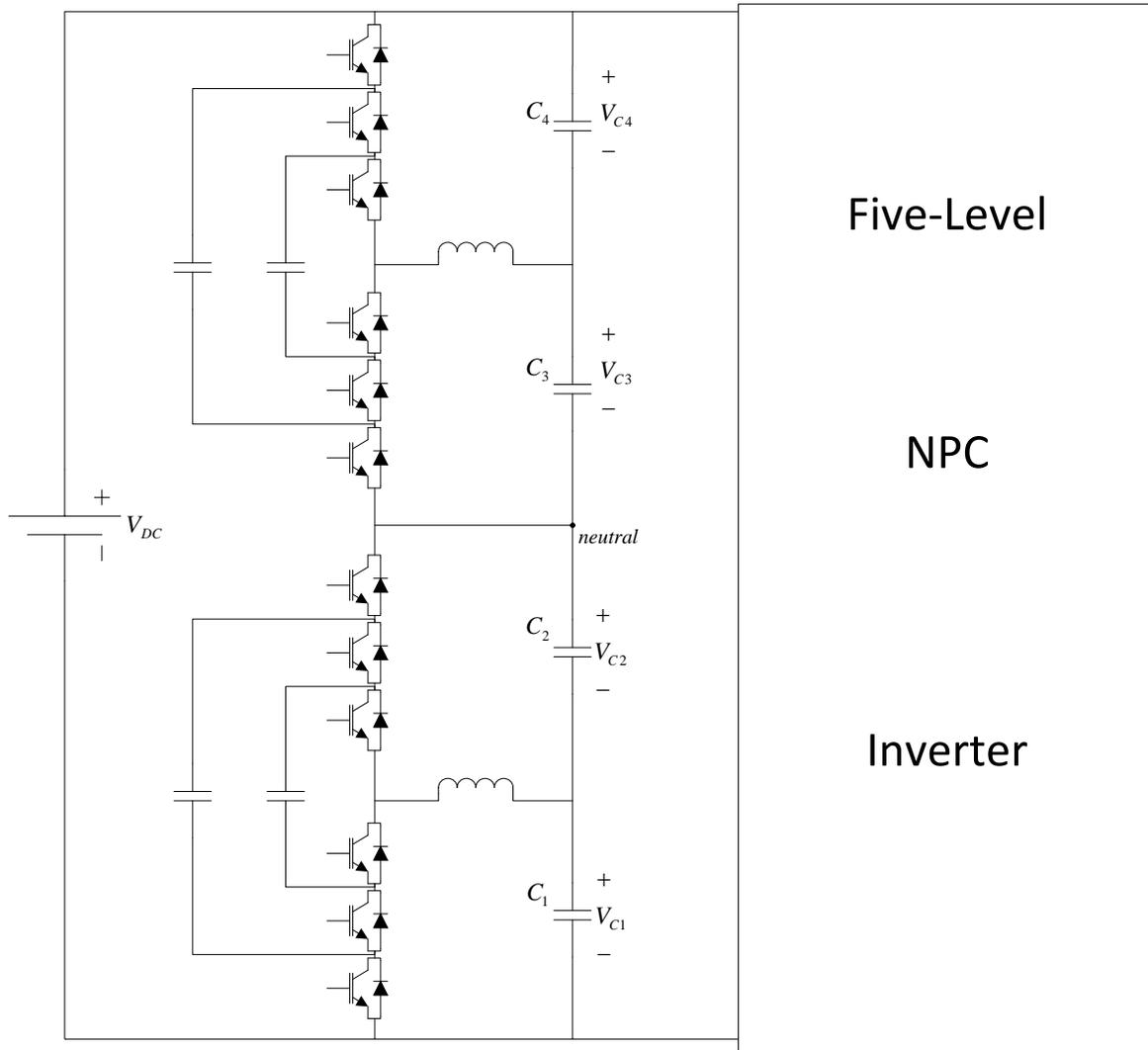


Figure 6.4: Flying-capacitor based dc link voltage balancing circuit proposed in [4]

The balancing circuit proposed in [4] provides effective bidirectional capacitor current deviation correction; however, the added complexities of the flying capacitor voltage balancing coupled with the large deviation in the balancing circuit topology with the five-level NPC power stage makes this scheme unattractive in practical inverter systems.

7.0 A CAPACITOR BALANCING CIRCUIT AND ALGORITHM FOR ACTIVE FRONT-END CONVERTER SYSTEMS

Integrating appropriately designed capacitor balancing auxiliary circuits in back-to-back pulse width modulated converter systems enables mitigation of dc link voltage ripple due to reactive power mismatch and average capacitor current deviation mitigation without the need to commute across multiple levels. This dissertation analyzes a new capacitor balancing circuit for back-to-back five-level NPP converter systems based on the five-level NPPP topology [39]. The five-level NPP topology, along with several other multilevel VSI topologies, can be electrically split by separating the power semiconductors that conduct current into the dc link capacitors and with the power semiconductors that conduct current out of the dc link capacitors as detailed in 4.

The devices that conduct current into the dc link form the capacitor charging circuit, and the devices that conduct current out of the dc link form the capacitor discharging circuit. A balancing reactor wired between the charging and discharging circuit provides an energy buffer that is used to shuttle charge between all dc link capacitors in both directions. Figure 7.1 identifies the auxiliary circuit. An ideal switch model of the auxiliary capacitor balancing circuit for an N -level system is shown in Figure 7.2.

An average current of a single polarity is established in the balancer reactor and is used as both charge and discharge correction current. The reactor serves as an energy buffer between the charge and discharge circuits. The charge and discharge circuits can operate independently if the reactor is sufficiently large using two independent finite state machines. The capacitor charging state machine and the discharging state machines are shown in Figure 7.3 and Figure 7.4 respectively for an N -level system.

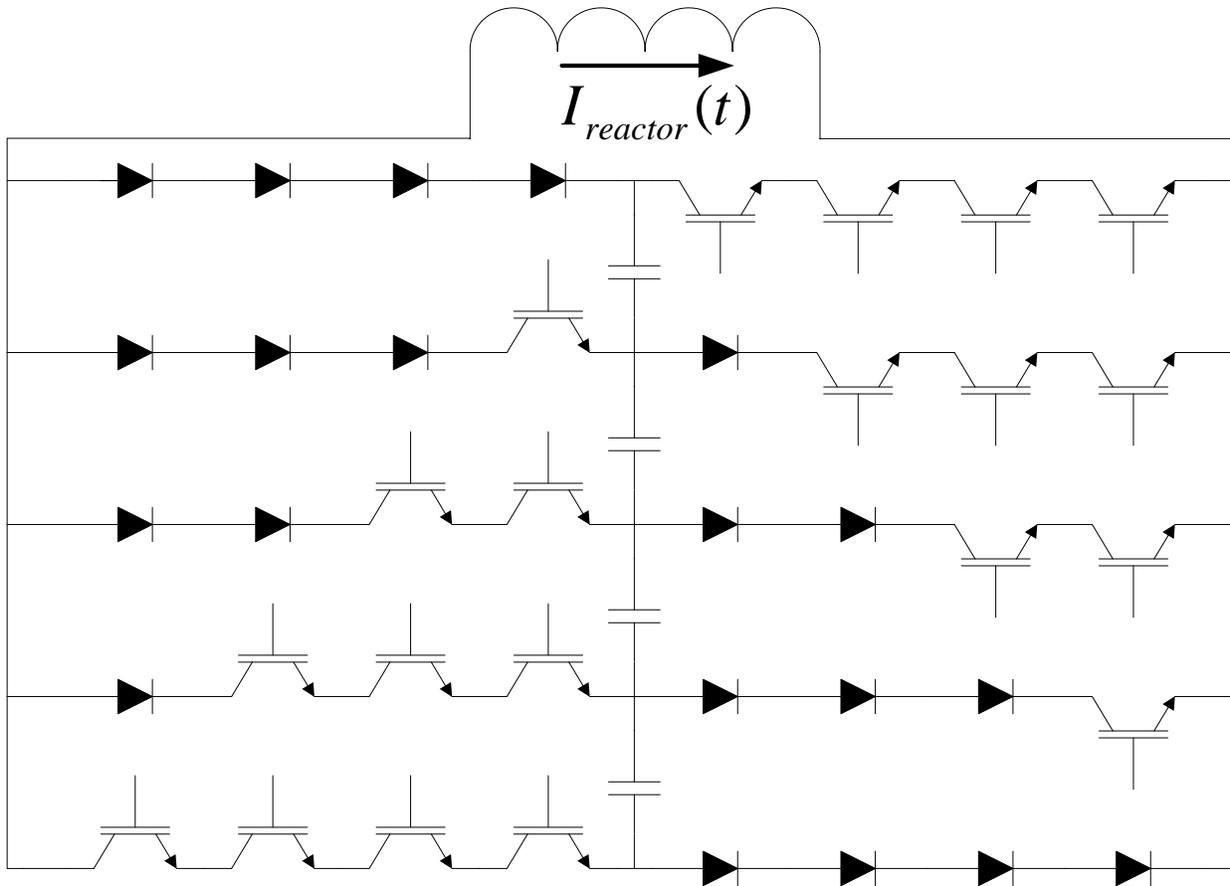


Figure 7.1: Auxiliary capacitor balancing circuit based on five-level NPP topology.

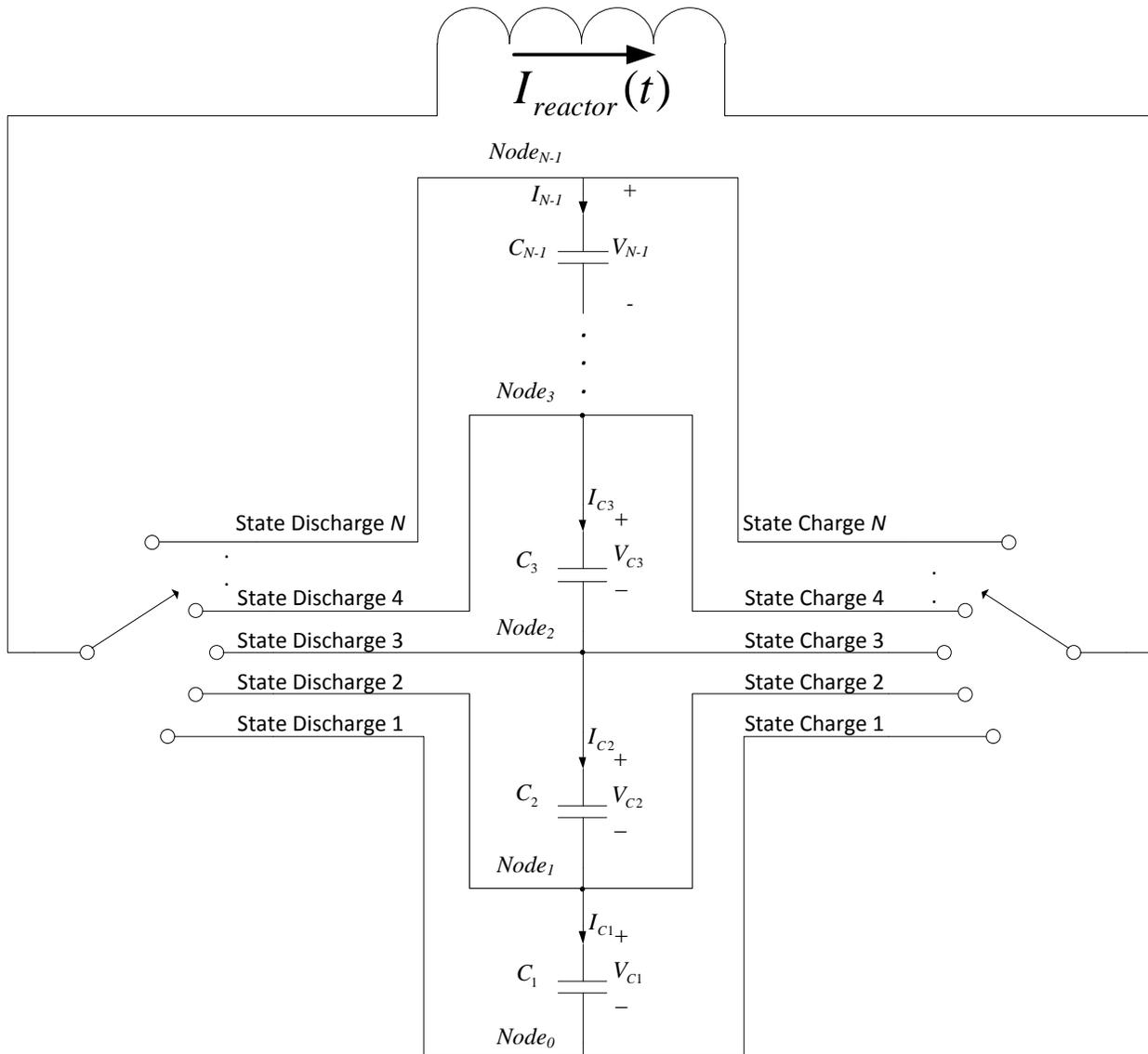


Figure 7.2: Ideal switch model of five-level auxiliary capacitor balancing circuit

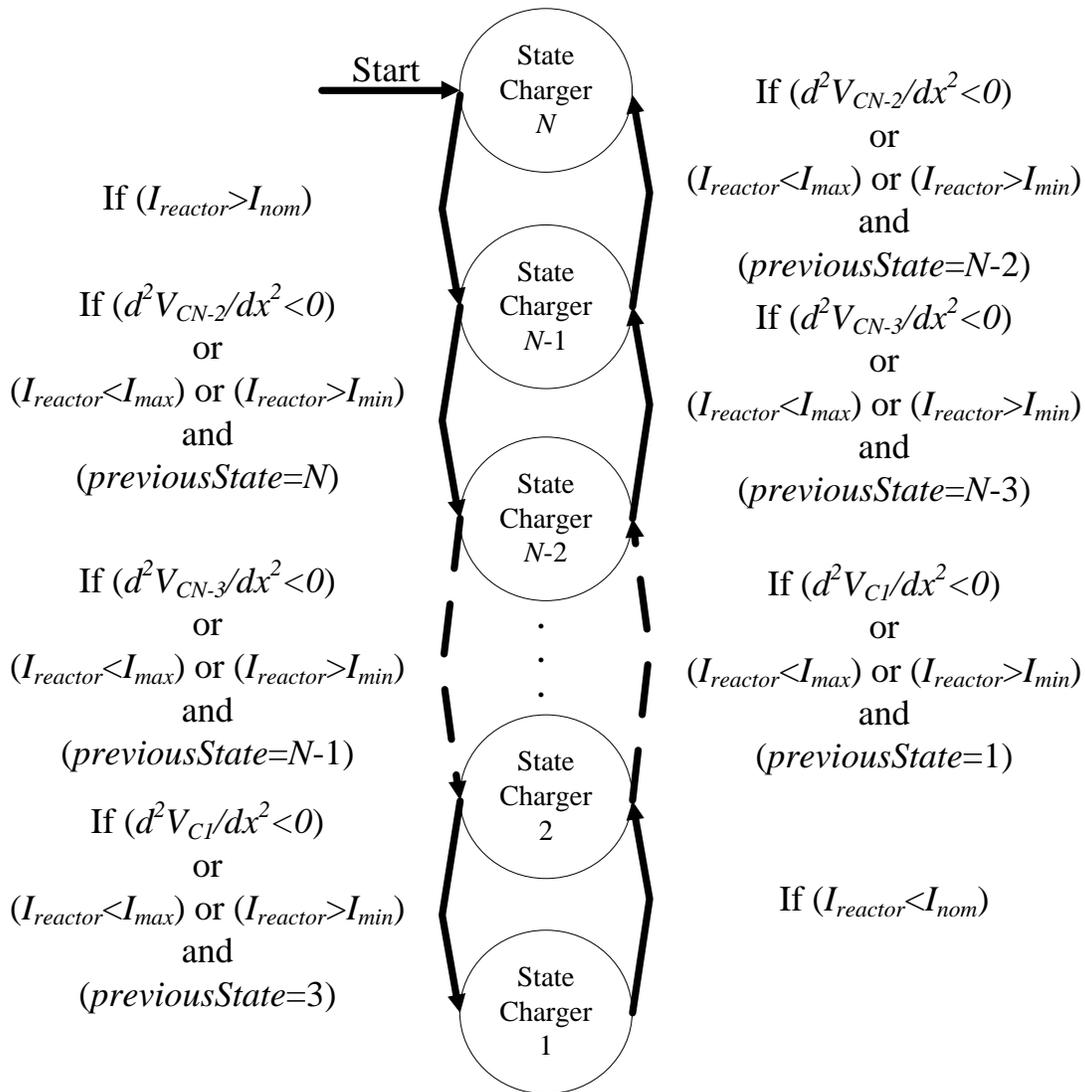


Figure 7.3: Capacitor charging finite state machine.

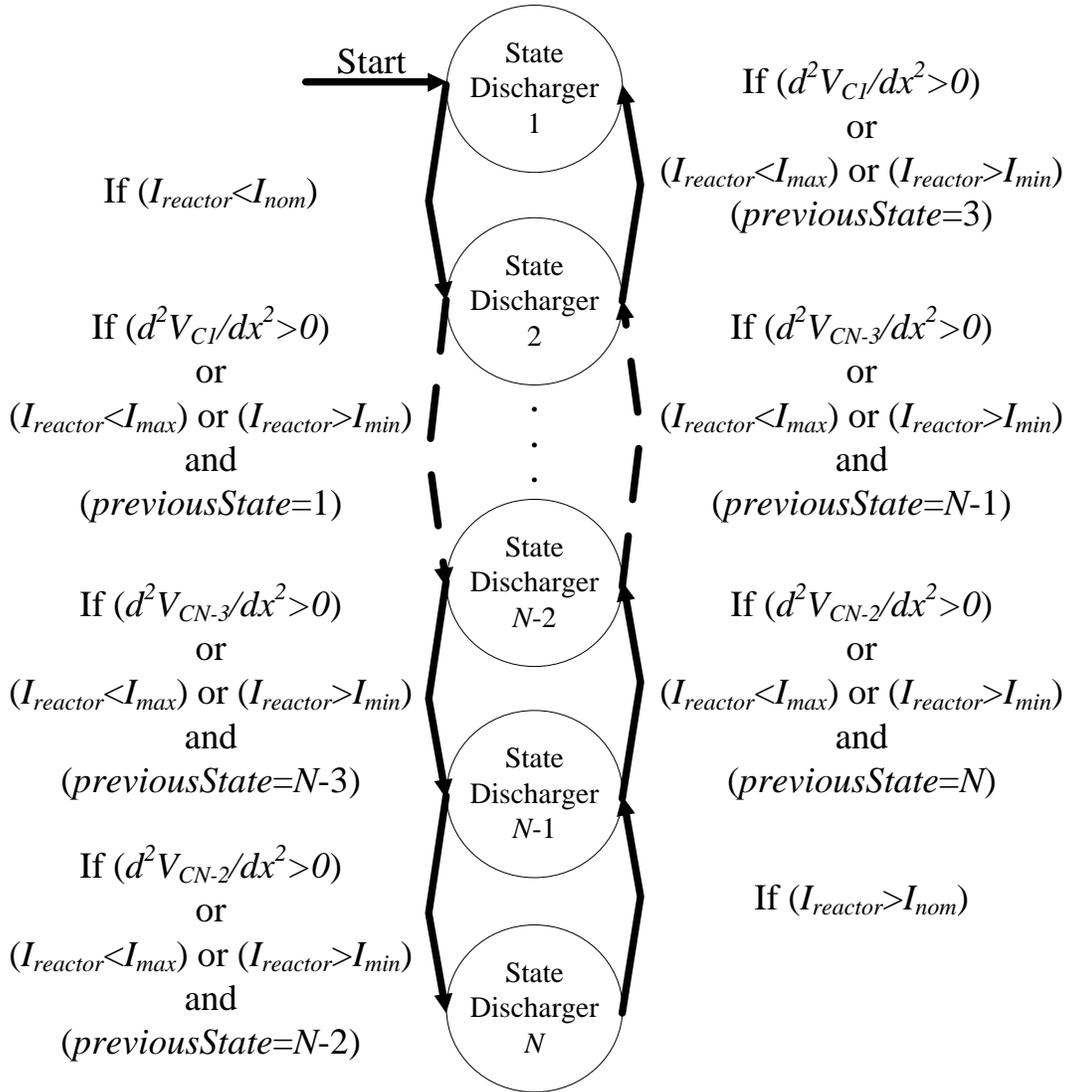


Figure 7.4: Capacitor discharging finite state machine.

Each state machine regulates dc current in the reactor while keeping the dc link capacitors balanced using the second derivative of each capacitor voltage with respect to discrete positions in space. The second derivative of each capacitor is calculated using finite difference theory. (7.1) summarizes the formula.

$$\begin{aligned}
 f_{Node_1} &= V_{Node_0} - 2V_{Node_1} + V_{Node_2} \\
 f_{Node_2} &= V_{Node_1} - 2V_{Node_2} + V_{Node_3} \\
 f_{Node_{N-2}} &= V_{Node_{N-3}} - 2V_{Node_{N-2}} + V_{Node_{N-1}}
 \end{aligned}
 \tag{7.1}$$

8.0 BALANCER AVERAGE CURRENT CAPABILITY STUDY

The results of 4.3 indicate that it would be useful to quantify the dc link capacitor voltage balancing capability of any balancing circuit and algorithm in the form of an average dc link capacitor current deviation. In other words, the capability of a balancing circuit should be measured in terms of the amount of average dc link capacitor current deviation the balancing circuit can overcome before the dc link capacitor voltages are no longer controllable. With this in mind, the capacitor balancing circuit and algorithm presented in 7 can be modeled using the simplified circuit illustrated in Figure 8.1.

The algorithm presented in 4.3 was simulated against the model illustrated in Figure 8.1 to begin to quantify the balancing capability of the algorithm. A series of simulations were formulated to sweep different component values and algorithm set points to experimentally optimize the capacitor balancing system.

8.0.5 I_{delta} Effect on Algorithm and Circuit Balancing Capability

A simulation was conducted in PLECS using the algorithm presented in 4.3 coupled with the circuit illustrated in Figure 8.1 to begin to investigate the optimal I_{max} and I_{min} set points in the algorithm. The I_{max} and I_{min} set points are defined in (8.1).

$$\begin{aligned} I_{max} &= I_{nom} + I_{delta} \\ I_{min} &= I_{nom} - I_{delta} \end{aligned} \tag{8.1}$$

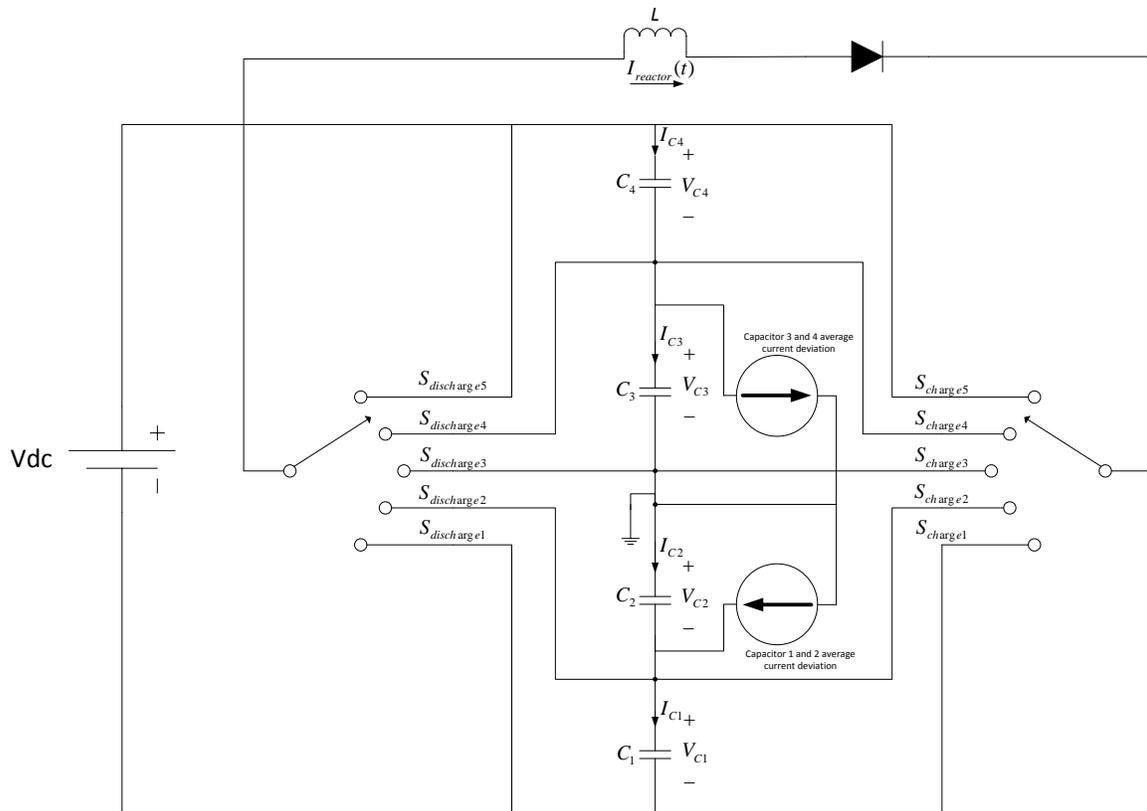


Figure 8.1: Simplified capacitor balancing circuit using ideal dc current sources version 1.

All circuit parameters and algorithm set points were configured with the values given in 8.1.

Table 8.1: Simulation parameter set points used to produce the simulation results illustrated in Figure 8.2

Simulation Parameters	Setting
C_1	$830\mu F$
C_2	$830\mu F$
C_3	$830\mu F$
C_4	$830\mu F$
L	$12mH$
I_{nom}	$35A$
I_{delta}	$.5A$ to $35A$

The simulation was configured to sweep I_{delta} values from $.5A$ to I_{nom} and determine the balancing capability of the system at each point in an attempt to identify the optimal I_{delta} value or value of I_{delta} that produces the largest balancer capability for this particular system configuration. The results of this simulation are shown in Figure 8.2. A maximum balancer capability of $21A$ was achieved for I_{delta} between $2A$ and $5.5A$.

In an effort to confirm that the dc link capacitance value of the system does not affect the balancing capability of a particular set of algorithm set points and balancing circuit parameters, another simulation was conducted with identical parameters except that the dc link capacitance was doubled per level. All circuit parameters and algorithm set points were configured with the values given in Table 8.2.

The results of this simulation are illustrated in Figure 8.3. These results are consistent with the dc link capacitance not affecting the performance of a particular set of algorithm set points and balancing circuit parameters. This is intuitive because the current deviation due to front-end and back-end operating point mismatches has previously been proven to be an average current deviation and this average current deviation needs to be compensated regardless of the size of the dc link capacitance.

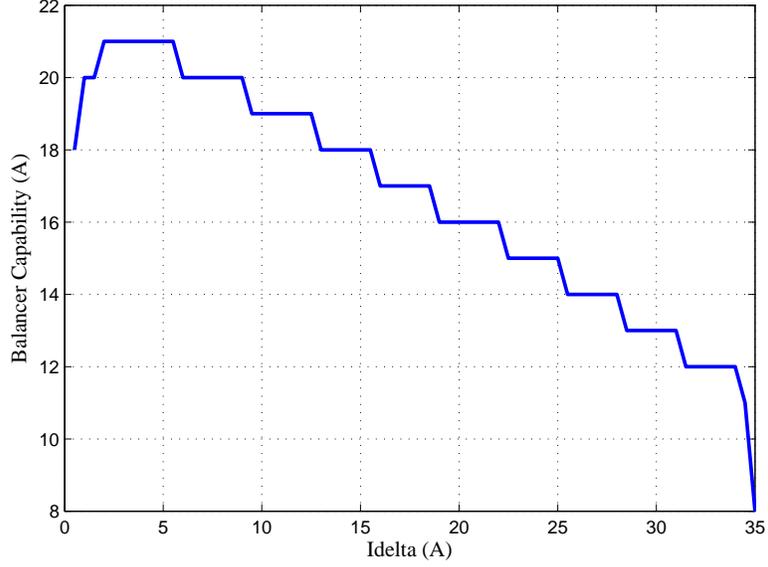


Figure 8.2: Algorithm and Circuit Balancing Capability as a function of the I_{delta} set point in the capacitor balancing algorithm for dc link capacitance = $830\mu F$, $I_{nom} = 35A$, $L = 12mH$.

Table 8.2: Simulation parameter set points used to produce the simulation results illustrated in Figure 8.3

Simulation Parameters	Setting
C_1	$1660\mu F$
C_2	$1660\mu F$
C_3	$1660\mu F$
C_4	$1660\mu F$
L	$12mH$
I_{nom}	$35A$
I_{delta}	$.5A$ to $35A$

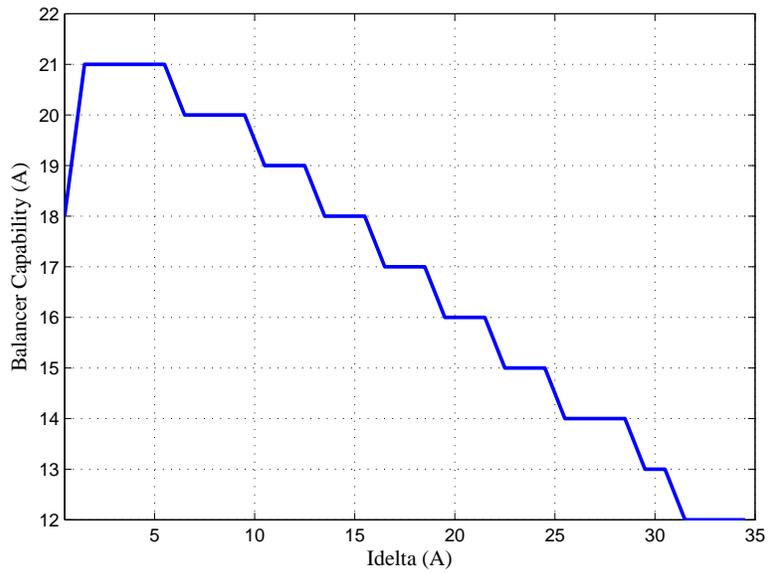


Figure 8.3: Algorithm and Circuit Balancing Capability as a function of the I_{delta} set point in the capacitor balancing algorithm for dc link capacitance = $1660\mu F$, $I_{nom} = 35A$, $L = 12mH$.

In an effort to investigate the effect of the balancing reactor size on the balancing capability of a particular set of algorithm set points and balancing circuit parameters, another simulation was conducted with identical parameters as given in Table 5 except that the balancing reactor inductance was doubled. All circuit parameters and algorithm set points were configured with the values given in Table 8.3. The results of this simulation are illustrated in Figure 8.4.

Table 8.3: Simulation parameter set points used to produce the simulation results illustrated in Figure 8.4

Simulation Parameters	Setting
C_1	$830\mu F$
C_2	$830\mu F$
C_3	$830\mu F$
C_4	$830\mu F$
L	$24mH$
I_{nom}	$35A$
I_{delta}	$.5A$ to $35A$

8.0.6 DC Link Capacitance Effect on Algorithm and Circuit Balancing Capability

Through the simulation efforts presented in 8.0.5, it was shown that for a given L and I_{nom} , the maximum balancing capability is achieved when I_{delta} is between $2A$ and $5.5A$. To show the size of the dc link capacitance does not have an effect on the balancing capability of a particular balancing circuit and algorithm set point configuration due to the average current deviation nature of back-to-back PWM converters, a simulation was conducted that swept from the dc link capacitance from $6.25\mu F$ to $51200\mu F$. All circuit parameters and algorithm set points were configured with the values given in Table 8.4.

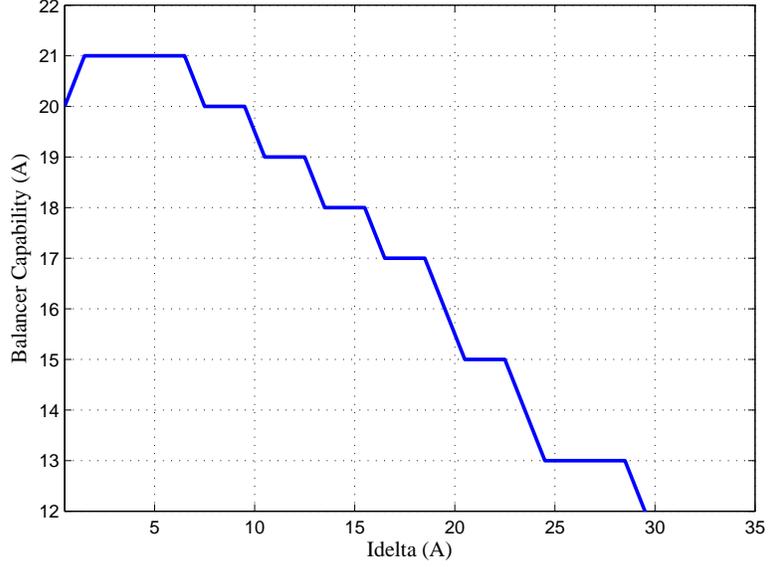


Figure 8.4: Algorithm and Circuit Balancing Capability as a function of the I_{delta} set point in the capacitor balancing algorithm for dc link capacitance = $830\mu F$, $I_{nom} = 35A$, $L = 24mH$.

Table 8.4: Simulation parameter set points used to produce the simulation results illustrated in Figure 8.5

Simulation Parameters	Setting
C_1	$6.25\mu F$ to $51200\mu F$
C_2	$6.25\mu F$ to $51200\mu F$
C_3	$6.25\mu F$ to $51200\mu F$
C_4	$6.25\mu F$ to $51200\mu F$
L	$12mH$
I_{nom}	$35A$
I_{delta}	$3.5A$

The results of this simulation are illustrated in Figure 8.5. It is clear that even when several orders of magnitude of dc link capacitance are swept for a given circuit and algorithm configuration, the size of the capacitance does not have an effect on the balancing capability of the configuration.

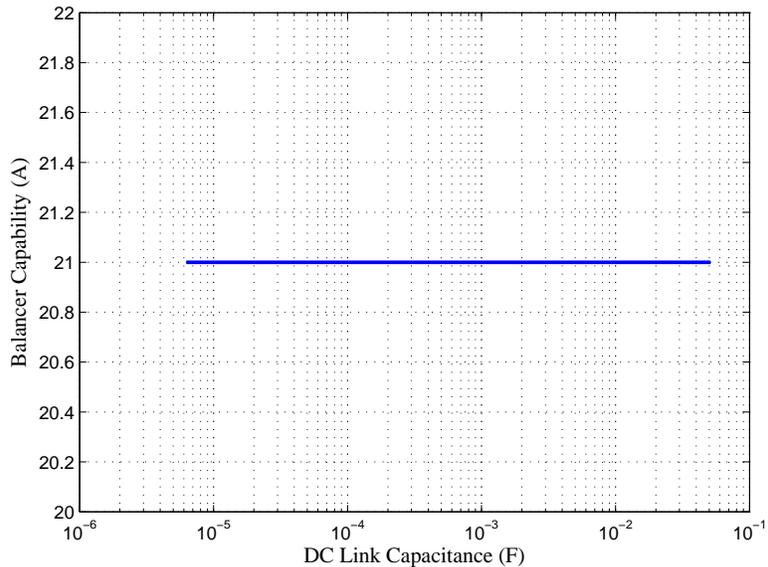


Figure 8.5: Algorithm and Circuit Balancing Capability as a function of the dc link capacitance value in the circuit.

8.0.7 Balancing Reactor Inductance Effect on Algorithm and Circuit Balancing Capability

In an effort to investigate the balancing reactor inductance effect on the algorithm and circuit balancing capability, a simulation was conducted that swept through several orders of magnitudes of balancing inductance with a constant I_{nom} , I_{delta} and dc link capacitance. It is clear that the balancing capability of the combined algorithm and balancing circuit are dependent on balancing reactor inductance. It is intuitive that I_{delta} needs optimized for a given balancing inductance. All circuit parameters and algorithm set points were configured with the values given in Table 8.5.

Table 8.5: Simulation parameter set points used to produce the simulation results illustrated in Figure 8.6

Simulation Parameters		Setting
C_1		$830\mu F$
C_2		$830\mu F$
C_3		$830\mu F$
C_4		$830\mu F$
L	$62.5\mu H$ to $2096.6H$	
I_{nom}		$35A$
I_{delta}		$3A$

The results of the simulation are illustrated in Figure 8.6. The results of the simulation are not intuitive. The balancing capability curve as a function of balancing reactor inductance has a normal distribution shape. Most interestingly, more balancing inductance does not necessarily mean more balancing capability. More investigation is required to understand the effect of balancing reactor inductance on the overall system performance.

Given the results of the balancing reactor inductance sweep illustrated in Figure 8.6, a simulation was created to investigate the effects of the I_{delta} set point for a very large balancing reactor inductance. All circuit parameters and algorithm set points were configured with the values given in Table 8.6. The results of this simulation are illustrated in Figure 8.7. These results indicate that the I_{delta} set point does not have any effect on the balancing capability of the system for a very large balancing reactor inductance. More investigation is required to understand the effect of balancing reactor inductance on the overall system performance.

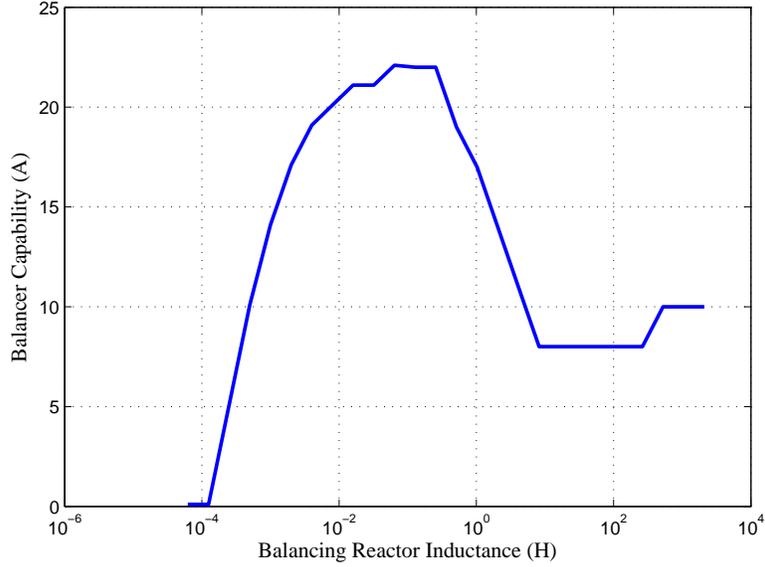


Figure 8.6: Algorithm and Circuit Balancing Capability as a function of the balancing reactor inductance value in the circuit.

Table 8.6: Simulation parameter set points used to produce the simulation results illustrated in Figure 8.7

Simulation Parameters	Setting
C_1	$830\mu F$
C_2	$830\mu F$
C_3	$830\mu F$
C_4	$830\mu F$
L	$2096.6H$
I_{nom}	$35A$
I_{delta}	$.5A$ to $35A$

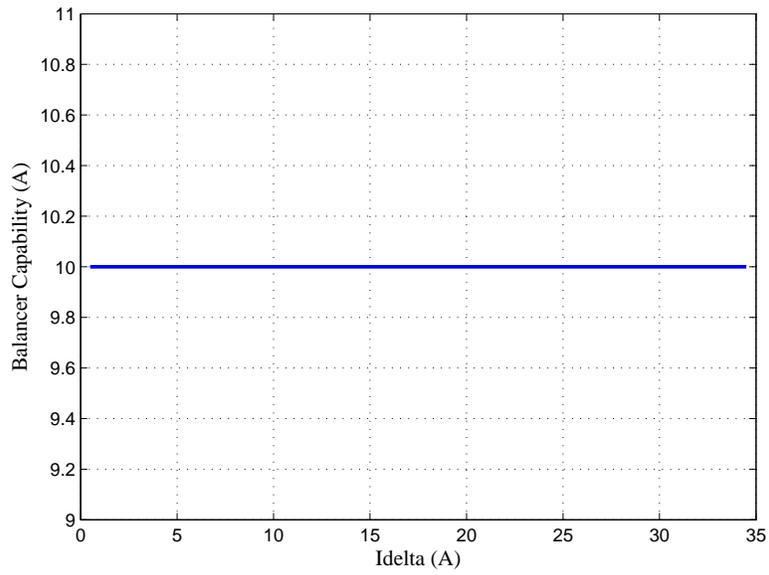


Figure 8.7: Algorithm and Circuit Balancing Capability as a function of the I_{delta} set point in the capacitor balancing algorithm for dc link capacitance = $830\mu F$, $I_{nom} = 35A$, $L = 2096.6H$.

8.0.8 I_{nom} Effect on Algorithm and Circuit Balancing Capability

In an effort to investigate the I_{nom} set point effect on the algorithm and circuit balancing capability, a simulation was conducted that swept through I_{nom} with a constant balancing reactor inductance, I_{delta} and dc link capacitance. The parameters used in the simulation are summarized in Table 8.7 and the results of this simulation are illustrated in Figure 8.8.

Table 8.7: Simulation parameter set points used to produce the simulation results illustrated in Figure 8.8

Simulation Parameters	Setting
C_1	$830\mu F$
C_2	$830\mu F$
C_3	$830\mu F$
C_4	$830\mu F$
L	$2096.6H$
I_{nom}	$5A$ to $100A$
I_{delta}	$3.5A$

These results indicate that the balancing capability of the system increases linearly with I_{nom} . More investigation is required to determine if this relationship holds true for all values of balancing reactor inductance, I_{delta} and dc link capacitance.

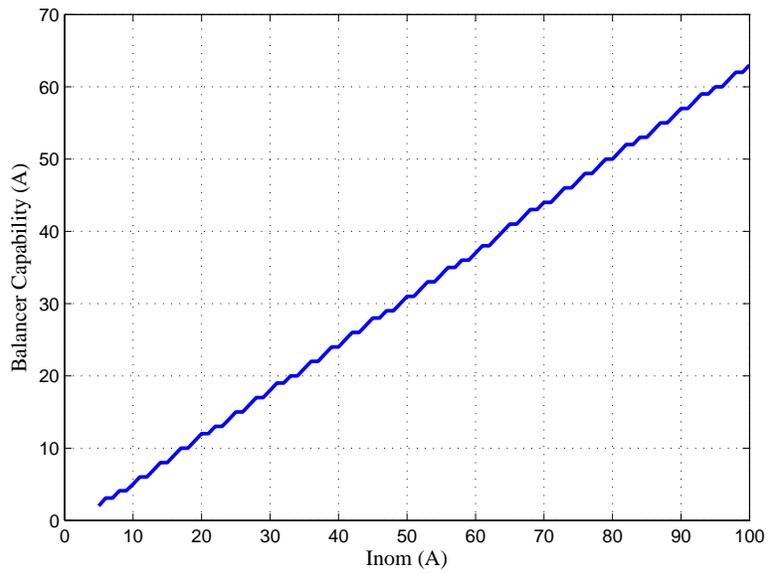


Figure 8.8: Algorithm and Circuit Balancing Capability as a function of the I_{nom} set point in the capacitor balancing algorithm for dc link capacitance = $830\mu F$, $I_{delta} = 3.5A$, $L = 12mH$.

9.0 IGBT GATE-DRIVE

A medium-voltage converter constructed as we propose requires the use of a gate-drive system that is low-cost, highly synchronized, and capable of overdriving the gates.

Each switching device or device group requires an isolated gate-drive. A large number may be required depending on the individual device rating, number of voltage levels in the power stage, and the overall voltage rating of the system. Traditional isolated gate-drive systems for series connected semiconductor modules make use of a costly isolated power supply and fiber optic connection for each device instance [50], driving the need for a low cost alternative.

When using series connected devices, the gate-drive system must be carefully designed to manage voltage imbalance during turn-on and turn-off events. The system must be tightly synchronized and overdrive the gates to account for any mismatch in the physical characteristics of the power semiconductors [51]. Methods for driving series connected devices using gate side control including synchronization [26, 27], and active voltage control [24, 25, 28]. These techniques are not well suited for this application due to high cost and complexity.

A magnetically-coupled, current-sourced gate-drive system [29] can be used to achieve all technical requirements while minimizing cost and complexity, as illustrated in Figure 9.1. The gate-drive system for k devices in series is comprised of a micro-controller (μC) to create turn-on and turn-off logic signals, a pulse amplifier circuit to create positive and negative current pulses, a pulse transformer string, and the pulse receivers that drive each gate.

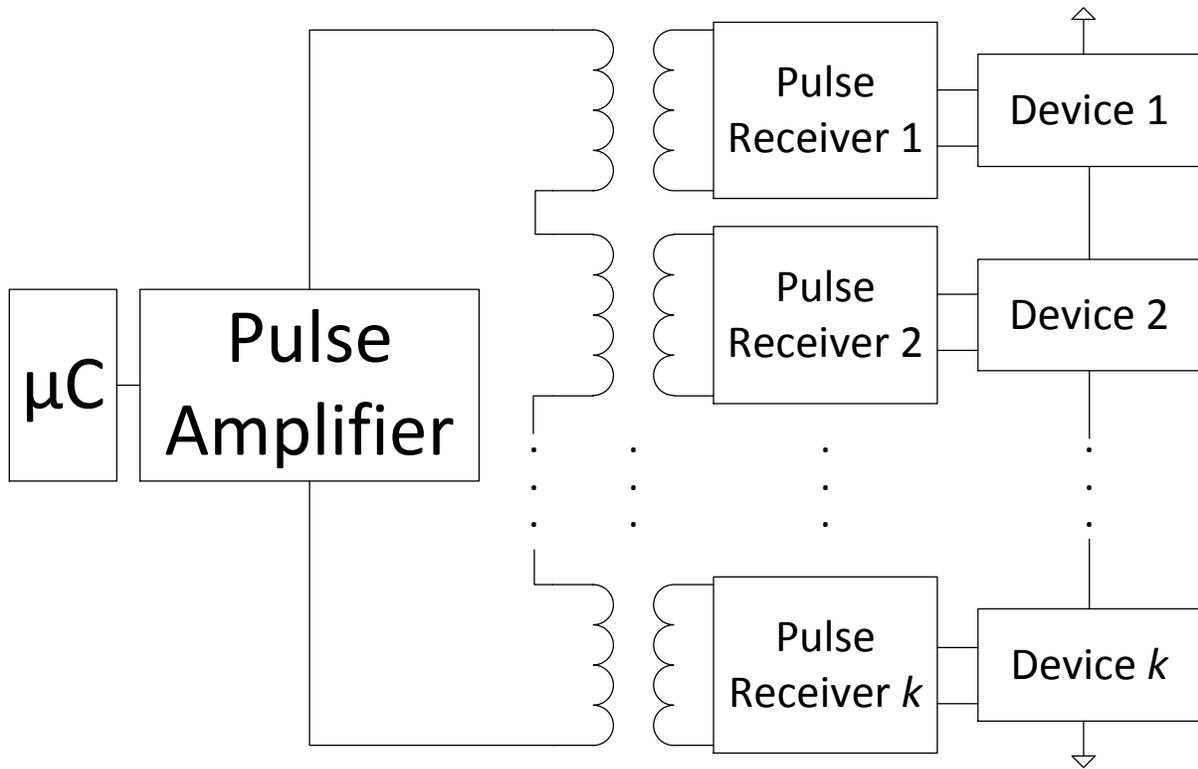


Figure 9.1: Magnetically coupled, current-sourced, gate-oxide insulated device gate-drive system for k devices in series commanded by a micro-controller (μC).

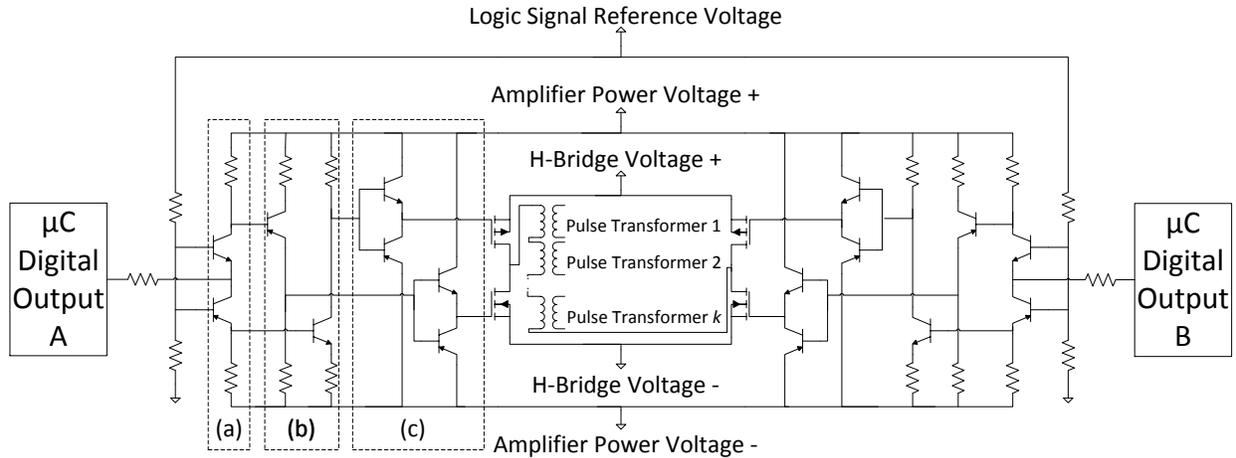


Figure 9.2: Pulse amplifier network.

9.1 PULSE AMPLIFIER

The pulse amplifier level shifts, inverts, and buffers the micro-controller gate signals so they can drive a MOSFET H-bridge that creates current pulses. The pulse amplifier is a series of bipolar junction transistor amplifier stages cascaded together as shown in Figure 9.2. The first stage of the pulse amplifier is a common-base stage Figure 9.2(a). This stage is driven by a micro-controller digital output to level shift the voltage signals from micro-controller voltage levels to H-bridge voltage levels. The second stage in the pulse amplifier is a common-emitter amplifier Figure 9.2(b). The common-emitter amplifier refers the output voltage of the common-base amplifier to the opposite power rail. The third stage of the pulse amplifier is an emitter-follower amplifier Figure 9.2(c). This stage is used to reduce the effective gating resistance of the MOSFET devices in the H-bridge to achieve adequate switching times while minimizing switching loss in the H-bridge.

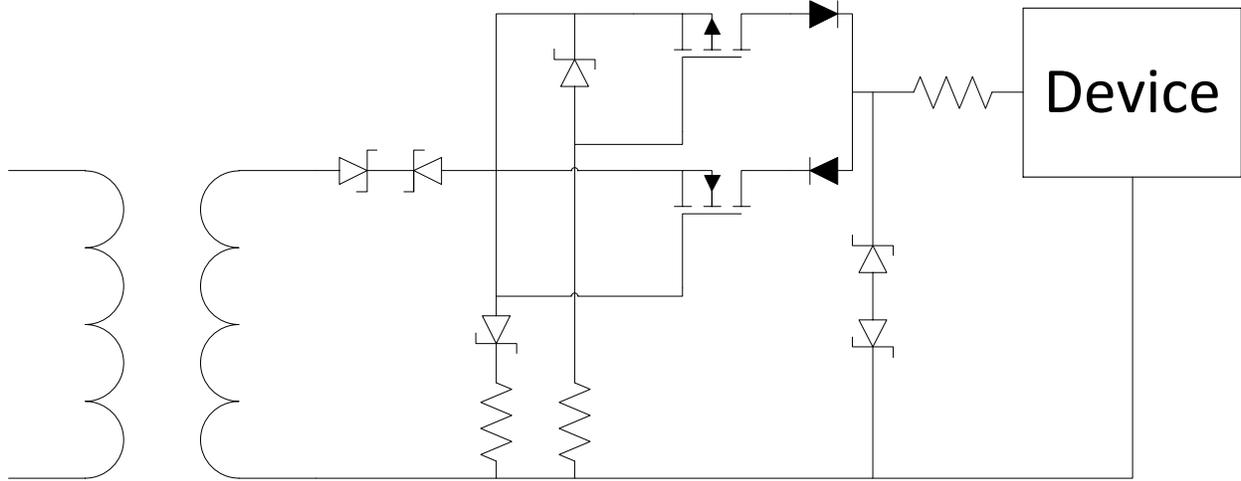


Figure 9.3: Pulse receiver network.

The MOSFET H-bridge is controlled to set up turn-on and turn-off current pulses on a network of pulse transformers for the power stage semiconductor devices. The primary windings of each pulse transformer are wired in series to ensure that the current pulses reflected to the secondary of each pulse transformer are identical. This enables the series connected devices within a device group to synchronously gate and ensure each device will share dynamic voltage evenly during the turn-on and turn-off events.

9.2 PULSE RECEIVER

Each power stage semiconductor device or parallel device group has an associated pulse receiver. The pulse receiver receives the commanded current pulse, sets up the appropriate gate voltage, and latches the commanded gate voltage of the device, as illustrated in Figure 9.3. The pulse receiver consists of MOSFETs and zener diodes that form a synchronous rectifier.

This circuit rectifies a turn-on (positive) current pulse to establish a positive gate voltage when a positive voltage is applied to the pulse transformer secondary, and a negative gate

voltage for a negative current pulse. During a turn-on current pulse, the N-channel MOSFET is not conducting and the P-channel MOSFET conducts until the current pulse decays to zero. At this time, the gate voltage has reached the appropriate turn-on level set by the bidirectional zener diode avalanche voltage. After the current pulse decays to zero, the P-channel MOSFET stops conducting and there is no longer a path for current to flow into or out of the gate of the device, therefore the gate is latched on. The process is similar but opposite during a turn-off current pulse. Figure 9.4 and Figure 9.5 illustrate scope captures of the synchronized gate to emitter voltage of two series connected IGBTs during a turn-on and turn-off event along with the corresponding pulse amplifier MOSFET H-bridge output voltage and current.

The power semiconductor device gate must be periodically refreshed on and off to keep the device in a desired state. The latched gate voltage of the device falls over time due to leakage current in the device gate-oxide layer and the pulse receiver. These refresh on and off current pulses are of the same polarity as their corresponding turn-on and turn-off pulses, but they can be shorter in duration.

To achieve a current-sourced gate-drive and reliably over-drive the devices, the pulse transformer turns ratio must be set so that the back EMF reflected from the device gates to the H-bridge is small compared to the H-bridge supply voltage. Galvanic isolation between the pulse transformer primary and secondary windings is achieved by using high-voltage silicon jacketed wire for the primary winding as shown in Figure 9.6.

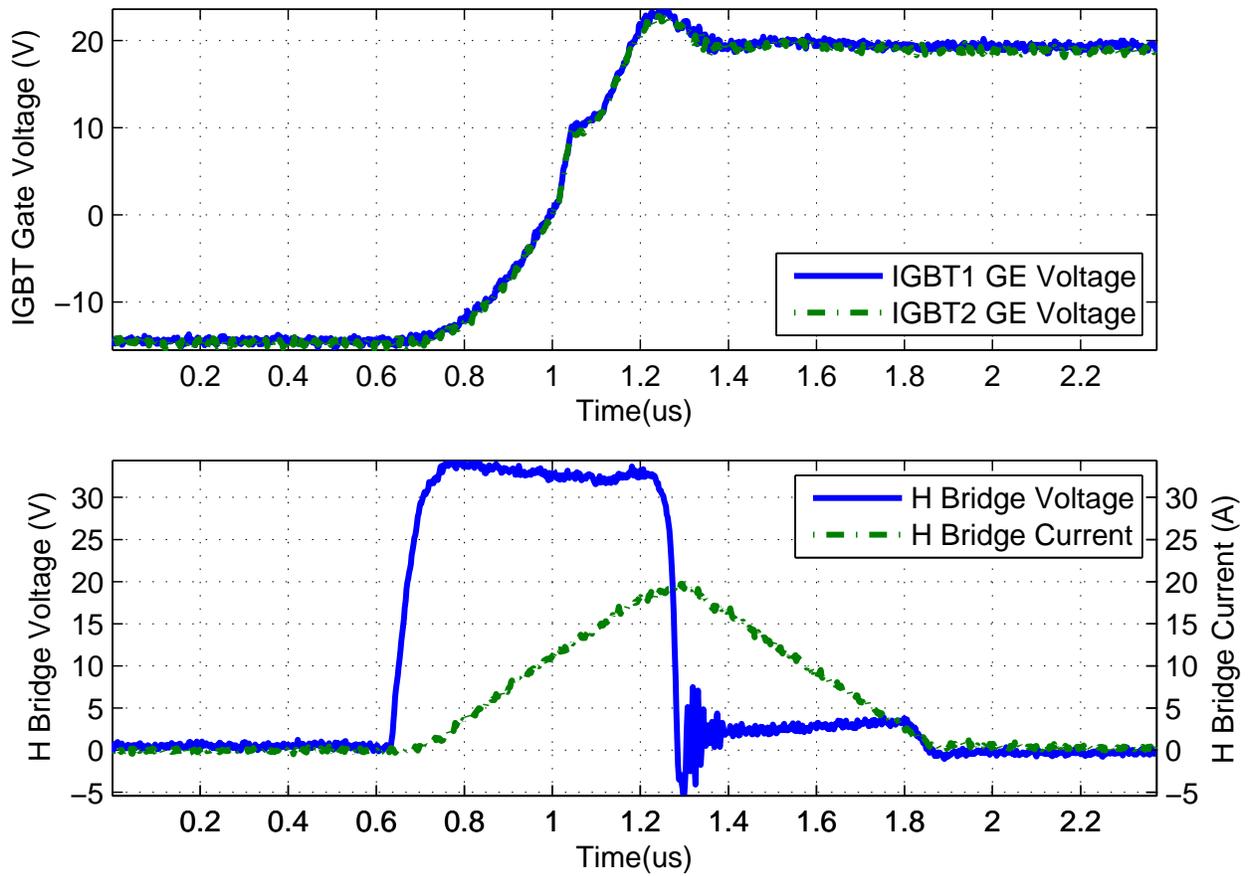


Figure 9.4: Gate to emitter voltage waveforms of two series connected IGBTs along with the corresponding pulse sender H-bridge voltage and current waveforms during a turn-on event.

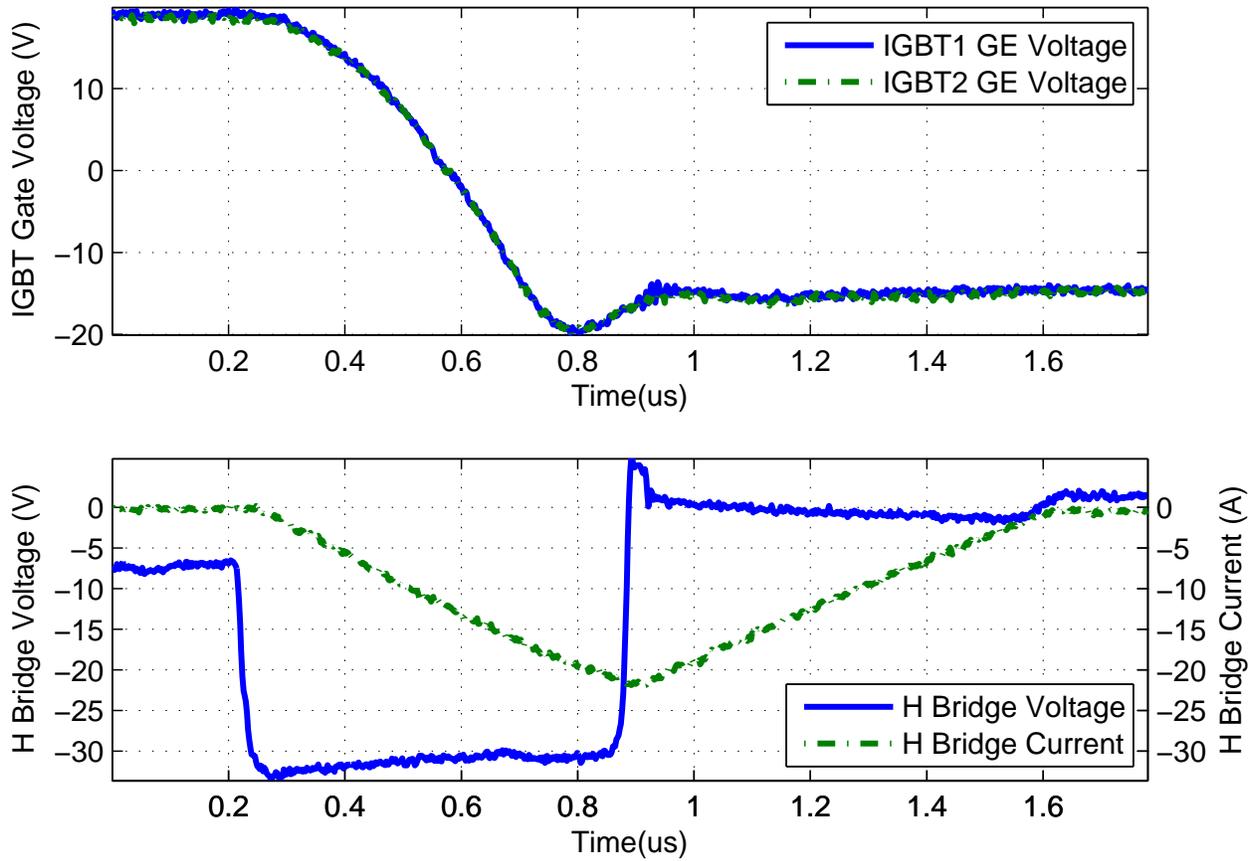


Figure 9.5: Gate to emitter voltage waveforms of two series connected IGBTs along with the corresponding pulse sender H-bridge voltage and current waveforms during a turn-off event.

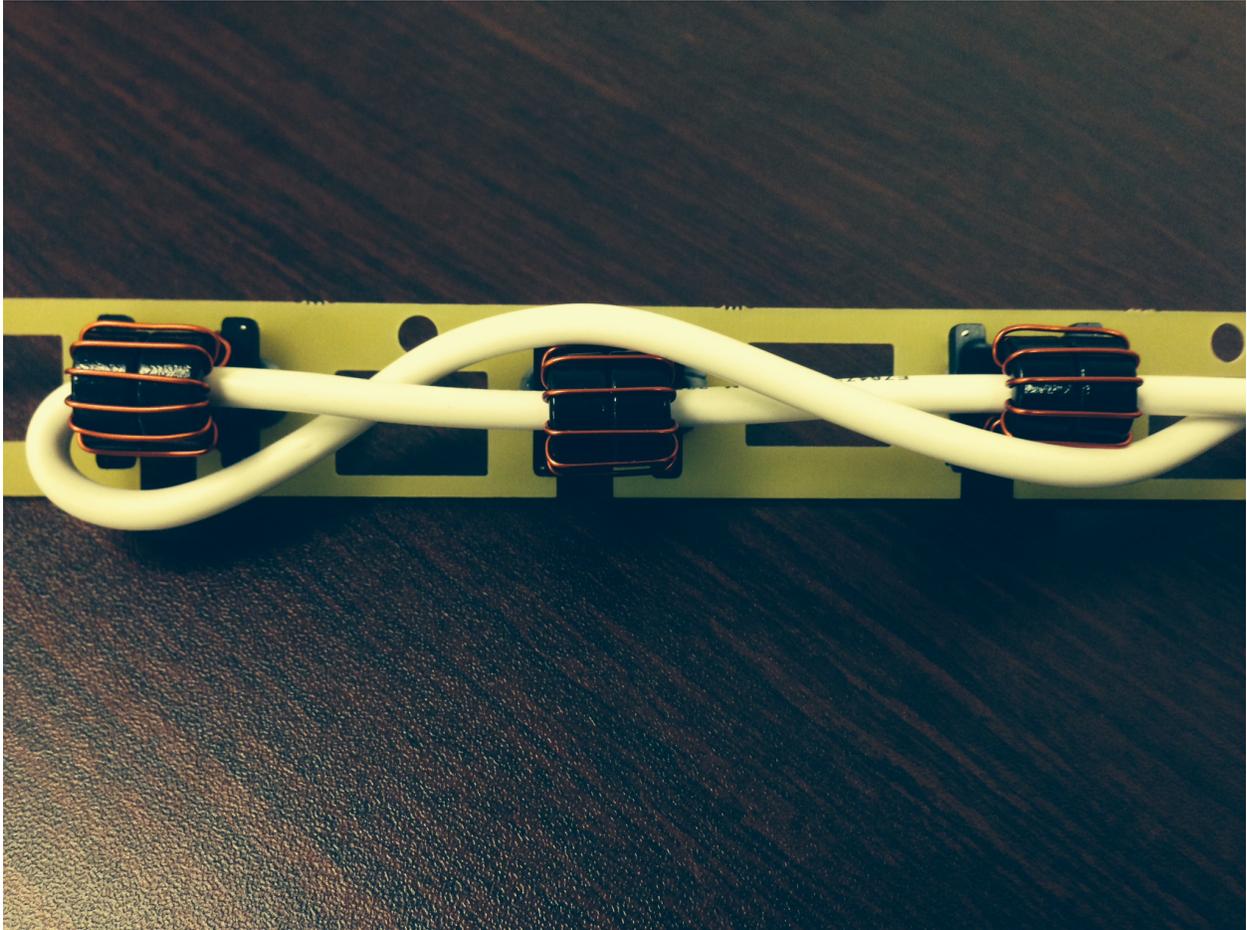


Figure 9.6: Pulse transformer primary winding shown with three secondary windings.

10.0 IMPLEMENTATION

A prototype of the proposed converter concept was constructed using the five-level NPP topology as illustrated in Figure 4.3b. The NPP topology variant was selected over the NPC topology for three main reasons. Firstly, the NPP topology inherently contains mechanical symmetry as each branch of the circuit contains the same number of semiconductor devices. This mechanical symmetry translates to symmetry in the commutation loops within the sub-circuits, allowing common snubber components to be used throughout the topology.

Secondly, the use of series connected devices inherent to the NPP topology allows for lower switching losses compared to the NPC topology [10].

Finally, semiconductor losses can be spread evenly in the converter for low modulation depth, high current operating points by taking advantage of redundant switch states using space-vector modulation or common-mode injection techniques. This loss spreading is possible because each branch of semiconductors conducts only if its output level is selected. For a given modulation depth and current direction, losses can be allocated to particular branches. This is in contrast to the NPC topology, where certain devices must conduct for multiple output voltages, limiting the ability to spread the losses.

Each capacitor level was designed for a nominal voltage of 1600 V for a total dc-link voltage of 6400 V. This power stage is appropriate for 4.16 kV motor-drive applications that are prevalent in North and South America. An array of metallized polypropylene film capacitors distributed throughout each power board were used to establish the dc-link capacitance.

All required sharing-resistor networks and snubber networks are easily implemented on the bottom of the board as surface mount components. The requirements for the sharing resistor and snubber networks will be discussed in Sec. 12.0.2. Board-to-board power con-

nectors are used along with a PCB backplane to network all common dc-link connections together for all power stages within a system. All sub-circuit components responsible for conducting current flowing out of the dc-link are grouped on one board and all sub-circuit components responsible for conducting current flowing into the dc-link grouped on another board.

11.0 TARGET RATING AND DEVICE SELECTION

The devices shown in schematics thus far each represent a device group, a group of one or more semiconductors operated as a single device. These groups have a voltage rating equal to the sum of the series-connected device ratings and a current rating equal to the sum of the parallel-connected device ratings. Multiple device groups can then be arranged on a PCB to achieve a medium-voltage power converter.

The base-plates of series-connected devices must be electrically isolated from each other because each operates at a different power circuit voltage.

Devices can be effectively used in parallel by ensuring both steady-state and dynamic current sharing [52]. Mounting parallel devices on a common heat sink provides thermal coupling and encourages steady-state current sharing because commercially available discrete devices are designed with a negative temperature coefficient that reduces the current through a device with a higher junction temperature relative to cooler devices in the parallel network. This feedback mechanism minimizes current mismatch in the parallel device network branches. To ensure dynamic current sharing, a geometrically symmetrical layout of the parallel device network was used. This symmetrical layout is sufficient because the relatively high inductance of the discrete device package coupled with the high di/dt of medium-voltage converter commutation events dominates the effective impedance of each device branch within the parallel network.

Devices are available in the DO-247 and TO-247 packages with ratings above 1200 V; however, these devices are only available through a limited number of suppliers. The devices chosen were 1200 V, TO-247 package IGBTs and 1200 V, DO-247 package diodes because these device ratings are standard in these packages and are offered by all of the major discrete semiconductor manufacturers. In order to achieve the appropriate voltage ratings

with a 6400 V dc-link, two 1200 V devices in series were used per level. Four parallel devices on a common heat sink were used to achieve the necessary current rating for a 746 kW converter. Thus, in total each device group contains eight discrete semiconductors operated together. To produce the bridge shown in Figure 4.3b requires 320 discrete devices.

11.1 THERMAL MANAGEMENT

In order to analyze the power circuit thermal management requirements, a dynamic fourth-order electro-thermal impedance network model [53] was created for the IGBT and diode groups. All electro-thermal model parameters must be appropriately scaled for the series and parallel networks of devices so that the model can be simulated using commercially available packages. In order to speed up the thermal simulations, the separation in thermal time constants between the devices and the heat sink were exploited by separating the simulation of each phenomenon with appropriately and independently set simulation time steps.

All operating points were simulated for the front-end, back-end, and capacitor balancing bridges to set thermal impedance criteria for the device heat sink. An extruded aluminum heat sink was designed to meet the thermal impedance requirements produced during the dynamic electro-thermal simulations. Heat sink temperature measurements were collected using isolated, fiber optic temperature measurement probes. The peak device junction temperatures were extracted using these heat sink temperature measurements and knowledge of the thermal impedance network. The dynamic electro-thermal model was verified to match the empirically collected temperature measurement data within device loss mechanism parameter variance published by the device manufacturers.

12.0 PCB ARRANGEMENT FOR MEDIUM VOLTAGE

12.0.1 Voltage Isolation

One major design consideration is providing appropriate voltage isolation between devices on the PCB. One convenient way to do this is to assign each device to its own heat sink and maintain proper creepage and clearance spacing between different circuit potentials. Forced-air cooling schemes are compatible with this arrangement to allow for different heat sink voltages while meeting device thermal requirements. The power circuit layout was designed using the distances defined in the UL61800-5-1 safety standard Tables 9 and 10 [54], which is the most appropriate standard for these voltages.

Figure 12.1 illustrates a top down view of the layout of four parallel TO-247 package IGBTs shown without the single common heat sink. Lead forming was implemented to meet the creepage and clearance distance requirements given in UL61800-5-1 and to allow for a thermally optimal heat sink design.

12.0.2 Series-Connected Power Semiconductor Devices

There are four main device characteristics that will create voltage imbalance associated with series-connected strings of devices: leakage current, tail-charge, threshold voltage, and effective input capacitance.

Any mismatch in leakage current between series-connected devices will cause the devices to not share static blocking voltage equally in the device's non-conducting state. This particular mechanism for voltage imbalance is easily addressed using a passive sharing-resistor network connected across each semiconductor device group in the series-connected string. An array of thick-film, 2512-package, surface-mount sharing resistors per heat sink were im-

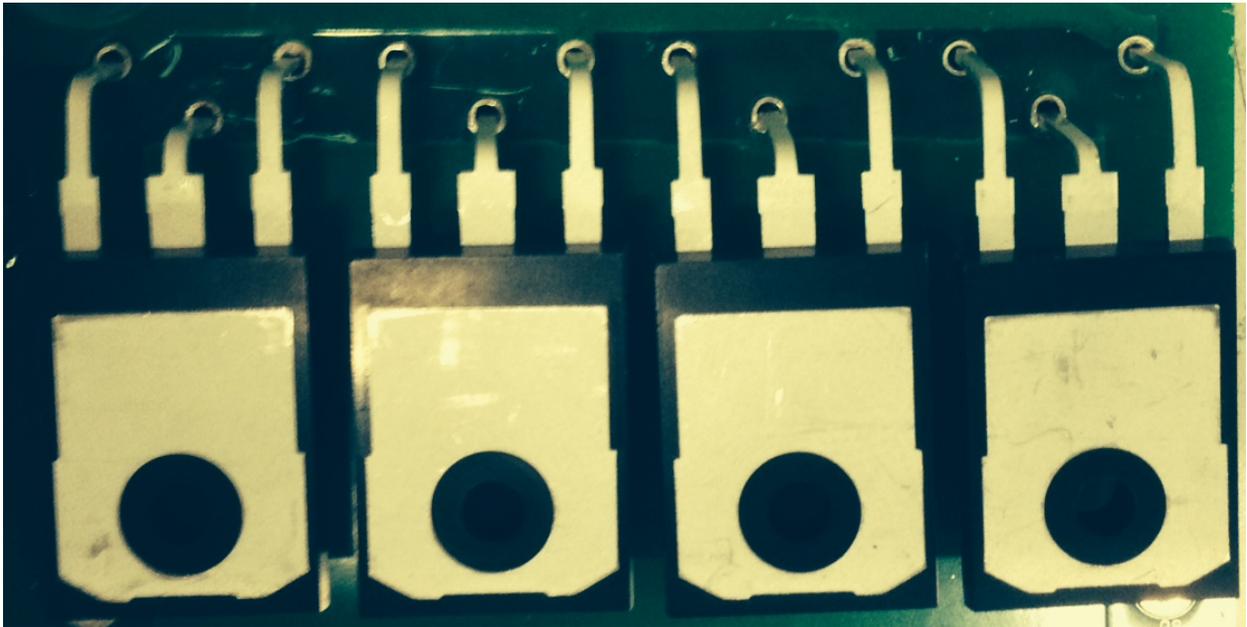


Figure 12.1: Four parallel device PCB layout with lead forming to meet UL61800-5-1 creepage and clearance requirements. Note that the layout is shown without the common heat sink to expose device pin layout details.

plemented for the prototype. The sharing-resistor network bias current was chosen to be ten times larger than the expected mismatch in leakage current to ensure a voltage mismatch of 5% or less of the nominal static blocking voltage.

Any tail-charge mismatch (IGBT) or reverse-recovery charge mismatch (diode) across series-connected devices that clears during device turn-off events will cause an uneven charging of the output capacitance of the devices and ultimately cause off-state voltage imbalance for the series-connected devices. Therefore a passive RC snubber is added across each semiconductor device, with the capacitor sufficiently large so that a tolerable amount of voltage mismatch is realized for the expected amount of charge mismatch. However, large snubber capacitance increases power loss due to dissipation of the energy stored in the capacitor during each On/Off switching cycle. The snubber resistor is chosen to minimize voltage overshoot during device turn-off by using an effective resistance value that is equal to the characteristic impedance of the resonant tank formed between the commutation loop inductance and the parallel combination of the device output capacitance and the snubber capacitance [55]. An array of 1812-package, surface-mount, ceramic capacitors were used for the snubber capacitance and a series-network of 2512-package, surface-mount, metal element type resistors were added per heat sink for the snubber resistance to handle the high pulsed power required.

Finally, any difference the series-connected IGBT threshold voltage or effective input capacitance will cause the devices to not share voltage during the initial turn-on and turn-off edges. These differences are easily dealt with by overdriving the devices as outlined in 9. Voltage sharing during these highly dynamic turn-on and turn-off edges is further encouraged by the negative feedback from the collector to the gate present in the IGBT due to the Miller capacitance [56].

The sub-circuit 1 PCB with heat sinks is shown in Figure 12.2; sub-circuit 2 is on a separate board.



Figure 12.2: Sub-circuit 1 PCB shown with heat sinks.

13.0 EXPERIMENTAL RESULTS

The authors constructed a 746 kW, 4.16 kV prototype to demonstrate this converter scheme. Three input bridges labeled a, b, c and three output bridges labeled u, v, w were each constructed by connecting the outputs of sub-circuit 1 and sub-circuit 2 together with a wire and one balancing bridge was constructed by connecting a 11 mH reactor between the outputs of sub-circuit 1 and sub-circuit 2. A single 2 mH inductor was placed between the outputs of each pair of input and output modules. The entire dc-link was fed from a 6400 V dc supply. A diagram of the dc fed test setup is shown in Figure 13.1.

The input modules' modulation depth was held constant at 0.88 and output modules were controlled to circulate a 60 Hz, 1 pu (130 A) three-phase current with a constantly varying back-end modulation reference to current angle ϕ_{BE} from 0 to 2π radians at a rate of 2π radians per hour. A 10 kHz, four-carrier, sine-triangle, out-of-phase disposition-modulation strategy was implemented [45]. The capacitor balancing requirements of this dc-fed front-to-back system topology for a constant input bridge modulation depth of .88 as a function of the current angle with respect to the input bridge modulation reference are shown in Figure 13.2 are always less than .05 pu. The balancing module was configured to regulate balancing reactor current to an I_{nom} of 0.3077 pu (40 A) with I_{min} of 0.1923 pu (25 A) and an I_{max} of 0.4231 pu (55 A). Plots of one phase current and one phase voltage are shown in Figure 13.3.

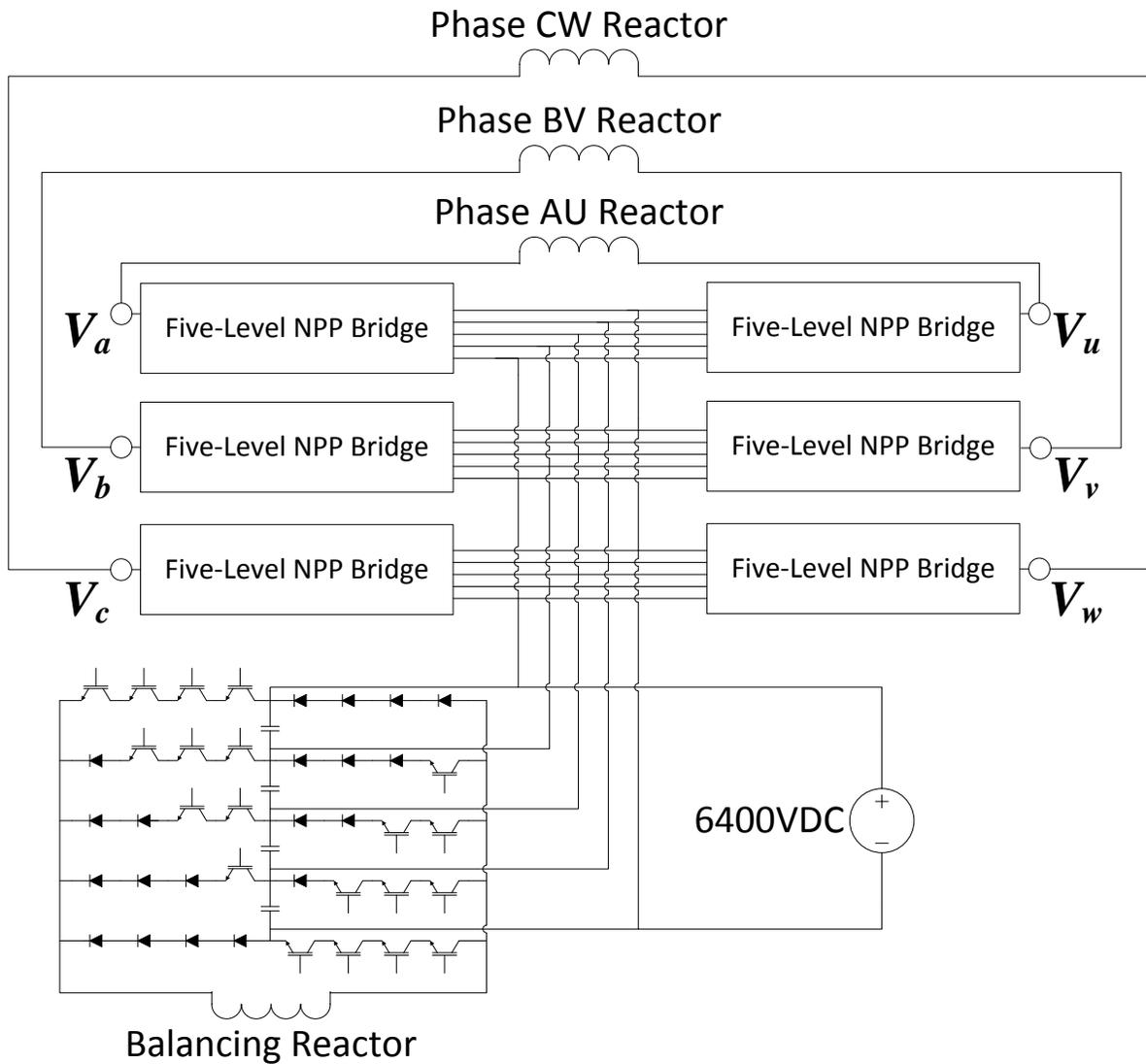


Figure 13.1: DC fed front-to-back test setup. The six bridges from Figure 4.3b are connected to another bridge and balancing reactor to form a complete motor-drive with balancing. To run the front-to-back test, the ac terminals are connected with a reactive load, and the losses are fed from a dc source connected to the dc bus.

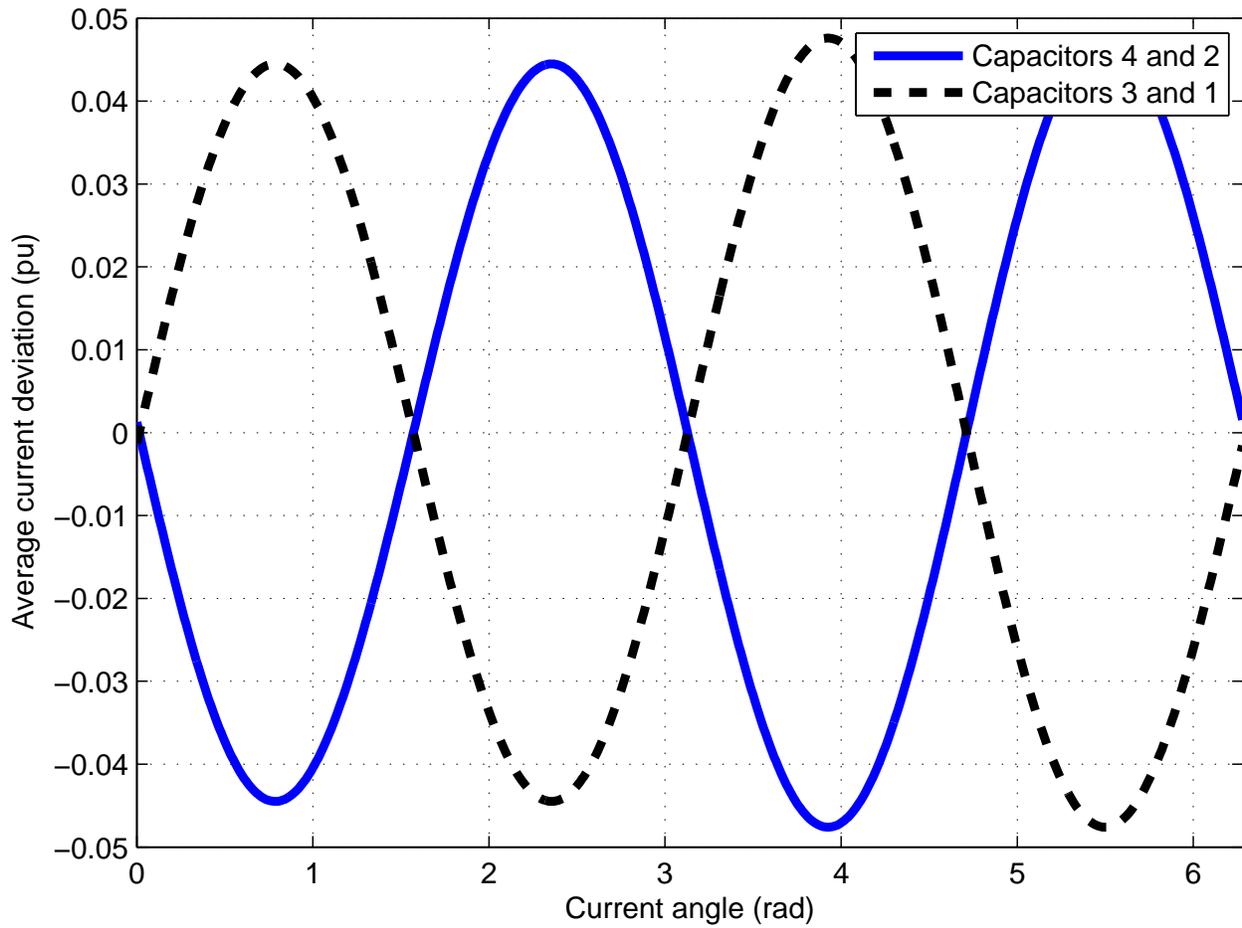


Figure 13.2: Average current deviation vs. Current Angle with a device under test modulation depth of .88 and 2mH of inductance between each phase module.

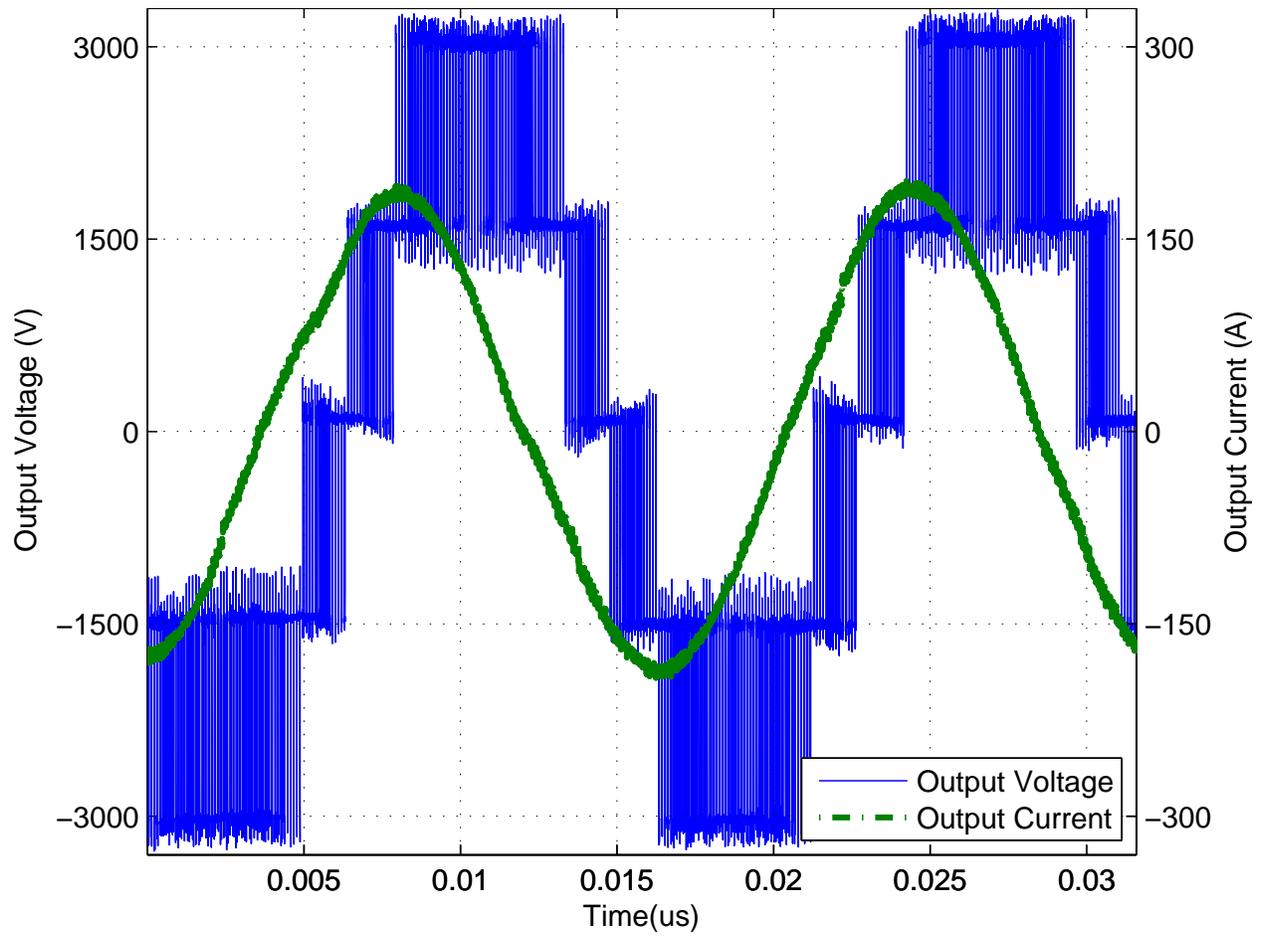
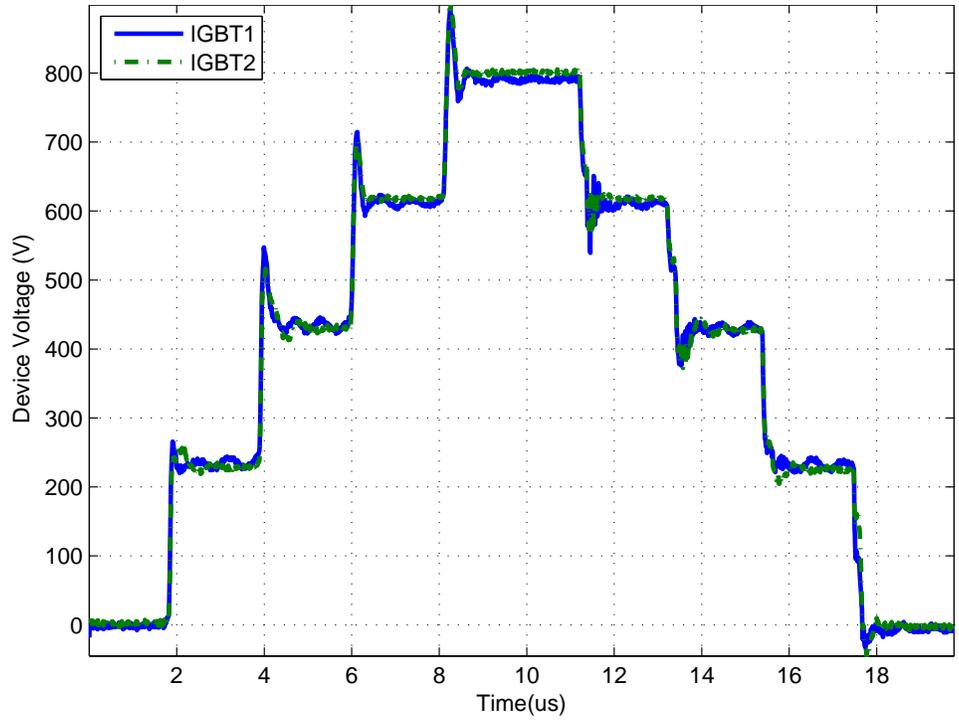


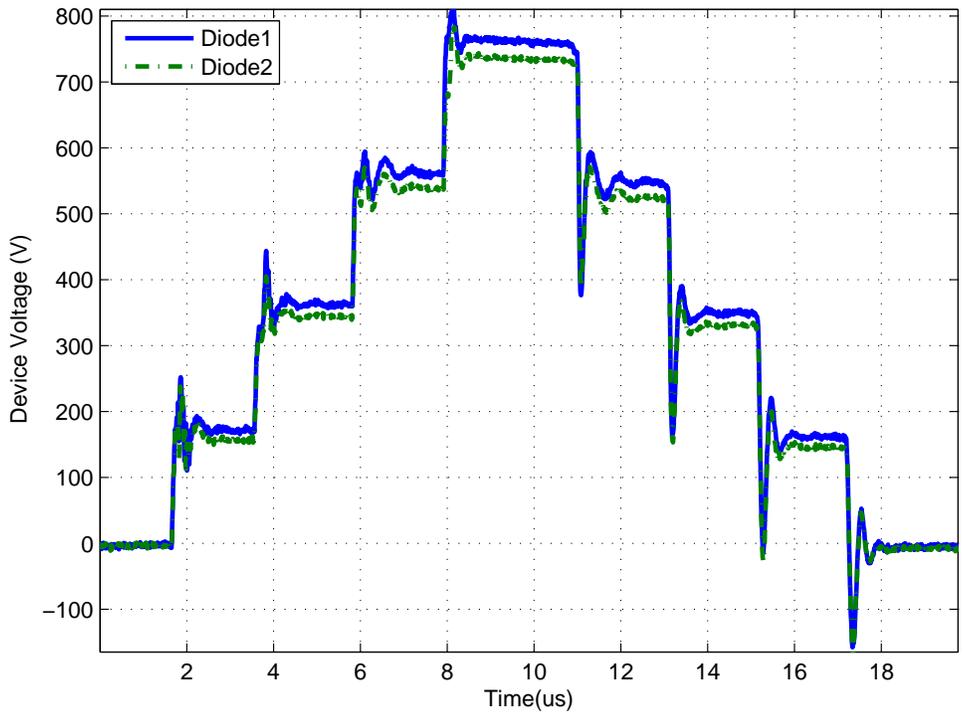
Figure 13.3: Five-level NPP output voltage and current with a 6400 V total dc-link voltage.

Series-connected device voltage sharing was measured and verified during peak current switching events in the dc-fed test configuration illustrated in Figure 13.1. During device voltage sharing verification, the bridges were operated to pass through each of the five voltage levels. Plots of the voltage waveforms for a series-connected IGBT pair in the string of IGBTs with eight series-connected devices, and a diode pair in the string of diodes with eight series-connected devices are shown in Figure 13.4.

Plots of the balancer discharger state machine output voltage, charger state machine output voltage, and balancing reactor current are shown in Figure 13.5. The waveforms presented in Figure 13.5 demonstrate that the dc-link voltage levels remained balanced while a symmetric three-phase current of 130 A and 60 Hz was circulated.



(a) IGBT voltage waveforms.



(b) Diode voltage waveforms.

Figure 13.4: Series connected IGBT collector-emitter voltage waveforms and series connected diode anode-cathode voltage waveforms during the bridge through all five levels and back.

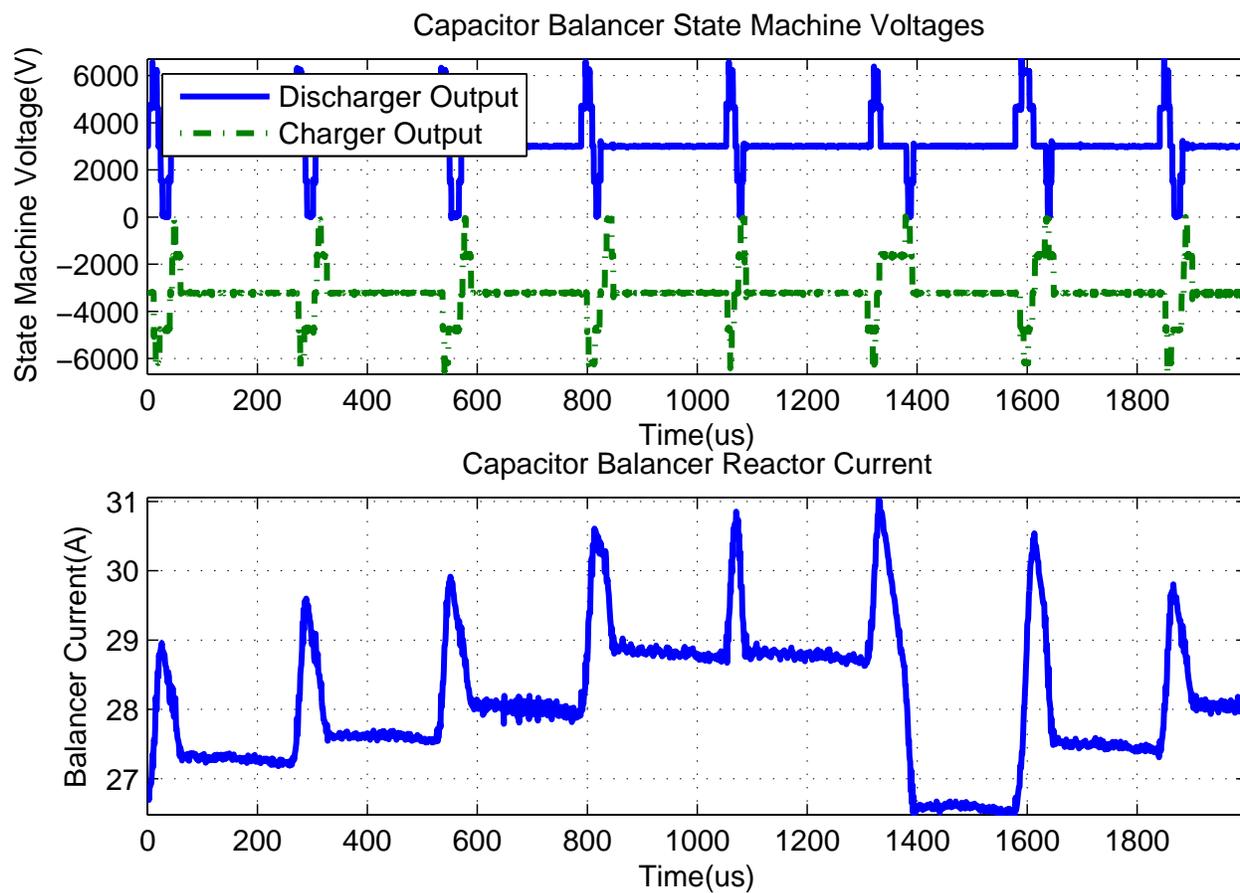


Figure 13.5: Capacitor balancer discharger state machine output voltage with respect to $Node_0$ voltage, charger state machine output voltage with respect to $Node_4$ voltage and balancing reactor current.

14.0 CONCLUSION

This dissertation presented a new philosophy for implementing an IGBT-based, low-power, medium-voltage power converter using discrete semiconductor devices and printed circuit board technology. A power circuit topology unwrapping technique for N -level NPC, ANPC, and NPP bridges was used to design a simple mechanical arrangement of the devices on a PCB with very low commutation inductance. This technique also allows the same power stage to be used as a dc-link capacitor balancing circuit for the N -level converter. The use of PCB technology and a commonality across power stages and balancer circuit allows extensive automated testing and quality control, along with minimal spare parts. A novel IGBT gate-drive system was developed that is well suited to gate large numbers of series-connected devices. The balancing circuit and an associated control algorithm were studied in a motor-drive application. Finally, a 4.16 kV, 746 kW, PCB-based prototype was built and tested at rated current and voltage including the power circuit topology unwrapping technique, the IGBT gate-drive system, and the capacitor balancing circuit that is identical to a power stage.

14.1 FUTURE WORK

Several aspects of the converter system presented in this dissertation would benefit from future work. The system behavior under dynamically varying conditions requires further investigation. This investigation should include the formulation of a dynamic behavior model of the entire system including front-end, back-end and capacitor balancing circuit control systems.

The non-ideal properties of the system need to be studied to analyze impacts on the controllability of the dc link voltages. For instance, the minimum-state time in each state machine represents the amount of time each balancing circuit must spend in a particular state, even if it is undesirable to be in that state from a capacitor voltage balancing standpoint or a reactor current balancing standpoint. The minimum-state time defined in the state machine is defined by the limitations of the selected semiconductor devices for a particular system. If IGBTs are selected for use in the system, a minimum-on time must be honored during the capacitor balancer operation in order to avoid degrading and destroying the IGBTs prematurely. More work is required to understand the implications of how large the minimum state time can be with respect to all other parameters of the system including, sweep frequency, maximum-state time, reactor inductance, and dc link capacitance.

As was explicitly presented in this dissertation, the optimization of the system design including the capacitor balancing circuit parameters and algorithm set points assume that the dc link capacitors are sized sufficiently so that the voltage ripple due to power factor mismatch between the front-end and back-end bridges is small. It is the scope of future work to investigate how the balancing circuit requirements might change if the dc link capacitance in the system is reduced so that the voltage ripple on the dc link capacitors due to power factor mismatch or voltage angle mismatch between the front-end and back-end bridges are not negligible. There may be a design optimization problem with further reducing the dc link capacitance while increasing the bias current in the capacitor balancing circuit.

The original capacitor balancing capability models presented in this dissertation were exercised without any common-mode injection techniques to assist in capacitor balancing functionality in the system. It is the scope of future work to investigate the combined effect of the auxiliary capacitor balancing circuit and algorithm presented in this dissertation with a common-mode injection strategy specifically designed to assist with capacitor voltage balancing for further system optimization.

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