OVERVOLTAGES ASSOCIATED WITH PHOTOVOLTAIC INVERTER TRANSIENTS

by

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Increased penetration of solar photovoltaic (PV) can cause significant overvoltages during faults and back-fed fault current into grid while causing miss-operation of protective relaying. Transient data from four single-phase PV inverters was collected during both open-circuit and short circuit transient events. Each inverter was tested at four different output power levels and multiple tests were run for each case to account for point-on-wave effects on the transient magnitudes. Test program designs are presented to cover a range of inverter operating conditions and grid configurations. The data was used to plot the overvoltages and overcurrents associated with the transient events. In some cases, the inverters can produce transient overvoltages > 1.6 p.u. and transient overcurrents > 14 p.u. In addition, theoretical magnitudes of transient overvoltages can be compared with the laboratory result.

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PREFACE

I would like to first thank my parents for their ongoing support of my educational pursuits, career choices, and emotional well-being. It is impossible to list the sacrifices they have made to give me the opportunity to be here pursuing and obtaining an advanced degree in electrical engineering.

Then, I would like to thank the ESIGELEC and Dr. Mahmoud El-Nokali for giving me the great opportunity of coming to study here in the United States.

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1.0 INTRODUCTION

Various interconnection challenges exist when connecting distributed photovoltaics (PV) into the electrical distribution grid in terms of safety, reliability, and stability of electric power systems. One of the urgent areas for additional research, as identified by inverter manufacturers, installers, and utilities, is the potential for transient overvoltage from PV inverters. Indeed, based on a 2014 EPRI Survey on Distribution Protection [1], 75% of those surveyed selected overvoltages as one of the greatest concerns when it comes to interconnection, in particular, overvoltages following an islanding event. The majority stated that overvoltages on the primary distribution system are the biggest concern when it comes to specifying an interconnection transformer. Because of the concern with primary-side overvoltages, this led to varying requirements of what transformer type would be used to limit overvoltages. In addition to the overvoltages associated with faulted conditions, some utilities are taking precautions against overvoltages caused by inverters being isolated from the utility [1]. It has been observed that when an inverter system is disconnected from the grid and left connected to only a very small amount of local load, sudden overvoltages can occur.

For traditional systems (synchronous machines), this overvoltage response is generally governed by the physical parameters of the generator, the interconnection transformer and the grounding method chosen. All those parameters are generally well-known with synchronous machines having been used by utilities over a very long period of time. But concerning inverters, those parameters are not well known due to the lack of modeling details from the inverter vendors and the diversity of the inverter technologies, which can differ from one manufacturer to another.

With these concerns in mind and to be able to get a deeper understanding of the inverter under transient conditions, our goal is to test and collect data from four single-phase PV inverters during two critical transient events: open-circuit (load rejection) and short circuit (ground fault). The overall objective is to enable more accurate planning and interconnection studies by power system engineers, and characterize the impacts of single-phase inverters on the electrical grid during faulted conditions.

2.0 LITERATURE REVIEW

Multiple studies have been conducted concerning the impact of inverter transients on the grid. National Renewable Energy Laboratory (NREL) in collaboration with the Electric Power Research Institute (EPRI) conducted some tests to determine the duration and magnitude of transient overvoltages created by several commercial single-phase PV inverters during ground fault (GF) conditions [2] and during load-rejection (LR) conditions [3]. Results confirmed previous theoretical analyses asserting that inverters do not drive ground-fault overvoltages in the same way that synchronous machines do, although they can do so to a limited extent in certain scenarios. In addition, the measured over-voltage magnitudes were all under 200% of nominal peak voltage, and the over-voltage durations were on the order of microseconds to milliseconds [2]. These over-voltages were less severe than some observers had feared and this allayed some utility concerns. These results corroborate the theory that in load rejection overvoltage (LRO) situations, treating inverters as ideal AC current sources greatly overestimates the severity of the overvoltage [3]. However, an LRO of up to 225% of rated overvoltage for as long as 3 cycles has been reported by Southern California Edison (SCE) as discussed in references [4] and [5], contradicting this conclusion.

Furthermore, presently, power engineering software packages will typically recommend using a constant current source generator model and setting a fault current contribution limit to 2 - 3 times ("rule of thumb") the current nameplate capacity rating of the inverter-based DER generator during ground fault events [6]. Utilities may be using a high (4.5 p.u. or more) fault current contribution from solar PV inverters in absence of actual test data. This practice may impact future projects where solar PV studies may cause circuit breakers (CB) and fuses to go beyond their ratings, which could cause unnecessary upgrades and additional costs to future projects. However, another collaborative research effort between NREL and SCE involving laboratory short-circuit testing of 20 single-phase (240 VAC) residential type PV inverters of various manufacturers and power ratings, ranging from 1.5kW to 7kW, revealed that the maximum fault current recorded was between 4-5 p.u. and lasted for approximately 0 - 1 cycle [7].

All those contradictions come from the diversity of inverter technologies and control schemes of those inverters which make them behave differently under the same transient conditions. This shows that more testing is required to get a better understanding of those PV inverters.

3.0 ELECTRIC POWER SYSTEM LABORATORY OVERVIEW

All our testing was done in the Electric Power Systems Lab (EPSL) shown in Figure 1. Located on the Swanson School of Engineering's 8th Floor in Benedum Hall, the EPSL includes six experiment stations with configurable loads, motor drives, meters, relays and controllers. The lab also includes a local area network (LAN), programmable logic controller (PLC) equipment, a sag generator, power factor correction capacitors, uninterruptible power supply (UPS), hardware development tools, smart meters and other test equipment. Both 480V AC and 208V AC systems are available, along with a direct current (DC) system. The six test benches provide a total 30 kW of adjustable RLC load, including harmonic-producing compact fluorescent lights. There is also a 25-kW synchronous generator for dedicated micro-gridding in the EPSL, and solar power from rooftop panels comes into the lab. [8]

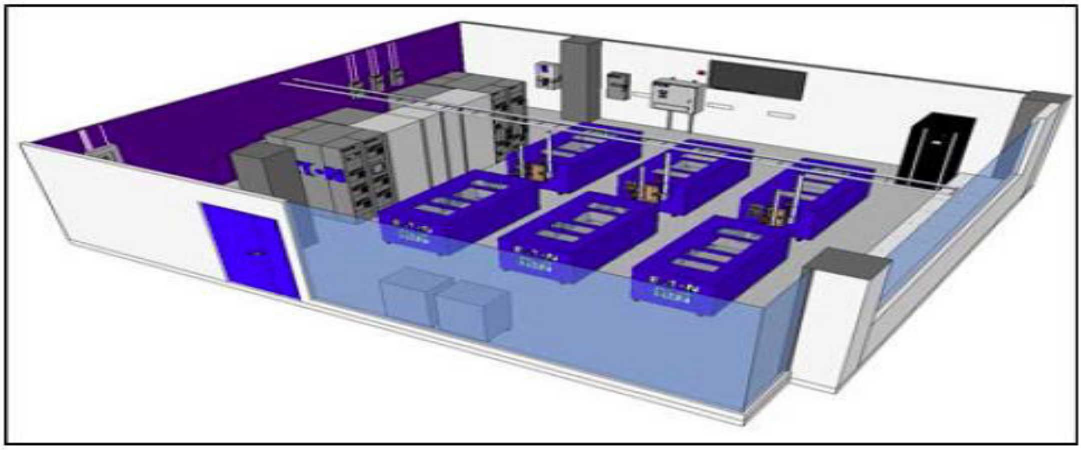

Figure 1. Layout of the Electric Power Systems Laboratory, with six test benches in dark blue and the Integrated Facility Switchboard (IFS) in gray [8]

Furthermore, for our testing, the laboratory also includes four single-phase PV inverters from four different vendors ranging from 2000 kW to 3000 kW, six configurable three-phase transformer banks, each rated 6 kVA, a sag generator, a 10 kW photovoltaic emulator, and some monitoring equipment. Each test equipment is described in further detail in the test set-up section.

4.0 TEST SET-UP

This section describes the laboratory set-up used to test the PV inverters. This test setup, used to evaluate the behavior of inverters in short circuit and short circuit scenarios, is designed in a way to accommodate most of the commercial inverters in the market and typical grid conditions. Figure 2 shows the one-line diagram of the inverter test set-up. A detailed description of each component is provided in the following sections.

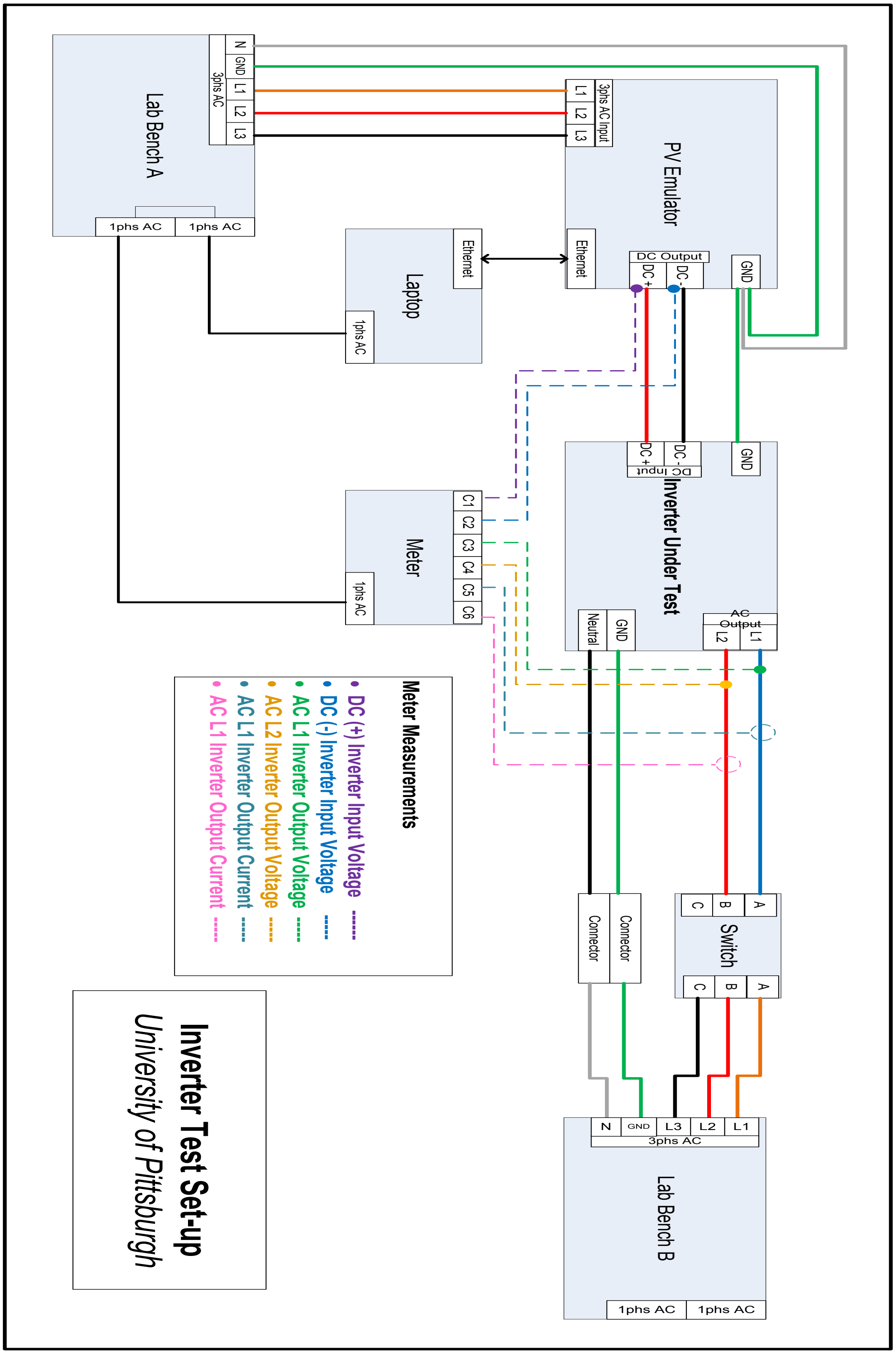

Figure 2. One line diagram of the test set-up

4.1 LAB TEST BENCHES

Figure 3 shows a one-line diagram of the laboratory benches in the EPSL. Lab bench 4 or lab bench A (See Figure 2) is only used to power the PV simulator connected to the 20A power outlet. Both the laptop and the monitoring equipment are connected to a separate control power outlet. Lab bench 5 (lab bench B) is used as the load connected between the inverter under test and the grid. It has been reconfigured to be connected to variable autotransformers and acts as a variable and controllable load to match the power output of the tested inverter in order to mitigate the transients from the switching of the sag generator.

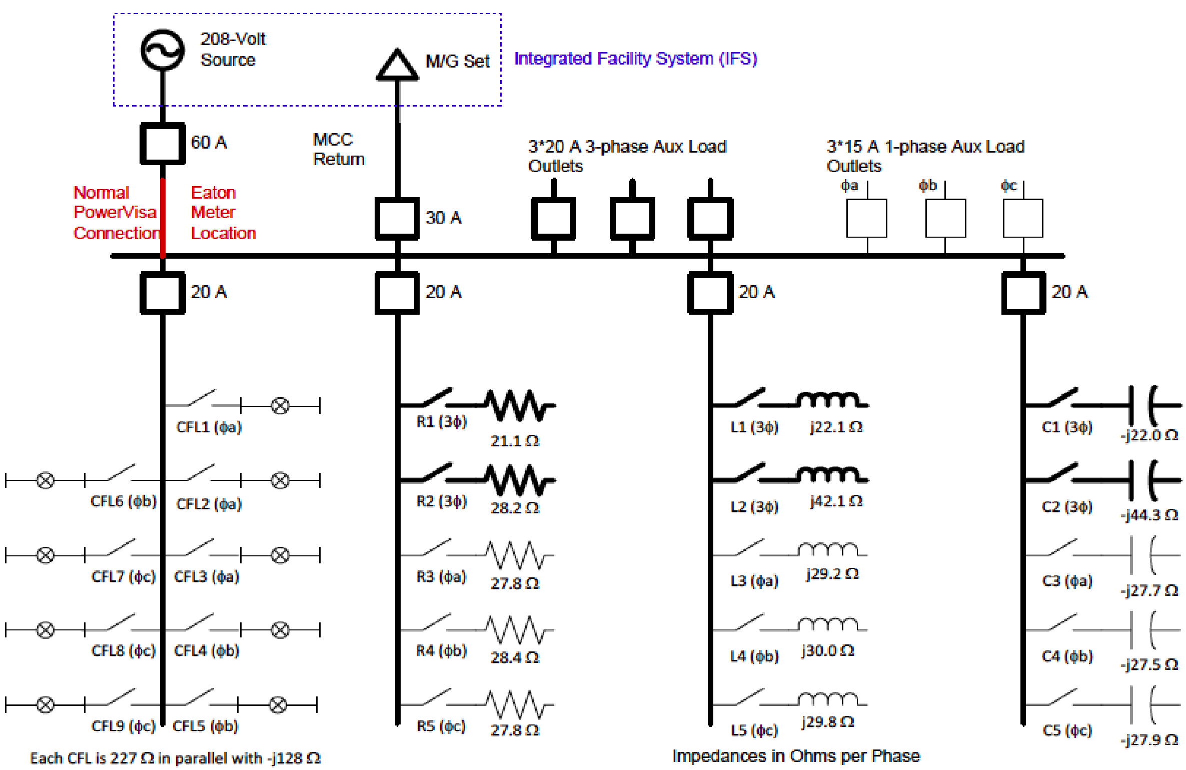

Figure 3. One-line diagram of a lab bench [8]

4.2 ELGAR ETS600X PV SIMULATOR

The Elgar ETS600X PV simulator is a programmable DC power source designed to simulate the current-voltage curve of photovoltaic arrays. The PV simulator, shown in Figure 4, is provided software that makes it fully controllable via personal computer (PC). It is able to provide a DC output voltage of 0-600V and a DC current output of 0-16.7A, which is sufficient to supply inverters up to 10kW in theory [9]. But the fill factor, more commonly known by its abbreviation "FF", in conjunction with V_{oc} (open-circuit voltage) and I_{sc} (short-circuit circuit) of a solar panel, determines the maximum power of that panel. Taking the FF into account, the practical maximum power from the emulator is about 8.5 kW. During our testing, we used this simulator to provide the inverter's dc input.

Figure 4. 10kW Elgar PV simulator [10]

4.3 SAG GENERATOR

A voltage sag generator is a device or equipment capable of generating the suitable voltage-time profiles at the terminals of the inverter under test. It was used to simulate a short-circuit during our testing because it can generate and maintain a zero voltage across the terminals of the inverter at any given moment for a predetermined duration. The sag generator was designed to be controlled by an Eaton touch-screen programmable logic controller (PLC) interface. From the PLC, the user can select the desired transformer tap and sag duration. Electrically, the generator is in parallel with the power source to the motors and lab benches. A selector switch is used to select the normal source, the sag generator, or to open circuit for both sources. A one-line diagram of a phase of the sag generator is shown in Figure 5. The two silicon controlled rectifiers (SCRs) are rated at 250 A and 1600 V. The top SCR is the bypass SCR and is shown in parallel with a contactor to its left in the one-line diagram. The sag path SCR is in series with the autotransformer and tap selection contactors. [11]

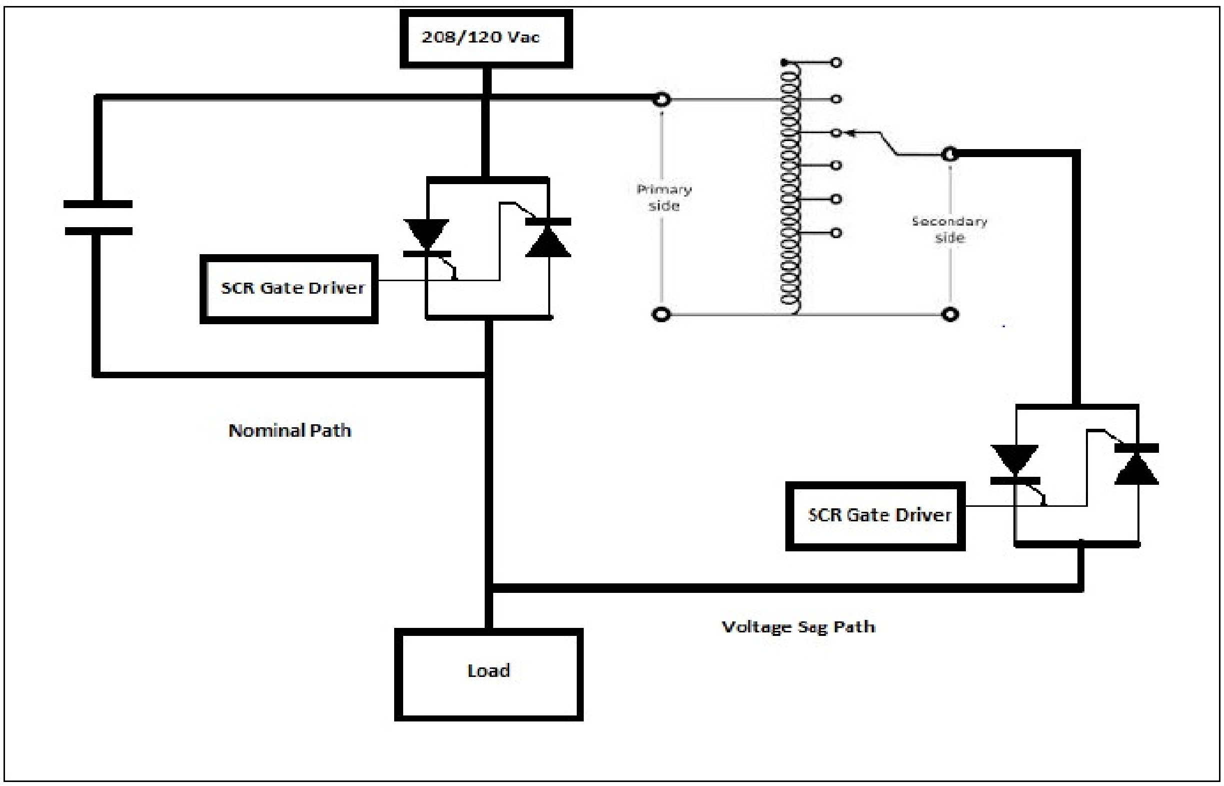

Figure 5. One-line diagram of a phase of the sag generator [11]

On the far left of the one-line diagram is shown a normally open contact. This contact represents the three-phase 200A Eaton XT series bypass contactor, which is in parallel with each of the bypass SCRs. This contactor is closed whenever the PLC is powered and a sag event is not in progress to take the normal load away from the SCR bypass path. This contactor opens before the SCR switching sequence occurs, so that the power electronics handle the actual sag event

[11]. However, there is always a 1 - 2 cycles break between each switching sequence because the SCR commutation is not fast enough. This situation added some undesirable transients during each sag event, which could affect our results due to the “break-before-make” phenomenon. Since the SCR switches used in the EPSL are not timed precisely during the sag event, the SCR switches open before the auto-transformer contacts are enabled to place the voltage sag. EPRI’s laboratory facility has a much faster 200A Tri-Mode sag generator which does not experience this problem. The difference between the University’s sag generator and EPRI’s is shown in Figure 6.

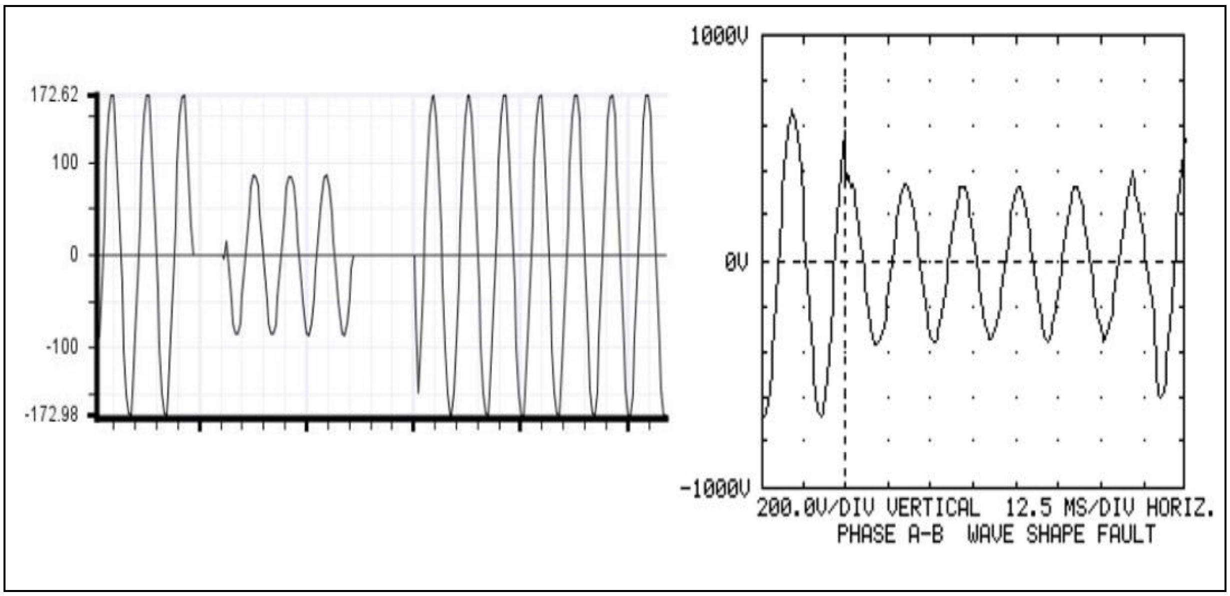

Figure 6. EPSL Three-cycle 50% Sag Event (left) and EPRI 40% Sag Event (right), no PV Inverter

The “break-before-make” operation of the EPSL sag generator is shown by the dead bands when the sag is enabled and removed. To remedy to that, we decided to do some load matching with the lab bench loads and some variable autotransformers as shown later.

Concerning the structure of each phase, there are thirteen tap selection contactors for each phase. These contactors are controlled by the PLC by using the graphical user interface (GUI) touch screen, shown in Figure 7, located in the lab.

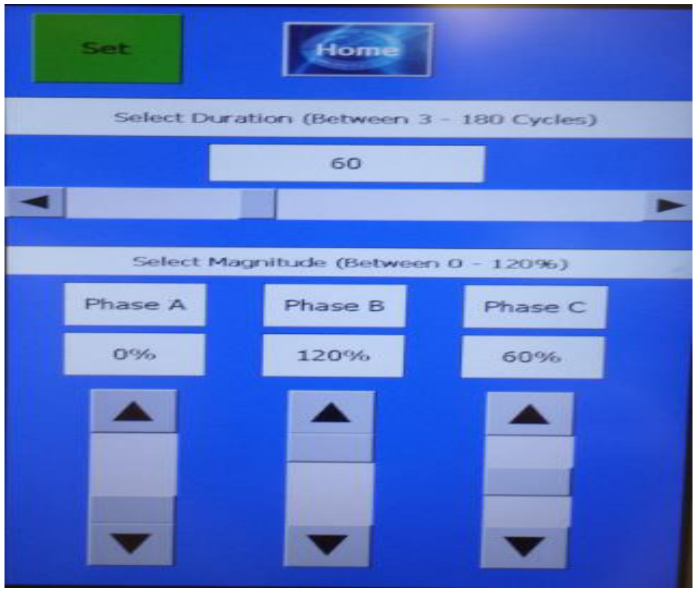

Figure 7. Sag Generator GUI

The generator can be set to apply a sag for a duration between 3 and 180 cycles by increment of 1 cycle. In addition, each phase can be individually programmed for a voltage magnitude from 0% (short circuit) to 120% (voltage swell) by increment of 10%. With this configuration, we could recreate in the lab a short circuit fault (sag to 0%) for our testing purposes. With reference to Figure 5, the sag generator autotransformer tapped at 0% output initiates this fault when the sag path SCRs begin conduction.

4.4 MONITORING EQUIPMENT

We used two instruments to monitor and record our testing results: The Dranetz-BMI PowerXplorer® PX5 and the Rigol DS1074Z 70Mhz. Both oscilloscope instruments were used to monitor and record the AC voltages at the output of the inverter under test during our testing but only the Dranetz monitored in addition the DC emulator output voltage as well as the injected currents from the PV inverter. It has eight analog channels in comparison to only four analog channels of the Rigol. Both were used to compare their voltage measurements and thus, enhance our confidence in the data.

4.4.1 Dranetz-BMI PowerXplorer® PX5

The Dranetz PX5, seen in Figure 8, is a portable, hand-held, 16 bit ADC, eight-channel power quality meter/monitor with a high-speed sampling board for capturing the details of fast transients. This power quality instrument is designed with a touch screen color liquid crystal display (LCD). It has four differential voltage inputs, 1-600 Vrms, and four inputs with current transformers (CTs) 0.1-6000 Arms CT-dependent, a high-speed sampling and data capture (1 microsecond/channel). It records samples at 256 samples/cycle and can be used for both AC and DC applications. Concerning the triggering modes, it can do independent voltage and current triggering with cross triggering. [12]

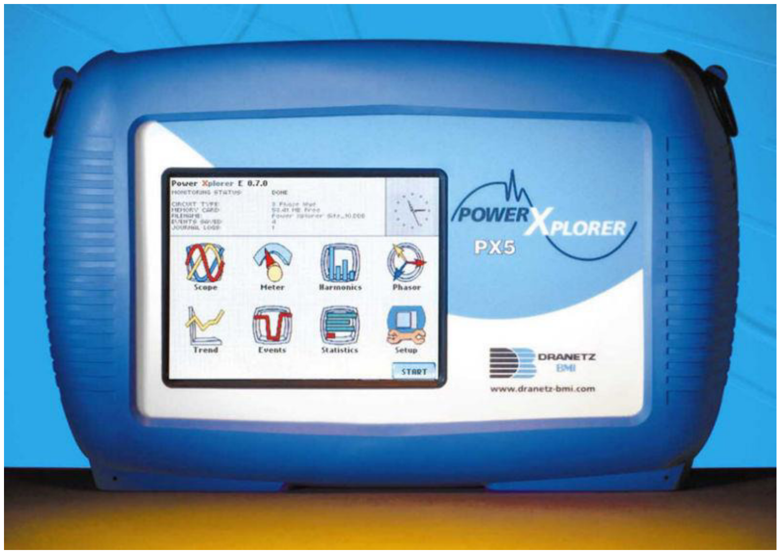

Figure 8. Dranetz PX5 [12]

We used the PX5 to record the line to neutral voltages Va and Vb of the load (lab bench B), the injected currents Ia and Ib of the inverters and the DC voltage from the PV simulator. The measurements were processed through the software called DranView to sort the data and exported to be used in Matlab for analysis.

4.4.2 Rigol DS1074Z 70Mhz

The Rigol DS1074Z 70Mhz (see Figure 9) is an 8-bit ADC digital oscilloscope with a 70MHz Bandwidth, 4 channels, a 1GSa/s real-time sample rate and a waveform capture rate of up to 30,000 wfms/s (waveforms per second). One advantage of the Rigol is that the waveforms can be directly saved to a flash drive in the CSV format, but the shortage of channels makes it impossible to monitor all necessary currents and voltages with this instrument.

Furthermore, it has a lower resolution than the PX5 and fewer trigger modes, thus it was not our main scope during our test. We used it mainly as a back up scope to record line-to-neutral inverter voltages and then compare them with the waveforms recorded by the Dranetz, to double-check our measurements. [13]

Figure 9. Rigol DS1074Z

4.5 VARIABLE AUTOTRANSFORMERS

Because of the transients created by the sag generator during its switching operations, we needed to do some load matching to mitigate the effect of the sag generator transients to get reliable results. However, the load of the benches is fixed and can only be changed in discrete steps, so we reconfigured lab bench 5 by connecting three single-phase variable autotransformers (variacs), seen in Figure 10, to the three single-phase load resistors of lab bench 5 as shown in Figure 11. This provides a variable and controllable 1-kW load in parallel with step-switched loads.

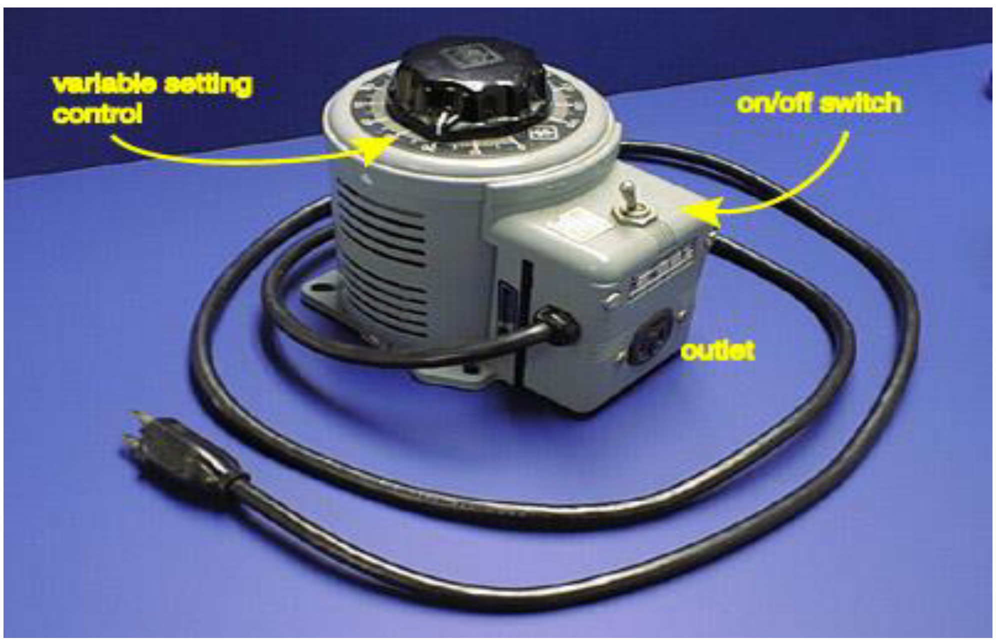

Figure 10. Example of a variable autotransformer [14]

Figure 11. Variacs connected to the load resistors

Variacs provide a voltage-adjustable source of alternating current (AC) electricity. Plugged into a wall outlet, they have a knob-controlled output that can range from 0 volts AC (VAC) to about 140VAC, depending on how the winding is connected. Let the primary side (grid) and secondary side (load) voltage ratings (single-phase voltage corresponding to each variac) be V_G (120V) and V_L (0 - 140V), respectively. The number of turns in primary and secondary side are N_G and N_L respectively. The voltage ratio and current ratio are respectively given by the equations $V_G/N_G = V_L/N_L$ and $I_G*N_G = I_L*N_L$. So we could easily control the voltage and current at the load side, thus we could control the load power output. Thus by monitoring the load power from the bench, we tuned it to match the power output from the inverter [15].

As seen in Figure 12, just before the voltage goes to zero (short-circuit), at the left, we can see that the line-to-line voltage dropped from 300V to 250V (red circle) but at the right, there is no voltage drop. That is due to the mitigation of the sag generator "break-before-make" phenomenon by load matching. It minimizes effect on the inverter during short period when the sag generator is open.

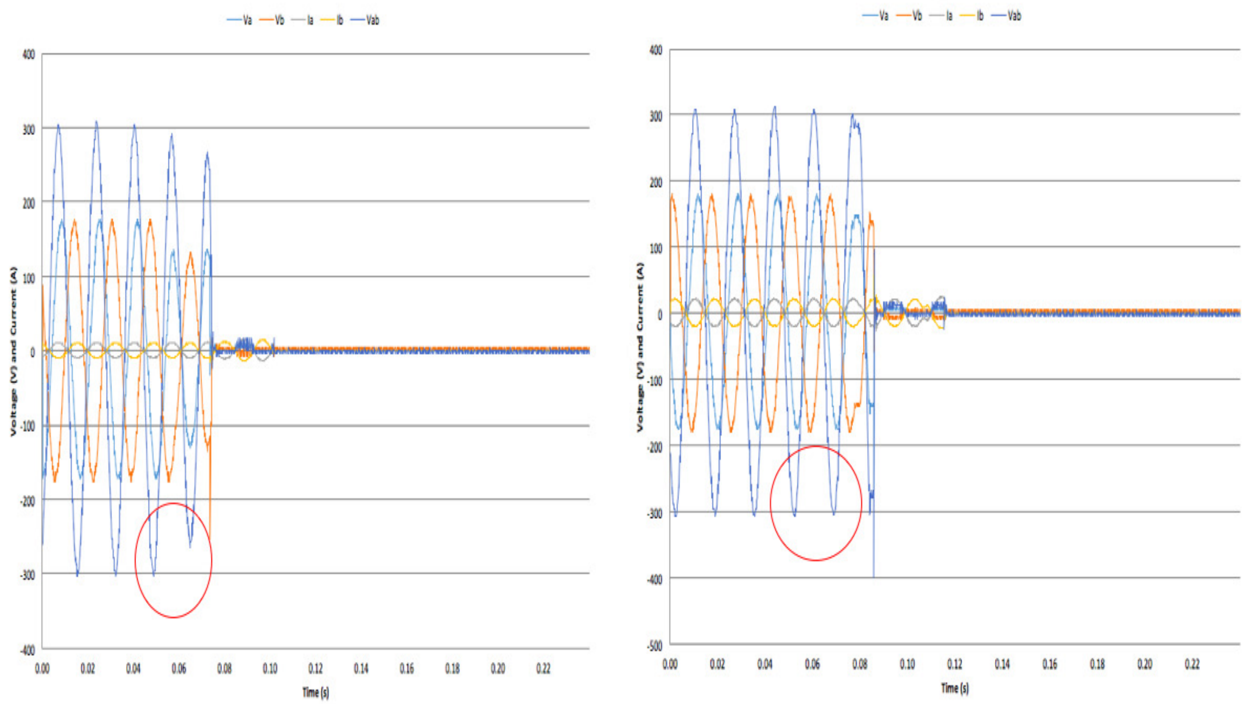

Figure 12. Voltage waveforms during a short-circuit test - Before load matching (Left) - After load matching (Right)

4.6 PHOTOVOLTAIC INVERTERS

A PV inverter, shown in Figure 13, or solar inverter, converts the variable direct current (DC) output of a PV solar panel into a utility frequency alternating current (AC) that can be fed into a commercial electrical grid or used by a local, off-grid electrical network. It is a critical balance of system (BOS) component in a photovoltaic system, allowing the use of ordinary AC-powered equipment. PV inverters have special functions adapted for use with photovoltaic arrays, including maximum power point tracking (MPPT) and anti-islanding protection. We used only single-phase PV inverters throughout the testing reported in this thesis. [16]

Figure 13. Example of an inverter (not tested in this project) [17]

4.7 SWITCH

The switch shown in Figure 14, is connected between the PV inverter and the load (Lab bench 5). It is used to manually connect or disconnect the tested inverter from the grid to simulate an open-circuit event.

Figure 14. Three-phase rotary switch [18]

4.8 LAPTOP

The PV emulator is controlled by a personal computer (PC) via a GUI display (see Figure 15). We can use it to change parameters such as the solar irradiance level, temperature value, voltage, current, and temperature coefficient in order to modify the voltage-current curve emulated by the simulator at a given test condition. One application of the emulator is to test inverter MPPT functions over a range at operating conditions. We used it to set specific operating points, for example 25% output, prior to each short-circuit or open-circuit test.

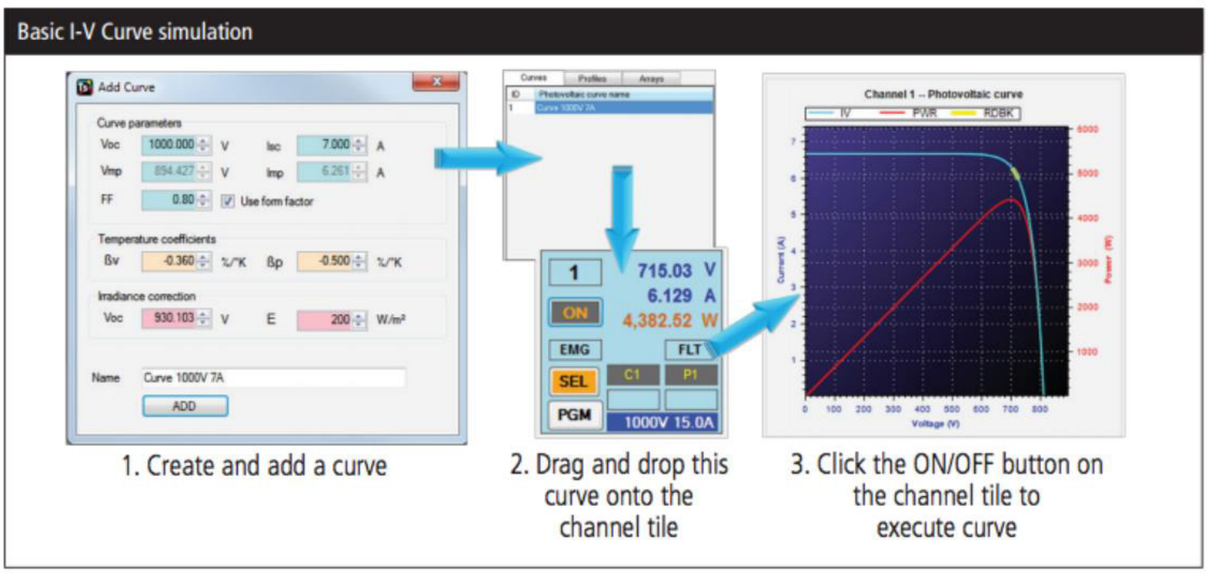

Figure 15. PV simulator software interface [9]

4.9 CONFIGURABLE THREE-PHASE TRANSFORMER BANK

A three-phase wye (ground)/wye (ground) transformer bank (comprised of three single-phase transformers) rated 6 kVA is connected between the inverter under test and lab bench 5. This transformer is used for grounding purposes and to synchronize the grid voltages and the inverter AC voltages during the testing. This transformer bank is shown in Figure 16**.** Via the patch pad, it can be reconfigured into various wye and delta configurations, as well as the single-phase residential center-tapped secondary transformer.

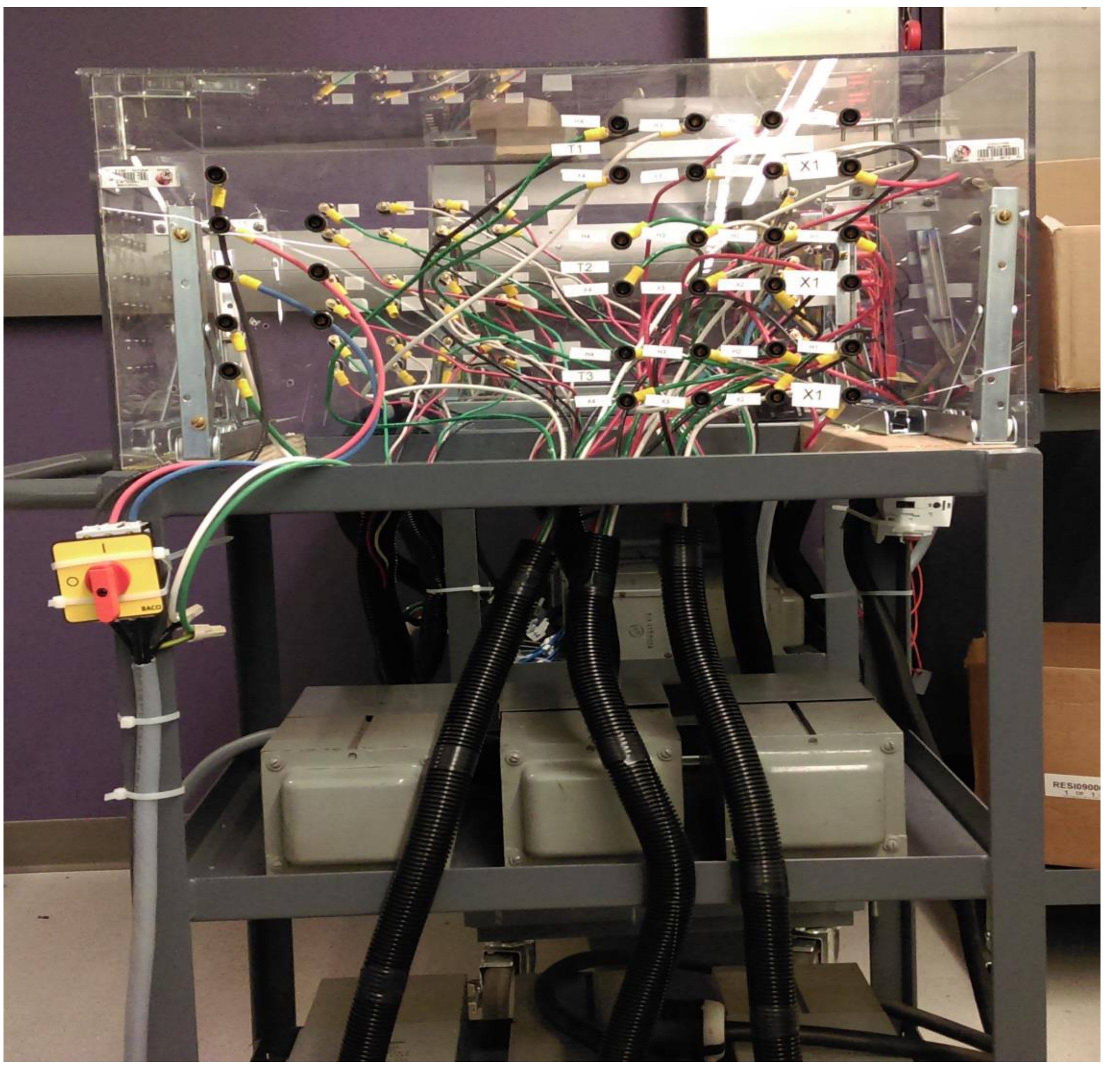

Figure 16. Three-phase transformer bank

5.0 TEST PROCEDURES

Using the test-set up described in section 4.0, we designed our test procedure to be universally applicable to all PV distributed resources. The test procedure is used to evaluate the behavior of inverters in two transient scenarios: open circuit and short circuit. We tested independently four different single-phase inverters at four different output levels, namely 25%, 50%, 75% and 100% of rated output because we needed to determine if the power output level of the inverter had an impact on the magnitude of its transients. In addition, for each inverter, at each power output level, we performed fifteen shots for short circuit tests and three shots for open circuit tests to take into account point-on-wave effects. Point-on-wave effects can be defined in our context as the fact that because a fault can occur at any given moment, the grid voltage being at peak, zero or any other value, this can create different effects, for example, different values of overvoltages or overcurrents at the inverter output. So we did multiple shots to make sure to record the possible variations. The rated power levels for the four single phase inverters is indicated in Table 1.

Table 1. List of tested inverters

Inverter Name	Type	Size
Inverter A	Single-phase	2kW
Inverter B	Single-phase	3kW
Inverter C	Single-phase	2.8kW
Inverter D	Single-phase	2kW

Using the log sheet (all the logs are in the appendix) to keep track of the tests done to a given inverter for each inverter under test, we executed the following sequence:

1) Complete each column's test sequence within the same lab period.
2) Assign a unique record number for each shot; this will become part of the data file name. Manually record a key variable for each shot, either a peak voltage/current or the time when the shot is recorded. Other observations may be written at the bottom of the log sheet.
3) Power the lab and all the testing equipment (reference the lab safety procedure). [8]
4) Pre-test setup for each inverter: lower the default reconnection time from 5 minutes to 5 seconds to avoid waiting 5 min between each test, and thus increase the testing efficiency.
5) Set the PX5 and Rigol to trigger on AC voltage disturbances and wave-shape faults.

6) **For open-circuit tests (Figure 17) :**

a) Set the emulator to produce nominal DC output voltage for the inverter under test.

b) Close the Switch to Lab Bench 5 (Figure 2) and wait for the inverter to connect.

c) Change the emulator DC output to 25, 50, 75, or 100% of the inverter rating.

d) Open the switch to simulate the open-circuit test.

e) Record key values and record number from the PX5; ensure that all channels were recorded.

f) When the inverter reconnection time has elapsed, repeat from 6a for the next shot.

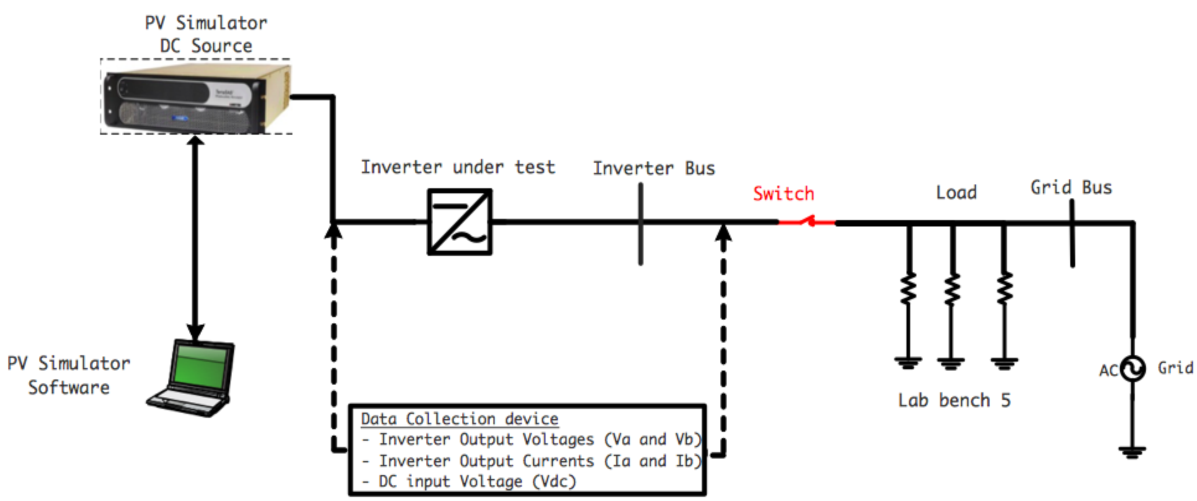

Figure 17. Open-circuit diagram

7) **For short-circuit tests (Figure 18),** the procedure is nearly the same as for open-circuit tests, except for 7d and 7e:

a) Set the emulator to produce nominal DC output voltage for the inverter under test.

b) Close the Switch to Lab Bench 5 (Figure 2) and wait for the inverter to connect.

c) Change the emulator DC output to 25, 50, 75, or 100% of the inverter rating.

d) Operate the variacs till the power output of the inverter is matched by the lab bench 5 (load power).

e) Initiate a 0% voltage sag on all three phases, lasting 180 cycles, at the sag generator interface (Figure 7).

f) Record key values and record number from the PX5; ensure that all channels were recorded.

g) When the inverter reconnection time has elapsed, repeat from 7a for the next shot.

8) At the end of the testing session, power off the lab and disconnect all power cords from lab benches; stow cables underneath the benches.

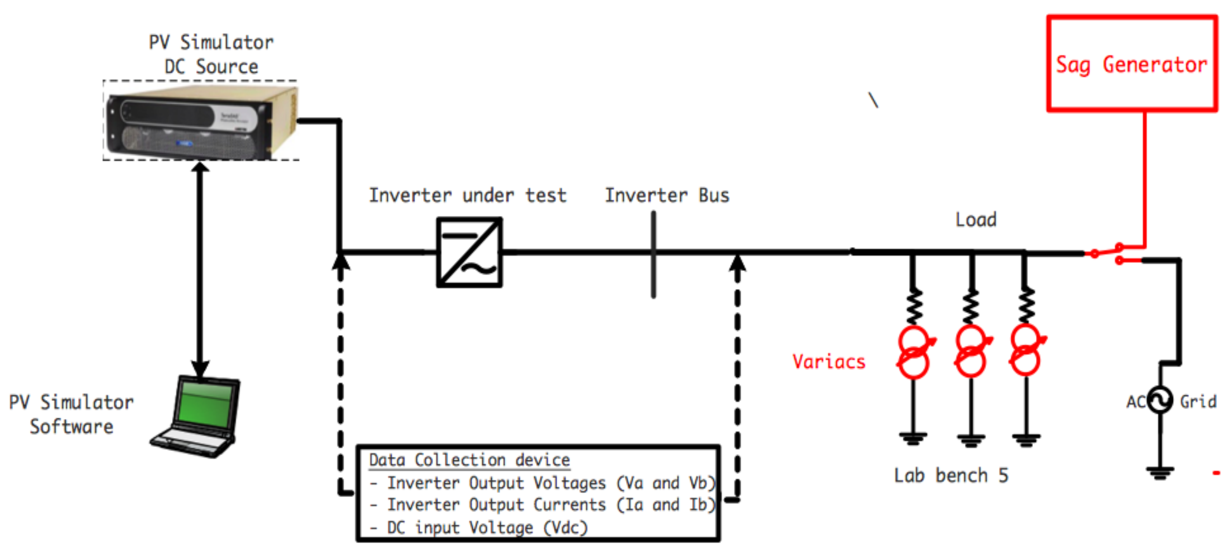

Figure 18. Short circuit diagram

6.0 DATA PROCESSING

As indicated in the test procedure, four inverters were each tested for both open-circuit and short-circuit tests. The data was stored using the compact flash (CF) card internal to the Dranetz PX5 and then was downloaded to a PC. As said previously, the data from the scope can be viewed using the DranView software but the software does not allow the data to be mathematically processed. Therefore, we created a software script using AutoHotkey (AHK) software which can be used to automate some tasks on Windows OS. This AHK script exported the PX5 data into comma-separated value (CSV) files. Then, a MATLAB script was created to import the CSV files created by AHK into MATLAB. A block diagram showing the flow of data processing is shown in Figure 19.

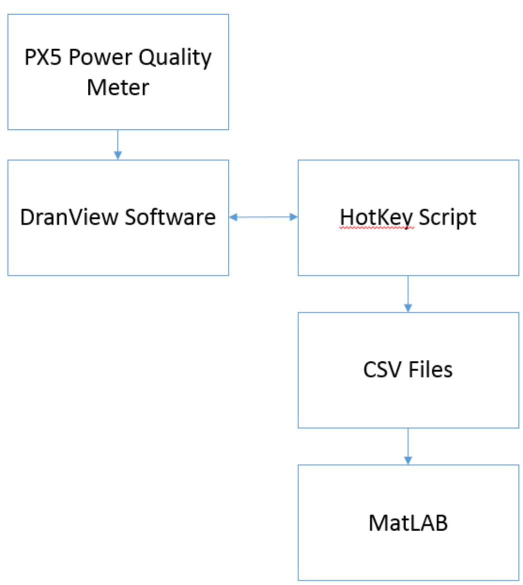

Figure 19. Flow of Data Processing

The script in MATLAB was written so that the data could be viewed, plotted, and analyzed with respect to the inverter manufacturer (Inverter A-D), type of test (open-circuit, short-circuit), and the inverter output power (25%, 50%, 75%, 100%). The majority of the mathematical processing is currently done using MATLAB. Concerning the data from the Rigol scope, we directly used its save options to store the data to a flash drive in CSV files. Then we processed these CSV files in the same way we processed those from the AHK script.

7.0 TEST RESULTS

All test results for OC and SC testing are provided in the following sections for each of the four tested inverters. As stated before, OC testing was repeated three times and SC testing was repeated fifteen times to take into account point-on-wave effects. Each inverter had unique responses to the fault events, making it difficult to see the common points between them. This section contains some waveforms that are considered typical inverter responses, along with others that had a unique, outlying, or particularly interesting response.

Each waveform plot shows the line to neutral AC terminal voltages Va and Vb, the line to neutral inverter currents Ia and Ib and the line to line terminal voltage Vab. However, the inverter D is missing some data because of a corrupted CF card that we used to record the data, which deleted some measurements.

7.1 INVERTER A

7.1.1 Open-circuit

Figure 20 shows the worst case scenario waveforms of inverter A during open circuit testing at 100% power output (2kW). After we closed the switch and isolated the inverter from the grid, the current went to zero immediately as expected, but the line to neutral voltages, Va and Vb, became a square wave during one cycle, reaching saturation at 1.372 p.u. Then they decreased linearly until they reached zero. This particular behavior is due to the internal control of the inverter, which might have a saturation block to prevent the overvoltage from becoming too high.

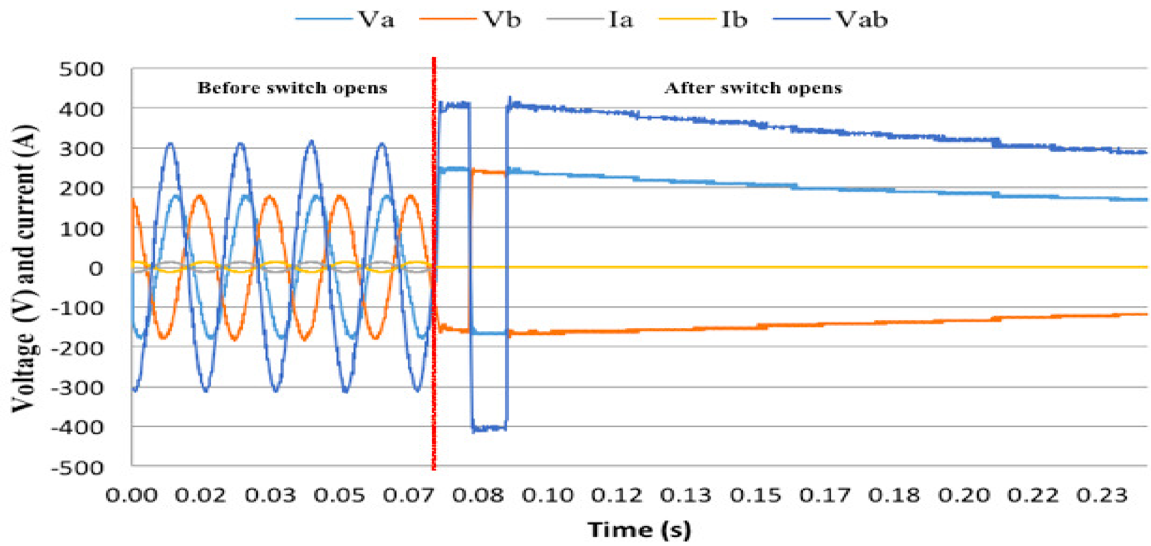

Figure 20: Inverter A - Waveforms during OC test

7.1.2 Short circuit

Figure 21 shows the worst case scenario waveforms of inverter A during SC testing at 100% power output (2kW). After creating a sag to 0%, there is a small spike of the voltage at 1.3 p.u. w that quickly goes to zero, then, there are overcurrents just after the sag event at about 0.14s (see Figure 22) where both currents spiked from 14.4A to 75.2A (7.52 p.u.), peak values. Finally, the currents decay to zero in a damped oscillation after about 9 cycles.

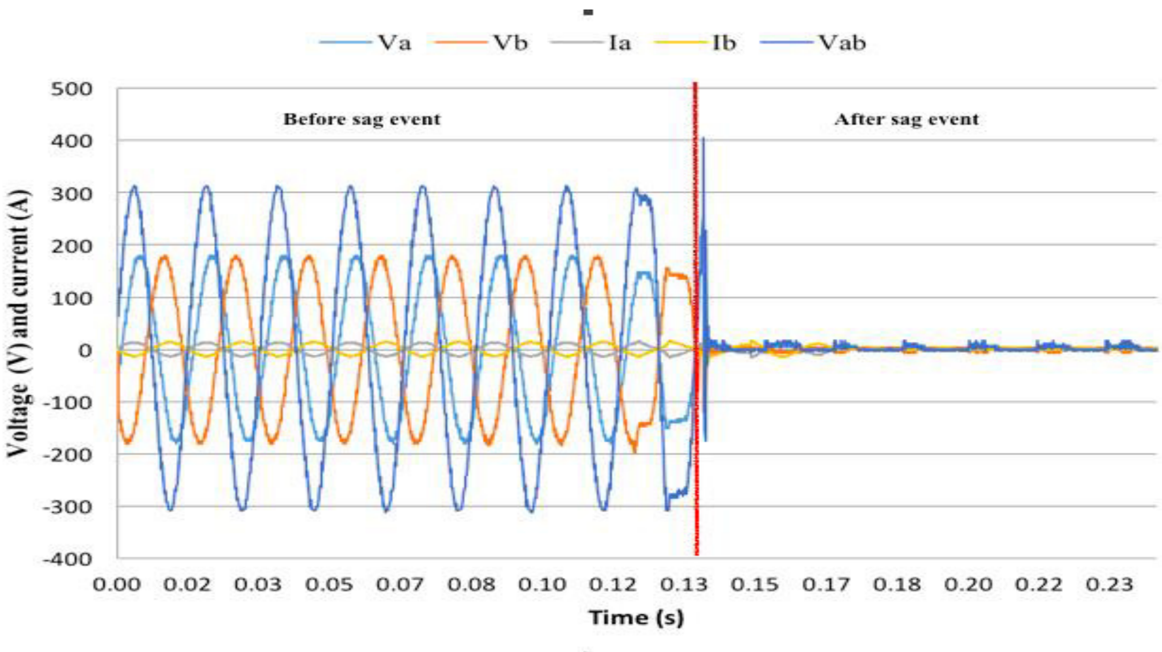

Figure 21. Inverter A - Waveforms during SC test at 100% power output (Worst case scenario)

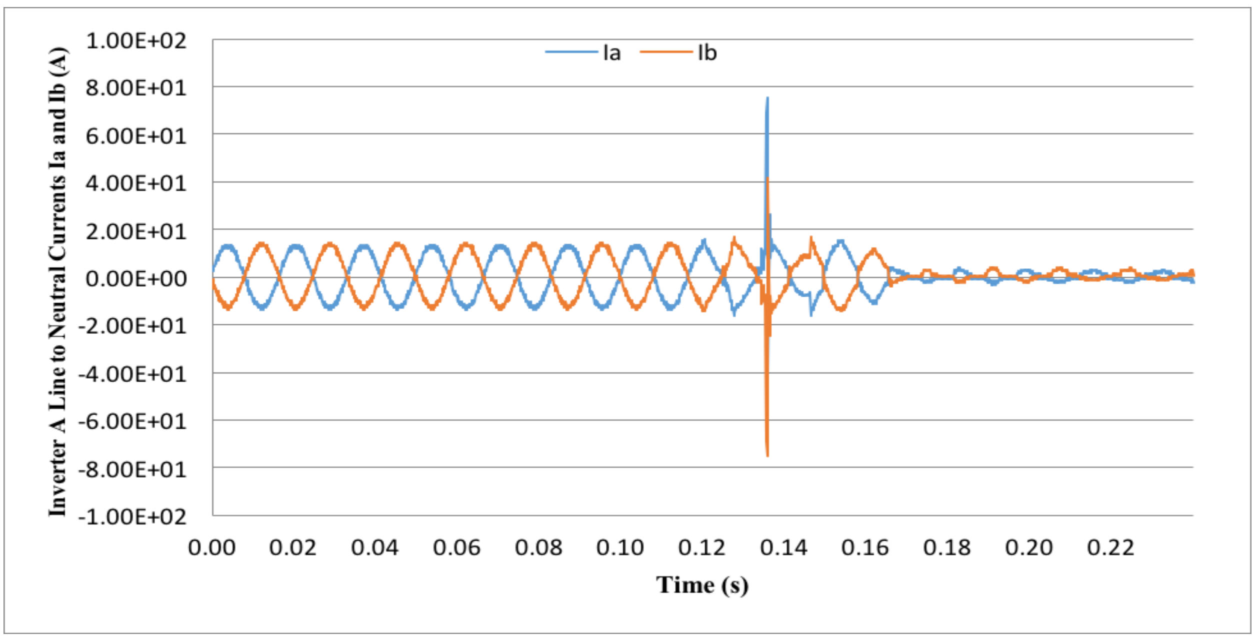

Figure 22. Inverter A – Line to neutral currents at 100% power output (Worst case scenario)

7.2 INVERTER B

7.2.1 Open-circuit

Figure 23 shows the typical waveform plot of the inverter B during an OC event. It is interesting to see that it is different from Inverter A by the fact that after the fault event, the slope at which the voltages are decreasing is really small in comparison to slope of Inverter. The voltages stay almost constant after 9 cycles and the peak continuous voltage after and before the fault event is almost the same (not taking into account the spike just after the switch is opened).

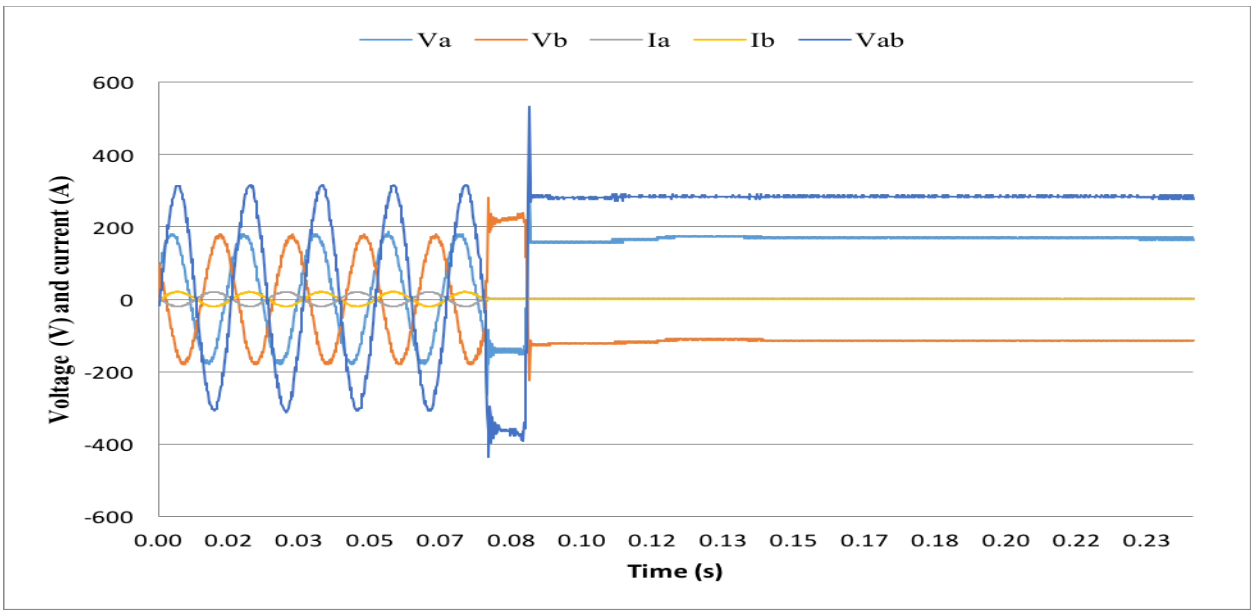

Figure 23. Inverter B – Typical waveforms during OC test

7.2.2 Short circuit

In contrast to the plot waveforms during open circuit tests, the waveforms during SC tests are pretty similar between inverter A and B. The main difference is the time for the current to reach zero after the sag event. This duration is between 6 to 10 cycles for inverter A and 3 to 4 cycles for inverter B. Also the overvoltage values are generally lower for Inverter B than Inverter A.

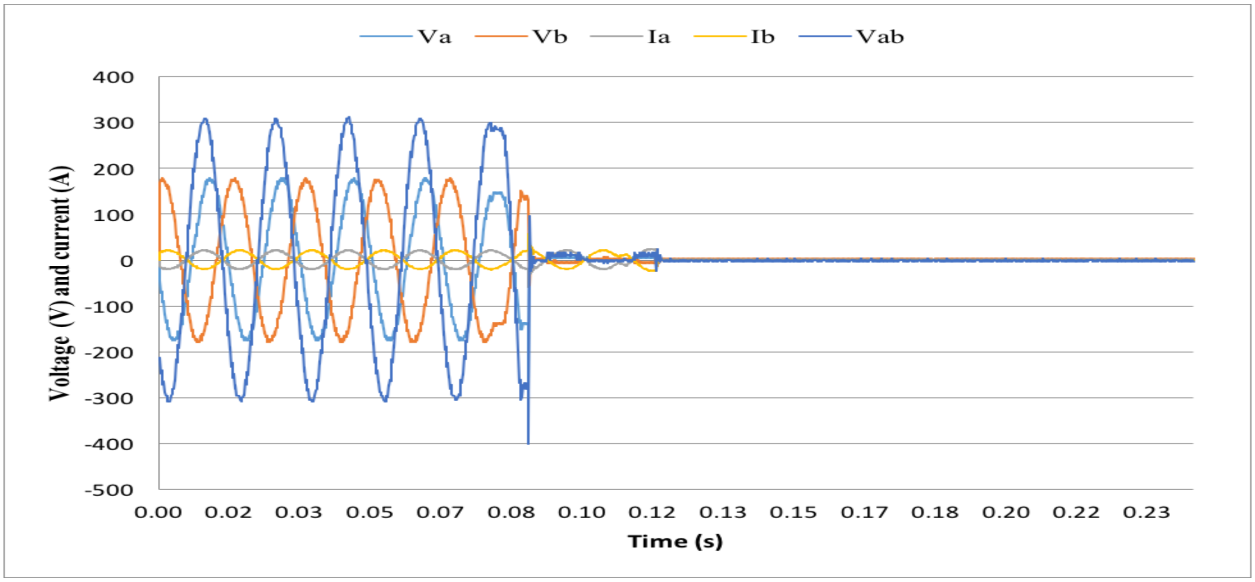

Figure 24. Inverter B – Typical waveforms during SC test

7.3 INVERTER C

7.3.1 Open-circuit

A common response of inverter C is shown in Figure 25. Just after the opening of the switch, the voltage Va spiked to 1.72 p.u. and then decayed, leading to immediate shut down. This plot looks almost like the underdamped response of a second order system and that could be the main focus to characterize the transient response of inverter C during open circuit events.

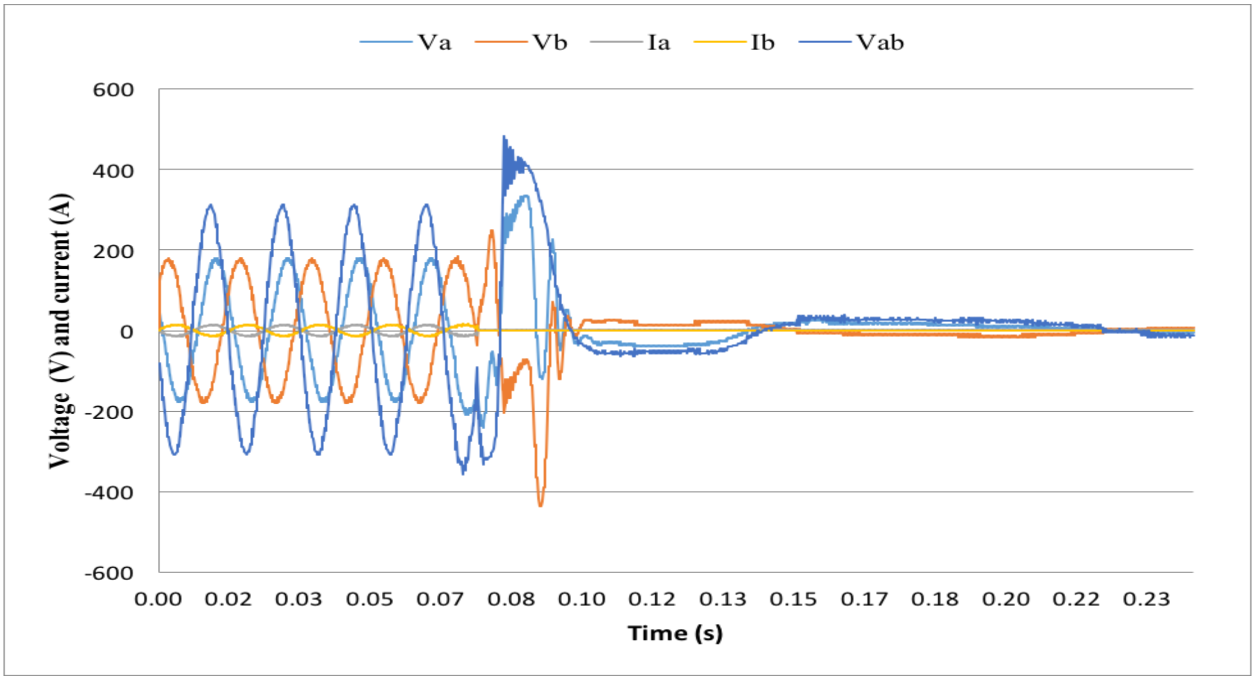

Figure 25: Inverter C - Waveforms during open circuit test at 100% power output

7.3.2 Short circuit

The SC response, seen in Figure 26, looks the same as for the other inverters, with the difference being again the number of cycles after the transient event for the current to die off. In comparison to inverters A and B, inverter C current dies off pretty quickly, generally after 0.5 – 2 cycles.

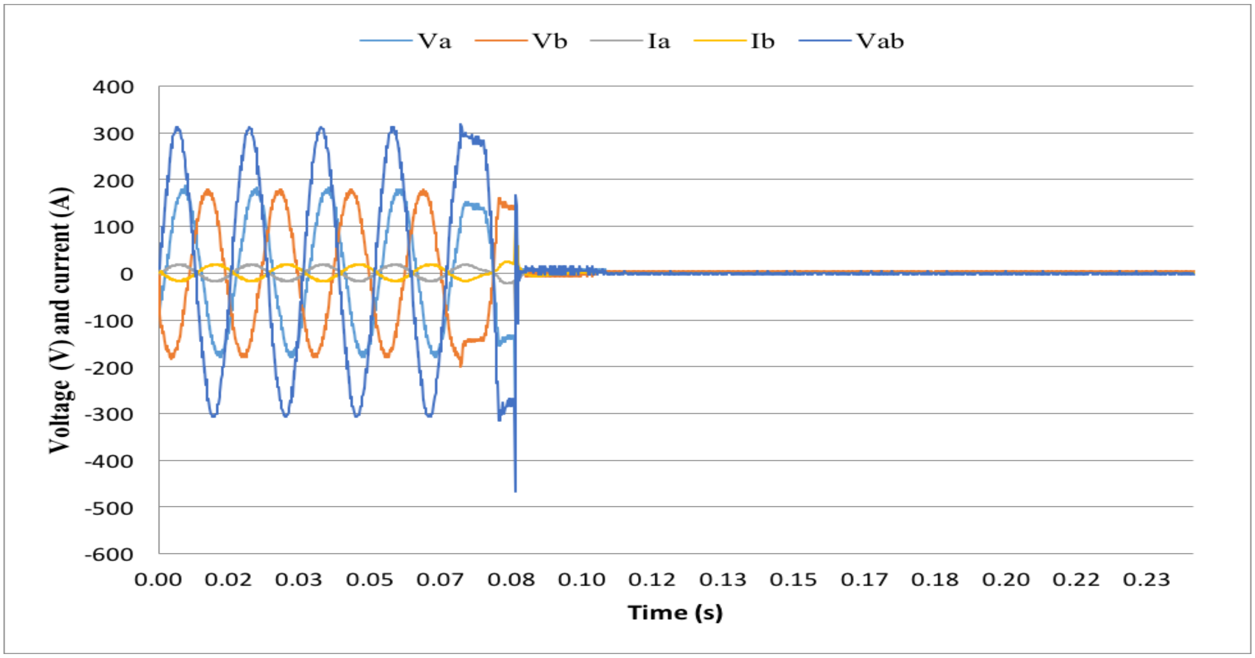

Figure 26. Inverter C - Waveforms during SC test at 100% power output

7.4 INVERTER D

7.4.1 Open-circuit

Figure 27 and Figure 28 show two responses (currents are missing) of inverter D during open circuit at respectively 100% and 50% power output. The waveforms are almost square after the fault event for 2 to 3 cycles and they increase in magnitude for the first couple of cycles. The line-to-line overvoltages peak at 480V (1.63 p.u.) then the voltage decays to zero. Again this might be due to the saturation scheme of this specific inverter to limit overvoltages. Without this, Figure 27 and Figure 28 indicate that resonant overvoltages could occur.

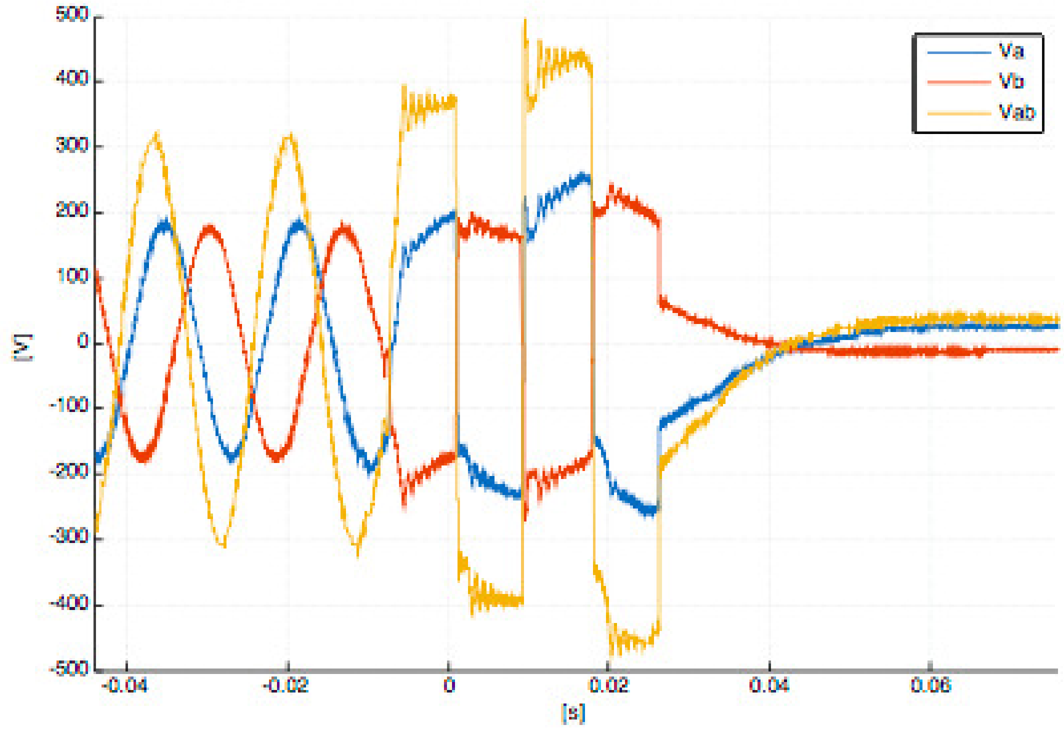

Figure 27. Inverter D - Waveforms during OC test at 100% Power output (Worst-case scenario)

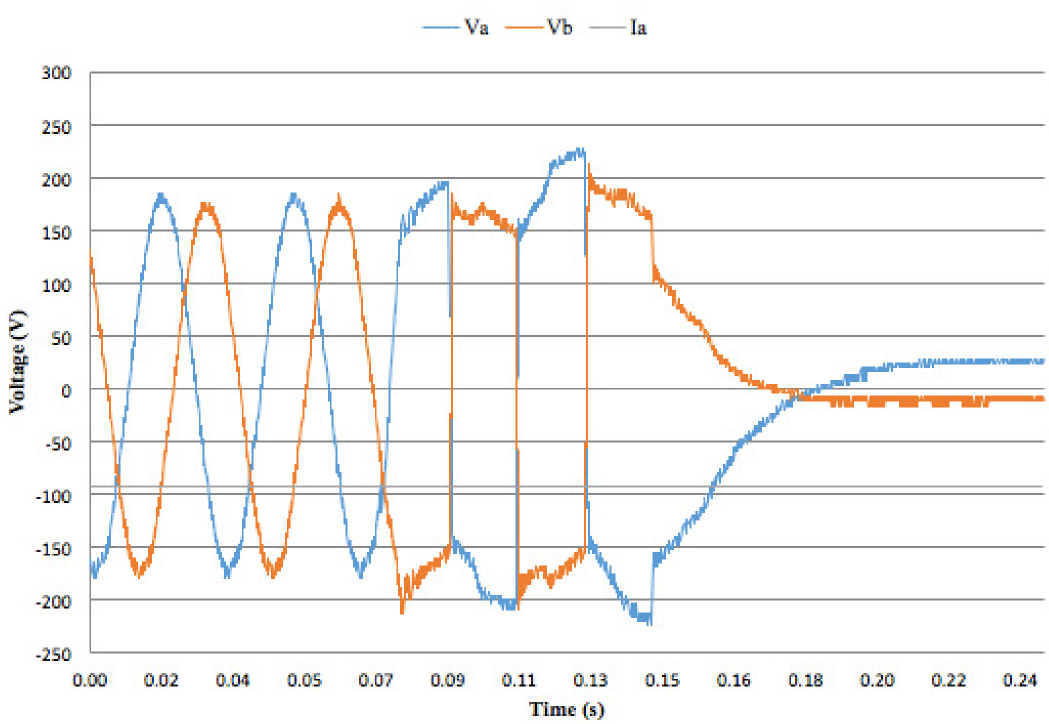

Figure 28. Inverter D - Waveforms during OC test at 50%

7.4.2 Short circuit

Figure 29 and Figure 30 show two typical responses (voltage Vab and current Ib are missing) of inverter D during open-circuit at respectively 25% and 100% power output. The inverter D responses have in general no overvoltages after the transient event, and the current lasts for 1-3 cycles.

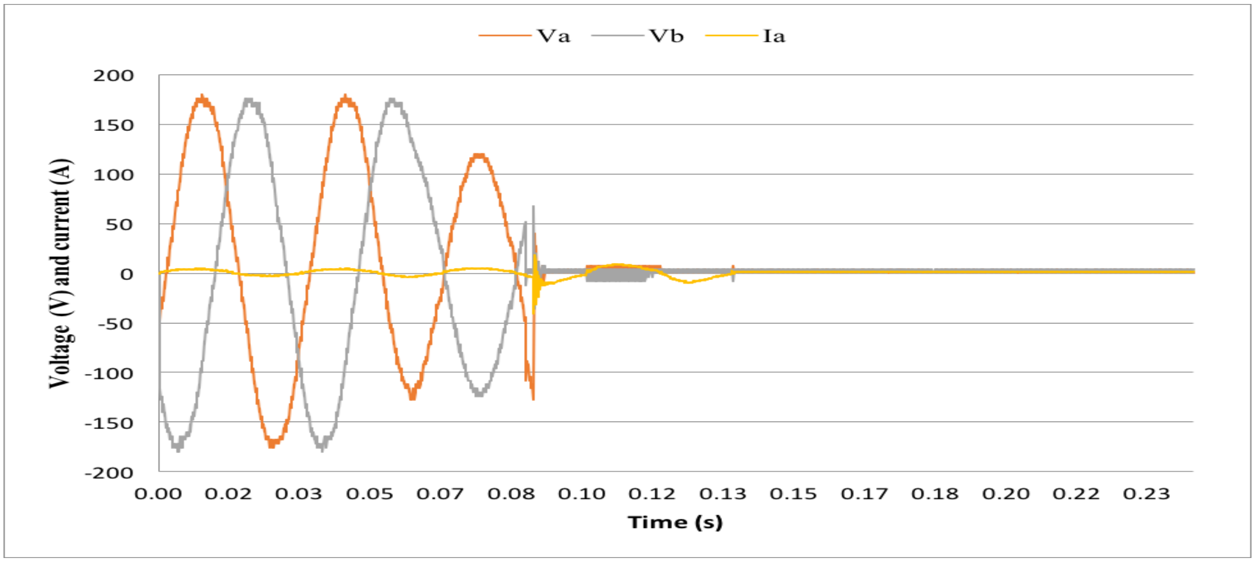

Figure 29. Inverter D - Waveforms during SC test at 25% power output

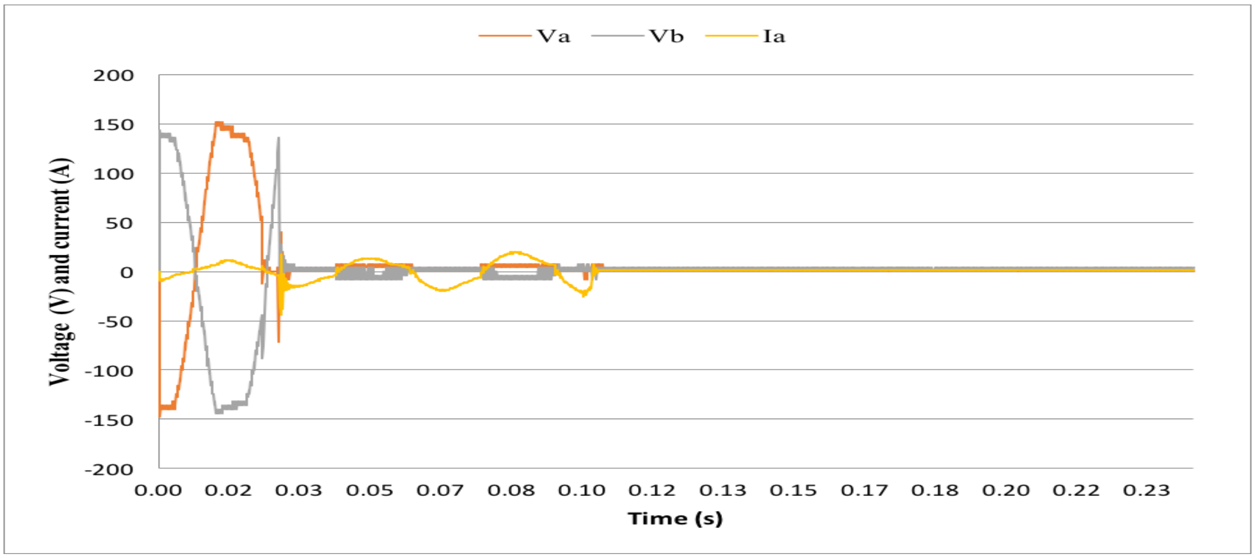

Figure 30. Inverter B - Waveforms during SC test at 100% power output

8.0 OBSERVATIONS

To save time due to the long period it could take to analyze all the data recorded from our testing, one method used for viewing transient over-voltages (TOV) and transient over-currents (TOC) produced through OC and SC tests is through spectrum plots. Spectrum plots compare the per unit (p.u.) TOV or TOC to the power output level in percentage.

8.1 OVERVOLTAGE SPECTRUM PLOTS

In order to provide preliminary overvoltage results, the spectrum plots for three of the single-phase inverters and the corresponding maximum and minimum overvoltages with the respective power output level percentage for each of the open circuit tests are outlined in this section.

The voltage spectrum plot for Inverter A is shown in Figure 31. The largest overvoltage was 1.37 per unit voltage and occurred at 100% power output level. The lowest overvoltage occurred at 25% power output level and reached 1.28 per unit voltage. In addition, we can also notice that the peak TOV is increasing in general with the power output level for inverter A.

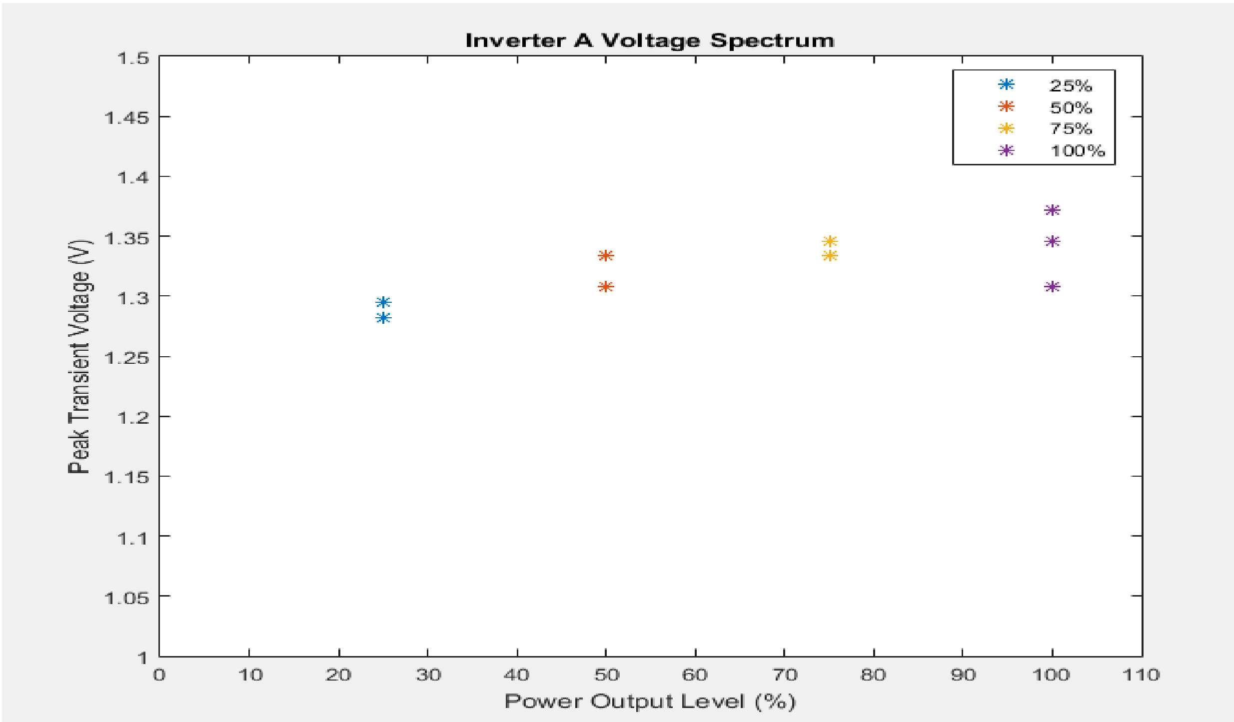

Figure 31. Inverter A – OC Voltage Spectrum

The voltage spectrum plot for Inverter B is shown in Figure 32. The largest overvoltage for it was 1.75 per unit voltage and occurred at both 75% and 100% power output level. The lowest overvoltage occurred at 75% power output level and had an overvoltage of 1.368 per unit voltage. Moreover, for inverter B, the range of peak TOV gets larger with the increase of power output level (the range goes from 0.16 p.u. at 25% to 0.35 p.u. at 100%).

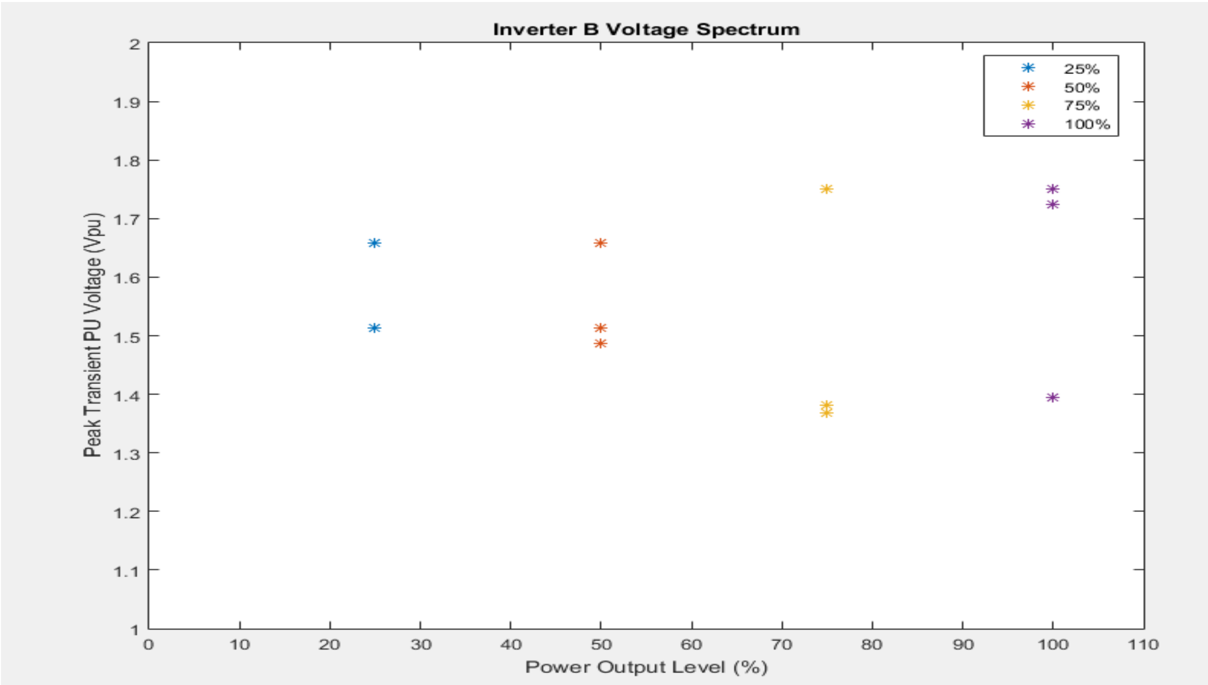

Figure 32. Inverter B – OC Voltage Spectrum

The voltage spectrum plot for Inverter C is shown in Figure 33. The largest overvoltage was 1.64 p.u. voltage and occurred at 50% power output level. The lowest overvoltage occurred at 25% power output level and reached 1.07 per unit voltage. Furthermore, in the contrast with inverter B, the range of peak TOV of inverter C gets smaller with the increase of power output level (peak TOV range goes from 0.46 p.u. at 25% to 0.03 p.u. at 100%).

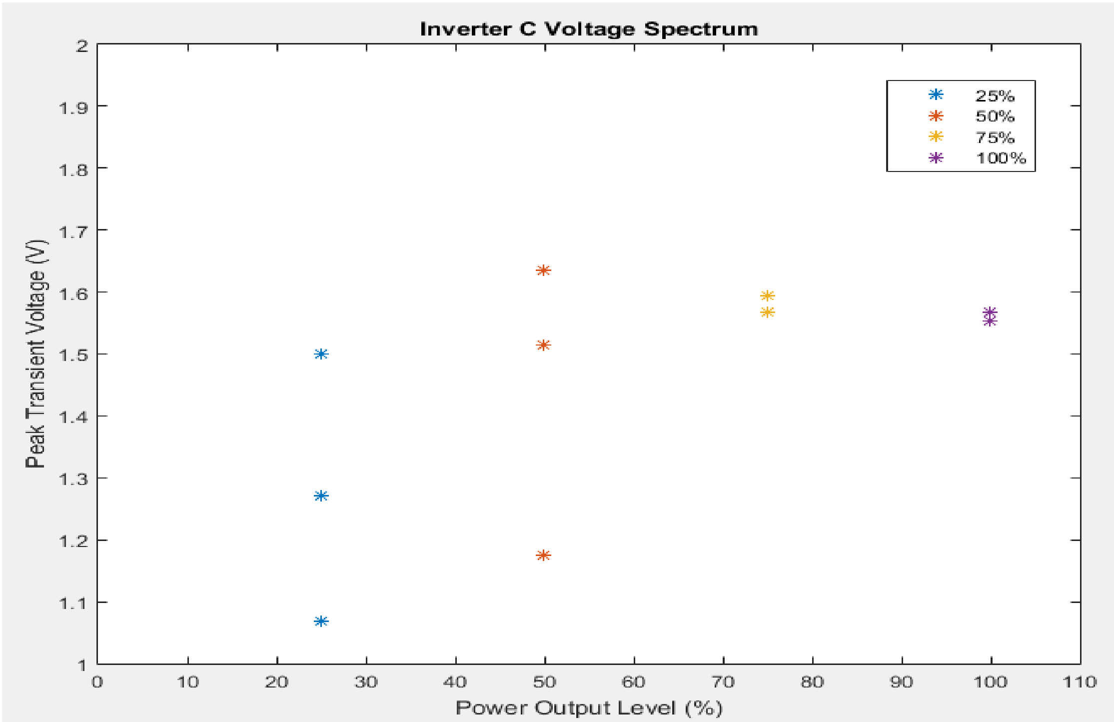

Figure 33. Inverter C – OC Voltage Spectrum

The overvoltage spectrum for Inverter D is shown in Figure 34. (Note: the per unit values for Inverter D were determined using the peak line to neutral voltage). The largest overvoltage was 1.38 per unit and occurred at 100% power output level. The lowest overvoltage occurred at 25% power output level and reached 1.08 per unit. The overvoltage increases with inverter output power level and is not affected much by point-on-wave effects.

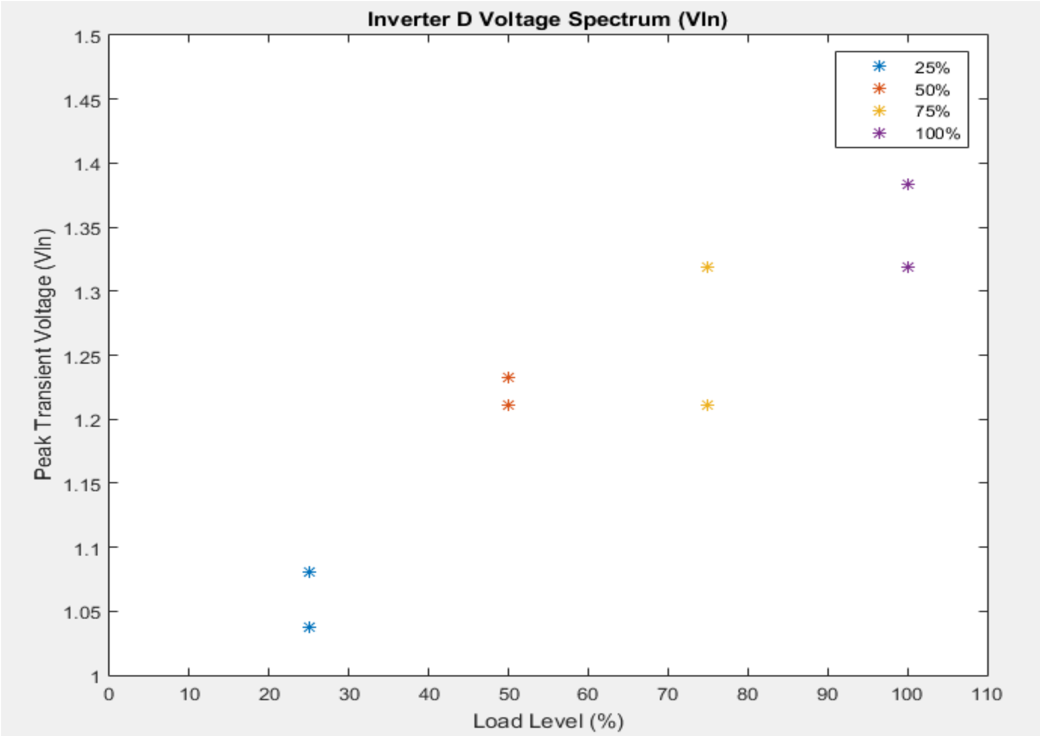

Figure 34. Inverter D – OC Voltage Spectrum

One interesting point is that the maximum overvoltage recorded from all our testing of the single-phase inverters was 1.7 per unit voltage or less, is as expected in prior theoretical research [19].

8.2 OVERCURRENT SPECTRUM PLOTS

In order to provide preliminary results, the TOC and TOV spectrum plots for the four single phase inverters are included in this section. Overall, the peak TOV is smaller during SC tests than OC tests as we would expect. For a given SC shot, a higher TOV value doesn't imply a higher TOC value. In addition, each inverter has several unique behaviors listed below.

- **Inverter A**

The higher the peak TOV, the higher the peak TOC. There is a direct correlation between peak TOC values and peak TOV values for inverter A, but surprisingly, the peak TOV (1.5 per unit) and peak TOC (12 per unit) are reached at 75% of the rated power output instead of 100%.

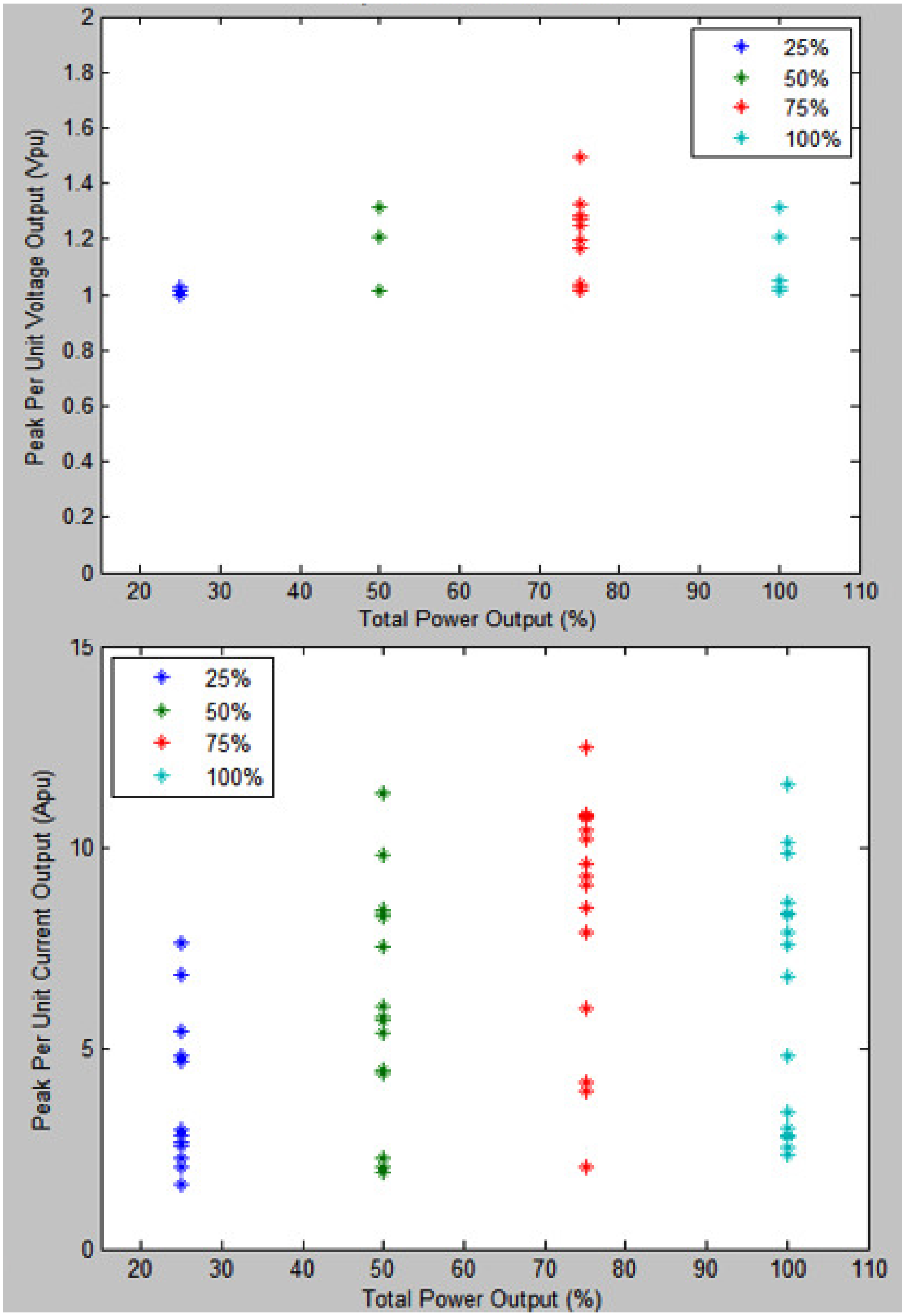

Figure 35. Inverter A - Short Circuit Test - TOV Spectrum (Top) and TOC Spectrum (Bottom)

- **Inverter B**

Inverter B reached almost its maximum TOC value at 25% (4.75 per unit), 50% (4.77 per unit) and 100% (4.9 per unit) power output levels but at 75%, the peak TOC is just 3.75 per unit.

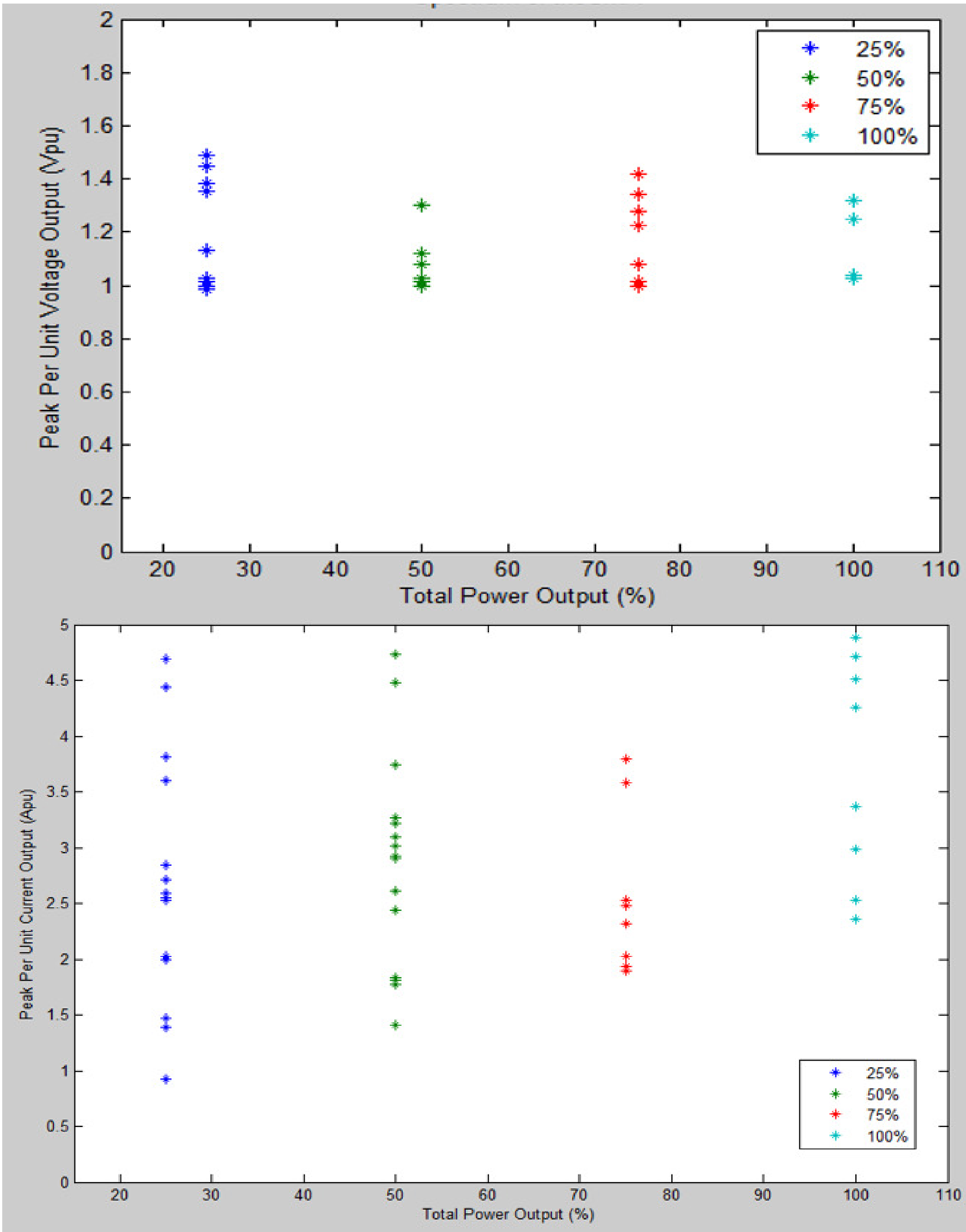

Figure 36. Inverter B – Short circuit Test - TOV Spectrum (Top) and TOC Spectrum (Bottom)

- **Inverter C**

Inverter C reached its peak TOC at the three highest power output levels at which it was tested, 50% (14.85 per unit), 75% (14.88 per unit) and 100% (14.9 per unit). However, the peak TOV (1.7 per unit) is only reached at 75% power output level. Overall, the peak TOC value can occur at almost any given power output level of 50% or greater for inverter C. And similarly to inverter A, the peak TOV value (1.7 per unit) is recorded at 75% of rated power output.

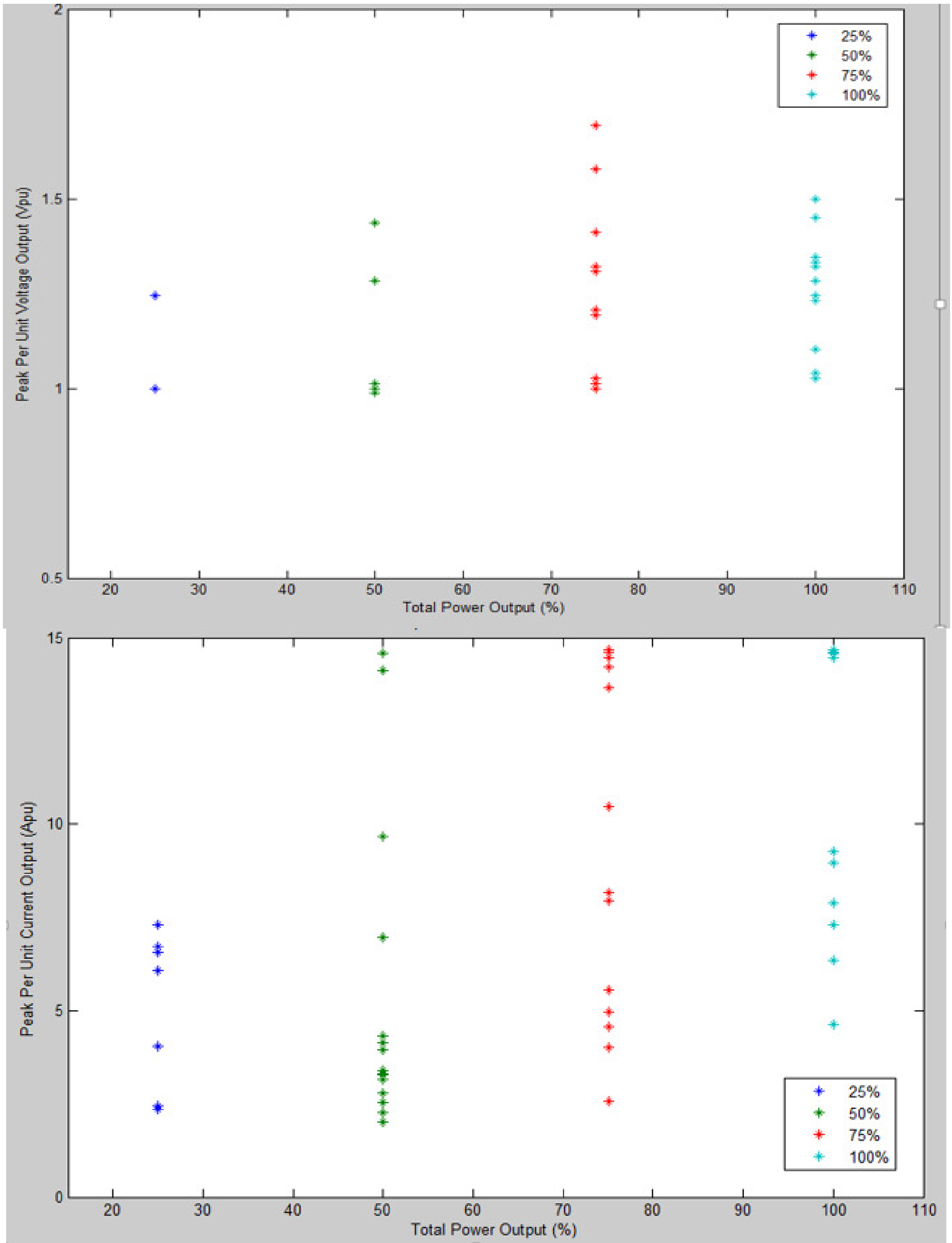

Figure 37. Inverter C - Short Circuit Test - TOV Spectrum (Top) and TOC Spectrum (Bottom)

- **Inverter D**

The higher the TOV, the higher the TOC so there is a direct correlation between peak TOC values and peak TOV values just as inverter A, but in this case, for inverter D, the peak TOV (1.67 per unit) and peak TOC (9.85 per unit) are reached at 50% of the rated power output instead of 100%.

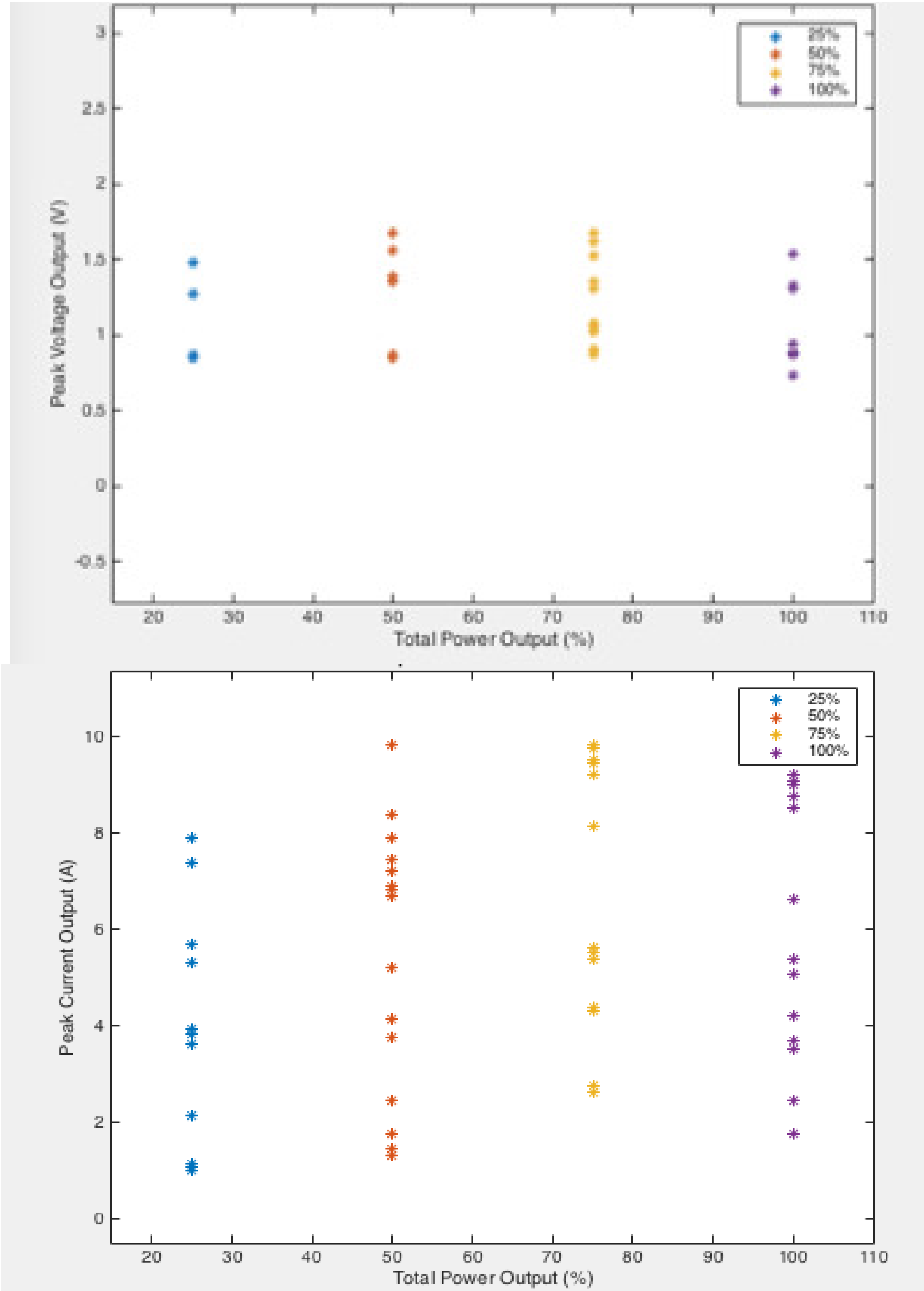

Figure 38. Inverter D - Short Circuit Test - TOV Spectrum (Top) and TOC Spectrum (Bottom)

8.3 SUMMARY OF SPECTRUM PLOTS

A recap of all the extremum values from the short-circuit and open circuit single-phase inverter tests are shown in Table 2 and Table 3.

Table 2. Maximum and average values of overvoltage's during OC testing

Inverter	Worst case TOV (per unit)	Average TOV (per unit)
Inverter A	1.37	1.33
Inverter B	1.7	1.5
Inverter C	1.63	1.5
Inverter D	1.38	1.2

Table 3. Extremum values of overvoltages and overcurrents during SC testing

Inverter	Lowest TOV (per unit)	Highest TOV (per unit)	Lowest TOC (per unit)	Highest TOC (per unit)
Inverter A	1	1.5	1.2	12
Inverter B	1	1.5	0.95	4.95
Inverter C	1	1.7	2	14.9
Inverter D	0.73	1.67	1	9.85

9.0 CONCLUSION

This project aims to characterize the behavior of photovoltaic (PV) inverters under various transient, dynamic and unbalanced conditions. To accomplish that, we tested 4 different single phase inverters under critical transient conditions (open-circuit and short-circuit) and collected the data (voltages and currents) to record the transient responses of those inverters. This project successfully quantified the overvoltage and overcurrent transient responses and confirmed the results expected in prior theoretical research [19]. This will be a great help for installers, and utilities that encounter many issues when it comes to interconnection and planning of distributed PV into the distribution grid.

Indeed, utilities are interested in overvoltages created by inverter backfeed because overvoltages may damage other customer equipment such as large-screen TVs or utility-owned surge arresters. Most existing systems are designed to limit those overvoltages with an effective ground at the substation, but inverters do not provide an effective ground. We found that inverter TOV during OC events can go as high as **1.7 p.u.** which should be taken into account during planning studies.

In addition, utilities are also interested in characterizing short circuit behavior of inverters in order to coordinate fault sensing devices, and to make sure existing equipment is not damaged due to additional current from the inverters. The existing system was designed and coordinated assuming short circuit current comes only from the substation. However, we found that during SC events, inverters will inject current in the system that can be as high as **14.9 p.u.** This current can cause misfires of circuit breakers and potentially damage grid equipment if not taken into account during protection studies.

Throughout this testing, we encountered many difficulties. For instance, we had to learn how to configure and use the testing equipment. Especially for each inverter, we needed to learn how to connect it to our system properly reading the installation manual. Moreover, because we were testing it in the lab, we had to sometimes change the software settings of the inverter. For example, we changed the reconnection time, the frequency and voltage limits because our lab system is deliberately less stable than the electric grid those inverters are manufactured for. Therefore, we needed either to get into contact with the company though calls or emails to get some access codes for advanced software settings, or we needed to buy additional devices to communicate with the inverter. Additionally, because each inverter response is different, we needed to reconfigure all the scope triggers whenever we changed the tested inverter, and those triggers were mostly found by trial and error. Furthermore, because the electric lab is relatively new and we were the first to intensively use the sag generator, we encountered some issues such as the “break-before-make” phenomenon, which we solved using load matching. Also, during the testing, there were times when a contactor inside the sag generator was disconnected. As long as the problem was found out rapidly, it was easily solved by just powering off the lab and rewiring this contactor.

Future work includes expanding the range of retained voltage levels at which the single-phase inverters are tested during short circuit events and also begin the testing of three-phase inverters. Concerning the three-phase inverters, more diverse tests could be added to the test procedures such as single line to ground fault (SLGF) test with different interconnection transformers or line to line fault test. The data collected could be also used to attempt a black box modeling of single-phase inverters, which will be useful for distribution planning and protection engineers given that transients models of inverters are scarce and sometimes lack portability among computer programs.

APPENDIX A

TEST LOG SHEET OF INVERTER A

Table 4. Inverter A - test log sheet

Model:	INVERTER A						**Output [W]**		2000		**DC Input [V]:**			500		
Event:	**Open Circuit**								**Short Circuit**							
Load [%]:	**25**		**50**		**75**		**100**		**25**		**50**		**75**		**100**	
Shot:	**File # / Abs. Inst. Peak**								**File # / Abs. Inst. Peak**							
1	Event 24/56	200.3	Event 6_1/50	226.8	Event 15/53	264.7	Event 45/59	226.7	Event 3/77	84.16	Event 50/92	87.75	Event 111/107	89.26	Event 2/62	285.4
2	Event 30/57	263.7	Event 14_1/51	251	Event 18/54	219.7	Event 51/60	227.7	Event 6/78	84.85	Event 54/93	87.95	Event 114/108	88.71	Event 12/63	218.4
3	Event 39/58	223.6	Event 12/52	376.2	Event 21/55	215	Event 54/61	243.3	Event 9/79	85.06	Event 58/94	87.68	Event 117/109	90.09	Event 18/64	201.1
4									Event 12/80	84.78	Event 63/95	87.88	Event 120/110	89.4	Event 22/65	173.3
5									Event 15/81	84.37	Event 67/96	87.81	Event 123/111	89.54	Event 26/66	178.4
6									Event 18/82	84.92	Event 71/97	87.88	Event 126/112	89.4	Event 28/67	175.2
7									Event 22/83	84.3	Event 75/98	88.02	Event 129/113	89.54	Event 30/68	175.6
8									Event 26/84	84.44	Event 79/99	87.95	Event 132/114	88.92	Event 32/69	174.3
9									Event 29/85	84.99	Event 84/100	87.33	Event 135/115	89.19	Event 34/70	174.1
10									Event 32/86	84.71	Event 88/101	87.75	Event 138/116	89.33	Event 36/71	174.3
11									Event 35/87	85.06	Event 92/102	88.09	Event 144/117	89.47	Event 38/72	221.3
12									Event 38/88	85.06	Event 96/103	87.61	Event 2/119	189.7	Event 40/73	174.3
13									Event 41/89	85.47	Event 100/104	87.54	Event 4/120	221.1	Event 42/74	274.8
14									Event 44/90	84.02	Event 104/105	87.81	Event 6/121	173.6	Event 44/75	173.2
15									Event 47/91	84.85	Event 107/106	87.68	Event 8/122	174.4	Event 46/76	287.4
Date:	5/18/15		5/18/15		5/18/15		5/18/15		5/19/15		5/19/15		5/19/15		5/18/15	

APPENDIX B

TEST LOG SHEET OF INVERTER B

Table 5. Inverter B - test log sheet

Model:	INVERTER B						Output [W]		3000		DC Input [V]:			240-300		
Event:	Open Circuit								Short Circuit							
Load [%]:	25		50		75		100		25		50		75		100	
Shot:	Dranetz Date Stamp / CSV File								File # / R							
1	11:18/20		10:52:58/17		12:12/14		12:05/11		11:21/26	R2	11:58/41	R1||R2	12:34/56	R1||R2	13:15/71	R1||R2
2	11:43/21		11:04/18		12:23/15		12:09/12		11:24/27	R2	12:00/42	R1||R2	12:40/57	R1||R2	13:16/72	R1||R2
3	11:55/22		11:05/19		12:27/16		12:10/13		11:26:58/28	R2	12:11/46	R1||R2	12:53/58	R1||R2	13:17/73	R1||R2
4									11:28/29	R2	12:05/43	R1||R2	12:56/59	R1||R2	13:18/74	R1||R2
5									11:29/30	R2	12:06/44	R1||R2	12:57/60	R1||R2	13:30/75	R1||R2
6									11:30/31	R2	12:07/45	R1||R2	12:59/61	R1||R2	13:42/76	R1||R2
7									11:31/32	R2	12:13/47	R1||R2	13:00/62	R1||R2	10:52/77	R1||R2
8									11:32/33	R2	12:14/48	R1||R2	13:02/63	R1||R2	10:55/78	R1||R2
9									11:34/34	R2	12:15/49	R1||R2	13:03/64	R1||R2	10:58/79	R1||R2
10									11:35/35	R2	12:18/50	R1||R2	13:04/65	R1||R2	11:00/80	R1||R2
11									11:36/36	R2	12:19/51	R1||R2	13:05/66	R1||R2	11:01/81	R1||R2
12									11:37/37	R2	12:20/52	R1||R2	13:06/67	R1||R2	11:02/82	R1||R2
13									11:38/38	R2	12:21/53	R1||R2	13:08/68	R1||R2	11:03/83	R1||R2
14									11:41/39	R2	12:23/54	R1||R2	13:09/69	R1||R2	11:04/84	R1||R2
15									11:44/40	R2	12:25/55	R1||R2	13:11/70	R1||R2	11:06/85	R1||R2
Date:	6/8/15		6/8/15		6/3/15		6/3/15		6/10/15		6/10/15		6/10/15		6/11/15	

APPENDIX C

TEST LOG SHEET OF INVERTER C

Table 6. Inverter C - test log sheet

Model:	INVERTER C						Output [W]		2650		DC Input [V]:			360		
Event:	Open Circuit								Short Circuit							
Load [%]:	25		50		75		100		25		50		75		100	
Shot:	File # / Abs. Inst. Peak								File # / Abs. Inst. Peak							
1	Event 2/123	436.2	Event 9/126	319.7	Event 20/129	325.5	Event 27/132	330.9	Event 2/NA	174.6	Event 36/164	251.9	Event 65/149	248.8	Event 35/135	292.7
2	Event 5/124	309.6	Event 11/127	325.4	Event 22/130	328.4	Event 29/133	325	Event 2/NA	173.2	Event 38/165	222.4	Event 2/150	202.2	Event 37/.csv	284.4
3	Event 7/125	320.0	Event 16/128	333.5	Event 25/131	324	Event 33/134	331.6	Event 4/NA	173.9	Event 40/166	174.3	Event 4/151	236.5	Event 39/136	281.8
4									Event 6/NA	174.1	Event 42/167	175.4	Event 6/152	228.4	Event 41/137	175.1
5									Event 8/NA	174.4	Event 44/168	174.8	Event 8/153	175.1	Event 43/138	175.1
6									Event 10/10	173.1	Event 56/169	237.2	Event 10/154	175.4	Event 45/139	286.9
7									Event 12/NA	175.9	Event 4/1	225.5	Event 12/155	176	Event 47/140	229.5
8									Event 14/NA	170.3	Event 8/2	232.9	Event 14/156	245.2	Event 49/141	174.3
9									Event 16/NA	170	Event 10/3	237.8	Event 16/157	175.9	Event 51/142	174.9
10									Event 18/NA	174.1	Event 12/4	242.8	Event 18/158	241	Event 53/143	174.6
11									Event 20/NA	172.8	Event 14/5	228.6	Event 22/159	174.5	Event 55/144	175.1
12									Event 22NA	172.5	Event 16/6	232.5	Event 24/160	231.8	Event 57/145	249.4
13									Event 24/NA	174	Event 18/7	229.7	Event 28/161	215.3	Event 59/146	256.5
14									Event 26/NA	173.4	Event 22/8	232.8	Event 30/162	175.7	Event 61/147	276.6
15									Event 28/NA	174	Event 24/9	243.9	Event 30/163	175.6	Event 63/148	202.3
Date:	5/21/15		5/21/15		5/21/15		5/21/15		5/28/15		5/27/15		5/26/15		5/21/15	

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APPENDIX D

TEST LOG SHEET OF INVERTER D

Table 7. Inverter D - test log sheet

Model:	INVERTER D						Output [W]		2000		DC Input [V]:			500		
Event:	Open Circuit								Short Circuit							
Load [%]:	25		50		75		100		25		50		75		100	
Shot:	File # / Abs. Inst. Peak								File # / Abs. Inst. Peak							
1	Event 4	202.0	Event 11	231.7	Event 17	196.3	Event 23	252.5	43	7.163	6	21.36	47	5.536	80	22.37
2	Event 5	206.0	Event 13	232.2	Event 19	242.5	Event 27	182.9	45	9.718	8	9.152	50	17.89	86	7.381
3	Event 9	228.6	Event 15	216.5	Event 21	251.9	Event 29	251.7	*52	6.226	10	15.93	52	3.747	99	23.91
4									54	6.118	13	27.9	56	11.21	4	4.66
5									*56	5.834	15	8.04	58	7.903	6	7.648
6									*59	11.25	18	17.52	60	7.176	8	11.97
7									62	3.97	20	20.11	62	1.64	10	3.563
8									64	3.563	22	9.227	66	7.325	15	4.511
9									66	2.46	24	11.47	70	3.656	17	4.231
10									70	13.43	26	14.89	72	1.678	23	4.66
11									75	4.008	28	13.78	76	10.68	31	5.092
12									77	4.738	31	10.72	80	18.54	34	12.33
13									79	4.141	33	17.35	84	9.898	38	8.071
14									82	6.174	35	1.957	85	20.54	42	22.85
15									84	7.158	41	2.274	92	9.14	44	4.884
Date:	4/16/15		4/16/15		4/16/15		4/16/15		5/1/15		5/1/15		4/28/15		4/28/15	
5/4/15	Event 13/39	281.8	Event 9/37	227.2	Event 5/35	245.8	Event 1/33	254.1	Event 14	60.02	Event 10	51.45	Event 5	37.02	Event 1/42	57.82
5/4/15	Event 15/40	198.9	Event 11/38	230	Event 7/36	236.8	Event 3/34	253.5	Event 19	9.525	Event 12	23.69	Event 8	85.54	Event 3/43	64.4

BIBLIOGRAPHY

[1] EPRI Survey on Distribution Protection: Emphasis on Distributed Generation Integration Practices. EPRI, Palo Alto, CA: 2013. 30002001277

[2] Hoke, Andy, et al. Inverter Ground Fault Overvoltage Testing. No. NREL/TP-5D00-64173. National Renewable Energy Laboratory (NREL), Golden, CO (United States), 2015.

[3] Nelson, A., et al. Inverter Load Rejection Over-Voltage Testing: SolarCity CRADA Task 1a Final Report. No. NREL/TP-5D00-63510. National Renewable Energy Laboratory (NREL), Golden, CO., 2015.

[4] Bravo, Yinger, Robles and Tamae, "Solar PV Inverter Testing for Model Validation," IEEE PES General Meeting, Detroit, MI July 5, 2011

[5] Yinger, Bravo, and Salas, "IEEE 1547 Standard and Utility Needs A Utility Perspective," UWIG Distributed Generation Users Group, April 24, 2012

[6] Bravo, R.J.; Chuong Ly, "Electronic-Coupled Generators Short Circuit Impacts," in Green Technologies Conference (GreenTech), 2015 Seventh Annual IEEE, vol., no., pp.158-161, 15-17 April 2015

[7] Keller, J.; Kroposki, B.; Bravo, R.; Robles, S., "Fault current contribution from single-phase PV inverters," in Photovoltaic Specialists Conference (PVSC), 2011 37th IEEE, vol., no., pp.001822-001826, 19-24 June 2011

[8] McDermott T. E., Student Guide to Safety in the Electric Power Systems Lab (EPSL), August 24, 2015

[9] ETS600X Photovoltaic Simulator, Operation and Maintenance Manual. Available: http://www.programmablepower.com/custom-powersupply/ETS/downloads/ETS600X_Operation-Maintenance_Manual_M551066-01_RevC.pdf. [Accessed: Nov-27-2015].

[10] ETS600X Photovoltaic Simulator. Available: http://www.ametek.com/pressreleases/news/2015/august/programmable-power-photovoltaic-simulator-provides-higher-output-and-power. [Accessed: Nov-27-2015]

[11] Fink, Matt, and Eric Hoover. "Eaton Voltage Sag Generator Final Report." 2013.

[12] PX5 User's guide. Available: http://dranetz.com/wp-content/uploads/2014/02/PX5-UsersGuide-RevJ.pdf. [Accessed: Nov-27-2015]

[13] Specifications of the Rigol DS1074Z 70 Mhz.

Available: http://www.rigolna.com/products/digital-oscilloscopes/ds1000Z/ds1074z/. Accessed: Nov-27-2015

[14] Variable autotransformer. Available: http://orgchem.colorado.edu/Technique/Equipment/Communityequip/Variac.html. Accessed: [Nov-20-2015]

[15] http://www.nmr.mgh.harvard.edu/~reese/VariacPage/. Accessed: [Nov-20-2015]

[16] Wikipedia, Solar inverter. Available: https://en.wikipedia.org/wiki/Solar_inverter. Accessed: [Nov-21-2015]

[17] PV inverter. Available: http://www.mitsubishielectric.com/company/environment/policy/product/appliances/pv_inverter/index.html. Accessed: [Nov-21-2015]

[18] Switch. Available: http://www.aliexpress.com/store/product/Ui-600V-Ith-32A-ON-OFF-Position-3-Phase-Rotary-Cam-Changeover-Switch/817555_2028861406.html. Accessed: [Nov-24-2015]

[19] Wieserman, L.; McDermott, T.E., "Fault current and overvoltage calculations for inverter-based generation using symmetrical components," in Energy Conversion Congress and Exposition (ECCE), 2014 IEEE, vol., no., pp.2619-2624, 14-18 Sept. 2014