ELECTROLYTE GATING OF TIPS-PENTACENE AND GRAPHEHE FIELD EFFECT TRANSISTORS

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Ziwei Guo, M.S.

University of Pittsburgh, 2017

Electrolyte gating is widely used to explore transport in new materials for field effect transistors (FETs). An electric double layer (EDL) is formed within a few nanometers of the semiconductor surface leading to a huge accumulation of carriers in the channel (e.g., 10^{13} – 10^{14} cm^{-2} for electrons and holes). The improved gate control means that a lower operating voltage is required to achieve a particular drain current. In this thesis, we use electrolyte gating to explore the electrical performance of both an organic semiconductor, TIPS-pentacene, and a two dimensional (2D) semi-metal, graphene. To study whether or not the valency of the ions affects the sheet carrier density, Hall measurements were made on epitaxial graphene gated with a new solid polymer electrolyte, polyethylene oxide (PEO)/$Mg(ClO_4)_2$ in which Mg^{2+} can induce two electrons while the commonly used Li^+ salt can only induce one. A side gate is used to drift ions into place and the temperature is lowered below the glass transition temperature of the polymer electrolyte to lock the ions into place. The highest sheet carrier densities are $7.9 \pm 5.1 \times 10^{13}$ cm^{-2} for holes and $3.4 \pm 1.3 \times 10^{13}$ cm^{-2} for electrons, which is an order of magnitude higher than that without electrolyte gating, and the values are comparable with those from Hall measurements on the same epitaxial graphene gated with PEO/$LiClO_4$ by our group. These results indicate that the valency of ions will not have large impact on sheet carrier density. Additionally, a maximum hall

mobility of 9.8 ± 4.5 × 10^4 $cm^2V^{-1}s^{-1}$ was achieved. For TIPS-pentacene FETs, an ionic liquid. DEME-TFSI, was employed as the electrolyte gate. However, in this case, it was not possible to achieve strong gate control, and possible reasons for this observation are studied. One reason is that the large ionic mobility of DEME-TFSI leads to a large leakage current to the top gate. Also, the large device dimensions (*i.e.*, channel wide of 960 μm and channel length of 50 μm), and a possible reaction between DEME-TFSI and TIPS-pentacene could contribute to the ineffective electrolyte gating. What is needed is a gate dielectric for which the leakage current to the top gate is at least 100 times smaller than I_{DS}, chemical compatibility with TIPS-pentacene, and smaller gate and channel dimension.

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PREFACE

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1.0 INTRODUCTION

1.1 MOTIVATION

Metal-oxide-semiconductor field-effect transistors (MOSFET), or insulated-gate field-effect transistors (IGFET) are arguably the most important component of the integrated circuit that drives the $ 330 billion electronics industry.[1] The size of the transistor has been scaled for the past six decades to address the need for device minimization (e.g., portable devices), faster computing speeds and lower power consumption.[2] A good example is the microprocessor, which is driven by billions of MOSFETs on a single chip[1] and according to Moore`s law, the density of the devices will double every two years.[2] This aggressive scaling has improved the performance of microprocessors, including processing speed: 740 kHz for the first Intel microprocessor to 3 GHz for modern processors.[3]

An MOSFET is used to amplify or switch an electronic signal by controlling current using an electric field. A schematic of a MOSFET is shown in Figure 1a. Generally, a MOSFET is comprised of three terminals (source, drain and gate), an insulating layer, and a semiconducting channel. Channel length (L) is the distance between source and drain (i.e., the path of the current), and W indicates the channel width (Figure 1b). When there is a difference in electric potential between source and drain, charge is injected at the source electrode, passes through the semiconducting channel and out the drain electrode. The insulating layer serves to separate the gate electrode from semiconducting channel and enables field-effect control over the number of

charge carriers in the channel. The gate metal completely covers the channel region, and by applying voltage on the gate, carriers near the interface inside of the semiconducting material can be induced to form a more conductive path for current to flow. Essentially, the gate metal in combination with the insulating layers and the semiconductor forms a capacitor.[4] When a positive bias is applied to the top gate, negative charge will be induced inside the semiconducting channel, just like any normal capacitor, and these induced carriers will form an electron rich region. On the contrary, if we apply negative bias on top gate, it will form a hole rich region in the channel material. As a result, current can flow from drain to source through this induced channel while electrons are driven to flow from source to drain in the channel. By varying the strength of bias on the gate electrode, we can effectively adjust the electrical field so as to modulate the drain-source current. The transistor can be considered as a switch, or a current amplifier, where the gate electrode turns the switch on and off for binary logic.

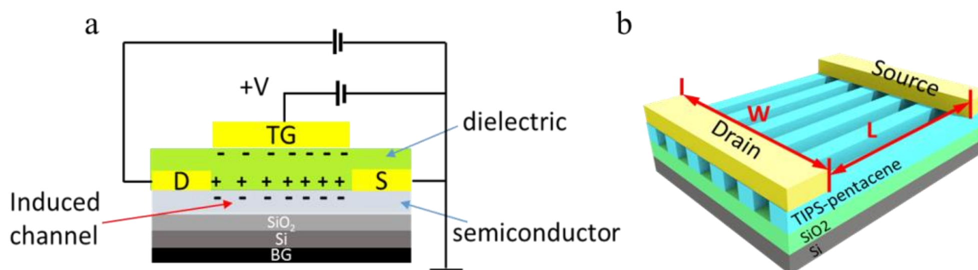

Figure 1: a) Top-gated MOSFET with a positive bias on top gate (TG) and on drain electrode (D) and the source electrode (S) is grounded. This positive gate voltage will induce negative charges in the semiconductor to form a conductive channel; b) back-gated TIPS-pentacene[1] organic field-effect transistor (OFET) where W indicates channel width, L indicated channel length and TIPS-pentacene is the active material.

[1] 6,13-bis(triisopropylsilylethynyl)pentacene

MOSFETs meet the needs for high performance computational devices (e.g., computers, servers) because of the high drive current.[1] The emphasis on MOSFETs now focuses on scaling to pack more transistors on a single chip to gain high-performance and to reduce the cost, we are at a physical limit for further shrinking the size of MOSFETs. In 2014, 5 billion MOSFETs and 20 nm gate length on a processor has been achieved for commercial market production.[5] However, more and more difficulties and challenges are met when further scaling the size of MOSFET. For example, one problem for channel lengths smaller than 5 nm is source-drain tunneling, where electrons directly pass through that the channel barrier and can no longer be controlled.[5] One approach to address this scaling problem and to increase carrier mobility is to introduce two-dimensional (2D) materials into the structure of MOSFETs and these materials will be discussed in section 1.2.

While MOSFETs provide a solution for high performance computing needs, this also makes MOSFET expensive, however, such high performance is not required for all applications. The need for lower cost transistors has been addressed through the development of thin-film transistors (TFT), using inexpensive materials such as amorphous silicon (a-Si), organic semiconductors such as pentacene for applications like biological sensors, optical detectors[1] and light emission devices. For TFTs, the number of transistors that can be packed in a certain area is not as important, but the challenge is to prepare large area TFTs with flexibility and stability at the same time with relatively lower cost for application like displays[1]. TFTs will be introduced in section 1.3.

1.2 REVIEW OF TWO DIMENSIONAL (2D) MATERIALS

Ranging from a single monolayer to multiple layers of atoms, from semiconductors to superconductors, and from flexible materials (i.e., few layer) to inflexible (i.e., many layers), 2D materials, have attracted world-wide attention in electronics since 2009.[6] Their superior and tunable properties, like high carrier transport[5], efficient photon harvesting[6], light-weight and excellent thermal conductivity, make them a possible candidate for the next generation applications in electronics and optoelectronics.[6]

A crystalline material which has at least one dimension smaller than 100 nm is classified as a nanomaterial,[5] and layered nanomaterials with one dimension restricted to a single layer are called 2D materials.[5] One type of 2D material that has been extensively studied is X-enes (*X*= *C, Si, Ge, P*), which are a group of layered materials consisting of a single element organized in a hexagonal lattice, like graphene.[5] Additionally, the most recently investigated transition metal dichalcogenides (TMDs) have attracted attention due to the finite band gap, which is an intrinsic character for a semiconductor and this makes them a potential candidate for application in FETs.[5] TMDs have the formula MX_2, which includes a transitional metal, *M* from group 4, 5 and 6 in the periodic table, and an element, *X* (where *X = S, Se or Te*).[5] These elements combine to form a 2D layered structure. So far, 40 TMDs have been confirmed[5]. One of the most popular is MoS_2, structure shown in Figure 2a.[7]

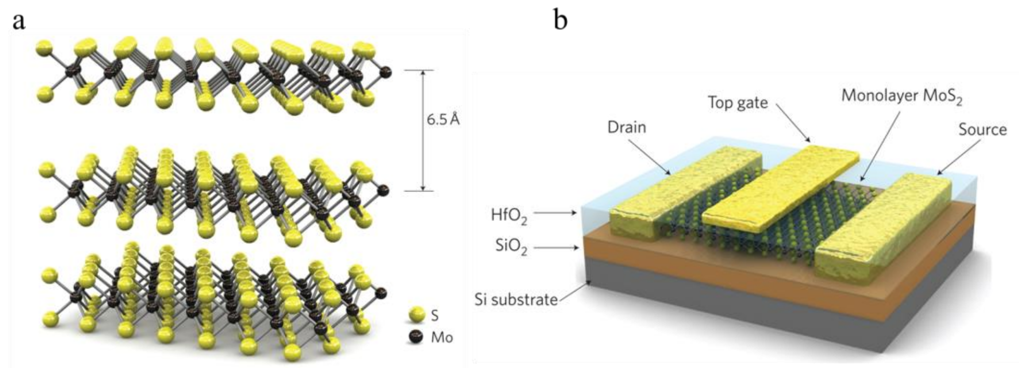

Figure 2:[7] a) *MoS_2* structure where yellow balls are sulfur atom and black balls are *Mo* atoms. In this figure, the distance between two layers of *MoS_2* is 6.5 angstroms; b) top-gated monolayer *MoS_2* FET with *HfO_2* as gate dielectric. Schematics from reference 7.

In these few-atom-thick layered materials, strong in-plane covalent bonding or strong ionic interactions render them a perfectly flat 2D plane while the weak Van der Waal out-of-plane interactions hold these planes together along the third axis to form layered structure.[5] This unique structure not only makes them easy to exfoliate (because of the weak Van der Waals bonding between layers) but also contributes to the special electrical properties, including charge carriers that can freely migrate and are confined within the plane. The feature of this fast charge transport could possibly be used in the application of logic FETs, which require quick reaction to the variation of input signals and large on-state current.[8]

One early example of 2D materials used in FETs comes from Radisavljevic *et al*.[7] They fabricated top-gated single-layer *MoS_2* FETs employing a halfnium oxide dielectric, as shown in Figure 2b, and reported mobility of 200 $cm^2V^{-1}s^{-1}$ and an on/off ratio of 10^8 compared to previously reported mobilities on MoS_2 FETs between 0.5 to 3 $cm^2V^{-1}s^{-1}$ with a SiO_2 dielectric.[7]

Among the 2D materials, carbon nano-materials play an important role in nanotechnology. Since the successful isolation and characterization of graphene[9] (structure shown in Figure 3), it has been studied extensively due to its high switching speed and high carrier velocity, as high as

1000 m/s for electrons in this large conjugation system[10], and these remarkable properties make it attractive for applications like energy storage and, if a bandgap can be created, also render it as a promising candidate for transistors. These properties are in addition to the obviously exciting physical properties of ultimate scaling (i.e., single atomic thickness) and ultra-light weight.

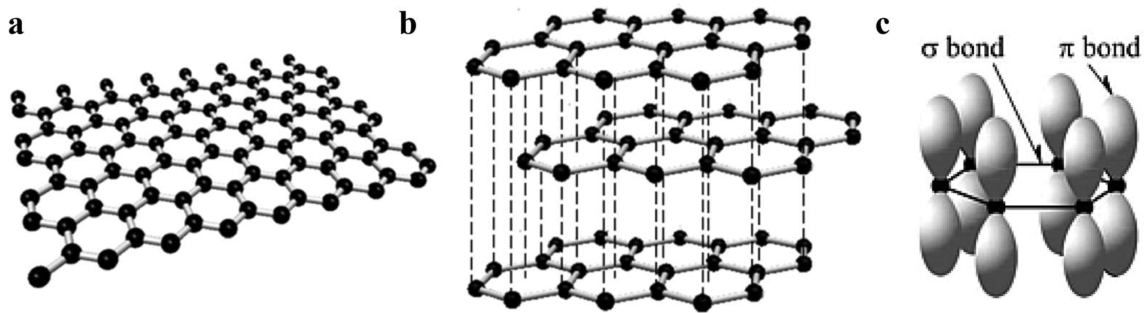

Figure 3:[11] a) Graphene monolayer where carbon atoms are shown in black; b) stacking of multiple layers of graphene; c) bonding in graphene where *p* orbitals are perpendicular to the plane of graphene to formπbonds.[11] Schematics from reference 11.

Graphene and other X-enes, like silicone, have zero band gap and they all show a double-cone shape band structure, referred to as Dirac cones, shown in Figure 4.[8] The zero band gap explains why carriers can move extremely fast along the 2D plane in graphene and also explains the ambipolar behavior (i.e., ability to conduct both electrons and holes).[10] As a result, due to the lack of band gap and cone-shape electrical bands, graphene is classified as a semimetal. What`s more, its superior mechanical properties and flexibility make it beneficial in the application in sensors.[10] However, a finite band gap is essential for many electrical applications, like transistors because they must be turned off and on (i.e., be able to switch from a non-conductive state to a conductive state). One way is to use multilayer graphene instead of monolayer graphene, and an example of band structure of bilayer graphene (BLG) is shown in Figure 4. Another way is to

make chemical modification of monolayer graphene, like hydrogenation, to fabricate FETs with an on/off characteristic, but this will either hamper the carrier mobility or increase the operating voltage.[8]

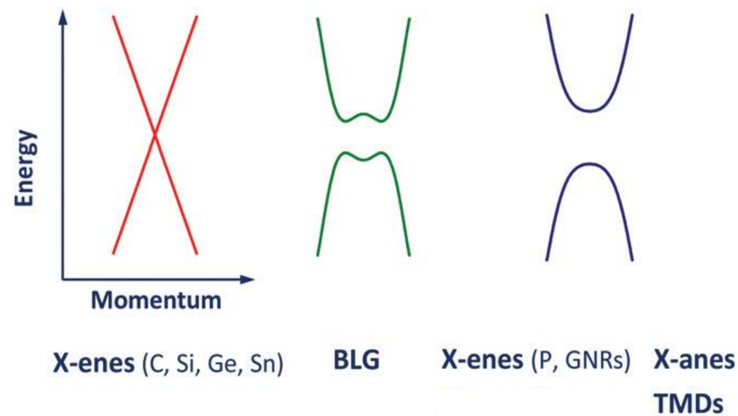

Figure 4:[8] Band structure of 2D materials relevant for transistors. BLG: bilayer graphene; TMD: transition metal dichalcogenide. The *y*-axis shows energy of the conduction and valence bands and *x*-axis is momentum. From the figure, we can tell that for graphene, the band gap is zero because the two bands merged into a point which makes it a semimetal because for metals two bands should overlapping and for semiconductors there should be a finite band gap. However, for TMDs and BLG, the band structure of separate parabolic curves indicates a finite band gap. Schematics from reference 8.

1.3 REVIEW OF ORGANIC SEMICONDUCTORS

While 2D materials (i.e., inorganic semiconductors) are being explored for high-performance devices, organic semiconductors have attracted more attention for TFTs to meet the needs for inexpensive, flexible and large area devices. What`s more, due to their easy fabrication, compatibility with various substrates such as flexible plastics, organic materials are more and more used as active materials in the TFTs and are promising in many applications, like large area displays and sensors.[12] In this section, we will review organic semiconductors because in addition to 2D materials, they are also explored in this master`s thesis.

Organic semiconductors have π-conjugated structure for molecular packing and charge transport. In these π-conjugated materials, *p* orbitals are overlapped (conjugated) to form the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) with a band gap between them as shown in Figure 5a. As a result, in those materials, carriers not only travel within a single molecule but between molecules. As shown in Figure 5b, when the intermolecular interactions between molecules (Van der Waal interactions) are weak, the overall electronic properties just resemble a single molecule's electronic properties. However, when there are strong interactions between molecules, as shown in Figure 5c, the HOMO and LUMO of single molecules merge into conduction and valance bands, just like traditional inorganic semiconductors.[13]

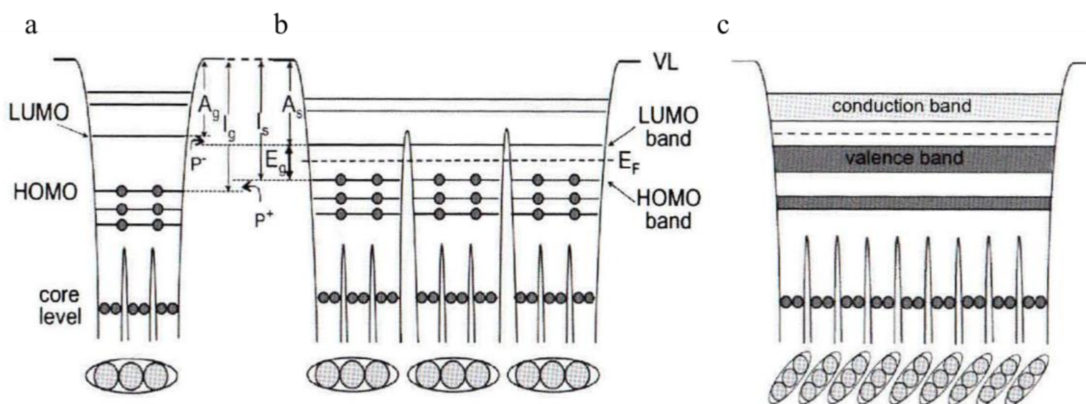

Figure 5:[13] a) HOMO and LUMO for single conjugated molecule; b) HOMO and LUMO bands of conjugated materials when the interaction between molecules are weak; c) Valance and Conduction bands of organic semiconductors when the interactions between molecules are strong. Schematics from reference 13.

For organic materials, both small molecules, like rubrene, and long chain polymers, like P3HT[2], can form semiconductors. Although polymeric semiconductors have the potential to be applied in the fabrication of large area displays, small molecule organic semiconductors have better crystallinity contributing to a larger carrier mobility exceeding 1.0 $cm^2V^{-1}s^{-1}$. A few examples of molecular and crystal structures of commonly used small molecule organic semiconductors are shown in Figure 6 in which TIPS-pentacene is the channel material studied in this thesis. One example of an OFET is reported by Ono *et al.*,[14] shown in Figure 7. The organic FET was fabricated with a special architecture that employed an ionic liquid (IL) under the semiconductor. The IL was drawn under the semiconductor by capillary force using EMIM-FSI[3] as gate dielectric and rubrene single crystal as active material. The mobility is as high as 9.5 $cm^2V^{-1}s^{-1}$, 0.3 V turn-on voltage and an on/off ratio of 10^4. Although these electrical parameters are not comparable to the FETs employing inorganic semiconductors, they can satisfy the needs in applications, like bio-sensors and displays. Because of the randomness of backbone chains, polymer-based transistors often show a smaller mobility, on the order of 10^{-5} – 10^{-1} and on/off ratio from 10^2 to 10^7.[12] Another advantage of small molecule organic semiconductors is that the molecules can be chemically tailored to have a wide variety of electrical, mechanical and thermal properties. A good example of this is pentacene and its derivatives.

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[2] Poly(3-hexylthiophene-2,5-diyl)

[3] 1-Ethyl-3-methylimidazolium bis(fluorosulfonyl)imide

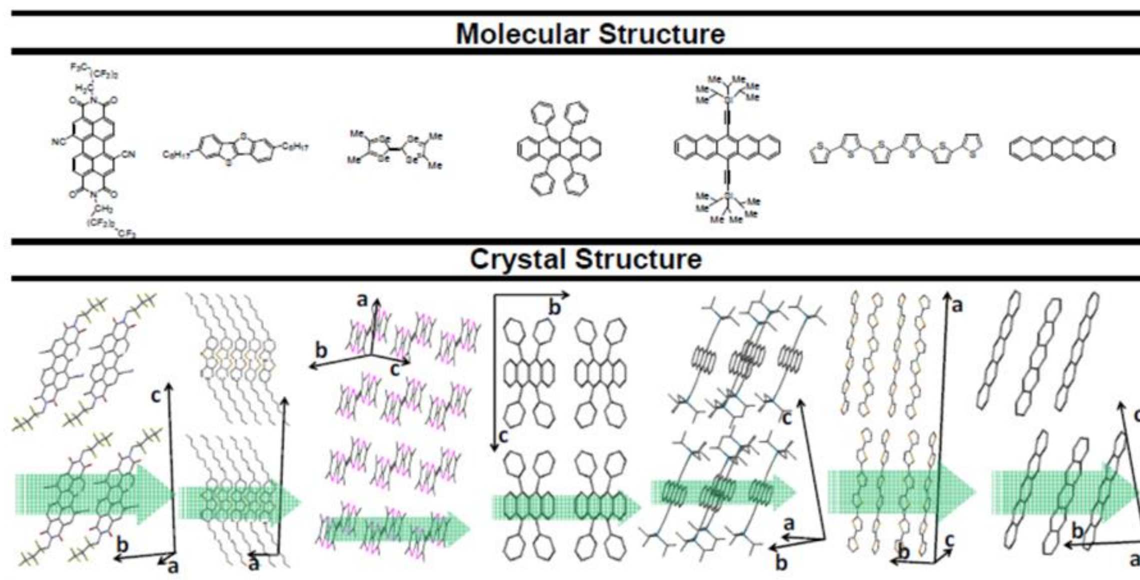

Figure 6:[15] Molecular and crystal structure of common used small molecule organic semiconductors. From left to right: PDIF-CN_2[4], C8-BTBT[5], TMTSF[6], rubrene, and TIPS-pentacene, sexithiophene, pentacene. Schematics from reference 15.

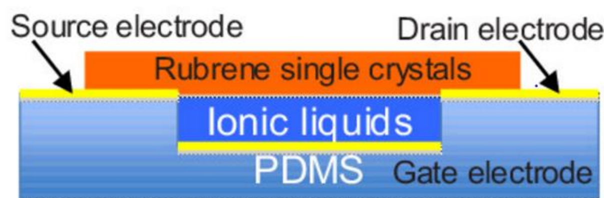

Figure 7:[14] Rubrene organic FET gated by IL. Schematic from reference 14.

As the most extensively studied small organic molecule semiconductor, pentacene and its derivatives, for example TIPS-pentacene, are often employed in OFETs due to their high carrier mobility.[16,17] Their fused rings make them suitable for stacking leading to a good molecular registration. Additionally, this ordered structure through π-π stacking between molecules

[4] N,N'-1H,1H-perfluorobutyl-dicyanoperylene di-imide

[5] 2,7-Dioctyl[1]benzothieno[3,2-b][1]benzothiophene

[6] tetramethyltetraselenafulvalene

improves the transport of carriers leading to an improvement of overall performance of OFET. Lin *et al.*, fabricated organic thin film transistor base on pentacene as the active material and mobility of 1.5 $cm^2V^{-1}s^{-1}$, on/off ratio as high as 10^8, and near 0 threshold voltage was achieved in their experiment.[17] Due to tendency of oxidation in ambient surroundings, low solubility and requirement of vacuum deposition of pentacene[18], multiple types of side chains have been added to this molecule to improve its properties while not compromising the crystallinity and electrical performance. TIPS-pentacene, with modification on pentacene at the 6 and the 3 positions by TIPS groups, is one of the best derivatives, and we are using this material as the channel material in this thesis. Due to its ordered, brick-wall stacking pattern, it shows hole mobility of 5.0 $cm^2V^{-1}s^{-1}$ and on/off ratio of 10^5 as reported by Li *et al.*,[16] and is soluble in almost all organic solvents making it easy to prepare and much more stable than pentacene.

1.4 REPLACING THE GATE DIELECTRIC WITH ELECTROLYTE

As discussed in the previous sections, inorganic materials, like SiO_2, are often employed in the structure of FETs as gate dielectrics. However, to deposit inorganic dielectric on the surface of organic material is challenging. Also, it is difficult to deposit high quality gate dielectrics on a 2D surface when they have no dangling bonds for the gate dielectric to stick to. Also, for both 2D materials and organic semiconductors, in order to prove whether or not these materials have the properties we need for FETs, especially the materials first employed in FETs, we need to explore their transport properties which require excellent gate control and the dielectric should be easy to deposit.

One solution to the problems above is to use electrolyte, like IL, which consists only anions and cations and solid polymer electrolyte (SPE), which is a salt dissolved in a polymer. They are ionically conductive but not electrically conductive and this property makes them able to form electrical double layers (EDL) at the electrolyte-semiconductor and electrolyte-gate interfaces when the ions respond to an electrical field as shown in Figure 8a. Due to the huge capacitance density formed by electrolyte-gating (~ 1 $\mu F/cm^2$)[19], large sheet carrier densities can be induced (~10^{13} to 10^{14} cm^{-2}) in electrolyte-gated FETs[6].

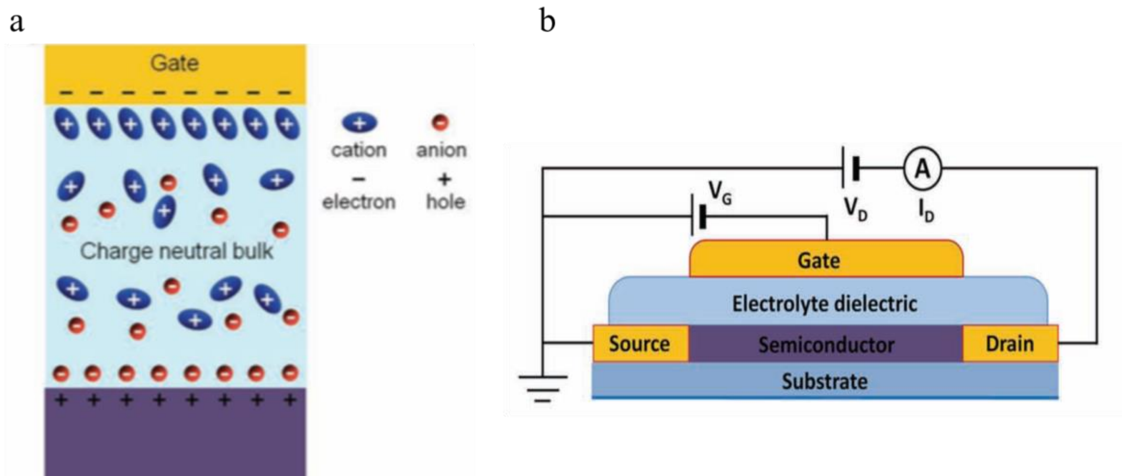

Figure 8:[19] a) EDLs form when a negative bias is applied on the gate and this will attract cations moving to the gate and form an ELD at gate-electrolyte interface to screen the electric field, at the same time, this will drive the opposite ions to the semiconductor to form another EDL, as a result, charges are induced in the channel; b) electrolyte gated transistor. Schematics from reference 19.

Figure 8b shows a typical architecture of an electrolyte gated transistor (EGT). The insulator between gate and semiconductor is an electrolyte consisting of mobile ions. By applying a voltage to the gate electrode, the cations or anions will be attracted and accumulate at the gate-electrolyte interface and, as a result, corresponding opposite ions will migrate and accumulate at

the electrolyte-semiconductor interface. As we can see in Figure 8a, the ions at gate-electrolyte interface will screen the gate charges while the ions at electrolyte-semiconductor interface will induce opposite-sign carriers to form a conducting channel. Consequently, EDL are formed at each interface, and this process results in doping the semiconductor channel *n*- or *p*-type (i.e., doping with electrons or holes, respectively).

Because the EDL is thin, about 1 nm, the potential through the dielectric under steady state conditions will hardly drop within the charge neutral bulk but only drops across the EDL. Additionally, due to the formation of the EDL, there is little driving force for bulk ions to move, leading to small ionic current between gate and drain. Compared to traditional transistors gated with an inorganic oxide that is several nanometers thick, EDLs achieve even smaller thicknesses and therefore better gate control. Essentially, the EDL brings the gate contact to within a nanometer of the semiconductor surface. Because capacitance density, *C*, is proportional to $\kappa\varepsilon_0/\lambda$, where k is the effective dielectric constant, ε_0 is the vacuum permittivity and λ is corresponding to the thickness of EDL, *C* can be ~ 1 μF/cm^2, which is at least one order of magnitude greater than the values for conventional dielectrics.[19] Because drain-source current is proportion to *C* and operating voltage is inversely proportional to *C*, it is possible for EGTs to operate at low voltage while delivering large current.

Some examples related to EGTs are provided here. Ono S. *et al.*, used two ionic liquids, EMIM-FSI and EMIM-TFSI[7], as the gate dielectrics and an organic material, rubrene, as the semiconductor to fabricate the first EDL-OFET in 2008.[20] They reported a mobility of 1.2 cm^{2}V^{-1}s^{-1} which is comparable with SiO_2 gated devices (~1.5 cm^{2}V^{-1}s^{-1}).[20] Electrolyte gating is also

[7] 1-Ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide

employed in inorganic 2D materials. Xu *et al.*, uses a polymer/salt, PEO/$CsClO_4$, as the electrolyte dielectric to electrostatically gate 2H-$MoTe_2$. They report a sheet carrier density of 1.6×10^{13} cm^2, which is an order higher than gated by regular dielectrics, and a EDL capacitance density of 4 μF/cm^2.[21]

1.5 INTRODUCTION OF ELECTROLYTE

1.5.1 Solid Polymer Electrolyte (SPE)

SPE is an electrolyte in which a salt is dissolved in a polymer. In the case of PEO, it is the lone pair electrons on the ether oxygen atom in the PEO backbone that solvates the cation, such as Li^+. The ionic conductivity ranges of a variety of electrolytes are showed in Figure 9. In this figure, we can see that the polymer electrolyte, PEO/$LiClO_4$, has a relatively low ionic conductivity. One reason for this low ionic conductivity is that the lone pair electrons on oxygen in the PEO chains can coordinate with Li^+ ions. While this interaction allows the cation to be soluble in the

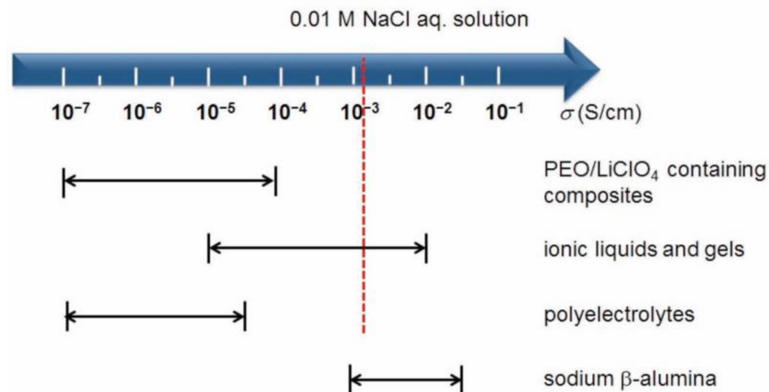

Figure 9:[19] Ionic conductivity σ for different types of electrolyte at room temperature. Schematics from reference 19.

PEO, it also decreases the mobility of the ions in the PEO. In addition, the ion mobility is limited by the polymer mobility, and at room temperature, polymer mobility is low for PEO. With this low ionic conductivity and the electrical non-conductivity of PEO, the leakage current from drain to gate electrode can be extremely small. Because the flexibility of the PEO chains depends strongly on temperature, the motion of ions is also a function of temperature.[19] These principles apply to other polymer/salt systems and are not limited to PEO electrolytes.

1.5.2 Ionic Liquids

Ionic liquids consist only of cations and anions – they are liquid salts and some examples are showed in Figure 10. Due to their large ionic conductivity and the ability to form EDLs, they are utilized in fast switching EGTs.[19] Additionally, they are non-volatile, non-flammable, non-corrosive and stable in large range of temperature. What`s more, the electrochemical window is large (>3V), which is larger than the electrochemical window of solid polymer electrolytes. Due to the weak electrostatic interactions between cations and anions, and the absence of a slow-moving polymer, the ionic conductivity is higher than the polymer/salt system and can therefore form an EDL faster.[19] However, because the IL is liquid-phase, this limits its application in solid state devices. One solution to give IL some mechanical integrity is to add gelators, like a polymer, to form 'ion gel'.[19]

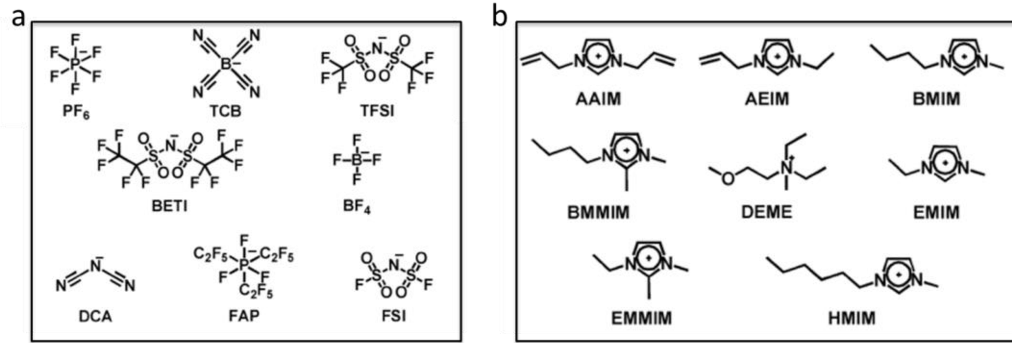

Figure 10:[22] Common anions, a), and cations, b), used in IL.[22] Schematics from reference 22

1.6 SUMMARY OF THE THESIS

In this MS thesis, we explored electrolyte gating of both inorganic, 2D FETs made of graphene and organic, 3D FETs made of organic semiconductor TIPS-pentacene. Generally, the objective that united my work on both of these devices was to study the effect of ions on both organic semiconductors and inorganic, 2D materials.

The goal of the work on the 2D devices is to use PEO/$Mg(ClO_4)_2$ electrolyte to side gate the graphene devices to determine whether the ion valence has an impact on the electrolyte gating. In our experiment, we use divalent ion, Mg^{2+} compared with widely used PEO/$LiClO_4$ with monovalent ion, Li^+. The motivation is that Mg^{2+} can induce two charges in the channel while Li^+ can only induce one. By applying a bias to the side gate, the EDL is formed on graphene channel. Then, we decrease the temperature to 220 K to lock the ions at graphene-electrolyte interface and then perform hall measurement to directly measure the sheet carrier density induced by the divalent ions. In the experiment, we obtained sheet carrier densities of $3.7 \pm 2.8 \times 10^{13}$ cm^{-2} for holes and $2.4 \pm 0.8 \times 10^{13}$ cm^{-2} for electrons at V_{SG} equal -2 V and +2 V respectively and both of them are an order of magnitude larger than that of the devices without

electrolyte. Additionally, our group member reported 5×10^{13} cm^{-2} for holes and 1×10^{13} cm^{-2} for electrons by top gating the same graphene field effect transistors (GFETs) by $PEO/LiClO_4$ with a monovalent ion, Li^+, at the same gate voltage. These results show that the sheet carrier density is comparable using monovalent or divalent cations which indicates valency will not be a factor to alter the sheet carrier density in electrolyte gating.

The goal of the work on the 3D organic semiconductors is to use an IL, DEME-TFSI, to top gate the device in order to find out whether or not an IL can be used to achieve better gate control of TIPS-pentacene device and exceed the performance that has already been published on this material using a traditional backgate. The motivation is that larger source-drain current might be achieved with a smaller source-drain voltage by using an IL, compared to the back-gated devices, because of the formation of the EDL yielding larger capacitance density. Unfortunately, due to the large dimension of the channel compared to the top gate, we are not able to effectively dope the channel using an IL. We also observe that the leakage current through the IL to the top gate is comparable to the current from drain to source. In addition, there is also evidence that the IL is reacting with the channel material, TIPS-pentacene.

2.0 EXPERIMENTAL TECHNIQUES

2.1 INSTRUMENTATION

An MBraun Double-Bay Glovebox, Figure 11, filled with argon is used to prepare and deposit the electrolytes, keeping the samples from exposure to oxygen and water. The water and oxygen concentrations are controlled to < 0.1 ppm. Preventing exposure to water and oxygen is important for several reasons. One reason is that TIPS-pentacene will be slowly oxidized.[23] Another important reason is that the performance of the electrolytes we employed in the experiments will be affected by exposure to ambient conditions. For the IL, due to its large polarity, it can easily absorb water from the air and this will lead to increase of leakage current due to the increase of the ionic conductivity. For the PEO/salt system, water will weaken the coordination between ions and PEO due to solvation of ions by water (the water essentially acts like a small molecule plasticizer); the water screens the EDL, making gate control less effective. Additionally, if water is present in the electrolyte, it can lead to hydrolysis during the voltage sweeping, yielding undesired redox reactions that contribute to the current.

Figure 11: MBraun Double-Bay Glovebox in our lab in 813, Benedum Hall

A Lake Shore CRX-VF Probe Station (Figure 12a) is used for electrical measurement in this experiment. The probe station operates under high vacuum, 10^{-6} torr, over a temperature range of 10 to 500 K. Additionally, the adjustable magnetic field, provided by 22.5 kOe vertical field superconducting magnet, can operate from +2.5 to -2.5 T. There are six probe arms and a microscope with for landing the probes on the device.

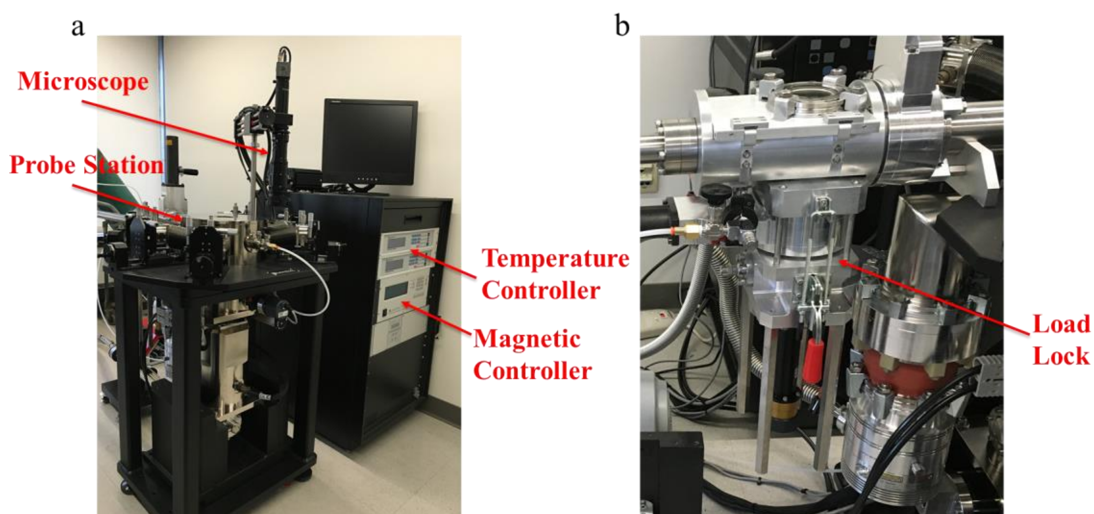

Figure 12: Probe Station in our lab in 813, Benedum Hall. a) Probe Station, microscope and thermal and magnetic controllers; b) load lock

One unique feature of our probe station is the custom load-lock shown in Figure 12b. This load lock is connected to a secondary pump so that this architechture is available for transfer samples directly from glovebox to the probe station sample stage or vice versa. In this case, the sample will not be exposed to air at all during the experiment.

A Keysight B1500A Semiconductor Parameter Analyzer (Figure 13), is used for electrical measurements. Current-voltage sweep measurements and capacitance-voltage measurement are both available, and in this thesis, we use it to current-voltage measurments. Keysight EasyExpert software is used for I/V sweep and I/V-t Sampling. Also, the temperature and magnetic fields can be controlled by this software.

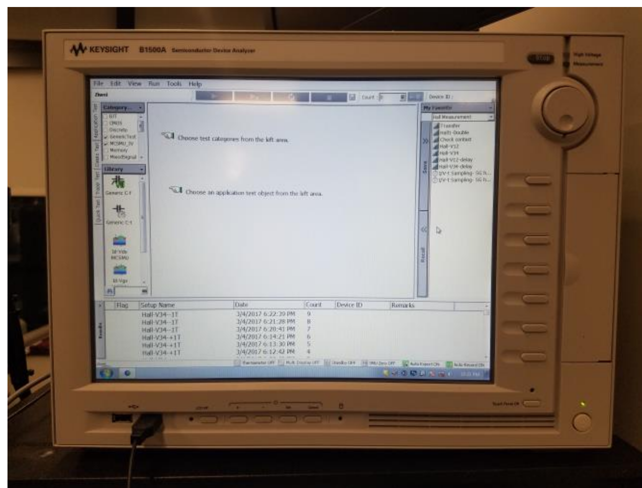

Figure 13: Keysight B1500A Semiconductor Device Analyzer

2.2 ELECTRICAL MEASUREMENTS

As presented above, FETs are three-terminal capacitor-like devices. In this work, the source electrode is always grounded and bias is applied to the drain electrode. The source and drain

electrodes work together to drive current through semiconductor channel to form a closed circuit. The third terminal, the gate electrode, turns the FET off and on by varying the magnitude of the applied gate voltage. The voltage difference between source and drain is denoted V_{DS} *(V)*, and the voltage difference between source and gate is denoted V_{GS} *(V)*.

Due to the capacitor-like configuration, the average potential in the channel caused by drain and source is $(V_D + V_S)/2$ equal to $V_D/2$, assuming the ideal situation. As a result, the overall potential applied on channel is $V_{eff} = (V_G - V_D/2)$, because V_G is applied on the opposite side of the dielectric. The charges per unit area, Q (C/m^2), in two capacitor plates is described by equation 2.1:

$$Q = C_i V_{eff} = C_i(V_G - \frac{V_D}{2}) \quad (2.1)$$

where C_i (F/m^2) is the capacitance per unit area of the dielectric. This equation can also be described in terms of the current density *(A/m)* given as $j = \sigma E$ where σ *(S)* is conductivity and E *(V/m)* is the electrical field strength. The conductivity is described as $\sigma = en\mu$ where e is the elementary charge (1.602×10^{-19} *C*), n (m^{-2}) is the charge carrier density and μ $(m^2V^{-1}s^{-1})$ is the mobility of carriers. E is equal to V_D/L. As a result, we can have:

$$j = en\mu E = Q\mu E = C_i(V_G - \frac{V_D}{2})\mu\frac{V_D}{L} \quad (2.2)$$

and because drain-source current is the multiplication of current density and channel width W *(m)*, this gives:

$$I_D = jW = \frac{W}{L}C_i\mu(V_G - \frac{V_D}{2})V_D \quad (2.3)$$

where L *(m)* is channel length. However, in the above case, we assume that threshold voltage V_T is zero, which is the minimum voltage needed for gate to form a conducting channel in semiconductor. With a non-zero V_T, we can have the following equation:

$$I_D = \frac{W}{L} C_i (V_G - V_T - \frac{V_D}{2}) V_D \quad (2.4)$$

Equation 2.4 describes the relationship between drain-source current and drain-source and gate voltage. We can use this equation to extract parameters from the data, like threshold voltage and carrier mobility.

2.2.1 Output and Transfer Characteristics

We can use three terminals to acquire output and transfer characteristics. The top row of Figure 14 shows a top-gated FET. In Figure 14a to 14f we can find two regimes: (1) the linear regime and (2) the saturation regime. The pinch-off point connects the two regimes.

In the linear regime, shown in Figure 14a and14b, V_{DS} is much smaller than V_{GS}, as a result, carrier density is mainly determined by gate voltage, and because V_G is set to be constant in this measurement, the carrier is generally distributed evenly in the channel as shown in Figure 14a. Consequently, the current through the channel is linearly increasing with the increase of V_{DS}, as shown in Figure 14b. Because $V_D \ll V_G$, equation 2.4 becomes:

$$\mathrm{I}_D^{lin} = \frac{W}{L} C_i \mu (V_G - V_T) V_D \quad (2.5)$$

Figure 14c and Figure 14d show the situation at pinch-off point where $V_D \approx V_G$-V_T. As a result, V_G is totally cancelled by V_D and the potential will decrease linearly from source to drain.

Further increase of V_D will push the pinch-off point toward source while the current will not increase, that is, I_D is independent of V_D and we call this regime the ‘saturation regime’. In this

regime, the potential difference between pinch-off point and source is a constant *($V_G - V_T$)*. Therefore, we can get the saturation current easily by replacing V_D with *($V_G - V_T$)* in equation 2.4:

$$I_D^{sat} = \frac{W}{2L} C_i (V_G - V_T)^2 \tag{2.5}$$

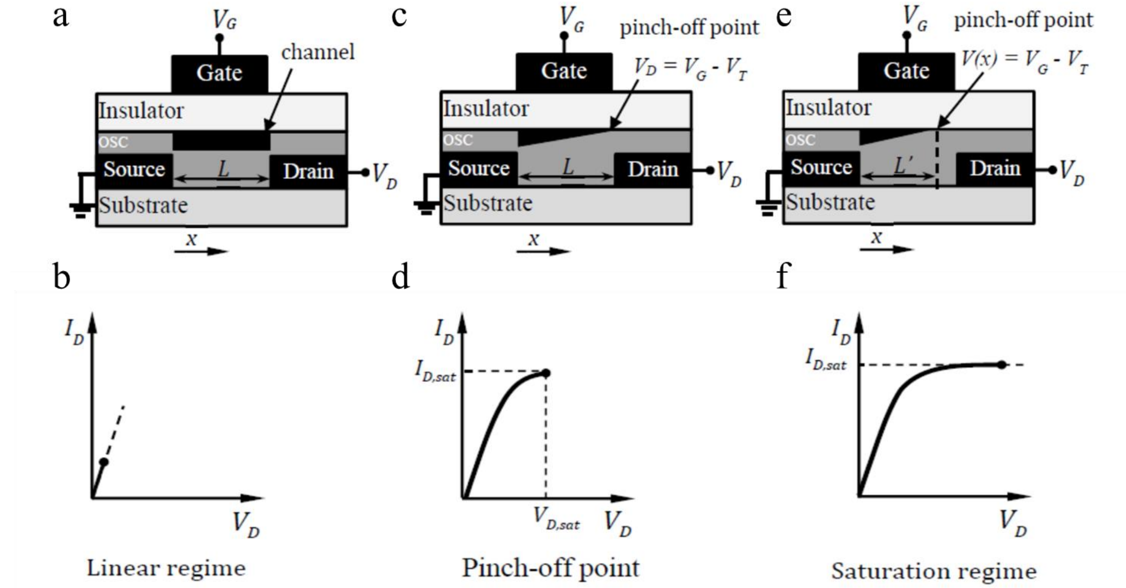

Figure 14:[24] Operation regime in output characteristics.[24] a), c) and e) show the carrier distribution in channel material at linear regime, pinch-point and saturation regime; b), d) and f) show the corresponding output characteristics. Schematics from reference 24.

Whereas the drain current is measured as a function of V_{DS} in output characteristics, the drain current is measured as a function of V_{GS} in transfer characteristics, as showed in Figure 15. One of the most useful features of transfer characteristics is that they show on and off current state of the device (i.e., maximum and minimum current). When V_G is much smaller than V_D, most of the electric field created by V_G will be canceled out by electric field created by V_D. Consequently, no effective conductive channel can be formed because charges are not induced in the channel material. Once V_G is larger than V_T, the electric field created by gate induces charge in channel,

creating a conductive path between drain and source and therefore increasing I_D. When the device is turned on, the ratio of the on-state current to the off-state current is called the on/off ratio which is an important parameter for device performance. It is desirable to have a transistor with a high on current and a low off current.

Figure 15 shows one example of transfer characteristics of TIPS-pentacene – one of the channel materials studied in this thesis. In this Figure, $|I_D|$ is plotted in log scale which is shown in black and $|I_D|^{1/2}$ is plotted in linear scale which is showed in blue. Threshold voltage is shown by the intercept of the tangent line of $|I_D|^{1/2}$ on V_G.

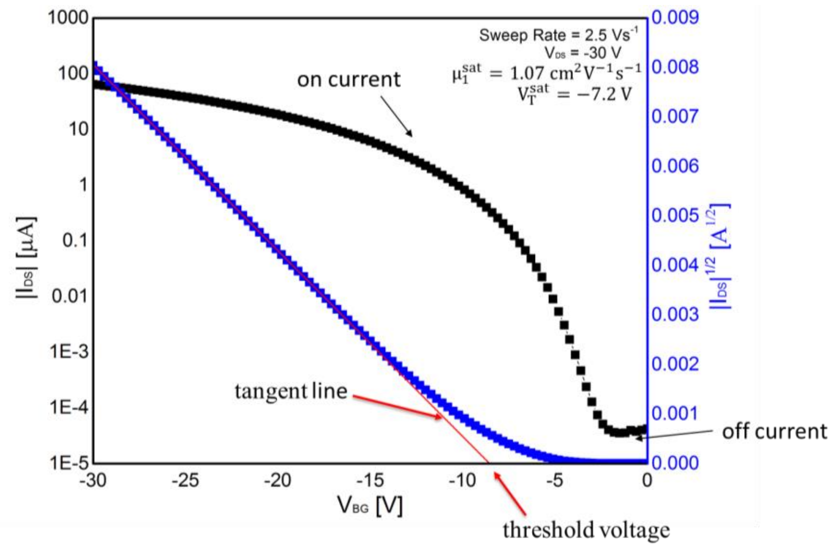

Figure 15. Transfer characteristics of TIPS-pentacene in this study. Black curve shows the absolute value of I_{DS}, blue curve shows the square root of the value on black curve and red line is the tangent line of the blue curve by linear regression.

2.2.2 Extracting the Threshold Voltage and Calculating the Field Effect Mobility

We can extract the threshold voltage in the transfer characteristic plot. As showed in Figure 15, first we have to plot $|I_D|^{1/2}$ vs. V_G. Then, a line tangent to the data is plotted in red and the intercept on V_G is the threshold voltage. Another important parameter that can be obtained in this

plot is the carrier mobility μ. The mobility can be extracted according to equation 2.5 by plotting $|I_D|^{1/2}$ to V_G. And the slope, $\sqrt{\frac{W}{2L}C_i}$, of tangent line of the data includes the mobility, where W, L and C_i are already known. Finally, we could calculate mobility using the slope.

2.2.3 Hall Measurement

The objective of hall measurement is to directly measure the sheet carrier density *(i.e.* the amount of major carriers per unit area). The measurement is usually performed according to Van der Pauw method[25] as shown in Figure 16. To understand this method, we have to introduce some basic concepts first. Assuming electrons are travelling along the electrical field, now we apply a magnetic field perpendicular to this electrical field. In this case, there will be a magnetic force perpendicular to the direction of both electrical and magnetic fields, which is referred to as Lorentz Force. The direction of this force is determined by right hand rule. Directed by this force, electrons will accumulate at one side of the material resulting in a potential drop, *i.e.* Hall voltage V_H, across the channel material, as shown in Figure 16. So, a Hall measurement is a measurement of the Hall voltages under a constant magnetic field. Using the dimension of the channel material, the Hall coefficient, sheet carrier density and Hall mobility of carriers can be calculated (details will be presented in section 2.2.5).

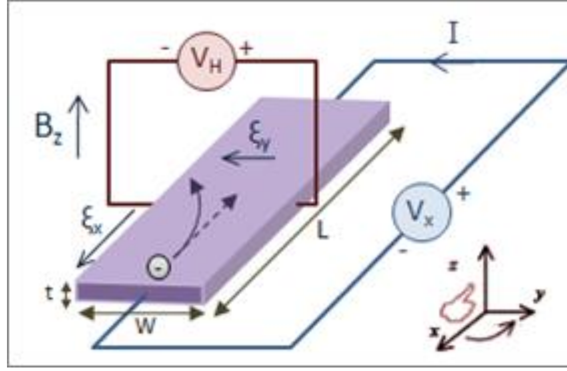

Figure 16:[25] Hall Measurement with Van der Pauw method where a current source is applied in x direction and a magnetic field is applied at a direction perpendicular to the material as shown in z direction. In this case, we will test the voltage difference caused by accumulation of carriers at one side at the y direction across the material. Schematic from reference 25.

To perform a Hall measurement, graphene is patterned into a Hall bar geometry as showed in Figure 17a and b. Source and drain are labeled S and D, and the other 4 contacts are labeled Hall 1, 2, 3, and 4. The pattern that is used forms two pairs of hall bars *(i.e.* Hall 1 and 2; Hall 3 and 4). The potential difference between Hall bar 1 and 2 is noted as Hall voltage V_{12} while the potential difference between Hall bar 3 and 4 is noted as Hall voltage V_{34}. Longitudinal voltage is the voltage difference between two Hall bars on the same side (i.e. V_{24} between Hall 2 and 4; V_{13} between Hall 1 and 3), which can be used for Hall mobility calculation. Six probes are used during the measurement. The source-drain current is swept while the probes on Hall bars are set to zero, thereby acting like voltmeters to detect the voltage at each Hall bar. When there is no magnetic field, most carriers will go from drain to source driven by the bias on the drain electrode in Figure 17a. We will use this zero magnetic field test as our baseline because there might be some carrier motion due to thermal energy. When we apply a magnetic field, the carrier will drift away from their path to the Hall bars on one side of the device due to the Lorentz force, as shown in Figure 17b. In this situation, we will measure voltages under this magnetic field *B*

for each Hall bars. With these voltages tested by each probe, we can extract sheet carrier density of the channel material and the Hall mobility of the carriers.

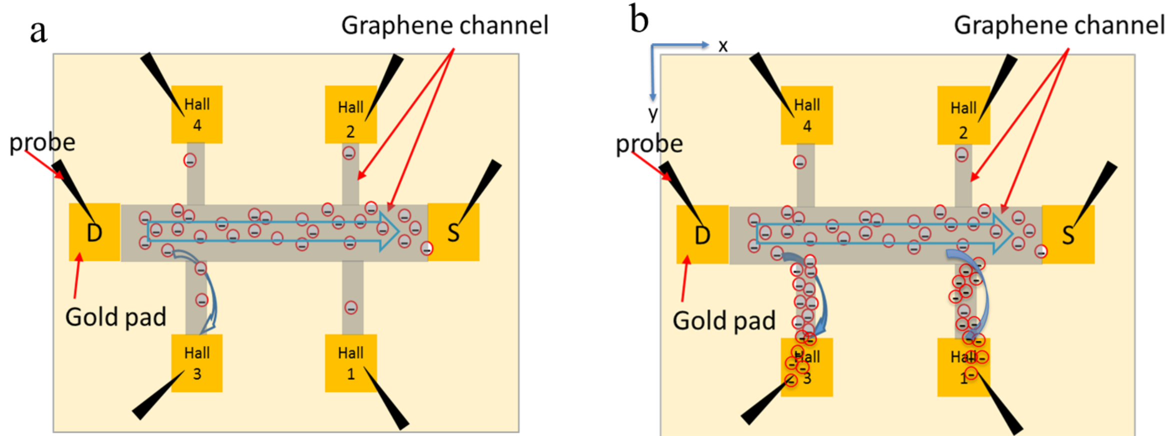

Figure 17: Hall effect measurement. a) when the magnetic field strength is set to zero, most electrons move directly from drain to source but there will still be some electrons go to Hall bars due to thermal agitation; b) When we apply a finite magnetic field, which is in the z-direction, electrons will stray to Hall bars due to Lorentz Force.

2.2.4 Sheet Carrier Density and Hall Mobility Extraction

The measured voltages at each Hall bar at the same current I_D, will be labeled as V_{10}, V_{20}, V_{30} and V_{40} at zero magnetic field (where the subscript '0' denotes zero magnetic field) and V_1, V_2, V_3 and V_4 at a magnetic field B. The voltage difference of each pair of Hall bars, (*i.e.* the Hall voltage) is V_{120}, V_{340}, V_{12} and V_{34} by the following subtraction

$$V_{120} = V_{10} - V_{20}$$

$$V_{340} = V_{30} - V_{40}$$

$$V_{12} = V_1 - V_2$$

$$V_{34} = V_3 - V_4$$

The real voltage difference between each pair of Hall bars, (*i.e*. Hall voltages), caused by magnetic field is $V_{12,eff} = V_{12} - V_{120}$ and $V_{34,eff} = V_{34} - V_{340}$. Then, with the Hall voltages, we can calculate Hall effect coefficient, R_H (m^2C^{-1}), by the following equations:

$$R_{H34} = V_{34,eff}/(I_D B)$$

$$R_{H12} = V_{12,eff}/(I_D B)$$

where R_{H34} is the Hall coefficient for the pair of Hall bars of Hall 3 and 4, and R_{H12} is the Hall coefficient for the pair of Hall bars of Hall 1 and 2. With R_H we can calculate sheet carrier density, n_s (m^{-2}):

$$n_{s34} = 1/(eR_{H34})$$

$$n_{s12} = 1/(eR_{H12})$$

Next we have to calculate longitudinal voltage, V_L, to calculate hall mobility.

$$V_{L31,eff} = V_{L31} - V_{L310}$$

$$V_{L42,eff} = V_{L42} - V_{L420}$$

where

$$V_{L31} = V_3 - V_1$$

$$V_{L310} = V_{30} - V_{10}$$

$$V_{L42} = V_4 - V_2$$

$$V_{L420} = V_{40} - V_{20}$$

The hall mobility μ_H is:

$$\mu_{H34} = R_{H34}(L/W)(I_D/V_{L31,eff})$$

$$\mu_{H12} = R_{H12}(L/W)(I_D/V_{L42,eff})$$

where W and L are the channel width and length respectively. Finally, we have to plot I_D and these calculated parameters, R_H, n_s and μ_H with respect to time, t (s), and an example is shown in

Figure 18. To extract the value of n_s and $\mu_{H,}$ which is indicated by the red line in Figure 18, the data are averaged over the range from 0 to 500 nA by eliminating the data points that are 100 times larger than the average value.

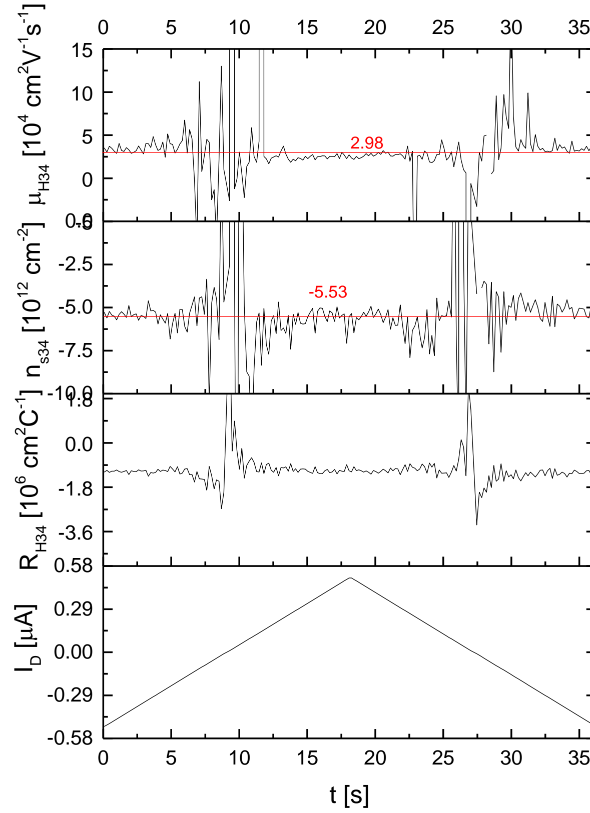

Figure 18: Example of Hall effect measurement for graphene in this study. By applying a ramped I_D, hall voltages are measured and R_H, n_s and μ_H are calculated as a function of time t.

3.0 EXPERIMENTAL DETAILS

3.1 DEVICE FABRICATION

3.1.1 Graphene Field Effect Transistor(GFET)

The graphene FETs were fabricated by Dr. Ke Xu, a Visiting Research Assistant Professor in our group and the fabrication details can be found in reference 26[26]. Generally, Hall bars were patterned on epitaxial graphene provided by Prof. Josh Robinson's group at Penn State by photolithography. Figure 19 shows the optical image of the graphene devices. Ti/Pd/Au (1/25/15 nm) drain, source electrodes and Hall bars are deposited on graphene channel material which is grown on SiC. The channel length is 160 μm and the channel width is 80 μm.

Then, PEO (molecular weight 94,600 g/mol, Polymer Standards Service) and $Mg(ClO_4)_2$ (anhydrous, Alfa Aesar) with a molar ratio of 20 PEO oxygen atoms to 1 Mg^{2+} was dissolved in acetonitrile solvent to form a 1 wt% solution and then the solution was drop-cast onto the device in the glovebox. The device was kept in the glovebox while the solvent, acetonitrile, evaporated, leaving an electrolyte film of approximately 1 μm thickness. After that, the sample was annealed on a hot plate at 80 °C for 5 minutes to drive off any residual solvent, and then it was transferred to the probe station via the load lock for electrical measurements.

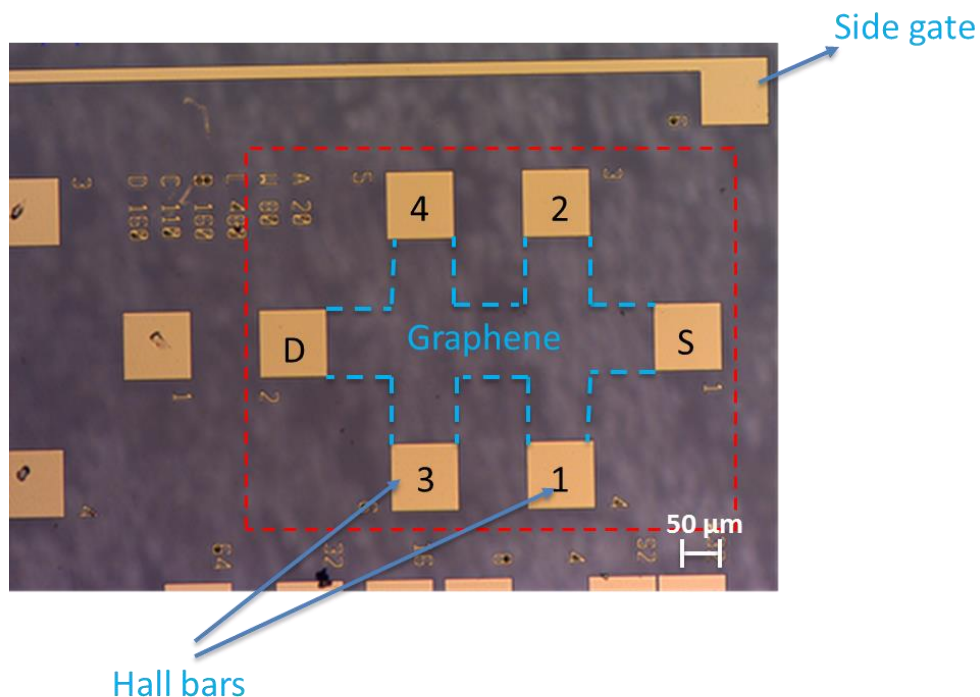

Figure 19: Optical image of GFET. There are six pads for hall measurement. Pad 1 and 2 act as drain and source and the other four pads act as Hall bars. Also, a long side gate was used in the experiment for the ions to form EDL at interface between graphene and electrolyte.

3.1.2 TIPS-pentacene Field Effect Transistor

The TIPS-pentacene devices and films are provided by our collaborators in Professor Hanying Li's group in Zhejiang University in China. The fabrication details of TIPS-pentacene FET can be found in Hanying Li's paper[16]. Briefly, TIPS-pentacene (Sigma-Aldrich) crystals were dissolved in hexane (TCL, HPLC) to grow TIPS-pentacene ribbons by Droplet Pinned Crystallization method (DPC method). Then, Au source and drain electrodes were deposited using shadow masks. The devices measured in this experiment have the channel length of 50 µm and channel width of 960 µm received from our collaborators.

We characterized the morphology of the devices after we received them, as shown in Figure 20, by optical microscopy (Carl Zeiss AxioScope) and atomic force microscopy (AFM, Bruker Dimension Icon). The thickness of Au electrodes is 90 nm. The real width of channel is

calculated by measuring 10 ribbons of TIPS-pentacene which is about 667 µm. The thickness of TIPS-pentacene ribbons is from 35 – 175 nm and the width is from 3.3 – 43 µm.

With this bottom gate OFET, a small drop (5 µL) of pure DEME-TFSI[8] (≥98.5%, ≤ 500 ppm H_2O, Sigma-Aldrich) was dropped on the device in glovebox to cover the whole area of the channel for top gating the device. Then the sample was transferred via load lock to Lakeshore probe station for electrical measurements.

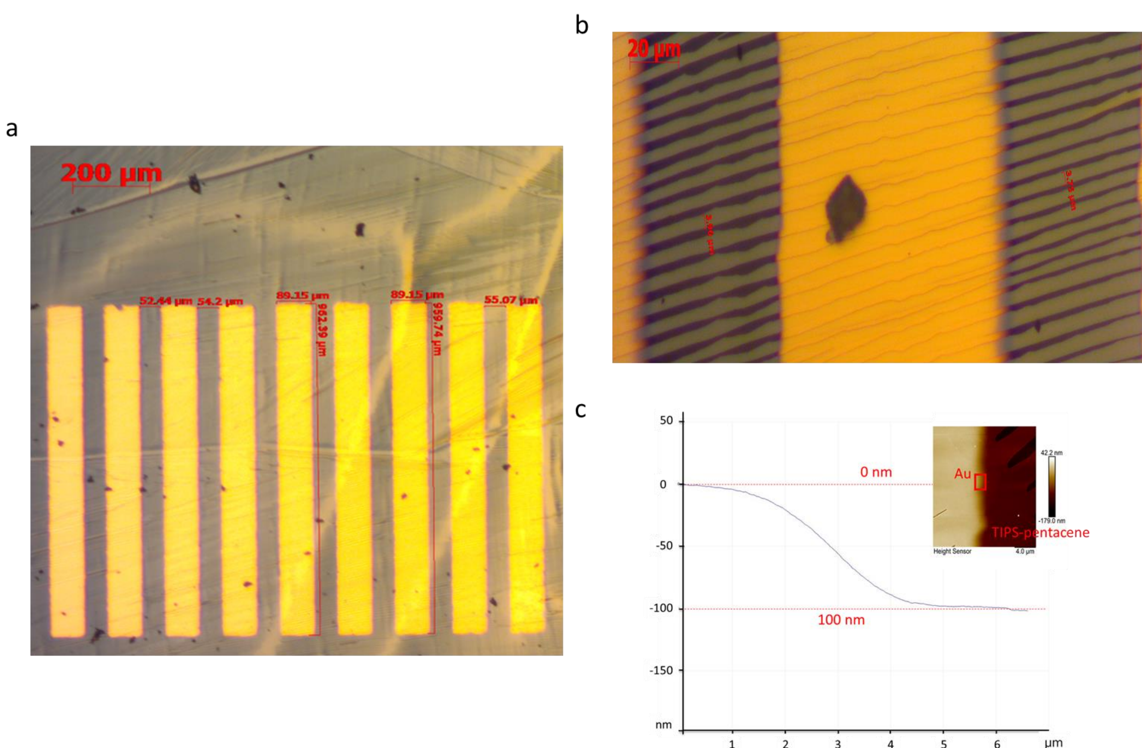

Figure 20: Optical (a and b) and AFM (c) image of TIPS-pentacene FET. a) shows the configuration of the device in which the L = 50 µm and W = 1 mm; b) shows the optical image of the TIPS-pentacene ribbons, which is used to recalculate the actual channel width. c) inset of c shows the AFM image of the tested area and c shows the result of the height of the Au electrodes on TIPS-pentacene which is 100 nm.

[8] Diethylmethyl(2-methoxyethyl)ammonium bis(trifluoromethylsulfonyl)imide

3.2 ELECTRICAL MEASUREMENTS

3.2.1 OFET Electrical Measurement

The output characteristics were acquired at room temperature by applying fixed back gate voltages from 0 to -30 V with a step of -5 V, and double sweeping drain voltage from 0 to -30 V at a sweep rate of 1.8 V/s. The source electrode is grounded and an example of output and transfer characteristics in this experiment were shown in Figure 21a.

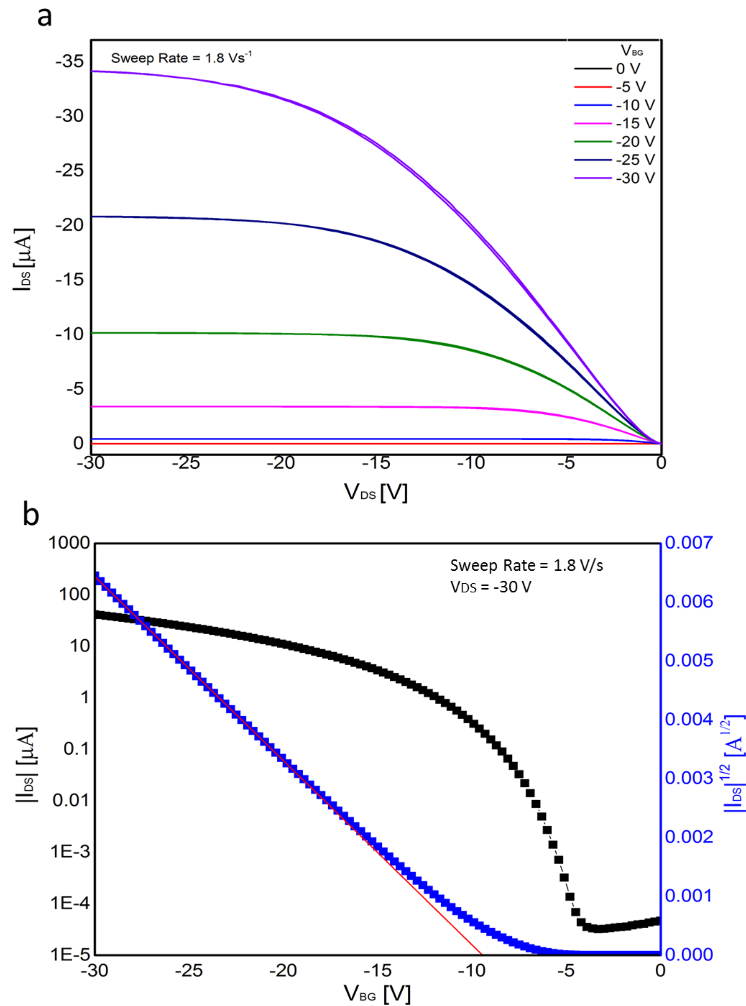

Figure 21: Output, a) and Transfer, b), characteristics of back-gated OFET

Room temperature transfer characteristics were acquired by applying a fixed drain voltage of -30 V, and double sweeping the gate bias from 0 to -30 V at a sweep rate around 1.8 V/s as shown in Figure 21b.

For the top gated OFET, as shown in Figure 22, the same procedure was done however the sweeping voltage should be within ± 3 V due to the limitation of electrochemical window of IL. Also, to top gate the device, we just penetrated one probe in to the IL above the channel to act as a top gate. The sweep rate is much slower, around 0.2 V/s, than the case without electrolyte because the formation of EDL needs more time to achieve equilibrium, that is, the ions need time to respond to the field and form the EDL at the interfaces.

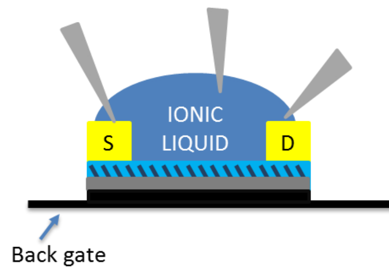

Figure 22: Top gating OFET by a third, top-gate probe. In this figure, IL is dropped onto FET for top gating. When we apply a bias, for example negative bias, on the probe of top gate, cations will be attracted to the gate and the anions will be driven to the semiconductor surface forming a EDL.

3.2.2 GFET Hall Measurement

Just as showed in Figure 17, we use 4 probes to perform the test. Two of them were landed on source and drain pads. Another two probes were landed on either 1 and 2 Hall bars or 3 and 4 Hall bars, to perform the Hall measurement at 220 K. Before we deposit the electrolyte, we swept current from -500 to 500 nA on the drain electrode and set zero current through the Hall

bars at a sweep rate of 25 nA/s. Hall voltages are measured on each Hall bar at 0 and ±1 T magnetic field for calculation of sheet carrier density and hall mobility.

For the side-gated GEFTs by PEO/$Mg(ClO_4)_2$ electrolyte, we first increased the temperature to 343 K to make the ions freely move in the system. Then, we put two probes on source and drain electrodes with a drain-source voltage of 20 mV. After that, we put a third probe on the side gate with a gate voltage of ±3, ±2, ±1 and 0 V in separate experiments. Next, we did an I/V-t sampling and when the current saturated, we started to decrease the temperate at a cooling rate of 6 K/min to 220 K which is below the glass transition temperature of PEO/$Mg(ClO_4)_2$ so that we could lock the ions in place. I/V-t sampling is continuously performed to make sure the ions are doping the channel during cooling process, that is, if the current is about the same compared to saturation current at 434 K during the cooling process, the ions are locked in place and we succeed to dope the channel. At 220 K, we did the same Hall measurement as presented above to obtain sheet carrier density and hall mobility with electrolyte doping.

4.0 GFET RESULT AND DISCUSSION

Summary: The objective of this portion of the project is to determine whether or not the valency of cation in the electrolyte will impact the doping behavior of the electrolyte (i.e., a valency of 2+ may induce twice as many charges as 1+). To evaluate this hypothesis, we performed Hall measurement on GFETs, side-gated with a divalent ion electrolyte, PEO/$Mg(ClO_4)_2$ and sheet carrier densities of $3.9 \pm 2.9 \times 10^{13}$ cm^{-2} for holes and $2.2 \pm 0.4 \times 10^{13}$ cm^{-2} for electrons were obtained at V_{SG} equal -2 V and +2 V respectively. Our group previously reported $5.1 \pm 0.4 \times 10^{13}$ cm^{-2} for holes and $1.1 \pm 1.0 \times 10^{13}$ cm^{-2} for electrons at the same gate voltage by top gating the same GFET using PEO/$LiClO_4$ (i.e., a monovalent ion, Li^+).[28] Therefore, the preliminary results of this work suggest that valency of cation does not impact the sheet carrier density; however, there are a few important experimental details that may cause differences between the measurements of the divalent versus monovalent electrolytes, and these will be described below.

The sheet carrier density of the graphene Hall bar is first measured prior to adding an electrolyte. This approach both (1) ensures that the device is performing as expected with sheet carrier densities and mobilities consistent with the literature and (2) provide a control measurement for comparison to the electrolyte-gated devices. Figure 23 shows the time-resolved Hall measurements at 220 K at the magnetic field of +1 T before depositing the electrolyte. The measurement is repeated three times and I_D and the average values of R_H, n_s and μ_H of the three measurements are plotted in Figure 23 as a function of time. The results for Hall bars 3 and 4 are

show in Figure 23a and the results for Hall bars 1 and 2 are shown in Figure 23b. The sheet carrier density is $-5.5 \pm 1.8\times10^{12}$ cm^{-2} and Hall mobility is $2.9 \pm 0.8\times10^{4}$ cm^{2}V^{-1}s^{-1} in Figure 23a; while the calculated sheet carrier density in Figure 23b is $-5.7 \pm 1.7\times10^{12}$ cm^{-2} and Hall mobility is $0.89 \pm 0.1\times10^{4}$ cm^{2}V^{-1}s^{-1}. These results are in good agreement with the previously reported values on monolayer graphene which is on the order of 10^{12} cm^{-2} and 10^{4} cm^{2}V^{-1}s^{-1} for sheet carrier density and mobility, respectively.[27] In Figure 23, the large spikes at zero I_{DS} are caused by the appearance of zero I_{DS} in the numerator when calculating R_H, n_s and μ_H and the fluctuations around zero I_{DS} might come from the instability of the probes at temperatures below room temperature. Additionally, fluctuations in mobility might also come from two separate measurements for V_{12} and V_{34} and if the two measurements do not match, the fluctuations around mean value could become larger.

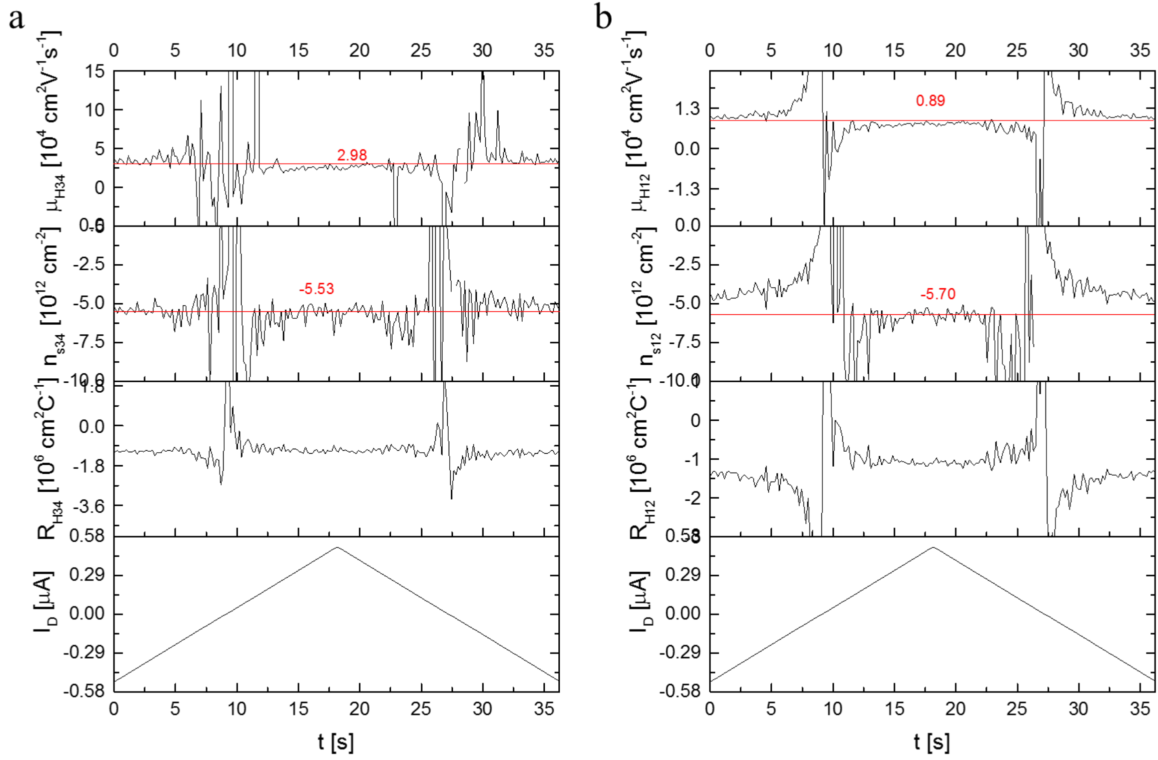

Figure 23: Time-resolved Hall measurement of GFET without electrolyte at T = 220 K and B = +1 T by sweeping I_{DS} from 500 to -500 nA. The figure shows I_D, R_H, n_s and μ_H as a function of time. a) result of Hall measurement using Hall bar 3 and Hall bar 4; b) result of Hall measurement using Hall bar 1 and Hall bar 2.

Whereas the data for Figure 23 were collected at +1 T, the data for Figure 24 are collected at -1 T at 220 K prior to depositing the electrolyte. Hall bar 3 and 4 are shown in Figure 24a and Hall bar 1 and 2 in Figure 24b. The sheet carrier density and hall mobility in Figure 24a are $-5.8 \pm 1.3\times10^{12}$ cm^{-2} and $2.0 \pm 0.8\times10^{4}$ $cm^2V^{-1}s^{-1}$, and in Figure 24b are $-4.3 \pm 1.1\times10^{12}$ cm^{-2} and $1.1 \pm 0.2\times10^{4}$ $cm^2V^{-1}s^{-1}$. Because these results are in good agreement with the results obtained at +1 T (Figure 23), this indicates that the direction of magnetic field will only change the direction of electron migration but will not change the sheet carrier density and Hall mobility.

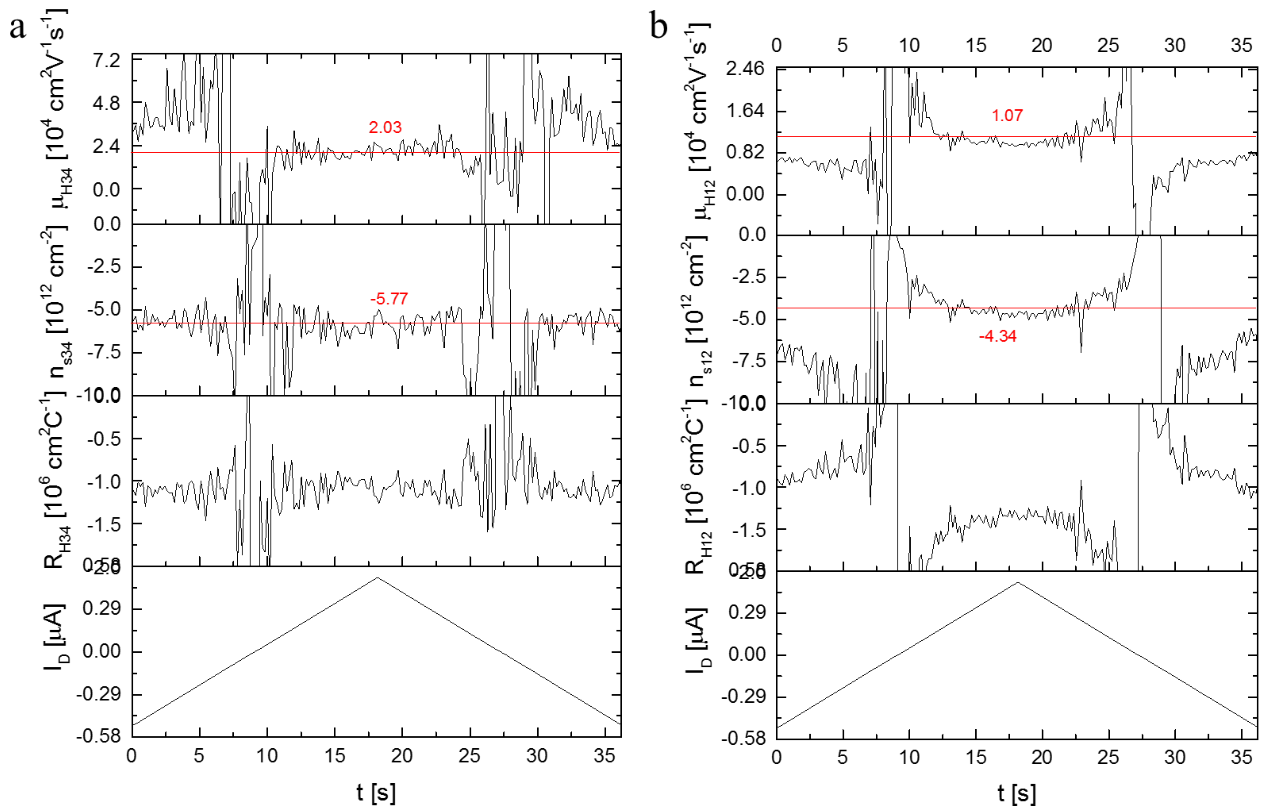

Figure 24: Time-resolved hall measurement of GFET without electrolyte at T = 220 K and B = -1 T by sweeping I_{DS} from 500 nA to -500 nA. The figure shows I_D, R_H, n_s and μ_H as a function of time. a) result of Hall measurement using Hall bar 3 and Hall bar 4; b) result of Hall measurement using Hall bar 1 and Hall bar 2.

Table 1: Summary of sheet carrier density and Hall mobility before deposition of electrolyte on GFET

	Sheet carrier density [cm^{-2}]		**Hall mobility [cm^{2}V^{-1}s^{-1}]**	
	+1T	-1T	+1T	-1T
Hall bar 1&2	-5.7 ± 1.7×10^{12}	-4.3 ± 1.1×10^{12}	0.89 ± 0.1×10^4	1.1 ± 0.2×10^4
Hall bar 3&4	-5.5 ± 1.8×10^{12}	-5.8 ± 1.3×10^{12}	2.9 ± 0.8×10^4	2.0 ± 0.8×10^4

$PEO/Mg(ClO_4)_2$ is drop-cast onto the samples in glovebox and transferred to the probe station using the load lock without air exposure. The first measurements are I/V-t sampling with V_{DS} = 20 mV, and side gate biases of 0, ±1, ±2, and ±3 V at 343 K in each measurement. When a positive side gate bias is applied, anions will migrate to the side gate and cations will migrate to the channel, forming an EDL. On the contrary, when a negative side gate bias is applied, cations will be attracted to the side gate and the EDL will formed between anions on the channel and induced charge. An example of a current versus time measurement with a side gate voltage of 3 V and V_{DS} = 20 mV is shown in Figure 25. An increase in the drain current and simultaneous decrease in the leakage current to the side gate indicate that the ions are migrating in the system to form EDL. After about 20 seconds, I_{DS} saturates indicating the device has reached equilibrium, or complete EDL formation. Once the EDL is established, the temperature is decreased to 220 K while continuously applying the side gate voltage to lock the ions in position.

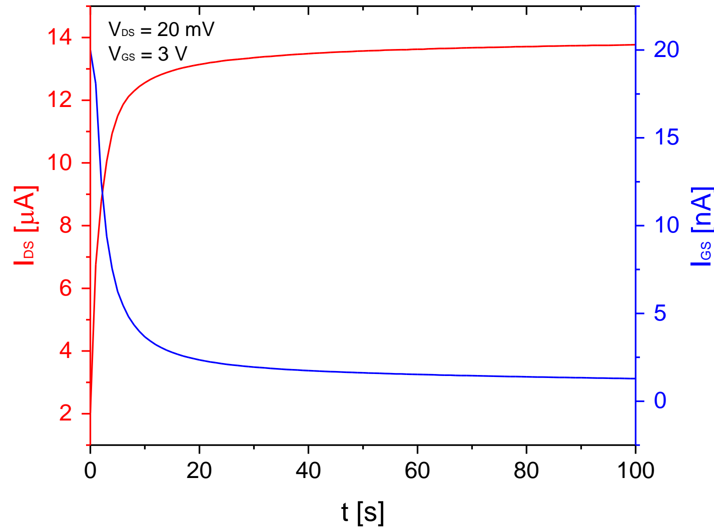

Figure 25: I/V-t sampling with $PEO/Mg(ClO_4)_2$ side gating at side gate of 3 V and V_{DS} = 20 mV. The left y-axis shows I_{DS} and the right y-axis shows I_{GS} and we can see clear the increase of I_{DS} and decrease of I_{GS} which indicates the motion of ions to form EDL.

Figure 26a and b shows the sheet carrier density, and Figure 26c and d shows the Hall mobility, for the electrolyte-gated GFET at varying side gate bias and magnetic fields at 220 K. Figure 26a and c show the result at magnetic field of +1 T and figure 26b and d show the result when the magnetic field is -1 T. Both at -1 T and +1 T magnetic field, the sheet carrier density increase with the increase of side gate bias as expected. The reason is that when the gate bias increases, larger amount of ions will pack into the EDL at the gate, and more counter ions will be driven to the surface of graphene channel. Consequently, a larger number of ions at the graphene surface will induce more carriers in the channel to maintain charge neutrality, leading to a larger n_s. What`s more, the similar trend and magnitude at both magnetic field polarities confirms that the sign of magnetic field will not change the behavior of this GFET.

The largest sheet carrier density shown here is $7.9 \pm 5.1 \times 10^{13}$ cm^{-2} for holes at V_{SG} = -3 V and $3.4 \pm 1.3 \times 10^{13}$ cm^{-2} for electrons at V_{SG} = 3 V and the sheet carrier densities obtained with a side gate bias are all an order of magnitude larger than that in the case without electrolyte gating. This indicates the effective EDL doping.

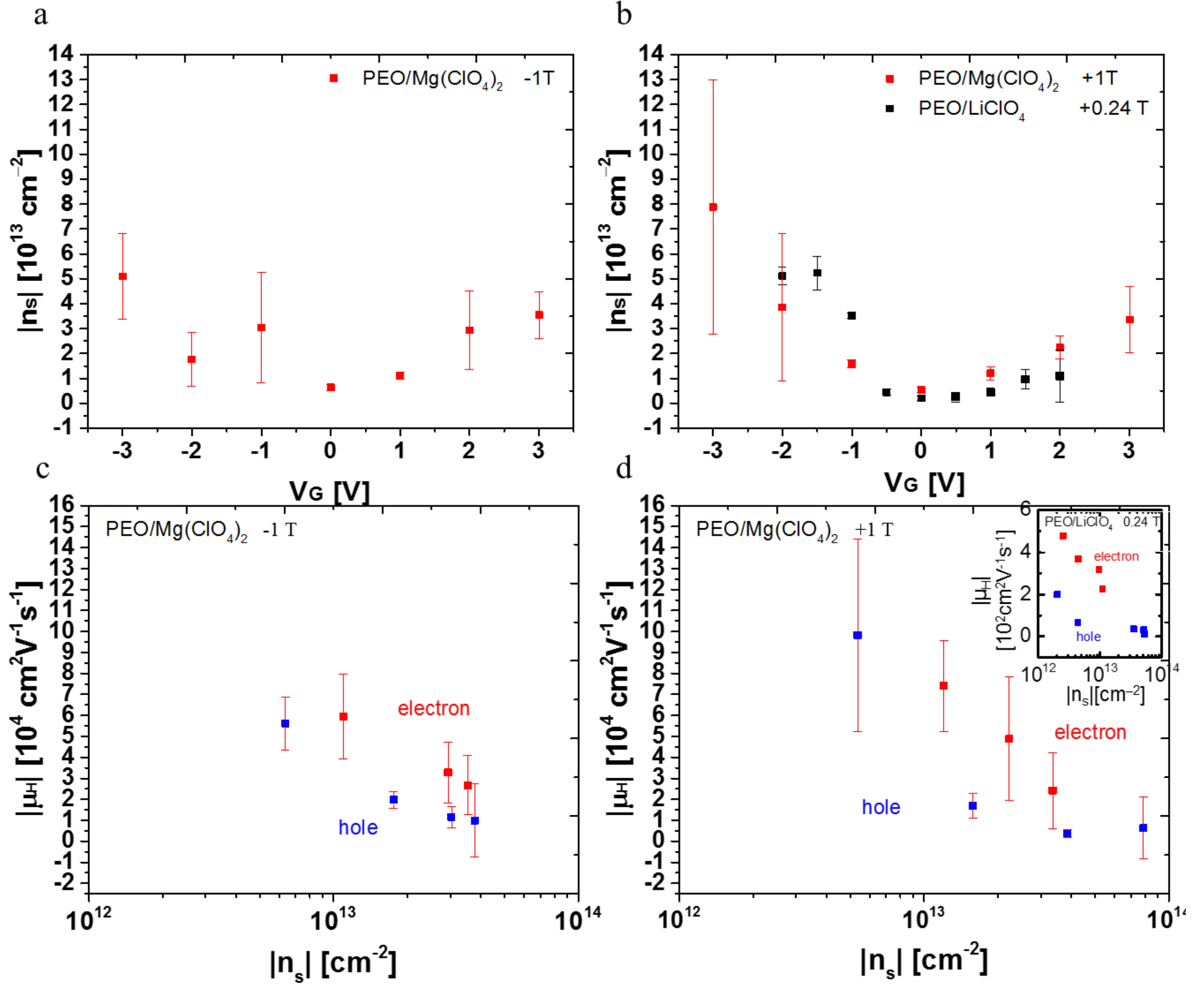

Figure 26: Results of Hall measurements. Sheet carrier density, n_s, as a function of gate voltage, V_G, at 220 K for Hall bar devices at (a) negative and (b) positive magnetic field. Devices gated with PEO/$Mg(ClO_4)_2$ are shown in red with +/- 1 T magnetic field, and PEO/$LiClO_4$ are shown in black with a magnetic field of 0.24 ± 0.01 T measured at 298 K; c) and d) hall mobility, μ_H, as a function of sheet carrier density, n_s. Mobility of electrons is shown in red and mobility of holes is shown in blue. The inset The GFET gated with PEO/$LiClO_4$ is shown in black in inset figures at magnetic field of 0.24 ± 0.01 T measured at 298 K.

In the field of electrolyte gating, PEO/$LiClO_4$ is often employed to induce large carrier density. Li *et al.*,[28] reported sheet carrier densities of $5.1 \pm 0.4 \times 10^{13}$ cm^{-2} for holes and $1.1 \pm 1.0 \times 10^{13}$ cm^{-2} for electrons by top gating the GFET with PEO/$LiClO_4$ at the gate bias of ±2 V.

Their Hall measurements are performed at a magnetic field of 0.24 ± 0.01 T at 298 K on the same GFET but with a top gate. At the same side gate bias, a sheet carrier density of 3.9±2.9 $\times 10^{13}$ cm^{-2} for holes and 2.2±0.4 $\times 10^{13}$ cm^{-2} for electrons can be achieved by using PEO/$Mg(ClO_4)_2$ which suggests comparable sheet carrier density for both electrons and holes in our case. The similar electron and hole sheet carrier densities in PEO/$Mg(ClO_4)_2$ and PEO/$LiClO_4$ gated GFETs suggest that valancy of the ions will not have an impact on the carriers induced in the channel at the same gate bias although Mg^{2+} can induce two electrons in formation of EDL while Li^+ can only induce one electron. A possible reason for comparable sheet carrier density is that at same gate bias, the charges needed to screen this gate electric field are the same, that is, if we apply a same negative gate bias, one Mg^{2+} will be replaced by two Li^+, and the amount of ClO_4^- driven to the graphene surface is the same; while if we apply a same positive gate bias, Mg^{2+}, equal to half number of Li^+, will be driven to form the EDL. However, our side gate may not work as effective as top gate in electrolyte gating because the PEO/$LiClO_4$ film thickness is only 1 μm[28] while the distance between the side gate and the channel is at least 500 μm. So, with the same gate bias, the electric field felt by graphene channel could be in lower in side gating leading to lower sheet carrier density. Nonetheless, the best way to prove this is an issue is to repeat the measurements using a side gate for PEO/$LiClO_4$ gated GFET. Additionally, by linear regression, the estimated capacitance density of the EDL (C_{EDL}) using PEO/$Mg(ClO_4)_2$ is 2.92 ± 1.37 μF/cm^2 for anions` EDL and 1.84 ± 0.17 μF/$cm^2$ for cations` EDL by the linear relation of $n_S = C_{EDL}V_{SG}/(2q)$.

We measured a maximum Hall mobility of 9.8 ± 4.5 $\times 10^4$ $cm^2V^{-1}s^{-1}$ at +1 T at 0 V gate bias and 5.9 ± 2.0 $\times 10^4$ $cm^2V^{-1}s^{-1}$ at -1 T at +1 V gate bias. Figure 26c and d indicate that with the increase of sheet carrier density, Hall mobility decreases. This is because carrier scattering

increases with the increasing density of charge in the channel. The fact that the results at opposite magnetic field are consistent with each other except the data points at V_{SG} = -3 V.

As discussed above, PEO/$Mg(ClO_4)_2$ gated GFET shows comparable sheet carrier density as that of GFET gated with PEO/$LiClO_4$ which indicate the valency of ions will not have an impact on electrolyte gating. However, there are still some details needed to study, like to perform the Hall measurement at same magnitude and polarity of magnetic field on PEO/$LiClO_4$ side-gated GFET without exposure to ambient to make a better comparison with our results. What`s more, we can top gate the GFET with PEO/$Mg(ClO_4)_2$ to study whether top gate will deliver better results compared with our study in this thesis. Additionally, at high gate bias, like 3V, it seems the polarity of magnetic field will have an impact on the Hall measurement so that it is worthwhile to study the impact of magnetic field. Finally, how the water concentration affects PEO/$Mg(ClO_4)_2$ electrolyte is also interesting to know.

5.0 OFET RESULT AND DISSCUSSION

5.1 BACK-GATED TIPS-PENTACENE FIELD EFFECT TRANSISTORS

Several TIPs-pentacene samples from Prof. Hanying Li at Zhejiang University were sent to the Fullerton lab for electrolyte gating. Prior results on this material from the Li lab are shown in Figure 27 where the backgate oxide is 300 nm SiO_2.[16] Figure 27 a) shows the output characteristics. They reported a maximum saturation current of 20 μA when the gate voltage is -120 V sweeping V_{DS} from 0 to -120 V. Figure 27 b) shows transfer characteristics in black and the square root of I_{DS} in blue which is used to calculate mobility and threshold voltage which are 5.0 $cm^2V^{-1}s^{-1}$ and -82 V separately with an on/off ratio of 1.1×10^5.

The samples used in this thesis were prepared in a similar manner; however, the backgate was 90 nm SiO_2 and there was no BCB[9] layer, which is to eliminate electron traps in the OFET. Because the electric field that the dielectric can withstand is proportional to the dielectric thickness, and because the breakdown strength of a good dielectric is ~ 1 V/nm, we choose to use approximately one-third of this maximum (i.e., -30 V) for both V_{DS} and V_{GS}, and the voltage is negative for the reason that TIPS-pentacene is a *p*-type semiconductor.

[9] divinyltetramethyldisiloxane-bis(benzocyclobutene)

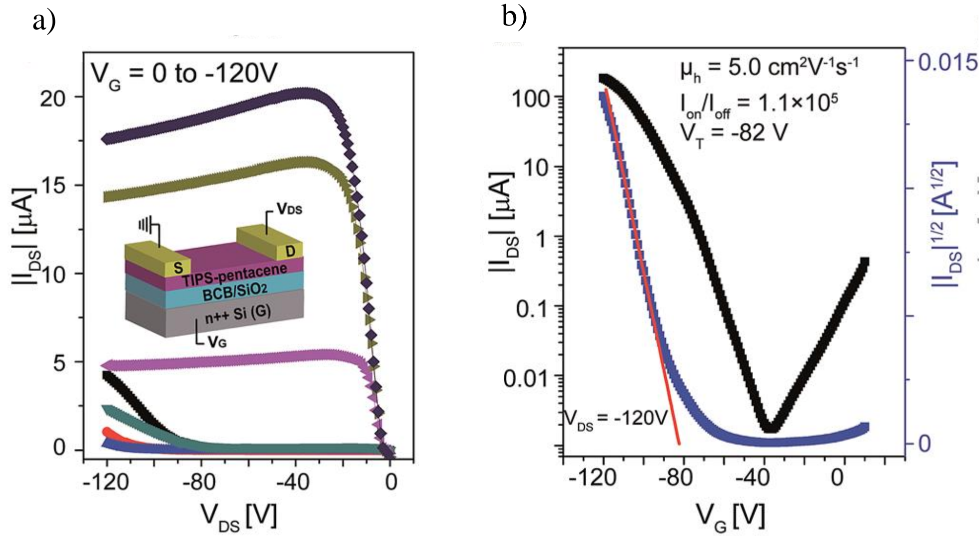

Figure 27: Output, a), and transfer, b), characteristics of bottom-gated TIPS-pentacene FET reported by Xue *et al.*[16]. With a backgate oxide thickness of 300 nm, they used a maximum voltage for both V_{DS} and V_{GS} of -120 V. a) shows a maximum saturation current of 20 μA. In b), black curve shows the transfer characteristics and blue one shows the square root of black curve which is used to calculate mobility and threshold voltage as 5.0 $cm^2V^{-1}s^{-1}$ and -82 V with an on/off ratio of 1.1×10^5. Schematics from reference 16.

The first measurements on the TIPS-pentacene devices without electrolyte were designed to characterize the effect of sweep rate on the transfer characteristics (*i.e.*, $I_{DS} – V_{BG}$), as shown in Figure 28. The double sweep started an ended at zero V_{BG} and the red arrows indicate the sweep direction. The difference observed between forward and backward sweeps is called hysteresis and this is usually caused by charge traps in semiconductor or dielectric. We can see that with the decrease of sweep rate from 1.8 V/s to 50 mV/s, the hysteresis is getting larger as shown in Figure 28. This might be explained by the fast response of carriers in TIPS-pentacene, and small amount of carrier traps, like oxygen, due to tests under vacuum. However, when we slow down the sweep rate from 1.8 V/s to 50 mV/s, the hysteresis becomes a little larger and the maximum current decreases. As mentioned above, this phenomenon is likely caused by charge traps which is a kind of defect that can "trap" carriers. If the traps, either in semiconductors or dielectrics, are filled fast and emptied slowly, a faster sweep rate could give larger maximum current.[29] Based

on these results, we determined to use 1.8 V/s as our sweep rate because it has the highest I_{DS} and smallest hysteresis among the sweep rate range.

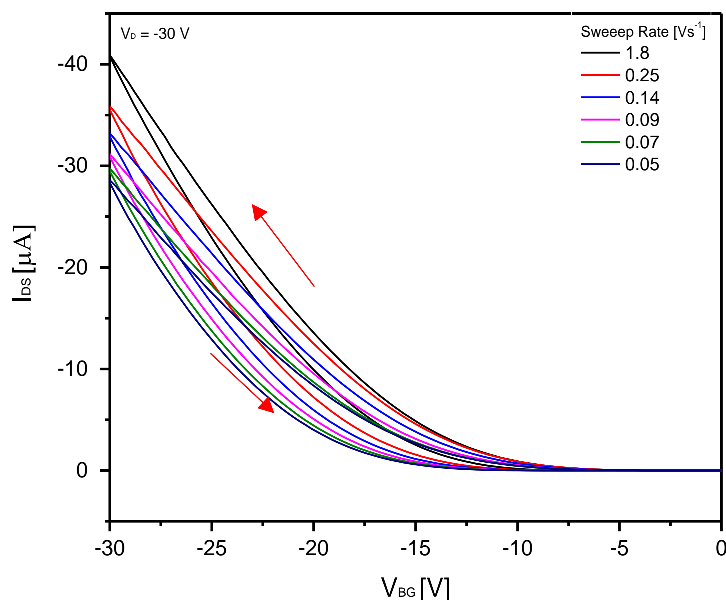

Figure 28. Effect of sweep rate on transfer characteristics on back-gated TIPS-pentacene OFET. V_{DS} is set to -30 V.

To ensure that the devices we received have similar electrical characteristics as those published by the Li lab previously (i.e., data shown in Figure 27), we measured the output and transfer characteristics, shown in Figure 29. As a reminder, the difference between the devices in Figure 27 and 29 is that Figure 27 has 300 nm of SiO_2 backgate oxide while Figure 29 has 90 nm SiO_2. The output characteristics in Figure 29a show that with the increase of negative backgate bias, the saturation current becomes larger, which indicates *p*-channel operation mode because when a negative bias is applied on the gate, holes will be induced in the channel. The magnitude of the drain current versus V_{DS} is well controlled by modulating the backgate voltage, indicating good gate control. The maximum saturation current at -30 V is 45 μA compared with

20 μA at V_{BG} = -120 V in the manuscript by Xue et al.[16]. In our experiments, all the devices showed a maximum saturation current above 20 μA in the output characteristics at V_{BG} = -30 V.

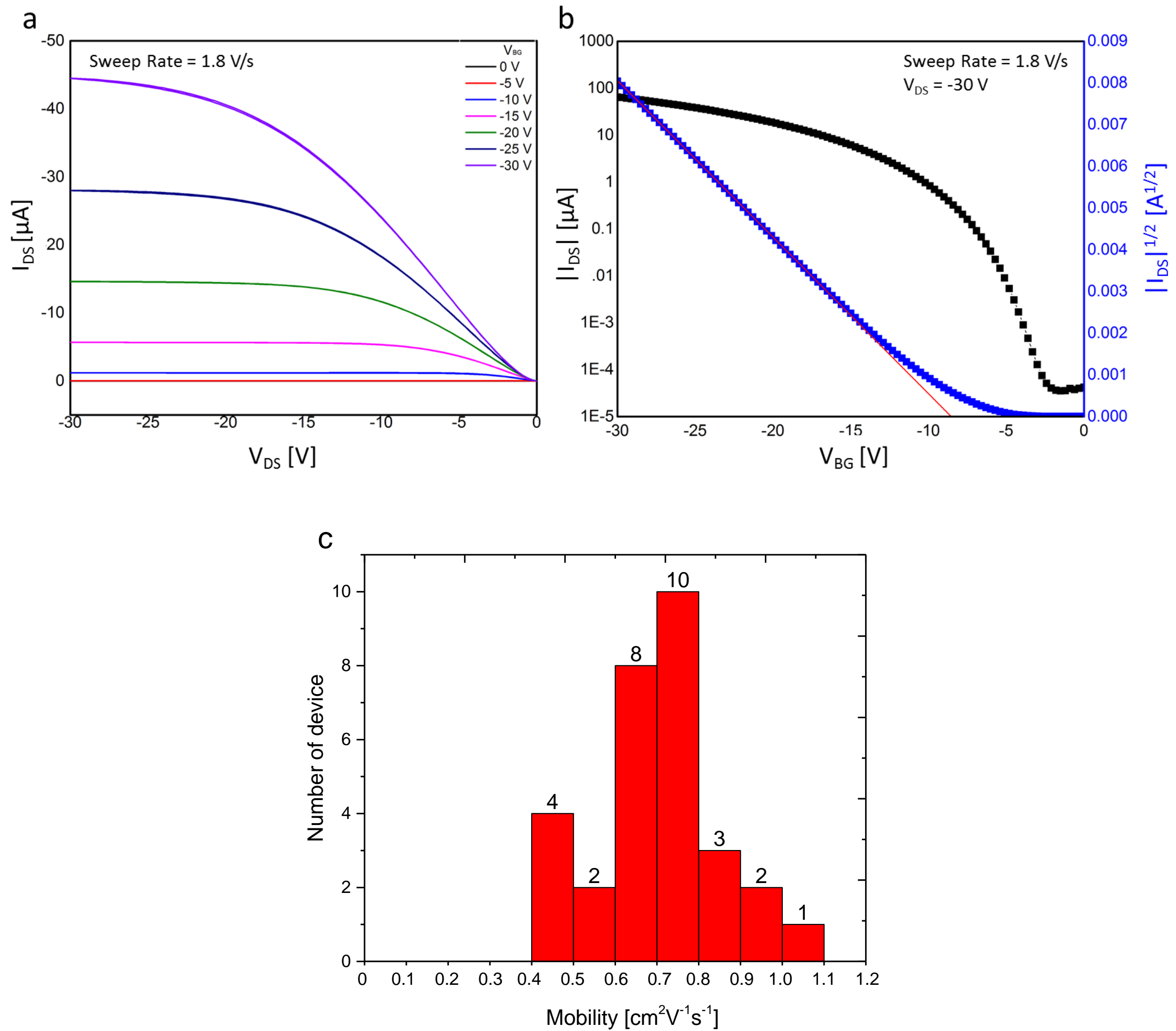

Figure 29: Output, a), and transfer, b), characteristics of SiO_2-gated TIPS-pentacene OFET and c) shows mobility distribution of 30 devices.

Also, the backgate leakage current is small, about 2000 times smaller than I_{DS}, as shown in Figure S1. Figure 29b shows the single-sweep transfer characteristics (double sweep transfer

characteristics shown in Figure S1). The black curve is I_{DS} and blue curve is the square root of black curve. The average hole mobility is 0.72 $cm^2V^{-1}s^{-1}$ (range: from 0.47 $cm^2V^{-1}s^{-1}$ to 1.08 $cm^2V^{-1}s^{-1}$), as shown in Figure 29c, on/off ratio is larger than 10^5 and the threshold voltage range from -6.18 to -9.54 V. Due to a four times smaller electric field, five times smaller hole mobility and ten times smaller threshold voltage are obtained compared to what reported by Xue *et al.*[16].

5.2 IONIC LIQUID TOP-GATED TIPS-PENTACENE FIELD EFFECT TRANSISTORS

DEME-TFSI was employed as our electrolyte for top-gating of the TIPS-pentacene OFET. The main reason why we choose this ionic liquid is the large electrochemical window (ECW), -3.5 to 3 V. Figure 30 shows our measurement of the electrochemical window of DEME-TFSI. Two probes were inserted into a drop of the ionic liquid and the current between the probes was measured as a function of voltage. We can see in this figure that the current through two probes are pretty small, only 11.1 nA within the range of -3.5 V to 3 V, which indicates small ion conduction in this range. However, when we further increase the voltage, the current increase sharply outside that range which indicates high ion conduction due to reduction and oxidation reactions. These data show that the voltage must be limited within the range from -3.5 V to 3 V to achieve purely electrostatic doping. This large ECW could possibly meet the requirement of larger sweeping voltage range required for OFETs with such large channel dimensions and low electrical conductivity.

Another reason for choosing DEME-TFSI is that it has a large anion, size of 3.9×8.0 Å^2,[30] compared with the distance between two TIPS-pentacene molecules which is 3.47 Å,[31] so that when we apply negative bias on top gate, anions will be driven to the surface of TIPS-pentacene

and the lager anion ensures there will be no intercalation of anions into the semiconductor. Additionally, volume of the cation is 169.7 Å^3,[32] which is not possible to intercalate in the case of positive bias.

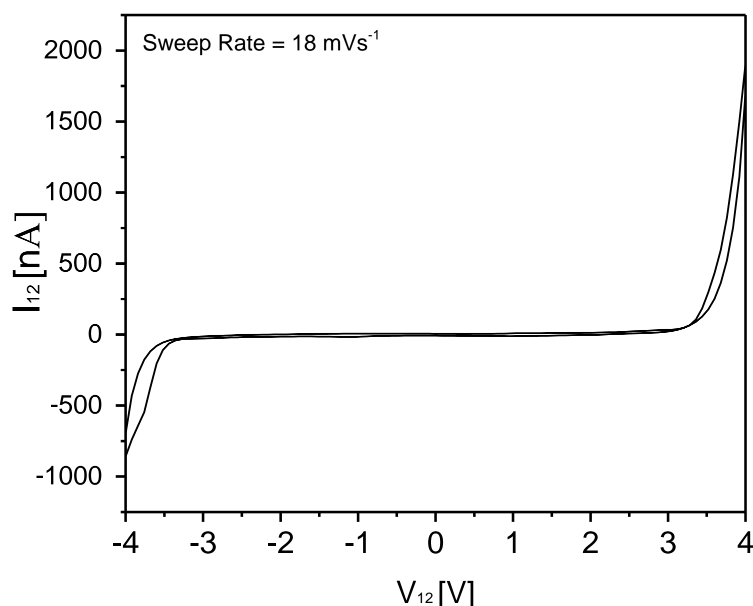

Figure 30: Electrochemical window (-3.5 V to 3 V) of DEME-TFSI.

Provided with the informaton above, we top-gated the TIPS-pentacene devices with DEME-TFSI. Figure 31a shows the output characteristics at top gate voltage (V_{TG}) = -2 V when sweeping V_{DS} from 0 to -3 V. The left y-axis shows drain-source current and the right y-axis shows leakage current to the top gate. Unfortunately, I_{DS} is only one order of magnitude larger than leakage current to the top gate, I_{TG}, which indicates that this ionic liquid is too leaky to use as a dielectric in this device. Figure 31b shows that when we float the top gate in vacuum, and only land two probes on drain and source electrodes, I_{DS} is the same as that in Figure 31a, however, I_{TG} is near zero. This confirms that the leakage current is from drain to the top gate and this large leakage current might due to large ionic conductivity. Furthermore, the more important

conclusion from these two figures is that the top gate is not doping the channel at all because the I_{DS} is the same with or without the top gate. The reason why the current is not saturating is because the bias we can apply (i.e., within the ECW) is too small due to the electrochemical limitation of ionic liquid.

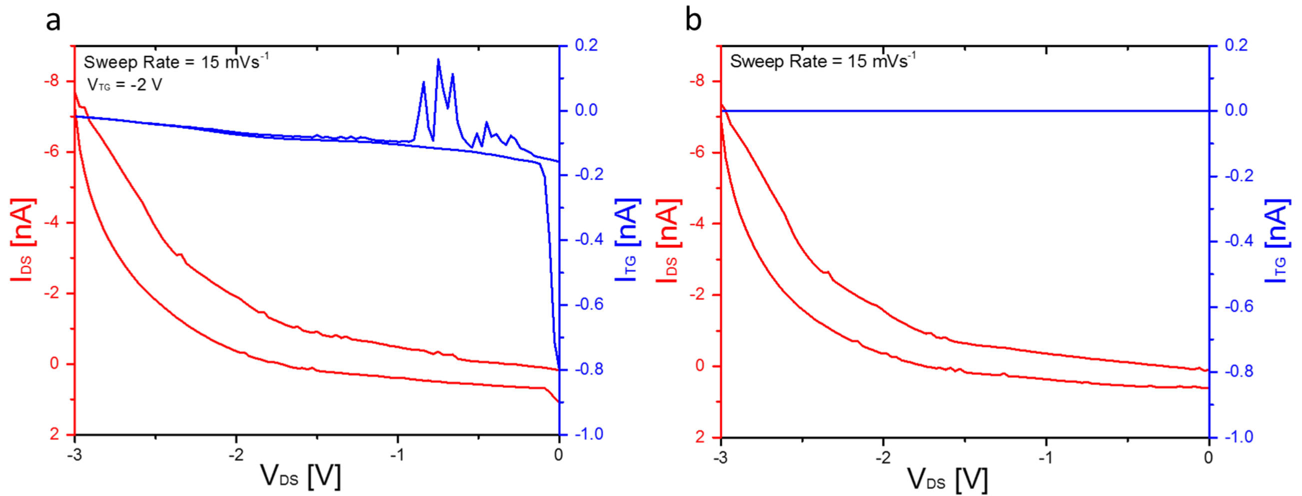

Figure 31: Output characteristics of TIPS-pentacene OFET when top gated by DEME-TFSI at V_{TG} = -2 V. a) red curve shows the drain-source current and blue curve shows the leakage current to the top gate. Leakage current is just an order of magnitude lower than drain-source current; b) output characteristics when floating the top gate in vacuum. We can see that similar drain-source current is achieved in this case. We can conclude that top gate is not doping the channel.

In Figure 31a, when we use one probe as our top gate, a very weaker electrical field is produced due to the small area of the tip (~10 μm tip radius), and this may not be sufficient to drive enough ions to effectively dope the long channel. However, much larger area of drain and source electrodes can provide more spots for ions to attach even if V_{DS} is small leading to large leakage current. In addition, the ionic liquid is actually more conductive than the channel material, consequently, it is very hard to tell whether the tested I_{DS} is through the channel or directly flowing through ionic liquid. Even if the current is flowing through channel, the top

gating is not better than the original device at V_{BG} = -20 V, as shown in Figure S2. To conclude this part, a much smaller top gate compared to the channel dimension leads to inefficient doping of the channel material and this will contribute to large leakage current and small I_{DS}.

In the experiment, we also found that due to the motion of the liquid itself, a side leakage path can exist due to the spreading of the IL to the sample holder during transfer. To prevent the spreading of the IL to the sides of the device, electrically insulating Kapton tape was added, as shown schematically in Figure 32. However, when we apply a bias to the back gate, redox peaks are observed, as shown in Figure 33. This observation is similar to what is reported by Fujimoto et al.,[33] in which the authors indicates that electrochemical reactions are occurring between DEME-TFSI and their organic channel material, Octathio[8]circulene.

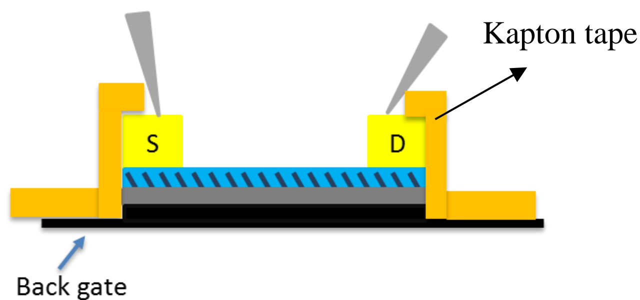

Figure 32: Attach Kapton tape around the device to avoid ionic liquid spreading out.

There are three possibilities for the redox reactions. First, electrochemical reactions are occurring in DEME-TFSI itself, possibly due to the large area of the electrodes providing sufficient area for the DEME-TFSI molecules to attach and react. However, this is not very likely because we are staying within the electrochemical window of the electrolyte. The second possibility is that electrochemical reactions happen within the TIPS-pentacene itself, possibly because the electric field-driven molecular configuration changes during the experiments and

this change might create dangling bonds on TIPS-pentacene which are prone to react. The most possible case is the reaction between DEME-TFSI and TIPS-pentacene because of the attachment of Kapton tapes which might stretch the TIPS-pentacene backbone so that the packing distance is larger and ions can intercalate between the molecules. Furthermore, as mentioned above, there are previous reports of this IL reacting with an organic semiconductor.[33]

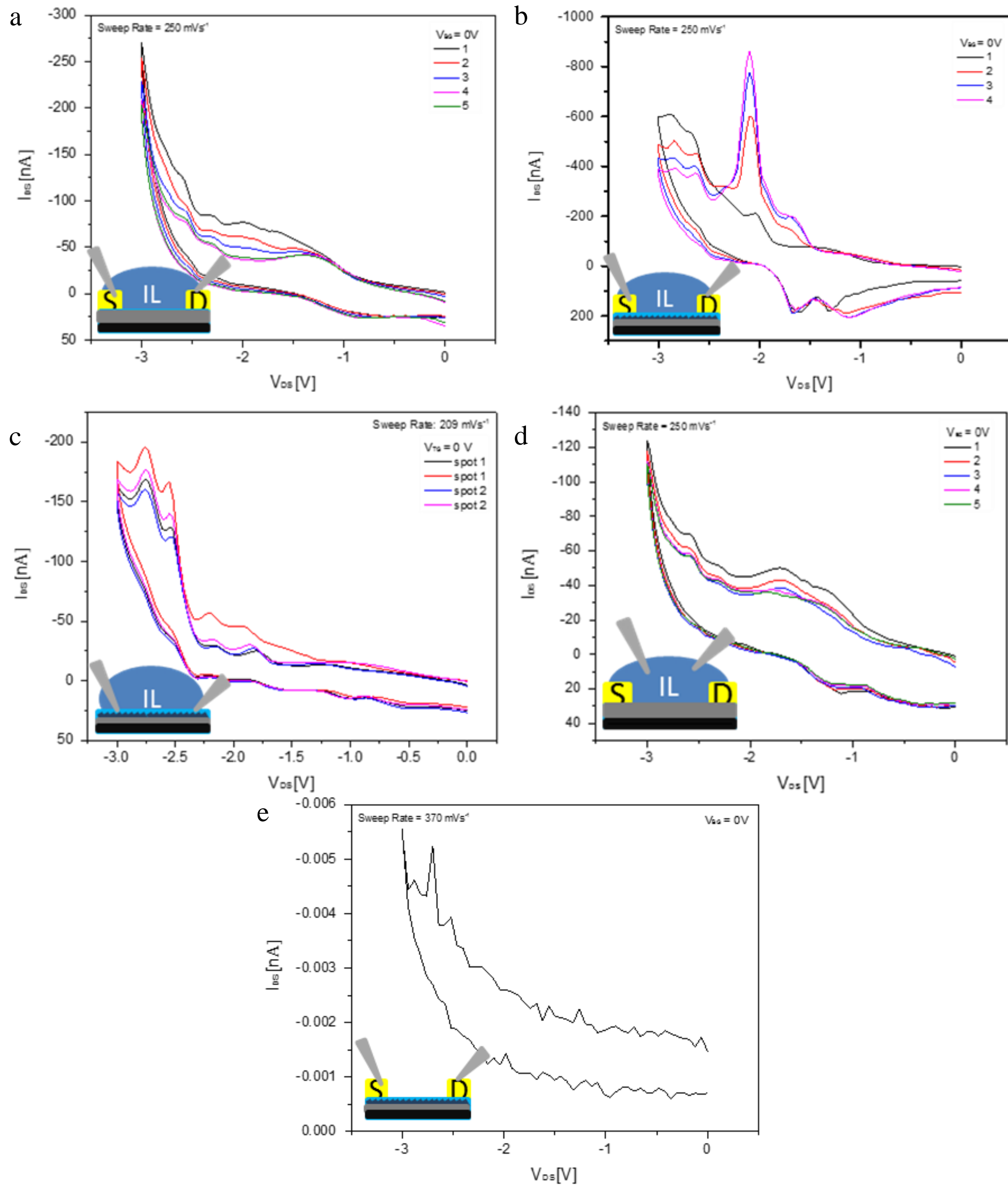

Figure 33: Output characteristics when back-gated to prove reaction between DEME-TFSI and TIPS-pentacene and the inset shows where the probes are landed. a) to d) shows the case with IL and f) shows the case without IL. a) shows the case when two probes are landed on Au pads deposited directly on SiO_2; b) shows the case when two probes are landed on Au pads on TIPS-pentacene; c) shows the case when two probes are landed directly on TIPS-pentacene; d) shows the case when two probes floated in IL where there is no TIPS-pentacene in this area; e) shows the output characteristics before we top gate the device.

To determine the mechanism, we set V_{BG} to zero and use two probes with different placement in the IL to perform I/V tests. Figure 33 a to f shows multiple consecutive I/V sweeps when back gate is 0 V and the inset figures shows the position of the probes for each case. In Figure 33a, the probes were placed on two adjacent Au pads on SiO_2 without any organic semiconducting channel and there are no obvious redox peaks. This indicates that although the Au pads are large, the redox reactions will not happen on DEME-TFSI itself, which make sense because we are confining our applied bias window to the ECW of the electrolyte. Figure 33b shows that when we land probes on two Au pads on TIPS-pentacene in IL, there appear redox peaks and we can see that in the consecutive sweeps, the intensity of peaks increase. Figure 33c shows that when we directly land two probes on TIPS-pentacene in IL but not on Au pads, we can not see obvious redox peaks and comparing Figure 33c to Figure 33b, both of which include IL and TIPS-pentacene, when the contact area for the IL is smaller, (i.e., no Au pads) the intensity of peaks is lower suggesting that the redox reactions correlate to the area of contacts. Figure 33d shows that when we float two probes above the SiO_2 in the IL and there is no semiconducting channel in this case. In this figure, there is no obvious redox peaks and here 'float' means that we do not let the probes touch the Au pads but just penetrate them into the IL and this confirms that the contact area matters because by comparing Figure 33a and d, where there is no TIPS-pentacene in both case, we know there will be no redox reaction, however, when the contact area for DEME-TFSI is larger in Figure 33a, the current from drain to source is larger which indicates that there will be a portion of current in Figure 33b contributed by ionic conduction, i.e., ionic liquid will be too leaky when the dimension of the source and drain electrode is much larger than gate. Figure 33e shows the output characteristics before we drop

ionic liquid onto the device with the same voltage range and there is no redox peaks in this figure indicating TIPS-pentacene itself will not be oxidized in this voltage range.

With the discussion above, we think a possible explanation for the peaks is that there are electrochemical reaction happens between IL and TIPS-pentacene. Additionally, the contact area matters a lot - larger contact area provides more spots for the molecules to react, resulting in larger current. What`s more, as explained by Fujimoto[33], in Figure 33b, the first run is not showing obvious redox peaks is because of overpotential effect which indicates that the first penetration of ions into the channel materials needs an extra potential and after this very first run, due to an increasing number of ions penetrating into the channel material, the intensity of the peaks increases. Because the oxidation peak is at -2 V and the first reduction peak is at about -1.2 V, we have to limit our sweeping window within -1.2 V which further limit the operation of this top-gated device, and further decreases the already poor gate control.

With the knowledge above, we further scale down the sweep range: V_D from 0 to -60 mV and V_{TG} = -0.2 V. One reason is to avoid the redox reactions shown in Figure 33, and another reason is the need to use a larger V_{TG}, compared to V_{DS}, to effectively dope the channel and have smaller leakage current. We first did an I/V-t Sampling, as shown in Figure 34a. In this figure, I_{TG} = -5.43 pA, I_{BG} = 0 pA, I_D = -37 pA and I_S = 41.2 pA which indicates that current flows from source to both drain and top gate, because drain and top gate current have the same sign which is opposite to source current, and most of current flows from source to the drain. However, it is also possible that the current is flowing through ionic liquid but not channel. When we decrease the sweep rate, we can see a decrease in I_{DS}, as shown in Figure 34b, which also indicate that there might be a large contribution of ion conduction. Additionally, hysteresis is related to the sweep rate as well. Slower sweep corresponds to smaller hysteresis which

results from the fact that when we sweep slower, we give ions more time to reach equilibrium, as a result, ionic current contribution is smaller and the hysteresis becomes smaller. However, when we use different top gate voltage in output characteristics measurement, the curves overlap on each other, as shown in Figure 35, which indicates that top gate is not controlling the channel. A possible reason is mentioned above - the dimension of the channel is too large for our small top gate so that the EDL is not effectively formed.

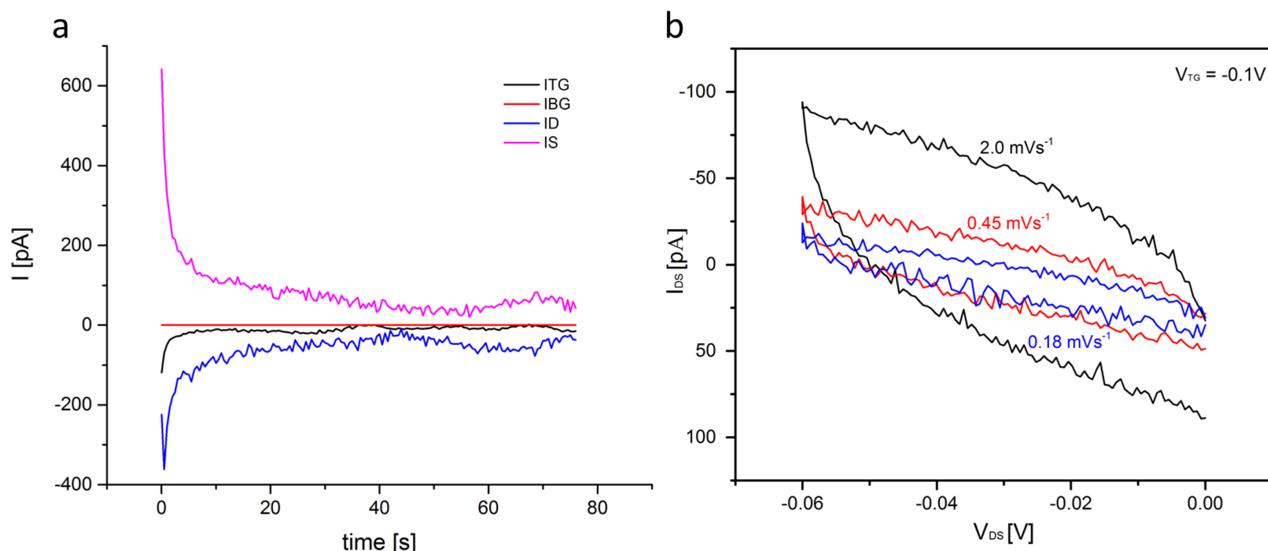

Figure 34: a) shows I/V-t sampling of IL gated OFET at V_{TG} = -0.2 V and V_{DS} = -60 mV in which I_{TG} = -5.43 pA, I_{BG} = 0 pA, I_D = -41.2 pA and I_S = 37.0 pA. This indicate most current flow from drain to source, however, this current might also flow through ionic liquid but not channel; b) output characteristics at V_{TG} = -0.1 V at sweep rate of 0.18 mVs^{-1}, 0.45 mVs^{-1} and 2 mVs^{-1} separately.

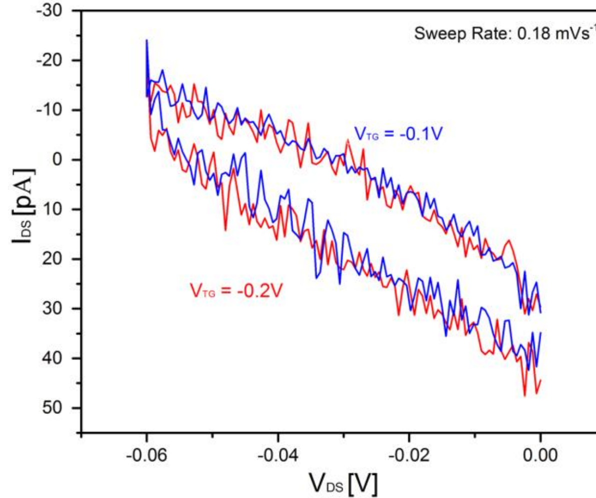

Figure 35: Output characteristics of TIPS-pentacene OFET gated with IL at V_{TG} = -0.1 V and V_{TG} = -0.2 V.

We tried two more modifications to address these issues: (1) we decrease the size of the source and drain to 100 × 100 μm with a channel length of 100 μm and channel width of 100 μm and at the same time added PEO to DEME-TFSI to decrease the mobility of ions to make the leakage current smaller. Although the leakage current became smaller in top gating, on the order of pA, I_{DS} also decreases to pA as well due to the shrinking of channel width. Therefore, our two approaches were not effective for this device.

For a future work, a more detailed study should be done to address the possible reaction between TIPS-pentacene and DEME-TFSI. If there actually is no reaction between them, then a possible way to electrolyte gating this organic semiconductor is to use smaller dimension of source, drain and channel and make sure the gate can cover the channel area for effective doping. If there is reaction, it will be important to identify an IL that does not react with TIPS-pentacene. Additionally, due to the large ionic conduction of this ionic liquid, PEO could be added into the electrolyte to decrease the leakage current, and to also make the electrolyte solid state, which

will eliminate the issue of leakage to the backgate due to the spreading of the liquid phase material.

6.0 CONCLUSION

The major focus of this thesis is on electrolyte gating. By formation of an EDL in the process of electrolyte gating, huge capacitance density, ~ 1 μF/cm^2,[19] could form resulting in the accumulation of carriers in the channel and heavy doping. We explored electrical performance with electrolyte gating on both a two dimensional (2D) material, graphene and an organic semiconductor, TIPS-pentacene.

For graphene, Hall measurements were performed to determine whether or not the valency of the ions affects the sheet carrier density because for a divalent ion, it can induce two carriers in the channel while monovalent ion can only induce one. We gated the GFET with a new solid polymer electrolyte containing a divalent cation, polyethylene oxide (PEO)/$Mg(ClO_4)_2$ and compared the results of sheet carrier density with the same GFET gated with PEO/$LiClO_4$, a monovalent cation. The highest sheet carrier densities of $7.3 \pm 4.9 \times 10^{13}$ cm^{-2} for holes and $3.8 \pm 1.5\times10^{13}$ cm^{-2} for electrons are obtained and both of them are an order of magnitude higher than that without electrolyte gating. Additionally, these values are comparable with those from Hall measurements on the same epitaxial graphene gated with PEO/$LiClO_4$ by our group. These results suggest that the valency of ions will not have large impact on sheet carrier density. Maximum hall mobility of $10.2 \pm 4.7 \times 10^4$ cm^{2}V^{-1}s^{-1} was achieved at V_{GS} = 0 V. However, the comparison is not completely direct for the two electrolytes. The first difference is that in PEO/$LiClO_4$ gated GFET, a top gate is employed and gate bias is continuous applied during the whole experiment at 298 K while for our PEO/$Mg(ClO_4)_2$ gated GFET, we used a side gate to

dope the channel at 343 K and after the temperature is decreased down to 220 K, when the ions are locked in place, we removed the gate bias and then perform the Hall measurement. Additionally, our devices were never exposed to ambient while PEO/$LiClO_4$ gated GFET was exposed to air during transferring. In addition, lager magnetic field, ± 1T, was used in our experiments compared with 0.24 T in their measurements. All these differences could contribute to a different result. Therefore, for future work, exactly the same device should be used, except electrolyte, to draw more solid conclusions.

For TIPS-pentacene FETs, we used an ionic liquid, DEME-TFSI, to top gate the devices. However, the results show no effective gate control because of the large ionic mobility of DEME-TFSI, relative to the conductivity of the channel, and it will cause large leakage current to the top gate. In addition, we found evidence of a possible reaction between DEME-TFSI and TIPS-pentacene, which could contribute to the ineffective electrolyte gating. This reaction is related to the dimension of the contact area of both IL and TIPS-pentacene on the electrodes or probes. With a larger contact area, the redox peaks will have higher intensity.

It is the first step in the community to study whether or not valency of ions in electrolyte will make a difference in electrolyte gated FETs. It is important because with one more charge induced in the channel, it can end up strongly affecting drain current. This work lays the foundation for a benchmarking effort in our lab for electrolytes.

For TIPS-pentacene OFET, this work shows how difficult it is to use electrolytes to gate semiconductors that are already with a pretty low channel current. Isolation of the IL on only the surface of the channel is often done in the literature to help with gating this kind of materials with electrolytes, so that the IL is not touching the source and drain pads or other devices nearby. However, it is not clear why, and it requires special processing steps.

APPENDIX A

SUPPLIMENTARY INFORMATION

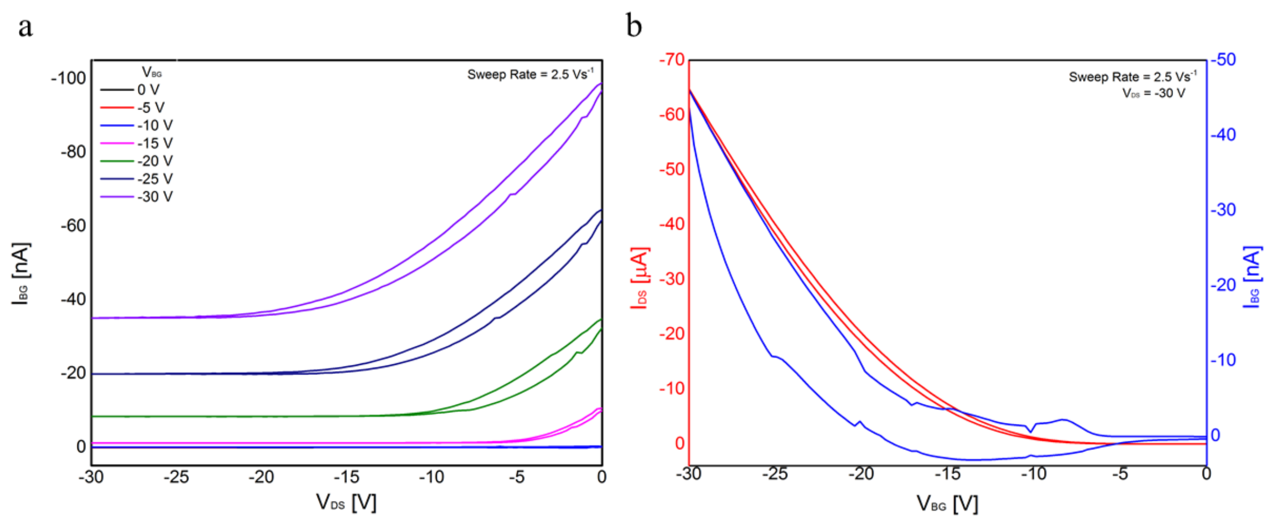

Figure S1: a) Leakage current of output characteristics of TIPS-pentacene OFET gated with 90 nm SiO_2 when V_{DS} = -30 V and V_{BG} = 0 V, -5 V, -10 V, -15 V, -20 V, -25 V and -30 V separately; b) double sweep of transfer characteristics in red and leakage current in blue of TIPS-pentacene OFET gated with SiO_2.

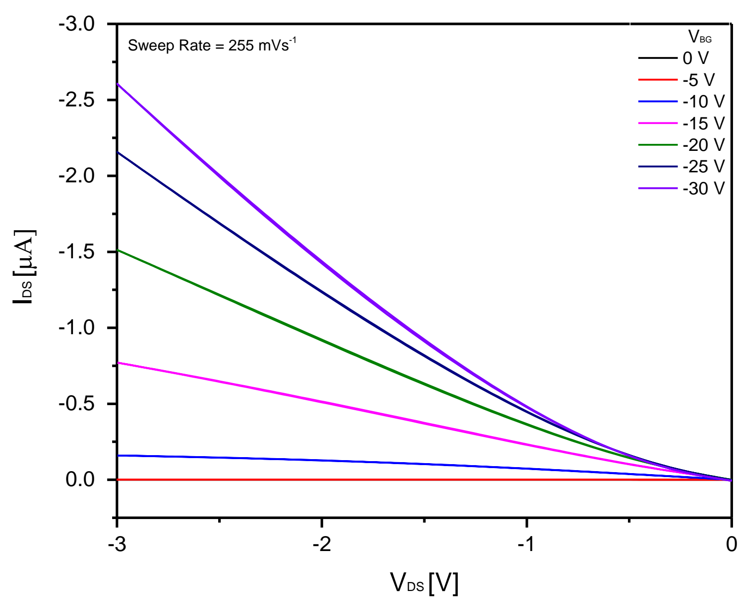

Figure S2: Output characteristics of back gated TIPS-pentacene OFET with V_{DS} = -3 V and V_{BG} = 0 V, -5 V, -10 V, -15 V, -20 V, -25 V and -30 V separately.

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