QUANTUM-DOT ORGANIC LIGHT-EMITTING DIODES ON SILICON SUBSTRATE

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University of Pittsburgh, 2017Utilization of quantum dots (QDs) as luminophores in organic light emitting diodes (OLEDs) has proven to be an effective way to produce a highly-efficient and cost-effective LED structure. Integrating a light emitting function on a silicon platform is expected to complement Si electronics advancing Si photonics. As an efficient means of driving electrons and holes into a QD layer of OLED structure formed on Si substrate, we have developed a novel injection method that exploits two-dimensional electron gas (2DEG) available at Si/SiO2 interface. By employing a stacked p-Si/SiO2//SiO2/n-Si structure having a cleaved edge on one side we demonstrated that Coulombic repulsion at the cleaved edge enables low-voltage emission of 2DEG. To utilize this low-voltage injection phenomenon, we fabricated OLED on an n-Si substrate using Si as a cathode and the inorganic quantum dots as a luminophore. In this device structure the junction area is defined by a lithographically patterned oxide layer on Si substrate and is designed to allow a wide range of scalability of lateral dimension down to a nanometer range. By varying the junction dimensions and geometry, the electron injection process is found to occur predominantly at junction periphery, not area, resulting in low turn-on voltage (~1-2V). Moreover, to utilize the ballistic injection of 2DEG through a void channel, we fabricated an OLED structure stacked on a 2D material (h-BN monolayer) suspended on a nano-hole-etched SiO2/Si substrate. The 2DEG injection produces one-dimensional emission of light along junction edges. This edge

injection/emission QD-OLED structure, when scaled down to a sub-10nm range, offers an interesting approach to developing single quantum-dot light sources for quantum information processing.

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PREFACE

This work would not have been possible without helpful guidance, generous support, and valuable suggestions from others. First and foremost, I would like to express my heartfelt appreciation to my advisor, Dr. Hong Koo Kim. It has been an honor and privilege to be his student. I am grateful to him for his guidance, encouragement, and inspiration throughout my doctoral program. Furthermore, I express a sincere gratitude to the members of my dissertation committee, Dr. William E. Stanchina, Dr. Dietrich W. Langer, Dr. Jung Kun Lee, Dr. Sangyeop Lee and Dr. El Nokali Mahmoud for giving me valuable comments and suggestions on my project. I am also grateful to my colleagues, Hai Ming and Yu Shi and former colleagues, Dr. Siyang Liu and Dr. Myungji Kim, for their support and help. I enjoyed sharing ideas and thoughts with them. Lastly, I would like to thank my parents, Hasan Ali and Ferdose Hasan, and my siblings Ratul and Sonia for their encouragement and support. They have provided great guidance in life and supported me in all my pursuits. And I would like to express my great appreciation to my fiancé, Quitterie Larrouture, for her support and patience during my doctoral period.

1.0 INTRODUCTION

There have been many ongoing efforts to develop optoelectronic devices that can be integrated with Si based microelectronic systems. Due to the materials' limitation, the LED devices are still lacking a strong bridge to silicon semiconductor technology. If a light emitting function of high efficiency were incorporated into a silicon platform, it would greatly complement the silicon electronics, advancing Si photonics for next generation optoelectronic devices. In this thesis, we develop an efficient LED structure on a silicon substrate by combining inorganic quantum dots as an emissive layer and organic semiconductors as carrier transport layers.

Conventional discrete light-emitting diodes (LEDs) utilize compound semiconductor materials, requiring expensive processes of preparation of materials such as high vacuum epitaxial growth. Also, lack of convenient fabrication processes is impeding the large-scale employment of conventional solid-state LEDs. There have been many attempts to find alternatives to semiconductor LEDs. Organic LED (OLED) proposed by Kodak in 1987, is one of the most extensively studied structures [1]. OLED utilizes organic polymers that transport holes or electrons from electrodes to an emissive layer, where they form bound pairs which can recombine and emit photons corresponding to the emission spectrum of the compound layers. OLED has the advantage of low power consumption, high brightness and relatively small required thickness (~200 nm), promoting its usability in many optoelectronic devices. Main bottlenecks of current OLED are heat-induced damage during operation and degradation from exposure to ambient air. To increase

the emission stability, quantum efficiency and better spectrum control, the OLED technology has incorporated quantum dot as the emissive layer. The inorganic quantum dots are uniquely suited as luminophores in light-emitting devices for their tunable luminescence properties, narrow emission spectrum, high quantum yield and solubility in various organic solvents [2]. In contrast to epitaxially-grown quantum dots, colloidal quantum dots can be deposited over large device areas by simple and inexpensive solution- deposition processes, such as spin-coating and roll-to-roll production.

In an effort to integrate OLED in monolithic Si circuit, Ashiwini et al. fabricated a colloidal quantum dot (QD) based LED that uses p-Si as the hole transport layer, and utilizes microcontact printing to pattern QD film [3]. To develop an optical transmitter to be integrated with a Si detector, Helen et al. fabricated OLED on a highly doped (n^{++}) Si substrate with a thin tunneling oxide buffer layer [4]. And lastly Baigent et al. fabricated OLED on Si by depositing an intermediate Al layer on Si to improve electron injection [5]. He explained that the native surface oxide of Si impedes electron injection from Si towards organic polymers or emissive materials. Most of the Si based OLED reported in literature uses Si substrate for the advantage of integrability to monolithic optoelectronic circuits. However, an effort to utilize the superior electronic properties and established fabrication technologies of Si into the OLED, is still lacking. In this report, we attempted to address this gap by fabricating micro/nano OLED on Si substrate.

The principle of OLED is driving the electrons and holes through n-type and p-type materials to confine them into an emissive material, following an exciton formation, which results in radiative recombination. However, the organic structures in OLED suffer from ambient moisture, oxidation, thermal and electrochemical degradation. Therefore, it is highly desirable to replace the organic polymers with inorganic semiconductors while maintaining the advantages of

OLED. To drive holes and electrons separately in a semiconductor platform, first, we designed a PIN diode with p-Si/SiO_2//SiO_2/n-Si structure. One would expect no carrier flow in this structure when the oxide thickness is greater than the tunneling limit (~20 nm) [6]. But, interestingly, we observed current flowing in this PIN structure when one of the Si edges is6 cleaved. This transport phenomenon can be explained by well-known 2DEG (2-dimensional electron gas) induced transport through a vertical void channel in MOS structure [7]. From the current-voltage characteristic, the forward characteristic is found to have a slope of 1.5, that is, a $V^{3/2}$ voltage dependence, suggesting the Child–Langmuir space-charge-limited (SCL) current flow in a vacuum. Since light-emitting devices need to be transparent at least on one side, we can't apply this structure directly in fabricating LED devices by just placing emissive material in between p- and n-Si. Therefore, we developed a method of fabricating OLED on an n-Si substrate using Si as a cathode as well as electron transport material. This generates some great advantages and interesting carrier injection mechanism in OLED operation.

In this report, we present a QD-based hybrid, top-emitting OLED on a silicon substrate. Our proposed LED takes an inverted structure (top p- and bottom n-layers) and replaces the traditional ITO coated glass substrate of OLED with n-Si. The effective junction area is defined by a lithographically-patterned oxide layer on Si substrate, allowing an opportunity to scale the LED dimension down to nanometer range. The oxide thickness is chosen to be an intermediate thickness of ~20 nm so that the tunneling leakage is suppressed, but the carriers can accumulate at the Si-oxide interface at a small forward bias. We observed an interesting carrier injection mechanism originating from the two-dimensional electron gas (2DEG) system at the interface between the oxide and the semiconductor. The Coulomb repulsion in 2DEG reduces the energy barrier between the cathode and the emissive layer, leading to a high current density injection

under a low bias voltage. To utilize the ballistic injection of 2DEG through a void channel, we fabricated an OLED structure stacked on a 2D material (h-BN monolayer) suspended on a nanohole-etched SiO_2/Si substrate. This injection mechanism allows one-dimensional emission of photons in the proposed LED structure, making the device less prone to thermal damage and environmental degradation. Moreover, as we approach nanoscale dimension in our proposed OLED, the perimeter-to-area ratio goes higher. This means almost all the injection will be with 2DEG at the edges, which is believed to be a more efficient process than the area injection. If we keep shrinking our device diameter, we expect to generate sub-10nm diameter OLEDs containing a single quantum dot. This can be used as a silicon-based, single-photon source on demand [8], which will be an important optical component in future quantum information technology.

2.0 CHAPTER 2: CURRENT CONDUCTION THROUGH MOS DEVICES

2.1 SILICON-OXIDE-SILICON (SOS) DEVICES

2.1.1 Introduction

The metal oxide semiconductor (MOS) capacitor is one of the significant building blocks of the modern semiconductor industry. The enabling nature of MOS capacitors, formation of a carrier channel (electron or hole) at Si/SiO_2 interface in proper voltage bias, is the working principle of numerous electronic devices (e.g. MOSFET). The charged carriers in MOS oxide/Si interface region, whether in accumulation or inversion bias, form a quasi-two-dimensional (2D) system that is confined in a narrow (~2 nm) potential well in silicon [9]. Like the Si side, the metal side of the oxide layer also harbors charges of opposite polarity in a confined space (< 1 nm) [10]. It is reported that coulomb repulsion in a two-dimensional electron system induced in the cathode (Al or Si) of MOS structure reduces barrier height at the edge, enabling threshold less emission of electrons (figure 2.1.1) [7]. For simplicity of labeling we will call this quasi 2D electron gas system as 2DEG throughout this report due to its nanoscale confinement across the oxide-Si interface plan of MOS.

Now, let's consider an SOS (semiconductor-insulator-semiconductor) structure which is similar to an MOS capacitor, except that the metal gate is now replaced with Si (figure 2.1.2). The

major effect of replacing metal with doped semiconductor would be the change in the amount of dopant energy levels that are filled with charge carriers. As a result, the device parameters, such as threshold voltage, energy band bending and the effective insulator thickness at different bias, would be changed. In this chapter, by employing a stacked p-Si/SiO2//SiO2/n-Si structure having a cleaved edge on one side we demonstrated that Coulombic repulsion at the cleaved edge enables low-voltage emission of 2DEG.

2.1.2 Device principle

To understand the carrier transport in semiconductor-oxide-semiconductor (SOS) structure, it is critical to understand the band diagram of the device at different bias voltages. Depending on the band bending nature of semiconductors, we can determine the density of accumulation or inversion charges at the interface. In our SOS device, n and p doped Si were placed across the SiO_2 insulator layer (figure 2.1.2 a). In this section, we have combined N-MOS and P-MOS device theories together and calculated the bias voltage response of SOS structure.

To form the SOS device we used n-Si and p-Si wafer with 20 Ohm-cm resistance, which gives an impurity concentration of $2x10^{14}$ cm^{-3} for phosphorus doped n-Si, and $5x10^{14}$ cm^{-3} for boron doped p-Si. For the sake of simplicity of calculation, let's assume both have the same impurity concentration of $5x10^{14}$ cm^{-3}. Therefore, the flat band voltage of stacked structure is:

$$V_{FB} = \frac{-1}{q}\,(E_{FN} - E_{FP}) \tag{2.1}$$

$$V_{FB} = -\frac{kT}{q}\left[ln\left(\frac{N_D}{n_i}\right) + ln\left(\frac{N_A}{n_i}\right)\right] \tag{2.2}$$

By replacing appropriate parameter values in equation 2.2, we get a flat band voltage of -0.56V. When a bias voltage is applied, band bending occurs both at n and p-Si side at the oxide interface (figure 2.1.2 d). The bias voltage (V_G) is distributed across three places: flat band voltage (V_{FB}), oxide voltage (V_{ox}) and surface potential (φ_s). Since the impurity concentration is equal, we can assume a similar nature of band bending for both n- and p-Si, resulting in an equal and opposite surface potential across the oxide layer ($\varphi_{sp} = \varphi_{sn}$). Therefore,

$$V_G = \varphi_{sp} + V_{FB} + V_{ox} + \varphi_{sn} \tag{2.3}$$

In accumulation bias, SOS capacitance is the oxide capacitance itself. Therefore, we can relate the space charge Q_s with V_{ox} and oxide capacitance C_{ox} by the following equation :

$$V_{ox} = \frac{C_{ox}}{Q_s} \tag{2.4}$$

The surface potential φ_s depends on the charge distribution and can be obtained as a function of distance by using Poisson equation:

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho(x)}{\varepsilon_r \varepsilon_o} \tag{2.5}$$

$$\frac{d^2\varphi}{dx^2} = -\frac{q(N_D - N_A + p_n - n_n)}{\varepsilon_r \varepsilon_o} \tag{2.6}$$

Where N_D and N_A are the ionized donor and acceptor densities.From charge neutrality condition at deep in the n-Si substrate, $N_D - N_A = n_{no} - p_{no}$. Here, n_{no} and p_{no} are equilibrium electrons and holes at flat band condition. However, the local charge densities(p_n or n_n) depends on local band bending of intrinsic energy band, and can be expressed as the following:

$$n_n(x) = n_{no} e^{\beta \varphi_n} \tag{2.7}$$

$$p_n(x) = p_{no} e^{-\beta \varphi_n} \tag{2.8}$$

Where. $1/\beta$ (=kT/q) is the thermoelectrical potential at temperature T. Replacing these terms in Poisson's equation [6] :

$$\frac{d^2\varphi_n(x)}{dx^2} = -\frac{q}{\varepsilon_s}\left[n_{no} - p_{no} + p_n - n_n\right] \tag{2.9}$$

$$\frac{d^2\varphi_n(x)}{dx^2} = -\frac{q}{\varepsilon_s}\left[p_{no}\left(e^{-\beta\varphi_n} - 1\right) - n_{no}\left(e^{\beta\varphi_n} - 1\right)\right] \tag{2.10}$$

Similarly, for p-Si side,

$$\frac{d^2\varphi_p(x)}{dx^2} = -\frac{q}{\varepsilon_s}\left[p_{po}\left(e^{-\beta\varphi_p} - 1\right) - n_{po}\left(e^{\beta\varphi_p} - 1\right)\right] \tag{2.11}$$

Integrating this equation from bulk Si, where potential φ and dφ/dx=0 to the surface with φ= φ_s and dφ/dx= -E_s, we can derive the surface electric field for n-Si side of SOS stack:

$$\int_0^{-E_{ns}} \frac{d\varphi_n}{dx} d\left(\frac{d\varphi_n}{dx}\right) = \int_0^{\varphi_{ns}} -\frac{q}{\varepsilon_s}\left[p_{no}\left(e^{-\beta\varphi_n} - 1\right) - n_{no}\left(e^{\beta\varphi_n} - 1\right)\right] d\varphi_n \tag{2.12}$$

$$E_{ns}^2 = \left(\frac{2kT}{q}\right)^2 \frac{qn_{no}\beta}{2\varepsilon_s}\left[\frac{p_{no}}{n_{no}}\left(e^{-\beta\varphi_{ns}} + \beta\varphi_{ns} - 1\right) + \left(e^{\beta\varphi_{ns}} - \beta\varphi_{ns} - 1\right)\right] \tag{2.13}$$

$$E_{ns} = \pm\frac{\sqrt{2}kT}{qL_{Dn}}\left[\frac{p_{no}}{n_{no}}\left(e^{-\beta\varphi_{ns}} + \beta\varphi_{ns} - 1\right) + \left(e^{\beta\varphi_{ns}} - \beta\varphi_{ns} - 1\right)\right]^{\frac{1}{2}} \tag{2.14}$$

Similarly, for p-Si, surface electric field is:

$$E_{ps} = \pm\frac{\sqrt{2}kT}{qL_{Dp}}\left[\left(e^{-\beta\varphi_{ps}} + \beta\varphi_{ps} - 1\right) + \frac{n_{po}}{p_{po}}\left(e^{\beta\varphi_{ps}} - \beta\varphi_{ps} - 1\right)\right]^{\frac{1}{2}} \tag{2.15}$$

Where, the Debye length L_{Dn}= $\sqrt{\frac{\varepsilon_s kT}{q^2 n_{no}}}$ and L_{Dp}= $\sqrt{\frac{\varepsilon_s kT}{q^2 p_{po}}}$, is the distance from the surface to the nearest neutral region in semiconductor.

We can derive the surface charge distribution using Gauss's law [6].

$$Q_{ns} = \varepsilon_s E_{ns} \tag{2.16}$$

The carrier concentration of n-type silicon can be approximated as, $n_{no}=N_D$ and $p_{no}=n_i^2/N_D$. In a similar way, for p-Si case $p_{po}=N_A$ and $n_{po}=n_i^2/N_A$. Considering Boltzmann statistics:

$$n_{no} = N_D = n_i exp\left(\frac{E_F - E_i}{k_B T}\right) = n_i exp\left(\frac{q\varphi_B}{k_B T}\right) \tag{2.17}$$

The hole density

$$P_{no} = \frac{n_i^2}{N_D} \tag{2.18}$$

Therefore,

$$\frac{p_{no}}{n_{no}} = \exp(-2\varphi_B\beta) \tag{2.19}$$

Which yields,

$$|Q_{ns}| = \frac{\sqrt{2}\varepsilon_s}{\beta L_{nD}}\left[\frac{p_{no}}{n_{no}}\left(e^{-\beta\varphi_{ns}} + \beta\varphi_{ns} - 1\right) + \left(e^{\beta\varphi_{ns}} - \beta\varphi_{ns} - 1\right)\right]^{\frac{1}{2}} \tag{2.20}$$

$$|Q_{ns}| = \frac{\sqrt{2}\varepsilon_s}{\beta L_{nD}}\left[\ exp(-2\varphi_{Bn}\beta)\left(e^{-\beta\varphi_{ns}} + \beta\varphi_{ns} - 1\right) + \left(e^{\beta\varphi_{ns}} - \beta\varphi_{ns} - 1\right)\right]^{\frac{1}{2}} \tag{2.21}$$

Figure 2.1.3-a&b shows the surface charge density in n- and p-Si sides of SOS structure with variation of surface potential. Due to the equal doping density in n- and p-Si, their surface charge vs surface potential plots are mirror image of each other. In the accumulation bias, $\varphi_{ns} > 0$ and

the charge Q_{ns} becomes closely proportional to $e^{\frac{\beta\varphi_{ns}}{2}}$[11]. At depletion bias: $0>\varphi_{ns}> -2\varphi_{Bn}$ yields,

$$Q_{ns} \propto \sqrt{-\beta\varphi_{ns}} \tag{2.22}$$

Lastly, at inversion bias where $\varphi_{ns}< -2\varphi_{Bn}$

$$Q_{ns} \propto e^{-\frac{\beta\varphi_{ns}}{2}} \tag{2.23}$$

The electric field inside oxide layer of SOS structure can be expressed as:

$$E_{ox} = \frac{V_{ox}}{t_{ox}} \tag{2.24}$$

$$E_{ox} = \frac{V_G - V_{FB} - 2\varphi_s}{t_{ox}} \tag{2.25}$$

From Gauss's law,

$$E_{ox} = \frac{\varepsilon_s E_s}{\varepsilon_{ox}} \tag{2.26}$$

$$\frac{V_G - V_{FB} - 2\varphi_{ns}}{t_{ox}} = \frac{\sqrt{2}\varepsilon_s}{\varepsilon_{ox}\beta L_D}\left[\, exp(-2\varphi_{Bn}\beta)\left(e^{-\beta\varphi_{ns}} + \beta\varphi_{ns} - 1\right) + \left(e^{\beta\varphi_{ns}} - \beta\varphi_{ns} - 1\right)\right]^{\frac{1}{2}} \tag{2.27}$$

The above equation relates the surface potential to the applied gate voltage. We can get the surface charge as a function of gate voltage by solving equation (2.21) and (2.27). Figure 2.1.4-a shows the charge density at the oxide interface of n-Si of SOS device with variation of bias voltage. Here, we varied semiconductor doping density with a fixed oxide thickness of 20 nm and confirmed that the dopant density only affects the flat band voltage and has little effect on charge density at a

given voltage. On the other hand, figure 2.1.4-b shows the same plot with fixed doping density but variable oxide thickness. We observe that, the surface charge density at a given bias voltage is much higher for an SOS with thinner oxide (e.g. 10 nm) compared to one with thicker oxide (e.g. 40 nm). Later in this chapter, we show that electron injection from a quasi 2D electron gas can occur from cleaved SOS device at accumulation bias. Knowing the surface charge at any specific bias would be helpful to model and predict the injection current. Figure 2.1.2 shows a schematic diagram of band profiles in an SOS structure. Figure 2.1.2 (a) shows the device structure of proposed SOS capacitor. 2.1.2(b) shows the equilibrium band structure of two oppositely doped semiconductors linked with an insulating oxide. Figure 2.1.2 (c) shows the flat band voltage creating a charge-free structure while (d) shows the SOS band structure during accumulation bias. We limited our analysis only at accumulation bias in this work considering its probable application in developing semiconductor light-emitting devices. In Srisonphan et al.'s work [7], it is shown theoretically that for Gr/SiO_2(23nm)/n-Si structure, the accumulation carrier density is ~10^{12} cm^{-2} at ~1V. In our structure, the contribution of gate voltage towards surface potential would be devided in half due to band bending at both gate and substrate side. Therefore we can assume the accumulation electron density to be 0.5 x 10^{12} cm^{-2} on both n and p-Si side of oxide interface. Now, if we create a discontinuity by cutting an edge (i.e. trenches, holes, cleaved edges etc.) along the interface, as shown in figure 2.1.1 (a) for an MOS structure, the 2D layer serves as a charge reservoir that would release electrons through the edge under appropriate bias. To understand carrier injection through cleaved SOS capacitor, a review of well-known quasi 2DEG emission in MOS structure would be useful.

In MOS capacitor 74% of total accumulation electrons in the semiconductor side is balanced by adjacent polarization charges induced at Si/SiO_2 interface corresponding to the

permittivity ratio $\varepsilon_o/\varepsilon_{SiO2}$. Therefore, the other 26% of accumulation electrons are balanced by induced charges across the oxide layer. It is well known that the SiO_2/Si interface can accumulate a high concentration of 2D electron gas at proper bias, e.g., 10^{12} cm^{-2} at ~1V forward bias. To find the spacing between this 'net effective' charges we can apply Wigner-Seitz formulae for 2D system:

$$\pi r^2 = \frac{A}{N} = \frac{1}{n} \tag{2.28}$$

$$r = \sqrt{\frac{1}{\pi n}} \tag{2.29}$$

$D = 2(\pi n)^{-\frac{1}{2}}$ = 2*(3.14*0.26*10^{12})$^{-1/2}$ cm = 11.06 nm

From the above equation, the spacing between adjacent charges is ~10 nm which is smaller than the vertical space gap of 20 nm, defined by the oxide thickness. At this density level the average spacing between electrons in the 2DEG is estimated to be ~10 nm, smaller than the oxide thickness (23nm). This close spacing will ensure that the in-plane interaction of 2DEG electrons becomes stronger than the dipole charge interaction across the oxide layer. Due to this Coulombic repulsion at the edge, the energy barrier for electron emission into outside is lowered (figure 2.1.1 b), enabling electron emission at relatively low bias voltage [12]. In the case of an MOS with a void-well channel, the emitted electrons travel ballistically through the void channel. To get ballistic transport through air, the channel length (i.e., the thickness of oxide layer) is designed to be ~20nm, much smaller than electron mean-free path in air (60 nm). It also has been stated that the channel current is proportional to the perimeter of the well, indicative of edge injection/emission of 2DEG [13]. The current is reported to follow well-known one-dimensional (1D) Child-Langmuir (CL) law for unipolar space-charge-limited current [14, 15].

2.1.3 Experiment, result and discussion

In order to observe 2D electron and hole system effect on proposed SOS structure, we stacked p-Si/SiO_2 on top of SiO_2/n-Si device such that the top device is cleaved, enabling edge transport towards the bottom device (figure 2.1.5). As substrate, we chose wafers of n-Si <100> (phosphorous doped with a resistivity of 20 Ohm.cm) and p-Si<100> (boron doped with resistivity 10 Ohm.cm). To remove the organic contaminants and grease, the wafer was first cleaned with acetone and then with methanol in an ultrasonic bath for 10 minutes each. The wafer was then rinsed with DI water and went through the RCA cleaning process flow for native oxide removal and contamination cleaning. Then the wafer was placed in the oxidation furnace (Thermco.MB-71), which was set to 950^oC (for thick oxide) or 832^0C (for thin oxide). According to previous oxidation calibration performed in this furnace, to grow 20 and 40 nm thermal oxide we placed the sample at 950^oC in air ambience for 20 and 90 minutes respectively. Thickness was confirmed by Alpha step profiler. To grow 1 nm and 2 nm oxide, the wafer was placed at 832^0 C for 30s and 1 min respectively. The thickness of the thin oxide layer was confirmed by an ellipsometer. After oxidation of silicon substrate, to make an Ohmic contact, 150-nm-thick Al (Alfa Aesar,5N purity) was deposited by thermal evaporation process at a vacuum of ~10^{-5} Torr. Before Al deposition, the thermal oxide on the back was removed by etching with 6:1 BHF, while protecting the front oxide layer with photoresist.

To observe transport mechanism in stacked SOS device, experimentally, we stacked p-Si/SiO_2(23 nm) on top of SiO_2/n-Si (figure 2.1.5). Before stacking, we passivated n-Si surface with 1-2 nm thin thermal oxide. The thin oxide layer reduces surface dangling bonds and other non-ideal leakage sources, while field-induced charges can easily pass through tunneling mechanism. In order to create edge emission, we cleaved the p-Si/SiO_2 wafer into 1 mm square pieces and

placed it on top of thin oxide/n-Si substrate such that the oxide layer is sandwiched between p and n-Si. When a forward bias is applied to the stacked device, accumulated holes and electrons are expected to form 2D charged channels across oxide layer in p and n-Si respectively. In the effective device area of n-Si/SiO_2, Coulomb force among adjacent electrons in 2D electron system pushes out the electrons into the air through the thin tunneling oxide. In the presence of an electric field, these free electrons travel towards the 2D hole system in p-Si. Since the mean-free path of an electron in the air is ~60nm, which is greater than the oxide thickness of p-Si, the electron flows ballistically through air.

In figure 2.1.6 the experimental measurement data of I-V characteristics in stacked SOS structure is shown. In the I-V curve of 2.1.6(a), p-Si/SiO_2(1 nm) is stacked on SiO_2(2nm)/n-Si, which gives an SOS capacitor structure with 3 nm of oxide insulator in between. In the reverse bias regime, the slope is 1, indicating Ohmic nature of conduction. In the forward bias, at very low voltage the slope is ~1.4, where at higher voltage it grows to 2. This indicates two different transport mechanisms depending on the applied field. From the energy band characteristics discussed in the previous section, we need to apply a bias of 0.56 V for achieving flat band state in our structure. The I-V slope becomes steeper once flat band voltage is reached and accumulation starts. Due to thin oxide interlayer thickness, the carrier transport occurs predominantly by direct tunneling. In figure 2.1.6 (b) the SOS device consisting of a cleaved p-Si with 23 nm oxide on a planar n-Si with tunneling oxide (2 nm) is shown. Quite interestingly, the slope at a lower voltage is 1.5 while at higher voltage it increases to 2. Figure 2.1.6 (c) and (d), shows the similar I-V graphs for top p-Si with 40 and 265 nm oxide, which also shows slope 1.5 at lower voltage and slope between 2 to 3 at a higher voltage. As mentioned earlier in this thesis, $V^{3/2}$ dependence corresponds to collision less ballistic transport of space charge limited current through vacuum. Where the V^2

law corresponds to the Mott-Gurney's space-charge-limited current where charge carriers experience collision during transport process through a trap free insulator [16]. The rapidly-rising current at higher bias voltage corresponds to the Fowler-Nordheim (FN) tunneling of electrons from cathode [17]. Figure 2.1.6 (e) shows I-V characteristics for similar device structure as figure (b), except that now p-Si with 23 nm oxide is placed on a thinner tunneling oxide (1 nm)/ n-Si. The log I-log V slope shows similar phenomena with initial $V^{3/2}$ dependence and later V^2 dependence. Although, this time due to higher tunneling probability through thinner 1 nm tunneling oxide, the forward current is about three times higher than 2 nm oxide case. The last figure, (2.1.6(f)) shows the I-V result of an exploratory structure, where n-Si with thin 1nm oxide were stacked on each other. Interestingly, in both forward and inversion regime the log I-log V slope is found to be Ohmic (unit value). This can be explained by the fact that, through a very thin oxide barrier, the electron transport is instantaneous without much barrier. Therefore, the current is proportional to the drift velocity of carriers inside bulk Si, which is proportional to the applied voltage. Lastly, I-V curve shown in figure 2.1.7 compares the log I-log V curves for 3 different combinations of SOS structure. For the case of SOS device with cleaved p-Si/SiO_2(23 nm) on planar SiO_2(23)/n-Si structure, the log I-log V slope is found to be 3, which corresponds to bipolar charges (electrons and holes) injected through a void channel [18]. The other two sample configurations have already been discussed in figure 2.1.6.

2.1.4 Conclusion

In summary, in this section we showed that at low voltage region the 2D electron gas can be injected from the cathode (n-Si) to air through a thin oxide layer (~2nm) and then travel ballistically along the edges of a thick insulator (cleaved SiO_2/p-Si) towards the direction of an

electric field. We also observed that if very high electric field is applied across the insulator, FN tunneling current becomes dominant over 2DEG injection current. Similarly, if there is only a thin oxide between anode and cathode, the 2DEG injection becomes negligible compared to the direct tunneling current. However, the 2DEG injection through a thin oxide confirms that the surface oxidation of bare Si is not a limiting factor of 2DEG injection through nanovoid channels of MOS devices.

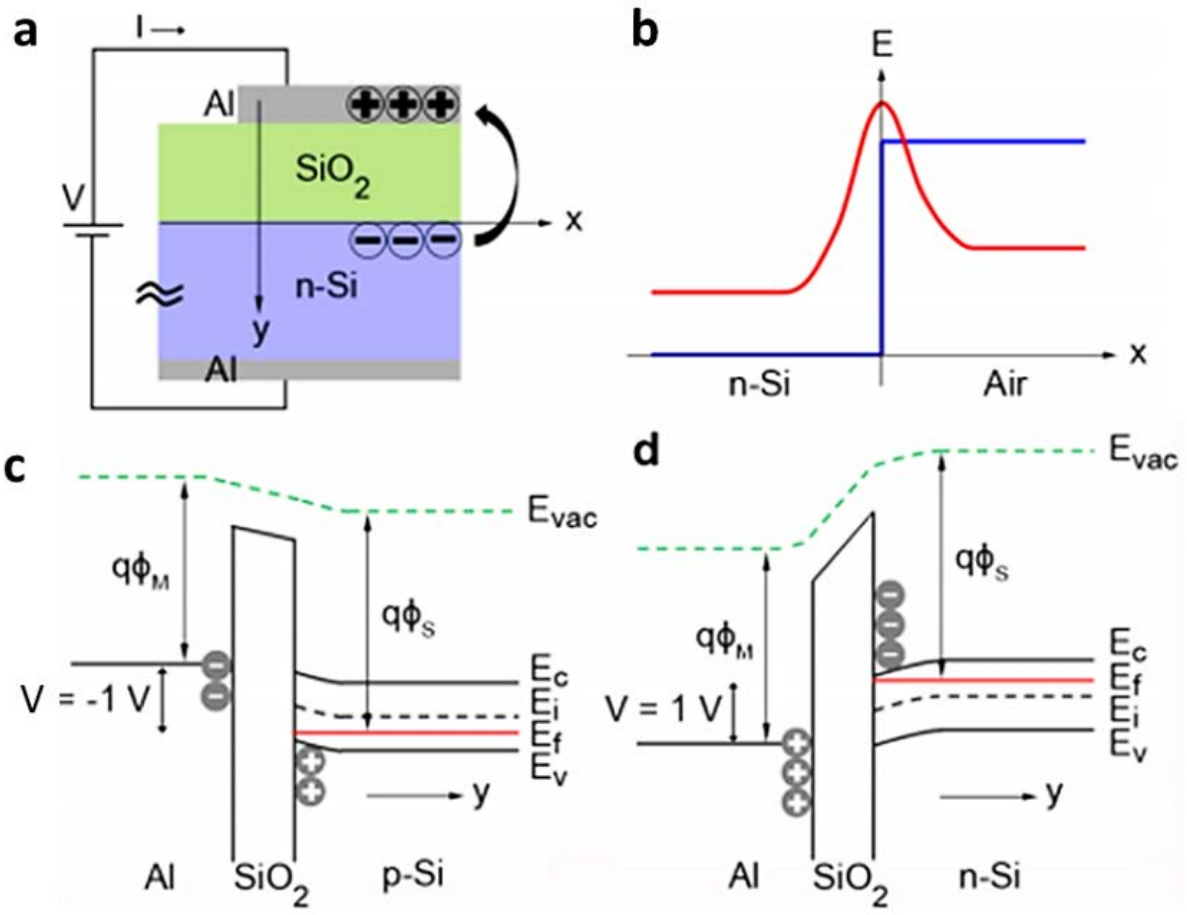

Figure 2.1.1: Energy band diagram of nano void channel in MOS structure at forward bias. (a) 2DEG formation at oxide interface, (b) Schematic illustration of electron potential (red) and air energy barrier on the plane of 2D electron layer, (c) energy band diagram of p-Si MOS and (d) energy band diagram for n-Si MOS at 1 V forward bias [13].

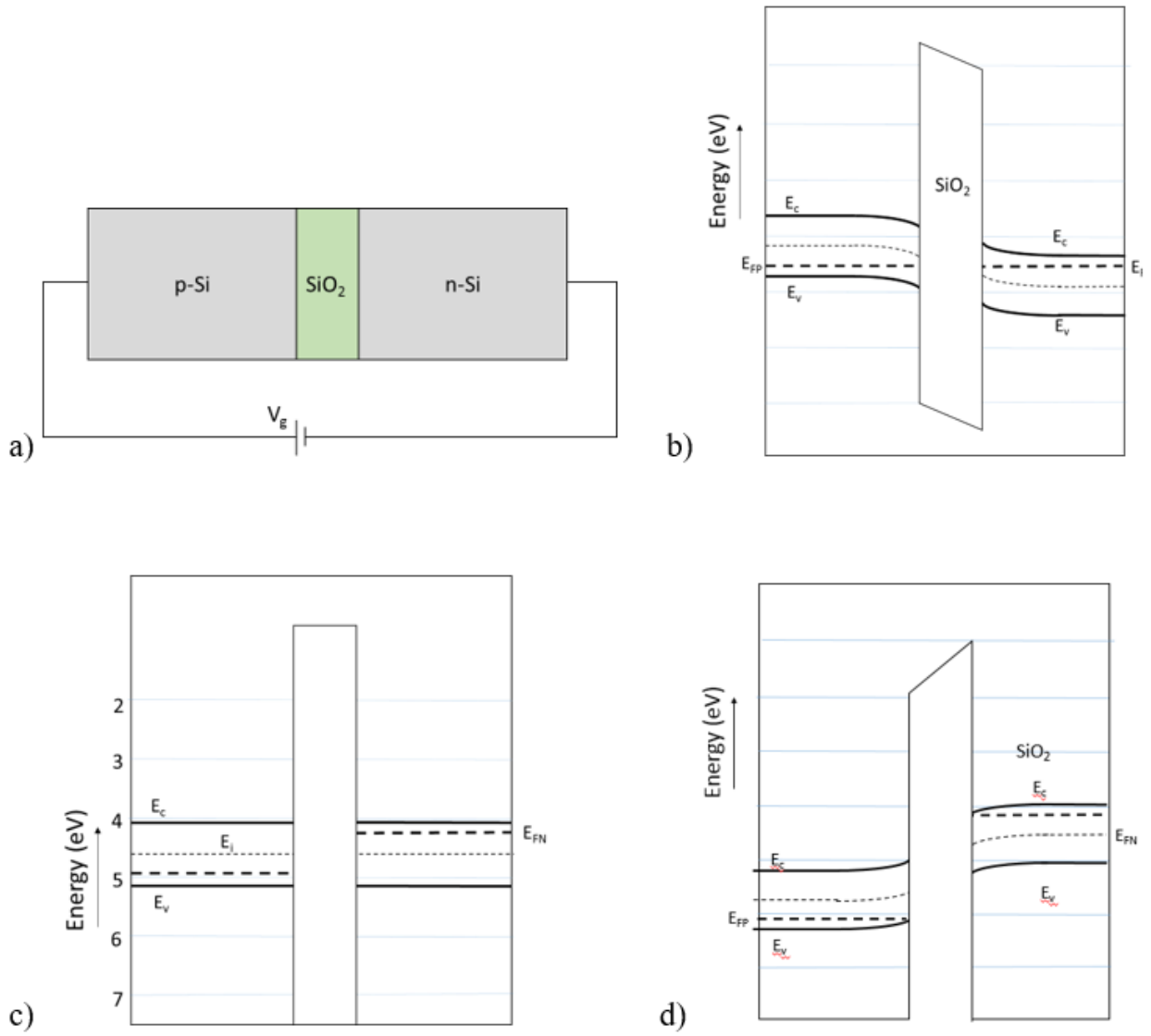

Figure 2.1.2: (a) n-Si/SiO2/p-Si structure, b) +Energy band diagram in thermal equilibrium at zero gate voltage, c) band diagram at flat band voltage, and d) band diagram at accumulation.

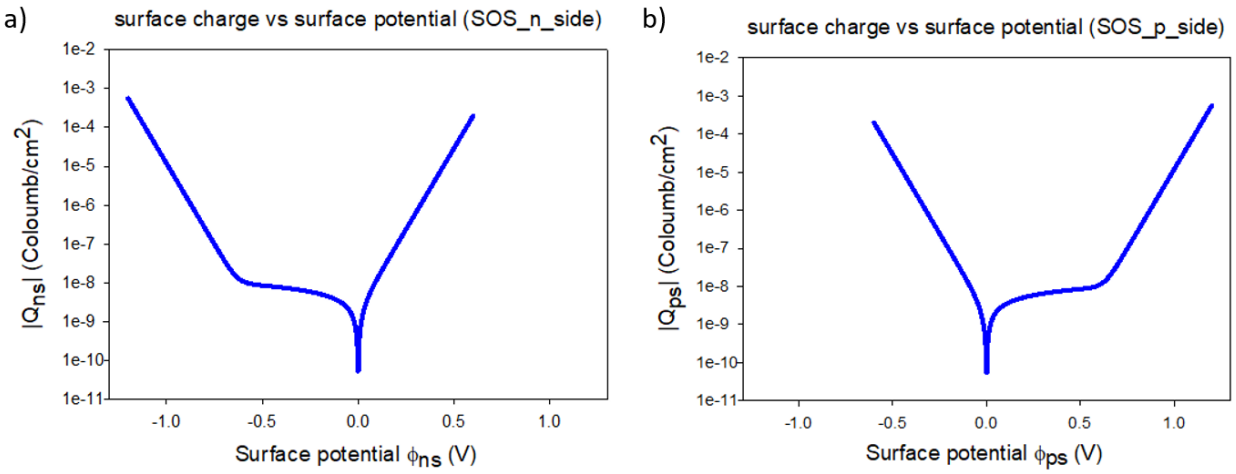

Figure 2.1.3: Charge density vs surface potential of two semiconductor sides of an SOS structure: a) n-Si side and b) p-Si side

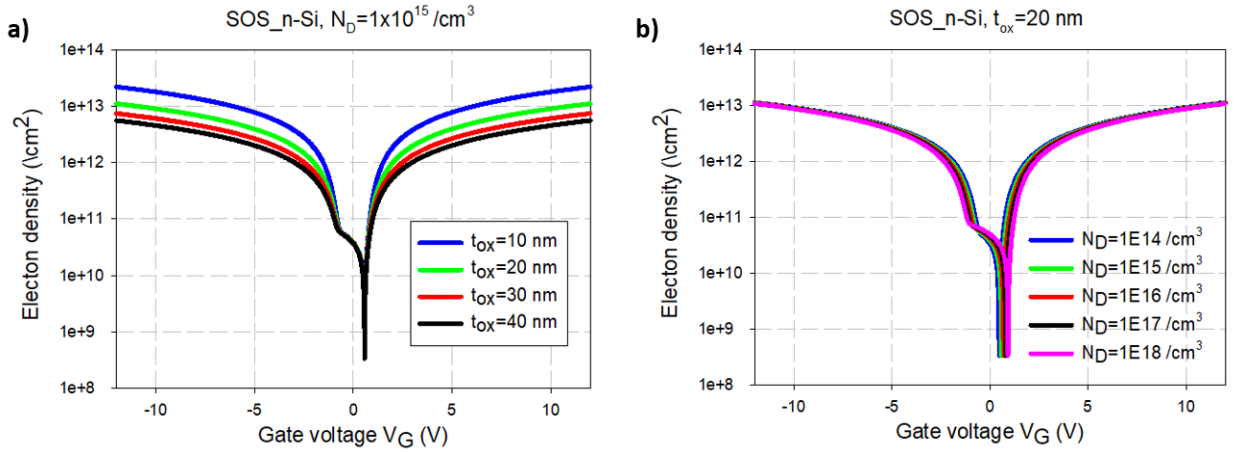

Figure 2.1.4: Charge density vs bias voltage in the n-side of proposed SOS structure: a) effect of changing oxide thickness and b) effect of changing doping density. In both cases n- and p-Si doping is equal (N_D=N_A).

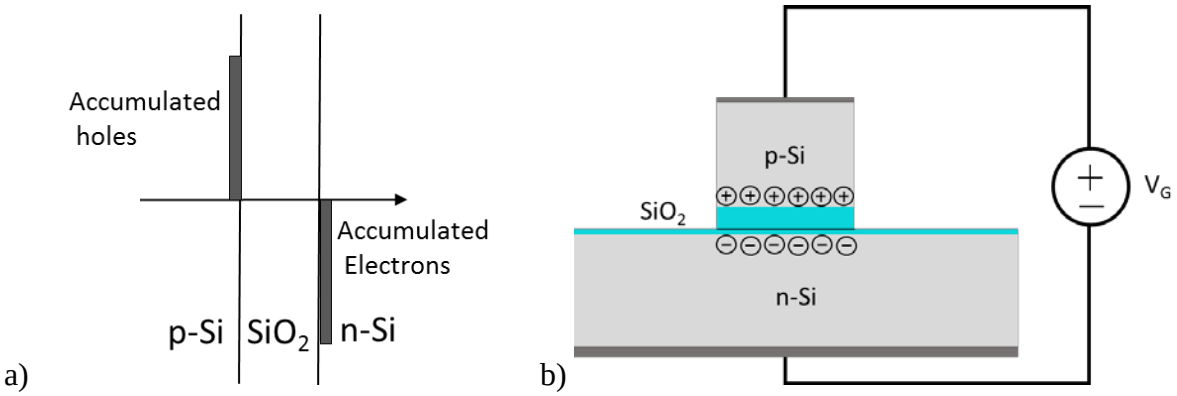

Figure 2.1.5: a) accumulation charge formation in forward bias, and b) 2DEG injection mechanism in stacked SOS structure.

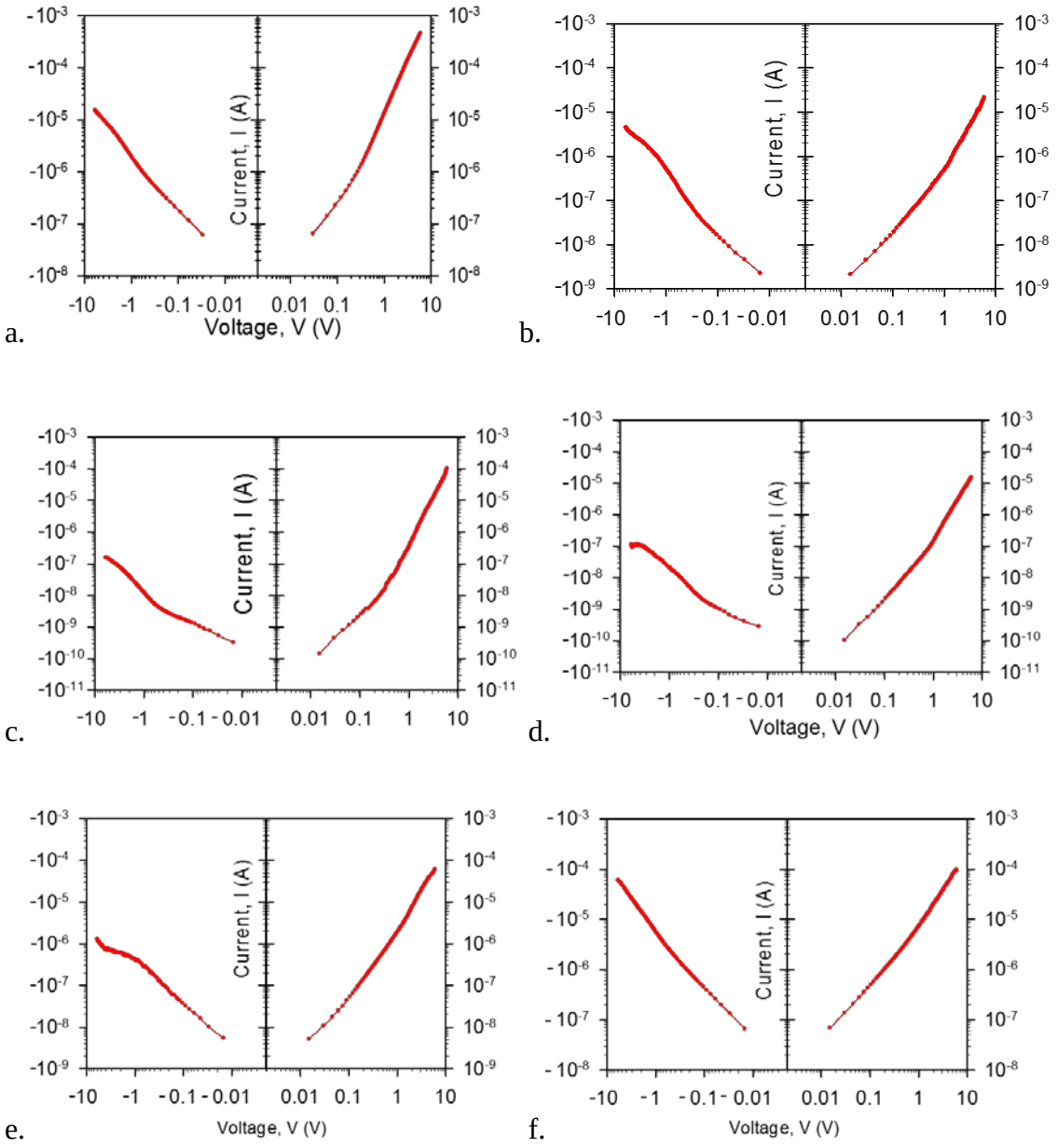

Figure 2.1.6: a) p-Si/SiO2(1 nm) on SiO2(2 nm)/n-Si, b) p-Si/SiO2(23 nm) on SiO2(2 nm)/n-Si, c) p-Si/SiO2(40 nm) on SiO2(2 nm)/n-Si, d) p-Si/SiO2(265 nm) on SiO2(2 nm)/n-Si, e) p-Si/SiO2(23 nm) on SiO2(1 nm)/n-Si and f) n-Si/SiO2(1 nm) on SiO2(1 nm)/n-Si.

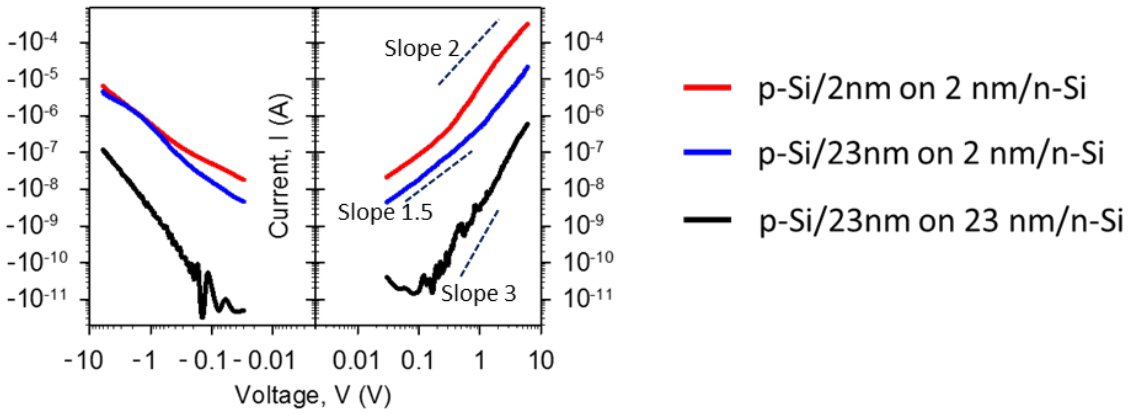

Figure 2.1.7: A Comparison of I-V characteristics of stacked SOS structure with various thickness of oxide insulators.

2.2 VACUUM EFFECT ON VERTICAL CHANNEL TRANSPORT IN MOS EDGE

2.2.1 Introduction

In previous sections, field-driven transport of electrons has been observed at proper biasing condition through a vertical void channel that creates a discontinuity at 2D charge system in SOS (semiconductor oxide semiconductor) capacitor structure. If the physical path traveled by the electron is smaller than its mean-free path in air, we can assume a collisionless ballistic transport as if the transport is occurring in a vacuum. We indeed confirmed this hypothesis with the $V^{3/2}$ dependence of current. Now, let's consider introducing a vertical travel path of ~2µm which is much greater than the electron mean free path limit in air. Even at this channel length, if appropriate bias is applied, we expect to see small current flow through the air, which is continuously impeded by collision and scattering. Therefore, if we perform this experiment in a vacuum chamber, gradually pumping out the air, we should see a proportional increase in current

flow. Since we are performing this experiment at a very high voltage of 1-40V bias, we also need to consider other nonideal means of carrier transport through oxide such as F-N tunneling, Poole–Frenkel effect etc.

2.2.2 Result

Figure 2.2.1 shows the I-V characteristics of our proposed SOS structure in various vacuum pressure levels. On the left side, we present log I – log V graph, while on the right side we show $\ln(I/V^2)$-$\ln(1/V)$ graph. The later graph, if shows linear relation, indicates F-N tunneling mechanism for electron transport. The I-V characteristics of the SOS was measured at 0.25 mTorr. At this vacuum level, the electron mean-free path is much larger (>1 mm) than the device space gap (2.2 μm). That means even at a very small pressure drop, the electron mean-free path exceeds the space gap limit, and therefore 2DEG emitted current wouldn't increase even though we reduce pressure further. The small increment of current we saw when pressure goes down from 0.25 mTorr to $4.5x10^{-5}$ Torr appears to be caused by gas molecules (air molecules including water/moisture) adsorption/desorption process [19]. In vacuum, high voltage electron bombardment might desorb gas molecules on the anode surface, which results in decreasing the work function, hence better/more collection of incoming electrons (therefore current). This electron-stimulated desorption effect would be stronger at a higher voltage (40V, 2.2μm case), as observed with the 2.2um sample. In the 2.2um sample case, electrons gain large kinetic energy from the applied voltage (up to 40V). These kinetic electrons bombard the anode surface desorbing adsorbed molecules (therefore increasing the current level). The I-V at higher voltage (>3V or >6V: slope, much steeper than $V^{1.5}$ or V^2) may suggest that the overall current flow is governed by Fowler-Nordheim tunnel emission/admission, not by space charge limited. Indeed, the $\ln(I/V^2)$

vs ln(1/V) shows a linear trend at high voltage level (>10 V), which is a strong indicator of F-N tunneling mechanism. The measurement voltage limit of 40V is determined by the voltage range of I-V measurement instrument.

2.2.3 Conclusion

In this experiment, we observed the effect of ambient pressure in 2DEG injection and transport through a microscale long void channel in a cleaved SOS structure. We measured I-V characteristics in three different pressures: air ambience, medium vacuum and high vacuum. At the medium vacuum, the electron can ballistically travel through micron long void, therefore, the current increases by ~5 times compared to air ambience. Interestingly, we observed further increase of current by reducing the pressure to high vacuum resulting in desorption of gas molecules at the corresponding device structure. The most important conclusion of this experiment is that 2DEG injected current in MOS structure can travel scattering free for a long distance through void channels, where electron mean free path is dramatically increased by reducing the ambient pressure. This finding renders an opportunity to explore the use of MOS 2DEG injection in e-beam based tools, such as SEM, TEM, and EBL.

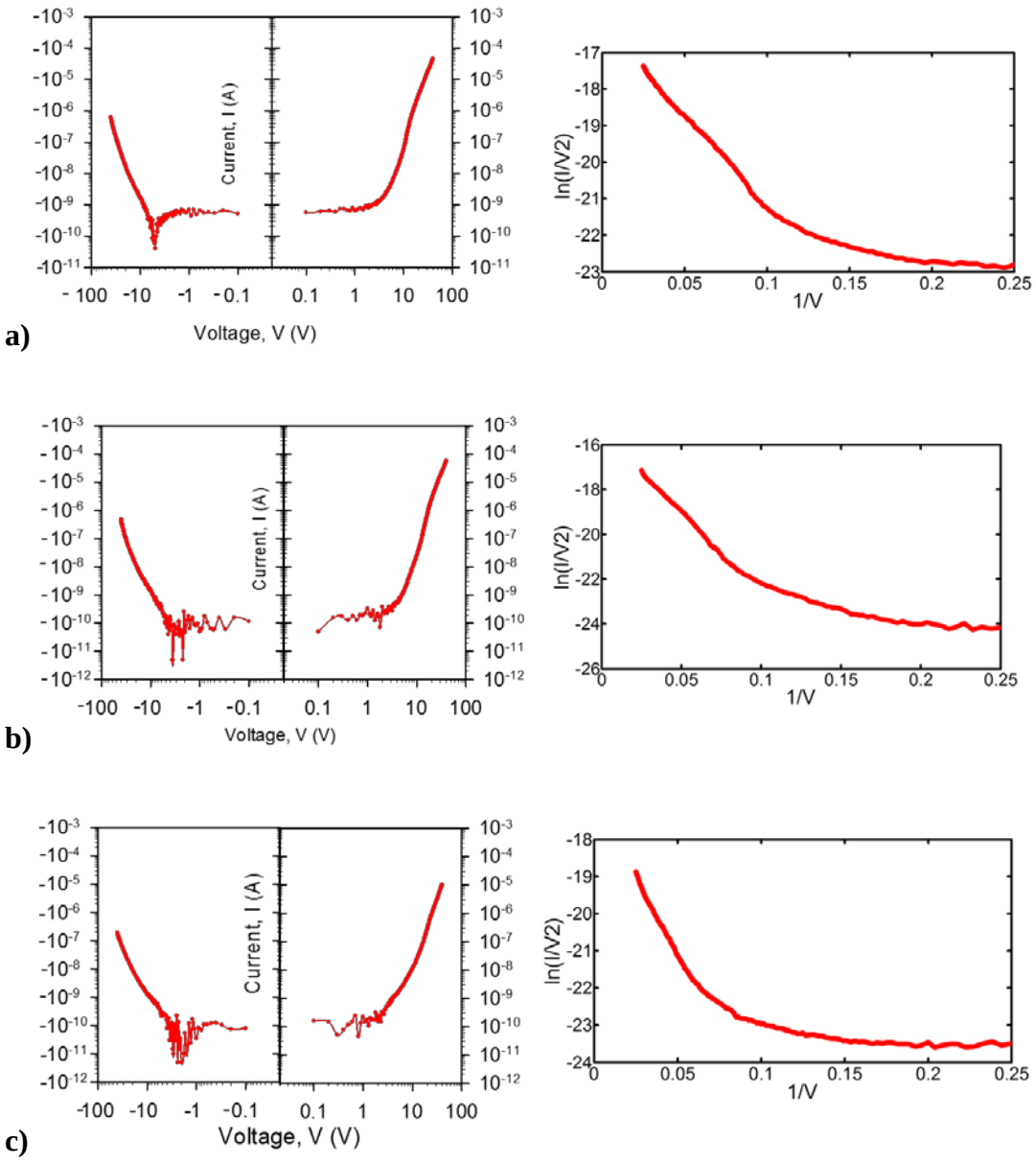

Figure 2.2.1: I-V characteristics of the stack of 2.2um p-Si(1x1mm) on 2nm n-Si(1x1cm) at the chamber pressure of a) at 0.25 mTorr, b) at 4.5x10*-5 Torr, and c) at air ambient after venting vacuum chamber.

2.3 STACKED SOS WITH GRAPHENE INTERLAYER

2.3.1 Introduction

It is well known that a quasi-two-dimensional electron gas (2DEG) induced at the oxide-semiconductor interface of a metal-oxide-semiconductor (MOS) structure can be easily emitted into the air (void channel) at low voltage (~ 1 V) [7]. If the metal electrode of MOS is replaced with a graphene sheet, we get a graphene-oxide-semiconductor (GOS structure). In GOS structure, if graphene is suspended on a void channel, interesting phenomena such as charge neutralization and double injection of charge carriers can be observed due to in- and out-of-plane interactions of 2D electron system [13]. In the previous section, we have discussed a proposed semiconductor-oxide-semiconductor structure where a cleaved p-Si/SiO_2 was placed on a broad n-Si with very thin oxide on top to observe the edge emission of 2D charge system from the anode (p-Si) through a space gap which is equivalent to its oxide thickness. The thin tunneling oxide on the cathode (n-Si) was chosen to facilitate the transmission of any charges that reach from anode side. In this section, we built the Semiconductor-graphene-oxide-semiconductor(SGOS) structure by stacking a cleaved p-Si/SiO_2 on top of Graphene sheet covering the n-SI/SiO_2 with void channels.

2.3.2 Fabrication

The graphene/SiO_2/Si structure with a void channel was fabricated by using electron-beam lithography (EBL) and reactive-ion etching (RIE) process. After conventional RCA cleaning process, an n-type silicon (phosphorous-doped, resistivity 5 Ω-cm) wafer ((100)-oriented; thickness, 525 μm) was placed in an oxidation furnace at 950^o C to grow 23 nm thick oxide. An

Al Ohmic contact was prepared on the back of Si substrate by thermal evaporation (Al thickness, 150 nm), followed by annealing at 350^{o} C in a nitrogen ambient. By using e-beam lithography, a narrow stripe pattern (400-nm-width, 1-mm-length trench) was defined in the polymethylmethacrylate (PMMA, ~200nm thickness) layer using electron-beam lithography (Raith e-Line: 10keV, beam current 220pA). After developing PMMA pattern, the e-beam patterned substrate was etched to 210 nm depth by RIE process in CF_4/O_2 ambient. The PMMA was then removed by acetone. The sample is now ready to transfer a monolayer graphene on top. CVD grown graphene on Cu foil was purchased from Graphene Supermarket Inc. and was transferred to the oxide substrate following a wet transfer process [20]. In order to remove moisture trapped in the etched trench, the sample was dried at 70^{o} C for 2 hours. These samples reveal graphene membranes suspending flat on trench-patterned substrate and showing 2D charge injection phenomena through void channel at proper bias [12].

2.3.3 Result and Discussion

Srisonphan et al. reported electron transparency and hole charge induction response of a GOS (graphene oxide semiconductor) structure where a suspended graphene anode is placed on top of a void channel formed in a SiO_2/n-Si substrate [13]. They reported that under forward bias a quasi-2D electron channel is formed in the Si while a 2D hole system is developed in Graphene (figure 2.3.1), resulting in a strong 2DEG injection flow at the trench edge. The I-V characteristics show a V^3 dependence of current, a phenomenon known as double injection or injected plasma [18]. Furthermore, to block electrons bypassing through Gr, a Ga droplet was placed on top of graphene that enhanced current flow through the device. The I-V characteristic slope remains the same as graphene only structure, indicating similar carrier injection mechanism.

In this section, we explored an interesting structure by adding a cleaved p-Si/ SiO_2 piece (1 mm^2 area) on top of a GOS structure (graphene oxide semiconductor) with an EBL trench of 200nm width, 200 nm depth and 1 mm length (figure 2.3.2 a). The I-V characteristics for two different devices are shown in figure (c). In both devices, cathode is Gr/SiO_2(23 nm)/n-Si structure where Gr covers an EBL trench, while in one device anode p-Si has 23 nm insulating oxide, in the other device it has 1 nm oxide. In accumulation bias both anode (p-Si) and cathode (n-Si) develop 2D carrier channels at corresponding oxide interfaces. Due to coloumbic repulsion of electrons around the trench edge, the 2 DEG in n-Si cathode emits into air and travels up towards the graphene/SiO_2 interface. Covering the trench top suspended Gr with insulating oxide (p-Si anode) ensures that all the incident electrons would be blocked and collected by Graphene. In response to electron injection, graphene anode supplies hole charges that neutralize electrons and reduces the space charge field. In the I-V graph shown in figure 2.3.2-c at low forward bias the current follows $V^{1.5}$ law which means conduction is limited by Child-Langmuir's ballistic transport. However, at higher voltage range the cathode emission is governed by availability of hole charges on graphene, which has quadratic proportionality to the electric field ($n \propto E_F^2$) [21]. Here, the electric field across Gr depends on the oxide voltage drop at both sides of graphene($V_{ox} \sim V_G$). However, due to absence of interface, the electric field at nano void channel is determined by the charge states of graphene that covers it ($E_{channel} \propto n_{gr} \propto V_G^2$). The drift velocity of carriers through nanochannel is proportional to the channel electric field ($v_{av} \sim V_G^2$). Interestingly, this implies that net current through the entire device is controlled by graphene and can be expressed as charge injection rate as $Q/t \approx \frac{V_G^2}{\frac{L}{v_{av}}} \approx V_G^4$. The I-V characteristics shown in figure 2.3.2-c support the slope V^4 dependence in case of thick SiO_2/p-Si. In the tunnel oxide case (2nm) the I-V slope is even greater than 4. The very large slope usually indicates tunnel transport (exponential dependence on voltage instead of

constant slope in log-log plot). In that case the holes will directly tunnel through the oxide (onto the graphene/trench area) and will involve less lateral conduction on graphene. This implies that the current is limited by thin oxide of anode instead of the graphene's charge states.

2.3.4 Conclusion

In this section, we introduced a complex p-Si/SiO_2//Gr//SiO_2(nano-channel)/n-Si structure. We observed an interesting carrier transport phenomenon through the nano void channel in the oxide layer of n-Si cathode. From the I-V relationship, we showed that the current conduction originates from 2D electron gas injection via nano channel and is solely limited by graphene's density of states that has quadratic dependence on the applied gate voltge. By controlling the graphene's charge states, one can control the current transport throughout this device. This feature makes it an attractive candidate for developing novel field controlled electronic devices.

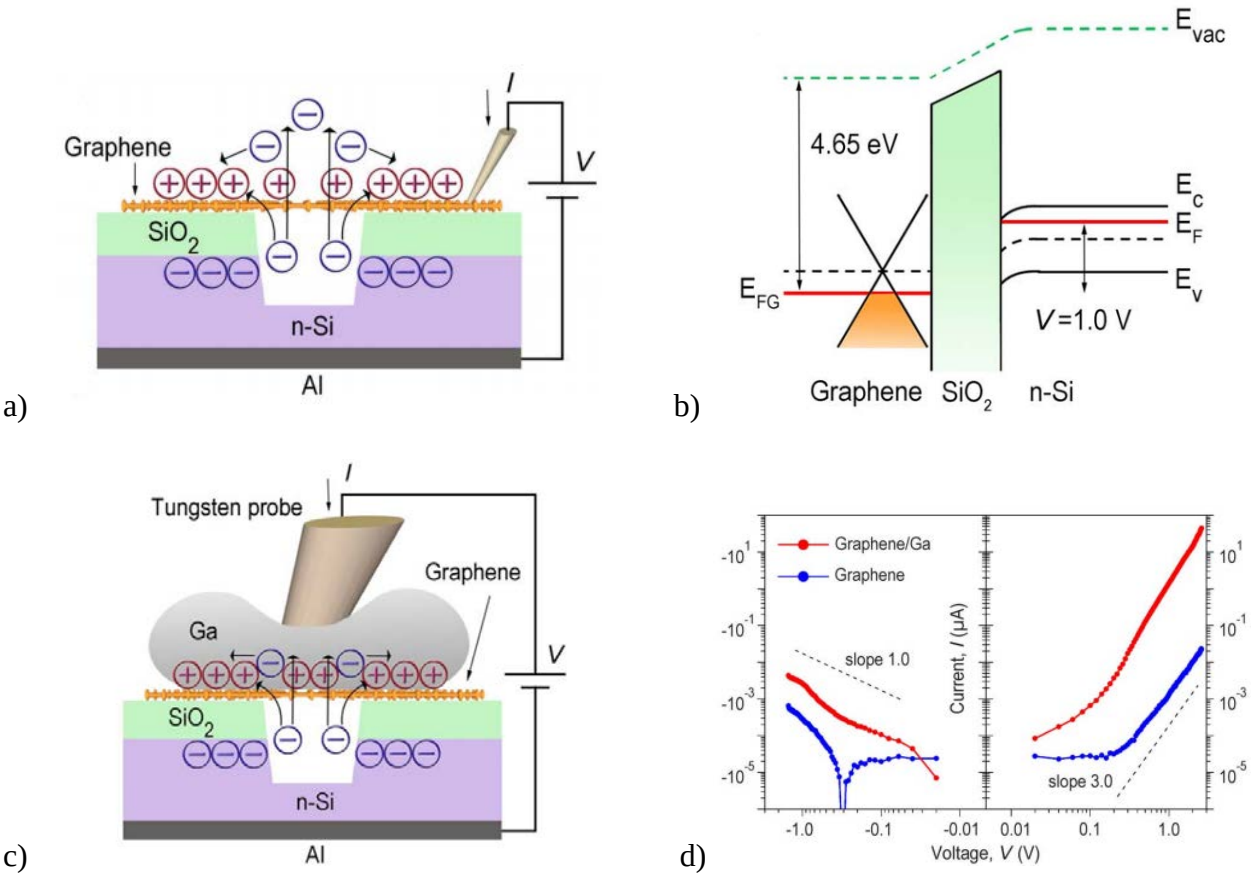

Figure 2.3.1: a) Schematic of electron emission from the 2DEG at SiO2/n-Si interface and capture/transmission at the graphene anode, b) energy band diagram of proposed GOS structure, c) schematic of carrier injection when Ga droplet blocks the trench of GOS structure, and c) I-V characteristics of corresponding device structures [13].

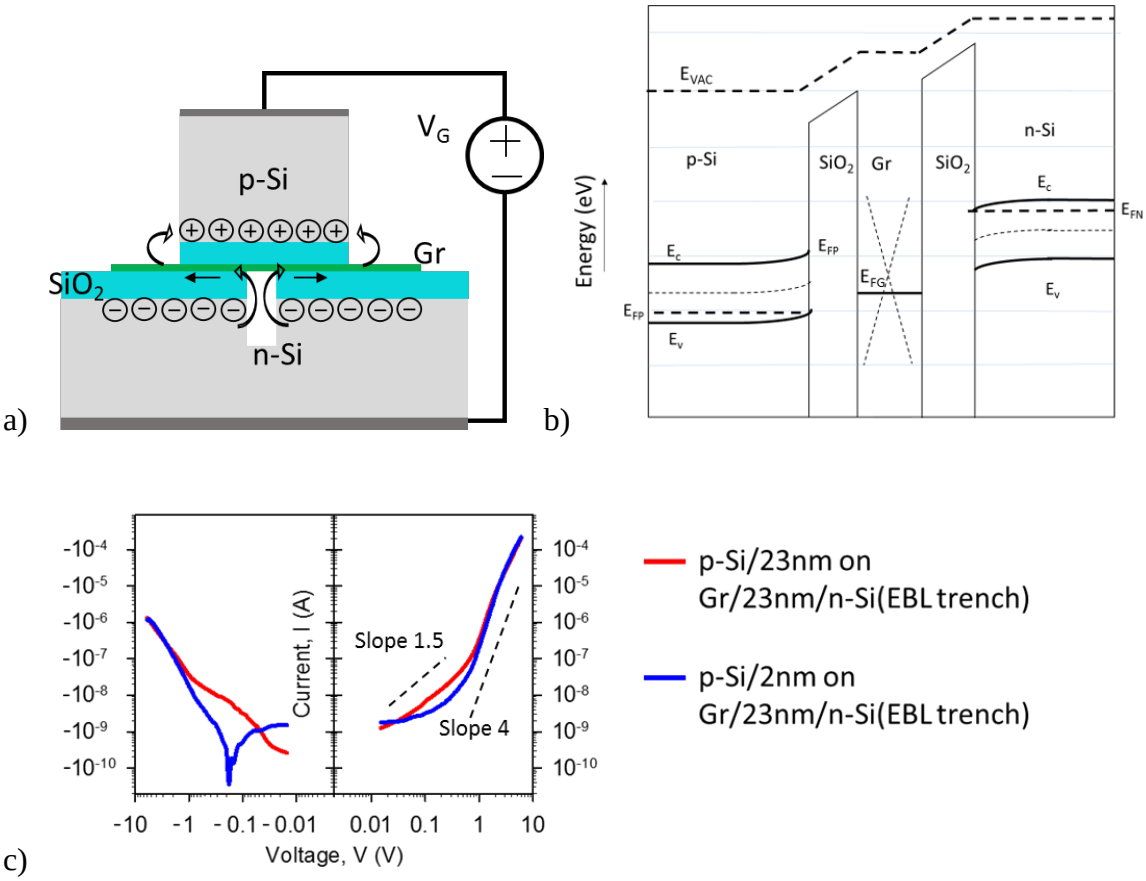

Figure 2.3.2: SOS structure with sandwiched Graphene sheet suspending on EBL trenched sample: a) Schematic of for utilizing 2D charge system injection through the structure, b) energy band diagram during accumulation bias and c) measured I-V characteristics: with 2 nm thin oxide anode (blue) and 23 nm thick oxide anode (red).

2.4 MOS I-V HYSTERESIS

2.4.1 Introduction

We observed an interesting effect of MOS voltage sweep that produces a hysteresis current depending on sweep direction and starting biasing condition. To analyze the observation a series of experiments were designed and we found that the hysteresis characteristics are affected by substrate-doping, gate material, optical excitation, temperature and sweep speed. From the experimental results, we concluded that the hysteresis originates due to low dissipation rate of minority charges during the sweep from inversion to accumulation bias. In the following section, the experimental observations are presented and explained with a possible mechanism.

2.4.2 Device fabrication and characterization

To begin with, we took n-Si substrate with thermally-grown silicon-di-oxide. To build the MOS structure we deposited metal electrodes by thermal deposition through a patterned shadow mask (1.5 mm diameter circular dots). To fabricate GOS (graphene oxide semiconductor), we placed a monolayer graphene on top of oxide by wet transfer method as described in Section 2.3.2. Since transferred large area graphene contains uneven edges and local defects, to define electrode area, we patterned the graphene into variable electrode sizes by photolithography. The lithography process follows standard positive photoresist process used for Si devices. After developing the patterns, graphene was etched by reactive ion etching using oxygen gas. After photoresist removal, the final sample topography with different sizes of graphene electrodes is shown in figure 2.4.1-a.

For I-V measurement, we used HP 4145B semiconductor parameter analyzer. The hysteresis hump is found to be very sensitive with change of these parameters which can be explained with the MOS device physics.

2.4.2.1 Sweep direction effect

Figure 2.4.2 shows the I-V sweep characteristics when bias voltage is applied on a graphene stripe of 400 µm X 100 µm. In figure (a) the sweep direction starts from inversion towards accumulation and in (b) the direction is from accumulation towards inversion. The measurement was performed at room temperature in a dark setup. As seen from I-V graph, a hump appears when sweep is done from inversion to accumulation bias, but not in the opposite direction. The hump can be explained by inversion charge characteristics. At the initial high inversion bias a large quantity of minority charge states is created that is filled up with initial current surge. When the bias is swept towards low voltage, these inversion states shrink rapidly. Now, the excess charges freed from higher-bias states need to be dissipated by a recombination process. However, if the recombination rate is lower than the field-induced charge state-reduction rate, a hump is expected that indicates dissipation of the carriers through external circuitry.

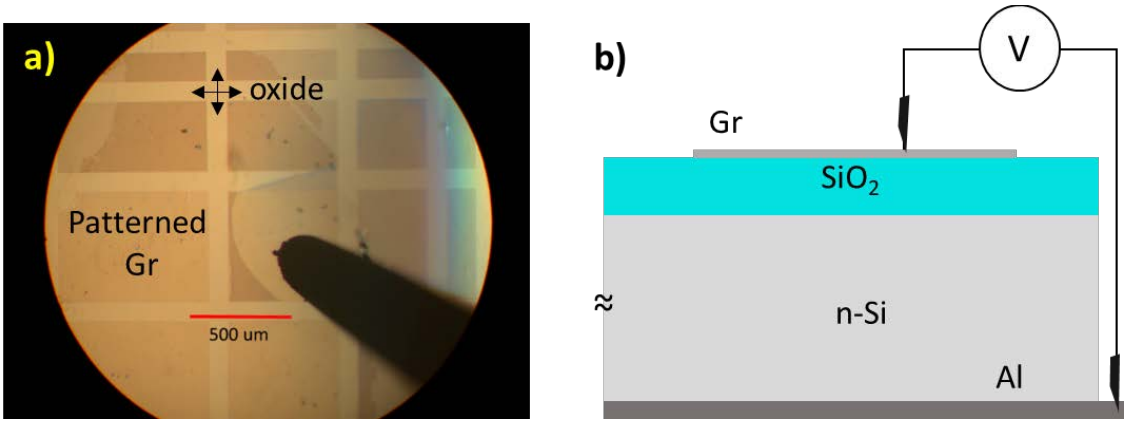

Figure 2.4.1: a) Lithographically patterned Gr and b) measurement setup for voltage sweeping

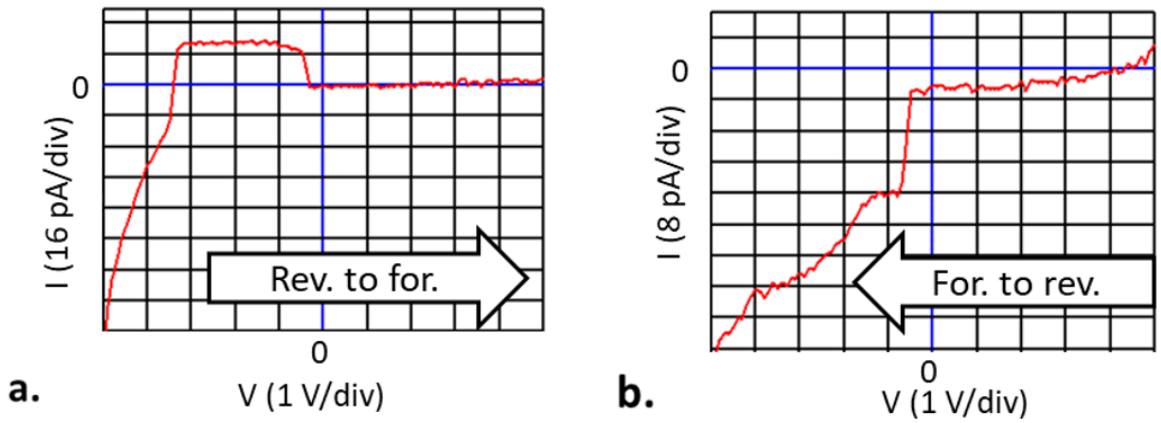

Figure 2.4.2: Effect of sweep direction and starting point on MOS I-V characteristics. (a) sweep from deep inversion towards accumulation. (b) sweep from accumulation towards inversion.

2.4.2.2 Sweeping voltage effect

Figure 2.4.3 shows the effect of the sweep voltage start point for GOS sample with 400 µm X 100 µm graphene anode. The voltage sweep starts from 5 and 12 V for figure a and b respectively, while sweep time is 7.5 s for both cases. For both cases, the hump current amplitude is similar (~20 pA), while the duration of hump is prolonged following the duration of inversion bias. In MOS devices the rate of change of inversion charge with respect to applied bias (dQ/dV) depend only on oxide-induced capacitance (C_{ox}) i.e. oxide thickness. However, for the higher voltage case, we kept the total sweep time same as the lower voltage sweep; therefore, the voltage change rate (dV/dt) is higher for high voltage sweep. This should generate higher hump current which we do not observe significantly from the I-V graphs. This phenomenon indicates that, hysteresis amplitude doesn't only depend on recombination rate, but also on other factors, such as generation time and instrument response time etc. An interesting trend to note for figure b is that, the hump current increases with reducing voltage, while the forward current increases with increasing voltage. The forward conductivity indicates that a stress-induced leakage channel (SILC) has been

created in the oxide layer due to high bias field [22]. At inversion bias sweep, this leakage channel provides charges to neutralize a portion of excess carriers. As the leakage current reduces with lowering of voltage, hump current regains its original value. From the forward I-V, the leakage channel conduction is 2E-12 S. Therefore, the SILC or other defect related oxide current can easily be detected and quantified through hump current change with voltage.

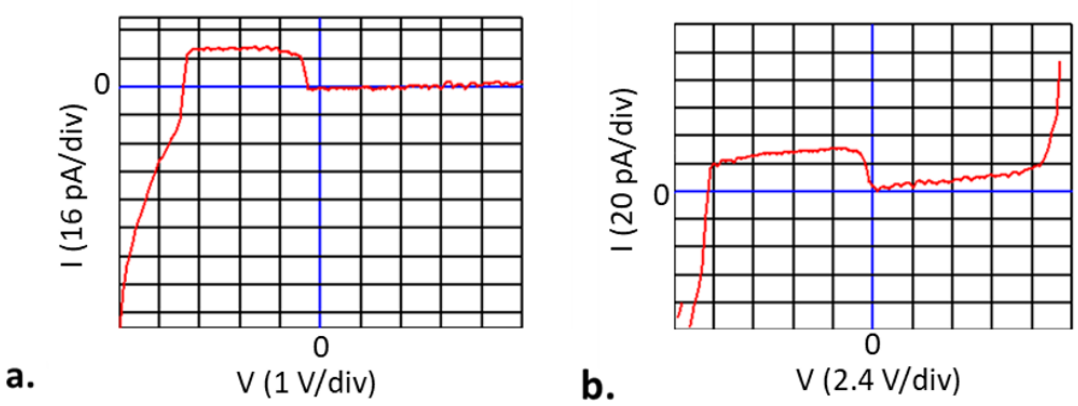

Figure 2.4.3: Effect of sweep voltage range on MOS I-V characteristics. Sweep starting from (a) 5V inversion and (b) 12 V inversion.

2.4.2.3 Electrode material effect

To find the effect of electrode material and work function in MOS I-V sweep, we fabricated MOS structure on SiO_2(50 nm)/n-Si (5 Ω-cm) with Graphene, Aluminum and Silver electrodes. The area of all three electrodes are similar (~ 1 mm^2). Irrespective of the electrode materials, the hysteresis hump appears when sweep direction is from inversion to accumulation. Figure 2.4.4(a) shows the device structure for measurement while b, c & d show the I-V characteristics for Al, Ag and Gr electrodes respectively. The sweeping time for Al and Gr MOS is 30s, while for Ag MOS it's 15s.

We can observe that in Al MOS the hump current diminishes earlier than Ag or Gr MOS. An explanation of this behavior is explained here by showing the inversion threshold voltage variation in MOS due different electrode materials. If there is no charge present in the oxide or oxide semiconductor interface, Flat-band voltage is simply the difference between work function of Metal and Semiconductor ($V_{FB} = \emptyset_M - \emptyset_S$). For n-Si (10 ohm-cm, 5E14 dopant/cm^3) the work function is calculated as:

$$\emptyset_S = |E_i| - |\emptyset_F| = \left|E_i - V_T \ln\frac{N_D}{n_i}\right| \tag{2.30}$$

Replacing the parameters' vlues,

$$\emptyset_S = 4.61 - 0.026 \ln\left(\frac{5\times10^{14}}{1\times10^{10}}\right) = 4.33 \text{ eV} \tag{2.31}$$

For different Electrodes (Al, Ag, Mg, Graphene) on n-Si (10 ohm-cm) substrate, the flat-band voltage voltage would be:

$$V_{FB,Al} = 4.1 - 4.33 = -0.23 \tag{2.32}$$

$$V_{FB,Ag} = 4.7 - 4.33 = 0.37 \tag{2.33}$$

$$V_{FB,Graphene} = 4.6 - 4.33 = 0.27 \tag{2.34}$$

The I-V hump position, especially the end point, depends on the work function difference between semiconductor and metal electrode. For example, Al, Ag and Gr work functions are 4.1, 4.7 and 4.6, while n-Si fermi level is at 4.33 eV. We can see that in case of Ag and Gr MOS, the inversion occurs at lower voltage then Al case. Therefore, in Al MOS, the hump is expected to end at relatively higher reverse bias then Ag or Gr. We indeed observed experimentally that Ag and Gr MOS hump ends at ~0.2V reverse bias, while for Al, hump ends at ~1.5 V.

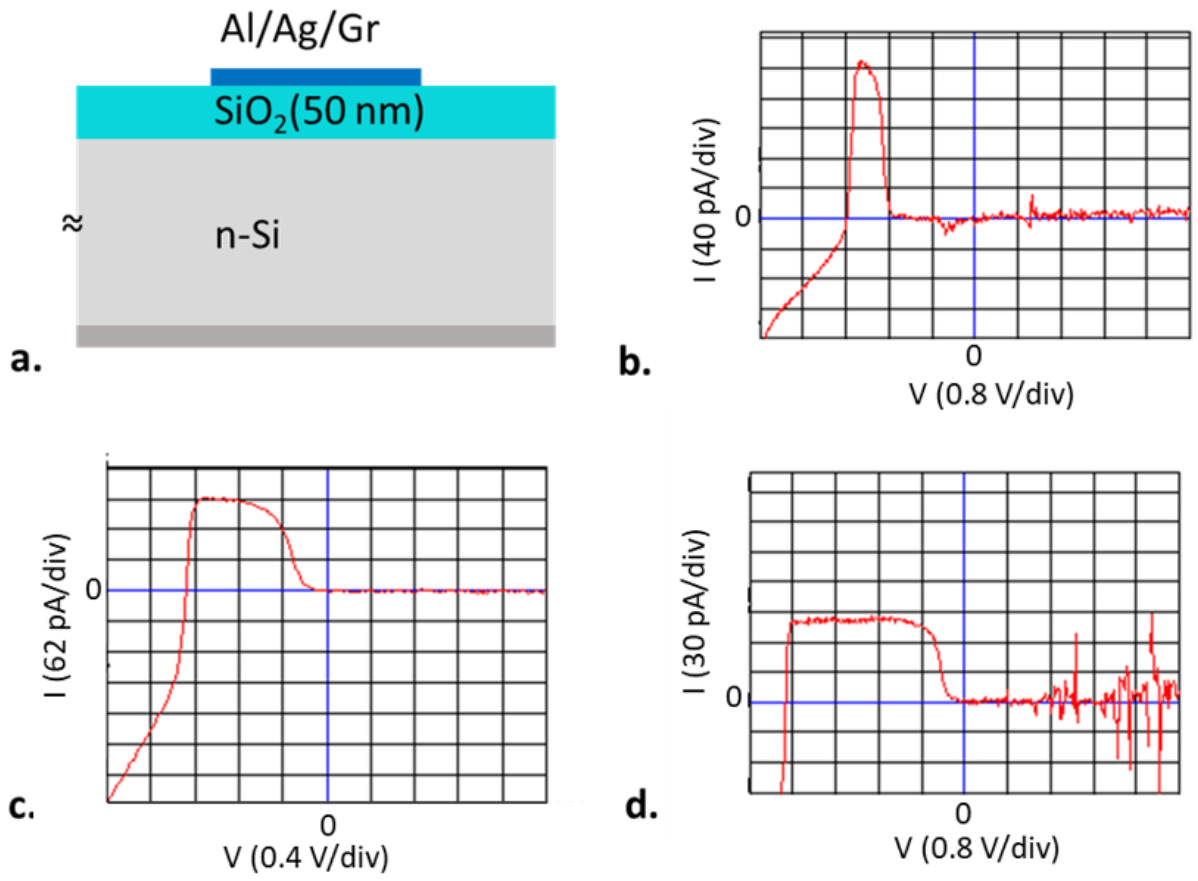

Figure 2.4.4: Effect of gate electrode material on MOS I-V characteristics. (a) device cross section, and MOS I-V plot for b) Al, (c) Ag and (d) Graphene electrode. Sweep direction is from inversion to accumulation.

2.4.2.4 Doping effect

To observe the effect of n and p-type doping of Si substrate on I-V hysteresis, Ag MOS on n- and p-Si is fabricated. The impurity density is $2x10^{14}$ cm^{-3} for phosphorus-doped n-Si, and $5x10^{14}$ cm^{-3} for boron-doped p-Si. The MOS oxide thickness (50 nm) and electrode size (~1 mm^2) are same for both cases. The resultant I-V graph is shown in figure 2.4.5 where the sweep time is 15 s for

both samples. For both PMOS and NMOS, I-V hump occurs when voltage is swept from deep inversion to accumulation bias, but not the other way round which proves our hypothesis

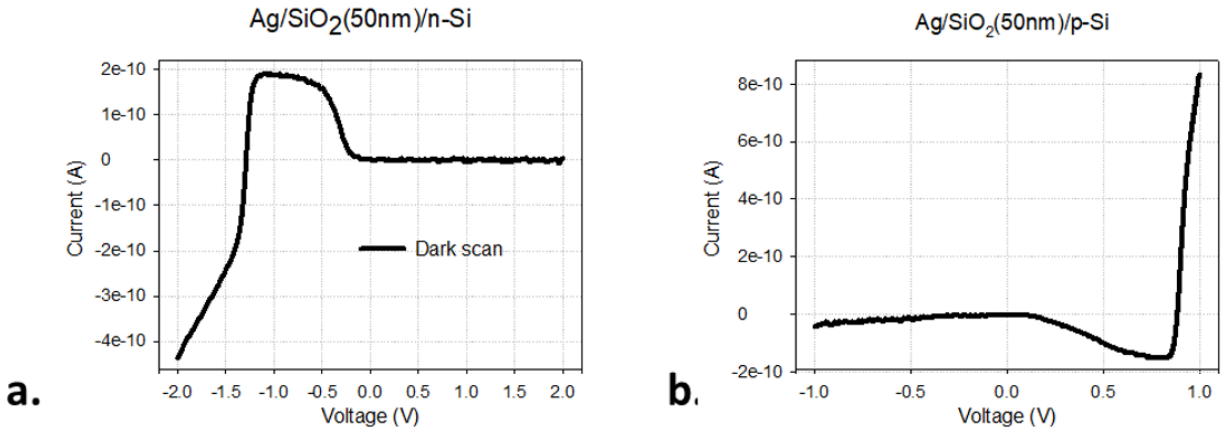

Figure 2.4.5: Effect of Substrate-doping type on MOS I-V sweep characteristics: a) n-type and b) p-type substrate

2.4.2.5 Electrode area effect

By varying the electrode area in Gr GOS we observed that the hump current closely follows the area scaling. Figure 2.4.6-a and b shows GOS I-V characteristics with Graphene electrode area of 0.04 mm^2 and 0.02 mm^2 respectively. The oxide thickness is 25 nm and the sweep time is 7.5 s for both I-V plots. In Figure 2.4.6, the area of graphene electrode reduces by 2 times, resulting in a current reduction by ~1.8 times. The MOS oxide capacitance is proportional to the electrode area, therefore the rate of inversion charge change follows the area scaling as well. Since the carrier lifetime is unchanged irrespective to electrode area, the undissipated inversion carriers increase which is transformed into hump current.

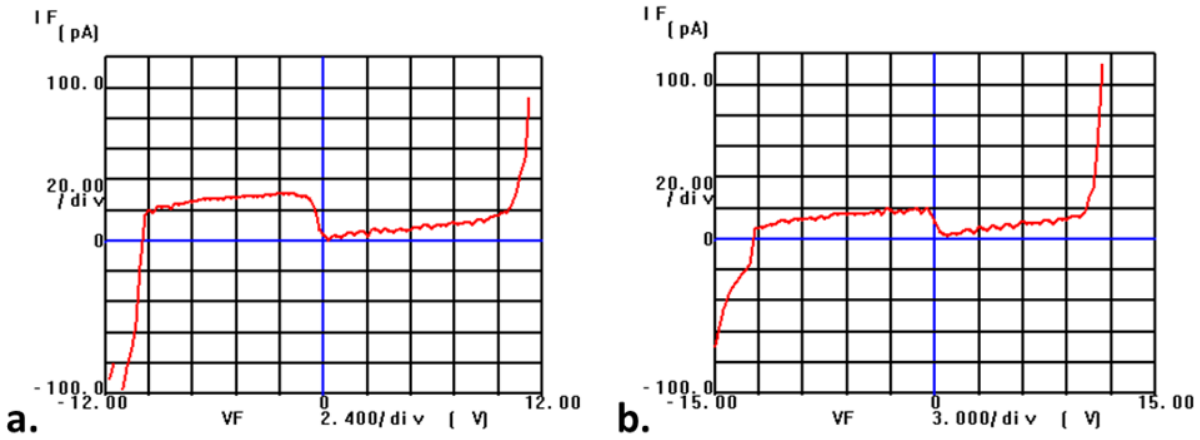

Figure 2.4.6: Effect of electrode area on hump formed on Gr/SiO_2(25 nm)/n-Si. Graphene area is (a) 400x100 μm^2 and (b) 200x100 μm^2

2.4.2.6 Doping density effect

To observe the effect of substrate doping density on hump characteristics, NMOS was fabricated with medium doped ($2x10^{14}$ cm^{-3}) and highly doped ($1x10^{18}$ cm^{-3}) n-Si substrate whose I-V responses are shown in figure 2.4.7. For the highly doped substrate no hump was observed. This phenomenon can be attributed to the effect of doping concentration on minority carrier lifetime. Since additional traps are created at a high doping level, lifetime decreases with increased dopant density. The bulk recombination lifetime of minority carriers in Si originates primarily from Auger or Shockley-Read-Hall (SRH) recombination. In SRH recombination the charge carriers, electrons and holes, are trapped by defect states whose energy levels are located in the forbidden bandgap region. The recombination of trapped carriers occurs most effectively when the defect state seats at the mid bandgap level. Higher doping creates more defect traps, as a result the SRH recombination lifetime increases. The relation between minority carrier lifetime and dopant density can be expressed as:

$$\tau_{p,SRH} = \frac{\tau_{po}}{1 + \frac{(N_D + N_A)^{\gamma}}{N_{ref}}} \tag{2.35}$$

Where N_{ref} and γ are the fitting parameters for holes [23]. $\boldsymbol{\tau}_{po}$ is the hole minority carrier lifetime at a low doping level.

On the other hand, the Auger recombination process involves three carriers. In this process, the energy emitted during a band to band recombination is given to a third carrier. The excited third carrier later thermalizes back to its original position. While SRH recombination depends on lattice impurities and defects in Si, the Auger process depends on the carrier density. Therefore, Auger recombination is most prominent in higher doping and can be expressed as below,

$$\tau_{Auger} = \frac{1}{CN_A^2} \tag{2.36}$$

Where C is the auger coefficient having a value of 1.66×10^{-30} cm^6/s for Si [24]. Figure 2.4.8 shows the bulk lifetime change of minority carriers in Si based on semi-empirical models [25].

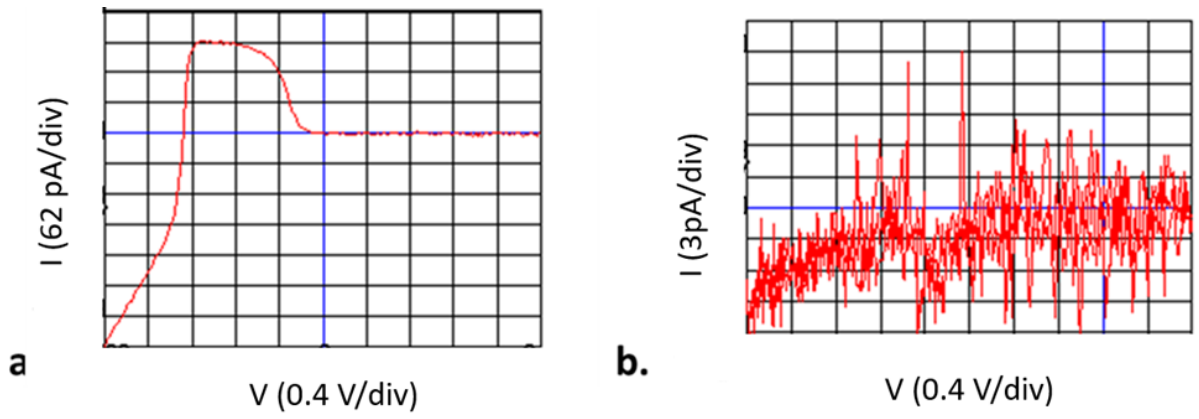

Figure 2.4.7: Effect of doping density of n-Si substrate in Ag MOS case: a) Si resistivity of 20 Ohm-cm (dopant density 2E14 cm^{-3}) and b) Si resistivity of 0.005 Ohm cm (dopant density 1E18 cm^{-3}).

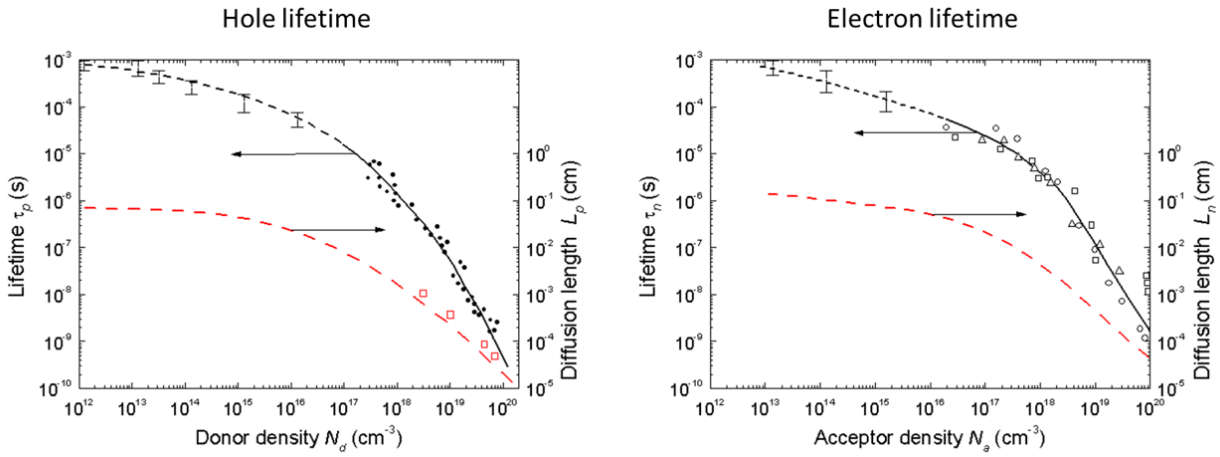

Figure 2.4.8: Change in electrons' and holes' lifetime with doping variation in Si [25, 26].

2.4.2.7 Effect of sweeping speed

The inversion hump amplitude and duration is affected strongly by the voltage sweeping speed. Figure 2.4.9 shows the I-V characteristics for Gr MOS in three different sweeping speeds. The bias voltage was changed from -2V reverse to +2V forward bias. The fast, medium and slow scan takes 22, 30 and 130 s to sweep the entire voltage range. This time rates come from the I-V

measurement instrument setup. As shown in the I-V curve, the hysteresis hump current reduces as the sweep speed is slowed. At the slowest scan speed, the hump current completely disappears.

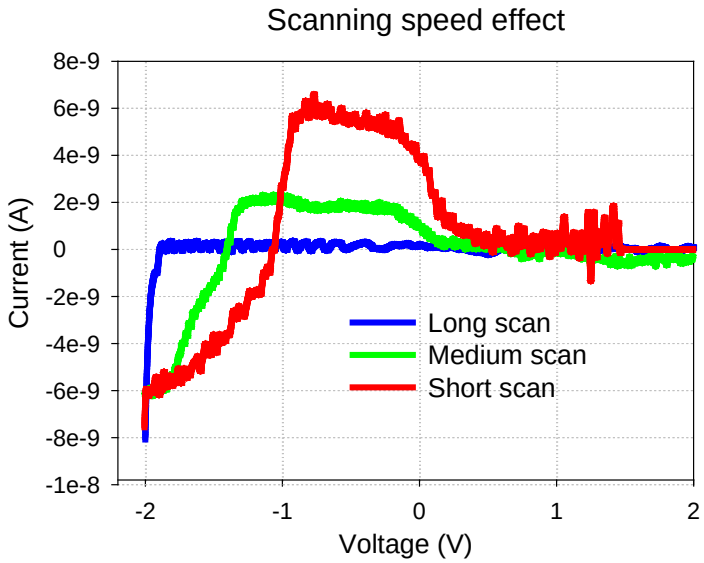

Figure 2.4.9: **effect of sweeping speed on Gr (2 mm^2)/SiO_2(25 nm)/n-Si device**

2.4.2.8 Photon excitation dependence

We observed that the optical excitation also has a strong effect on MOS hysteresis characteristics. To observe the photon excitation effect, we illuminated the transparent GOS (graphene oxide semiconductor) and the opaque MOS samples with a 633nm laser beam. Figure 2.4.10 (a) shows the I-V response of GOS at dark and 40 nW illumination. Due to excellent transparency (98%) of Gr monolayer, the hump completely disappears by illumination as low as 40 nW. While, in case of metal MOS, the effect of illumination is less drastic because of the opaque metal electrode (Figure 2.4.10 (b)). The Ag electrode with 100 nm thickness blocks almost entire photon transmission. In the graph, Photo_1 is lowest and photo_3 is highest illumination intensity giving rise to higher and lower hump current. The illumination effect on hump characteristics might be

explained by the effect of photo-generated carriers on minority carrier lifetime. Upon illumination, Si absorbs the photon energy and generates many electron-hole pairs. When minority carrier density increases due to photo-generated carriers, the lifetime decreases exponentially. Figure 2.4.11 shows a plot of carrier lifetime variation with minority carrier concentration [27]. The relationship between lifetime (τ), doping density (N_D) and minority carrier concentration Δp is given by [28]:

$$\frac{1}{\tau} = (\Delta p + N_D)(1.8 \times 10^{-24} N_D^{0.65} + 3 \times 10^{-27} \Delta p^{0.8} + 9.5 \times 10^{-27} \quad (2.37)$$

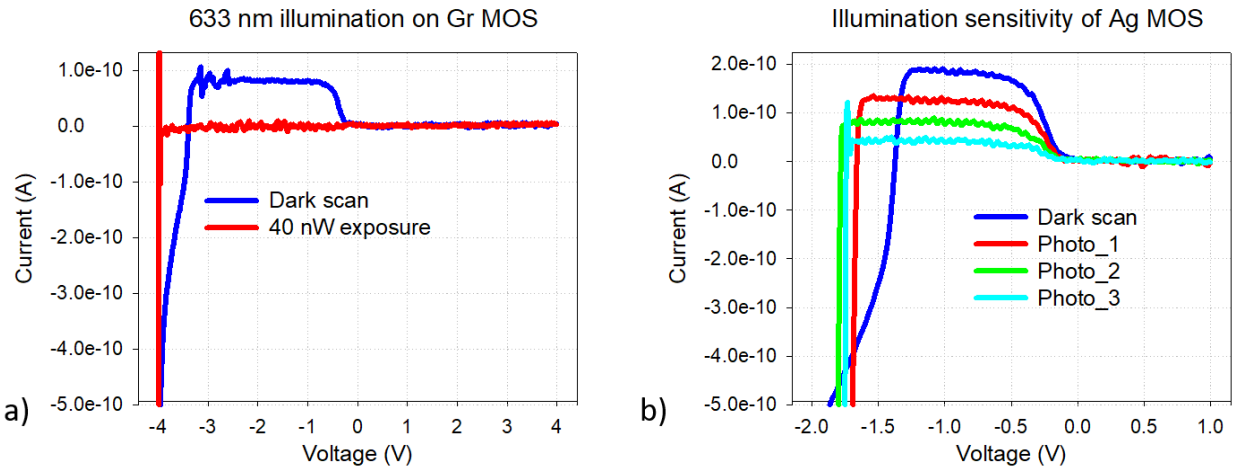

Figure 2.4.10: Effect of photo excitation on a) Gr/SiO_2(25 nm)/n-Si device and b) Ag/ SiO_2(50 nm)/n-Si device

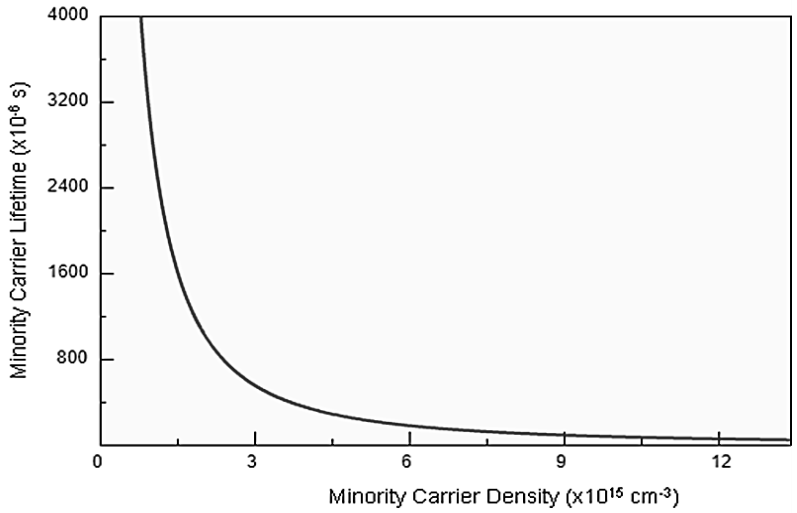

Figure 2.4.11: Change of minority carrier lifetime with excess carrier density [27].

2.4.2.9 Effect of temperature

To observe the effect of temperature on MOS I-V, we mounted the Gr MOS sample (2 mm^2 electrode) on a heating stage and heated the sample to 100^oC. Figure 2.4.12 compares the room temperature vs high temperature I-V hysteresis. The hump appears much earlier in case of heated sample, but the hump amplitude remains the same as the room temperature measurement. The effect of high temperature is more availability of thermal-generated minority carriers. According to the previous section, that should reduce carrier lifetime. But at the same time, higher temperature means higher diffusion-length for minority carriers, therefore higher lifetime. Our assumption is that these two opposite effects balance each other and therefore the minority carrier dissipation rate remains unchanged. On the other hand, increase in minority carrier generation will fill up the deep inversion states immediately. Therefore, slight reduction of bias voltage results in hump current (figure 2.4.12)

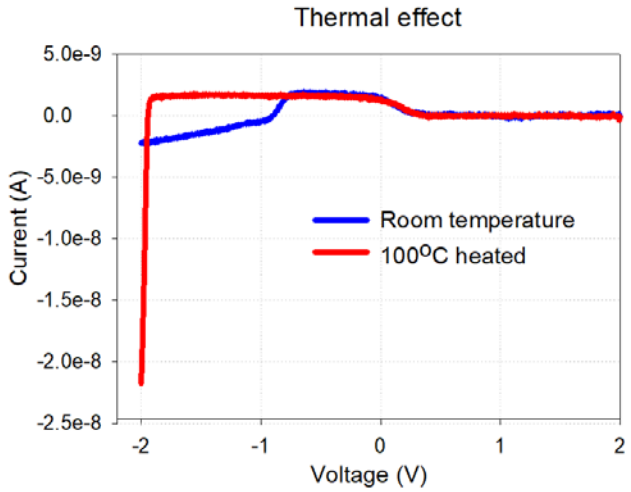

Figure 2.4.12: Effect of temperature increase on Gr/SiO_2(25 nm)/n-Si device

2.4.3 Inversion charge Calculation:

When a small reverse bias is applied at the gate of MOS capacitor (with n-Si), the negative charge on the gate pushes the interface mobile electrons deep into the substrate. As a result, a positive charged region is created consisting of the ionized donor ions. If reverse Gate voltage is increased gradually, at one point the semiconductor surface inverts its conduction type from n to p-type. The gate voltage at which this phenomenon (known as inversion state) occurs is called threshold voltage (V_T) and the positive charged region is called depletion region. If the reverse voltage is further increased, the semiconductor does not keep depleting any longer because of the abundance of positive charge states generated at the interface. Rather, minority carriers (holes) from the bulk region starts accumulating at the oxide semiconductor interface.

After the full depletion is formed (Gate voltage is greater than threshold voltage), inversion layer charge increases linearly with increasing V_G following the oxide capacitance effect:

$$Q_{inv} = C_{ox} (V_G - V_T) \tag{2.38}$$

For 1mm^2 area capacitor and 50 nm oxide thickness, C_{ox} = 0.69 nF; the threshold voltage V_T depends on the electrode material. The following section shows a derivation to calculate V_T for different electrodes.

Let's assume at full depletion the depletion width is x_d, MOS electrode area is A, substrate doping density is N_D. Therefore,

Full depletion charge, $Q_D = q N_D x_d A$

Surface electric field, $E_S = q N_D x_d A / \varepsilon_s$

So, surface potential, $\varphi_S = \int E_S x dx = q N_D A x_d^2 / 2\varepsilon_s$

As full depletion occurs (gate voltage V_T) the surface potential (φ_S) becomes twice the bulk potential (φ_F).

$$\frac{q N_D A x_d^2}{2\varepsilon_s} = 2\,\varphi_F = 2\,V_T\,ln\frac{N_D}{n_i} \tag{2.39}$$

Therefore, full depletion width at threshold Voltage,

$$x_{d,T} = \sqrt{\frac{4\varphi_F \varepsilon_s}{q N_D A}} \tag{2.40}$$

Bulk potential for n-Si is, $\varphi_F = 0.28$ eV and N_D = 5E14 /cm^3; for typical 1 mm^2 area metal electrode, full depletion width:

$$\boldsymbol{x_{d,T}} = \sqrt{\frac{4 \times 0.28 \times 11.9 \times 8.85 \times 10^{-14}}{1.6 \times 10^{-19} \times 5 \times 10^{14} \times 0.01}} = 12.1 \text{ um} \tag{2.41}$$

Therefore, total depletion charge is,

$$Q_{d,T} = q N_D x_{d,T} A = 1.6 \times 10^{-19} \times 5 \times 10^{14} \times .00121 \times 0.01 = 9.68 \times 10^{-10}\, C \tag{2.42}$$

Total number of hole charges in depletion width = $Q_{d,T}/q = 5.8 \times 10^9$

Gate voltage (V_G) is distributed in flat band voltage, surface potential and across oxide capacitor.

$$V_G = V_{FB} - \varphi_S - \frac{Q_M}{C_{ox}} = V_{FB} - \varphi_S - \frac{Q_D + Q_{inv}}{C_{ox}} \tag{2.43}$$

At threshold voltage(V_G=V_T), inversion charge Q_{inv}=0 and surface potential is twice the bulk potential:

$$V_T = V_{FB} - 2|\varphi_F\Big| - \frac{Q_{D,T}}{C_{ox}} = V_{FB} - 2|\varphi_F\Big| - \frac{qN_D x_{d,T} A}{C_{ox}} \tag{2.44}$$

For 1mm^2 area capacitor and 50 nm oxide thickness, $C_{ox} = 0.69$ nF; flat band voltage for Al, Ag and Graphene can be calculated as a difference between metal work function and n-Si Fermi level (4.33 eV in our case).

$$V_{FB,Al} = 4.1 - 4.33 = -0.23\ eV \tag{2.45}$$

$$V_{FB,Ag} = 4.7 - 4.33 = 0.37\ eV \tag{2.46}$$

$$V_{FB,Graphene} = 4.6 - 4.33 = 0.27\ eV \tag{2.47}$$

Therefore,

$$V_{T,Al} = -0.23 - 2 * 0.28 - \frac{9.68 \times 10^{-10}}{0.69 \times 10^{-9}} = -2.235\ V \tag{2.48}$$

$$V_{T,Ag} = 0.37 - 2 * 0.28 - 1.445 = -1.63\ V \tag{2.49}$$

$$V_{T,Graphene} = 0.27 - 2 * 0.28 - 1.445 = -1.735\ V \tag{2.50}$$

Now we can calculate inversion charges for MOS and GOS by plugging the derived values into equation 2.38:

$$|Q_{inv,AL|} = 0.69 \times 10^{-9} * (|V_G| - 2.235) \quad (2.51)$$

$$|Q_{inv,Ag\,|} = 0.69 \times 10^{-9} * (|V_G| - 1.63) \quad (2.52)$$

$$|Q_{inv,graphene\,|} = 0.69 \times 10^{-9} * (|V_G| - 1.735) \quad (2.53)$$

Interestingly, now we can find out the minimum power of photoexcitation needed to diminish the inversion hump (figure 2.4.10). In the above-calculated samples at reverse bias V_G=5V, the number of inversion charges:

$$N_{e,Al} = Q_{inv} / q = 2.77 \times 10^{-9} / 1.6 \times 10^{-19} = 1.73\times 10^{10}\ per\ cm^2 \quad (2.54)$$

$$N_{e,Ag} = Q_{inv} / q = 3.37\times 10^{-9} / 1.6 \times 10^{-19} = 2.1\times 10^{10}\ per\ cm^2 \quad (2.55)$$

$$N_{e,graphene} = Q_{inv} / q = 3.26\times 10^{-9} / 1.6 \times 10^{-19} = 2.03\times 10^{10}\ per\ cm^2 \quad (2.56)$$

Now, the number of photons per second in 1 nW, 633 nm beam is;

$$N_{ph} = \frac{P\,\lambda}{hc}$$

$$= \frac{(1 \times 10^{-9} * 633 \times 10^{-9})}{(3 \times 10^{8} * 6.63 \times 10^{-34})}$$

$$= 3.18 \times 10^{9} \quad (2.57)$$

Assuming each photon can generate one electron hole pair, 10 nW charges would be sufficient to neutralize all the inversion charges. In that sense, our experimental result showing complete nullification of hump or hysteresis effect supports our analytical calculation.

2.4.4 Conclusion

In this extensive study of MOS hysteresis, we carefully varied different device parameters and recorded the effect by I-V measurement. A few observations are confirmed throughout this study: firstly, the instrument's measurement speed has a profound effect on the hump current, the faster sweeping rate results in a higher hump current. Therefore, for fair comparisons, all the measurements were done at similar scanning speed. An interesting finding is that the hump current is affected by a wide range of MOS device parameters, for example, electrode materials, electrode area, temperature, illumination, substrate doping type and impurity concentration, oxide quality, etc. Since the hump current is already very low, in order of pA range, any small change in these parameters is found to have a distinguishable effect on hump current. Surprisingly, we did not find any literature explaining these phenomena of MOS deep inversion sweep. The most likely reasons are the appropriate oxide thickness, high capacitance and dark ambience needed to observe the effect of excess inversion charges during the voltage sweep. The high sensitivity of various device parameters in hysteresis current opens up an opportunity to fabricate economic sensing devices using simple MOS structure.

3.0 CHAPTER 3: QUANTUM DOT ORGANIC LED ON SILICON

3.1 INTRODUCTION

A semiconductor quantum dot (QD) can be defined as a body where the electron and hole wave functions are confined on all sides by the crystal boundaries, and the quantum mechanical effect of this confinement is that the electron-hole pairs can only have discrete energies. To use quantum dots as luminophores in optoelectronic devices, organic light-emitting diodes (OLEDs) have received considerable attention in recent years due to their advantage in terms of low manufacturing and material cost, convenient fabrication methods, decent efficiency and a wide range of material variety. In this chapter, we summarize our work on incorporating semiconductor QDs (CdSe/ZnS) as an emissive layer into an inverted OLED structure that utilizes a semiconductor substrate. In the first section, we studied the carrier transport mechanism in organic layers and calculated their carrier mobility. The fabrication methods for OLED and its optical and electrical characteristics have been presented in later sections. Through the electroluminescence results of OLEDs with various sizes and geometries, we demonstrated a novel 2D electron gas injection along the periphery of OLEDs.

3.2 ELECTRONIC PROPERTIES OF ORGANIC POLYMERS

3.2.1 HOMO and LUMO levels

Organic polymers are covalently coupled hydrocarbon molecules in repeated units, generally deposited by evaporation or spin coating. The carbon atoms in polymers are sp2 hybridized and therefore can form π-bond using their non-hybridized p_z-electrons. The semiconducting nature of organic polymers originates from this weak π-bond. The π-orbital of unsaturated hydrocarbons splits into bonding π-orbital and the anti-bonding π∗-orbital, which are called Highest Occupied Molecular Orbital (HOMO) and Lowest Unoccupied Molecular Orbital (LUMO) respectively. The band splitting in ethane is shown in figure 3-1(a). Overlapping of HOMO and LUMO levels of all the molecules in the material forms energy profile similar to valance and conduction band. Using the analogy of inorganic semiconductors, their energy difference is called the energy gap of that organic material. If the material is intrinsic, which means without any doping, the Fermi level of a material is expected to be in the middle of the energy gap. The solubility of an organic semiconductor material in an organic solvent depends on its side chains. The side chains also control the degree of electronic interaction, relative orientation and inter-chain interaction. By this way, side chains eventually control the luminescence and carrier mobility of organic polymers [29].

Charge transfer mechanism in organic polymers is quite different from the highly ordered, single- or polycrystalline inorganic semiconductors, where intermolecular interaction can be sufficiently large for band transport of carriers. The localization of molecular orbitals and the large degree of disorder in conjugated polymers makes such kind of band transport impossible. Instead, charge transport in organic semiconductors occurs by carrier hopping between localized orbitals,

each of which has a defined energy and an orientational disorder parameter. Electronically, 6-8 molecules form pi-conjugated segments, that are bonded by non-conjugated sections. Figure. 3.2.1(b) illustrates carrier hopping between segments of a conjugated polymer.

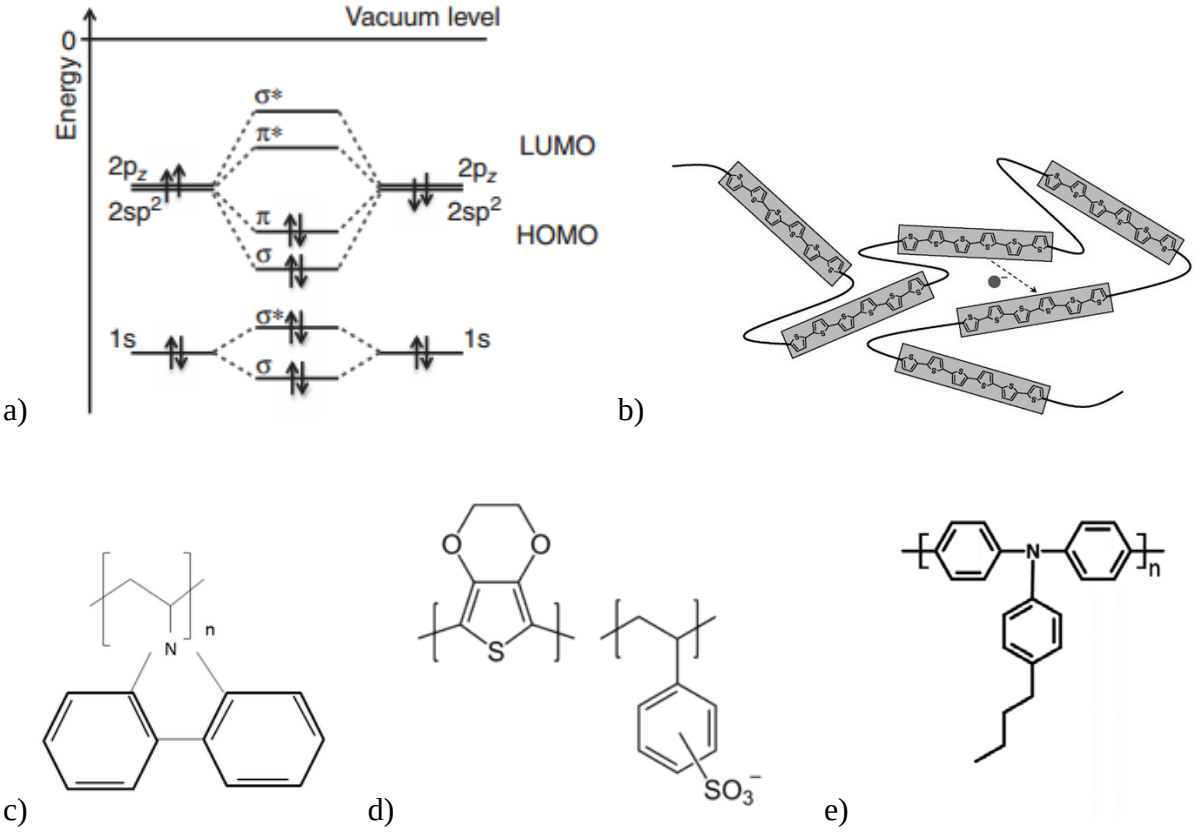

Figure 3.2.1: (a) the formation of σ and π bonds from atomic orbitals for ethane [30], b) conceptual diagram of hopping mechanism of charge transport in conjugated polymer, chemical compositions of c) PVK (poly-(N-vinyl carbazole)), c) PEDOT: PSS (poly(3,4-ethylenedioxythiophene) polystyrene sulfonate) and d) Poly-TPD (Poly-tetraphenyl diamino phenyl)

3.2.2 Traps in organic polymers

The organic semiconductor consists of localized states that form molecular orbitals to transport carriers and form a narrow band. In classical semiconductor physics, a localized energy state

located in the forbidden energy gap is regarded as a trap. The energy favorable traps capture carriers and release them after a specific holding time. The traps slow down carrier mobility and change electric field distribution along carrier conduction path. If the trap energy state is located close to the conduction band, it's an electron trap and similarly, near the valance band it's a hole trap. But in organic semiconductors, the band consists of molecular orbitals that are highly localized. So, the difference between a trap and a HOMO/LUMO state is not straight forward. One way to define traps using transport energy concept is explained by D. Monro [31]. This approach is based on the energy transfer process in the deep tail states in DOS distribution (figure 3.2.2). Statistically it can be found that the carriers in deep tail states are the most probable to jump up to a transport energy state (E_T) irrespective of their initial position. So, transport energy state is similar to the band edge of inorganic semiconductors. In short, the carriers above E_T participate in current transport process, while the carriers below need to jump back to this state to participate in conduction. Therefore, energy states below the transport energy can be regarded as traps. There can be several intrinsic reasons of trap formation in organic polymers, for example, impurities [32], structural defects [33], Germinate pairs [34] and self-trapping [35]. Each of these reasons is critical to analyze organic device's performance and are briefly explained below:

An impurity in organic polymers forms a trap state when its HOMO or LUMO level is in the band gap region of the host molecules and is generally associated with a species of different chemical composition from the organic semiconductor. The impurity associated trap is significant in polymers since their chemical purity lags far behind the inorganic semiconductors, for example, silicon [36]. Moreover, intermolecular interactions in an organic polymer film are determined by relatively weak van der Waals force, which makes it susceptible to the process-related chemical impurities, such as solvent and ambient gas molecules [36]. Structural defects can cause a change

in conjugation length in organic polymers. As a result, the molecular orbital levels (HOMO/LUMO) will have wider tails that will increase trap states. Structural imperfection can occur during synthesis, coating or the annealing process of polymer based OLED fabrication. Structural motif, such as twisting in a conjugated polymer chain, can create immobile electron-hole pairs [37]. The Germinate pair originates from the Coulomb interaction of electrons and holes when they exist simultaneously in an organic film. The Germinate pair acts either as a recombination center (when electron and holes meet) or a trap center (when recombination is suppressed). The last mechanism of trap formation we mentioned is self-trapping, which occurs when the organic molecules themselves contain any excess carrier. An excess carrier creates molecular deformation that eventually lowers its energy. As a result, the mobility of an excess carrier is much lower than the free carrier mobility. In some polymers, the energy lowering of excess electron in a molecule can be several hundreds of mV which may immobilize the carrier.

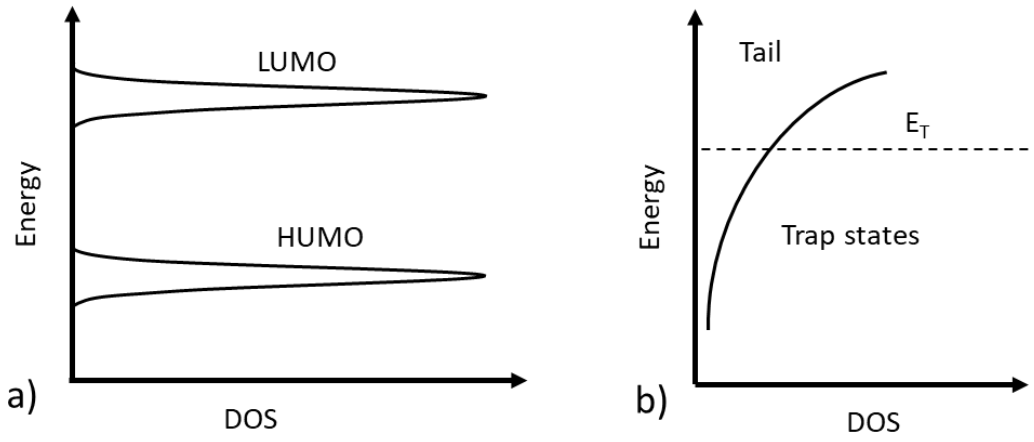

Figure 3.2.2: (a) Energy levels and Density of State (DOS) distribution of organic polymers, and (b) trap states defined by energy states below a threshold transport energy level in DOS tail states.

3.2.3 Carrier mobility

In the inorganic semiconductors, like Si, the electrons and holes move as delocalized waves (Bloch states), giving them mean-free paths that are two to three orders of magnitude higher than the semiconductor's lattice constant. Therefore, the resulting mobility is very high, on the order of 10 to 1000 cm^2/V.s. On the other hand, in organic polymers electrons and holes are localized in single molecules, and charge transport occurs by the hopping process where electrons and holes can quantum mechanically tunnel towards favorable adjacent or non-adjacent molecules in the material. Now, if we express the intrinsic density of charge carriers (n_i) in an organic polymer in the same way as inorganic semiconductor:

$$n_i = N_o \, exp\left(-\frac{E_g}{2k_B T}\right) \tag{3.1}$$

where N_o is the density of molecules in organic polymers, E_g is the energy gap, k_B is the Boltzmann's constant and T is the device temperature. Low energy gap in common semiconductors yields very high intrinsic carrier density (e.g. ~$5x10^9$ cm^{-3} for Si). On the other hand, organic semiconductors generally have a large bandgap, usually in the range of 2.5 to 3.5 eV, resulting in a small number of intrinsic carriers. For example, an organic material with 2.5 eV would have an intrinsic carrier density,

$$n_i = 10^{21} \, exp\left(-\frac{2.5}{2 * 25.3}\right) = 0.35 \, cm^{-3} \tag{3.2}$$

Due to the extremely small number of intrinsic carriers, the conductivity of organic polymers is very low, while interestingly their charge mobility can be significant, ranging from 10^{-7} cm^2 / V.s to 10 cm^2 / V.s [38]. As stated earlier, this originates from the

hopping process of charges from one molecule to the next and can be altered by dopants, electric field, and temperature variation. For example, high doping into organic polymers (e.g. PEDOT: PSS) can increase conductivity as high as a few hundred Siemens. At an electric field of 10^4 to 10^6 V/cm, the Poole-Frenkel conduction formalism can be applied to find the carrier mobility in an organic semiconductor [39]. In this model, the mobility of carriers can be expressed in terms of electric field in the following expression:

$$\mu(E) = \mu_o \exp\left(\gamma\sqrt{E}\right) \tag{3.3}$$

where μ_o is zero field mobility, E is the electric field and γ is the electric field dependence parameter. The temperature dependence of carrier mobility is analogous to Arrhenius-like behavior [40] resulting in the following relationship. Here, E_a is the activation energy.

$$\mu_o(T) = \mu_\infty \exp\left(-\frac{E_a}{k_b T}\right) \tag{3.4}$$

3.2.4 Current transport mechanism

The current transport mechanism in organic polymers can be limited by several parameters depending on the chemical composition, contact nature and applied field. A simple way to observe electrical characteristics, such as carrier mobility and trap density, is to analyze I-V characteristics and find an appropriate carrier transport model. In this section, we briefly discuss the most commonly observed transport mechanisms in organic polymer based devices and highlight their I-V equations. In the next section, we will use these equations to explain the carrier transport mechanism through our OLED materials.

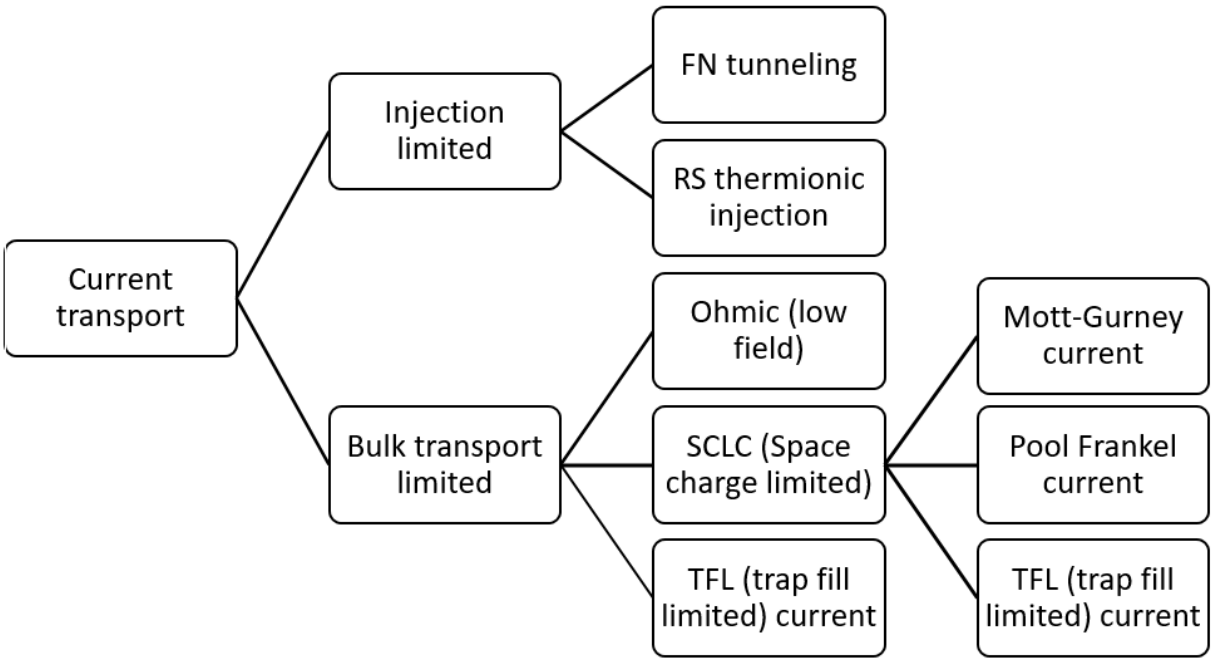

Figure 3.2.3: Current injection mechanism in organic semiconductors

3.2.4.1 Injection limited current

The two important carrier injection mechanisms into semiconductors are Fowler-Nordheim (FN) tunneling and thermionic emissions. According to FN theory, the charge carriers can quantum mechanically tunnel through the insulator at the presence of a high electric field. The large electric field reduces the effective energy barrier width and helps the carriers to overcome it. The calculation of FN tunneling is based on WKB (Wigner, Kramer, Brillouin) approximation and can be expressed as:

$$J = AE^2 e^{-\frac{B}{E}} \tag{3.5}$$

Where, $A = \frac{q^3 m}{8\pi h m^* \varphi_b}$ and $B = \frac{8\pi}{3}\frac{\sqrt[3]{\varphi_b}\sqrt{2m^*}}{hq}$, h is planks constant, Φ_b is the carrier injection barrier from electrode to semiconductor, k_B is the Boltzmann constant, m is the electron mass in vacuum,

and m^* is electron's effective mass in insulator. The OLED transport layers and electrodes are carefully chosen to minimize the carrier transport barriers. Since FN tunneling involves a high potential barrier, it is unlikely that the carrier injection in efficient OLED stack is limited by F-N tunneling.

On the other hand, if the potential barrier between the electrode and the organic material is small, a number of carriers can gain enough thermal energy to cross over the barrier at moderate or high temperature. When a bias voltage is applied across such a metal-semiconductor interface, the carriers start accumulating in the semiconductor beneath the contact surface. In response to the semiconductor charges, image charges build up in the metal electrode such that the net electric field is zero. The electric field associated with the interface charges reduces the effective potential barrier for charge injection from metal to semiconductor [41]. This phenomenon is known as Schottky effect, and together with thermal injection, it can explain injection mechanism through low barrier interfaces. The resultant current can be expressed by the Richardson Schottky equation:

$$J = A^* T^2 e^{\left(-\frac{q\left(\varphi_b - \left(\frac{qE}{4\pi\varepsilon}\right)^{\frac{1}{2}}\right)}{KT} \right)} \tag{3.6}$$

where A^* is Richardson constant and φ_b is the interface barrier.

3.2.4.2 Bulk limited current

Ohmic transport and space charge limited conduction (SCLC) are the two primary mechanisms for bulk transport in organic semiconductors. An Ohmic conduction is linearly proportional to the applied electric field and occurs when an infinite reservoir of charges (Ohmic contact) sustains a steady state SCLC throughout the device. The I-V relationship for Ohmic conduction is:

$$J_{Ohm} = qN\mu E \tag{3.7}$$

where N is the carrier density, E is the electric field and μ is the charge mobility.

On the other hand, space charge limited current (SCLC) occurs when injected carriers build up and create an internal electric field among themselves that becomes dominant over applied bias. The device current is then controlled by the carrier mobility rather than carrier injection. For SCLC to occur, one of the electrodes should be able to supply an unlimited number of carriers into the bulk [42]. Following the field independent mobility assumption, the SCLC current for a bulk material can be expressed with Mott-Gurney equation:

$$J_{TFSL} = \frac{9}{8}\frac{\varepsilon_0\varepsilon_r\mu E^2}{d} \tag{3.8}$$

where $\varepsilon_0 = 8.854E-12\ Fm^{-1}$ is the vacuum permittivity, ε_r is the relative permittivity of the medium, d is the film thickness and E is the applied electric field. This quadratic voltage dependence model is applicable when the conducting film is not affected by trap states, which means either it is trap free or all the traps are filled, and the carrier mobility is field independent. However, as stated in the previous section, the mobility of a disordered system such as organic polymers changes with applied electric field. The modified space charge limited current can be derived by replacing Pool-Frenkel mobility into Mott-Gurney equation [43]:

$$J_{TFSL}^{PF} = \frac{9}{8}\frac{\varepsilon_0\varepsilon_r\mu_o E^2}{d}\exp\left(0.89\gamma\sqrt{E}\right) \tag{3.9}$$

where μ_0 is zero field mobility and γ is the electric-field coefficient determined by experiments and generally have a value of ($10^{-2} - 10^{-4}$ $(cm/Vs)^{0.5}$) for organic materials [44].

Now, let's consider the effect of trap states in organic film current. Presence of trap states generally lowers the current in organic film. Since all the charges are not free mobile carriers, the drift mobility needs to be replaced by the product of free carrier's drift mobility and a fraction of charges that is free. Therefore, the effective drift mobility would be reduced. For shallow traps that lie close to HOMO or LUMO bands, this fraction is determined by the number and depth of traps and independent of applied voltage. But if the traps are uniformly distributed throughout the forbidden energy gap, the Fermi energy level shifts and the free carrier fraction shows electric field dependency. Traps gradually fill up with carriers as electric field is increased and this results in a faster current increase which translates into higher I-V slope. At a moderate temperature, the trap-limited current can be described by the following equation [45]:

$$J = q^{l-1}\mu N_V\left(\frac{2l+1}{l+1}\right)^{l+1}\left(\frac{l}{l+1}\frac{\varepsilon}{H_b}\right)^{l}\frac{V^{l+1}}{d^{2l+1}} \tag{3.10}$$

where N_v denotes the density of states in the valance band (HOMO level) of the organic film, H_b denotes the total trap density, l is the ratio of characteristic temperature (T_C) and device temperature (T).

3.2.4.3 Thickness dependence

A useful difference between injection-limited and bulk-limited current is the thickness dependence of current transport [46]. If the conduction is purely injection-limited, the current is independent of the thickness of bulk material. On the other hand, space charge-limited current shows various degrees of thickness dependence. At a constant electric field, the trap-free space charge-limited

current is inversely proportional to thickness ($J \sim \frac{1}{d}$), while in the presence of traps, it scales down much more rapidly with thickness increment ($J \sim \frac{1}{d^{l}}$). The relationship is useful to find moblity.

3.2.5 Experimental result for mobility measurement

To develop an efficient OLED device, it is critically important to balance the hole and electron injection towards the emissive layer. The amount of electron and hole current injected into the emissive layer depends on several factors, such as transport layer thickness and mobility, carrier injection barrier, recombination centers and trap sites. Therefore, it is important to choose the OLED components carefully in terms of HOMO/LUMO level, mobility and thickness. To determine the electrical properties of OLED components, we fabricated hole-only or electron-only devices by placing either hole transport layer [HTL] or electron transport layer (ETL) between two electrodes. The electrodes were chosen such that the carrier injection barrier is the same as the real OLED device. For example, in the case of PVK and Poly-TPD HTLs, we used ITO as anode and Al as cathode. While, for ZnO ETL we used n-Si as cathode and Al as anode.

3.2.5.1 ZnO nano particle electron transport layer

ZnO nanoparticles are widely used as a hole blocking layer in current OLED research [47,48]. Since ZnO has a high bandgap energy of 3.3 eV with a large valance band edge of -7.5 eV (figure 3.2.4) [49], electrons can be easily injected from metals while holes can be blocked from the opposite side. However, due to high bandgap energy, the pristine ZnO film has a very low intrinsic carrier concentration of 10^6 cm^{-3} resulting in a low mobility. But intrinsic oxygen vacancy can be introduced in ZnO thin film in various ways to improve the carrier concentration up to 10^{16} cm^{-3}

[50]. Due to the convenient and economic fabrication method, many optoelectronic devices use ZnO nanoparticles to form a transport layer instead of using the thin film. Moreover, ZnO nanoparticles intrinsically contain oxygen vacancies due to their enhanced grain boundaries [51]. As the size of nanoparticles shrinks their mobility and conductivity increase. Jiangyong et al. showed that when the ZnO NP size is reduced from 5.5 to 2.9 nm, the mobility increases by an order of magnitude from 7×10^{-4} to 5×10^{-3} $cm^2/V.s$ [49].

We explored the effectiveness of commercially available ZnO nanoparticles as an electron transport layer, as well as a hole blocking layer in our OLED with n-Si cathode. We purchased ZnO nanoparticles dispersed in iso-propanol with 0.8 mg/mL density and 10-15 nm diameter from Sigma Aldrich Inc. To measure the NP film mobility, we fabricated an MOS type structure (Figure 3.2.4-a). We took an n-Si wafer with 5 Ohm-cm resistivity as a substrate as well as a cathode. After creating back side metal contact and removing the surface native oxide with BHF etchant, we spin coated the purchased ZnO NP solution and annealed it at 90^o C for 30 minutes. The thickness of NP film was measured to be ~40 nm. Finally, we deposited Al metal electrodes on top of ZnO by thermal evaporation. The I-V measurement data is shown in figure 3.2.4 d&e.

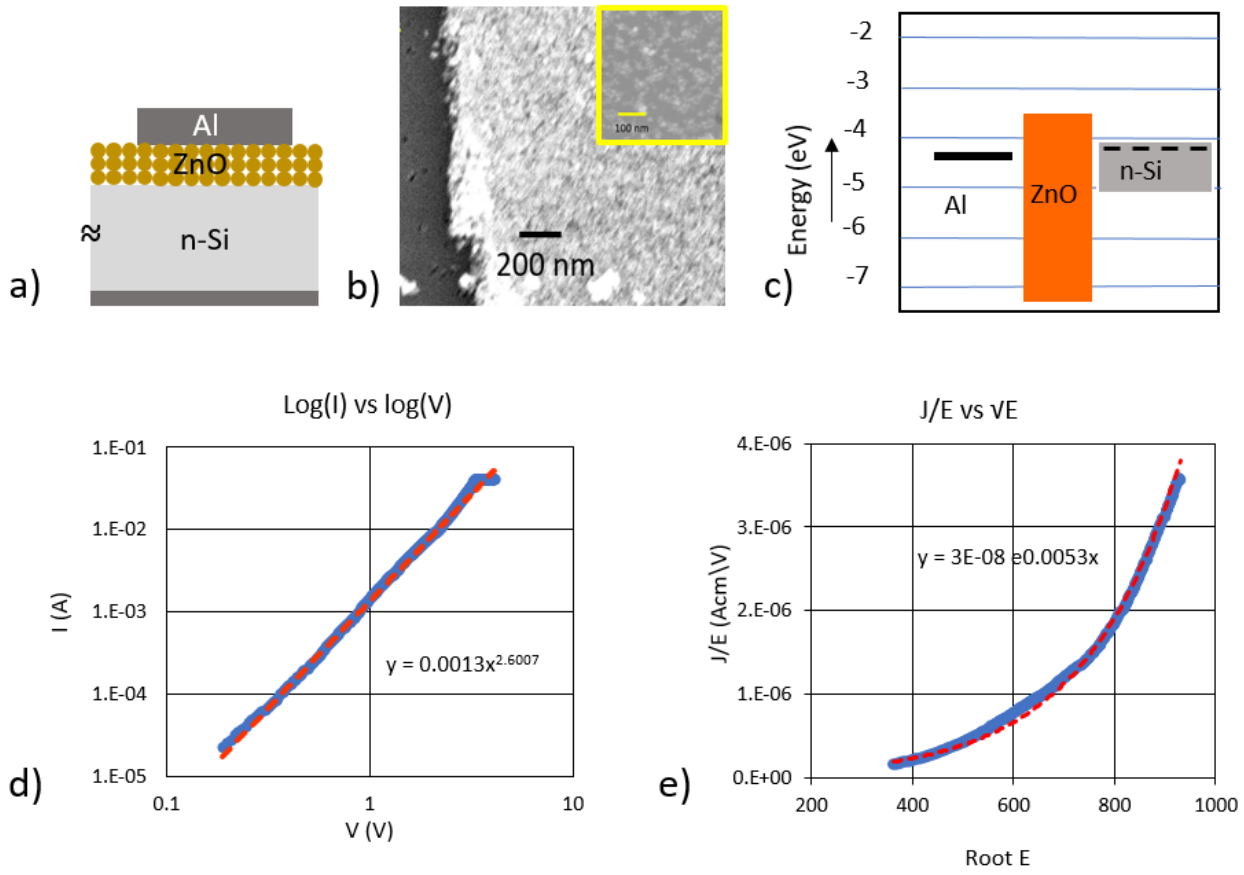

Figure 3.2.4: a) device cross section for ZnO mobility measurement, b) SEM image of ZnO NP film on oxide/Si substrate, inset shows the NP size, c) Band diagram of proposed device, d) log (I) vs log(V) plot with fitting power law, and e) (J/E) vs $\sqrt{E}$ plot with fitting exponential equation.

The mobility of a thin film can be extracted from its I-V characteristics by applying appropriate transport model. In figure 3.2.4-d, plotting I-V in log scale we can observe a slope of ~2.6 at operating voltage range. The deviation from quadratic voltage dependence (Figure 3.2.4-d) indicates that the transport is not purely SCLC limited. The faster increase of current might be originated from voltage-dependent mobility together with a space charge limit. Therefore, we can still use the Mott Gurney equation to find the mobility:

$$\frac{I}{A} = \frac{9}{8}\frac{\varepsilon_0 \varepsilon_r \mu V^2}{d^3} \tag{3.11}$$

where the relative permittivity of ZnO is ε_r =10 [52], film thickness d= 40 nm, and electrode area = 1.13 mm^2. Therefore,

$$0.0013 = \frac{9}{8}\frac{\varepsilon_0 \varepsilon_r \mu A}{d^3} \tag{3.12}$$

$$\mu = \frac{0.0013 * 8 * d^3}{A * 9 * \varepsilon_0 \varepsilon_r} = 7.5 \times 10^{-6} \tag{3.13}$$

Therefore, the mobility of electrons in ZnO nanoparticle film is 7.5E-6 $cm^2/(V.s)$.

Now, let's consider another transport mechanism to extract mobility from the I-V equation. Considering the current density in our device proportional to applied electric field,

$$J = nq\mu E \tag{3.14}$$

where n is the intrinsic carrier density and μ is the carrier mobility. Since in an organic semiconductor the mobility is dependent on electric field, therefore we can apply Pool-Frenkel equation for field-dependent mobility:

$$\frac{J}{E} = nq\mu_0 e^{\gamma\sqrt{E}} \tag{3.15}$$

Therefore, the ratio of the current density (J) and the electric field depends exponentially on the square root of the electric field. Figure 3.2.4-e plots the J/E vs $\sqrt{E}$ plot and it shows an exponential relationship. We can assume the exponential equation with the help of curve fitting and find the coefficient values:

$$\frac{J}{E} = (3 \times 10^{-8}) e^{0.0053\sqrt{E}} \quad (3.16)$$

Therefore, $nq\mu_0 = 3 \times 10^{-8}$,where n is the intrinsic carrier density, q is the charge of a single carrier, and μ_0 is the zero-field mobility. If we estimate the intrinsic carrier density in our ZnO nanoparticle film as n= 10^{16}cm^{-3}, we find a mobility of 2E-5 cm^{2}V^{-1}s^{-1}. The mobilities we calculated from two different approaches are quite similar. However, the ZnO mobility that we found for 15 nm nanoparticle is about an order of magnitude smaller than the mobility reported for ~5 nm diameter ZnO nanoparticle film [49]. We concluded that the higher diameter of the commercially available ZnO generates lower mobility. We also observed from our test OLED structure (not shown in this thesis) that using commercially available ZnO NP does not improve luminescence or efficiency, instead it increases the nonuniformity of emission.

3.2.5.2 ITO /PEDOT/PVK (45 nm)/Al

In our OLED structure, we used PEDOT as the hole-injection layer and PVK as the hole-transport layer. To measure the hole mobility of p-type layers we placed thin film of PEDOT and PVK sandwiched between ITO (Indium Tin Oxide) and Al electrodes. To begin with, an ITO-coated glass with resistivity of 10 ohm-cm, was cleaned thoroughly in an ultrasonication bath with acetone, methanol and DI water for 15 minutes each. After N_2 blow drying, a de-moisturizing baking was performed on the cleaned ITO at 100^{o}C for 30 minutes. PEDOT:PSS was spin-coated on top of it at 2krpm spin speed. The PEDOT was purchased from Heraeus, Clevios (TM PH1000) with a conductivity of 1000 S. After annealing the sample at 120^o C for 30 minutes we got 30 nm bluish film. On top of it, we spin-coated PVK at 2krpm spin speed and annealed again at 120^o C for 30 minutes. The PVK solution was prepared by dispersing PVK powder in chlorobenzene at a

weight ratio of 1.1 mg/mL. On top of the annealed film an Al electrode of 1 mm^2 area was deposited by thermal evaporation. The schematic of device cross section is shown in figure 3.2.5-a. To find an appropriate carrier transport model the I-V characteristics of this device is plotted in two different ways (3.2.5-b and c).

As shown in figure 3.2.5-b, the J-V relationship can be expressed with a quadratic power law. This indicates that the current through PEDOT/PVK layers follows an SCLC mechanism that is not affected by traps meaning there are either no traps in these polymers, or all the traps are already filled. We can extract the mobility by plugging in the curve fitting equation into Mott-Gurney formulae. Here, the PEDOT relative permittivity (ε_r) is ~2.2 [53]. The relative permittivity of the PEDOT/PVK stack can be assumed to be 3 [54], total film thickness(d) is the sum of PVK(45 nm) and PEDOT (30 nm) thickness. From equation 3.8,

$$\frac{9}{8}\frac{3 \times 8.854 \times 10^{-14} \times \mu}{(75 \times 10^{-7})^3} = 0.0005 \qquad (3.17)$$

Therefore, the hole mobility of the entire structure is 8.5×10^{-7} cm^2/vs. This value is quite similar as reported by Khalifa et al. [55] for similar device configuration. Also, in figure 3.2.5-c the plot of log(J/E) vs √E is shown. It clearly doesn't show any meaningful trendlines, which indicates that the field dependency of carrier mobility is not significant. Since the SCLC depends on the thickness of the transport layer, we reduced the PVK thickness to ~15 nm to enhance the hole injection into the emissive layer, CdSe quantum dots.

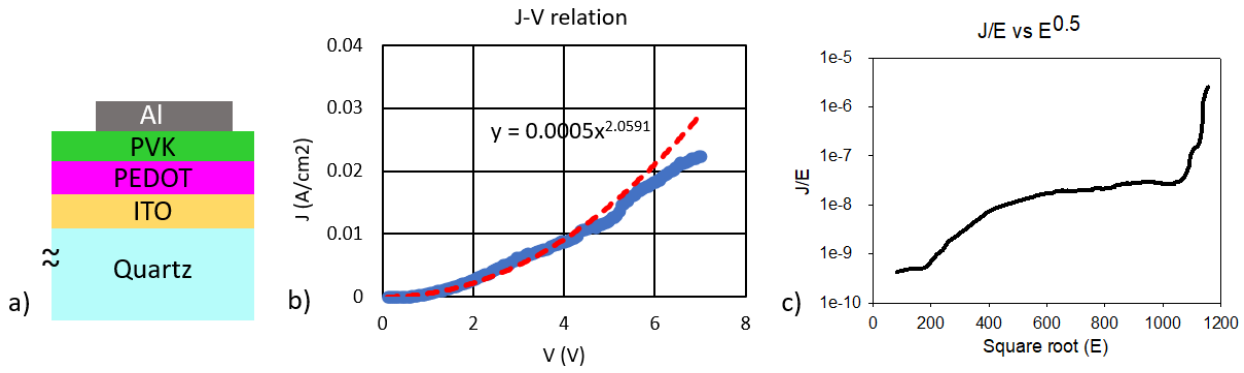

Figure 3.2.5: a) Device cross section of Al/PVK/PEDOT/ITO, b) J-V characteristics, c) log(J/E) vs √E plot

3.3 CORE-SHELL QUANTUM DOT: CdSe/ZnS

Semiconductor nano crystals, known as quantum dots (QD), are widely used in optoelectronic devices due to its unique ability to confine the exciton pair of electrons and holes in a nanoscale regime [56]. Depending on the synthesis process, QDs can be categorized as colloidal and epitaxial/self-assembled. In this report, we utilized colloidal QD due to their size and shape precision, mono-dispersity, spectral purity and high photoluminescence quantum yield. In contrast to surface bound epitaxial growth of QDs, colloidal quantum dots are freestanding and favorable for post chemical processing and thin film assembly. However, the colloidal quantum dots have a very high surface-to-volume ratio due to their spherical shape with a few nm of diameter, and therefore, the optical and structural property of a QD is severely influenced by the nature of its surface. If not properly passivated, the QD surfaces tend to harbor surface defects, for example, dangling bonds and trap states that can generate non-radiative recombination sites, degrading the device performance. [57]. To alleviate this problem a passivation layer, usually, a secondary semiconductor layer can be grown as a shell around the core particle (Figure 3.3.1). It is reported

that the shell passivation layer increases QD quantum yield by as much as 10 times and gives stability from photo-oxidation, air borne moisture and environment-induced degradation. [58].

In this study, we used core shell QDs as the luminophore having a CdSe core (E_g=1.74 eV) surrounded by the ZnS (E_g=3.61 eV) shell. This large bandgap shell confines the excitons to the core and passivates the surface defects. ZnS shell also prevents the core from degradation processes, such as photo bleaching and reaction with oxygen and moisture. However, there is a ~12% lattice mismatch between CdSe and ZnS, and due to this limitation, ZnS can't be thicker than one or two nanometers [59]. The intrinsic advantage of inorganic QDs is that emission can be tuned throughout the entire visible spectrum by changing their size, and this way a single material can be used to generate blue, green and red colors. Furthermore, inorganic QDs are more stable than any organic lumiphore, which is crucial for the commercial production of long lifetime OLEDs. In this study, we utilized inorganic QDs on a Si platform incorporating organic layers for carrier-injection, transport, and confinement for high-efficiency LEDs.

3.3.1 Quantum Dot (QD) properties

3.3.1.1 Size dependent optical characteristics

The carriers in a 3D bulk semiconductor experience the boundless periodic potential of the crystal lattice and reside in a well-defined continuous band structure. In this structure, when an electron from the conduction band fills up a hole from the valance band by a radiative recombination process, a photon is emitted with energy equal to the semiconductor band gap E_g. Now, if we shrink the semiconductor size down to few nanometers diameter, a quantum confinement effect starts to develop. Such a nanocrystal is known as semiconductor quantum dot where the electrons' and holes' wave functions are confined by the higher potential crystal boundaries. Due to this

confinement effect, electrons and holes are allowed only in discrete energy states instead of continuous conduction or valance band (figure 3.3.1). The transition energy between lowest conduction and highest valance band state in a QD is greater than the bulk band gap energy E_g by a size dependent energy shift $\Delta E_{n,l}$ [60], where n denotes the discrete energy level and l values denote transition to molecular orbitals like s and p. The energy discretization and bandgap energy shift disappears as the size of the nano crystal gets order of magnitude larger than the electron's wavelength. Therefore, after a certain size limit, the quantum confinement diminishes, and the nano crystal energy bandgap merges with the bulk bandgap. For example, in CdSe nanocrystals, increasing the radius from 0.6 nm to 4.15 nm changes the absorption peak from 3.02 eV to 1.88 eV [61].

The absorption peak states in CdSe QD can be calculated by the following equation [60]:

$$E_{n,l} = E_g + \Delta E_{n,l} \tag{3.18}$$

$$E_{n,l} = E_g + \frac{1}{R^2}\left(\frac{m_o}{m_e} + \frac{m_o}{m_h}\right)\frac{h^2 \propto_{n,l}^2}{8m_o} \tag{3.19}$$

where m_o is the free electron mass in vacuum, m_e and m_h are electron and hole effective mass, and $\alpha_{n,l}$ is a variable which takes discrete values to define different energy levels. The value of $\alpha_{n,l}$ is π, 2π, 3π .. for value of n=1,2,3… respectively and it takes intermediate values for different l values to denote transition to molecular orbitals like s and p [60]. For bulk CdSe, E_g is 1.7 eV, m_e/m_o is 0.13, m_h/m_o is 0.45, and $h^2/8m_o$ is 0.376 eV nm^2 [62]. If the QD radius is R, then the emitted photon energy in eV will be,

$$E_{1s-1s} = E_g + \frac{1}{R^2}\left(\frac{m_o}{m_e} + \frac{m_o}{m_h}\right)\frac{h^2}{8m_o} \tag{3.20}$$

$$E_{1s-1s} = 1.7\,(eV) + \frac{1}{R^2}\left(\frac{1}{0.13} + \frac{1}{0.45}\right) 0.376 = 1.7\,(eV) + \frac{3.73}{R^2} \tag{3.21}$$

The CdSe QD we purchased has Photoluminescence peak at 625nm. We can find the corresponding Energy band gap as:

$$E = \frac{hc}{wavelength} = \frac{1239.7}{625}\ eV = 1.98\ eV \tag{3.22}$$

Plugging in this Energy gap value in the equation 3.2:

$$1.98 = 1.7 + \frac{3.73}{R^2} \tag{3.23}$$

Therefore, the quantum dots we purchased have a diameter of 2R=7.3 nm. Considering the ZnS shell structure having a thickness of 1 nm, the total diameter of our core shell structure is ~9 nm. To calculate the discrete energy states for E_c and E_v we can apply equation 3.20 separately for electrons and holes. In case of conduction band,

$$E_{C,n} = E_{C,bulk} + \frac{1}{3.65^2}\left(\frac{m_o}{m_e}\right)\frac{\propto_{n,l}^2 h^2}{8m_o} \tag{3.24}$$

Which gives the following discrete energy states,

$$\begin{aligned} E_{C0} &= -4.25 + \frac{1}{3.65^2}\left(\frac{1}{0.13}\right)0.376 = -4.03\ \text{eV} \\ E_{C1} &= -4.25 + 4 * 0.22 = -3.37\ \text{eV} \\ E_{C2} &= -4.25 + 9 * 0.22 = -2.27\ \text{eV} \\ E_{C3} &= -4.25 + 16 * 0.22 = -0.73\ \text{eV} \end{aligned} \tag{3.25}$$

Similarly, valance band energy states:

$$E_{V0} = -6.15 - \frac{1}{3.65^2}\left(\frac{1}{0.45}\right)0.376 = -6.15 - 0.063 \text{ eV} = -6.213 \text{ eV} \quad (3.26)$$

$$E_{V1} = -6.4 \text{ eV}; E_{V2} = -6.717 \text{ eV}; E_{V3} = -7.15 \text{ eV}, E_{V4} = -7.725 \text{ eV} \quad (3.27)$$

Figure 3.3.1 shows the energy band structure of CdSe/ZnS core shell quantum dot we used in our OLED. Here the conduction and valance band edges of CdSe is 0 and -8.2 eV [63]. The electron affinity of CdSe is -4.15 eV and the bandgap is 1.75 eV [*64*] while for ZnS shell they are 3.35 and 3.5 eV respectively [65].

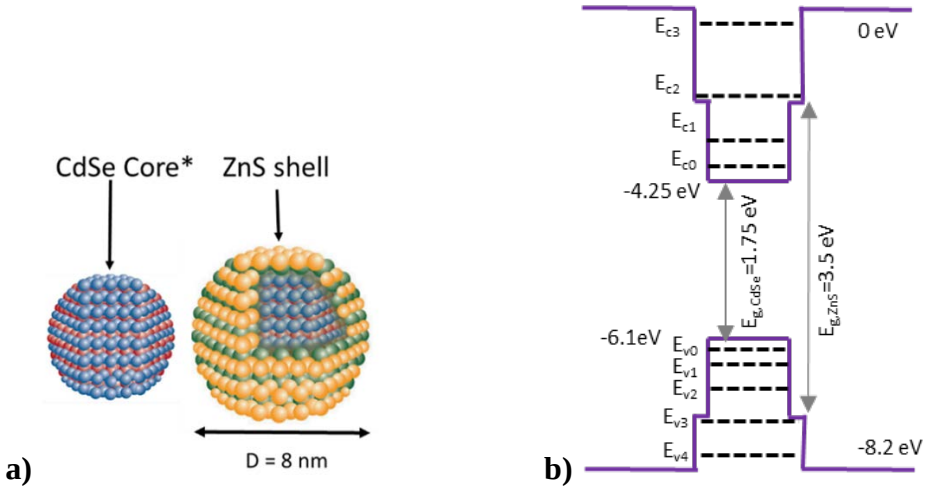

Figure 3.3.1: a) Structural diagram [image courtesy of Evident technologies] and b) band energy diagram of CdSe/ZnS core shell quantum dot

3.3.1.2 Luminescence Quenching mechanisms of QDs

One of the limitations of semiconductor quantum dots in real world devices is their luminescence quenching by various intrinsic (i.e. surface defects) and extrinsic processes (i.e. electric field effect, Auger recombination, photooxidation). Among them, the Auger recombination process is very efficient for confined structures like quantum dots and has a recombination lifetime in order of picoseconds, which is much faster than QD radiative recombination lifetime (nanoseconds)

[66]. In bulk unconfined semiconductors, Auger recombination is greatly suppressed by reduced Coulombic interaction between charges and kinematic restrictions regarding energy and momentum conservation [67]. On the other hand, due to quantum confinement effect, the Auger recombination in QD structures is not limited by such energy constraint, rather enhanced greatly due to increased Coloumbic interaction between same polarity charges. For this reason, the Auger process is much more probable in QDs compared to their bulk counterpart having a wide bandgap energy [67].

A widely observed PL-quenching phenomenon in QD is photo blinking or fluorescence intermittency, that is, during photoluminescence, some QDs turn off completely and eventually recover after arbitrary time periods [68]. The consensus from literature indicates that the PL-blinking occurs due to a random charging and discharging process in QDs during constant photo-illumination [69]. Upon optical excitation, an electron from the valance band can absorb a photon and migrate to the conduction band, thus creating an electron-hole pair/exciton. In neutral QDs, this electron-hole recombines and releases the recombination energy as a photon. However, if the QD is charged with an excess electron and/or hole, the Auger recombination may occur where the recombination energy is transferred to the excess carrier instead of photo-emission. Figure 3.3.2(a) shows a neutral QD energy diagram where a photoexcited electron-hole pair recombines radiatively and emits a photon. Now, if the QD is ionized with an extra charge, the recombination energy will be transferred to that carrier. After acquiring the energy, the excess carrier will jump up either to the continuum (figure 3.3.2-b) or to one of the higher bounded states (figure 3.3.2-c), depending on the localization potential U_0. The extra carrier can emerge from various non-ideal sources. In case of photoexcitation, the extra charge originates from a photoexcited electron-hole pair when one of the charges of the pair gets captured in a trap state [70]. On the other hand, in

case of OLEDs that use quantum dots (QDs) as luminophore, the imbalance between the number of injected electrons and holes can induce extra charges in QDs causing OLED efficiency roll-off [71].

To reduce non-radiative Auger recombination several schemes have been adopted by various researchers such as, incorporating surface bound ligands, growing thick semiconductor shells around nano crystal, graded/alloyed core formation, changing energy states by varying QD size etc. Figure 3.3.3 shows the variation of Auger recombination lifetime with various QD sizes and potential profile. George et. al. qualitatively showed that softening the QD confining potential results in suppression of the Auger rate by attenuating the high-frequency component of carriers in ground state levels [72]. This soft confining potential can be achieved by creating alloyed QD structure, for example with $Cd_xZn_{1-x}Se$ core with decreasing x with distance from the center [70]. An interesting fact is that, when the excess charge acquires exciton recombination energy during the Auger process, it needs to jump to a higher energy level which satisfies the energy conservation formula. Therefore, QDs of certain sizes can have a confinement potential distribution that suppresses Auger recombination by limiting the final states of excited excess charges. In figure 3.3.3, George et. al. calculated the confinement width of QDs that can suppress the Auger recombination. We used a commercially available core-shell QD in our QD-OLED. We did not perform a vigorous optimization of carrier transport layers in term of material and film thickness, which might have resulted imbalance in the number of injected holes and electrons into the QD. Therefore, all our OLEDs are affected by Auger recombination and show lower efficiency compared to optimized structures reported in literatures. Due to the synthesization complexity of quantum dots, we did not focus on optimizing the diameter of QD to avoid Auger recombination. Nevertheless, the analysis of various luminescence quenching methods and ways to suppress them

remain as future optimization tasks in order to maximize our QD-OLED efficiency. Another approach to reduce Auger recombination would be optimizing the carrier transport layers and operating voltage to balance the injection of electrons and holes into quantum dots.

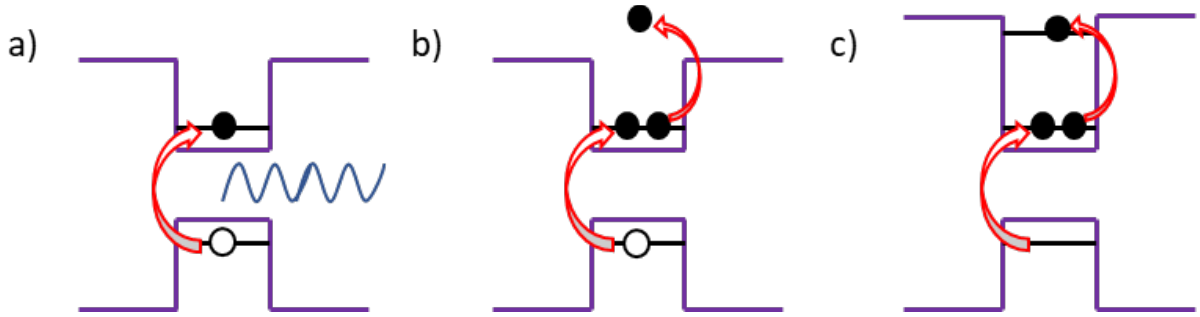

Figure 3.3.2: a) radiative recombination, Auger recombination with excess elector driven to (b) continuum and (c) higher bounded energy state

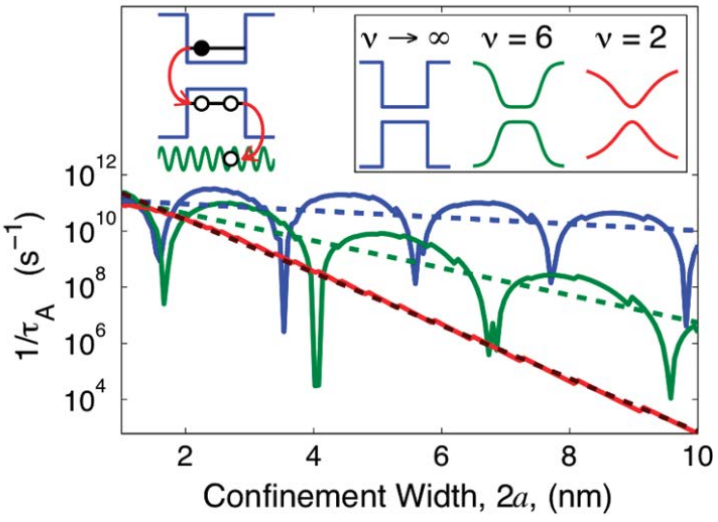

Figure 3.3.3: Auger recombination lifetime dependence on confinement width and potential wall smoothness [72]

3.3.1.3 Optical characterization of CdSe QD solution

We purchased CdSe/ZnS core-shell QD colloidal solution (630 nm PL peak wavelength) from Ocean Nanotech Inc. The specification provided by the company is listed in the following table [Evident Technologies. Web]

Table 3.1: Specification of CdSe/ZnS QD

Product name:	CdSe/ZnS core/shell quantum dot in toluene
Solvent:	Toluene
Emission wavelength:	630 nm
Emission tolerance:	±10 nm
FWHM:	<25 nm
Quantum yield:	>50%
Surface group:	Octadecylamine
Concentration:	10 mg/mL

Photoluminescence of CdSe QD was characterized using a 325-nm excitation beam. To begin with, 10 uL QD solution was spin-coated on a clean quartz substrate in 2000 rpm speed followed by baking at 70^{o}C for 30 minutes. For PL measurement, He-Cd laser of 325 nm pump beam (vertically polarized E-field) was projected in a 45^{o} angle on QD-coated quartz. The PL signal was collected from the incident side with an optical fiber probe and was fed to the VIS-NIR spectrometer. Figure 3.3.4 shows the detailed measurement setup.

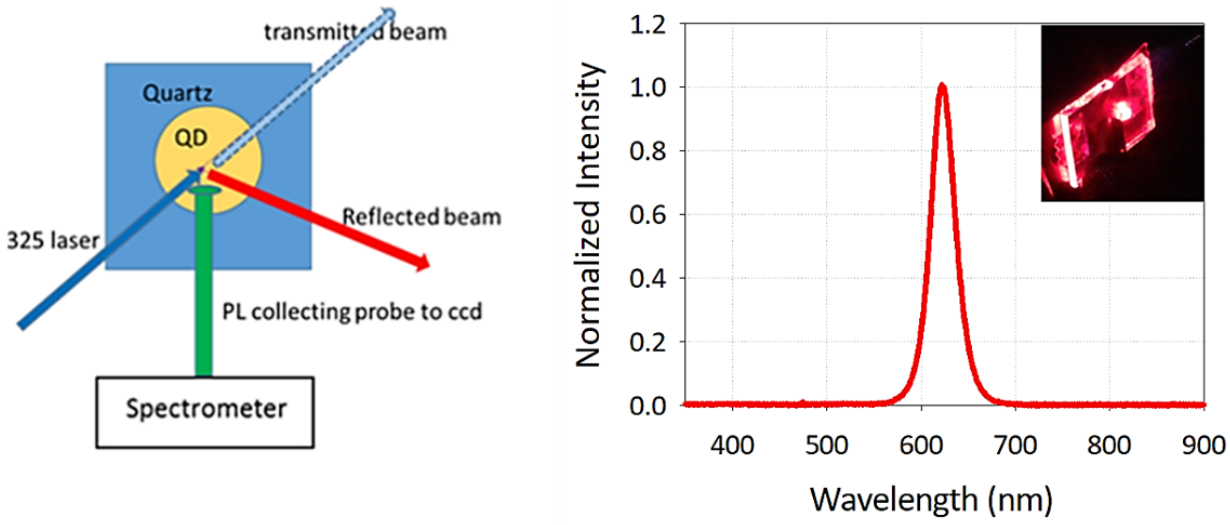

Figure 3.3.4: (left) PL measurement setup for CdSe QD. (right) PL spectrum of CdSe QD, inset shows the digital camera image of photoluminescence

3.4 ORGANIC LIGHT EMITTING DIODE (OLED)

The first breakthrough in organic LED was introduced by Tang and Van Slyke [1] showing its potential to be used as an efficient light source for flat-panel displays. Thereafter numerous research has been done and the OLED is being industrially used in cameras, cellular phones, televisions and other display devices. The advantages of OLED over existing light-emitting devices are: it is a thin (few hundreds of nm) and lightweight structure, it has a fast response rate (~100ns) [73], a wide viewing angle and high-power efficiency [74]. In its minimal form, an OLED is made with an organic material sandwiched between an anode and a cathode with favorable work functions. However, in such devices electron and hole injection, transport, exciton formation and radiative emission- all occur in a single organic material. Generally an organic material is suitable for only one or two of these purposes, for example, depending on homo and lumo level, an organic

polymer can be either electron-carrier or hole-carrier material. Therefore, in order to achieve a more efficient OLED, different materials are used to serve different purposes. In the figure 3.4.1 the band diagram of Tang's OLED is shown. The OLED consists of Diamine as the hole injection layer and Alq_3 as the electron injection layer, as well as emissive material. The HOMO level of Diamine is closer to the work function of the anode; therefore, holes can be injected easily into this layer. On the other hand, the LUMO of Alq_3 is closer to cathode work function enabling an easier route for electron injection and transportation. Here, exciton forms at the interface of HTL and ETL due to the barrier of electron and hole transport after this limit. These excitons recombine radiatively in a few nm distances inside Alq_3 from the interface.

In an OLED stack, the contact barrier between electrodes and the organic layer have a significant influence on charge injection. Instead of depending entirely on the work function difference between the metal and organic transport layer, the polymer-metal interface is also affected by dipole charge created at the interface. Dipoles can be created in different ways depending on the nature of organic materials. In case of weakly interacting metal/organic interface, dipoles originate from direct charge transfer between metal and organic molecules due to chemical interaction [75]. The induced interface states can pin the Fermi level relative to the organic material's HOMO and LUMO level. The dipoles can also form effectively in the case of physio-absorbed chemicals on the metal surface. In close proximity, the electrons or holes from polymers are attracted towards the metal by their image charges [76]. As a result, at the contact point with metal, the vacuum level shifts (VLS) as shown in figure 3.4.2. The VLS can change the carrier injection barrier height as large as 1 eV that can have a significant effect on OLED efficiency [77]. In our proposed OLED device, we replaced the metal electrode with a semiconductor and due to the relatively inert interface nature between semiconductor and organic polymer, we expect fewer

dipole charges at the Si/OLED interface. OLED can be composed of many specific layers, each having its purpose in terms of charge transport or charge blocking. In figure 3.4.3, a multilayer structure is shown which consists of an emissive layer sandwiched between n-type and p-type layers. The n-type stack consists of an electron injection layer (EIL) to provide low electron injection barrier from Cathode, an electron transport layer (ETL) having high electron mobility and a hole blocking layer (HBL) having a large valance band offset to confine holes without impeding the electron flow towards the emissive layer. After the emissive layer, similarly p-type layer structure is formed in reverse order for holes, namely electron blocking layer (EBL), hole transporting layer (HTL), hole injection layer (HIL) and anode. Generally, it is not practical to use these many layers due to the inconvenience of deposition and solvent miscibility. Also, some layers can serve more than one purpose, for example, Alq_3 in Tang's OLED serves as an electron transport layer, as well as an emissive layer.

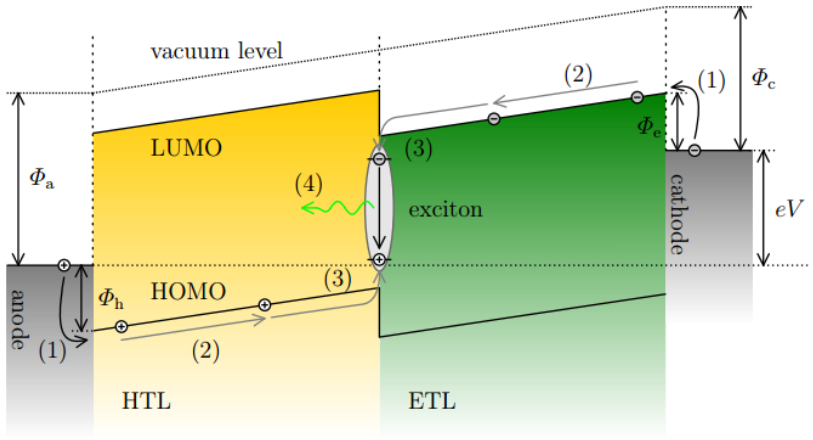

Figure 3.4.1: Energy band diagram and device working principle of OLED fabricated by Tang and Slyke [1].

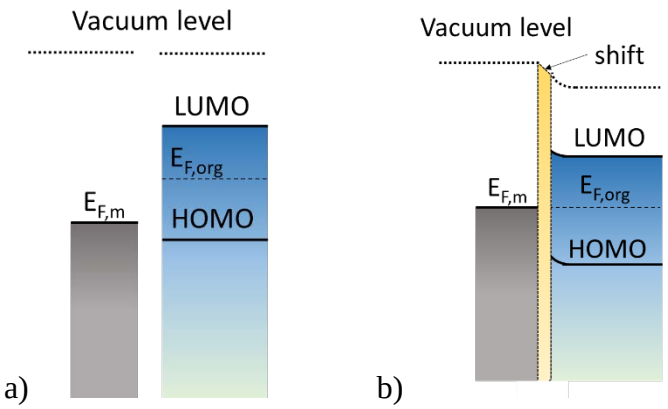

Figure 3.4.2: a) Metal-organic material interface before contact, and b) After contact; a shift in vacuum level occurs due to dipole charges formed at the interface.

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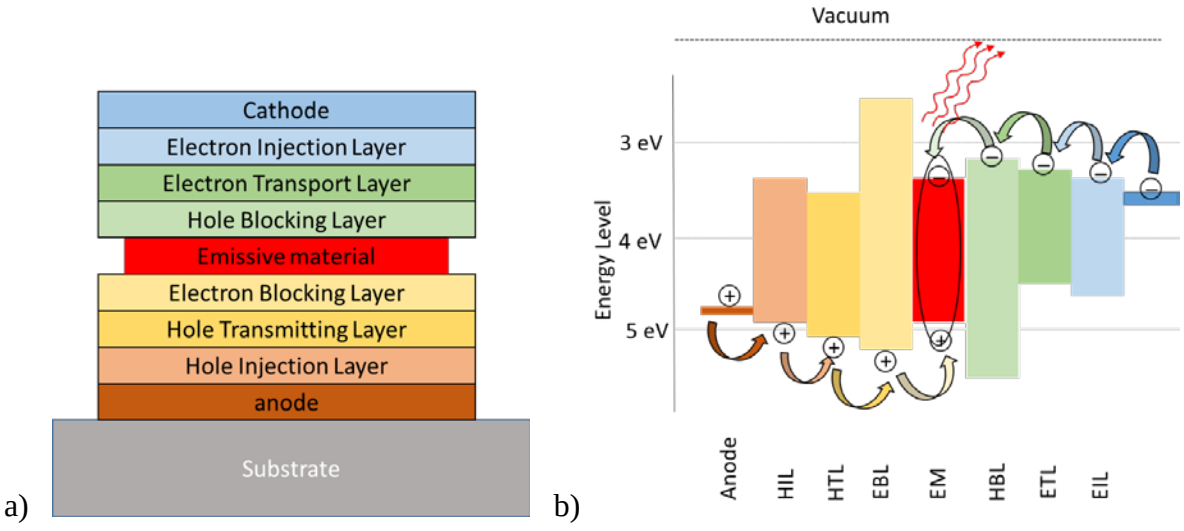

Figure 3.4.3: (a) Multilayer OLED system and (b) energy band diagram of OLED system.

3.5 QD-OLED ON METAL-ELECTRODE-PATTERNED QUARTZ SUBSTRATE

3.5.1 Introduction

Conventional OLEDs are mostly built on an ITO-coated glass substrate with the ITO as the anode (hole supplier). In this study, we have developed an inverted configuration on Al-electrode deposited on a quartz substrate. In this inverted structure (top p and bottom n structure) the bottom Al replaces the ITO substrate of conventional OLED while the top ITO thin film electrode enables top emission. We stacked emissive QD layer, HTL PVK, PEDOT and ITO on top of Al metal layer. The band diagram in figure 3.5.1-e shows that the barrier height for both electron and hole injection is favorably low. The large band gap of ZnS shell layer allows confinement of injected carriers within CdSe core with smaller band gap.

3.5.2 Preparation of hole transport layer (HTL) and electron transport layers (ETL)

The performance and efficiency of OLED depend on the effectiveness of carrier transport layers (TL) as well as carrier blocking layers (BL). In this entire QD OLED study, we have used a different combination of TL and BL layers depending on the active material and substrate used. However, the preparation and spin-coating of any specific organic layer were kept similar throughout the study. Following is a brief process description for preparing organic solutions used in this study:

1) PEDOT: PSS mixture preparation:

PEDOT: PSS solution was purchased from Heraeus, Clevios (TM PH1000) with a specified conductivity of 1000 S. To remove the contaminant and aggregated particles PEDOT was filtered

with 0.45 um filter. To increase the surface adhesion and uniformity of spin-coated PEDOT, a non-ionic Triton X-100 ($C_{14}H_{22}O$ $(C_2H_4O)_n$) was mixed with PEDOT in a volumetric ratio of 0.25%. To mix it well, the solution is ultra-sonicated for 30 minutes.

2) Preparation of PVK solution

PVK was purchased from Sigma Aldrich. To make the PVK solution we mixed 55 mg of PVK with 10 mL of chlorobenzene (1.1 gm/mL). The solution was stirred overnight on a rotating magnet unit. Moreover, before using to fabricate OLED, all the organic solution was stirred for 30 minutes at 70-80^{o}C every time to make sure that any aggregation or solid precipitation was well dissolved.

3) Preparation of poly-TPD solution

Poly-TPD was purchased from American Dye Source Inc. 8 mg poly-TPD was dissolved in 1 ml chlorobenzene. Then it was stirred for several hours in a rotating magnet plate.

4) Preparation of TPBI solution

TPBI was purchased from Sigma Aldrich. 20 mg of TPBI was mixed in 5 ml of methanol and stirred for several hours.

3.5.3 Fabrication of CdSe OLED structure on Al patterned substrate

A process flow of fabricating OLED on metal is described briefly in the following section. All wet processing and baking of the layers were performed in air ambient.

1) Substrate Preparation:

Quartz (0.5mm thick) was cut into a 1cm x 1cm piece. To remove the organic contamination and grease, the sample was cleaned first in acetone and then in methanol for 10 minutes in an ultrasonic bath. After rinsing in DI water, the cleaned sample was blow dried and transferred to a thermal evaporator for Al deposition.

2) Al deposition using a shadow mask:

200 nm Al was deposited by thermal evaporation in 10^{-5} Torr vacuum using a shadow mask. The deposition rate was kept ~2A^{o}/min. (The shadow mask we used was home-made from stainless steel sheet using the following steps: To create the mask, firstly the desired pattern was transferred on 100um thick steel sheet by photolithography. Then the pattern was etched with strong acid using photoresist as an etch mask. This way we were able to create less than 100um pattern window.)

3) CdSe QD spin-coating:

Before spin-coating, the QD container was shaken well without using ultrasonication. The substrate should be thoroughly dried to de-moisturize. 10 uL solution of CdSe was spun on the Al/Quartz sample at 2000 rpm speed for 1 minute. Then the sample was baked in air ambient at 70^{o}C temperature for 30 minutes. The thickness of QD layer is ~20 nm.

4) PVK spin-coating:

Before using, all the polymers were stirred with a magnetic bead at ~70^{o}C for 30 minutes in a closed-cap bottle. After that, 50 uL solution was spun on the QD/Al/Quartz sample at 2000rpm speed for 1 minute, followed by baking for 30 minutes at 120^{o}C in air. The thickness of PVK layer was ~15 nm.

5) PEDOT spin-coating:

50 uL of PEDOT was spun at 2000 rpm for 1 minute followed by baking at 110^{o}C for 40 minutes. The thickness of PEDOT layer was 30 nm.

6) ITO electrode sputter deposition:

The top ITO electrode was deposited using an RF magnetron sputtering unit. A home-made shadow mask (100-um thick stainless steel) was used to define an array of electrode dots of desired dimensions. The sputtering process starts with mounting a source material (sputter target) on an

RF magnetron gun. The sputtering target that we used as ITO source is composed of 90% In_2O_3 and 10% SnO_2, and has a disc shape with a 2-inch diameter and 0.25-inch thickness. To enhance the cooling efficiency and mechanical strength of the target disc, a copper-backing plate was bonded with indium solder. The samples were positioned 2 inches above the target surface, aligned with the source. The chamber was vacuum-pumped to the level of $1x10^{-5}$ Torr or below. Pure Ar gas was then introduced into the chamber to the pressure level of 5 mTorr. While sputtering, Ar gas pressure was kept constant at 5 mTorr and total deposition time was 7 minutes. The RF power was kept constant at 30W and the sample was placed 2" above the center of the target. ITO layer thickness of ~75 nm was measured in Alpha step profiler. Since there was an unavoidable micro gap between shadow mask top-face and the sample surface, ITO thickness at the pattern edge was smaller than the other part. This effect actually imposes a limitation on the minimum opening of shadow mask pattern.

3.5.4 Device optimization

To understand the OLED operation and performance, it is crucial to know how the organic layers are stacked and how carriers are transported through them. Figure 3.5.1(a) shows our OLED device cross section. There are many parameters, such as cathode and anode dimension, organic layers' thickness, emissive materials, transport materials etc. which we can optimize to achieve better luminescence and longer lifetime from OLED. For the Al cathode-based OLED, we varied the cathode spacing and dimension and observed interesting phenomena related to each. We were able to come up with optimization criteria for anode and cathode dimension, based on these observations. However, due to lack of precise control and complicacy of measurement, in this thesis we did not study the thickness or concentration variation effect of organic layers.

From the structure shown in figure 3.5.1(a), together with the energy band diagram shown in figure 3.5.1 (e), we can postulate hole and electron injection mechanism in the quantum dot. Holes are injected from ITO anode and are transported by PEDOT and PVK layer towards the QD layer. On the other side, electrons are injected from Al into the QD. It is noteworthy that in this structure there is no extra electron transport layer or electron injection layer other than Al metal and very thin (1-2nm) native oxide layer that might be formed on it. The holes injected from the p side would not bypass the QD layer if the QD concentration is sufficiently high. We confirmed by SEM imaging that our colloidal QDs are densely packed and have a height of 2-3 monolayers. Once injected into QD the carriers will remain confined due to the large bandgap shell layer of ZnS. The electrons injected from Al electrode will be blocked by the potential barrier at PVK side. The high quantum yield of CdSe QD also facilitates most of the injected electrons and holes to recombine radiatively, rather than accumulating in the active layer. An interesting observation is the current crowding at the periphery of large ITO Anode. Current crowding occurs when the electrical resistance of the vertical path through the stacked layers is much higher than the lateral ITO resistance. In our device, ITO sheet resistance is ~500 Ohm/square where the underlying amorphous organic layers stack, has much lower conductivity. In organic polymers charge mobility is quite low, ranging from 10^{-7}-10^{-4} cm^2/Vs [78], while in ITO film it can go 10-100 cm^2/Vs [79]. During the operation of OLED, the current crowding effect causes the ITO stripe edges to be brighter than the middle region. Figure 3.5.1 (d) shows the effect of current crowding in ITO.

One of the major problems of OLED, especially un-encapsulated and fabricated in non-cleanroom air ambience, is its short lifetime and thermal damage during operation. Thermal damage can be attributed to many electro-chemical processes introduced and/or enhanced by the

pinholes formed in organic layers. When organic layers are processed, any dust particles from the environment or aggregated particles in organic solution can create pinholes between stacked layers. These pinholes provide a pathway for moisture and oxygen to get into the organic layers, which then triggers chemical reactions responsible for degradation of carrier transport and blocking layers [80]. Degradation accelerates during the operation of OLED due to thermal and electrical stress, which would cause degassing of moisture and decomposition of chemicals, creating black spots. Over time these black spots expand and degrade the entire device. Apart from creating a physical barrier from moisture by encapsulation and nitrogen ambient fabrication of OLED, a proposed way to avoid this degradation is to reduce the total area of individual pixels and using multiple miniature pixels to form one pixel. Later in this report (chapter 4), we implement this idea by creating nanoscale OLEDs by non-lithographic nano fabrication.

The use of metal electrodes in OLED further affects OLED efficiency and stability. For example, in our proposed OLED, where the conduction band of CdSe/ZnS QD is quite low (~4 eV), the metal anode needs to have an even lower work function to inject electrons easily. This requirement leads to use of very low work function metals such as Mg, Ca, and Li, which are known to be highly susceptible to oxidation by ambient exposure, affecting the conductivity or even morphology of metal film. As a result, cathode delamination and dark spots formation commonly occur, which significantly reduces OLED lifetime [81,82]. Figure 3.5.1 (c) shows the bubble formation in our metal anode-based device occurring even at lower voltage and short operation time. Apart from damaging issues, the metal electrodes also quench the luminescence of emissive materials in close proximity. Alexander et. al. [83] explained that emissive molecules locating within 10-20 nm distance from a metal electrode transfer their energy to metal and lose

their luminescence property. In the same report, another source of metal proximity quenching is pointed out as the exciton diffusion from luminophore to the metal interface.

As stated earlier, one way to overcome OLED thermal damage is to reduce the effective injection area of OLED and effectively cooling the heated device during injection. The hypothesis is that the reduced junction area devices will have less thermal stress and if they have a way to dissipate heat, the bubble formation can be reduced. Moreover, current crowding is also less severe in case of small area device such as a thin ITO stripe (anode) or Al stripe (cathode) defining OLED injection area. Therefore, we fabricated 200um x 2mm devices, defined by the bottom Al cathode (figure 3.5.2 a). To deposit these thin strips of Al we used a finger type shadow mask made from 100um stainless steel. Figure 3.5.2 also shows I-V data for injection measured by the HP4145B analyzer. From the luminescence image, it is clear that reducing the effective device area improves the brightness and lifetime of OLED.

Due to the mechanical limitation of shadow mask dimension, it is not feasible to produce shadow masks less than 100 μm in our lab. Also, to access the Al electrode we need minimum-size probe pad area. This limitation of bottom electrode scaling is no longer an issue when we fabricate OLED on a silicon substrate with field oxide.

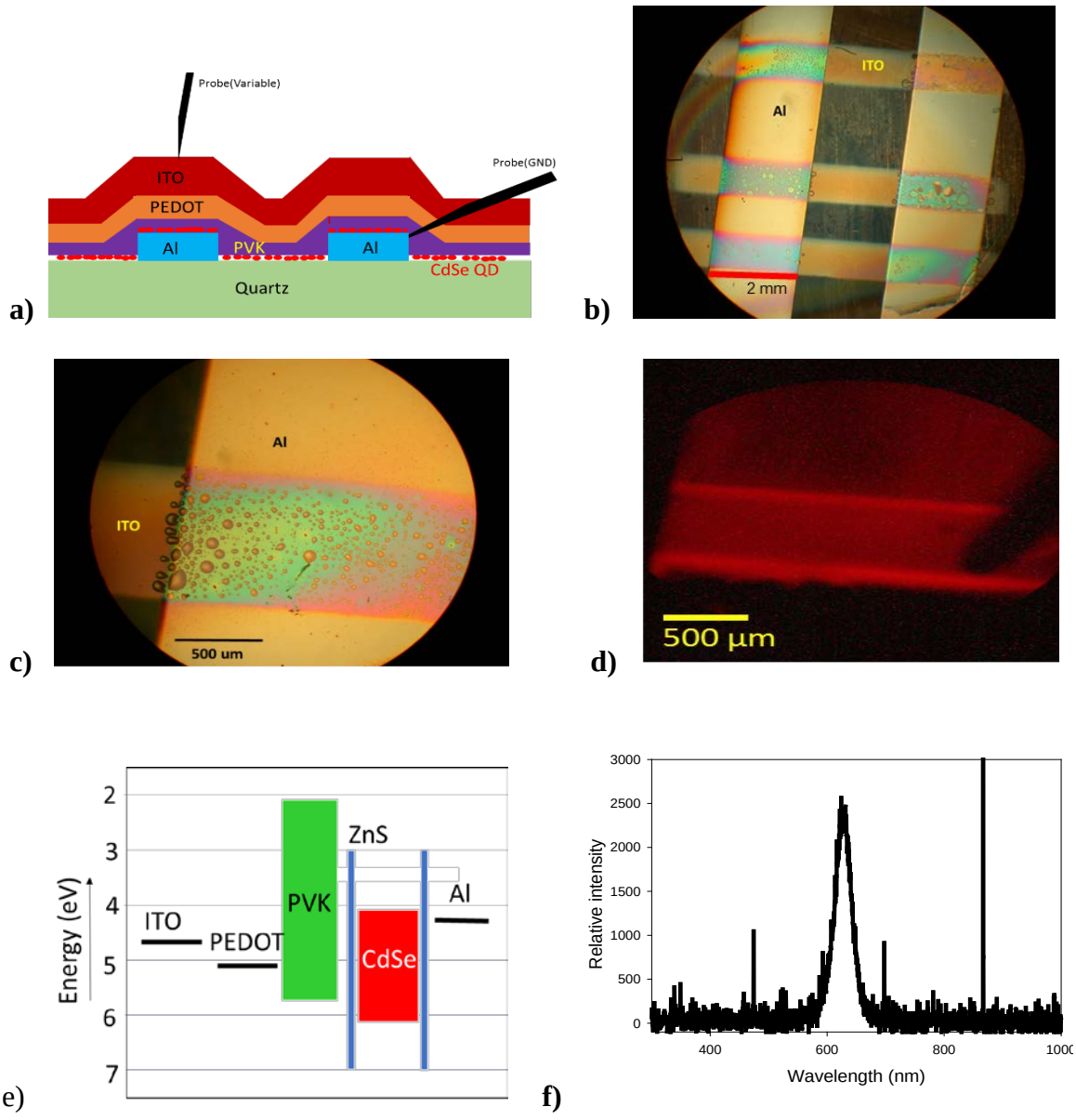

Figure 3.5.1: a) Cross section of OLED structure on metal. This device used highly conductive PEDOT layer treated by ethylene glycol b) Effect of bubble formation during luminescence c) Zoomed image of bubble formation for figure b device d) Effect of current crowding and e) corresponding energy band diagram of the device and f) spectrum measurement for luminescence.

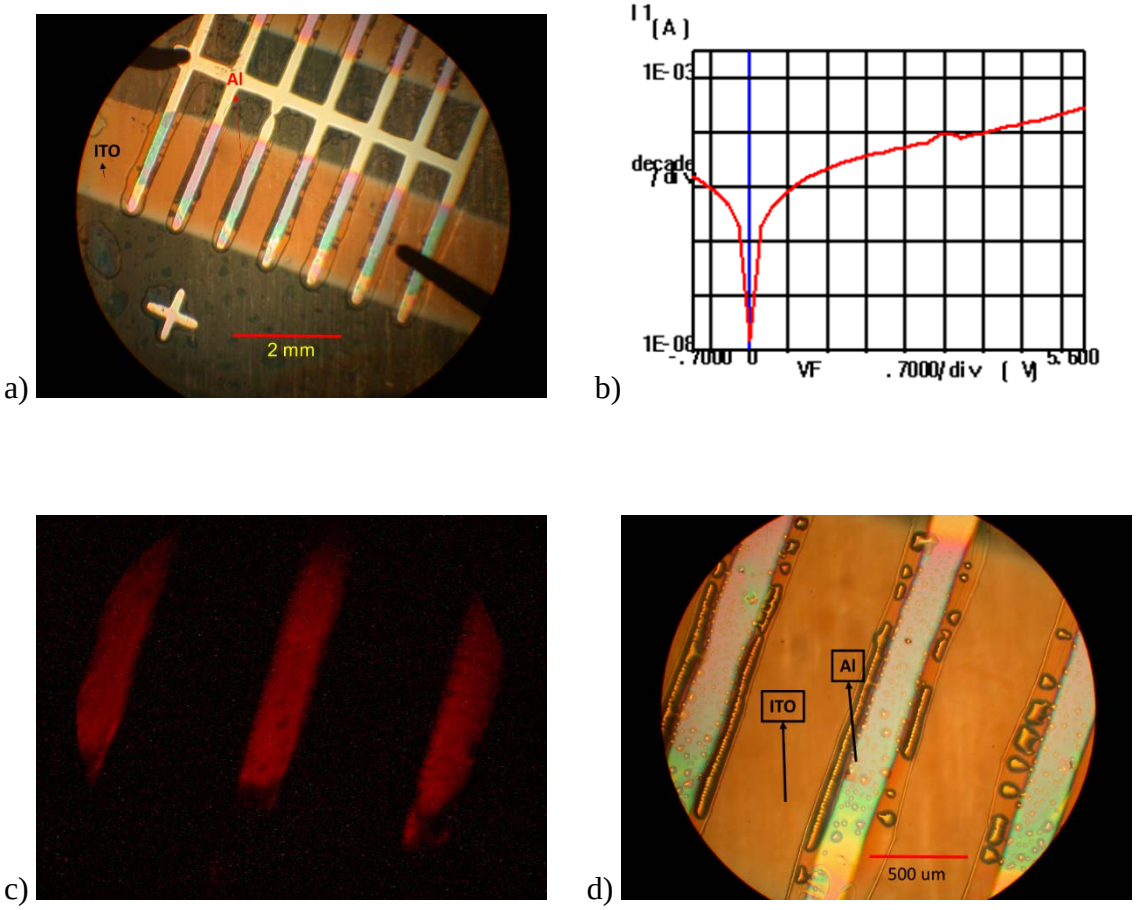

Figure 3.5.2: a) Plan view of OLED having reduced effective device area, b) I-V characteristics, c) luminescence of active devices at 5V and 100 µA injection, and d) corresponding device area after injection.

3.6 QD OLED ON n-SI SUBSTRATE

3.6.1 Introduction

In the previous section, we summarized that down-scaling of the injection area helps to improve OLED performance in terms of stability against degradation. Using a very simple

photolithographic process we can build micron scale devices on silicon with thick oxide. In this configuration, the metal cathode is replaced by bare n-silicon substrate, thus overcoming the adverse effect of low work-function metal cathode degradation described in the previous section. To define the OLED device area and create an isolated OLED array, thermally grown SiO_2 can be utilized as an insulator. By employing a nanolithography technique, OLED dimensions on Si can be reduced to a sub-10nm range. This nanometer-scale OLED structure is expected to find applications in future quantum computing and ultra-high resolution displays. To demonstrate the above idea of Si based OLED, a window etching was performed on 20-nm thick field oxide to reveal bare n-Si substrate. Detailed fabrication and characterization of this device will be discussed in this section.

3.6.2 Device fabrication

For fabricating OLED on n-Si, organic layers were kept similar to OLED on metal described in section 3.3.

1) Wafer cleaning, oxidation, and back side Ohmic contact formation:

We chose an n-Si <100> wafer (phosphorous doped with a resistivity of 5 Ohm.cm). To remove the organic contaminants and grease, the wafer was first cleaned with acetone and then in methanol for 10 minutes each in an ultrasonic bath. The wafer was then rinsed with DI water and went through the RCA cleaning process flow for oxide removal and contamination cleaning. Then the wafer was placed in the oxidation furnace (Thermco.MB-71) which was set to 950^{o}C. According to previous oxidation calibration performed in this furnace, we put the sample inside for 20 minutes to grow a 20-nm oxide layer. Thickness was confirmed by Alpha step profiler.

After the trench fabrication process, the sample was put into the oxidation furnace which was stable at 832^{o}C. Again, according to the previous calibration data, in this temperature, expected 2 nm oxide grows in 1 minute. The thickness was confirmed to be ~2nm by Ellipsometry. After oxidation of silicon substrate, to make an Ohmic contact, a 150-nm-thick Al (Alfa Aesar,5N purity) was deposited by thermal evaporation process at a vacuum of ~10^{-5} Torr. Before Al deposition, the grown oxide on the back side was removed by etching with 6:1 BHF, while protecting the front side oxide layer with a photoresist layer. After Al layer deposition, the front side protective photoresist layer was removed and the specimen was annealed in a furnace at 350 ^{o}C in inert N_2 ambient for 30 minutes.

2) Trench window formation on SiO_2 (23nm)/n-Si/Al:

For down-scaling of our OLED, we created smaller dimension patterns by photolithography. The wafer was cut into 1 square cm pieces. Shipley 1827 photoresist was spun on the samples at 3000 rpm for 30 seconds followed by soft baking at 90^{o}C for 30 minutes. After baking, the sample was exposed in Karl Suss MJB-3 mask aligner in constant power mode, preset at 195 watts for 15 minutes. The exposed sample was then developed in 20% Microposit 391 developer for 2 minutes. To etch the developed photoresist window, BHF (6:1) etchant was applied for 4 minutes. Finally, the photoresist mask was removed by acetone followed by methanol solvent, and thus the substrate was prepared for the stacking organic layer.

3) CdSe QD, PVK, PEDOT coating and ITO deposition:

The process of QD, PVK, PEDOT coating and ITO sputtering are similar to the one described in OLED fabrication on metal in Section 3.3. For one of the devices, we used TPBI as the electron transport layer. TPBI was spin-coated at 2000 rpm speed followed by baking for 1 hour at 50^{o}C.

3.6.3 Working principle

In order to understand the mechanism of carrier transport in the proposed n-Si OLED device, it is crucial to look at its energy-band diagram. Figure 3.6.1(a) shows the cross-section schematic and band diagram for the OLED device. Since the work function of n-Si is very close to Al, the electron injection barrier in Si OLED is expected to be similar to Al OLED, although electronic properties are very different between metal and semiconductor. Our proposed OLED area is defined by patterning the oxide film on Si. Therefore, an MOS type structure is formed in the field oxide region surrounding the OLED [figure 3.6.1-a]. When a forward bias is applied to this structure, a thin sheet of densely populated electrons accumulates at oxide-silicon interface. Apart from bulk injection mechanism, this quasi-two-dimensional electron gas (2 DEG) promotes an interesting injection phenomenon, which will be discussed in this section. Besides the outstanding potential of nm-range scalability, the SiO_2/Si substrate offers an interesting mechanism of carrier injection into the junction area. The OLED structure, when formed on SiO_2/Si substrate, can be viewed as a metal/oxide/semiconductor (MOS) structure. OLED stacks on field oxide SiO_2/Si interface can harbor a large concentration of 2D electron gas. The accumulation 2DEG formed with forward bias can then serve as electron reservoir/supply that is readily available for injection into an emissive layer through the junction edges. Figure 3.6.1(a) shows the cross section of our proposed OLED device. Figures 3.6.1 (b) and 3.6.1(c) show carrier flow in two different areas of OLED device, the insulating oxide area (outside the window) and the emissive area on Si (within the window) respectively. We can calculate the Fermi level of n-Si from wafer resistivity (5 Ω-cm). The dopant density becomes 9.12 x 10^{14} cm^{-3} considering mobility as 1365 cm^2 /V-s. Therefore, the energy level difference between conduction and Fermi level is around 0.28 eV [kT* ln (10^5)], which sets Fermi level at 4.38 eV. This Fermi position is sufficient to inject electrons effectively

into QD, therefore we did not use any electron transport layer. Since we carried out the fabrication process in air ambience, there might be an intermediate native oxide interface with ~1nm thickness. This interface oxide may help to block hole spill-over to Si substrate. The large bandgap of ZnS shell layer, together with thin native silicon dioxide, inhibits holes from passing into Si from p-type layers. The QD emissive layer will also prevent any hole from bypassing if the QD concentration is sufficiently high, fully covering the silicon surface. PVK (20 nm) is used as a hole transport layer as well as an electron-blocking layer due to its low HOMO and high LUMO level. PEDOT: PSS (30 nm) is used as a buffer layer to increase anode work function from 4.7 eV (ITO) to 5.2 eV and also to reduce surface damage by sputtered ITO film (70 nm) [85]. Once injected into the QDs the carriers will remain confined due to the large-bandgap shell layer of ZnS. The 2-nm ZnS shell surrounding the CdSe core also passivates the surface defects. The high quantum yield of CdSe/ZnS QD facilitates most of the injected electrons and holes to recombine radiatively. However, to improve efficiency and to balance the carrier injection, later in this paper we also have investigated/compared an OLED structure with a TPBi electron-transport layer.

It should be noted that the OLED structure in the field oxide area resembles an MOS capacitor structure (Figure 3.6.2 (a)). We already have discussed the 2D electron gas formation in MOS case in chapter 2. In Srisonphan et al.'s work [7], it is shown that under ambient conditions, 2D electron gas accumulated at the interface between oxide and semiconductor, reduces the energy barrier for electron emission and leads to a high emission current density of 10^5 A/cm^2 under only 1 V bias. They fabricated a vertical channel etched into MOS substrate and proved that electron gas is ballistically transported through the edges of the channel due to coulomb repulsion from the electron reservoir. In the same paper, they showed that the channel current is proportional to the perimeter of the well, due to the fact that electron transports through the edges only. A similar

behavior is expected with our OLED structure: The SiO_2/Si interface in the field oxide area under ITO electrode will accumulate 2DEG at forward bias, which will emit at the edge into the adjacent layer (i.e., the QD emissive layer) (Figure 3.6.1-c). Although in the present OLED device structure, instead of the vacuum channel, the trench area is filled with stacked organic layers, still the edge transport concept will be quite valid due to a large number of accumulation electrons near the trench region. Experimentally, we indeed observed edge transport of 2D electron gas in the form of a bright line formed along the edge line of the trenches.

In order to calculate the density of accumulation charges inside Si at Si/SiO_2 interface of proposed OLED, we can follow a similar process as MOS capacitor. In the previous chapter we have discussed charge accumulation in stacked SOS capacitor. We assumed that the accumulation electron density depends on the band bending nature of both semiconductors across the oxide layer. In a similar way in the case of Si-OLED, flat band voltage, surface potential, and threshold voltage all will depend on the nature of band bending in organic polymer layers. The theoretical modeling of Si-OLED band bending is beyond the scope of this thesis. We simply assumed the OLED will behave in a similar way to the MOS capacitor in terms of 2D electron gas accumulation and injection towards the QD layer.

3.6.4 Result and discussion

We have optimized our OLED on n-Si in several steps. All these steps reveal important information regarding carrier injection mechanism; therefore are discussed in this section. At first, we fabricated a trench area of a 100um square with 100 um of spacing. The plan view of the device, luminescence image, spectrum and I-V measurement is shown in figure 3.6.3. For spectrum measurement, we simply collected the emitted light using an optical fiber probe and fed it to VIS-

NIR spectrometer. For I-V measurement we used an HP4145B semiconductor analyzer. In the EL emission, although we can observe bright red luminescence (figure 3.6.3(c)), the device area gets damaged as soon as injection begins, due to heating and bubble formation (figure 3.6.3(d)).

To address the issue of the short lifetime of n-Si based OLED, we decreased the device area to 20 μm square and put a passivation layer of 2 nm thermally grown oxide between the n-Si cathode and organic layers (figure 3.6.3). The motivation of reducing device area is to facilitate efficient thermal cooling and increase perimeter-to-area ratio for enhanced 2DEG injection. However, growing a 2 nm oxide layer not only passivates the bare n-Si surface but also has the effect of promoting 2D electron gas formation in the window area. A thin (tunnel) oxide layer introduced in between an active layer and n-Si substrate will also have the effect of blocking the holes transported from the p-type organic layers. Moreover, H. H. Kim [4] showed that carrier injection from Si electrode into the emissive layer of OLED is greatly improved by an intermediate thin oxide layer, because voltage drop can occur mostly across the oxide layer and the Fermi level of Si can be aligned to the LUMO level of emissive material. Since, in our proposed Si-OLED, the conduction band of the luminescent material is already aligned to n-Si Fermi level and also because of the large bandgap of ZnS shell layer surrounding CdSe quantum dot, growing an intermediate oxide layer is not a critical requirement. Moreover, as the oxide thickness grows, the operating voltage of OLED is expected to rise due to voltage drop in the oxide layer. Therefore, later devices only have a thin native oxide layer (~1nm) on the Si surface. Figure 3.6.4 shows the schematic, electroluminescence image and I-V characteristics of the proposed OLED device on the 2nm oxide layer. Figure 3.6.4(c) reveals an interesting feature of ring-shaped luminescence, providing very strong evidence of edge transport of 2D electron gas. Since the camera shutter was kept open for a long time (8s), weak luminescence from bulk n-Si also shows bright red luminescence. However,

the center of the hole still remains dark, indicating almost no carrier is injected from the center. This diagram showing the donut shape of luminescence suggests that, as we are getting away from the trench edges into the device, 2D electron gas injection by Columbic repulsion is becoming weaker. Therefore, at the same bias voltage, luminescence brightness is monotonically decreasing from edge to center. Regarding the lifetime, this device was tested at elevated bias (20V) for several minutes, and it did not show any degradation or thermal heating damage. However, since the edge was very brightly emitting, indicative of the high density of carrier injection, we expected thermal degradation in the form of a bubble will appear at the trench edges. But surprisingly the edge region remains very stable and degradation-free, even after a long time of high voltage injection at 20V. This observation suggests that 2D electron gas injected into the active layer has a higher efficiency (than bulk injected electrons) to generate photons, instead of recombining non-radiatively producing heat and thermal degradation. Figure 3.6.4 (e) plots log I vs log V at forward bias, showing a slope of 4 at a higher voltage where the device is switched on. 3.6.4 (f) shows the emission spectrum where CdSe emission at ~627nm is the prominent peak.

Since we observed strong and robust 2D electron gas injection along the edges of trenched OLEDs, as a next step we wanted to maximize the edge area, as well as leaving enough spacing between two rings to promote 2D electron gas formation. We fabricated a ring pattern (50-μm ring width and 500-μm inner diameter) of windows etched into an oxide layer (Figure 3.6.5). (This time there was no oxide layer grown on the device window other than a native oxide layer from ambient fabrication process). This ring trench pattern provides two edges (inner and outer sides) and was chosen in order to test/avoid any ambiguity that may arise, related to an oxide/Si step effect on lateral conduction or a spin-coating process induced non-uniformity. When we start injection, the device turns on and emits visually detectable luminescence at less than 5V. To capture a digital

image at relatively short integration time (0.5s) we went up to 12V bias. At 12V pulsed-injection, short exposure time captures the brightest emission region, which appears in this device as the circle along the edges (Figure 3.6.5(b)). But increasing the exposure time to 8s reveals that the other bulk device area also emits light, although less bright than the edge lines (Figure 3.6.5(d)). The bright circles along both the inner and outer edges of the ring trench strongly suggest quasi-one-dimensional emission induced by 2DEG injection. Regarding the lifetime, this device was tested at elevated bias (20V) for several minutes and it did not show any degradation or thermal damage. Since the edge was very brightly-emitting, we expected that thermal degradation might appear at the trench edges. But surprisingly and interestingly the edge region remains very stable and degradation-free, even after a long-time operation at large bias voltage (~20V). This observation suggests that direct injection of 2DEG into the active layer has greater efficiency (than bulk area injection of electrons) in generating photons, possibly by minimizing/avoiding the non-radiative recombination processes of injected electrons which would otherwise produce heat, causing thermal degradation. Figure 3.6.5 (e) is the measured electroluminescence spectrum showing an emission peak at 627 nm from CdSe/ZnS QDs.

In the device set shown in Figure 3.6.6, we have fabricated another exploratory device structure to explore other QD luminophores. We spin-coated a layer of blue luminescence graphene quantum dot (GQD) (in IPA solvent, purchased from ACS nano) on the CdSe layer. We also introduced an intermediate electron transport layer named TPBI in between n-Si and CdSe QD. We see quite a few interesting phenomena, such as 2DEG edge emission, only CdSe PL peak appearing in the PL spectrum, and, lastly, the two-stage slope in the log I –log V plot. Since this device structure is more complicated to analyze, in this section we will try to fit some hypothesis with the results. Figures 3.6.6 c and d show similar edge transmission like previous structure of

Figure 3.14. Therefore, in this device also, 2D electron gas is the main process of carrier injection through the edge. In figure 3.6.6 (e) the emission spectrum doesn't show any blue region peak of GQD. It only shows the red emission from CdSe. This suggests electrons don't recombine at GQD, rather it produces strong emission at CdSe QD. The reason can be the higher energy bandgap of GQD. Presence of an electron transport layer (TPBI) also has the effect of blocking the holes injected from the p-side and confining them into QD layers.

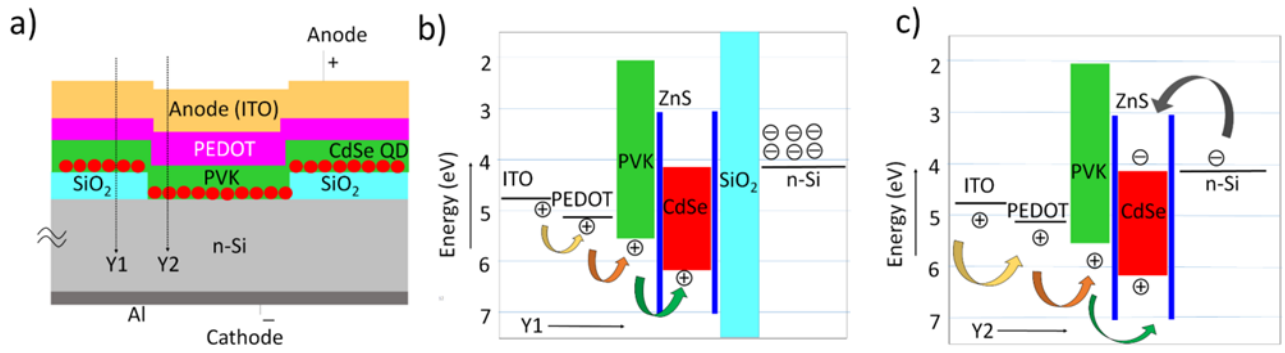

Figure 3.6.1: Proposed QD-OLED device structure on Si substrate (a), band diagram in the field oxide area (b), and band diagram in the active device area (c).

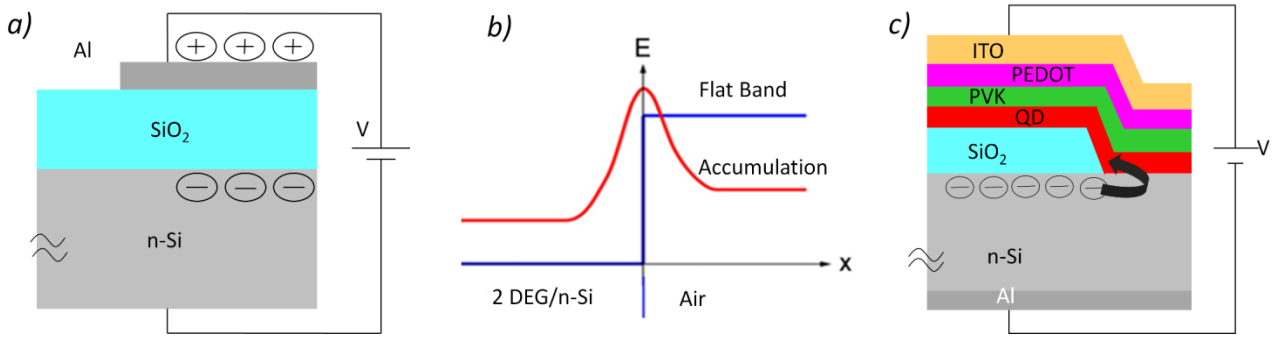

Figure 3.6.2: (a) 2DEG formation in an MOS capacitor structure, (b) energy barrier lowering as a result of Coloumbic repulsion between 2DEG at the edge, and (c) 2DEG injection into the emissive layer (QD) at forward bias.

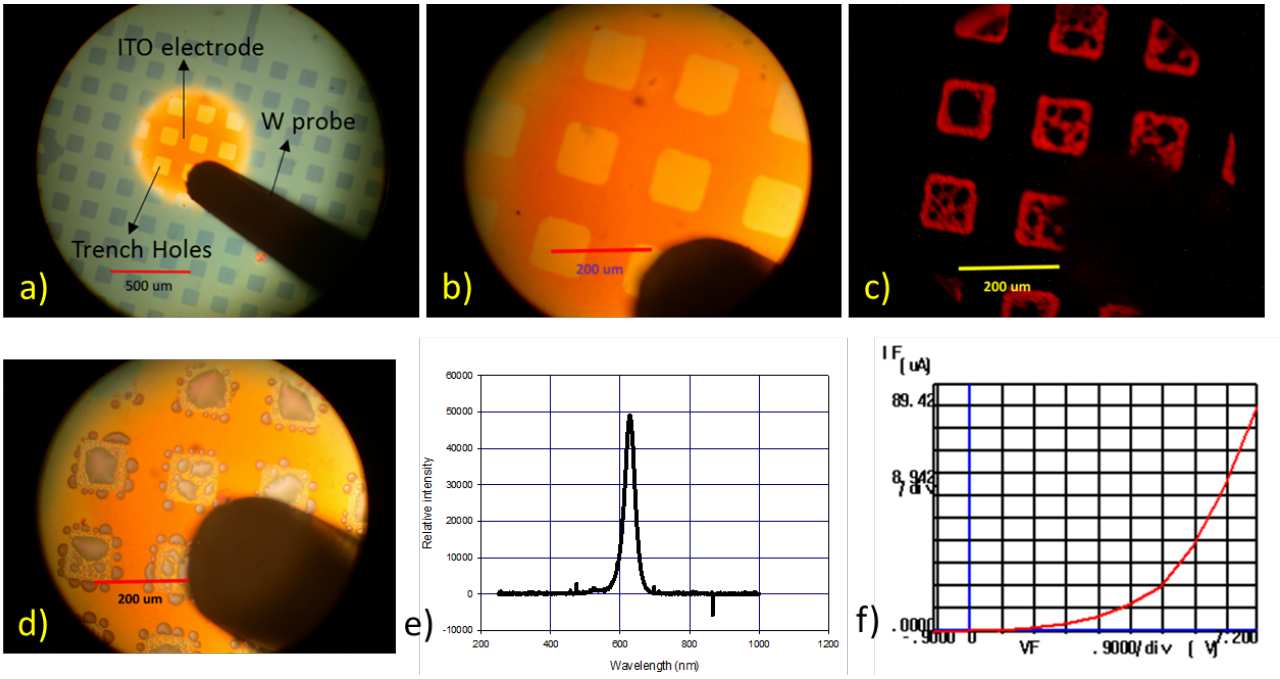

Figure 3.6.3: Bubble formation and injection damage on n-Si based OLED structure: a) plan view of ITO electrode deposited on OLED where square wells indicate trenched windows of SiO2(20 nm)/n-Si. Here trench width is 100um and spacing is also 100um. b) Device area before electron injection started c) Digital image of lamination during 8 V pulsed injection (15 s shutter opening) and d) Injection induced damage and bubble formation; it is clear that bubble forming places shows dark spots during the lamination. e) The emission spectrum of luminescence and f) I-V characteristic for luminescence.

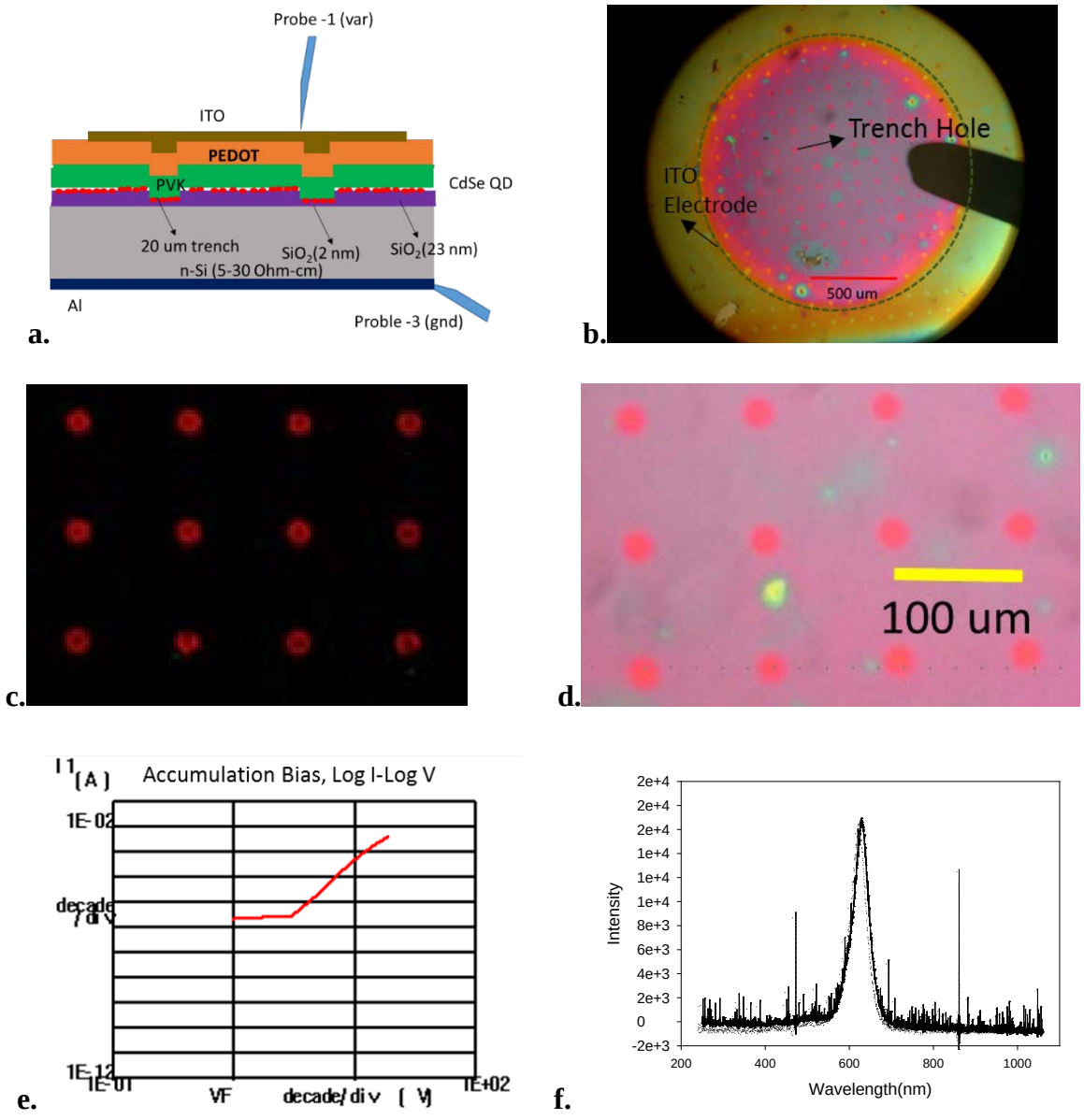

Figure 3.6.4: Effect of scaling down device area and creating thin oxide passivation layer on n-Si based OLED structure a) cross-section of device b) plan view of ITO electrode deposited on OLED where holes indicate trenched windows of SiO2(20 nm) /n-Si. Here trench width is 20um and spacing is 100um. c) Luminescence image at 12V pulsed injection (8s shutter opening). d) Undamaged device area even after high injection. e) I-V characteristic for 10V bias injection. And f) Emission spectrum of luminescence**.**

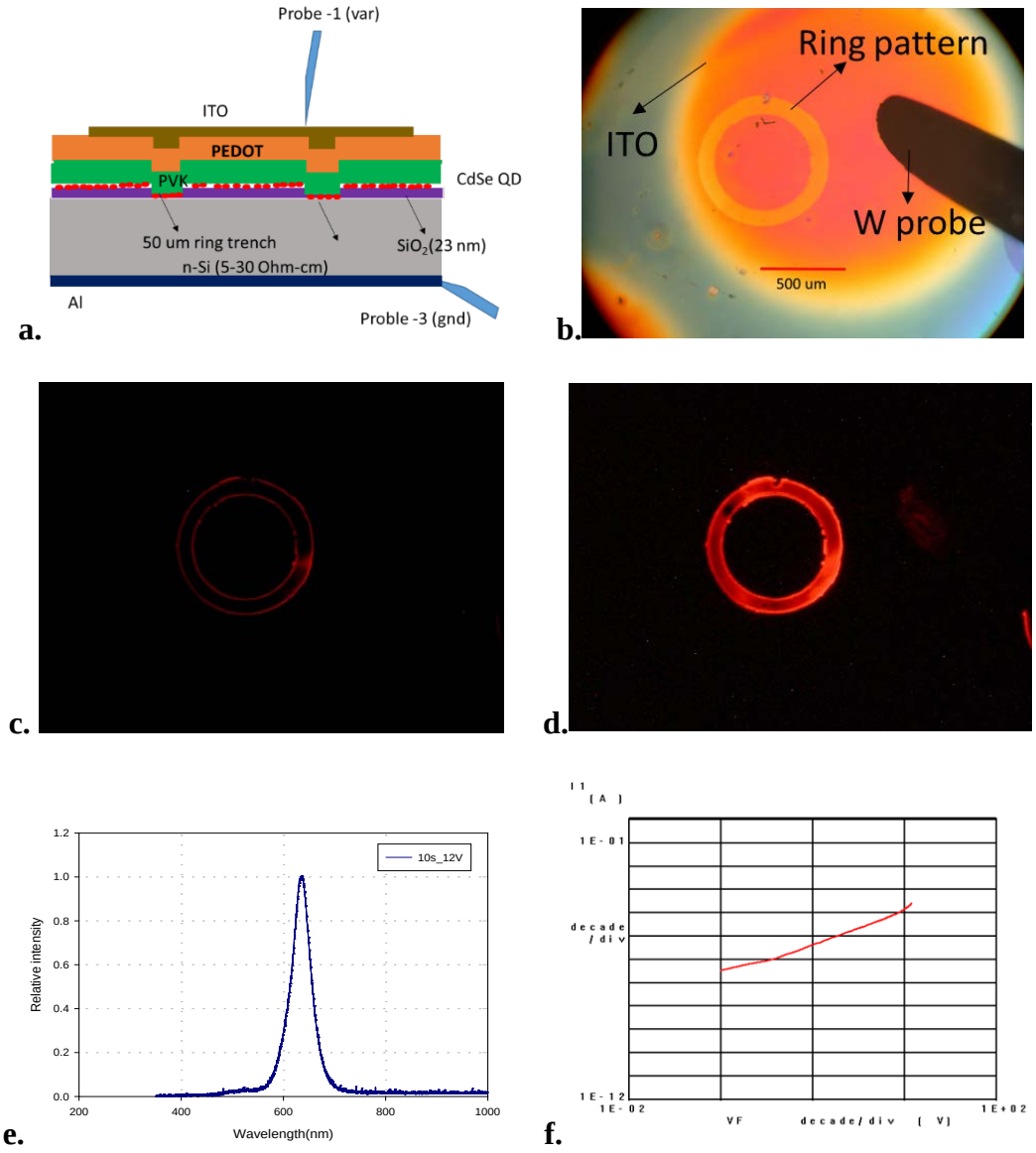

Figure 3.6.5: Effect of increasing trench edge perimeter by ring shaped pattern. a) cross-section of device b) plan view of ITO electrode deposited on OLED where ring indicates trenched windows of SiO2(20 nm)/n-Si. Here ring width is 50 um and inner diameter 500um. Center to center spacing of Ring pattern is 1.5mm c) Luminescence image at 12V pulsed injection (0.5s shutter opening) d) same bias voltage longer (8s) shutter opening e) Linear I-V characteristic for 10V bias injection. And f) log I vs log V plot showing slope 1.5, indicating space charge limited current transport.

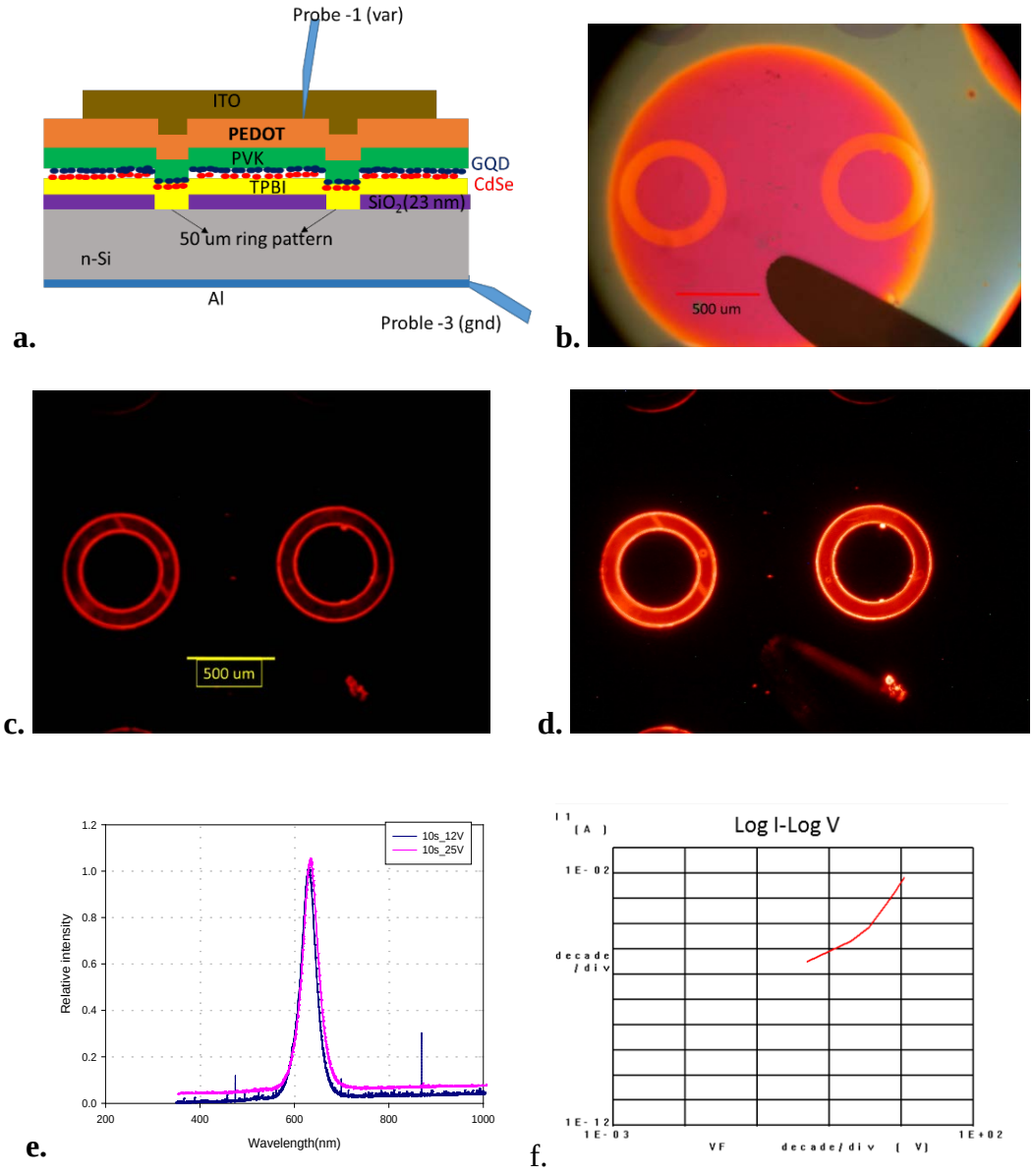

Figure 3.6.6: Applying combined Active material of CdSe, GQD and introducing TPBI between bare –Si and QD; a) cross-section of device b) plan view of ITO electrode deposited on OLED where ring indicates trenched windows of SiO_2(20 nm)/n-Si. Here ring width is 50um and inner diameter 500um. Center to center spacing of Ringpattern is 1.5mm c) Luminescence image at 12V pulsed injection (0.125s shutter opening) d) same bias voltage longer (8s) shutter opening e) Spectrum measurement at 10 and 12 V bias and f) log I vs log V plot at 12 V bias sweep

3.7 SILICON OLED OPTIMIZATION

3.7.1 OLED perimeter dependence

Since we observed strong and robust emission of light along the edges of trenched OLEDs, as a next step we wanted to determine/compare contributions from area injection and perimeter injection of carriers. We patterned circular holes of 20-, 200- and 500-μm diameter on SiO_2/Si substrate by photolithography, and built the proposed OLED structure. The fabrication process is similar to the previously described process. The emission photos of the devices are shown in Figure 3.7.1(a), revealing a strong tendency towards edge emission. A comparison of I-V characteristics of the devices shows that the injection current is proportional to the perimeter of the hole, not the area of the hole (Figure 3.7.1 b). Here we note that the diameter (and perimeter) is scaled up an order of magnitude whereas the area is scaled up 2 orders of magnitude. The current at higher voltage follows perimeter scaling. (The larger current of 20-μm circle at lower bias is not clearly understood yet and is ascribed to non-ideal leakage current). The measured I-V characteristics also reveal relatively low turn-on voltages (1-2 V) of OLED and this can be attributed to low-voltage injection of 2D electron gas at the window edges.

In applications where nanoscale confinement is not a strict requirement (e.g., display LEDs where minimum pixel size requirement is in microscale), we can reduce the non-ideal recombination components resulting from the transport of non-captured holes by introducing an additional electron transport layer (ETL) on Si surface. Adding TPBi, an organic electron transport polymer layer, in between the silicon and QD layer shown in figure

3.7.2 can improve OLED luminescence in two ways. Firstly, bypassed holes from the QD layer would recombine with electrons in the TPBi layer. As a result, high energy photons will emit due to the large bandgap of TPBi (Figure 3.7.2 b) and the adjacent QDs absorb these photons leading to photoluminescence at desired wavelength [86,87]. Secondly, the TPBi layer adds a potential barrier for electrons coming from n-Si towards the QD layer, without which the hole injection rate would be significantly lower than electrons. This way, TPBi creates charge balance at QD and reduces non-radiative recombination. From the emission photo (Figure 3.7.2 c) the edge emission is not as profound as the case without TPBI. Also, the uniformity over large area devices looks better with TPBi. This can be attributed to current spreading, charge balance and passivation of recombination sites adjacent to TPBi layer. However, the I-V characteristics show a strong evidence of perimeter dependence of current rather than area dependence (Figure 3.7.2 d). In nano-OLED fabrication, we have used the OLED structure without any ETL in order to attain a better confinement of emission area.

For display purpose, generally large area of OLEDs is needed. It is well known that large area OLED are more prone to having short life time due to contamination during the fabrication process, pinhole generation, thermal damage, and non-uniformity. In this thesis, we have shown that miniature OLED devices on lithographically-patterned Si are more uniform and brighter than their large area counterpart. We also demonstrated edge injection of 2D electron gas which is formed in insulating oxide area of the device. Now, if we create a large display using arrays of microscale devices separated by SiO_2 insulator, an interesting research question would be the effect of inter-device distance and device diameter on carrier injection and EL intensity. Therefore, we fabricated arrays of microscale OLED having same inter-device spacing with different diameters and also, in a complementary way, same diameter devices with different inter-device

spacing. First, we fabricated arrays of micro LED of 20-, 200- and 500-μm diameter with an edge to edge spacing of 200 μm on SiO_2/Si substrate by photolithography. The actual size of the device is enlarged slightly from the mask, mainly due to optical lithography resolution. The luminescence image is shown in 3.7.3 a-c. For each section, the left side of the figure is the top view photograph and the right side is the EL image at 8V bias. The luminescence and bias current are shown against bias voltage (figure 3.7.3 d and 3.7.3 e respectively). Total device area and perimeter of each array are calculated and presented in the graph legend considering the lowest area and perimeter of 20 μm device array as a unit. The effective device area of 50 μm and 100 μm OLED arrays are ~3.5 and ~9.5 times higher than that of 20 μm OLED arrays, while their perimeters are only ~2 and ~3 times larger. Quite interestingly we observed from the L (luminescence)-V (figure 3.7.3 e) and I-V characteristics (3.7.3 f) that the luminescence and the current changes proportionally with device parameter, not area. This supports our hypothesis that, in the proposed OLED structure, the dominating mechanism of carrier injection into QDs is 2DEG injection at device edges/peripheries. The experimental setup to measure luminescence is shown in 3.7.3-g. (actual measurement was done in a completely dark room with a power meter covering the LED display area). Luminescence was measured from output optical power, voltage, and current data:

$$\text{Externalefficiency} = \frac{\text{number of emitted Photons per second}}{\text{number of injected electrons per second}} \tag{3.28}$$

$$\text{Number of emitted Photons} = \frac{\text{Optical Power}}{\text{photon energy}} \tag{3.29}$$

$$\text{Number of emitted Photons} = \frac{\text{Current}}{1.6\text{E} - 19} \tag{3.30}$$

To measure the luminescence in terms of sensitivity of the human eye, we can express the OLED optical output power in lumens. It is defined that 1 watt of optical power at 555nm wavelength is

equivalent to 683 lumens. The human eye's sensitivity peaks at 555nm, and therefore 555 nm wavelength light is given a photopic luminosity of 1. Our device luminates at 625 nm wavelength, that has a relative photopic luminosity of 0.38 from luminosity graph [88]. Therefore, 1 Watt of Optical power from 625nm wavelength is (683*0.38) =260 lumens;

For uniform and isotropic light source, the luminous intensity in unit of candela(cd) is defined as luminous flux in lumens (lm) per solid angle in steradians (sr):

$$I\ (cd) = \Phi\ (lm) \ / \ \Omega\ (sr) \tag{3.31}$$

We assumed that in our measurement setup we could capture lumen flux in a solid angle of 150^{o} (figure 3.7.3-g), which yields 4.65 sr angle.

3.7.2 OLED spacing effect

To optimize n-Si QD-OLED performance, we fabricated micro OLED pixels of similar diameter but variable spacing. Our initial assumption was that increasing the spacing between OLED channels would allow a higher concentration of 2DEG and the injection current would increase. But from simple calculations, we realized that this effect is prominent only in sub-micron spacing range and may not be visible in micron scale dimensions. Surprisingly, we observed experimentally that increasing spacing in micro-scale dimension, increases the luminescence of Si OLED significantly. This phenomenon can be explained by the accumulation of hole flux in p-layers. P-type polymers, PVK and PEDOT, are located underneath wide area ITO that covers all the pixels universally (figure 3.7.3-d). Therefore, holes are injected universally into the large polymer areas and become accumulated above the oxide. Larger spacing between OLED pixels allows more hole accumulation in polymers, which are driven towards the OLED holes by

diffusion mechanism at the operating bias. Figure 3.7.4 shows the effect of pixel spacing in 50 µm OLEDs. Figure (a) shows the luminescence of 50 µm OLED pixels with spacing of 200, 100 and 50 µm spacing at 6V operating voltage. Figure (b) compares the current density and optical emission power for the devices. The current density of devices with 100 and 200 µm is quite similar, while the luminescence power for 200 µm distance is 2-5 times higher. Therefore, the efficiency also increases as the spacing between OLED pixels increases.

Figure 3.7.5 summarizes the effect of perimeter and spacing on OLED luminescence per device area. It also compares the Si-OLED performance with Al OLED that was discussed in section 3.5. The Si cathode-based OLED shows much better luminescence performance compared with metal cathode-based OLED. However, there is more room for improvement within Si OLEDs by simply changing pixel size and distribution. In terms of device sizes, the smaller OLED gets, the higher its perimeter-to-area ratio becomes which results in better optical performance. On the other hand, as the spacing between OLED pixels increases, the hole flux increases and eventually device efficiency improves. In the luminescence comparison graph, the highest performance is achieved from 20 µm OLED with 200 µm distance, while the poorest performance was observed for 50 µm OLED with 50 µm diameter. This leads us to fabricate a nano scale OLED with large relative spacing to maximize OLED performance.

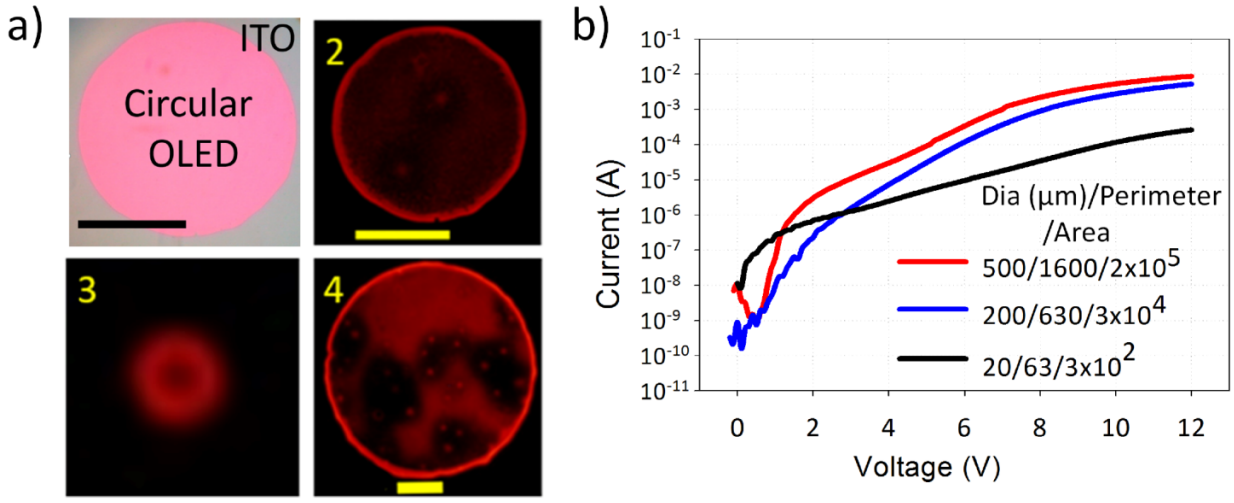

Figure 3.7.1: Circular-window patterned OLEDs: top view (a,1), emission photo at 8V of 200-µm-diameter window (a, 2), 20-µm-diameter window (a, 3) and 500-µm-diameter window (a, 4), and the measured I-V characteristics of these three devices (b). Scale bar is 100 µm.

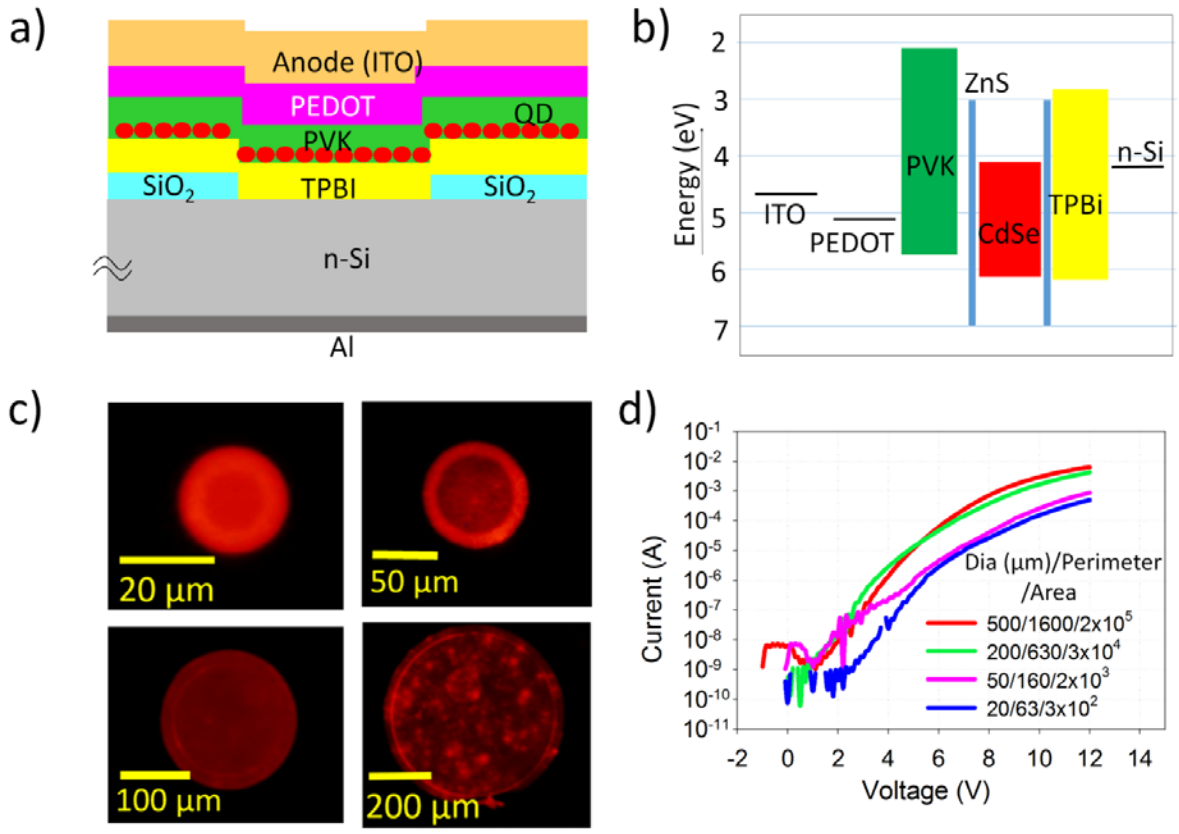

Figure 3.7.2: QD-OLED structure with a TPBi layer (a), energy band diagram of the device (b), emission photos (c), and measured I-V characteristics demonstrating perimeter dependency of carrier injection (d).

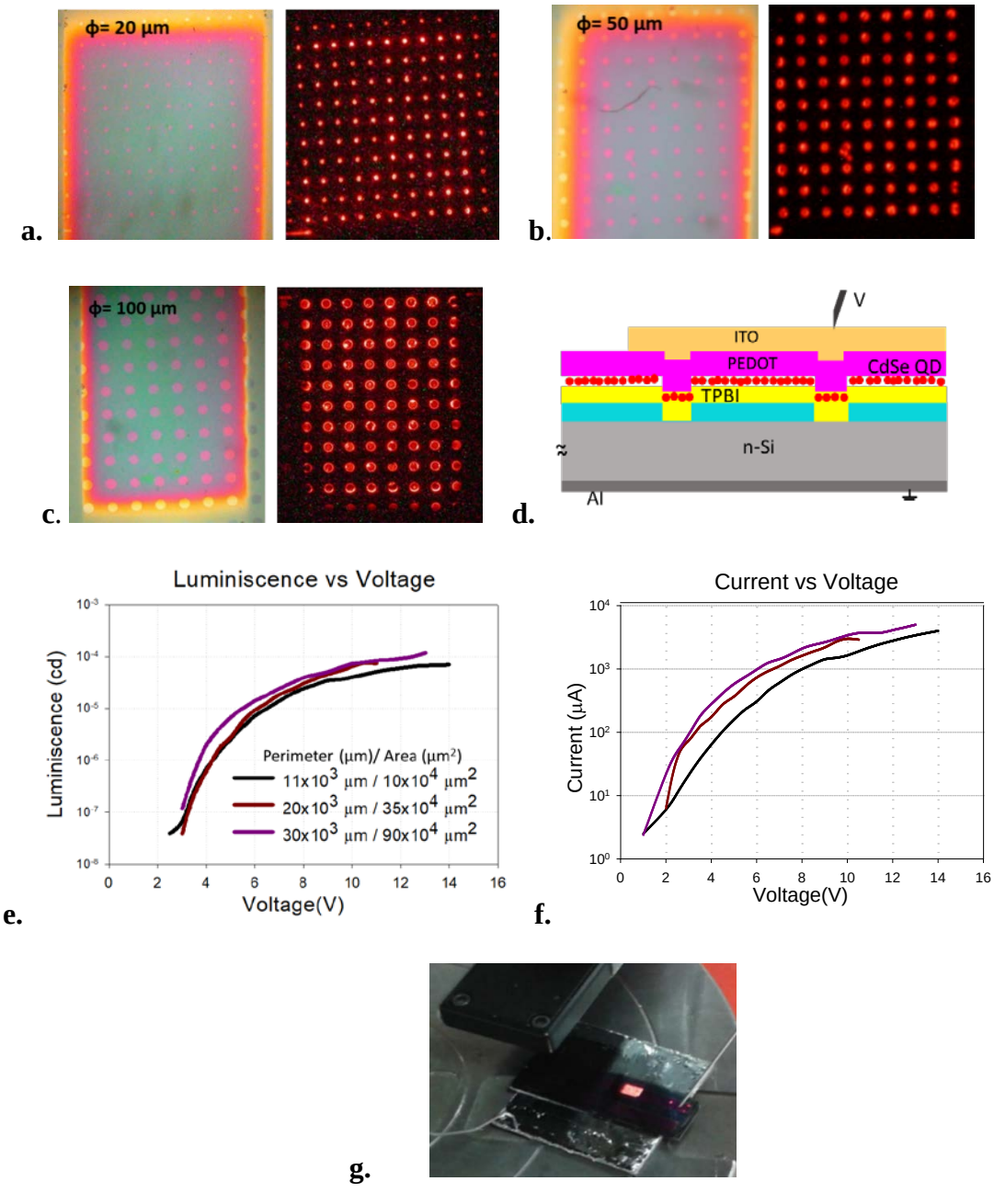

Figure 3.7.3: Luminescence and uniformity comparison of different size LEDs combined with active material of CdSe; For each section, the left side of the figure is the top view photograph and the right side is the EL image at 8V bias. A section of a) 20 um diameter,10x10 dot arrays; b) 50 um diameter, 10x9 arrays; c) 100um diameter, 10x8 arrays; d) cross section of the device e) the luminescence vs voltage and f) the I-V characteristics of OLED devices with different dimensions. g) luminescence measurement setup.

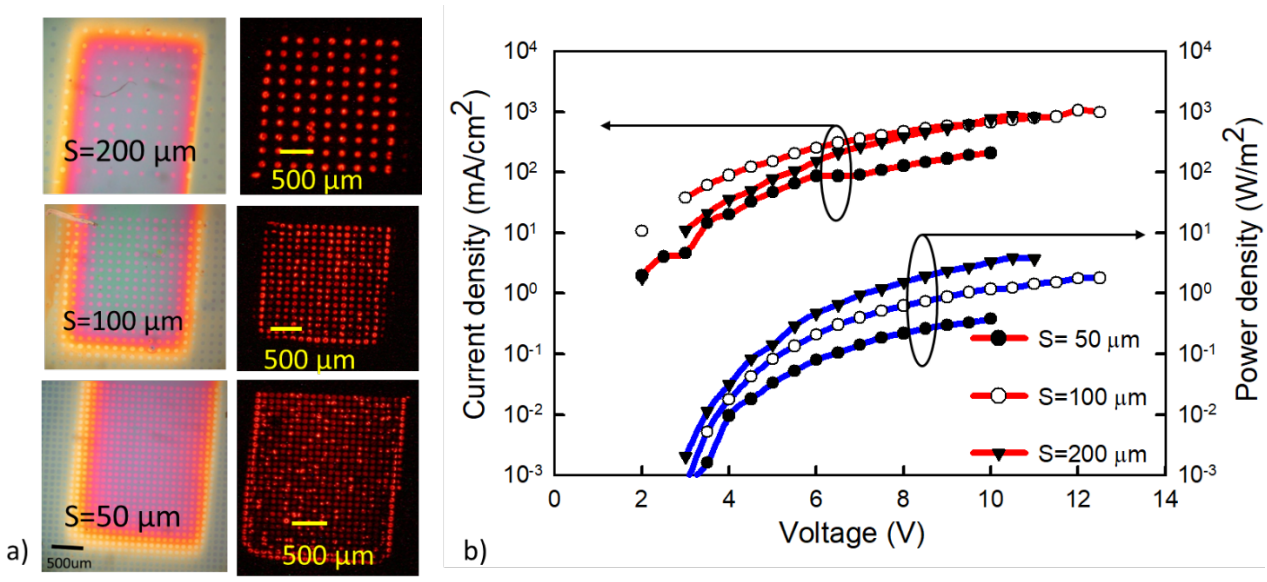

Figure 3.7.4: Spacing effect on current and luminescence between constant sized OLED of 50 µm diameter.

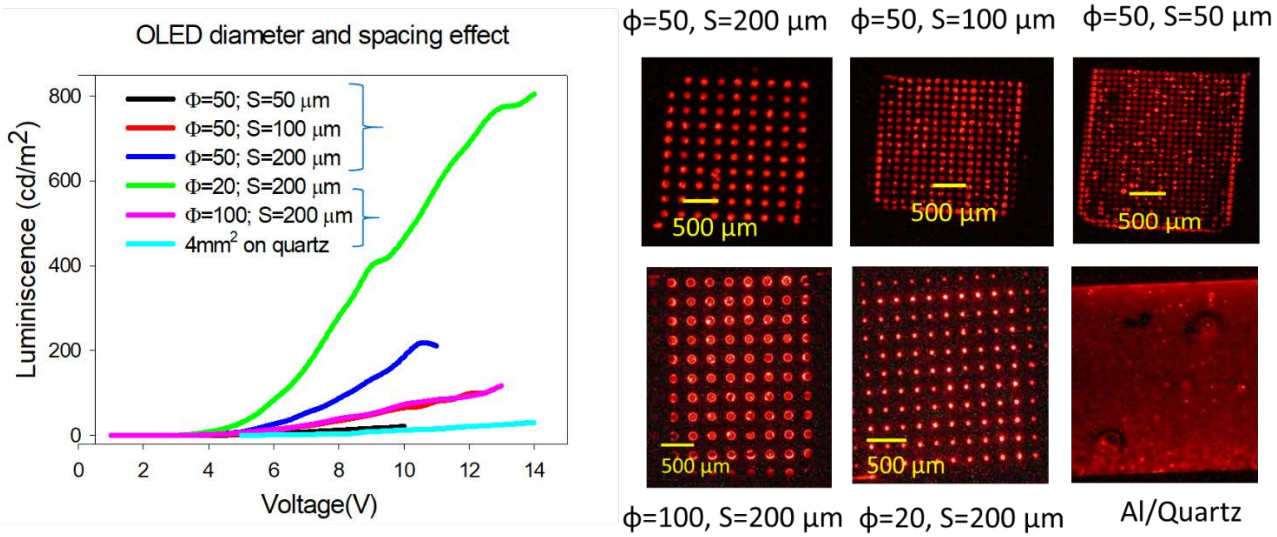

Figure 3.7.5: Overall comparison of perimeter and spacing dependency of OLED luminescence.

4.0 NANO-SCALE QD-OLED ON SILICON FOR SINGLE PHOTON SOURCE DEVELOPMENT

4.1 INTRODUCTION

With the development of quantum information technology, the demand for narrowly confined light sources, which can emit controlled numbers of photon at a predetermined time, has been increased. For example, the basic element of a linear optical quantum computation (LOQC) is a single photon source that can emit regulated and entangled photons on demand [89]. In an effort to generate single photon source, Benson et al. proposed theoretically that an entangled and regulated single photon can be generated from a single quantum dot in a p-i-n diode [90]. Yuan et al. integrated a single quantum dot within a conventional light-emitting diode structure and showed the generation of a single photon at room temperature [91]. However, integrating quantum dot into a semiconductor p-i-n diode is an expensive and complex process. Also, there are significant technological limitations in scaling-down the conventional inorganic semiconductors stemming from their large exciton diffusion length and current spreading nature [92]. These limitations can be addressed by generating nanoscaled p-i-n light-emitting diodes where p and n-type materials consist of organic semiconductors. Due to their inherent low mobility and charge-hopping mechanism, organic polymers are less prone to lateral spreading of current, enabling better confinement. In this section, we scaled down our proposed Si-OLED structure to nanoscale using

conventional EBL lithography, as well as inexpensive nanosphere lithography using gold nanoparticles. For the OLED stack, we utilized our p-layer-only structure without any electron transport or blocking layer. Along with simplicity of fabrication, this device structure reduces device thickness and charge spreading through n-layers. Thus, it helps to confine the recombination zone in desired nanoscale dimension.

4.2 NANO OLED ON SILICON BY ELECTRON BEAM LITHOGRAPHY

As an effort to generate nanoscale OLED in Si platform, we scaled down our devices to 200-nm dimension. We used electron beam lithography (EBL) and reactive-ion-etching (RIE) to create an array of trenches to define OLED dimension. Firstly, a 23-nm thick SiO_2 layer was grown by thermal oxidation on n-type silicon wafers (<100> oriented, phosphorous-doped, 5 Ω-cm resistivity.) On the back side of Si, after etching off thermal oxide by BHF, an Al Ohmic contact was deposited by thermal evaporation (Al thickness, 150 nm). Before e-beam exposure, a thin layer of polymethylmethacrylate (PMMA, ~200nm thickness) was spin cast and annealed on SiO_2/Si surface (Figure 4.2.1). An array of trenches, which are 200nm in width, 200nm in depth and 1mm in length and 20 μm apart from one another, was defined in the PMMA layer using electron-beam lithography (Raith e-Line: 10keV, beam current 220pA). The e-beam patterned substrate was first developed and then etched to 210 nm depth by performing RIE in CF_4/O_2 ambient. Lastly, the PMMA was removed in acetone and the device was ready to fabricate OLED on it. The spacing between adjacent trench lines is 20 μm (Figure 4.2.3a), adequately large in order to clearly visualize individual line emission. Step coverage of organic polymers on the sidewalls of the shallow trenches depends on the surface tension of the liquid polymers, surface adhesion to

the substrate and capillary force of shallow trenches. We developed shallow trenches with the assumption that OLED polymers would cover the step and fill up the trench gaps partially or completely. When tested for electroluminescence, the trench luminescence became visible at 5 V. The photo image presented in Figure 4.2.3(b) was taken at 10 V. The injection current at this bias is ~100 μA as shown in log-log plot in figure 4.2.2(b). A few important observations can be made from the I-V plot and emission image. The OLED current reveals $V^{3/2}$ voltage dependence, which is indicative of Child-Langmuir's space-charge limited current in scattering free environment. This observation is rather surprising because we did not purposely introduce any suspended structure that can allow vacuum injection through the air. A possible explanation is that when the p-type layers were spin-coated on the nanoholes, the polymers could not follow the steep step of 200 nm depth of OLED. Therefore, at the edges of the trench walls, the polymers would be suspended, allowing 2 DEG electrons to be injected from the edges through a vacuum (figure 4.2.2-a). From the emission photo, the 200-nm trench emission seems to appear much broader due to the low resolution of the microscope. Also, the edge or area (trench bottom) emission was not resolved in this photo, due to the microscopy image resolution issue at this scale.

To develop nanoscale OLED, Farhad et. al has fabricated an OLED structure down to 100nm physical dimension by patterning SiO_2 of 300 nm thickness deposited on ITO [92]. They have reported that the PEDOT: PSS layer on ITO induces lateral broadening of the emissive area. Since PEDOT conductivity is relatively higher than the organic transport layers, injected holes diffuse around the device and broaden the emissive area. In our device, such broadening is less likely to occur because QDs are directly in contact with patterned Si area. As we approach nanoscale dimension in our proposed OLED, the perimeter-to-area ratio goes higher. This means almost all the injection will be with 2DEG at the edges, which is believed to be a more efficient

process than the area injection. If we keep shrinking our device diameter, we expect to generate sub-10nm diameter OLEDs containing a single quantum dot. This can be used as a silicon-based single-photon source on demand [93], which is an important optical component in future quantum information technology [94].

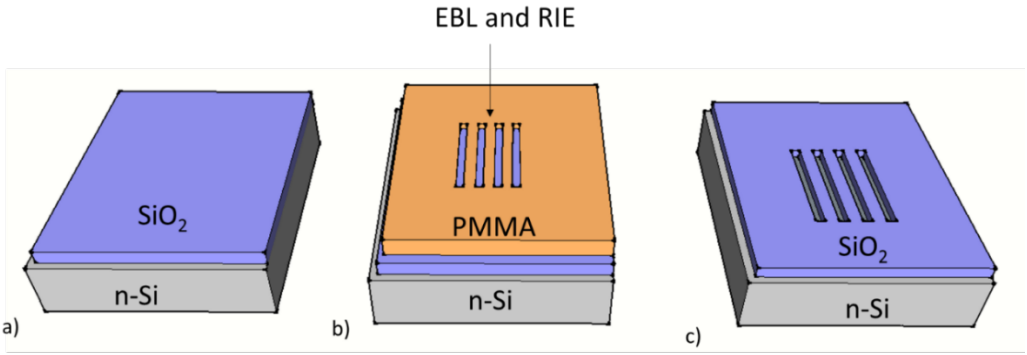

Figure 4.2.1: Nano trench fabrication by EBL method

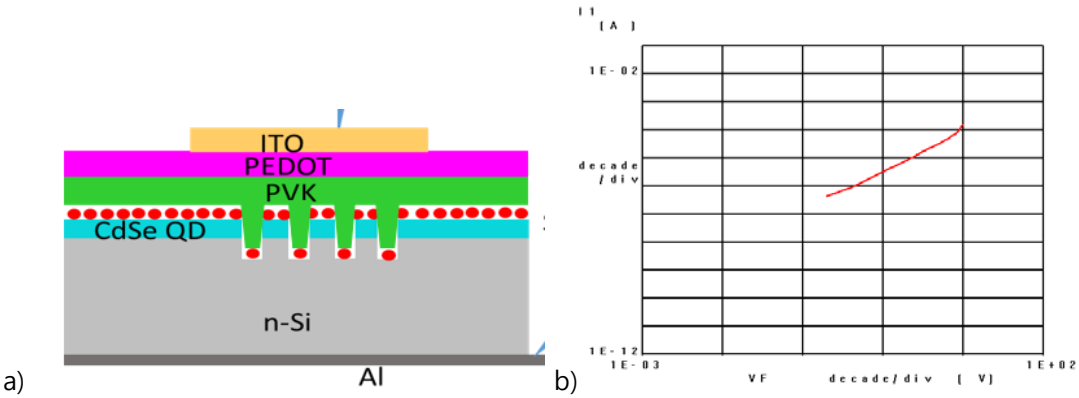

Figure 4.2.2: a) EL testing setup for nanochannel OLED, b) I-V characteristic of forward bias injection in the device

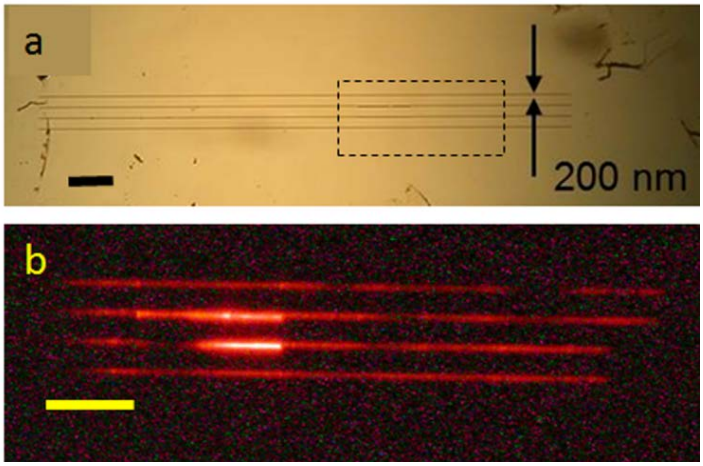

Figure 4.2.3: A micrograph of the trench-patterned SiO_2/Si substrate by electron-beam lithography: 200-nm width and 20-µm spacing (a), a photo image of electroluminescence of trench-patterned QD-OLED at 10V bias (b). Scale bar is 50 µm.

4.3 NANO-SPHERE LITHOGRAPHY: NANOPARTICLE AS OXIDATION MASK

4.3.1 Introduction

Although conventional nanolithography techniques (such as e-beam lithography) can yield well-controlled device position and dimension, the large-scale production of OLED is not considered to be economically practical in this process. We also note that individual addressing of nano-OLED is not a technical requirement in most envisioned applications. For example, one of the major applications of nanoscale OLED would be high-resolution displays in wearable devices and cell phones, where each micro pixel would consist of a few hundred nano-OLEDs. Another application of the nanohole itself would be optoelectronic devices with suspended 2D materials, for example, graphene photodiode where graphene is a suspended cathode on nanoholes formed in a SiO_2/Si structure [12]. In both devices, nanoholes are utilized mainly for their highly-efficient perimeter

(edge) injection of charge carriers rather than their nanometer resolution. Therefore, precise control over the individual hole is not a necessary requirement. These reasons lead us to search for an alternative process to the nanolithography technique for large-scaled and economically viable production of nanoholes.

As a first approach of patterning nano-holes in SiO_2, we covered Si surface with nanoparticles that can block oxygen from reaching underneath Si during high-temperature thermal oxidation. We utilized gold nanoparticles for its oxygen-blocking nature, easy fabrication method and various nanoscale size availability. Among the noble metals, gold is known to provide an effective barrier to oxygen solubility or diffusivity at any temperature. Eberhart et. al. explained this phenomenon by the fact that initially-diffused oxygen strengthens the nearest-neighbor bonds of gold lattice which inhibits interstitial movement of any further oxygen molecules [95]. One of the other candidate metals was silver. But due to its temperature (T) dependent oxygen diffusivity [3E-7 exp(-5560/T) m^2s^{-1}] and solubility [3E-7 exp(-5560/T) mf], silver is unable to block oxygen at high temperature.

The gold nanoparticles (Au-NPs) were introduced to Si substrates in two different ways: high-temperature annealing of gold thin-film and direct spin-coating of commercially available nanoparticles on Si substrate. To create area contact we sank the nanoparticles into Si by employing a metal-assisted chemical etching (MACE) process. Finally, by re-oxidizing the MACE-etched sample we fabricated desired nanoholes and demonstrated electroluminescence of nano-OLEDs.

4.3.2 Fabrication process, result, and discussion

Figure 4.3.1 shows the overall fabrication steps of nanochannel formation. To begin with, we chose n-Si <100> wafer (phosphorous doped with a resistivity of 5 Ohm.cm). To remove the organic contaminants and grease, the wafer was first cleaned with acetone and then with methanol for 10 minutes each in an ultrasonic bath. The wafer was then rinsed with DI water and went through the RCA cleaning process flow for contamination cleaning and a thin surface oxide layer formation. A thin Au film was deposited on this substrate using thermal evaporation. Heating this sample at 350^{o}C for 30 minutes renders nanoparticles/ nano-islands of various sizes and distributions by solid state dewetting (SSD) mechanism [96]. Figure 4.3.3 (top row) shows the resultant nanoparticle distribution for gold film of 5, 10 and 17 nm. As the thickness increases, the nanoparticle size and average spacing increases.

An alternative way to get more controlled particle size and distribution is to spin-coat colloidal solution of gold nanoparticles with a predefined size. The spacing between nanoparticles varies with solution density, generating a denser distribution for denser solutions. We used a citrate-stabilized colloidal solution of gold nanoparticles from Ted Pella Incorporation with a size distribution of 200 nm. At neutral pH, the negatively-charged citrate ions coat each individual gold particle, preventing agglomeration by coulomb repulsion. For the same reason, nanoparticles do not adhere to bare silicon, which also has a negatively-charged surface in water [97]. Jacob et al. proposed a method to overcome this adhesion problem by decreasing pH of NP colloidal solution [98]. At lower pH, for example, at pH of 2, the citrate ions are expected to be converted to neutral citric acid [99]. Based on this principle we mixed concentrated HCl with the NP solution in 1% volumetric ratio. Since the neutralization of citrate ions around a nanoparticle may cause agglomeration, NP solution was spin-coated on Si surface within two minutes after mixing with

acid. After drying at room temperature in air ambience, the NP-coated sample was dipped into DI water for 5 minutes to remove any solution-brought contaminants, followed by nitrogen blow dry.

In the next step, a nanoparticle-coated sample was placed in an oxidation furnace at 950^{o}C in an air ambience for 30 minutes to grow a 25-nm-thick oxide layer. Oxidation of Si surface occurs at Si-SiO_2 interface by the diffusion of oxygen through the oxide layer. Although the gold nanoparticles sitting on Si surface are expected to impede the oxygen diffusion [95], we observed that the growth rate of oxide beneath NPs is only partly reduced. A similar observation was reported by Bowker et al. [96] where he explained this phenomenon with contact nature of nanoparticle on Si: the spherical shape of NP makes only a point contact on Si, allowing oxygen to diffuse through the contact gap (figure. 4.3.2). This process accelerates as the oxide grows, allowing lateral oxygen diffusion. Thus, the nanoparticles float up on the oxide instead of being anchored to the Si surface (figure. 4.3.1- step 2). It is noteworthy that, after contacting Dr. Bowker from the Cardiff University of UK, we confirmed that the gold diffusion is negligible during NP masked oxidation process due to the presence of interface native oxide together with rapidly growing thermal oxide between gold and bulk Si.

From the above explanation and experimental findings, it is obvious that an area contact is necessary to use a gold nanoparticle as an efficient oxidation barrier to Si (figure. 4.3.2). We applied a metal-assisted chemical etching (MACE) process to sink the nanoparticles into a depth of ~100 nm from the surface (figure. 4.3.1- step 3). Our MACE etchant is an aqueous solution of HF and H_2O_2 with a volume ratio of 6% and 1% respectively. During MACE, the gold nanoparticle acts as a catalyzer in the reduction process of H_2O_2 and produces holes (h+) as a byproduct. These holes are injected into the Si valence band to form SiO_2 that is then etched by HF. In this method, a tunnel is produced inside Si with nanoscale diameter of the nanoparticle (NP). The MACE etch

depth was controlled such that a conformal contact between the lower half of NP sphere and Si is formed. It is noteworthy that in our process we did an extra oxidation step before the MACE etching process. We observed that the metal etching direction in our oxidized substrate is strictly vertical to the surface, whereas literature reports a gold-NP MACE process generating an arbitrary etch path on the sample surface [100]. The improved directionality can be explained by the fact that the oxide beneath a nanoparticle was defective/thinner caused by partial oxygen deficiency [96]. The MACE process leaves the bare Si substrate with submerged NPs. In the next step, 25-nm-thick thermal oxide is regrown on this Si sample. During the oxidation, Au-NPs act as an effective oxidation barrier due to area contact (Figure 4.3.1: step 4). Finally, the NPs are removed with aqua regia.

The morphology of finished nanoholes varies with nanoparticle size and MACE etch controllability. Figure 4.3.3 shows the nanoparticle distribution (top row) and resultant nanoholes (bottom row) for NP samples achieved from annealing 5,10 and 17 nm gold film. We can observe that the smaller and densely distributed nanoparticles resulting from the thinner gold film form continuous finger type trenches after MACE etching. This can be explained by the higher surface mobility of smaller nanoparticles during MACE etching. Eventually, individual trench paths merge together and form finger-like trenches. We chose relatively large and well-defined nanoholes formed from 17 nm gold film due to its well-defined hole structure. Figure 4.3.4-a&b shows the cross section and topography SEM image of final nanohole samples. In the SEM images, we can observe some unetched protruded materials besides the nanoholes having similar dimension as nanoparticles. To analyze its material content, we performed EDS (Electron Dispersive Spectroscopy) on both nanoholes and protruded area, and the result is shown in figure 4.3.4 (c) and (d) respectively. The protruded material is found to be composed of Si/SiO_2 and gold, while

the nanohole surface area is purely Si or oxide. The EDS data together with irregular shape of the protruded particles suggests that some nanoparticles get completely buried under Si due to MACE etching and aren't removable by gold etchant after the oxidation process.

We utilized this nanohole sample to fabricate a nanoscale OLED. The fabrication process of OLED stack is the same as described in the previous chapter: spin-coating and annealing of CdSe/ZnS core shell QDs, PVK, and PEDOT consecutively and then sputtering of ITO. A valid concern regarding nano-OLED is whether the polymers follow the steep steps of nanoholes or just become suspended on the holes due to their long polymer chains and high viscosity. Figure 4.3.5(a) shows the SEM image of OLED cross section confirming that the polymer layers indeed coat the nanochannels mostly following their steep steps. Although under a certain diameter limit (<10 nm) the polymers do not fill the nanochannels down to the bottom.

In figure 4.3.6 the structural morphology and electroluminescence of the nano-OLED is shown. Figures a, b and c show the optical microscope and SEM image of the OLED surface. Figure b shows an interesting contrast between nanochannel depth before and after OLED fabrication. The hole depth in the ITO coated sample is significantly less than the original nanohole depth in oxide. There can be two explanations of this feature. The first possibility is that the 70 nm ITO sputter deposition may close the hole openings that are less than 140 nm in diameter by edge deposition along the hole periphery. The second possibility is that the polymers partially fill the hole bottom instead of uniformly coating it. From SEM images in figure 4.3.5-a, the second explanation of hole filling seems applicable in case of larger holes. Figure 4.3.6-c shows the p type polymer layer coating on nanoholes before ITO sputtering. The clear visibility of holes confirms that they are not fully filled with polymers. In short, the viscosity of polymers and shadow effect of sputtering deposition play an important role in the conformal coating of nanoholes in nano-

OLED fabrication. When a voltage is applied, the OLED emits visible emission from 6-7 V and becomes considerably bright at 15-20 V. Since the nanochannel density is quite high, at microscale resolution we expect to see merged luminescence from adjacent holes. The nano-OLEDs are still distinguishable in the electroluminescence micrograph (Figure.4.3.6d) indicating that some of the holes do not participate in luminescence, possibly due to nonconformal ITO coating or due to being buried under Si by non-directional etching at MACE stage. In the former case, the QDs will not receive any carriers and hence there will be no carrier loss. But for the latter case, the emitted light from buried QDs will be blocked or absorbed by the surrounding Si substrate and will decrease the overall external quantum efficiency of OLED. Figure 4.3.6-e shows the I-V measurement data plotted on a log scale. The quadratic dependence of current on the operating voltage indicates that the conduction is limited by space charge-limited current through the organic polymers.

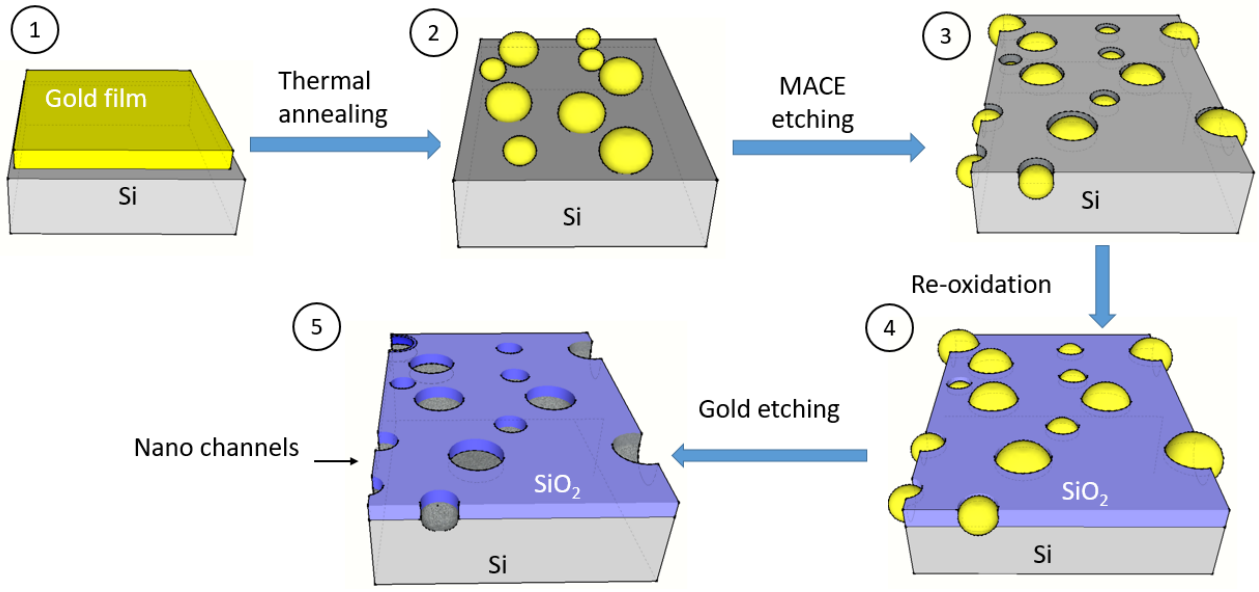

Figure 4.3.1: Process steps in fabricating nanoholes in SiO2/Si substrate: (first step) deposition of thin Au film or NPs on Si, (second) oxidation of Si with lifted nanoparticles, (third) MACE etching of NPs in Si to create area contact, (fourth) re-oxidation and (fifth) etching of Au NPs.

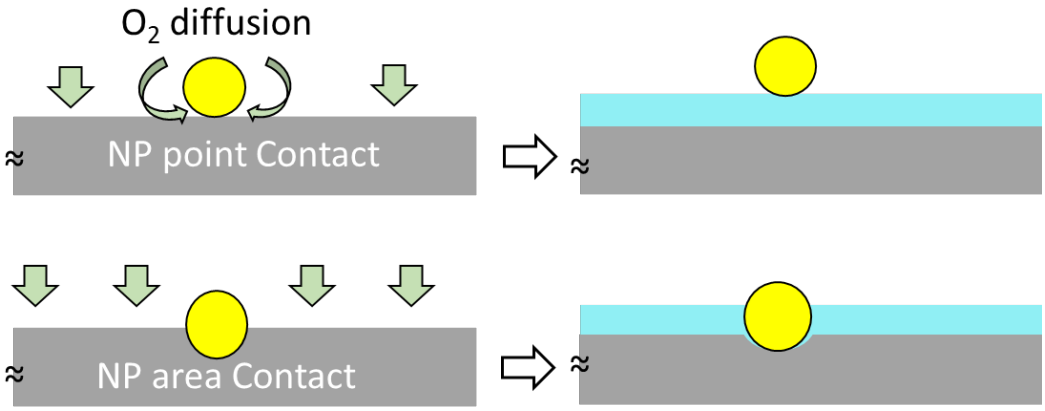

Figure 4.3.2: Advantage of Area contact made with MACE

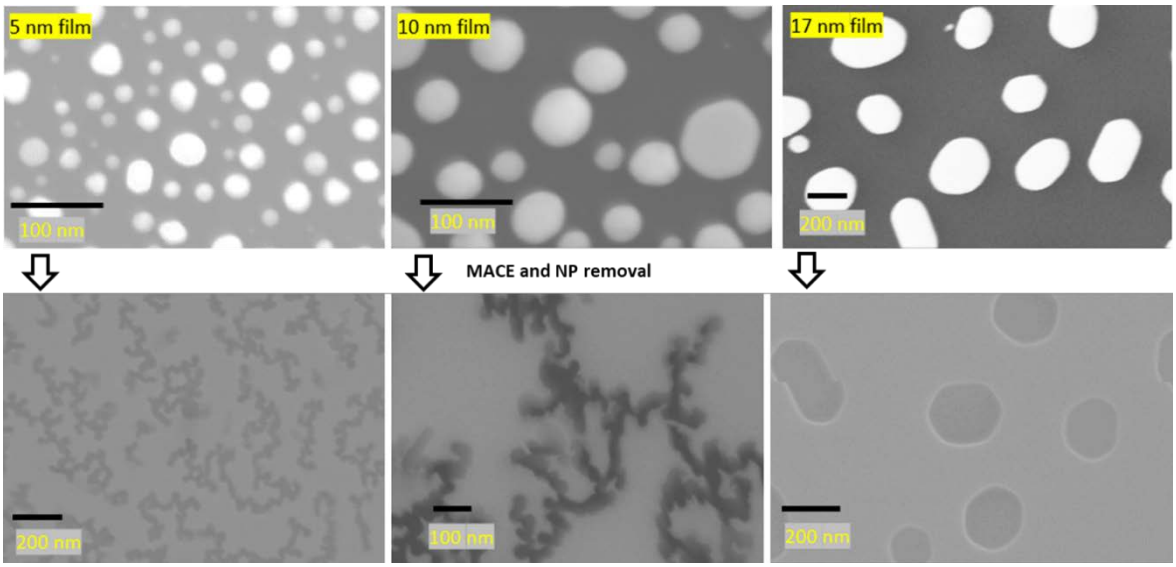

Figure 4.3.3: Effect of gold film thickness on nanoparticle distribution and trench shape. The top row shows nanoparticle formation and the bottom row shows resultant nano-trenches after MACE etching for 5 nm (left), 10 nm (middle), and 17 nm (right) thin films.

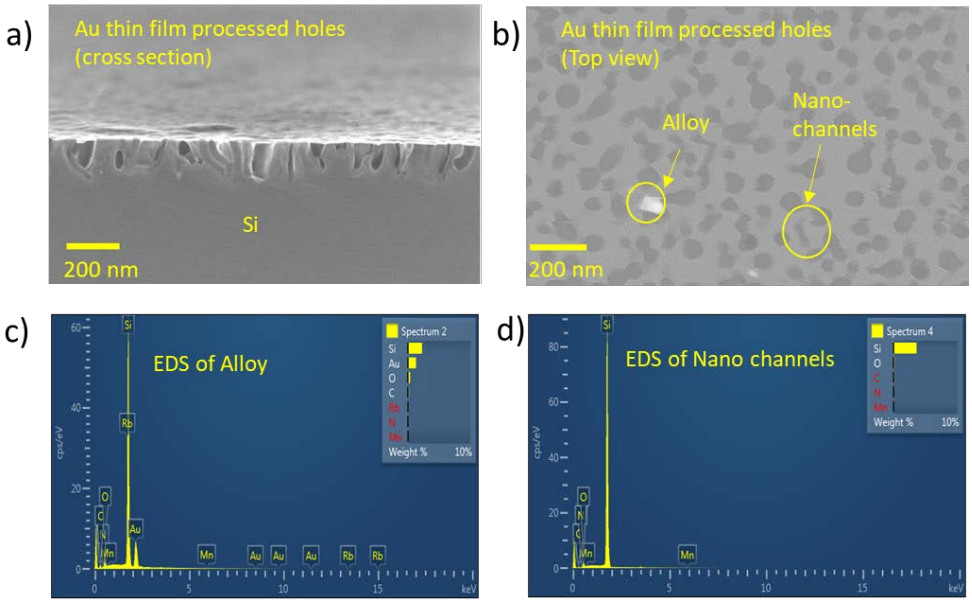

Figure 4.3.4: Au thin film processed nano-channel sample: a) SEM cross section b) topography image, c) EDS data of alloy and d) EDS data on channel region

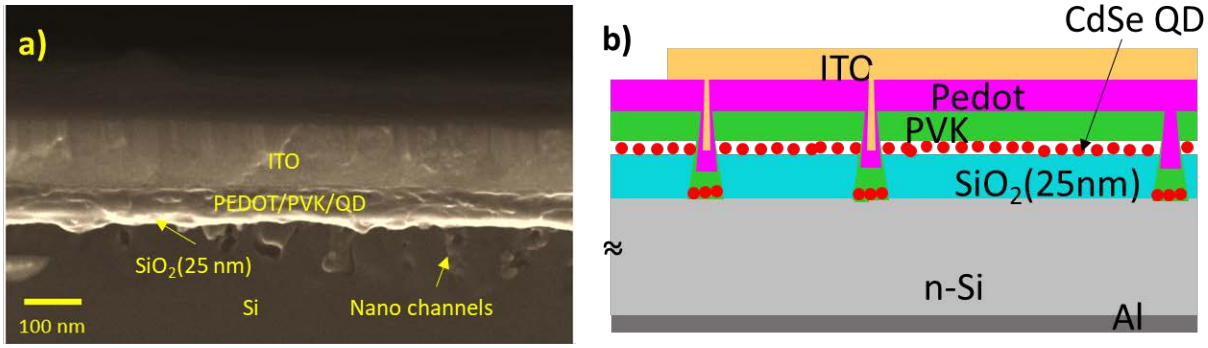

Figure 4.3.5: Nanoholes and OLED fabrication on Au thin film processed sample: a) cross section of nanoholes in SiO_2(25nm)/n-Si substrate and b) Schematic diagram of nano-OLED

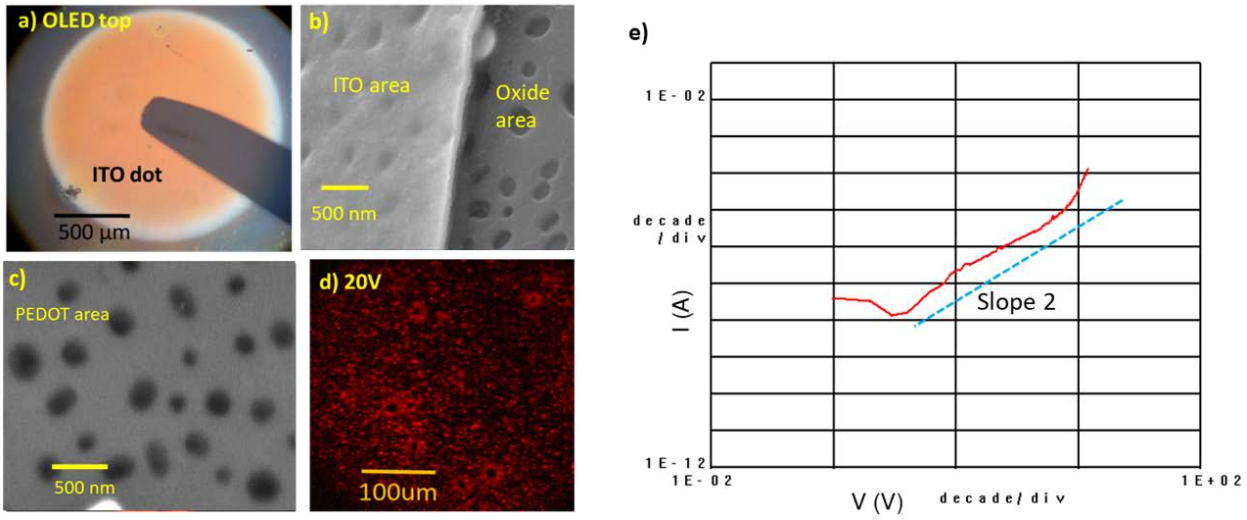

Figure 4.3.6: Electroluminescence of thin film processed nano-OLED samples: a) Top view of OLED defined by ITO dot, b) SEM image showing topographical contrast between OLED and oxide only region on same sample, c) Electroluminescence at 15V and d) 20 V bias.

4.4 NANOPARTICLE PATTERNED ETCH MASK

4.4.1 Introduction

In the previous section we demonstrated a novel non-lithographic nanochannel fabrication process using a gold nanoparticle as the thermal oxidation mask. However, one of the potential risks in the MACE process is the residual metal ions left in the nanochannel walls [101]. The process of post MACE oxidation may trap these ions and cause leakage of the current through field oxide. Therefore, we explored another fabrication process that does not require any high-temperature oxidation or MACE process after incorporating metal nanoparticles. Moreover, in this process we avoided thin film annealed NP formation to avoid irregularity in nanohole sizes. Colloidal gold nanoparticles were used to create circular etching windows in a dielectric etch mask film. The etched holes have a similar diameter to the nanoparticle. The following sections describe the fabrication process of nanoholes and corresponding nano-OLED samples.

4.4.2 Fabrication process

The overall process of fabrication flow is shown in figure 4.4.1. To begin with, we chose n-Si <100> wafer (phosphorous doped with a resistivity of 5 Ohm.cm). To remove the organic contaminants and grease, the wafer was first cleaned with acetone and then in methanol for 10 minutes each in an ultrasonic bath. The wafer was then rinsed with DI water and went through the RCA cleaning process flow for native oxide removal and contamination cleaning. A thermal oxide of 25 nm was grown afterwards by placing the wafer in an oxidation furnace for 30 minutes in air

ambience at 950^{o} C. An Ohmic contact was prepared on the back side of bare silicon by depositing 150 nm-thick aluminium and consecutive annealing at N_2 ambience at 350^{o}C for 30 minutes.

The first step in creating nanoholes is to deposit nanoparticles (NPs) on the substrate (figure 4.4.1-step 1). Three different sizes of citrate-stabilized Au NP colloidal solution were purchased from Ted Pella, Inc. having 20, 50 and 200 nm diameter. We encountered an issue while spincoating the gold nanoparticles on the SiO_2 surface. The hydroxyl group on the oxide surface lacks any affinity to citrate-passivated nanoparticles, and therefore NPs are easily washed away without adhering to the substrate. To improve the surface adhesion, we modified the oxide substrate with an N-(2-Aminoethyl)-3-aminopropyl-trimethoxysilane (AEAPTMS) coating that binds free amine (-NH2) group to the surface [102]. The silane group interacts with the hydroxyl-terminated oxide surface to form siloxane that consists of an amine (-NH_2) group at the tail (figure 4.4.2). When this sample is immersed in the gold colloidal solution, the amine group becomes protonated forming NH_3^+ which can now bind the negatively-charged citrate ions surrounding the gold nanoparticles (figure 4.4.2). Process-wise, the 0.1% AEAPTMS solution in water was spin-coated on the SiO_2(25nm)/n-Si sample at 2k rpm speed followed by a 30-minute baking at a temperature of 120^{o}C. The NP colloidal solution was then spin-coated at 2k rpm on this sample. The residual chemicals/ions on the surface were removed by submerging the sample in DI water for 5 minutes followed by nitrogen blow drying. Figure 4.4.3-a, b, and c show the NP-coated sample of 200, 50 and 20 nm diameter with a density of 0.15, 2 and 50 million/cm^2.

In the next step, we created a complementary hole pattern from the NP-coated sample by depositing a thin alumina film on it and then etching away the NPs (figure 4.4.1-step 2&3). Alumina (Al_2O_3) was chosen as the mask for its high etch-resistivity against gold and SiO_2 etchants. The film was deposited in an RF sputtering chamber using a 99.9% pure alumina source.

The samples were positioned 2 inches above the target surface, aligned with the source. The chamber was vacuum pumped down to $2x10^{-5}$ Torr pressure. Pure Ar gas was then introduced into the chamber to the pressure level of 8 m Torr. An RF magnetron gun was supplied with 30 W RF power for deposition of alumina at a rate of ~0.8 nm/min. To prevent complete covering of NPs, the alumina film thickness needs to be smaller than the NP radius. In our case, the total film thickness was kept at 30 nm, 15 nm and 7 nm for 200 nm, 50 nm and 20 nm NPs respectively. Thus, the Au NPs are expected to create discontinuities in alumina film, through which gold etchant can diffuse. Figure 4.4.2 shows the effect of alumina film thickness relative to the nanoparticle diameter to determine the mask opening dimension. Due to the uniformal coating nature of sputter deposition, the etch window size in alumina is expected to be less than the NP diameter. We used aqua regia as the gold etchant since it has a high etch selectivity (over 1000) for gold over alumina. We found that at room temperature aqua regia etches alumina at 0.3 nm/min, while gold is etched at a rate of 10 μm/min. We ultra-sonicated the sample in aqua regia for 5 minutes to break loosely-connected alumina film covering the upper half of the nano-particles. After rinsing and drying the sample, we get nano porous alumina film where the hole diameter follows NP size. In the fourth step (figure 4.4.1, step 4), a plasma reactive ion etching (RIE) was performed in CHF_3/O_2 gas to etch SiO_2 through the openings of alumina layer. The RIE chamber pressure and power were set at 30 m Torr and 150 Watt respectively. The etchant gas CHF_3 was introduced at a flow rate of 23 sccm. A very low amount of O_2 flow (1 sccm) was introduced to increase fluorine/carbon ratio and to prevent polymer formation on the etched surface. The CHF_3/O_2 gas mixture was found to have an etch selectivity of ~10 for Si and SiO_2 over alumina. The etch rate for Si, SiO_2, and alumina is 0.9, 1.1 and 0.1 nm/s respectively. We etched the nanoholes for 50 s, rendering a hole depth of 45 nm. In the final step, alumina was removed using

1:1:3 volumetric ratios of NH_4OH: H_2O_2: H_2O at 80 ^oC temperature (figure 4.4.1-step 5). At room temperature, this solution shows a high (>100) etch selectivity for alumina over Si or SiO_2. It also creates a monolayer of SiO_2 on bare Si surface, which helps to passivate the RIE etched hole surface. The SEM image of the final nanochannel samples processed from 200, 50 and 20 nm nanoparticles are shown in figure 4.4.3. As stated earlier, the resultant hole in the alumina film is always smaller than the original NP diameter. In our case, the 200 nm NP results ~160 nm hole diameter, 50 nm NP gives 40 nm, and 20 nm results in about the same sized holes. However, compared to the oxidation mask process of nanochannel fabrication, in the current process, nanoholes are more directional and uniform in terms of channel depth and density.

4.4.3 Nano QD-OLED

As a next step, we fabricated quantum dot OLED using the nanochannel substrate as a cathode. The OLED fabrication method and device structure is the same as described in the previous section. We need to consider a few facts before proceeding with the nano-OLED electro-luminescence result. Firstly, the density of nanoholes is limited by the density of gold nanoparticles on Si, which is less than 1 μm^{-2}. Even though we expect very high luminescence from individual nanoholes resulting from 2D electron gas injection, it might not appear bright, due to microscope imaging resolution. We used a Nikon microscope with 2000X magnification to capture the luminescence from nanoholes. The lens we used (Nikon #78754, BD 100X, Dry) has a numeric aperture of 0.9 mm and working distance of 0.39 mm. Considering the emission wavelength (625 nm) and OLED diameter (< 200 nm), the microscope working distance is into the far field region where intensity is inversely proportional to the square of the distance. Moreover, the image brightness or light-gathering power of the objective lens is inversely proportional to the square of

magnification. Therefore, the brightness of the image captured by microscope can underestimate the actual brightness of OLEDs significantly. Even at higher bias, the brightness of OLED is not expected to be very high in the emission image for this reason. Secondly, the enhanced capillary effect of nanoholes, together with organic polymer's hydrophilic nature, means moisture can get trapped inside the narrow holes. As stated in chapter 3, the trapped moisture can heat up during the OLED operation and cause physical damage to the OLED stack by bubble formation while being evaporated. Considering the effects of external parameters, in this report, we focused on individual nano-OLED emission rather than efficiency optimization/measurement.

Figure 4.4.6 a & b shows the micrograph of electroluminescence from 160 and 40 nm OLED holes respectively. In the micrograph, the bright 200 μm stripe patterns contain nanoholes, while the dark areas are planar oxide. We patterned the 200 μm stripes on alumina film by photolithography (1827 photoresist) so that the non-stripe oxide areas do not get exposed in the RIE step (figure 4.4.5). While patterning is a practical approach to define LED pixel size, it also allows us to confirm that even at high bias, emission originates from nanochannels, not due to oxide leakage or breakdown induced channel emission. From the insets of 4.4.6 a, we can distinguish the luminating nano-OLEDs. The average distance between 160 nm nanoholes can be measured from the SEM image (figure 4.4.4 a) and it matches the average spacing between nano-OLED emissions (~2-7 μm) surprisingly well, proving that most of the nano-OLEDs in this sample are active. For the case of the 40 nm hole sample, the hole spacing is 200-300 nm and it is expected that at this resolution the nano-OLEDS won't be distinguishable. From the I-V characteristics of OLED samples, interestingly the current does not follow area scaling. The effective hole area ratio between 30 nm and 150 nm OLEDs is 1:1.7, while their cumulative perimeter ratio is 2.5:1. Therefore, if the carriers are injected uniformly throughout the area, the current through the 30 nm

OLED sample would be higher than the 150nm hole device. From the I-V plot, the 30 nm OLEDs actually show almost equal current as the 150nm sample. Considering the average diameter of nanoholes as 50-nm, each hole is estimated to accommodate about 25 self-organized quantum-dots (8-nm diameter and 2-nm spacing in between). The hole density for the thin-film processed sample is estimated to be ~$3x10^8$ cm^{-2} (Fig.3a) rendering a QD density of $7.5x10^9$ cm^{-2}. In the case of the 200 nm NP processed sample, nanohole density is estimated to be $1x10^7$ cm^{-2} (Fig.5a) rendering a QD density of $4x10^9$ cm^{-2}. All the QDs in nanoholes sitting near the periphery are expected to emit even at low voltage injection [103]. Considering the fluorescence lifetime of CdSe/ZnS QD as ~10ns, the carrier injection density would be ~$5x10^{17}$ charges/s rendering a current density of 80 mA/cm^2. Assuming the maximum amount (100%) of carrier injection and quantum efficiencies, we can expect the emission power of ~150mW/cm^2.

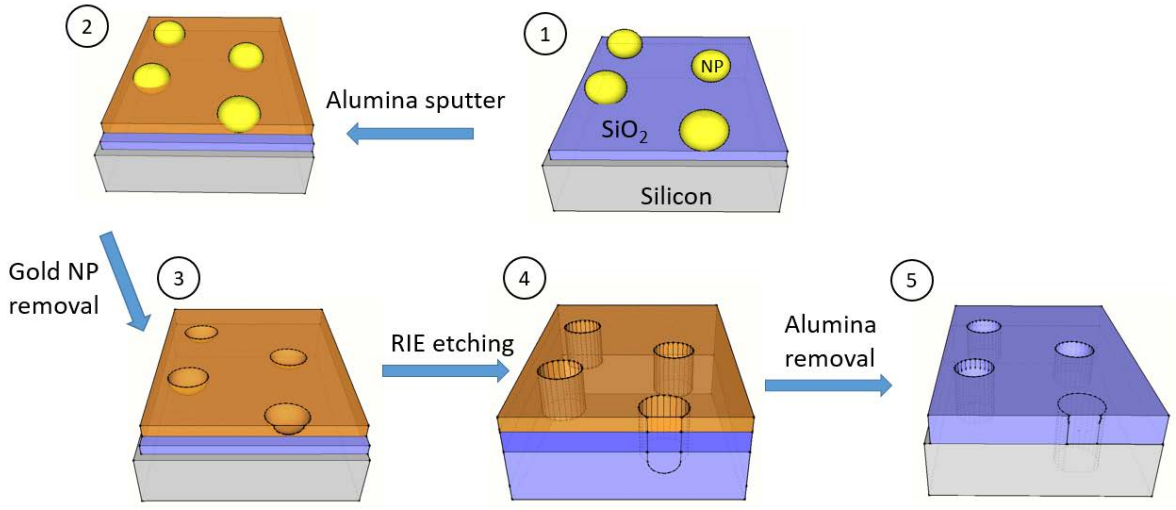

Figure 4.4.1: Process steps in fabricating nanoholes in SiO2/Si substrate: (first step) deposition of Au NPs on Si, (second) sputter deposition of alumina thin film on NPs, (third) wet etching of NPs to create etch window, (fourth) selective RIE etching of SiO2/Si and (fifth) removal of Alumina by wet etching.

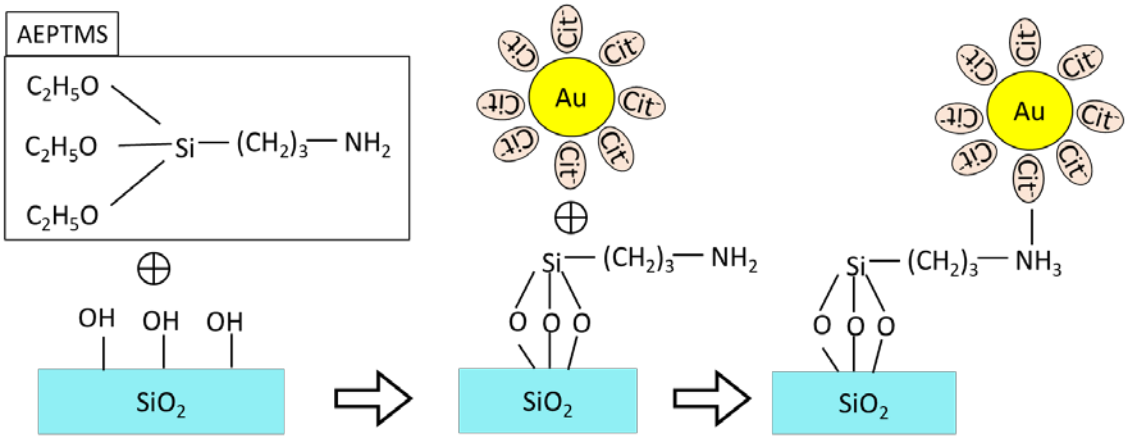

Figure 4.4.2: Gold NP adhesion on AEPTMS treated SiO_2 surface: Chemisorption of AEPTMS on OH-terminated oxide surface (left and middle), bonding of Au NP in AEPTMS Amine group (right)

Figure 4.4.3: Effect of nanoparticle size and alumina film thickness on etch mask window sizes.

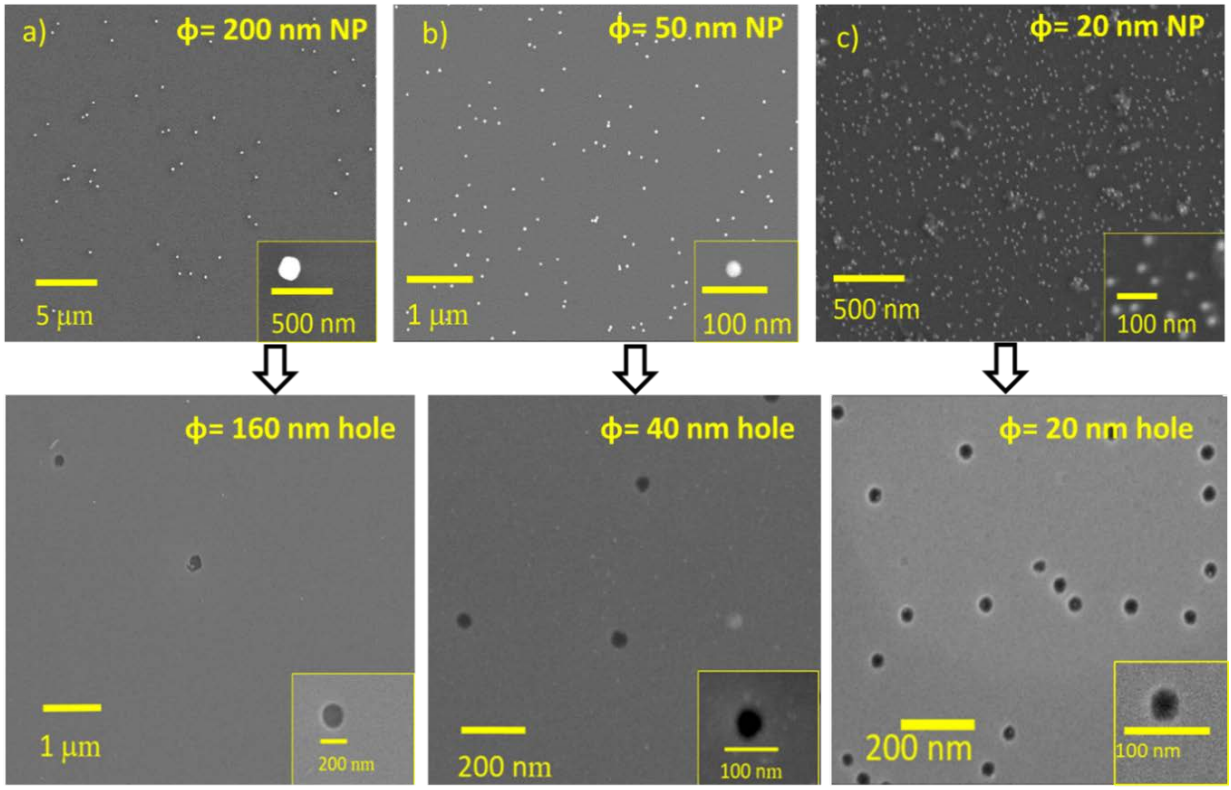

Figure 4.4.4: SEM image of spin-coated NPs on SiO_2(25 nm)/Si surface (top row) and corresponding holes (bottom row) (a) 200 nm, (b) 50 nm, and (c) 20 nm NPs.

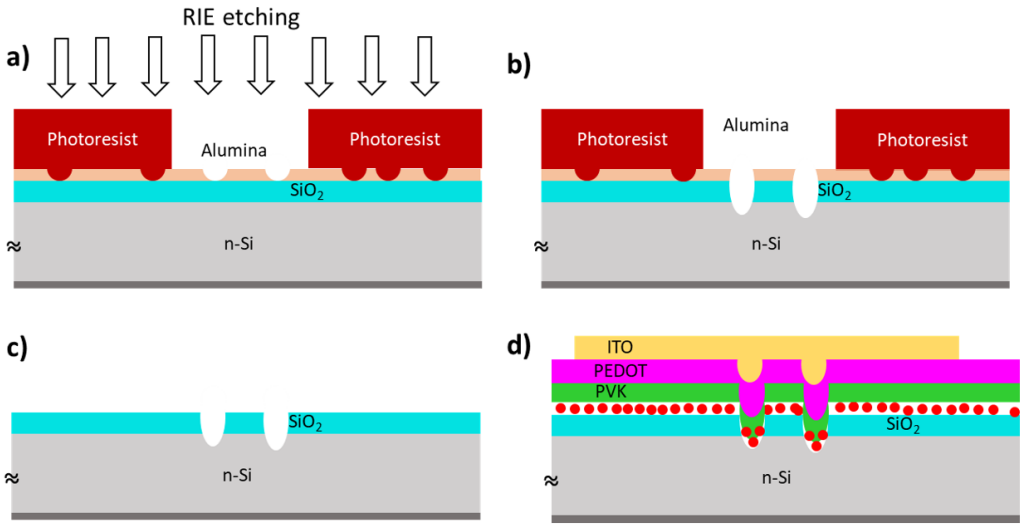

Figure 4.4.5: a) Patterning nanochannel samples and RIE etching of exposed area, b) hole pattern on the patterned area, c) removal of PR and Alumina and d) OLED cross section on patterned nanochannels.

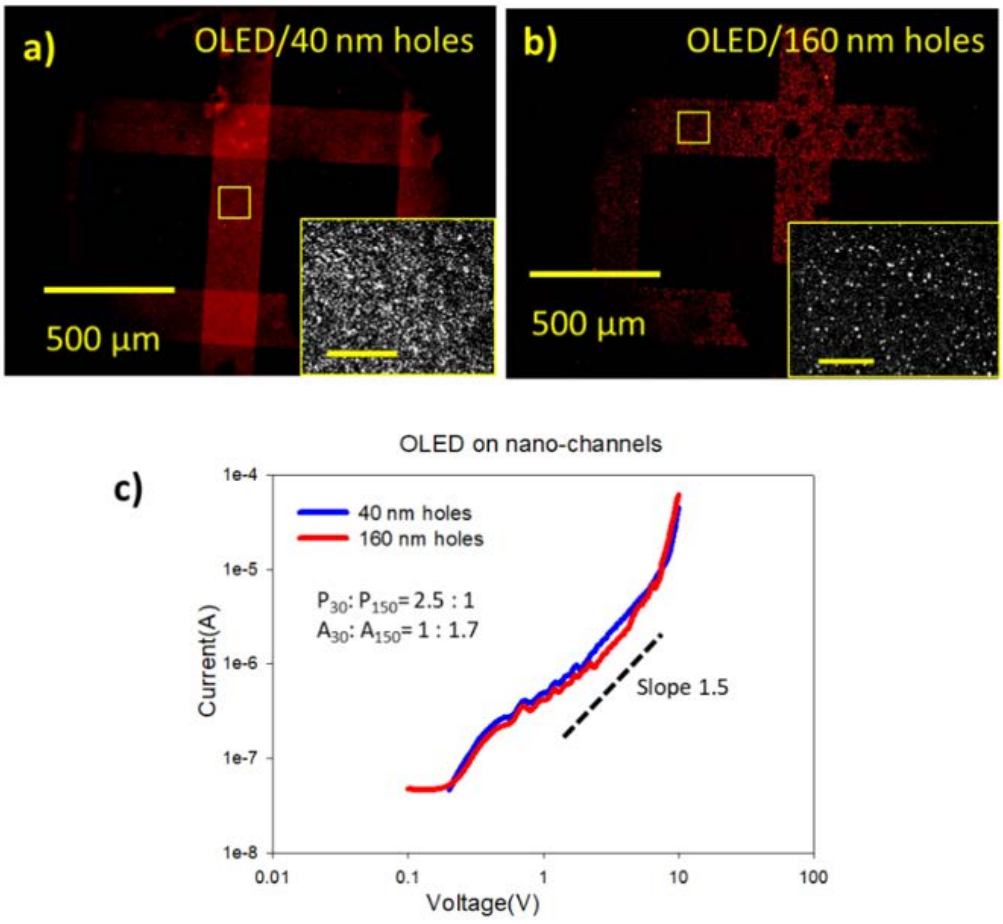

Figure 4.4.6: Micrograph of electroluminescence showing emission from a) 40 nm OLED with ~200-300 nm spacing; b) 160 nm diameter OLEDs with ~2-5 µm spacing, and c) Parameter vs area dependence of I-V characteristics

4.5 SUSPENDED NANO OLED

4.5.1 Introduction

In the previous sections, we demonstrated the nanoscale OLED on Si substrate by coating OLED stacks on patterned nano-trenches or holes in SiO_2. A couple of concerns regarding this structure are the coating fidelity of polymers along the nano hole walls and the optical coupling of emitted photons from narrow OLEDs. We proposed a novel way to overcome these problems by placing a monolayer sheet of hexagonal boron nitride (h-BN) on the patterned substrate and building OLED on top. Another advantage of suspended h-BN is that it utilizes a unique two-dimensional electron gas (2DEG) injection mechanism demonstrated in nanochannel devices. This low voltage, low power, and high-density carrier injection mechanism is well established in graphene oxide semiconductor (GOS) devices with nano-channels [12]. Electrons can travel through the vacuum, pass through the hBN monolayer and reach the emissive layer. G. H. Lee showed that like very thin SiO_2, monolayer h-BN allows direct tunneling at low bias while F-N tunneling occurs at high bias [104]. The advantage of vacuum channel conduction is that holes cannot bypass the vacuum channel and reach cathode Si. Therefore, the vacuum channel formed between Si and OLED is expected to act as an effective hole-blocking layer and a good electron transport layer. Moreover, optical outcoupling is an important concern for the directly deposited nano-OLED since the emissive layer is located at the bottom of the shallow trenches. In the following sections, we first built a suspended Graphene photodiode on nanochannel samples fabricated by RIE etching as described in section 4.4. In the next section, we described fabrication and characterization of h-BN suspended OLED.

4.5.2 Graphene photodiode

Myungji et. al. has shown that a Graphene oxide semiconductor (GOS) structure with EBL patterned oxide trenches can work as a very efficient photo diode by utilizing injection of photo generated 2D electron gas [12]. We decided to replicate the GOS photodiode structure by placing a monolayer graphene sheet on top of our nanohole-containing trenches. By replacing the time consuming and expensive EBL process with our newly developed non-lithographic approach, we aim to reduce the cost of GOS photodiode fabrication. To begin with, we fabricated 150 nm nanochannels on SiO_2(25 nm)/n-Si substrate by utilizing alumina RIE mask process (Sec 4.4). After creating back side Ohmic contact, we transferred CVD grown monolayer graphene on top of the nanochannel sample in the same process as described in section 2.3. After completing the GOS photodiode fabrication, we illuminated the Gr top with 632 nm He-Ne laser. We varied the laser power by 1, 5 and 10 μW and recorded the corresponding photo response in terms of I-V plots as shown in figure 4.5.1. The current responsivity for 1 μW illumination is 0.5 A/W which translates to an external quantum efficiency of ~100%. The graphene based photodiode that Myungji et al. reported was fabricated on p-Si, where photo-generated electrons gather at the oxide-Si interface due to a depletion field, and then are injected towards graphene ballistically through the EBL patterned nanochannels. In our case, since we are using n-Si as substrate, photo-generated holes create a 2D hole system at the interface. On the other side, due to reverse voltage, a lot of electron states are created in the graphene monolayer. The graphene's electrons form a quasi 2D electron system of sub nm depth, and are injected ballistically through the nanoholes.

4.5.3 h-BN suspended OLED

As a first step to fabricate suspended OLED, we placed a monolayer h-BN on SiO_2/Si substrate containing nanochannels (figure 4.5.2). A CVD-grown monolayer h-BN sheet on Cu foil was purchased from Graphene Supermarket Company. The transfer process of h-BN on oxide substrate is similar to the Gr wet transfer process described in section 2.3. After finishing the suspended h-BN sample preparation, we fabricated our usual OLED stacks consisting of QDs, PVK, PEDOT, and sputtered ITO on top. All these layers are deposited in the same process described in previous sections. The h-BN layer is expected to form an effective barrier against diffusion of OLED materials into the holes. Figure 4.5.3 shows the SEM image of cross section of the hBN-suspended OLED structure. Here, the hole opening is ~30 nm in diameter and ~40 nm in depth, matching well with topographical SEM image of hole samples and the RIE etch depth. However, in SEM image resolution the monolayer hBN is not visible, but we can anticipate its presence at the oxide-OLED interface as the LED stack is suspended on top of holes (figure. 4.5.3 a).

As described in chapter 3, the OLED stack on the field oxide area resembles an MOS capacitor structure. It is well known that the SiO_2/Si interface can accumulate a high concentration of 2D electron gas at proper bias, e.g.,10^{12} cm^{-2} at ~1 V forward bias [7]. At this density level, the average spacing between electrons in the 2DEG is estimated to be ~10 nm, which is smaller than the oxide thickness (23 nm). This close spacing will ensure that the in-plane interaction of 2DEG electrons becomes stronger than the dipole charge interaction across the oxide layer. Due to this Coulombic repulsion at the channel edge, the energy barrier for electron injection into the outside is lowered, enabling electron emission at a relatively low bias voltage. In the case of an MOS with a suspended graphene on void-well channel, it has been reported that the channel current is proportional to the perimeter of the well, indicative of the edge injection/emission of 2DEG [12].

Similar behavior is expected with our suspended OLED structure: the SiO_2/Si interface in the field oxide area under the ITO electrode will accumulate 2DEG at the forward bias, which will emit at the edge into the void nanochannel and tunnel through the monolayer h-BN towards QD emissive layer [figure 4.5.2 (c)].

Figure 4.5.3 shows the electroluminescence micrograph of h-BN suspended OLEDs of diameter 160 and 40 nm. The individual nanohole emission is not detectable due to the low resolution of the micrograph. It is noteworthy that the emissive area shows many defective sites and black spots when compared with planar oxide top nano-OLEDs from figure 4.4.6-a&b. The excessive damage can be attributed to the trapped moisture inside h-BN-covered nanoholes that may heat up and form bubbles during emission. As a next step, we wanted to determine/compare contributions from area injection and perimeter injection of carriers. We compared the I-V characteristics of the 160 and 40 nm hole samples having substrate area of 0.75 and 1 mm^2 respectively (figure 4.5.3). Considering the nanohole density mentioned in the previous section, the number of emissive holes are 0.11 million for larger (160 nm) and 2 million for smaller (40 nm) hole samples. The cumulative perimeter of larger holes is ~55 mm, while for the smaller holes it is 250 mm (~4.5 times longer). Interestingly the total areas of larger and smaller holes are almost equal, 2200 and 2500 μm^2 respectively. Figure 4.5.4 compares the I-V characteristics of these samples in forward bias condition. Interestingly, the current of the smaller hole sample is found to be ~4 times higher than the larger hole sample, indicating that the current ratio closely matches the perimeter ratio of the two devices, not area ratio. In the case of larger holes, h-BN may touch the hole bottom, creating a direct area contact between OLED stacks and Si. This shorting would increase the net current in larger holes, which explains why smaller-to-larger hole OLED-current ratio reduces by ~10% when compared with their perimeter ratio (4 instead of 4.5). Also, for both samples, OLED

turn-on voltage is quite low (1–2 V) and this can be attributed to low-voltage injection of 2D electron gas at the nanohole edges. Most importantly, the I-V characteristics show a slope of 1.5 which indicates Child-Langmuir's space-charge limited current in scattering-free vacuum environment [13]. In summary, we can conclude that the 2D electron gas is injected into the void nanoholes at the device edges, from where it travels ballistically towards the suspended emissive layer.

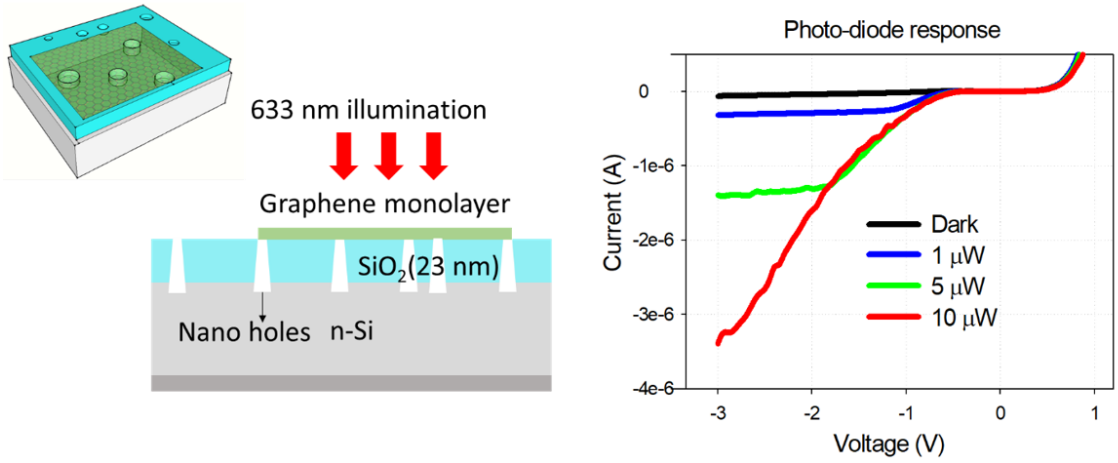

Figure 4.5.1: Graphene photodiode response for nanohole sample: Photoexcitation on Gr/nanochannel sample (left), Photo response at reverse bias (right)

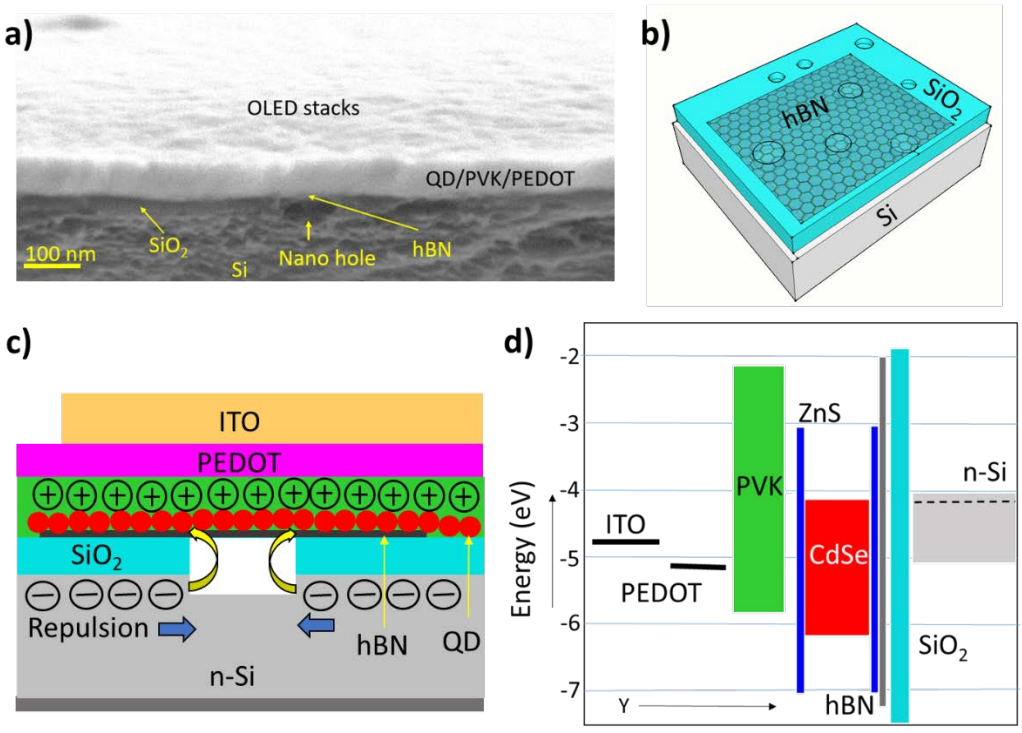

Figure 4.5.2: Device cross section and schematic band diagram of hBN suspended OLED

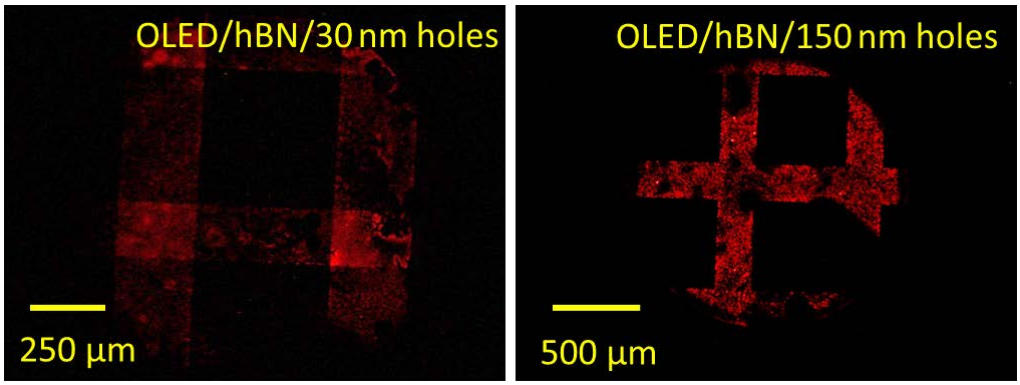

Figure 4.5.3: Electroluminescence micrograph of h-BN suspended OLED with nanohole diameter of a) 160 nm and b) 40 nm. The 200 µm stripes containing nanoholes were patterned by photolithography.

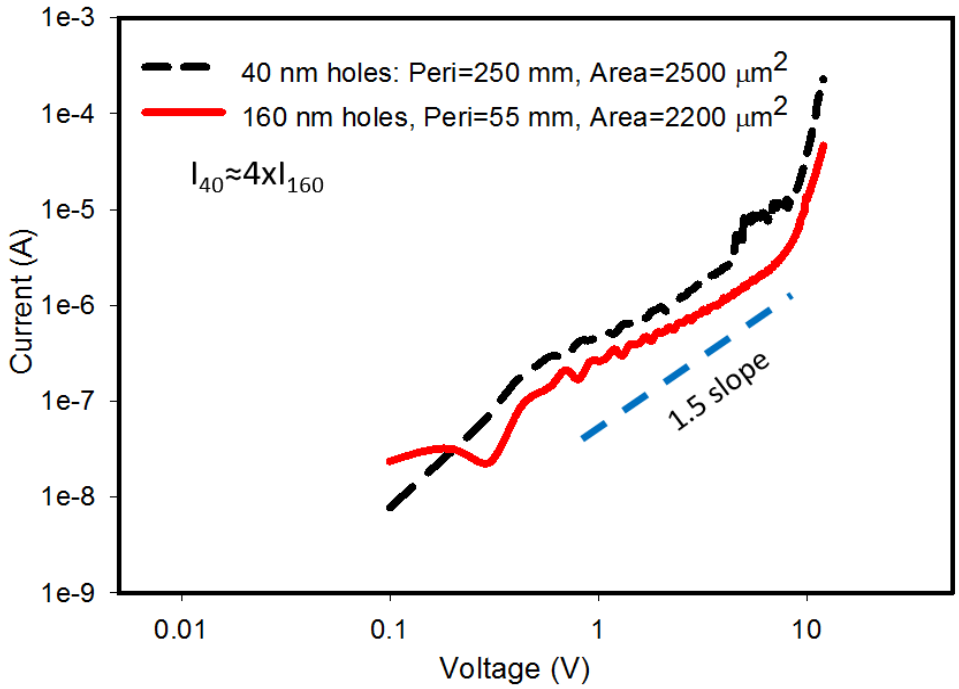

Figure 4.5.4: Current-voltage characteristics of nano-OLED samples with two different device sizes. The current ratio follows total perimeter ratio and shows a slope of 1.5, indicator of vacuum carrier injection mechanism.

4.6 APPLICATION FIELDS OF NANO OLEDS

We demonstrated a 2DEG injection mechanism along the junction boundary of nano-OLED samples down to 40 nm diameter. Using the low voltage emission of 2DEG, the confinement of carrier injection down to single-QD level is expected to be achievable. This edge-injected QD-OLED structure opens the possibility of developing nanoscale light sources for quantum computing and other silicon optoelectronics.

The proposed single photon source can be fabricated by developing nanoholes of 5-12 nm diameter on a SiO_2/Si structure by nano-sphere, E-beam or nano-imprint lithography. When QDs (diameter ~8nm) are spin-coated on these holes, a single QD may fall in (figure 4.6.1-a) or adhere

to the nanohole periphery (figure 4.6.1-b) depending on the nanohole diameter. From analyzing the cross-section image, electroluminescence, and I-V data, we can speculate the carrier transport mechanism in each of the structures. When a single quantum dot falls inside a nanohole, a few factors will play an important role in determining device performance. Since the hole aspect ratio (diameter/height) is less than 0.5, a uniform coating of hole transport layers is unlikely because of the viscosity of polymers and shadow effect of ITO sputtering. Moreover, due to non-directionality of the emitted photon, the probability of acquiring luminescence from a single photon source is very low. On the other side, if the nanohole diameter is less that the QD diameter, the QD OLED will be suspended on nanoholes, and the electron injection in QD will be governed by 2D electron gas emission through hole periphery, as described in the previous section for hBN suspended OLED. Since photons will be emitted from the surface, in this case, the coupling of emitted photons to external detector would be easier.

An approach to developing quantum computing devices is to use an all-optical architecture known as linear optical quantum computing (LOQC), in which the qubits are represented by photons and manipulated by mirrors and beam splitters. One of the biggest challenges for LOQC system is to integrate all these optical components that are usually incompatible with each other, onto a single platform. Another obvious challenge is generating an indistinguishable single photon source feasible to operate at room temperature. Our proposed nanoscale OLED on Si platform can effectively resolve both of these issues by utilizing very simple well-established technology. P. Michler et al. have shown that a single CdSe QD can act as a single photon source at room temperature [105]. Also, the OLED is reported to be effective to confine the emission area to true nanoscale dimension, utilizing the low conductivity and carrier mobility of organic polymers.

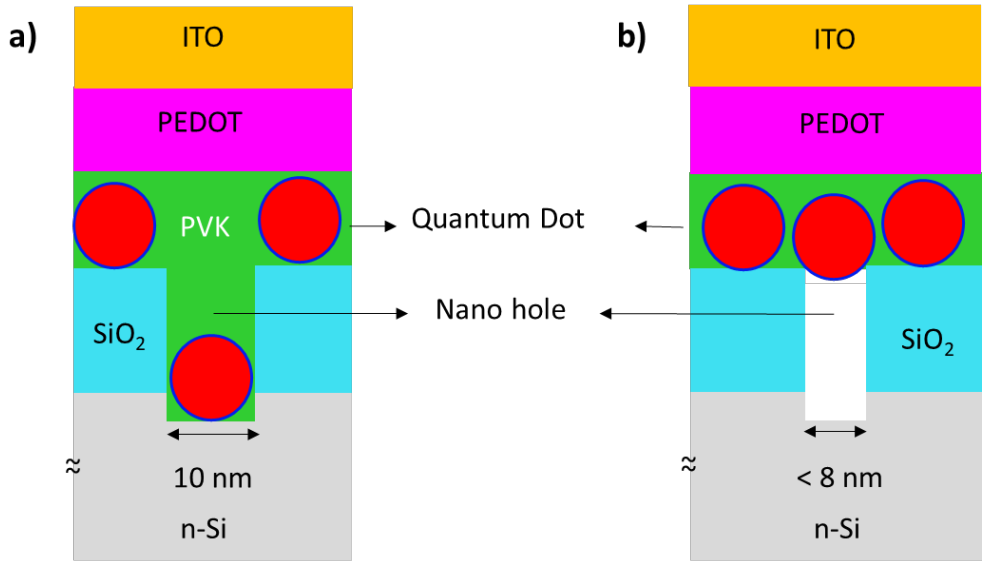

Figure 4.6.1: a) QD-OLED accommodating single quantum dot and b) suspended single QD-OLED

5.0 CONCLUSION

In Chapter 2 of this thesis, we demonstrated the theory and operation of stacked SOS (semiconductor-oxide-semiconductor) structure. By employing a stacked p-Si/SiO2//SiO2/n-Si structure having a cleaved edge on one side we demonstrated that Coulombic repulsion at the cleaved edge enables low-voltage emission of 2DEG. Later we inserted a monolayer of graphene between the oxide samples and explained the effect of graphene's density of states in the current conduction. As a part of transport characterization through insulators, lastly, we demonstrated I-V hysteresis in metal and graphene based MOS devices when the bias voltage is swept from strong inversion to accumulation. The hysteresis current is strongly affected by various device parameters and ambient conditions like temperature and illumination. We hypothesized that the origin of hysteresis is the slow rate of recombination of the excess inversion charges that are freed during voltage sweep from inversion to flat band condition.

In chapter 3 we fabricated a top emitting QD-OLED structure using Si as a cathode and the inorganic quantum dots as a luminophore. We still used organic polymers as hole transport layer due to the lack of transparent p-type inorganic materials. In this device structure, the junction area is defined by a lithographically patterned oxide layer on Si substrate and is designed to allow a wide range of scalability of lateral dimension down to a nanometer range. By varying the junction dimensions and geometry, the electron injection process is found to occur predominantly at junction periphery, not area, resulting in low turn-on voltage (~1-2V). Later in this chapter, we

compared between reference conventional OLED performance with our proposed OLED in terms of luminescence, and confirmed that Si-OLED performs much better when its edge emission is enhanced by shrinking the device size. This observation leads us to find a method to fabricate nanoholes in oxide/Si substrate to maximally scale down the OLED size. In chapter 4 we demonstrated emission from individual OLED pixels of 150 nm sizes with a few microns spacing in between. From electrical measurement, we observed that in nanoscale OLED the carrier is injected throughout the entire device area since the edge and area become indistinguishable. Lastly, to utilize the ballistic injection of 2DEG through a void channel, we fabricated an OLED structure stacked on a 2D material (h-BN monolayer) suspended on a nano-hole-etched SiO_2/Si substrate. The emission from the suspended OLED occurs one dimensionally along the edges, due to strong field directionality of 2D electron gas injection. This edge injection/emission QD-OLED structure, when scaled down to a sub-10nm range, offers an interesting approach to developing single quantum-dot light sources for quantum information processing. The main achievement in this report is a demonstration of 2D electron gas injection and resulting improvement in OLED performance. The emission from of nano-OLED or 2D material suspended OLED is regarded as a proof of concept to fabricate a single photon source which is an important component in quantum computing and quantum communication devices.

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