# THE STUDY OF A SINGLE-PHASE FULL-WAVE UNCONTROLLED RECTIFIER WITH A CONSTANT POWER LOAD IN A POWER GRID

by

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### THE STUDY OF A SINGLE-PHASE FULL-WAVE UNCONTROLLED RECTIFIER WITH A CONSTANT POWER LOAD IN A POWER GRID

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The single-phase uncontrolled rectifier supplying a constant power load (CPL) is common in a power system, especially for digital devices such as telecommunication equipment. The characteristics of CPLs may de-stabilize the system and cause the output voltage collapse if the initial capacitor voltage is too low. Based on a mathematical model of the rectifier-CPL circuit, a method is proposed to estimate the minimum initial voltage which makes the system converge. Also, some non-linear factors including the source impedance and the inertia of the CPL. When the rectifier operates in steady states, a high load power may cause the bifurcation phenomenon. Some analysis is made for the bifurcation and its negative effects on the power grid.

Keywords: Constant power load, Rectifier, Convergence, Bifurcation.

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### 1.0 INTRODUCTION

<span id="page-7-0"></span>The constant power load (CPL) is one of nonlinear loads which consumes constant power regardless the states of the power source. This conception has been focused since 1990's as the application of switched converters increases in power systems. When a resistive load is supplied by a converter with fast voltage control, and all the losses are neglected (Fig[.1\)](#page-7-1) , the power injected to the converter is constant since the voltage across the load doesn't change. Then the converter with resistive load can be treated as an instantaneous dc CPL. One



<span id="page-7-1"></span>Figure 1: A typical example of a CPL. This figure is reprinted from [\[1\]](#page-33-1)

typical example is the telecommunication equipment which takes more and more proportion in today's power system $|2|$ .

A system with CPLs could face the instability. [\[3\]](#page-33-3) and [\[4\]](#page-33-4) analyze this problem in the multi-converter systems. In general, CPLs have a negative impedance characteristic. Meanwhile, most sources also show the droop characteristic in  $i - v$  plot. Therefore, any disturbance could make the system lose its stability easily.

Many works has been done to deal with the de-stabilizing effects of CPLs. For the DC system, [\[5\]](#page-33-5) proposes a slide-mode control method to stabilize the dc/dc forward converter with a CPL in a automotive system. [\[6\]](#page-33-6) uses PD controller for a buck converter based on passivity system control. Also, boundary control is applied for dc/dc converters in [\[7\]](#page-33-7). For the AC system, relative researches are fewer compared to those for DC systems. [\[8\]](#page-33-8) proves that, based on Popov's Criterion, the required initial condition for the stability of a 3-phase rectifier with a CPL can be determined, but it only suitable for 3-phase devices which usually operates in continuous conduction mode (CPL). For many single-phase rectifiers, instead, the current is discontinuous because of a large filter capacitor. Besides, one-phase rectifier is studied in [\[9\]](#page-33-9) and this reference focuses more on interactions between the rectifier and CPL.

This thesis concentrates on a single-phase uncontrolled rectifier connected with a CPL, which is a common topology for the power supply of digital devices. For instance, Fig[.2](#page-8-0) from the datasheet [\[10\]](#page-33-10) is a basic circuit of a 12V output voltage supply, which is able to operate as the power source of many digital devices such as laptops. If the load connected to this



<span id="page-8-0"></span>Figure 2: A simplified circuit for a power adapter using LM78XX voltage regulator.

circuit is treated as a resistor, the whole system can be simplified as a rectifier-CPL model. in this example, the power level is relatively low, thus, the characteristics of CPL may not considerable in a macro power grid.

However, if similar topology is used for some high power devices such as a data center or telecom station, the effect may become significant. What's more, in the microgrid and

distributed power systems, the influence of CPL emerges since it could take up a large proportion of the total load  $[11]$ . Therefore, it is worthwhile to do more research on the properties of the system with a CPL.

In this paper, dynamic behaviors of the rectifier-CPL model is studied. In addition, this system is put into a non-ideal power system which indicates the source impedance is not zero. In this case, the interaction between the rectifier and the power grid is analyzed. In Chapter[.2,](#page-10-0) a mathematical model for the circuit is established and some non-ideal factors are involved. Chapter[.3](#page-14-0) discusses the convergence of the rectifier under CPL's influence. A method is proposed to estimate the minimum initial capacitor voltage which prevents the rectifier from voltage collapse. The effects of the non-ideal factors (source impedance and load inertia) are also considered. Chapter[.4](#page-23-0) focus on how the CPL affects the steady state operation of the rectifier. The bifurcation phenomenon in steady states is analyzed specifically. In this chapter, the influence of the bifurcation on the power grid is also discussed. Finally, conclusions of this thesis are made in Chapter[.5](#page-32-0) and, also, the limitation and future works are discussed.

### <span id="page-10-0"></span>2.0 THE MODEL OF THE SYSTEM

In order to analyze the dynamical behavior of the rectifier with a constant power load (CPL), a model should be built which can reflect the mechanism of the whole circuit. To eliminate too many non-ideal factors and make the simulation quicker and more accurate, the model is based on the state space equations rather than the real circuit topology in the simulation tool. In addition, source impedance and load inertia are intently considered as non-ideal factors to study their influence on the behavior of the system.

### <span id="page-10-1"></span>2.1 MATHEMATICAL MODEL FOR THE SINGLE-PHASE RECTIFIER

A simplified topology for the uncontrolled single-phase rectifier is shown in Fig[.3.](#page-10-2) In this



<span id="page-10-2"></span>Figure 3: the circuit of an uncontrolled single-phase rectifier

circuit, an ideal AC voltage source and the impedance represent the power grid. Four ideal diodes  $(D_1 - D_4)$  indicate that all the losses and non-ideal effects of the semiconductors are neglected. The source impedance is considered in order to reflect the rectifier's influence on the bus voltage. To reduce the ripple of output voltage, a LC filter is applied. In this thesis, the rectifier is assumed to operate in the DCM.

According to the different input voltage, the rectifier operates in two modes[\[12\]](#page-34-0)[\[13\]](#page-34-1). When the voltage on the left side of the diode bridge  $(v_1)$  is less than the one on the right side  $(v_2)$ , the diodes are off, the equivalent circuit (Fig[.4\)](#page-11-0) is actually a first-order system since only the capacitor works in this mode. Therefore, the state equation for this mode is



<span id="page-11-0"></span>Figure 4: the equivalent circuit for the first-Figure 5: the equivalent circuit for the order mode second-order mode

<span id="page-11-2"></span><span id="page-11-1"></span>
$$
C\frac{dv_C}{dt} = -i_{load}, \quad i_L = 0
$$
\n
$$
(2.1)
$$

where  $v_C$  is the capacitor voltage,  $i_{load}$  is the load current.

When  $v_1 > v_2$ , the diode bridge turns on depending on the polarity of the input voltage. Since the diodes are ideal, as is shown in Fig[.5,](#page-11-1) the bridge can be treated as a line and the input voltage is always positive. Then the circuit start to operate as a second-order system which can be expressed as (neglect the source impedance)

<span id="page-11-3"></span>
$$
L\frac{di_L}{dt} = |v_s| - v_C, \quad i_L > 0
$$
  

$$
C\frac{dv_C}{dt} = i_L - i_{load}
$$
 (2.2)

where  $v_s$  is the source voltage,  $i_L$  is the inductor current. It can be observed that Eq[.2.1](#page-11-2) and Eq[.2.2](#page-11-3) can be combined with a limitation of the inductor current  $(i_L \geq 0)$ .

if the source impedance is considered, it should be noticed that the impedance has no influence on the first-order mode  $(Fig.4, Eq.2.1)$  $(Fig.4, Eq.2.1)$  $(Fig.4, Eq.2.1)$  $(Fig.4, Eq.2.1)$ . In the second-order mode  $(Eq.2.2)$  $(Eq.2.2)$ , the source impedance  $(L_s, R_s)$  is in series with the filter inductor  $(L_f)$ . And that means if we only focus on the states  $i_L, v_C$ , the source impedance is equivalent to adding a series resistance to the filter inductor. Eventually, the mathematical model of the rectifier is

$$
(L_f + L_s)\frac{di_L}{dt} = |v_s| - R_s i_L - v_C, \quad i_L \ge 0
$$
  

$$
C\frac{dv_C}{dt} = i_L - i_{load}
$$
 (2.3)

#### <span id="page-12-0"></span>2.2 MATHEMATICAL MODEL FOR THE CONSTANT POWER LOAD

The rectifier with a LC output filter can be treated as a voltage source for the load, so an ideal constant power load operates like a voltage-controlled current source and the relationship is

$$
i_{load} = \frac{P_{load}}{v_C} \tag{2.4}
$$

where  $P_{load}$  is the load power of CPL and keeps constant. However, in the real world, the CPL is usually a voltage regulator or a DC-DC converter with a fast output voltage control. Although the converter can regulate the output voltage extremely quickly, it still need some time to transit from a transient state to a steady state. Therefore, a inertia element should be added to the current source model to represent the time response of the CPL (Fig[.6\)](#page-13-1). A simple inertial element can be expressed as a transfer function

<span id="page-12-1"></span>
$$
G(s) = \frac{1}{sT_s + 1} \tag{2.5}
$$

where  $T_s$  indicates how fast the system can restore into a steady state. If  $T_s = 0$ , the load becomes an ideal instantaneous CPL.



<span id="page-13-1"></span>Figure 6: the block diagram of the CPL model

### 2.3 THE REALIZATION OF THE MODEL

<span id="page-13-0"></span>Based on the mathematical analysis in the previous sections, the model for simulation can be built using MATLAB/Simulink. The important parts of the model are shown in Fig[.7.](#page-13-2) For the CPL model, the inertial element is added at the output  $(i_{Load})$  of the model because that can prevent the zero-dividing at the beginning of simulation. For the rectifier model,



<span id="page-13-2"></span>Figure 7: The Simulink model for the rectifier and the CPL

the limitation of  $i_L$  is realized by setting a lower saturation limit for the integrator. Other parts in the simulation model including the measurements and links between subsystems are not presented in this paper.

### <span id="page-14-0"></span>3.0 THE STUDY OF CONVERGENCE

For the rectifier working in the DCM, the state trajectory in the phase portrait should be convergent which means the system trajectory will converge into a limited cycle around an equilibrium point instead of the point itself. When the rectifier starts to operate, it could lose the convergence which is indicated by the output voltage collapse. A method is proposed to estimate a necessary condition of the convergence. Meanwhile, this chapter will study how the non-ideal factors (inertia of the load, source impedance) will affect the convergence of the rectifier. After that, some solutions will be discussed in order to avoid the voltage collapse and guarantee the convergence.

### <span id="page-14-1"></span>3.1 THE NECESSARY CONDITION FOR THE CONVERGENCE IN THE IDEAL CASE

By observing the mathematical model for the rectifier in the last chapter, similarities can be found between this model and the one for a buck converter. Therefore, it is expected that the rectifier would show similar characteristics as the buck converter when the initial capacitor voltage is low. Fig[.8](#page-20-0) displays the  $v_C - i_L$  phase portrait of a rectifier with different initial capacitor voltages  $(v<sub>C</sub>(0))$ . The arrows show the direction of each path alone the time. The phase portrait indicates that, like the buck converter, the initial capacitor voltage could determine whether the rectifier operates normally or the voltage collapse happens.

There must be a minimum  $v<sub>C</sub>(0)$  acting as the threshold below which the rectifier will face the voltage collapse. From Figure[.9,](#page-20-1) the first cycle of the trajectory (red curve) is much

larger than the ones in steady state, which means if the first cycle does not lead to the voltage collapse, then the system will be convergent unless other parameters change. So in this part, the dynamical behavior in the first period  $(0 < t < 0.0167s)$  is considered.

The reference [\[6\]](#page-33-6) provides a method to estimate  $v_c(0)_{min}$  for buck converter.A similar method could also applied for the rectifier. Define that  $v<sub>C</sub>(t<sub>0</sub>)$  is the capacitor voltage when the rectifier start to operate in the second-order mode (diodes turn on). It can be calculated (Eq[.3.1\)](#page-15-0) by the initial condition  $v<sub>C</sub>(0)$  easily if using a triangle wave to represent the sinusoidal waveform of the source voltage[\[9\]](#page-33-9).

<span id="page-15-0"></span>
$$
v_C(t_0) = \frac{1}{4fV_s} \left[ -\frac{P_{load}}{C} + \sqrt{\left(\frac{P_{load}}{C}\right)^2 + \left(4fV_s v_C(0)\right)^2} \right] \tag{3.1}
$$

where  $V_s$  is the RMS value of the source voltage. Once the rectifier operate as a 2nd-order system,  $v_C$  continue to decrease since at that time  $i_L < i_{load}$ . One sufficient condition for the voltage collapse is

<span id="page-15-1"></span>
$$
i_L < i_{load} \Rightarrow \frac{dv_C}{dt} < 0
$$
\n
$$
\frac{di_L}{dt} < \frac{di_{load}}{dt} \tag{3.2}
$$

<span id="page-15-2"></span>At the same time, Eq[.3.2](#page-15-1) is also a necessary condition for the convergence which can be used to estimate the minimum  $v<sub>C</sub>(0)$ . Combine the second line of Eq[.3.2](#page-15-1) and Eq[.2.2,](#page-11-3) we can obtain

$$
i_L < \frac{\frac{LP_{load}^2}{Cv_C^3} + v_C - v_s(t)}{\frac{LP_{load}}{Cv_C^2}}\n\n\varphi : i_L = \frac{\frac{LP_{load}^2}{Cv_C^3} + v_C - v_s(t)}{\frac{LP_{load}}{Cv_C^2}}\n \tag{3.3}
$$

Eq[.3.3](#page-15-2) actually provides a boundary  $\varphi$  in the  $v_C - i_L$  phase portrait. If the trajectory of the rectifier goes blow the boundary, voltage collapse will happen definitely. The dash line in Fig[.9](#page-20-1) is one example of the boundary.

One problem to estimate  $v_c(0)_{min}$  is that in Eq[.3.3,](#page-15-2) the term  $v_s(t)$  is not constant, so the boundary  $\varphi$  keeps moving in the  $v_C - i_L$  plate, as is shown in Fig[.10.](#page-20-2)

By observing this figure, although the boundary changes a lot in the  $v_C - i_L$  plate, it moves quickly when  $v_s(t)$  is relatively low. If  $v_s(t)$  is close to the peak value or is around the average value  $V_{avg}$ , the boundary tend to stay still. It is hard to describe the dynamical process by a brief mathematical algebra system, but it can be deduced that, at the beginning when  $v_c = v_c(t_0)$  (Eq[.3.1\)](#page-15-0), the trajectory of the rectifier could stay below the boundary temporarily, but shortly after that, the boundary moves down quickly as  $v_s(t)$  increases. When  $v_s(t)$  reaches a high value, the boundary changes slowly and the trajectory stays above  $\varphi$ , which means the voltage collapse is avoided. Therefore, in most cases, whether the rectifier converges depends on whether the trajectory penetrates the boundaries close to the red curve in Fig[.10.](#page-20-2)

In order to determine  $v<sub>C</sub>(0)min$ , a constant boundary should be selected. Through many times of simulation, it is found that the boundary corresponding to  $v_s(t) = V_{avg}$  (the red curve in Fig[.10\)](#page-20-2) is relatively accurate, in other word, most trajectories that penetrate or even too close to this boundary will hit the  $i_L$  axis (voltage collapse).

With the selected boundary,  $v_C(0)_{min}$  can be estimated following several steps:

- 1. Use the system parameters to calculate the boundary  $\varphi$  (in Eq[.3.3,](#page-15-2) let  $v_s = V_{avg}$ ), and then obtain its intersection point with the  $v<sub>C</sub>$  axis, which is denoted as  $v<sub>\varphi</sub>0$ .
- 2. Let  $v_C(t_0) = v_{\varphi 0}$ , then  $v_C(0)$  can be calculated using Eq[.3.1.](#page-15-0)
- 3. The result got in the previous step can be treated as the minimum voltage  $v_c(0)_{min}$ , but it should be noticed that the actual minimum initial voltage is usually higher than this result because not only the boundary we select is a approximation of the real one, but also the actual minimum  $v<sub>C</sub>(t<sub>0</sub>)$  is larger than  $v<sub>\varphi</sub>0$ .

The method proposed in this paper is a rough estimation because 1)the principle is a necessary condition of the convergent system; 2)many approximation is involved in the calculation; 3)this method is based on the ideal case without considering inertia, source impedance and other factors.

### <span id="page-17-0"></span>3.2 THE EFFECT OF THE NON-IDEAL FACTORS ON THE **CONVERGENCE**

In this part, several non-ideal factors are involved in the system. Usually, a real power grid is equivalent to an ideal voltage source in series with the source impedance  $Z_s$ . For the large-scale grid, the reactance is much larger than the resistance, so  $Z_s \approx X_s$ . However, for the microgrid, the resistance of the transmission line cannot be ignored and  $R_s$  should be considered in the source impedance. In addition, the inertia of the load could also affect the dynamical process.

#### <span id="page-17-1"></span>3.2.1 The effect of the source impedance  $L_s$ ,  $R_s$

If  $L_s$  and  $R_s$  are added in the system, the equation of boundary  $\varphi$  should be revised as

<span id="page-17-2"></span>
$$
\varphi : i_L = \frac{\frac{(L_f + L_s)P_{load}^2}{Cv_C^3} + v_C - v_s(t)}{\frac{(L_f + L_s)P_{load}}{Cv_C^2} - R_s}
$$
(3.4)

When  $R_s$  is neglected, the addition of  $L_s$  is the same as changing the value of L. Fig[.11](#page-21-0) shows the variation of the boundary with different  $L_s$ . In this figure, the boundary moves to the right as  $L_s$  increases, and the method proposed in Section 3.1 can be used to estimate the minimum initial capacitor voltage if replace the filter inductance L by  $L_s + L_f$ .

When only  $R_s$  is considered, it could let the denominator of Eq[.3.4](#page-17-2) equals to zero and change the boundary's shape. But if  $R_s$  is relatively low, this problem could be avoided, because the capacitor voltage which makes the denominator crosses zero is greater than  $v<sub>C</sub>(t)$ in the steady state. So the shape of the boundary corresponding to the low voltage is not changed. Fig[.12](#page-21-1) shows the variation of the boundary with different  $R_s$ . Since the intersection of the boundary and  $v_C$ -axis does not change, the estimation method in Section [3.1](#page-14-1) can't reflect the effect of  $R_s$ . However, the simulation results (Fig[.13\)](#page-21-2) indicates that the  $v_c(0)_{min}$ will increase linearly as  $R_s$  rises, or we can say the existence of  $R_s$  makes the capacitor voltage easier to collapse. This result is expected because the resistor reduces the changing rate of inductor current and consequently the capacitor will discharge more quickly.

### <span id="page-18-0"></span>3.2.2 The effect of the inertia element

In the section [2.2,](#page-12-0) an inertia element is set to represent the time response of a CPL depending on the parameter  $T_s$  (Eq[.2.5\)](#page-12-1). In practice, if the CPL refers to a voltage regulator, the time response to the input voltage or load shift could be several microseconds or even tens of nanoseconds. Compared to the source voltage, whose period is about 0.017s, the load can be treated as an instantaneous load  $(T_s \approx 0)$ .

If the CPL includes a DC/DC converter with voltage control, the time response could be hundreds of microseconds, so the inertia should not be ignored. According to Fig. 14,  $v_c(0)_{min}$ drops when  $T_s$  increases. This result is expected because the inertial element actually limits the change of the load current, thus it is easier for  $v<sub>C</sub>(t)$  to stop dropping at the beginning.

### <span id="page-18-1"></span>3.3 DISCUSSION ON THE SOLUTIONS FOR AVOIDING VOLTAGE COLLAPSE

There are several methods to prevent the rectifier from voltage collapse. The most straightforward way is to pre-charge the capacitor before operation. There are two main advantages for this solution:

- 1. Avoid the voltage collapse directly. The pre-charge voltage can be set close to the peak or average source voltage so that the estimation of  $v<sub>C</sub>(0)<sub>min</sub>$  could be unnecessary.
- 2. A high pre-charge voltage can reduce the inductor current at the start. From the phase portrait in Fig[.9,](#page-20-1) we can observe that the first cycle (red curve) is much larger than the other ones because the inductor has to generate a huge current to charge the capacitor to reach the voltage around the equilibrium point, which is also called the rush-in current of the capacitor. Pre-charge is commonly used in the converters to reduce this current no matter what the loads are.

Nevertheless, a main defect of the pre-charge is that some additional power source and facilities are required. Besides, especially for high-capacity converters, it takes a lone time to charge the capacitor before operation.

Another solution is the current protection which is also applied in many converters. Once the output voltage drops below a threshold, the load will be disconnected from the converter. If the current protection is applied, theoretically, there is no need to set a initial voltage for the capacitor. For the rectifier in this paper, current protection could be equivalent to precharge because the load is disconnected until the capacitor is charged to the threshold of the protection system. However, sudden disconnect and re-connect may not acceptable for some loads and , under some specific conditions, the spikes of the load current may appear if the protection threshold doesn't match the power level (Fig[.15\)](#page-22-0).



<span id="page-20-0"></span>Figure 8:  $v_C - i_L$  phase portrait of a rectifier with different  $v<sub>C</sub>(0)$ .  $P<sub>load</sub>$  =  $120W, v_s = |25\sqrt{2}sin(120\pi t)|, L =$  $600\mu H, C = 6mF$ . The cycles indicate the rectifier can operate normally while the blue trajectories mean the output voltage collapse happens



<span id="page-20-1"></span>Figure 9:  $v_C - i_L$  phase portrait of a rectifier with two different  $v<sub>C</sub>(0)$ .  $P<sub>load</sub> =$  $120W, v_s = |25\sqrt{2}sin(120\pi t)|, L =$  $600\mu H, C = 6mF$ . For the red trajectory,  $v_C(0)$  and  $v_C(t_0)$  are denoted.



<span id="page-20-2"></span>Figure 10: The boundary  $\varphi$  changes with different  $v_s(t)$ .  $P = 120W, L = 600 \mu H, C =$  $6mF, v_s(t) = |25\sqrt{2}sin(120\pi t)|$ 



Rs increases

<span id="page-21-0"></span>Figure 11: Boundary  $\varphi$  with different  $L_s$ .  $P_{load} = 200W, v_s = |25\sqrt{2}sin(120\pi t)|, L_f =$  $600\mu H, C = 6mF$ .  $L_s$  changes from 0 to  $300\mu H$ 

<span id="page-21-1"></span>Figure 12: Boundary  $\varphi$  with different  $R_s$ .  $P_{load} = 200W, v_s = |25\sqrt{2}sin(120\pi t)|, L_f =$  $600\mu H, C = 6mF$ .  $R_s$  changes from 0 to 0.3Ω.



<span id="page-21-2"></span>Figure 13: The relationship between  $v_C(0)_{min}$  and  $R_s$ .  $P_{load} = 200W, v_s =$  $|25\sqrt{2}\sin(120\pi t)|, L_f = 600\mu H, C = 6mF.$  $R_s$  changes from 0 to 0.3 $\Omega$ 



<span id="page-21-3"></span>Figure 14: The relationship between  $v_C(0)_{min}$  and  $T_s$ .  $P_{load} = 200W, v_s =$  $|25\sqrt{2}\sin(120\pi t)|, L_f = 600\mu H, C = 6mF.$  $T_s$  changes from 0 to 0.001s.



<span id="page-22-0"></span>Figure 15: The load current in the steady state when the current protection causes spikes.  $P_{load} = 400W, v_s = |25\sqrt{2}sin(120\pi t)|, L_f = 600\mu H, C = 6mF, v_C(0) = 0.$  The load is disconnected once  $v_C(t) < 0.8V_s$ .

#### <span id="page-23-0"></span>4.0 STEADY STATE ANALYSIS

The previous chapter discusses about the dynamical behavior of the rectifier when it starts with certain initial condition. In this chapter, it is assumed that the rectifier is able to operate with the convergence and its behavior in the steady state is studied.

### <span id="page-23-1"></span>4.1 THE STEADY STATE BEHAVIOR OF THE RECTIFIER WITH A CPL

The constant power load not only affects the convergence at the beginning of operation, it could also change the behavior of a rectifier in the steady state. To illustrate the effect of the CPL, another system is used as a comparison where the same rectifier is connected to a equivalent resistive load  $R_{eq}$ . The alternative load should consume the same power as the CPL in the steady state, which is expressed as

$$
P_{CPL} = P_R = \frac{1}{T} \int_{t}^{t+T} \frac{v_C^2(t)}{R_{eq}} dt
$$
\n(4.1)

A part of the simulation results is shown in Fig[.16.](#page-24-1) It can be observed that the CPL and  $R_{eq}$  share almost the same trajectories. What's more, other simulations with different parameters indicates that the inertia of the CPL may have no influence on the results. Therefore, in this case, it's hard to know the type of load by observing the input current of the rectifier in the steady state. In other word, we can use a resistor to represent a CPL in the steady state.



<span id="page-24-1"></span>Figure 16:  $v_C - i_L$  phase portrait and the plot of  $v_C(t)$  in the steady states.Both the results of CPL and  $R_{eq}$  are displayed in the same plot.  $P_{load} = 150W, v_s = |25\sqrt{2}sin(120\pi t)|, L_f =$  $600\mu H, C = 6mF.$ 

However, the rectifier with a CPL will have different characteristics if the CPL power increases. In Fig[.17,](#page-25-1) the trajectory corresponding to the CPL diverges into two cycles in the steady state, while the resistive load doesn't. This phenomenon is called bifurcation which is common in different types of converters. As the power continues to rise, the trajectory will bifurcate into more cycles until the voltage collapse happens.

### 4.2 THE ANALYSIS ON BIFURCATION

<span id="page-24-0"></span>For power converters, the bifurcation is noticed and analyzed in many researches. For example, [\[14\]](#page-34-2) presents the bifurcation in a buck converter with current-mode control but it dose not provide any explanation to the findings. [\[15\]](#page-34-3) provides simulation and experiment results of the bifurcation in a buck-boost converter. In these researches, some mathematical methods are proposed to determine the condition of bifurcation, but for now these methods are only suitable for LTI systems [\[16\]](#page-34-4) or fast-switching systems which can be linearized.



<span id="page-25-1"></span>Figure 17:  $v_C - i_L$  phase portrait and the plot of  $v_C(t)$  in the steady states. Both the results of CPL and  $R_{eq}$  are displayed in the same plot.  $P_{load} = 280W, v_s = |25\sqrt{2}sin(120\pi t)|, L_f =$  $600\mu H, C = 6mF.$ 

Many factors are involved to determine whether the bifurcation appears. In practice, since the power source and components of the rectifier are usually unchanged, the load power  $P_{load}$  is treated as the direct cause. Define that  $P_{TH}$  is the threshold and the bifurcation happens if  $P_{load} > P_{TH}$ . Therefore, the main task is to determine  $P_{TH}$  by other parameters including  $V_S, L_f$  and  $C_f$ . Unfortunately, it is hard to derive an exact relationship between  $P_{TH}$  and component parameters by mathematical equations. But simulation results illustrate some regulations which could provide some clues for the future study.

#### <span id="page-25-0"></span>4.2.1 The simulation results in ideal cases

In the ideal situation, both the source impedance and the inertia are not considered. Eighteen sets of simulation results are summarized in Fig[.18.](#page-26-1) For each time of simulation, different components  $(L_f, C_f)$  are used. In the figure,  $P_{TH}$  is an approximated value of the minimum load power when bifurcation appears. And  $v<sub>C</sub>$  is the average capacitor voltage when  $P_{Load} =$  $P_{TH}$ . The results indicate that if the source voltage is defined,  $P_{TH}$  should be found on a



<span id="page-26-1"></span>Figure 18: Summary of the simulation results.  $v_s = |25\sqrt{2}sin(120\pi t)|, L_f = 600 \mu H, C =$  $6m, v<sub>C</sub>(0) = 25V$ ,  $R<sub>s</sub>, L<sub>s</sub>$  and the inertia of CPL are not involved.

plane according to the filter inductance and capacitance, while the plane should only depend on the source voltage. At the same time, the averatge output voltage of the rectifier may have a linear relationship with the product of  $L_f$  and  $C_f$ , which indicates, when bifurcation starts, the output voltage could be determined by the cut-off frequency of the filter.

According to these findings, if the source voltage is known, the  $v_C - LC$  line and the plane can be obtained by at least three times of simulation or experiments. Then for any combination of  $L_f$  and  $C_f$ ,  $P_{TH}$  and the corresponding  $v_C$  can be estimated.

### <span id="page-26-0"></span>4.2.2 The effects of the non-ideal factors  $T_s$ ,  $R_s$

If the load is not equivalent to an instantaneous CPL, the inertia element should be added in the system, whose characteristic can be reflected by the parameter  $T_s$  in the inertia element (Fig[.6\)](#page-13-1). Meanwhile, source impedance also needs to be considered. The source inductance  $L_s$  is not studied because it can be combined with the filter inductance  $L = L_s + L_f$ . Then only the effect of  $R_s$  is studied.



<span id="page-27-1"></span>Figure 19: The change of  $P_{TH}$  and  $v_C$  when non-ideal factors are involved.

Fig[.19](#page-27-1) shows the effects of the parameters  $T_s$  and  $R_s$ . As the inertia of CPL increase, the threshold for bifurcation rises too, thus, if the CPL gets closer to an instantaneous one, the rectifier will be easier to face the bifurcation. In addition, the existence of source resistance could also increase  $P_{TH}$ . Recalling the conclusion in Section [3.2,](#page-17-0) although  $R_s$  leads the rectifier easier to face voltage collapse at the beginning, it brings a positive influence on the rectifier in the steady state.

It should be note that, the effect of non-ideal factors are considerable. But the linear dependency revealed in Section[.4.2.1](#page-25-0) does not change because the plots in Fig[.19](#page-27-1) also shows a linear relationship. So  $P_{TH}$  can be estimated by the method in the previous section when  $T_s$  and  $R_s$  are not zero.

### <span id="page-27-0"></span>4.3 THE PROBLEM BROUGHT BY THE BIFURCATION

In the steady state, even if the bifurcation appears, the rectifier and CPL connected can still operate normally unless the ripple of  $v<sub>C</sub>$  is too large. However, if we focus on the source side of the rectifier, some problems may appear. Since the diodes bridge is treated as an ideal switch, the input current  $i_{in}$  of the rectifier (denoted in Fig[.3\)](#page-10-2) should equals to the inductor current  $i_L$  but the polarities are different.

$$
i_{in} = \begin{cases} +i_{L}, & v_s > 0 \\ -i_{L}, & v_s < 0 \end{cases}
$$
 (4.2)

If the bifurcation appears, the waveform of  $i_{in}$  could be like Fig. 20. It's easy to see the



<span id="page-28-0"></span>Figure 20: Input current of the rectifier when the bifurcation appears

input current has a considerable DC component. When the load power is close to  $P_{TH}$ , the DC component is hard to observe unless using Fourier transform to obtain the frequency spectrum.

The most concerning problem is the DC-current injection to the power grid because it brings the transformer saturation. In each cycle, the core of transformer will be magnetized in on one direction according to the polarity of DC current. With the hysteresis nature, the core flux will increase until it reaches a maximum value, then the flux is hard to change, which means then voltage relationship between the coupled windings is no longer maintained and the transformer cannot transfer energy in this case[\[17\]](#page-34-5).

In order to explain this problem, a nonlinear single-phase transformer model is applied to supply the rectifier (Fig[.21\)](#page-30-0). A resistor (20 $\Omega$ ) is connected in parallel with the rectifier to accelerate the simulation. Parameters and magnetizing characteristics are listed in Table [1](#page-29-0) and Fig[.22.](#page-30-1) The simulation is conducted on the system with different load power. When the core flux of the transformer reaches its saturation flux, the simulation will stop because it is assumed the transformer loses its ability to transfer energy once the core saturates.

The results are presented in Fig. 23. When  $P_{load} = 255W < P_{TH}$ , there is no bifurcation

<span id="page-29-0"></span>Table 1: Transformer parameters

Nominal power	300 VA
Nominal voltage	$250/25$ V
Winding resistance	$0.0001$ pu
Leakage inductance $0.001$ pu	

in the steady state, so the transformer operates normally. Nevertheless, once  $P_{load} = 265W >$  $P_{TH}$ , an DC current component in the input current is observed. Then the excitation current increases significantly and the core flux reaches the saturation value after tens of seconds. Therefore, the bifurcation could cause the failure of the power grid in a short time especially when the CPL power takes a large proportion of the total load in a power system.



Figure 21: The circuit model including the transformer.

<span id="page-30-0"></span>

<span id="page-30-1"></span>Figure 22: The magnetization characteristic of the core (the elementary curve). The saturation flux is 1.2 p.u



<span id="page-31-0"></span>Figure 23: Relative states of the transformer when the load power is (a)255W and (b)265W. For each figure, the core flux, excitation current and the input current of the transformer's primary side are plotted

### 5.0 CONCLUSION

<span id="page-32-0"></span>The study of the rectifier with a CPL reveals that, the convergence of the system depends on the initial capacitor voltage. A method based on the reference  $\lbrack 6\rbrack$  is derived to estimate the minimum value of this voltage. The simulations show that both the source impedance and load inertia have an observable effect on the minimum initial voltage, which should be considered when estimating.

When the system operates in the steady state, in a low power level, there is no difference between a rectifier with a CPL and the one with a resistive load. However, if the load power is higher than a threshold, the bifurcation phenomenon appears. Although the bifurcation may not cause problem for the rectifier and CPL, it could inject DC current into the power grid, which brings the saturation and overheat of the transformer. Therefore, the bifurcation should be avoided in operation.

This topic still has much space for more researches. A significant limitation of this paper is that, it is hard to explain the findings of simulations by mathematical proofs. That is because the uncontrolled rectifier is a switched system which can't be analyzed directly as a LTI system. What's more, common averaging methods used for fast-switched system couldn't be applied to this case because the switched frequency of the rectifier is too low compared to its dynamic behavior we are interested. Therefore, in the future, one task is to find a suitable way to analyze the convergence and bifurcation phenomenon based on certain algebra method instead of simulations. Then try to derive a more accurate way to determine  $v<sub>C</sub>(0)_{min}$  for a convergent system and  $P<sub>TH</sub>$  for the bifurcation.

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