

# **Gallium Nitride Converters for Spacecraft Applications**

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# Gallium Nitride Converters for Spacecraft Applications

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University of Pittsburgh, 2019

This work presents the development and evaluation of several Point-of-Load (PoL) Gallium Nitride (GaN) high electron mobility transistor (HEMTs) based synchronous buck converters for computational loads in small spacecraft applications. Design modifications to existing controllers and their PCB layouts are discussed to maximize the benefits of GaN converters for these applications. The radiation performance of these converters and in-situ measurements is presented. This work also presents the development of a modular power system architecture for 1U CubeSat computing boards.

The PoL converters are based on the synchronous buck topology utilizing the Linear Technologies LTC3833 and the Texas Instruments LM25141-Q1 controllers, paired with the EPC 2014C, EPC 2015C, Teledyne TDG100E15B, and GaN Systems GS61004B GaN HEMTs. GaN devices are attractive to power electronics engineers due to their wide bandgap, low gate capacitance, and low ON resistance. GaN HEMTs also show promising performance in high radiation environments without the need for expensive radiation-hardened designs.

Several converters utilizing both commercial off-the-shelf products and radiation-hardened devices were developed and compared to the GaN converters to provide a performance evaluation between all of these devices.

**Keywords:** Point-of-Load, Gallium Nitride, High Electron Mobility Transistor, radiation-hardened, Commercial-Off-The-Shelf, synchronous buck converter, Small Satellite, CubeSat.

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## Preface

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The research conducted was made possible in part by the industry and government members of the NSF SHREC Center and the IUCRC Program of the NSF under Grant No. CNS-1738783. I would like to thank Dr. Javier Valle at Texas Instruments for supplying the TI TPS50601A-SP converter, Paul Traynham at Renesas for providing the ISL70001ASEH converter, and Teledyne e2v for donating the TDG100E15B GaN HEMTs for use in this research. Additionally, I would like to recognize the STP Houston team from providing support, design assistance, and flight opportunity. Finally, I also thank the University of Pittsburgh Central Research Development Fund for providing the funding for building several of the converters and equipment acquisition.

## 1.0 Introduction

With the increased number of commercial satellite launches in the past decade, the need for small, capable, and inexpensive processing systems and sensors has widened. Many in the space community are considering the move from multi-million-dollar projects to smaller, more replaceable satellites to accomplish their science objectives [13]. The space industry is set to expand to over \$8.8 billion dollars by 2030 fueled by the rapid increase in the number of small satellite launches and decreased costs resulting from rideshare companies and programs [13][7]. Many research and science experiments are currently on the International Space Station (ISS), which allows access to low Earth orbit (LEO) space with a reliable bus for communication and power [5][18]. With these more complex and ambitious experiments launching into orbit, a need exists for high-efficiency, compact, and inexpensive converters to power these missions. Converter power losses create significant heat and large package sizes waste valuable space that could be used for additional computational or remote sensing capabilities. These problems often require complex thermal and structural design trade-offs that increase mission complexity and cost.

The motivation of this work is the development of a full power system solution from CubeSat bus voltage generation down to directly generating FPGA core voltages [5][6]. Several experimental Gallium Nitride (GaN) based point-of-load (PoL) converters were designed to operate at 2.0 MHz with the bus power converters operating with an input voltage of 12 V and the direct FPGA converters operating with an input of 5V. The converters used for bus power generation were developed and tested with a 5V and 3.3V output which are common voltages for many experiments. The converters used for powering the FPGA are developed specifically for use on a new 1U-sized (10cm x 10cm) FPGA-based computing platform called the SHREC Space Processor (SSP), and looks at a variety of several PoL power electronic converters used to generate the 1.0V, 1.8V, and 3.3V voltages that are common for use in computational loads. The GaN converters are compared to a COTS Linear Technologies LTC7151S converter and two rad-hard converters, the Texas Instruments TPS50601A-SP and Renesas ISL70001ASEH. All converters are evaluated and compared for electrical and

thermal performance. For the proposed converters, an average efficiency of 87% to 91% is expected with comparable rad-hard converters reporting between 65% and 90% efficiency [19][11]. The increased efficiency represents a significant decrease in lost power and heat dissipation for space flight systems.

Converters with GaN high-electron mobility transistors (HEMTs) have shown considerable promise for LEO spacecraft applications. However, the current rad-hard controllers are typically very large and use older technologies that do not take full advantage of the high frequency capabilities of GaN HEMTs. Converters designed with COTs controllers and GaN HEMTs provide similar or higher efficiencies with lower volumes, mass, and cost when compared to conventional silicon based converters. This research takes advantage of the performance gains provided by commercial and flight-quality GaN HEMTs, and coupled with commercial fault-tolerant controllers to develop and test a set of converters for next-generation spacecraft electronics.

Finally, in-situ electrical performance measurements are presented of several GaN converters flying on the ISS as a part of the Department of Defense Space Test Program- Houston 6 (STP-H6) mission. As a sub-experiment of the experiment called Spacecraft Supercomputing for Image and Video Processing (SSIVP), three different GaN PoL buck converters will be evaluated throughout a multi-year mission on the exterior of the ISS [21]. Dedicated circuitry will measure the voltage and current to track each GaN PoL converters performance and degradation, enabling a multi-year characterization of efficiency and stability. Performing radiation testing on the COTS controllers and obtaining flight heritage should provide sufficient evidence for the viability of these converters for LEO CubeSat applications.

## 2.0 Motivation

The following section provides an overview of the design and layout of the power system for a CubeSat using PoL converters, the design of drop-on converter modules, and the design of a power system for an FPGA-based computing platform.

### 2.1 CubeSat Power System Layout

In general, CubeSat power systems and experiments on the ISS are powered off of a 28V bus. For experiments to interface with this bus an isolated power converter is used that offers protection and ease of interfacing for generating the experiments main voltage of 12V, 5V, or 3.3V. Isolated converters are generally more efficient for output voltages closer to 28V, which makes the generation of 5V and 3.3V bus voltages from 28V inefficient [5]. For example, on SSIVP power generation was performed with two isolated converters, each for generating 12V and 5V with a point of load converter used from the 5V rail for generating 3.3V. SSIVP's power system was on average 75.8% efficient. On Configurable Autonomous Sensor Processing Research (CASPR) experiment, a single isolated 28V to 12V converter is used with two PoL converters generating the 5V and 3.3V rails which has an expected system efficiency of 81.3%. By using this system a true single point ground isolation can be achieved as well as an increase in efficiency by 5.5%. The increase in efficiency allowed for more experiments to be performed on CASPR than if a dual isolated converter structure was used like SSIVP.

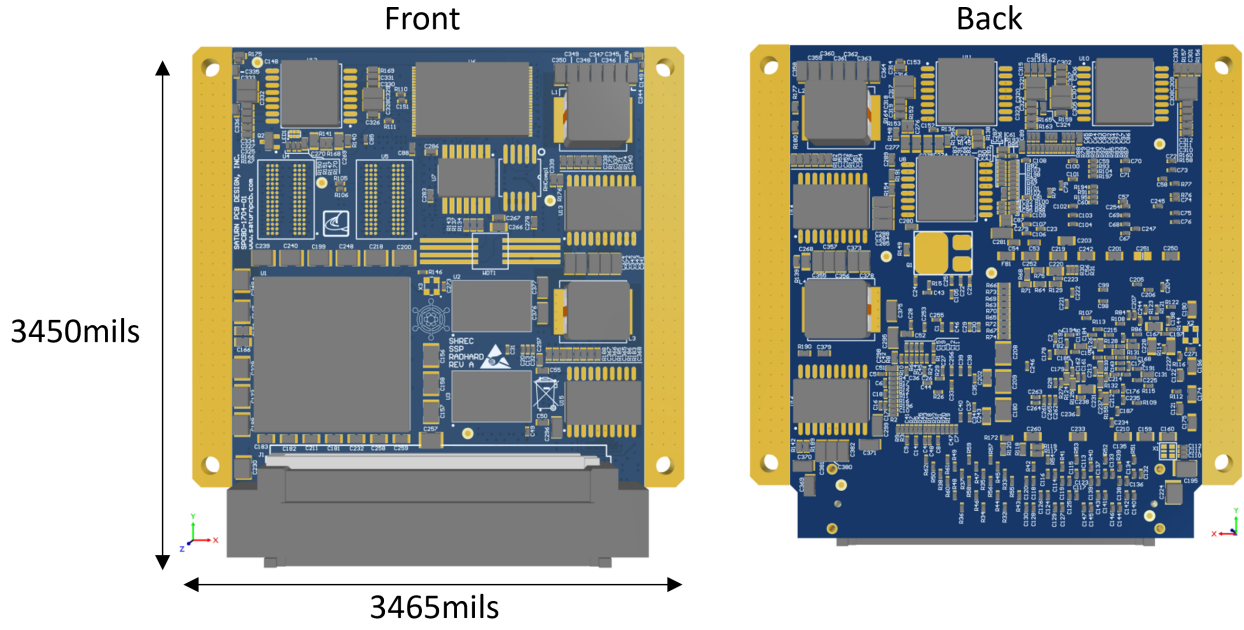
### 2.2 SHREC Space Processor

The CHREC Space Processor (CSP) is an inexpensive but highly reliable 1U-sized hybrid reconfigurable computing platform featuring a mix of COTS and rad-hard components aug-

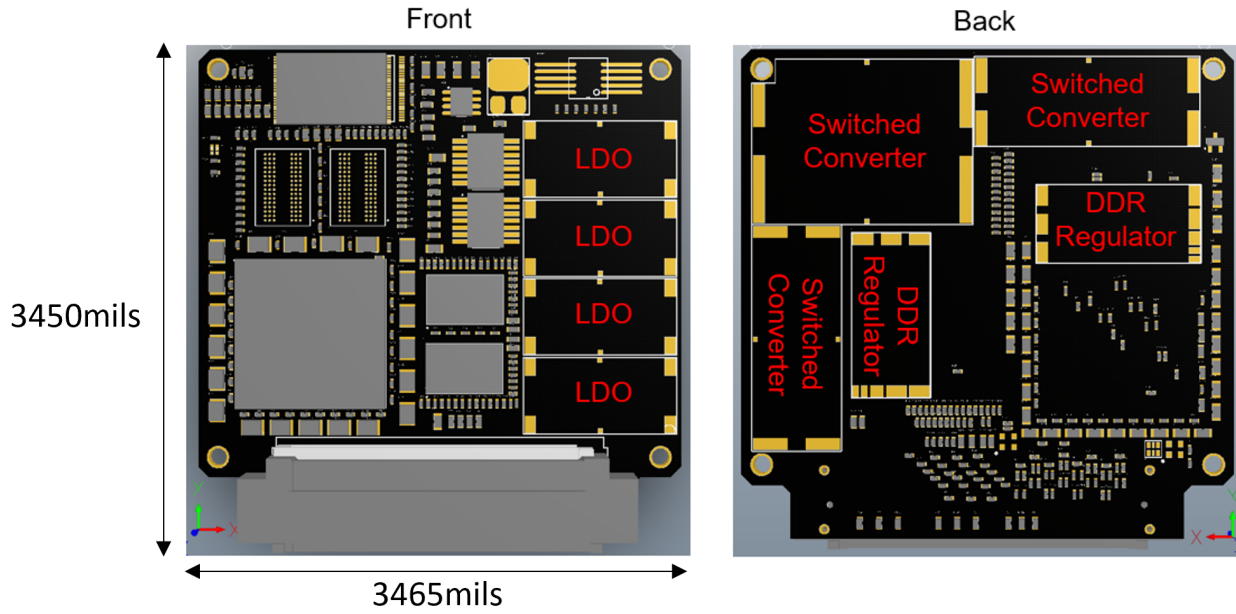
mented by fault-tolerant computing techniques developed by researchers at the NSF SHREC Center. The newest revision of this technology, the SHREC Space Processor (SSP), which builds upon the CSP, has four times more FPGA resources while maintaining the 1U form factor and is shown in Figure 2.1a. The original CSP used approximately 3.5W of power while the SSP can use up to 14W, due in part to the incorporation of multi-gigabit transceivers (MGTs) and a powerful Xilinx Zynq 7045 SoC. The increase in power required the use of a new power system architecture and different converters that were small yet powerful enough to meet increased demand. The SSP has up to 16GB of DDR3L RAM and 64GB of NAND flash for computational resources. A rad-hard watchdog monitors the heartbeat of the Zynq and power converters that can reset the Zynq in the event of a single-event latch up (SEL). The first use of the SSP will be on the STP-H7 mission to the ISS with the CASPR experiment and will be used as an image capture and processing device for several novel sensors. The CSP will act as a controller for the experiment due to its flight-proven design.

The SSP is powered from 5V and 3.3V voltage rails from 8 pins (14.4A) and 4 pins (7.2A) respectively of a SAMTEC 244 pin connector. A total of three switching converters are powered from the 5V rail and four low drop-out regulators (LDOs) powered from the 3.3V rail make up the power system of the SSP. All converters were designed to meet the operating criteria for the Zynq 7045 which has the capability to use over 20W of power with a base power draw of approximately 4W. Converter output ripple was to be minimized to 20mV, with load transient over and under-voltage response being designed to the strictest datasheet requirement of  $\pm 30\text{mV}$  for the 1.0V VCCPINT rail. The startup sequence of all converters and LDOs was designed according to the datasheet for each critical bank voltage. The 1.0V rail converter has the capability to draw approximately 10A with a maximum voltage overshoot of 30mV. Dual TI TPS50601A-SP 6A converters are used to supply the 1.0V rail. The 1.8V and 1.35V use single TI TPS50601A-SP converters and each of the rails are only expected to draw approximately 2.5A with a maximum overshoot of 90mV.

The SSP provides the framework for MGT protocols like SRIO and Aurora which are very high bandwidth communication and data-transfer interfaces. TI TPS7H1101-SP LDOs are used due to the tight voltage regulation requirements of 10mV for the protocols. MGTs require up to 1.9A of drive current and when powered off of 3.3V supplied LDOs makes for



(a) SSP Hybrid with Rad-Hard Power Converters



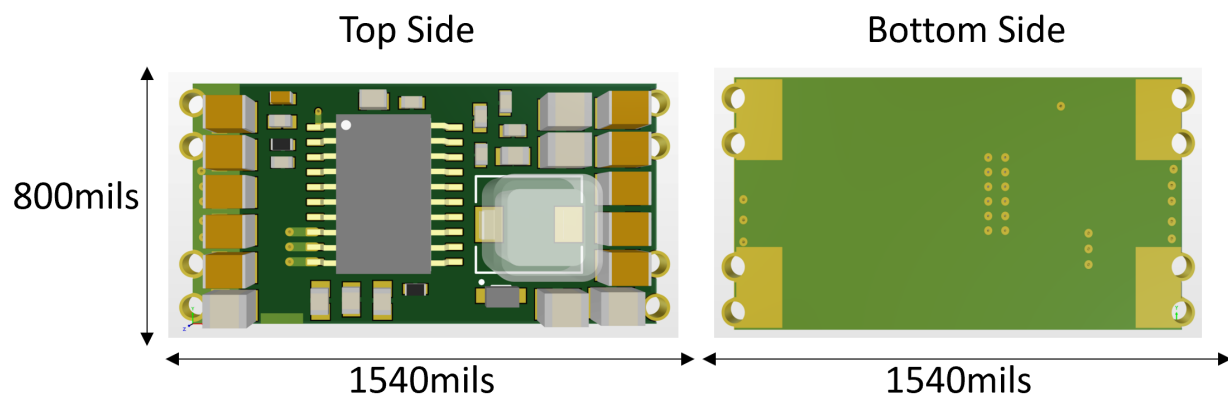
(b) SSP with Experimental Converter Module Layout

Figure 2.1: SSP PCB Layouts

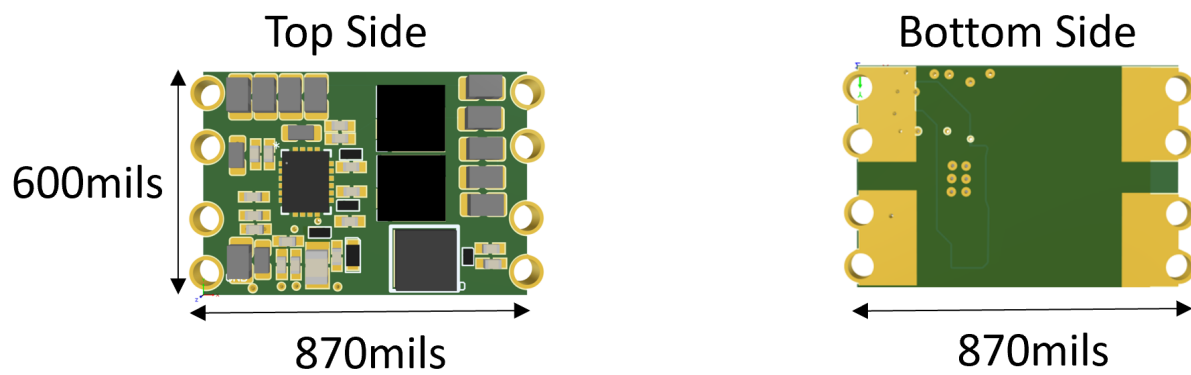
a system with significant power loss. Additionally, the SSP has four DDR3L modules, one NAND flash module, power sequencing circuitry, and a watchdog circuit. The DDR3L is arranged in two banks for the processing system (PS) and programmable logic (PL) sides of the Zynq SoC. Both DDR banks are powered from a 1.35V TI TPS7H3301-SP DDR regulator that produces the 0.675V reference voltage and can simultaneously sink or source up to 3A. Power sequencing is accomplished by cascading each converters and LDOs power good and enable signals with an RC time constant to power up the Zynq in the correct order. The watchdog works in conjunction with the power sequencing that in the event of an upset or latch up, the watchdog will power-cycle the Zynq forcing a restart.

### 2.3 Modular Power System Architecture

The CSP utilized a selective population parts scheme in order to employ both COTS and rad-hard components on the same PCB. This layout, while cost-efficient, wasted approximately 30% of the board space of the CSP. The SSP comes in two different versions, a full COTS solution and a hybrid solution featuring a mix of rad-hard and COTs components. An experimental version of the SSP is planned to use drop-on modules for all switched converters and LDOs that allows for COTS or rad-hard parts to be exchanged easily. If a converter goes bad or a part becomes unavailable, only the converter itself needs to be replaced and the whole board does not need reassembly. Only the input and output characteristics of the replacement module need to be matched. The drop-on module provides flexibility for converter manufacture selection as well as allowing for the potential use of more experimental GaN converters. Each module has connections for  $V_{in}$  and  $V_{out}$ , with individual GND connections as well as enable and power good signals used for power sequencing. Castellated vias and bottom-side pads are used for making the electrical connections, and non-conductive epoxy is used to increase the mechanical stability of the module. This style of module connection was successfully flown on the SSIVP experiment as part of the Department of Defense STP-H6 to the ISS in 2019 [5].



(a) Rad-hard module using Texas Instruments TPS50601A-SP



(b) GaN module using LTC3833 and GaN Systems GS61004B HEMTs

Figure 2.2: Drop-on Power Converter Modules

The modular converter power system offers several advantages for compute cards but also proposes some new challenges, namely mounting inductance, mechanical security, and thermal mitigation. By separating the power converter to a module, the electrical mounting pads ideally would be kept as short and wide as possible for decreased mounting inductance and increase structural and thermal contact. However, the large pad size requires a significant amount of board space taken up with unmasked copper, preventing any potentially necessary vias from being added into the board. The pad layout shown in Figure 2.2a was chosen to provide a 150mil by 250mil area for each pad with several vias to provide better electrical and thermal paths. Each pads connection can handle 20A with an inductance is 1.16nH and its thermal impedance is 9.9°C/W, with a total module thermal impedance of 2.5°C/W. Since the converters are relatively lightweight with a low center of mass, mechanical stability is less of a concern with epoxy used for added mechanical strength.

### 3.0 GaN Technology

While the space power electronics industry has primarily been dominated by silicon technologies, radiation testing of GaN has shown positive radiation performance while simultaneously offering better switching performance compared to silicon [28][17]. GaN devices provide comparable or higher efficiencies with lower volumes, mass, and cost when compared to conventional silicon rad-hard converters. The GaN high electron mobility transistors (HEMTs), which are a type of heterojunction field-effect transistor, tested in this paper are shown in Table 3.1.

The GaN devices under test are the EPC2014C, EPC2015C, GaN Systems GS61004B, and Teledyne TDG100E15B. These transistors are paired with the Linear Technologies LTC3833 and the Texas Instruments LM25141-Q1 synchronous buck controllers [3][4][24].

#### 3.1 Power Electronic Performance

GaN HEMTs allow electrons to move freely in the device as a 2D gas and which provides a fast gate turn-on [17][15][23]. In power electronic devices, GaN HEMTs offer several advantages over silicon, primarily with a significantly wider band-gap of 3.4eV compared to the 1.12eV gap of silicon [15]. The large band-gap energy allows GaN devices to operate at a higher temperature, despite poorer thermal conductivity [9]. Manufacturers have been able to improve GaN thermal conductivity with advanced packaging techniques, and have been able to achieve similar performance levels as silicon [25][14]. The larger energy gap also allows the physical depletion region of the transistor to shrink while maintaining a high blocking and breakdown voltage. The smaller depletion region has the added benefit of reducing ON resistance that improves the efficiency of switching converters during conduction. The small gate capacitance of GaN HEMTs allow switching at much higher frequencies with lower losses than silicon, making them very popular for radio frequency (RF) amplifier applications [23]. GaN HEMTs have no body diode due to manufacturing, eliminating diode reverse

recovery loss during switching, further improving efficiency [12]. With the combination of low gate capacitance and high-voltage switching capabilities, GaN allows designers to increase switching frequency that reduces magnetic device sizing and maintain the same output power of a silicon-based converter. GaN transistors are approximately 1/10th the size of a comparable silicon MOSFET, and providing the same or better performance in terms of voltage rating, current rating, and ON resistance [16]. The smaller package also decreases package inductances and ringing observed during switching that allows for stability margins to be increased. The ability to decrease the size and weight of a converter while maintaining power output makes them an attractive option for space.

Historically, manufacturing difficulties of GaN FETs led to higher costs, by a factor of three when compared to silicon devices, but recent advancements in manufacturing technology have driven costs down [14]. As a result of their innate radiation tolerance, special packaging is not needed to improve radiation fault tolerance, enabling more efficient operation at MHz switching frequencies that would be prohibitively inefficient to achieve with traditional silicon rad-hard components [16]. Most rad-hard converters using silicon operate in the 100 - 500 kHz range [11][5]. By operating in the MHz range, inductors and capacitors can be scaled down by an order of magnitude further reducing converters size and weight. The properties of GaN HEMTs provide several advantages to a very promising replacement transistor for space flight and for continued mission success of the CubeSat platform.

### 3.2 Radiation Performance

The construction and material properties of GaN HEMTs provide several advantages over silicon when operating in harsh radiation environments without the need for special manufacturing or design techniques [2][8]. Four main types of semiconductor radiation effects can impact the performance of a transistor: total ionizing dose (TID), single event effects (SEEs), dose-rate radiation, and radiation displacement damage [17]. Throughout the duration of a mission, TID develops from high-energy particles or photons passing through the oxide layer on a transistor that eventually leads to an accumulation of charge build-up at both the gate

and field oxide. The charge build-up causes the device to activate without a gate drive signal being applied. GaN HEMTs are manufactured with a Schottky metal gate that eliminates most TID effects by allowing the charge build-up to dissipate [28]. SEE effects are mitigated by the wide bandgap of GaN HEMTs due to the much higher energy that is required for energetic ions to deposit in the material of the semiconductor to form the electron-hole pairs that induce SEEs. The smaller depletion region volumes of GaN HEMTs collect less charge, reducing the probability of dose rate radiation effects. Radiation displacement damage caused by high energy protons displacing semiconductor atoms in the semiconductors crystalline lattice has shown to very rarely impact the functionality of GaN HEMTs [28]. GaN HEMT devices have shown sensitivity to neutron radiation displacement damage that causes an increase in ON resistance and bias current while decreasing the sustained blocking voltage [17][29]. When selecting GaN HEMTs for power electronic applications, the devices should be appropriately de-rated to account for the decrease in performance resulting from radiation effects over the lifetime of the mission. Testing at the NASA Jet Propulsion Laboratory (JPL) has shown that GaN HEMTs are extremely resistant to both radiation-induced TID and SEEs. However, more significant testing is necessary if GaN HEMTs are going to be used in a LEO, such as for the SSP [22].

Table 3.1: GaN HEMT Parameters

<b>Parameter</b>	<b>EPC EPC2014C</b>	<b>EPC EPC2015C</b>	<b>GaN Systems GS61004B</b>	<b>Teledyne TDG100E15B</b>
Drain-Source Voltage	4.5 - 40V	4.5 - 40V	3.8 - 100V	3.8 - 42V
Continuous Drain Current	10A	53A	45A	15A
Threshold Gate- Source Voltage	1.4V	1.4V	1.6V	1.3V
Maximum Gate- Source Voltage	6V	6V	7V	7V
Minimum Gate- Source Voltage	-4V	-4V	-10V	-10V
ON Resistance	16m $\Omega$	4m $\Omega$	15m $\Omega$	19m $\Omega$
Gate Charge	2.5nC	8.7nC	6.6nC	6.2nC
Package Type	Passivated BGA Die	Passivated BGA Die	GaNpx	SMD 0.5 Ceramic

## 4.0 Converter Design

The GaN HEMTs in Table 3.1 are paired with the Linear Technologies LTC3833 and Texas Instruments LM25141-Q1 synchronous buck controllers and are then compared to a silicon COTS Linear Technologies LTC7151S converter and two rad-hard buck converters, the Renesas ISL70001ASEH, and Texas Instruments TPS50601A-SP. These converters are all excellent examples of the current market offering [27][11][19]. All major parameters of the converters under test are listed in Tables 4.1 and 4.2.

### 4.1 Synchronous Buck Converter

The synchronous buck converter operation drives two gates instead of a single gate and allowing the natural forward drop of a diode operate as a switch as shown in Figure 4.1. This provides more control over how the device operates and also allows for operation at high efficiency. Control becomes more of an issue requiring a certain amount of dead-time is added in between firing the top and bottom gates so a source shoot-through state is not achieved.

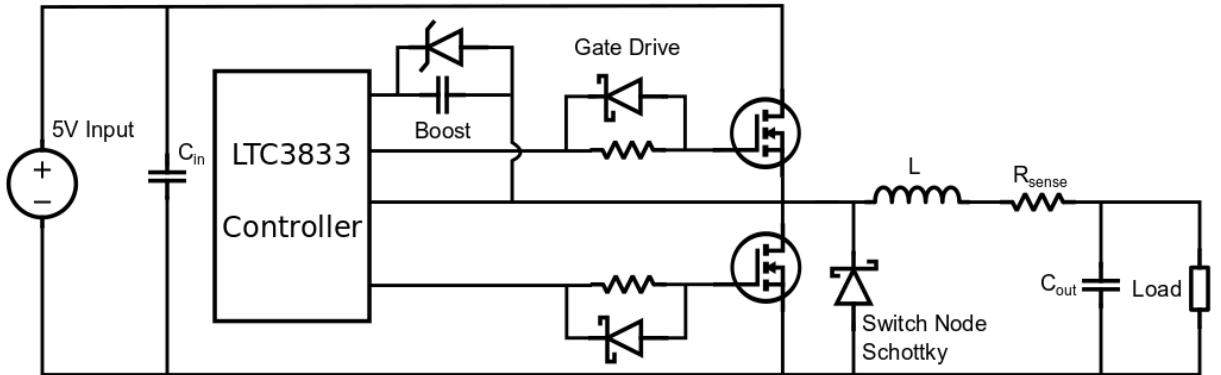


Figure 4.1: Synchronous Buck Converter Schematic

## 4.2 Device Selection and Design

This section provides an overview of the FPGA and Bus voltage converter that were used for all experiments highlighting the features of the GaN, rad-hard, and COTS devices.

### 4.2.1 COTS Converters

The Linear Technologies LTC7151S was selected as a representative COTS converter for incorporating several features that modern power converters have such as soft start, low EMI emissions, and monolithic integrated MOSFETs. The LTC7151S is capable of operating with a 400kHz to 3MHz switching frequency and delivers up to 15A at high- efficiency thanks to the integrated capacitors of the Silent Switcher 2 architecture. Datasheet and LT PowerCAD values were used to develop the simulation model and a 0.25H inductor was selected with a switching frequency of 500kHz.

### 4.2.2 Rad-Hard Converters

The Texas Instruments TPS50601A-SP and the Renesas ISL70001ASEH both feature soft-start, power good and enable signaling, monolithic integrated MOSFETs, and hermetic/ceramic packaging. Both converters are rated for 100krad of TID and 75MeV-cm<sup>2</sup>/mg and 86.4MeV-cm<sup>2</sup>/mg SEL for the TPS50601A-SP and ISL70001ASEH, respectively.

The TPS50601A-SP uses cycle-by-cycle current limiting on the high-side FET combined with low-side FET sourcing current limiting to protect the converter during overload and current runaway situations. The controller incorporates input and output voltage regulation with power good monitoring for protecting the device and load during voltage transients. Over-temperature is monitored and the converter will automatically turn OFF and soft start turn ON when the temperature is 10°C below the thermal trip point. The TPS50601A can be synced with another device to double the current output of the converters to 12A. The TI converter was designed with a 3.3μH inductor with a 500 kHz switching frequency.

The ISL70001ASEH has input under-voltage, output under-voltage, and output over-current protection to protect the device and load. The converter can be synchronized with

other devices  $180^\circ$  out of phase to lessen source RMS current ripple, improving efficiency and reduce EMI. The Renesas converter was designed with a  $1\mu\text{H}$  inductor with a 1MHz switching frequency.

### 4.2.3 GaN Converters

The PoL synchronous buck converters were selected based on prior performance in radiation environments. The Linear Technology LTC3833 has been tested as a PoL converter in the Large Hadron Collider (LHC) at CERN, and has shown promise in resisting the effects of SEE, TID, and strong magnetic fields [1]. The silicon process technology of the Texas Instruments LM25141 is expected to survive the radiation environment in LEO. The selected GaN HEMTs were chosen to provide high efficiency over the full converter range in both high-density commercial and flight-proven hermetic packages. Parameters for the selected controllers and GaN HEMT devices are given in Table 3.1 and Table 4.1, respectively.

The Linear Technologies LTC3833 synchronous buck controller, shown in Figure 4.1, can operate on a very wide voltage range up to 38V with a fast load transient response and up to 2MHz switching frequency [26]. The LTC3833 has fixed dead-time logic to safeguard the top and bottom gates from turning ON simultaneously, eliminating shoot-through and damage to the HEMTs. The controller features soft start or output voltage tracking and provides output overvoltage protection, programmable current limit with foldback, power good and enable signaling for power sequencing. Discontinuous conduction mode or pulse-skipping mode is allowable if the load current is less than half of the peak to peak inductor current ripple, which is a variable frequency mode. The LTC3833 senses inductor current with either a sense resistor or an RC circuit across the inductor (DCR sensing). The sense resistor is a more accurate measurement and is used for all GaN converters in this paper, but DCR is more energy-efficient and saves on large high-power sense resistors. The overall converter design and GaN devices selected for this paper are similar to those that were used in the SSIVP experiment on the STP-H6 mission [5]. The EPC2014C is the same part as that used on SSIVP and the GaN Systems GS61004B is functionally similar to the Teledyne TDG100E15B with parameters shown in Table 3.1. The EPC2015C was selected for use due

to its higher current carrying capabilities and lower on-resistance over the EPC2014C while still being 40V rated. Both EPC GaN HEMTs have a maximum gate drive voltage of 6V while the GaN Systems HEMT has a maximum of 7V. Testing at NASA JPL has shown the 40V rated EPC GaN HEMTs perform very well during radiation testing [22].

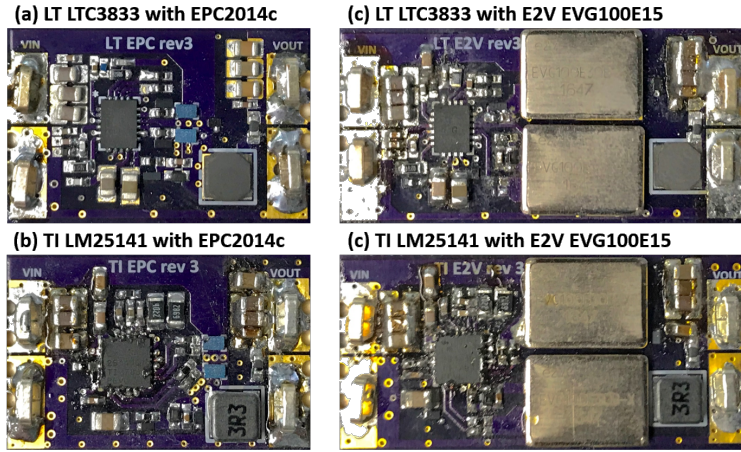
The Texas Instruments LM25141-Q1 has a wide operating range up to 42V with a minimum output voltage of 1.5V. The LM25141-Q1 is capable of operating at 2.2MHz with gate drive slew rate control to reduce EMI. At light and no load conditions it operates in a skip cycle mode for improved low power efficiency. The control method is peak current-mode control which provides inherent line feed-forward, cycle-by-cycle current limiting, and ease of loop compensation [10].

A key challenge of driving GaN HEMTs is controlling the gate-source voltage overshoot during device turn-on. To prevent this overshoot, a gate drive resistor and parallel Schottky diode was used to slightly slow the rise-time of the gate drive and reduce its magnitude. The Schottky diode provides a discharge path during device turn OFF, reducing switching losses and minimizing Miller turn-on effects. A 5.1V clamping Zener diode was added across the boost capacitor to ensure the high-side drive voltage does not drift during system transients. A 40V protection Schottky diode was added at the switching node to prevent over-voltage of the GaN HEMTs.

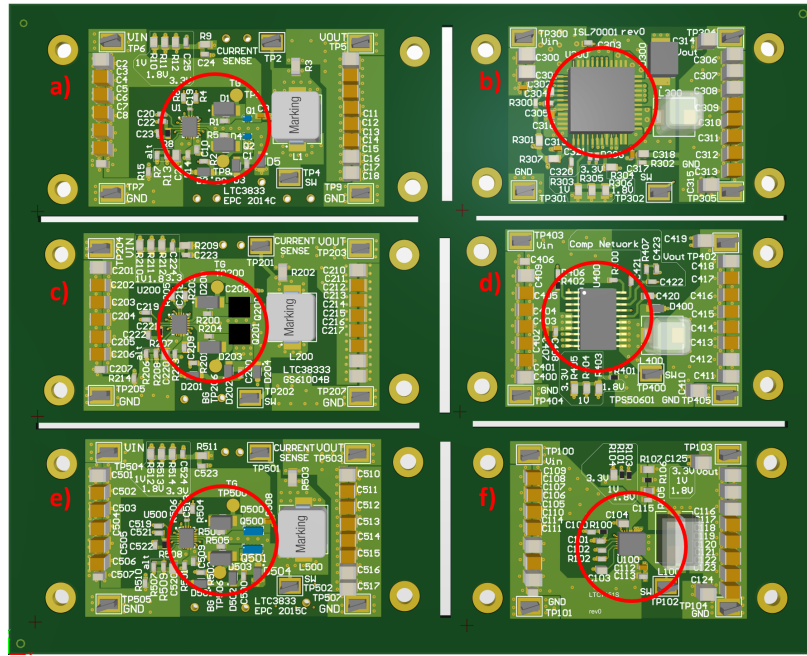
### 4.3 PCB Development

The FPGA converter PCBs were designed for experimental usage and to take measurements as shown in Figure 4.2, but similar designs for processor applications were also developed. The primary differences between the layouts include the removal of several test points and electrical contacts that reduced the total area by 40% as shown in Figure 2.2b.

The experimental FPGA converter boards have an average size of 2.5 x 2 using a four-layer stack-up of (Top) signal/power, (Layer 1) ground, (Layer 2) signal/power, (Bottom) power/ground. The application layouts have an average size of 1.54 x 0.80 for the TI TPS50601A-SP converters and 0.6 x 0.87 for a LTC3833 using GaN Systems GS61004B



(a) Assembled Bus Voltage Converters



(b) PCB Panel with converters under test: a) LTC3833 EPC2014C, b) ISL70001ASEH (Rad-hard), c) LTC3833 GaN Systems GS61004B, d) TI TPS50601A (Rad-hard), e) LTC3833 EPC2015C, f) LTC7151S (COTS). The red circle is a 1in diameter for scale.

Figure 4.2: Power Converters Under Test

HEMTs. Bulk input and output capacitance on all boards utilize ceramic  $47\mu\text{F}$ , 10V rated and  $10\mu\text{F}$ , 50V rated X7R capacitors in 1210 packaging. All other capacitors used are automotive-grade 50V rated or higher with X7R dielectric.

The bus power converters were designed for a 30% ripple current at 2.5 A. The inductor for the LTC3833 controller was the Taiyo Yuden  $2.2\mu\text{H}$  with a rated current of 2.5 A and a DC resistance of  $80\text{m}\Omega$ . The inductor for the LM25141 controller was the Würth Elektronik  $3.3\mu\text{H}$  with a rated current of 3.23 A and a DC resistance of  $33\text{m}\Omega$ . The inductors were selected based on manufacturer recommendations from the datasheets. However, depending on the application, the inductor can be sized appropriately to further optimize efficiency based on the desired load current, ripple current, and package dimensions. With a maximum input voltage of 38 V, the bypass capacitors were selected with a 50 V rating to allow future testing at 28 V, a common de-rating practice. High quality ceramic capacitors were selected based on trade-offs between size, performance, parasitics, and serviceability.

The bus power converter PCBs, shown in Figure 4.2a, were designed using a 4-layer stackup and manufacturing tolerances that include a 10 mil minimum via diameter with a 4 mil annular ring. The stackup of the test converter PCBs were designed to provide optimal performance at minimal cost: (Top) signal/power, (Layer 1) ground, (Layer 2) signal/power, (Bottom) ground. Castellated vias were placed at the input and output terminals to allow the converter PCB to act as a drop in power supply module that can be easily modified to meet the needs of individual missions.

During the PCB layout process, focus was placed on minimizing the footprint area for each GaN HEMT for two primary reasons: reduced harmonic content of high switching frequency, and address area constraints for CubeSat applications. Gate drive traces are as short and wide as feasibly possible to minimize inductance that can induce ringing on the gate. Since the switching node between the source and drain of the GaN HEMTs is also switching at high frequency, vias were designed to reduce inductance to the internal plane that provides a low impedance connection with high-current handling capability. Additionally, isolation of sensitive traces required for converter control becomes difficult as the dimensions of the PCB are reduced.

The PCB stackup was designed to provide a solid ground return path directly under the high frequency and high current traces that prevent coupling. Sensitive signals were carefully routed on the internal layer to increase the noise immunity of sensing signals.

The difficulties associated with mechanical and electrical parameters for CubeSat applications are well known. The proposed converter layouts represent a significant reduction in the average area (54%), volume (79%), and weight (84%) when compared to other representative PoL radiation-tolerant converters. Mechanical parameters are provided in Table 4.3.

#### 4.4 Test Setup

The FPGA converters were designed to operate with an input voltage of 5V and output voltages commonly used by modern processors of (1.0V, 1.8V, 3.3V) and corresponding currents ( $<6A$ ). While the GaN and COTS converters are capable of operating at much higher output currents, the limitation was imposed to simulate a CubeSat environment. All converters were simulated and measured for their turn ON and turn OFF transient behavior, load change transient response, full load and no-load output voltage ripple, switching waveforms, and efficiency. Thermal measurements were performed at an ambient temperature of 27°C from steady-state operation at a constant output current. Measurements were taken with a Tektronix MSO64 2.5GHz oscilloscope, Fluke 115 multimeter, Rigol DL3021 electronic load, BK-Precision 9183B DC power supply, and a FLIR E8 thermal imaging camera as shown in Figure 4.3.

The characterization of the proposed bus power converter PCBs was performed using the test setup shown in Figure 4.3. A B&K Precision 9183B DC power supply was configured to output a constant 12 V supply to the converters. An AMETEK SLH series electronic load was programmed to incrementally step converter load current for efficiency measurements. Load currents were verified with a Fluke 115 multimeter that was placed in series with the converters. Oscilloscope measurements on the test converter PCBs were taken on a Tektronix DPO7254 2.5 GHz to minimize distortion of the high-frequency switching signals.

Table 4.1: Bus Voltage Generation PoL Converters

Parameters	Converters			
	LT LTC3833 with Teledyne TDG100E15B	LT LTC3833 with EPC 2014c HEMT	TI LM25141-Q1 with Teledyne TDG100E15B	TI LM25141-Q1 with EPC 2014c HEMT
Input Voltage Range	4.5V to 38V	4.5V to 38V	3.8V to 42V	3.8V to 42V
Output Voltage	3.3V, 5V	3.3V, 5V	3.3V, 5V	3.3V, 5V
Maximum Output Current	2.5A	2.5A	2.5A	2.5A
Switching Frequency	1.887MHz	1.887MHz	2.2MHz	2.2MHz
Inductor	3.3 $\mu$ H	3.3 $\mu$ H	2.2 $\mu$ H	2.2 $\mu$ H
Input Capacitance	4.1 $\mu$ F	4.1 $\mu$ F	4.1 $\mu$ F	4.1 $\mu$ F
Output Capacitance	6.7 $\mu$ F	6.7 $\mu$ F	6.7 $\mu$ F	6.7 $\mu$ F
Compensation Network	24.3k / 56pF / 0.1 $\mu$ F	24.3k / 56pF / 0.1 $\mu$ F	1k / 10nF / 43pF	1k / 10nF / 43pF
Thermal Operating Range	-40°C to 125°C	-40°C to 125°C	-40°C to 125°C	-40°C to 125°C
Radiation Tolerance	Potentially Suitable for LEO	Potentially Suitable for LEO	Potentially Suitable for LEO	Potentially Suitable for LEO
FET Technology	GaN, External	GaN, External	GaN, External	GaN, External
Package Size	3.5mm x 4.5mm	3.5mm x 4.5mm	4.1mm x 4.1mm	4.1mm x 4.1mm
FET Dimensions	7.54mm x 10.16mm	1.1mm x 1.7mm	7.54mm x 10.16mm	1.1mm x 1.7mm
Watt/mm <sup>2</sup>	0.139	0.709	0.134	0.669

Table 4.2: FPGA Voltage Generation PoL Converters

Parameters	Converters					
	TI TPS50601A-SP	Renesas ISL70001ASEH	LT LTC7151S	LT LTC3833 with GaN Systems GS61004B HEMT	LT LTC3833 with EPC 2014c HEMT	LT LTC3833 with EPC 2015c HEMT
Input Voltage Range	3V to 7V	3V to 5.5V	3.1V to 20V	4.5V to 38V	4.5V to 38V	4.5V to 38V
Output Voltage	1V, 1.8V, 3.3V	1V, 1.8V, 3.3V	1V, 1.8V, 3.3V	1V, 1.8V, 3.3V	1V, 1.8V, 3.3V	1V, 1.8V, 3.3V
Maximum Output Current	6A	6A	15A	20A	10A	20A
Switching Frequency	500kHz	1MHz	500kHz	2MHz	2MHz	2MHz
Inductor	3.3 $\mu$ H	1 $\mu$ H	0.25 $\mu$ H	0.33 $\mu$ H	0.33 $\mu$ H	0.33 $\mu$ H
Input Capacitance	141 $\mu$ F	101 $\mu$ F	121 $\mu$ F	103.3 $\mu$ F	103.3 $\mu$ F	103.3 $\mu$ F
Output Capacitance	494 $\mu$ F	470 $\mu$ F	530 $\mu$ F	140 $\mu$ F	140 $\mu$ F	140 $\mu$ F
Compensation Network	6.81k / 100pF / 6800pF	Internal	10k / 22pF / 1nF	16.5k / 100pF / 670pF	16.5k / 100pF / 670pF	16.5k / 100pF / 670pF
Thermal Operating Range	-55°C to 125°C	-55°C to 125°C	-40°C to 125°C	-40°C to 125°C	-40°C to 125°C	-40°C to 125°C
Radiation Tolerance	100krad, 75MeV	100krad, 86.5MeV	N/A	Potentially Suitable for LEO	Potentially Suitable for LEO	Potentially Suitable for LEO
FET Technology	Si, Internal	Si, Internal	Si, Internal	GaN, External	GaN, External	GaN, External
Package Size	10mm x 13mm	14.5mm x 14.5mm	4mm x 5mm	3.5mm x 4.5mm	3.5mm x 4.5mm	3.5mm x 4.5mm
FET Dimensions				4.6mm x 4.4mm	1.1mm x 1.7mm	4.1mm x 1.6mm
Watt/mm <sup>2</sup>	0.155	0.094	0.75	0.267	0.770	0.672

Table 4.3: Converter Size and Weight Measurements

<b>Configuration</b>	<b>GaN HEMT</b>	<b>Area (in<sup>2</sup>)</b>	<b>Volume (in<sup>3</sup>)</b>	<b>Weight (g)</b>
Test Bus	EPC 2014c	0.62	0.09	2.32
Converter	TDG100E15B	0.85	0.11	4.74
Flight Bus	EPC	0.41	0.05	1.31
Converter	TDG100E15B	0.64	0.09	3.76
Representative Rad-Tolerant PoL Converter	-	1.16	0.31	16.00



Figure 4.3: Test Setup for Converter Measurements

## 5.0 Converter Testing

The following section covers all of the simulated and measured results of the converters under test. All converters were simulated and measured full load and no-load input and output voltage ripple, switching waveforms, and efficiency. Thermal measurements are taken at an ambient temperature of 25°C in still air operation. Additionally, the FPGA converters were simulated and measured for their turn ON and turn OFF transient behavior and load change transient response and the bus power converters were simulated and measured for their inductor current ripple.

### 5.1 Bus Voltage Generation

This section provides an overview of the bus voltage converters simulation, hardware, and thermal measurements performed on various GaN based converters.

#### 5.1.1 Simulation Results

The proposed converter topologies with SPICE models were obtained from and simulated in LTspice prior to manufacturing, ensuring the proposed topologies would operate within the design specifications. Each simulation was configured with the previously discussed design parameters, however only SPICE models for the EPC GaN HEMTs were commercially available. Individual simulations were used to evaluate a wide range of common converter parameters including: gate switching waveforms, inductor current ripple, and output voltage ripple. The waveforms for the LTC3833 controller and the EPC2014c converter topology are presented for 5 V and 3.3 V output voltages.

Simulations with the LTC3833 with the EPC2014c converter that was designed to regulate 12 V to 5 V driving a fixed load  $4.7\Omega$  load, as shown in Figure 5.2. An average steady state inductor current of 1.05 A was observed with a current ripple of 771 mA that corre-

sponds to 31% ripple. The simulation produced an output voltage of 4.95 V with a ripple of 6 mV ripple or approximately 0.1%. The gate voltage waveforms switched at 1.9 MHz with the top gate turning on slightly slower than the bottom gate, resulting from the  $5\Omega$  resistor placed in between the controller and the gate of the EPC2014c. No overshoot is observed since the simulation model does not account for trace and package inductance which are the primary factors impacting overshoot in high frequency converters. The results for the LTC3833 converter, configured to output 3.3 V under similar operating conditions as the 5 V converter, are shown in Figure 5.1. The output voltage ripple (0.1%) and inductor ripple current (28.1%) matched closely with the values predicted by the proposed design with a percent error of 5.2%. Similar results were observed with other controller and GaN HEMT configurations, with the proposed design and simulation data being consistent to within 3% for both LTC3833 and LM25141 controllers.

### 5.1.2 Hardware Results

Measurements were taken on the LTC3833 converter using EPC2014c GaN HEMTs that was configured to output 3.3 V, and the electronic load was programmed to sink 1 A. The data taken on this converter directly relates to Figure 5.3 but other converter configurations were found to have comparable waveforms and therefore their plots are omitted. Inductor current measurements were performed differentially across a  $0.015\Omega$  current sense resistor, and an 8 mV voltage drop was measured, corresponding to a 26.7% ripple as seen in Figure 5.3b. The measured ripple matches within 1.5% of the simulated converter. The output voltage ripple measurements of 13.2 mV were consistent with predicted and simulated results, representing less than 0.5% ripple as seen in Figure 5.3a. Measurements on the LM25141 controller provided an output voltage ripple less than 1%. If the degree of voltage ripple can be maintained for a 28 V input voltage with only minor component changes, the proposed converters may be suitable for use as direct PoL converters for other computational devices, such as processors or FPGAs [31].

As discussed previously, the gate of the GaN HEMT is expected to experience some ringing during turn-on and turn-off states, resulting from trace inductance and package

parasitics. The gate voltage oscilloscope waveforms in Figure 5.3d and Figure 5.3c show significant overshoot and undershoot on both the top gate and bottom gate. The  $5\Omega$  resistor on the top gate is successful in reducing overshoot, which is of primary concern for the top gate since the source node of the GaN HEMT is connected to the controller switching node. The bottom gate is inherently more tolerant to ringing because the source of the GaN HEMT is connected to ground. A  $0\Omega$  resistor was placed between the controller and the bottom gate to switch the transistor faster. As such, significant ringing was observed on the bottom gate during turn-off. However, all measured gate voltages are within the tolerances provided by EPC and E2V.

The 5 V test converters produced consistently high efficiencies ranging from 89% to 96% across the measured load currents seen in Figures 5.4. As expected, the measured efficiency of the 3.3 V converter was less than the 5 V converter, but measured efficiency values ranged from 72% to 85%. Both 5 V and 3.3 V high frequency GaN HEMT converter topologies performed nearly 20% better than commercially available rad-tolerant converter designed to regulate the same input and output voltages. In both 5 V and 3.3 V converter configurations, the EPC2014c performed consistently better with higher efficiencies when compared to the TDG100E15B, and was expected as a result of the hermetically sealed package.

### 5.1.3 Thermal Results

High-frequency GaN converters show promise for CubeSat missions in part because of the smaller package dimensions. However, the size reduction can increase thermal stresses placed on components that may negatively impact the rated lifetime, even in the presence of higher efficiencies. Analysis of the converters steady state thermal performance can provide insight into the expected lifetime of the components. Two of the test converter PCBs with the LM25141 controller were configured to output 3.3 V, and a current was selected on the electronic load. The test converter PCB was allowed to reach a steady state temperature in a controlled lab environment, at which point the peak temperature was measured with a FLIR thermal camera.

Analysis of Figure 5.5 shows the EVG100E15 test converter performed slightly better than the EPC2014c. This is likely the result of the larger PCB required to accommodate the TDG100E15Bs ceramic package, which provides a larger area of copper to dissipate the heat more efficiently. Additionally, the larger ceramic package is likely better able to dissipate the heat. The FLIR thermal images show that the GaN HEMTs are dissipating minimal heat in comparison to the LM25141 controller and the inductor. However, both converters are more than capable of operating within the recommended manufacturer temperature ratings even with load currents approaching 2 A.

## 5.2 Direct FPGA Voltage Generation

This section provides an overview of the bus voltage converters simulation, hardware, and thermal measurements performed on various GaN based, rad-hard, and COTS converters.

### 5.2.1 Simulation Results

All converters were simulated using LTSpice and OrCAD prior to manufacturing. The SPICE models for the ISL70001ASEH converter were encrypted and therefore its simulations for output voltage ripple, and simulated efficiency were unable to be obtained so datasheet values were substituted. The SPICE model for the TPS50601A-SP converter had difficulty with output current values less than 100mA leading to an inaccurate efficiency plot as seen in Figure 5.8. For output current greater than 100mA the efficiencies were as expected. A simulated load step from 0 to 6A with a  $1\mu\text{s}$  rise and fall time was used. A selection of simulated waveforms is shown in Figure 5.6 with many of the waveforms being very similar across all converters under test.

### 5.2.2 Hardware Results

Table 5.1 is a comparison summary of all the converters output voltage ripples, voltage output transient responses to load stepping, and output voltage turn-on transients from both

the simulated and measured converters. Output voltage ripple for both no-load and full load of all converters was higher than simulated which can be attributed to parasitic inductance and capacitance interaction with the switching waveforms. A selection of measured waveforms is shown in Figure 5.7. The simulated and measured efficiency plots for all converters at their respective output voltages of 1V, 1.8V, and 3.3V is shown in Figure 5.8. Efficiency measurements for all converters were below the simulation models due to parasitic losses in the PCB and components such as the inductor and capacitor equivalent series resistance.

The GaN converters efficiency for 1.0V output was much lower than expected at the 6A output however, peak efficiencies above 80% were still seen for lower current values. This is attributed to switching loss at the GaN HEMTs and AC loss in the inductor. Improvements to efficiency can be made by reducing the parasitic inductance in the switch node and gate drive, thus reducing switching losses significantly. Overall output voltage ripple was at or below 2.5mV at full load which is well below the target of 20mV, as seen in Figure 5.7c. Generally, GaN converter turn ON and load change transients performed near or better than simulated with one significant outlier on the 1.8V GaN Systems based converter producing a turn-on voltage transient peak of 18.93mV. This transient was corrected by adjusting a resistor and capacitor in the compensation network.

The LTC7151S converter had consistently high efficiencies around 90%. LTC7151S measured output ripple was higher at both no load and full load conditions than the GaN and rad-hard converters at an average of 3.5mV. Startup transients were slightly higher than simulated by an average of 12mV with a max seen of 36.141mV for the 3.3V output which is above the desired 30mV transient specification. Load change transients were lower by an average of 20mV, all of which were at or under the 30mV transient specification.

The TPS50601A-SP efficiency had a peak above 90% for outputs of 3.3V and 1.8V and a peak of 80% for a 1.0V output. Output voltage ripple at full load was 3.369mV and 1.557mV at no load, well below the desired 20mV. Turn on voltage overshoot was 0V for all output voltages which was better than simulated. Output voltage transients during load change of the TPS50601A-SP were similar to the simulation for 1.0V and 3.3V outputs at 80mV, while the 1.8V output was much lower at 47mV. These values were above the desired 30mV transient specification.

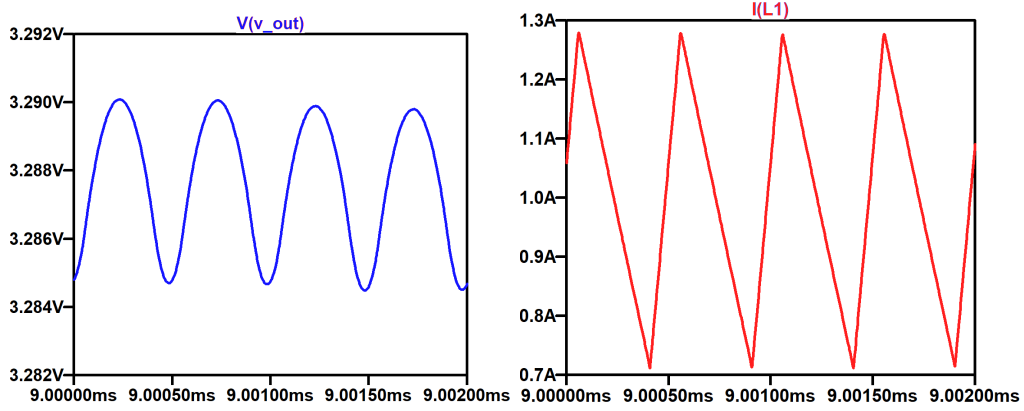
The ISL70001ASEH had efficiencies all above 75% and results were similar to those listed in the datasheet since simulated values could not be generated. The startup transient response of the ISL70001ASEH had 0V overshoot exactly as simulated. During load change transient overshoot was seen to at or better than simulated by an average of 30mV for both 1.8V and 3.3V outputs, but still above the 30mV transient specification.

The FPGA GaN converters had a better output voltage response than simulated with less output voltage ripple and less overshoot than simulated. During load transients, the voltage dip and overshoot was less than simulated and indicates a high potential for usage in load-sensitive applications where very clean voltages are required. From testing, input and output capacitance can be reduced with minimal impact on performance, further saving space. The rad-hard converters performed similarly well, with very close output voltage characteristics, load change responses, and steady-state temperatures at a fixed output current. The advantage of the TPS50601A-SP is its reduced size and ability to sync with an additional TPS501A-SP to output up to 12A. The LTC7151S had consistent transient responses for all output voltages and low output voltage ripple. The converter was very efficient over the full load range for all output voltages and was a power-dense solution. Overall, the GaN converters performed well when compared to the rad-hard and COTS equivalent converters.

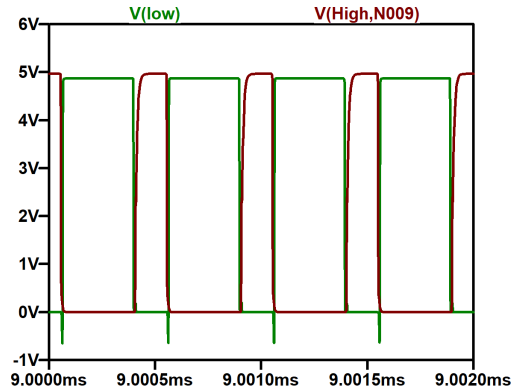
### 5.2.3 Thermal Results

The thermal performance of the converters showed that the GaN converters had most of their power loss and heat generation concentrated at the GaN HEMTs, which can be seen in the efficiency curves and attributed to switching loss. The thermal measurement results should prove for good reliability of the switching controller and the importance of a high thermal conductivity path for the GaN HEMTs when operating at high frequency. The switching losses led to the GaN converters being approximately 6°C hotter than the rad-hard converters and 2°C hotter than the COTs converter as shown in Figure 5.9. The GaN converters averaged 50°C at full load, which is well below operating maximums of 105°C. For the COTS and rad-hard converters, the heat is primarily generated at the converter, due to the nature of integrated MOSFETs. The vacuum of space this requires a more robust

method of heat conduction on the board because convection cooling is not available in order to take heat away from the converter and improve its reliability. The packaging of the rad-hard converters has a high thermal conductivity and significantly attributed to keeping both devices to approximately 44°C at full load. Both rad-hard converters operated well below their rated maximums of 125°C and the LTC7151S operated at 49°C, below its maximum of 125°C.

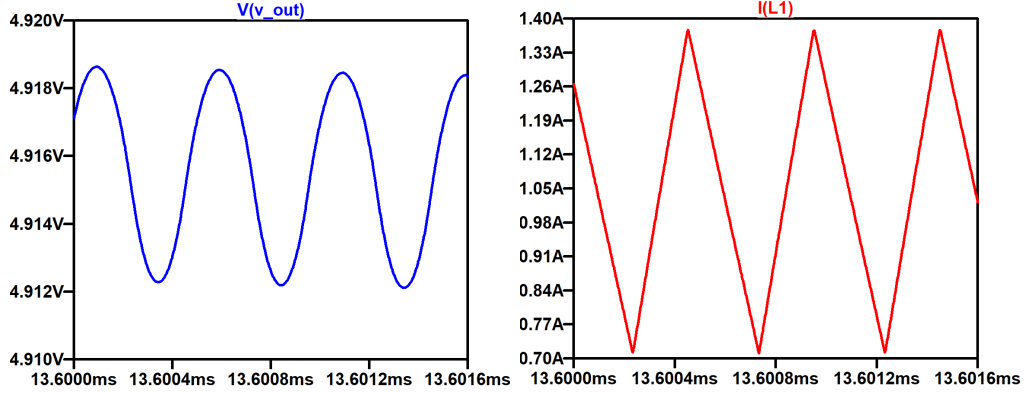


(a) Output voltage ripple of LTC3833 with EPC2014c configured to regulate 12V to 3.3V (b) Inductor current ripple of LTC3833 with EPC2014c configured to regulate 12V to 3.3V

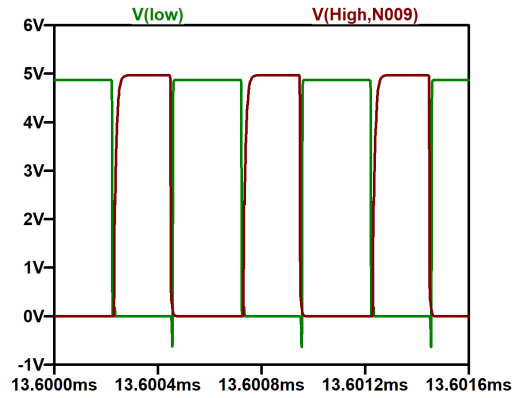


(c) Top gate (red) and bottom gate (green) drive voltage of LTC3833 with EPC2014c configured to regulate 12V to 3.3V

Figure 5.1: Simulated Waveforms of 3.3V Bus Voltage Converters

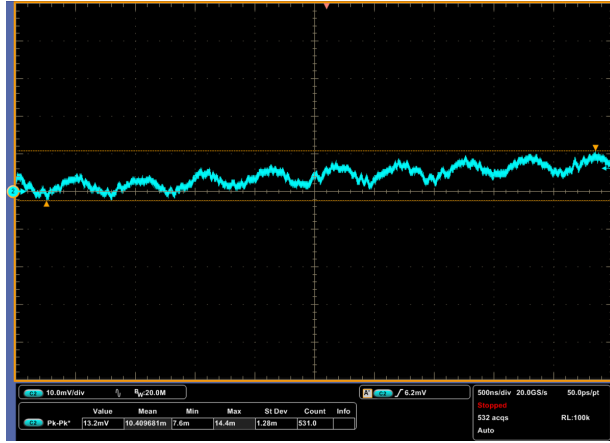


(a) Output voltage ripple of LTC3833 with EPC2014c configured to regulate 12V to 5V (b) Inductor current ripple of LTC3833 with EPC2014c configured to regulate 12V to 5V

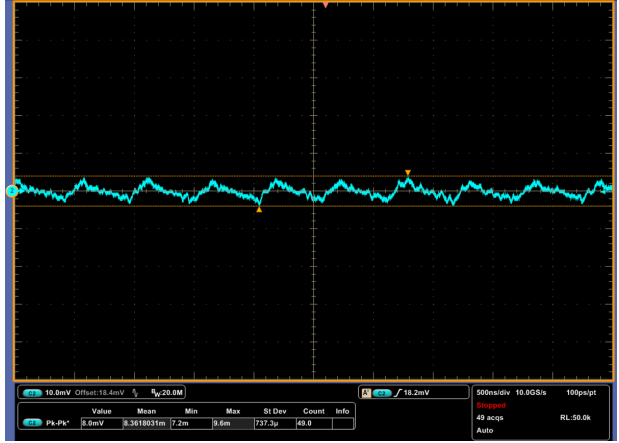


(c) Top gate (red) and bottom gate (green) waveforms of LTC3833 with EPC2014c configured to regulate 12V to 5V

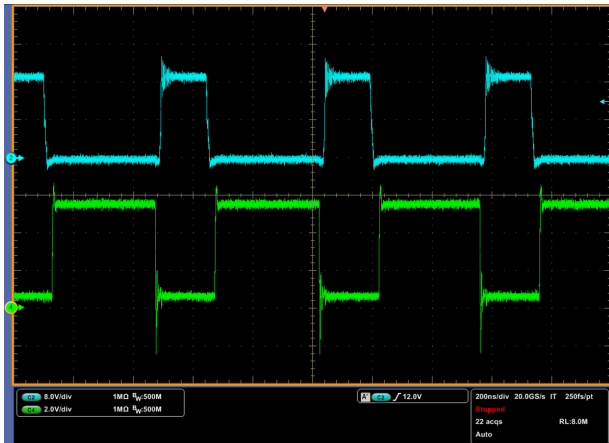
Figure 5.2: Simulated Waveforms of 5V Bus Voltage Converters



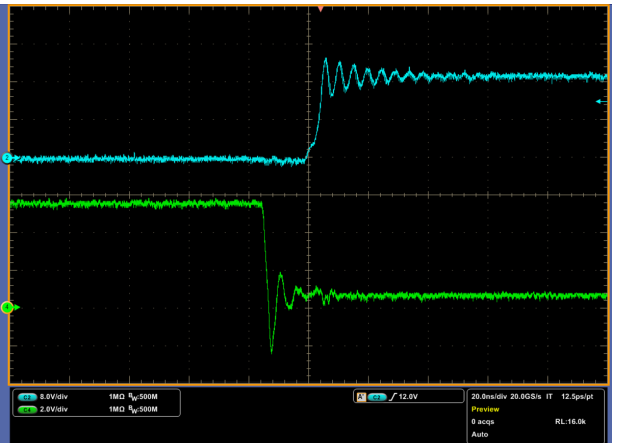
(a) Output voltage oscilloscope waveforms for the LTC3833 with the EPC2014c converter



(b) Inductor current oscilloscope waveforms for the LTC3833 with the EPC2014c converter

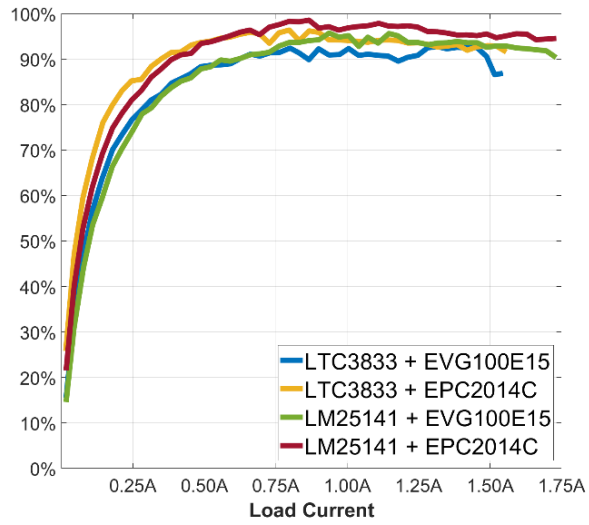


(c) Gate drive oscilloscope waveforms for the LTC3833 with the EPC2014c converter

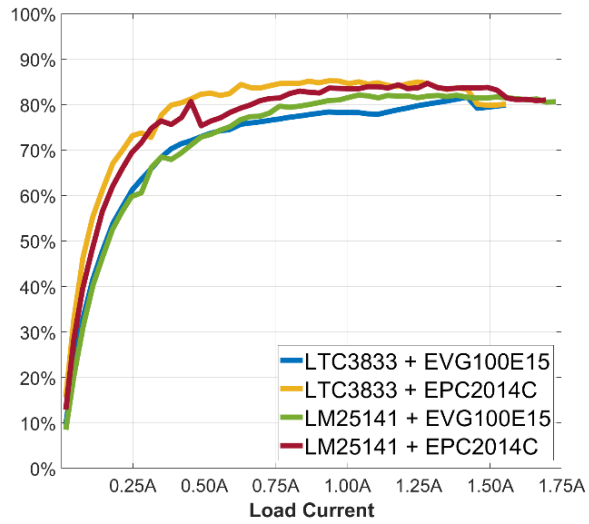


(d) Gate drive oscilloscope waveforms for the LTC3833 with the EPC2014c converter

Figure 5.3: Measured Waveforms of Bus Voltage Converters



(a) 5V Output Bus Voltage Converter Efficiency



(b) 3.3V Output Bus Voltage Converter Efficiency

Figure 5.4: Measured Efficiency of Bus Voltage Converters

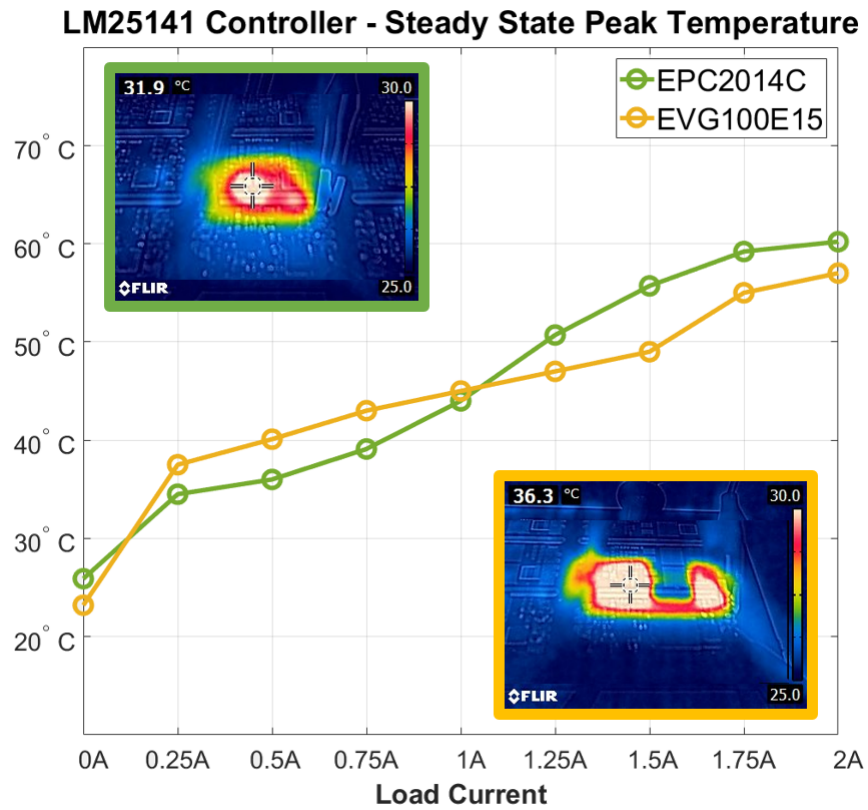
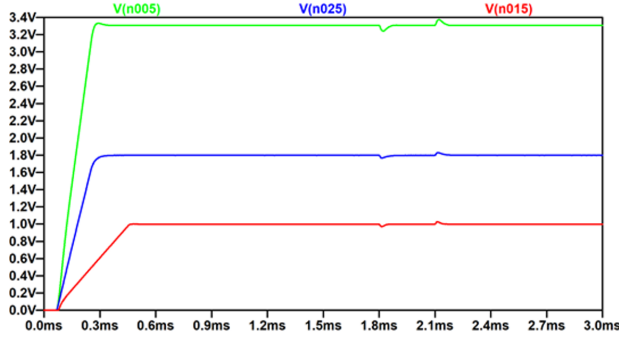
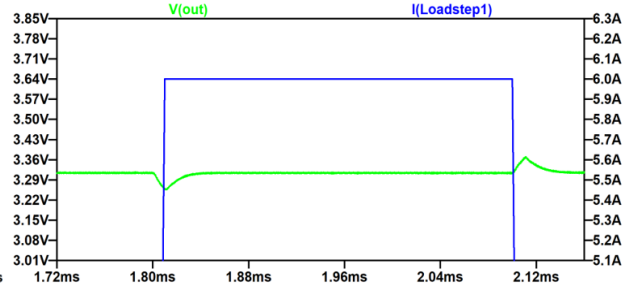


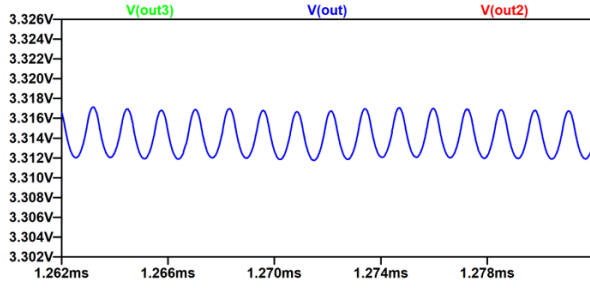
Figure 5.5: Peak Temperature at Steady State for Texas Instruments LM25141 Converter



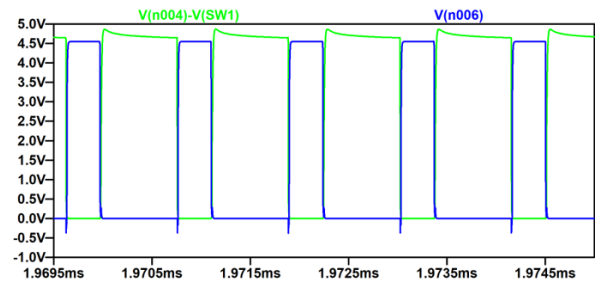
(a) LT LTC7151S Load Step and Turn ON Out-put Voltage



(b) LTC3833 EPC2014c Load Step Transient



(c) LTC3833 GaN Systems GS61004B Voltage Ripple

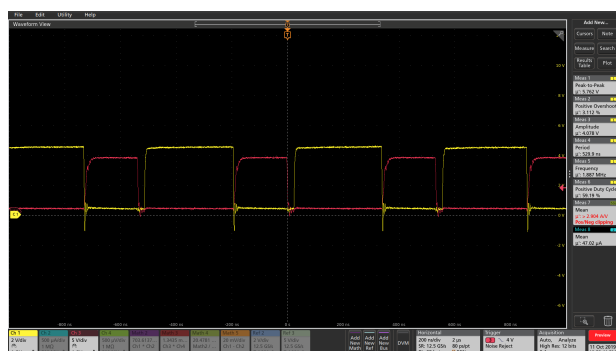


(d) LTC3833 EPC2014C Gate Drive Signals

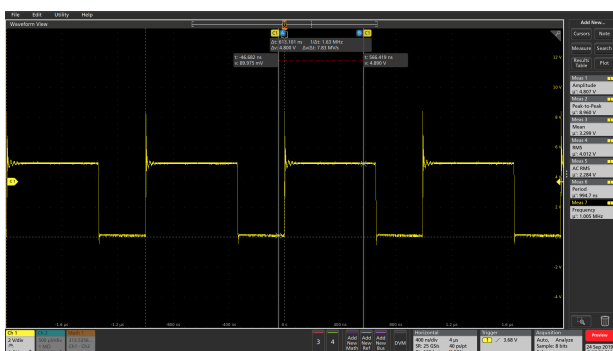
Figure 5.6: Simulated Waveforms of FPGA Voltage Converters

Table 5.1: FPGA Voltage Generation PoL Converter Output Characteristic Values

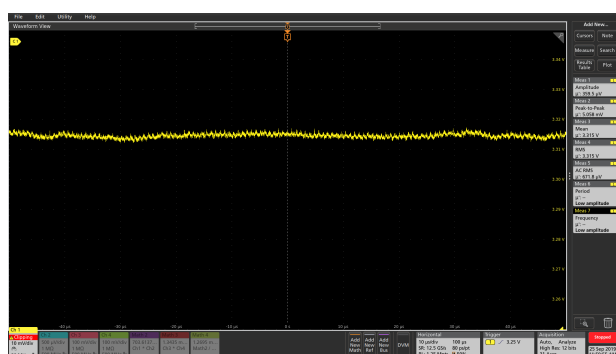
Parameters	Converters												
		TI TPS50601A-SP		Renesas ISL70001ASEH		LT LTC7151S		LT LTC3833 with GaN Systems GS61004B HEMT		LT LTC3833 with EPC 2014c HEMT		LT LTC3833 with EPC 2015c HEMT	
		<i>Simulated</i>	<i>Measured</i>	<i>Simulated</i>	<i>Measured</i>	<i>Simulated</i>	<i>Measured</i>	<i>Simulated</i>	<i>Measured</i>	<i>Simulated</i>	<i>Measured</i>	<i>Simulated</i>	<i>Measured</i>
Output Voltage Ripple	<i>No Load</i>	0.4mV	1.557mV	N/A	1.748mV	0.2mV	3.156mV	1.51mV	1.055mV	0.4mV	1.332mV	0.4mV	1.610mV
	<i>Full Load</i>	0.3mV	3.369mV	N/A	2.068mV	0.2mV	3.742mV	0.9mV	2.516mV	0.2mV	1.482mV	0.2mV	1.557mV
Startup Transient	<i>1V</i>	10.21mV	0V	0V	0V	0.1mV	1.284mV	9.1mV	4.561mV	8.1mV	7.633mV	8.2mV	8.635mV
	<i>1.8V</i>	32.2mV	0V	0V	0V	0mV	4.947mV	6.5mV	3.028mV	5.2mV	18.934mV	5.1mV	3.454mV
	<i>3.3V</i>	80.3mV	0V	0V	0V	22mV	36.141mV	8.1mV	11.386mV	10.3mV	5.253mV	10.4mV	9.339mV
Load Change Transient	<i>1V</i>	83.6mV	79.104mV	70mV	66.567mV	30mV	20.149mV	37.6mV	18.550mV	36.9mV	18.017mV	35.8mV	17.484mV
	<i>1.8V</i>	90.7mV	47.335mV	70mV	33.475mV	32mV	22.281mV	54.3mV	28.145mV	53.8mV	29.744mV	53.3mV	27.079mV
	<i>3.3V</i>	131.7mV	84.686mV	68mV	37.207mV	66mV	30.810mV	170.5mV	43.070mV	58.2mV	44.883mV	57.4mV	36.674mV



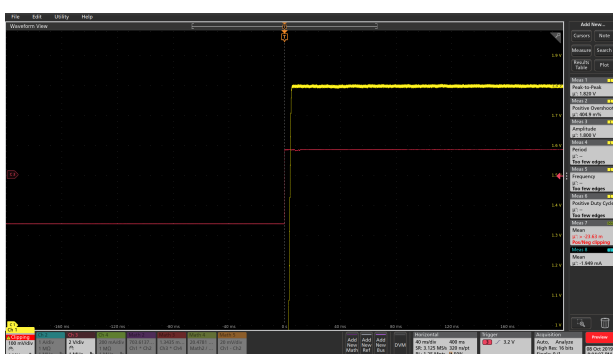
(a) Gate Drive Waveforms LTC3833 EPC2014c



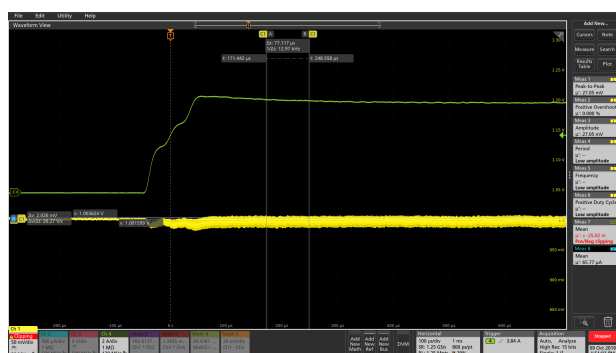
(b) LTC3833 EPC2015C Switch Node Voltage



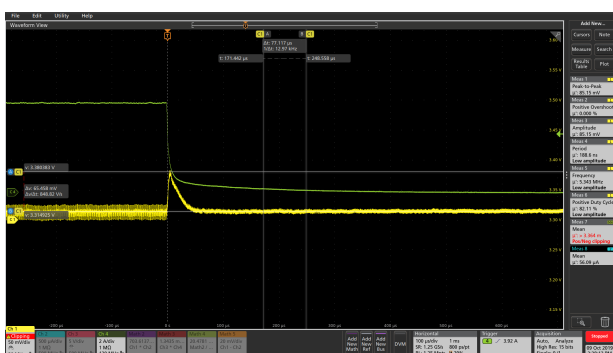
(c) LTC3833 GaN Systems GS61004B Output Voltage Ripple



(d) TPS50601A-SP Turn-On Transient



(e) LTC3833 EPC2015c Load Turn ON Transient



(f) LTC3833 EPC2015c Load Turn OFF Transient

Figure 5.7: Measured Waveforms of FPGA Voltage Converters

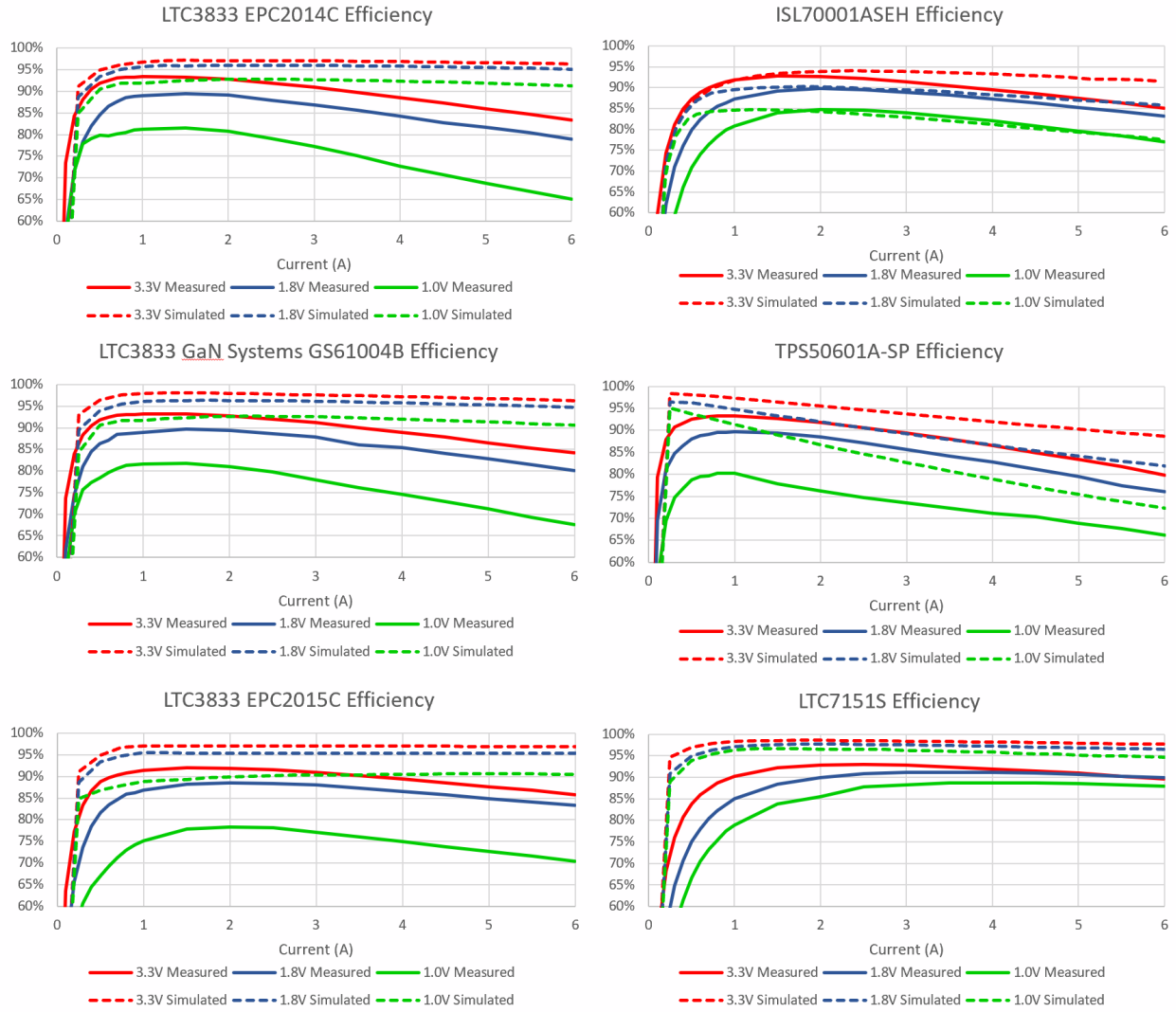


Figure 5.8: Simulated and Measured Efficiency of FPGA Converters

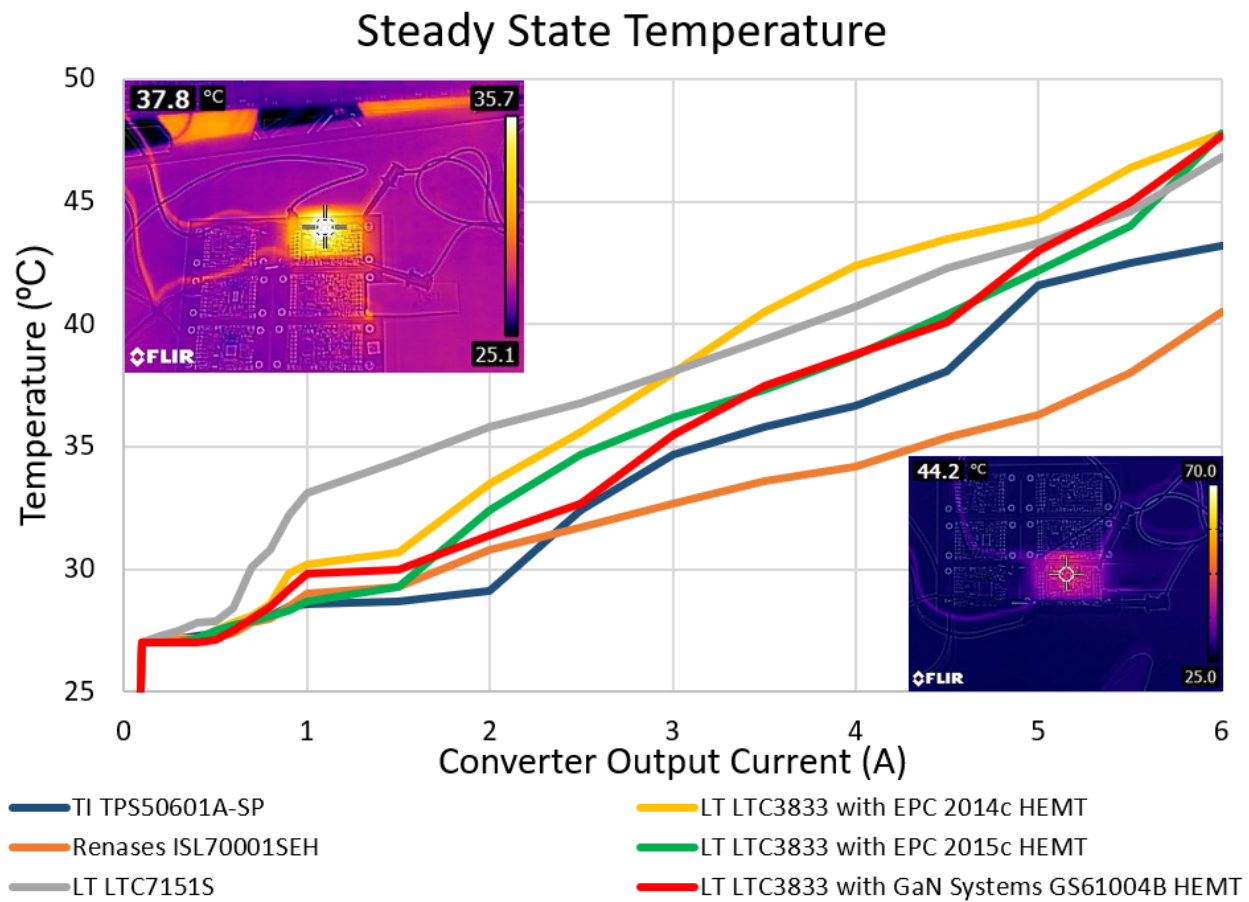


Figure 5.9: Steady-State Temperature of FPGA Converters

## 6.0 Application Areas

From testing on earth and evaluating efficiency and output data from SSIVP, the GaN HEMTs and LTC3833 driver are show great promise for use in LEO environment as both a direct computational load converter and a bus power generation unit.

### 6.1 SSIVP GaN Sub-experiment

This section provides a cursory overview of the SSIVP experiment on STP-H6 mission. Additionally, a discussion is presented of the measurement electronics, testbed, and GaN HEMT converters selected for the GaN sub-experiment on STP-H6 SSIVP.

#### 6.1.1 SSIVP Testbed

The CSP system is designed with a hybrid mix of COTS and rad-hard technology, supplemented with fault-tolerant computing [20]. With the success of the STP-H5-ISEM mission, the Technology Readiness Level (TRL) of the CSP card was increased to a flight proven technology (TRL-9) [29]. Building on the technology advancement and lessons learned during the ISEM mission, SSIVP provides a supercomputing platform for CubeSat missions and was developed by the NSF Center for Space High-performance, and Resilient Computing (SHREC) at the University of Pittsburgh, and launched to the ISS as part of STP-H6 in early 2019 [21]. Designed around the 3U CubeSat shown in Figure 6.2, the SSIVP computing system features five flight-qualified CSP compute nodes that interface with two cameras, one  $\mu$ CSP on Smart Module with the GaN converter experiment, one power card, and a backplane to distribute power and provide an interconnect topology between the computing nodes.

The power card is composed of an EMI filter and an isolated rad-hard DC/DC converter to reduce the supplied STP-H6 pallet voltage (28 V) down to the required voltages (12 V,

5 V, and 3.3 V) for the cameras and computing nodes. The reported converter efficiency is approximately 76% when operating over the proposed SSIVP power levels. Due to power and thermal limitations of SSIVP, the GaN experiment and cameras will be multiplexed with solid state relays to enable testing over the course of the multi-year mission. Data collection via the Smart Module will continue throughout the duration of the STP-H6 mission, or until the converters fail from radiation.

### 6.1.2 GAN Sub-Experiment

The Smart Modules concept is a framework for rapid development and integration of sensor experiments with networking capability in a reusable form factor. The  $\mu$ CSP is the second realization of the CSP concept designed for a System-on-Module (SoM) development platform with the commercial Microsemi SmartFusion2 hybrid SoC that includes a fixed-logic ARM Cortex-M3 microcontroller with fixed and reconfigurable logic, flash-based FPGA [30]. The  $\mu$ CSP serves as the controller for the smart module providing a data collection interface, sensor processing platform, and a networking interface that reduces experiment integration complexity, all of which is contained in a 1U form-factor. The three GaN converters and corresponding measurement circuitry were integrated onto a Smart Module with a  $\mu$ CSP as seen in Figure 6.1. The SSIVP experiment will be evaluated on the ISS with an altitude ranging from 401.1 km to 408.0 km, and inclination of 51.64 degrees. The ISS orbital path includes the South Atlantic Anomaly (SAA), which will be used to test the converters in a high upset-rate environment and provide valuable data on their reliability in LEO.

On the STP-H6-SSIVP system, three of the PoL synchronous buck converters were selected to fly on a smart module, including two Linear Technologies LTC3833 controllers and one LM25141. The Teledyne e2v TDG100E15B GaN HEMTs were selected to provide a comparison between the known flight-grade components and the ultra-small package. The synchronous buck controllers were designed to regulate 12 V down to 5 V. The flight converters were designed to drive a  $4.7\Omega$  load or 5.25 W.

The converter configurations used are the LTC3833 with EPC2014c and Teledyne TDG100E15B HEMTs and the LM25141-Q1 with EPC2014c HEMTs which are selected

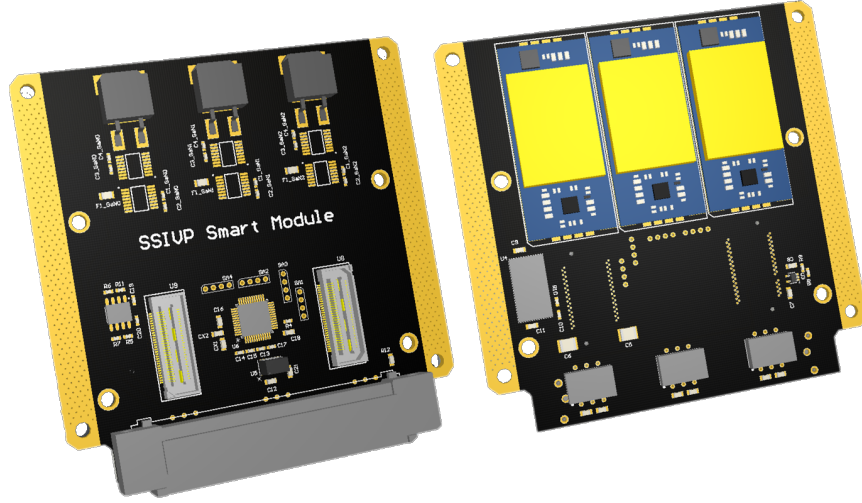


Figure 6.1: Front (left) and Back (right) of Smart Module with GaN Converters and Load Resistors

to allow for the remote deduction of component failure if it occurs throughout the course of the mission. The hermetically sealed ceramic TDG100E15B GaN HEMT has flight heritage, and extremely stable over a wide temperature range that enables controller testing. With a low probability of failure on the TDG100E15B, any in-flight converter failure on PoL-1 or PoL-2 is likely a result of the controller, and not the GaN HEMT. The primary purpose of PoL-3 is to provide flight heritage to the EPC2014c with a secondary task of testing the feasibility and survivability of the ultra-small package.

Each flight converter has isolated measurement circuitry to calculate the DC current and voltage at the input and output for in-flight calculation of efficiency. Individual converters are fused allowing the failure of any converter without impacting the success of the sub-experiment.

The FPGA GaN based converters presented use technologies and components currently in orbit on the SSIUP experiment [5]. The SSIUP GaN sub-experiment is currently collecting voltage and current data to determine if TID will cause drift in voltage regulation or efficiency capabilities or if recovery from a single event functional interrupt (SEFI) is recoverable. So far, preliminary data and initial passes through the SAA have shown no effect on voltage

regulation or efficiency as shown in Figure 6.3. Experimental data collection has been limited due to overall power limitations and priority of other additional experiments on SSIVP. Data is collected using a Texas Instruments (TI) INA260 and each converter is fused to prevent malfunctions from impacting the experiment.

## 6.2 Bus Rail Voltage Generation

The GaN PoL converters for stepping 12V down to 5V can be operated from from 0 to 2A reliably with the EPC2014C GaN HEMTs. With the GaN Systems and EPC2015C HEMTs the output current can be increased to up to 15A. With the size, weight, and power savings of these converters they make a strong replacement for current rad-hard converter usage in a LEO environment.

## 6.3 COTS Controllers with External FETs

As processing systems and FPGAs increase in power, their core voltage drops and current increases beyond what most rad-hard converters can handle. For example, the Xilinx UltraScale+ XCVU13P core voltage VCCINT supports 200A operating at 100°C for 10 years [31]. The use of a COTS controller with a high current rated external FETs adds the ability to switch much higher currents than currently available integrated FET converters while still providing a power-dense solution.

## 6.4 Switched Converters as LDO Replacement

LDOs are inefficient when operating with a large voltage drop or a large output current since they primarily dissipate power through heat due to their linear nature. This makes them primarily suited for generating reference voltages. The benefit is an extremely clean

output voltage with minimal noise and relative simplicity of integrating into a design. For MGTs, the efficiency tradeoff for clean voltage is severe, with efficiencies seen as low as 40% to 50% and high operational temperatures. The high switching frequency, fast response time, and low output voltage ripple of the GaN converters allow them to react faster to load steps, minimizing the voltage overshoot and undershoot on powering sensitive high-speed transceivers. The high switching frequencies allow them to use smaller passive components like inductors and capacitors, further increasing power density and saving board space.

## **6.5 High Switching Frequency Impact**

The higher switching frequencies capable from GaN means that the converter can respond faster to load step transients and puts less stress on the capacitors, requiring fewer of them, to maintain the same output voltage and eliminate droop. Due to fewer capacitors being required they become increasingly important to ensure that a clean voltage signal is coming through to the FPGA. Smaller value magnetics and capacitances have a greater effect on filtering the high frequencies; however, the source current draw from the PoL converter on the bus can potentially couple high-frequency noise into the ground plane causing previously unforeseen interactions with the FPGA.

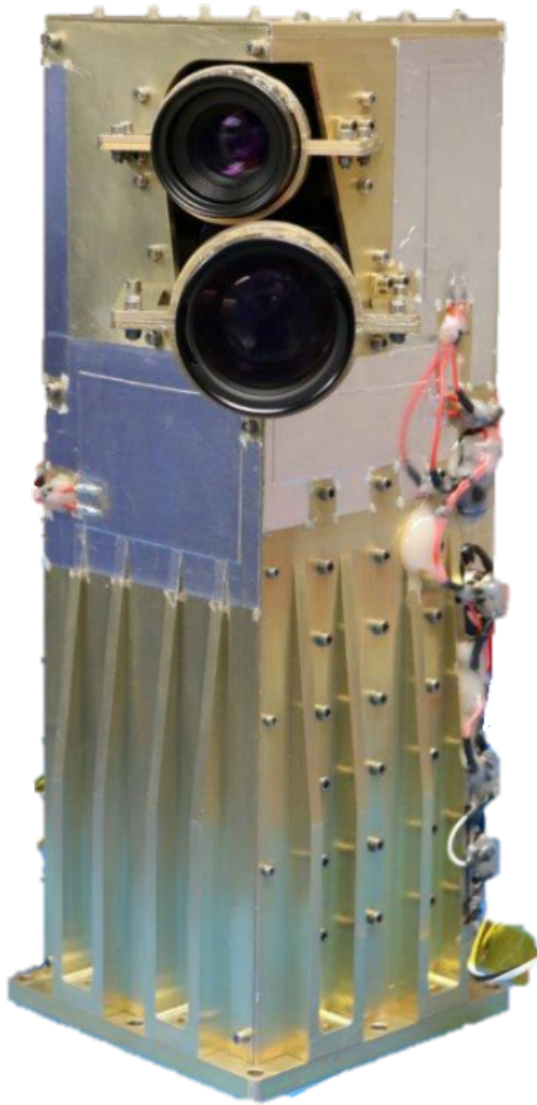


Figure 6.2: SSIVP Assembly for STP-H6

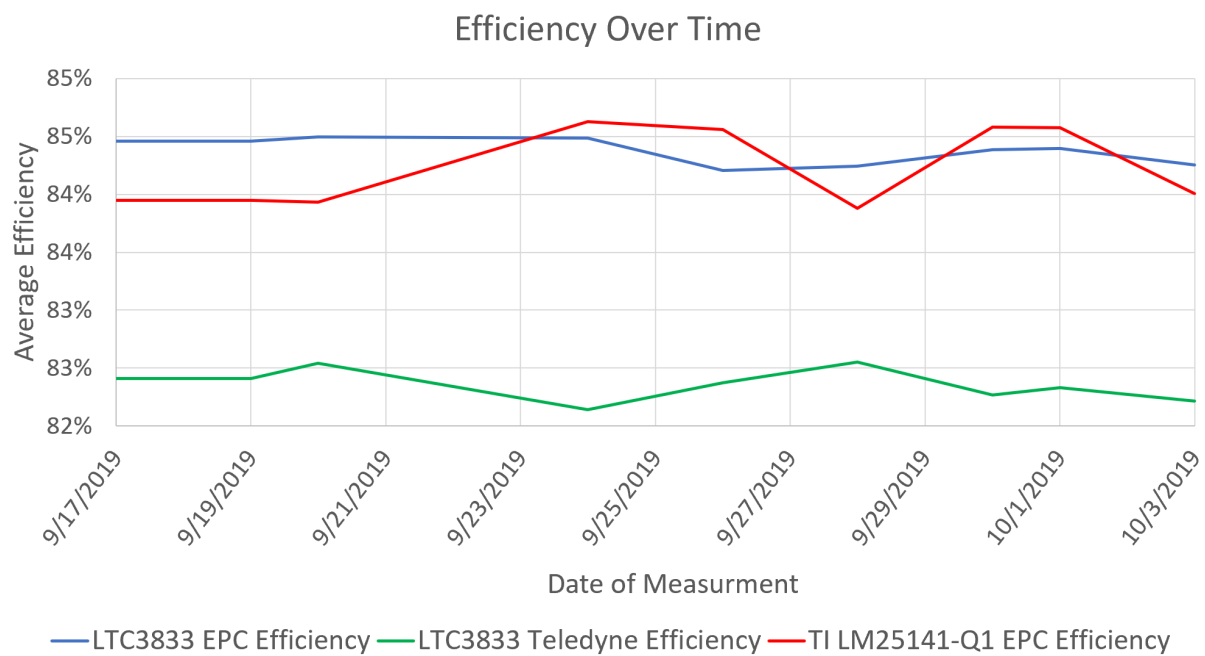


Figure 6.3: SSIVP GaN Converter Experiment Data

## 7.0 Conclusions

The proposed GaN-based converters offer several advantages for scalability and power density when used for supplying FPGA systems. They offer clean, consistent output voltages over a wide load range and quick response times to load changes. The radiation-tolerant nature of GaN, high switching frequency, and small size provides a significant cost reduction, size, and weight reduction for power systems while providing comparable efficiency to similar rad-hard components. The hybrid SSP currently utilizes the rad-hard TI TPS50601A-SP converters since they offer a power dense and efficient solution with excellent output voltage characteristics.

The benefits and advantages of the proposed controllers with GaN HEMTs are clear when compared to traditional rad-hard converters. The radiation-tolerant nature of GaN provide significant cost reduction when compared to traditional radiation-tolerant converters. High switching frequency require lower component values with smaller component packages that introduce less loss to the converter. Both combine to produce efficiencies as high as 96% with package areas as small as 0.41 in<sup>2</sup>. The in-flight success of the LTC3833 and the LM25141 controllers will provide a low-cost solution for CubeSat missions that costs orders of magnitude less than current offerings.

STP-H6 launched in May of 2019, at which point converter data collection in LEO began. Future plans for neutron-beam radiation testing at Los Alamos for the LTC3833 and LM25141 synchronous buck controllers is planned. NASA Jet Propulsion Laboratory is currently evaluating both controllers for their radiation tolerance for future small spacecraft missions.

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