Exploring Electrochemical Reactivity in Ionically-Gated Field Effect Transistors

by

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Electric double layer gated field effect transistors (EDL FETs) are devices commonly used to investigate the fundamental properties of new materials, such as two-dimensional (2D) layered materials. Despite this usefulness and further potential for integration into devices and circuits, EDL FETs have the possibility of undergoing electrochemical reactions during device operation. Most often, this electrochemistry goes unmonitored. Part of the challenge of detecting electrochemical reactivity within EDL FETs resides in a knowledge gap between the device and analytical electrochemistry communities; that is, what type of reference electrode should be used, how should one be used, and what does it mean to monitor one?

This work addresses this issue by introducing a silver metal quasi-reference electrode in a graphene EDL FET with a solid polymer electrolyte— polyethylene oxide lithium perchlorate (PEO:$LiClO_4$)— serving as the ion-conducting dielectric. The hypothesis was that Li^+ ion intercalation in graphene would drive irreversible changes to device transfer characteristics and be detectable by reference electrode monitoring. The reference electrode was used in two experiments in which the gate window of an EDL FET device was either increased with each measurement (starting from -2.5 V $\leq V_{SG} \leq$ 2.5 V and expanding to -2.5 V $\leq V_{SG} \leq$ 10 V) or fixed (-2.5 V $\leq V_{SG} \leq$ 7 V). Changes to the transfer characteristics of the devices after each experiment—an increase in average drain current, Dirac points shifted negative vs. V_{SG} in both forward and reverse transfer sweeps, an increased ON/OFF ratio, and higher-sloped side-gate current shifted negative vs. V_{SG}–were noted as possible evidence of electrochemical reactivity within the graphene channels. However, thanks to the Ag/Ag^+ reference electrode, the data from these experiments provide evidence that intercalation of Li^+ in graphene was highly unlikely. Possible alternative explanations will be discussed, including reduction of water, PMMA, and graphene oxide defects.

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Preface

From the journey that quite nearly rendered me hollow, I suddenly find myself poised for the next; by the grace of God, I have made it.

To Dr. Susan Fullerton, thank you for teaching me how to tread the graduate student's path and for instructing me that feeling out of place is different from being out of purpose.

To Dr. James McKone, thank you for preparing my chemist's lenses for a chemical engineer's plans and for redirecting my attention when my thoughts grew errant.

To Dr. Ke Xu, Jierui Liang, and Zhongmou Chao, thank you for your guidance through the arcane arts of 2D crystal exfoliation and nanofabrication and for your instruction on the supple science of device measurement.

To the rest of my labmates, thank you for your support, guidance, and tutelage, without which I should surely have perished.

I would also like to thank my friends here at the university for the opportunity to become adept in foosball (perhaps my only honed athletic skill), for reminding me of the solidarity of the well-trodden trail, and for keeping the stories going after months of papers and conferences.

Finally, I would like to thank my parents for their unending support, Sarah for her patience and understanding, and my grandparents for their ready encouragement.

— Eli Bostian

"Please, we're all friends here. Feel free to call me by my first name: Master."

— Master Elodin, *The Name of the Wind* by Patrick Rothfuss

1.0 Introduction

1.1 Field Effect Transistors: Ubiquitous and Evolving

The fundamental building blocks of computation are changing. New challenges in data processing and analysis have transformed niche fields of research like spintronics[1, 2, 3], photonics[4, 5, 6], and neuromorphic computing[7, 8, 9]. As a part of this wave of new paradigms and technologies in computing, the classical field effect transistor (FET), the class of device on which all modern binary computation depends, has seen a conceptual evolution as well.

A standard example of a FET— one that is used in modern, commercial computing— is the metal-oxide-semiconductor FET, or MOSFET. Depicted in Figure 1.1 (a), the MOSFET is predictably constructed from three components: metal, serving as the electric field-inducing electrode, an oxide, serving as a dielectric to pass the electric field while preventing electrical current, and a semiconductor, serving as a channel with variable resistance that can be adjusted by the field. When a strong enough electric field is passed to the semiconductor— the required electric field strength varies according to the semiconductor material— the semiconductor transitions from a state of low conductivity ("OFF state") to a state of high conductivity ("ON state") or vice versa. Throughout the computer revolution, this technology has predominately used silicon as the semiconductor in MOSFETs, but researchers have recently been exploring two-dimensional (2D) semiconductors in the hopes of developing devices that use less power, are ultra thin, have sharp band edges, and effectively function more efficiently in specialized (or even generalized) applications.[10]

Among this surge of investigations, electric double layer (EDL) gating has developed as a particularly effective method of gating 2D FETs.[11] As depicted in Figure 1.1 (b), EDL FETs are constructed differently from a traditional MOSFET. Instead of gating through a solid oxide dielectric, EDL FETs use electric fields to direct ions through an ionically-conductive dielectric to the semiconductor of the FET (the "channel"). By pushing charges to within a nanometer of the channel of the device, a capacitor forms at the channel-electrolyte

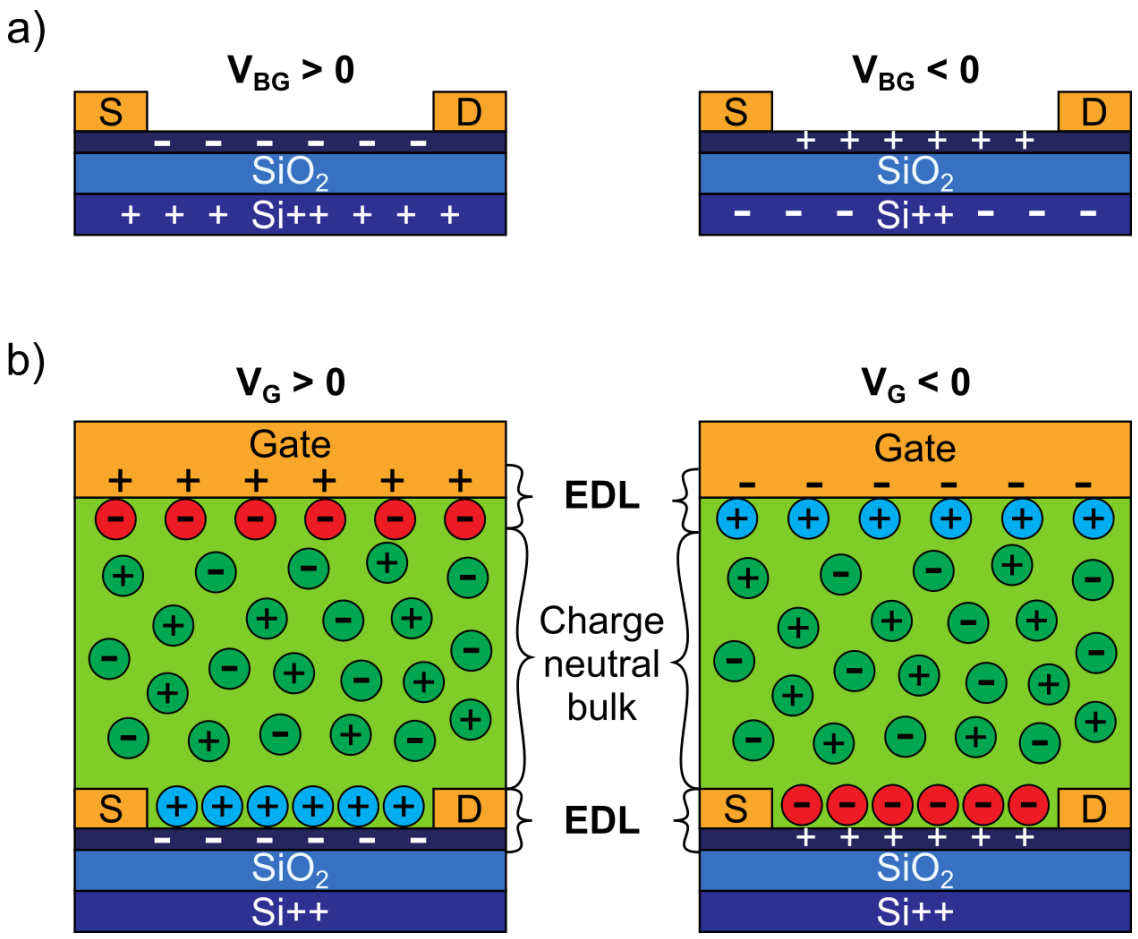


Figure 1.1: Schematic of a Back-gated FET vs. an EDL FET. (a) Back-gated FETs are fabricated atop a multilayer subtrate that functions as both the gate (bottom layer) and the dielectric (top layer) of the device. Biasing the gate positively vs. source (left) induces negative charges in the channel, while biasing the gate negatively vs. source (right) induces positive charges in the channel. (b) EDL FETs require an electrolyte to be deposited between the gate (which can be fabricated either above (top gate) or to the side (side gate) and the channel. Biasing the gate forces ions of the same charge polarity along the surface of the channel, inducing negative charges in the channel with a positive gate bias (left) and positive charges in the channel with a negative gate bias (right). The ions and their induced charges form an EDL along the channel surface. A similar EDL is formed along the surface of the gate as ions with charges opposing the gate are pulled to its surface.

interface and creates sheet carrier densities of $4 \times 10^{14}\,\mathrm{cm}^{-2}$, exceeding that of a conventional MOSFET by one to two orders of magnitude.[12] However, EDL FETs pose new challenges that are not frequently encountered in other device research, and have predominately been only indirectly addressed until now.[13, 14] Specifically, there is a frequently a standing uncertainty as to the types of electrochemical reactions that may be occurring as an EDL FET operates.

1.2 Exploring Electrochemistry in FETs as Nonaqueous Electrochemical Systems

EDL FETs, despite the presence of compounds and voltage biases that can certainly drive electrochemical reactions, are not typically designed to measure for and identify any reactions. In some cases, new or altered material characteristics such as heightened conductivity or even superconductivity have been dissociated from or attributed to hypothetical electrochemical reactions, but have not been confirmed by analytical techniques.[13, 14] This is not to say that electrochemical reactions occurring in EDL FETs are a complete unknown; there have been efforts to measure electrochemical potentials within EDL FETs or similar devices in previous research.[15] Some researchers have incorporated a reference electrode into the gate electrode of the devices to monitor electrochemical potential, although these devices are unable to simultaneously gate and read potential, requiring independent reading and programming sequences.[16, 17, 18] Others have even developed devices containing components similar to a 3-electrode electrochemical cell, allowing simultaneous monitoring of reference potential and gating.[19, 20, 21] The majority of these 3-electrode cell measurements have been conducted with organic thin-film EDL FETs and not with devices incorporating 2D crystal channels. However, it is the 2D crystal channeled devices we desire to investigate in this work. In order to learn from these efforts from others, we must first understand the 3-electrode cell and how it relates to EDL FETs.

The 3-electrode cell (as depicted in Figure 1.2 (a)) is a very common design for experimental setup in classical electrochemistry. A 3-electrode cell is comprised of three electrodes—

the working, counter, and reference electrodes— immersed in an electrolyte solution.[22] The working electrode is usually the site of the electrochemical reaction of interest, its potential monitored for reaction identification. The counter electrode completes the electrochemical circuit as the host of a complementary reaction, and its current is usually monitored for reaction onset. The reference electrode is the component of this setup that allows measurements in one experiment to be compared to another; a reference electrode with a stable potential can be mapped against electrochemical reactions from multiple experiments, allowing for a sense of continuity when the measurements are compared.

Although not directly analogous, the design of an EDL FET is similar to that of a 3-electrode cell. The two are compared side-by-side in Figure 1.2. Similar to a 3-electrode cell, an EDL FET device is immersed (or, more specifically, coated) in an electrolyte. The source electrode is held at 0 V, the drain electrode is held at a small bias versus the source (0.1 V, in the case of this work), and the channel forges an electrical connection between the two (depending on the potential held at the gate electrode). In this way, the channel, drain electrode, and source electrode can be comparable to a working electrode, as both are sites of electrochemical reactions of interest. On the other hand, the gate electrode can complete the electrochemical circuit and bias against the channel, much in the manner that a counter electrode would function. This leaves the standard EDL FET geometry only missing a reference electrode, the addition of which (as seen in Figure 1.2 (b)) is a driving motivation for this research.

By incorporating a device feature that will work effectively as a reference electrode, we stand to learn much about the chemistry of EDL FETs. The focus of our research here is to explore a method of applying a reference electrode (a silver quasi-reference electrode) to an EDL FET, to investigate gate potential ranges resulting in phenomenological changes in the devices, and to identify a collection of possible chemical reactions resulting from the voltages reached in the devices.

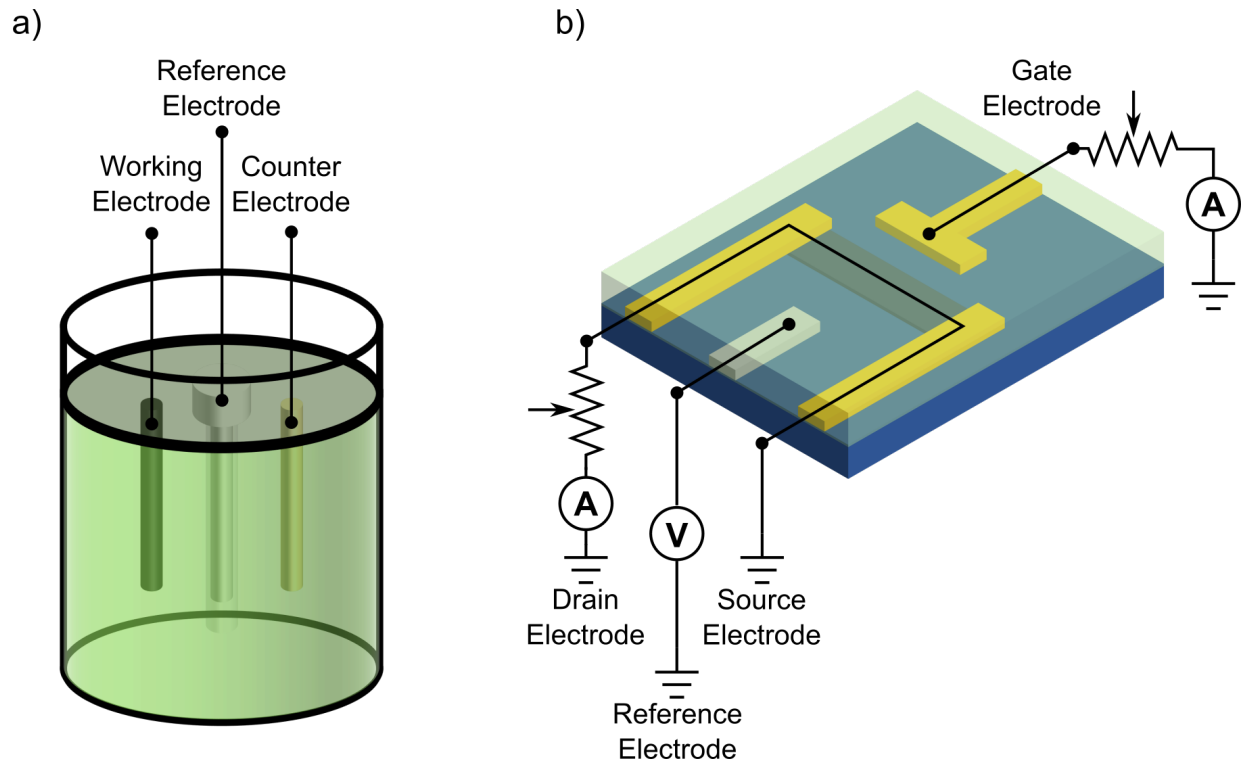


Figure 1.2: Diagram of a 3-Electrode Cell vs. an EDL FET with Reference Electrode. (a) A classical 3-electrode cell comprised of three electrodes— the working, counter, and reference electrodes— immersed in an electrolyte solution. (b) The components of an EDL FET as compared to those of a 3-electrode cell, consisting of four electrodes— the source, drain, gate, and reference electrodes. The source and drain are connected through a channel and may be compared to a working electrode. The gate electrode may be compared to a counter electrode. The reference electrode is directly analogous.

1.3 Purpose and Scope of the Content Herein

This thesis is divided into six chapters and two appendices. You are finishing the Chapter 1 now, which serves as an introduction to the content of the work presented here and its various motivations. Chapter 2 delivers a brief summary of research I have contributed to prior to the work that is closely documented here; my previous efforts do not directly relate to measuring and interpreting electrochemical reactions in EDL FETs, and so have been isolated to this separate chapter. Appendix B contains a copy of this paper resulting from the prior work, "Electric Double-Layer Gating of Two-Dimensional Field-Effect Transistors Using a Single-Ion Conductor." Chapter 3 describes the design methodology behind the FETs fabricated for this research, presents data representative of a bare graphene FET, and serves as an introduction to the interpretation of FET transfer characteristic measurements, the primary method of analysis in this work. Similarly, Chapter 4 outlines the design principles behind the reference electrode developed for this work, presents data collected to analyze the behavior of the reference electrodes with our solid polymer electrolyte, and identifies protocol used to condition the reference electrodes in all experiments with EDL FETs shown here. Chapter 5, easily the largest, outlines the experimental methods and measurements captured to explore electrochemical activity in EDL FETs. EDL FET transfer characteristics data are analyzed here. Chapter 6 brings the thesis to a conclusion, with a brief review of observations made and a restatement of work that will push the goals of this research forward in the future. Experimental details and representative experimental protocol are reserved for Appendix A.

2.0 EDL Gating of Two-Dimensional FETs Using a Single-Ion Conductor

During my first year as a graduate student researcher, I worked on a project focused on single-ion conductors (i.e., an electrolyte where one type of ion is mobile and one is immobile) for EDL gating of 2D FETs. Using a single-ion (instead of dual-ion) conductor is a new area of investigation for 2D FETs. By working on this project, I learned technical skills for 2D crystal exfoliation, nanofabrication (e-beam metal evaporation and deposition, optical and e-beam lithography, etc.), and FET electrical characterization, and the work resulted in the paper "EDL Gating of Two-Dimensional FETs Using a Single-Ion Conductor[23]." My contributions to this paper were 2D crystal exfoliation, device fabrication, ionomer solution preparation and deposition, and device transfer measurement.

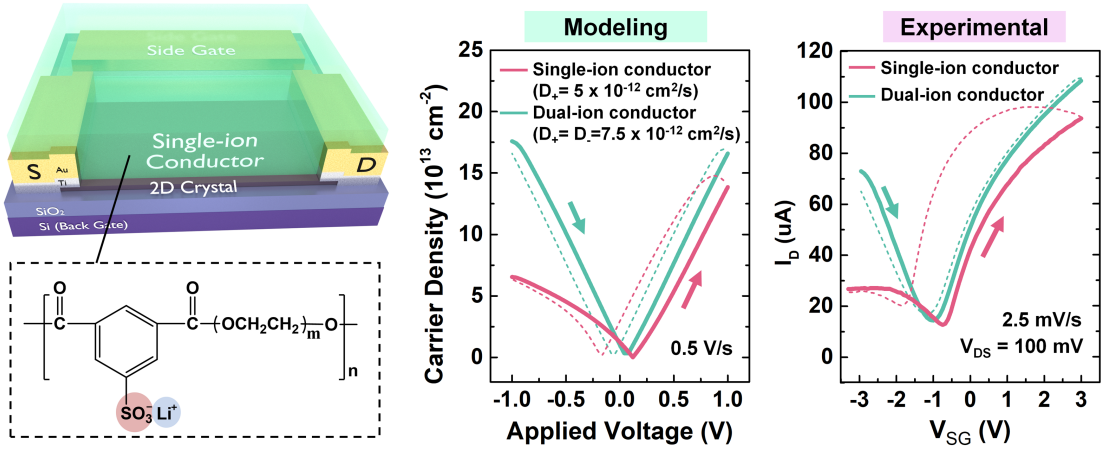


Figure 2.1: Table of Contents Graphic from "EDL Gating of Two-Dimensional FETs Using a Single-Ion Conductor[23]."

3.0 Designing Graphene FETs for Electrochemical Investigations

The FETs fabricated for this work were designed with several principles in mind, but chief among them was the intention of seeking and identifying electrochemical reactions contributing to changes in FET transfer characteristics as a result of increasing gate potential to sufficiently high biases. This chapter lays out the merits of graphene to test this hypothesis while also presenting some of the properties of the bare graphene FETs. These preliminary back-gated results were collected to establish a history of device performance from before electrolyte deposition but also provide an opportunity here to discuss the properties of a graphene FET relevant to the rest of this work.

3.1 A Case for Graphene Channels

At the start of this research, we knew from past experiences (personal and anecdotal) that EDL FETs can show unusual characteristics at gate potentials far beyond bounds typically present in FET research. Defining these bounds is difficult, largely due to the difference in field effect impact through different dielectric materials and lengths, but the typical range of top- and side-gated EDL FETs of -3 V $\leq V_{SG} \leq$ 3 V provide a sense of the gate potential region typically regarded as "safe."[24, 25, 26] Citing such unusual characteristic features is difficult as well, as device researchers frequently interpret the gate biases inducing these changes as "too high" and simply retreat from measuring at such bounds. As mentioned in Section 1.2, these unusual characteristics have manifested in the form of sharply increasing drain current, but other observations have likely existed but remain unreported. The assumption that electrochemical reactions are the root cause of these characteristic changes is surely reasonable, yet is also surprisingly under-investigated. As a result, when considering channel materials for this work, we sought materials that were well-established in the device research community, possessed material features relevant to our purposes, and that belonged in a wealth of already studied material relevant to these phenomena.

As an early approach to understanding electrochemistry in 2D EDL FETs, device material selection required careful consideration with the goal of choosing materials with as well-understood electrochemical activity (even outside of the FET community) as possible; it was this consideration that ultimately pointed us in the direction of graphene. 2D semiconductor crystals (such as the wide selection available from the family of materials known as transition metal dichalcogenides) are capable of displaying a plethora of beneficial properties for exploring electrical characteristics such as high ON/OFF ratio (over 4-7 orders of magnitude) and varying states of doping (n-type, p-type, or ambipolar).[27] By comparison, a semimetal like graphene typically finds less hold as a channel material in similar applications because its lack of a bandgap results in device ON/OFF ratios peaking at approximately 1-2 orders of magnitude across a typical EDL FET operational gate voltage, whether back, top, or side gated.[28] Graphene does, however, benefit from other qualities— high carrier

mobility (as high as $15\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ on room temperature SiO_2[29]) and a single-atom thickness to protect against short-channel effects, particularly[28]— leading to its implementation in a host of sensor and radio frequency applications. All of these features have the opportunity to result in interesting devices, but they do not fully address our goals of identifying electrochemical reactions in EDL FETs. More relevant to this research, graphene is ambipolar (allowing us the opportunity to determine which type of charge carrier is more or less impacted by electrical stress via high gate potential) and particularly sensitive to doping (as evident from its widespread adaptation in the sensor community).[30, 31, 32]

Graphene also boasts a wealth of existing literature regarding lithium intercalation from the battery community[33, 34, 35, 36, 37, 38, 39, 40, 41], providing us with a well-documented electrochemical reaction to investigate, this time in EDL FETs. By gating graphene FETs using a PEO:$LiClO_4$ solid polymer electrolyte, we produce a device environment that also puts three suspect reactants— graphene, lithium ions, and perchlorate ions— in close proximity. This creates the opportunity to evaluate if any unusual FET characteristics are caused by lithium intercalation in graphene, or if the changes occur as a result of some other factor. Thus our hypothesis is outlined: Lithium intercalation in graphene leads to the first notable occurrence of unusual FET electrical characteristics.

The types of graphene flakes produced for FETs can vary along several factors. A traditionally ideal graphene flake is of a very high aspect ratio, as charge carrier loss per unit length of the channel increases with a larger channel width[28]. To mitigate confusion, the material used as a channel in the devices produced for this research will be referred to as graphene. Technically, any graphene flakes consisting of more than one layer of graphene is not graphene at all; it is graphite. Graphite ultimately loses the ability to have its conductivity modulated by electric field as its layer number increases, which would effectively eliminate our ability to observe changes to its FET characteristics (it would no longer be a transistor). However, considering we were interested in exploring lithium intercalation, we wanted to ensure we had enough material available to serve as a reactant, increasing our ability to detect effects of intercalates during measurement. In order to suit both needs, I followed two rules in graphene flake selection for device channels. As long as the flakes were less than approximately 10 layers, they would exhibit predominately graphene (not

graphite) FET channel properties. Also, as long as flakes were still on the order of 5-20 nm along the channel width, they were permissible as device channels. In both cases, the additional volume would allow for more intercalation during experimentation.

3.2 Testing Graphene FET Functionality by Back Gating a Bare FET

Before depositing a solid electrolyte atop our graphene FETs (which significantly increases the chemical complexity of the system), measuring the electrical properties of the FETs provided an opportunity to confirm the functionality of the devices and establish a baseline to compare against post-deposition performance. It also provides an opportunity to describe the basic process by which FET transfer measurements may be evaluated; although the devices were not side-gated through a polymer electrolyte at this stage, they retained gate modulation functionality through the substrate, a wafer of p-doped silicon with a 90 nm top-layer of silicon oxide serving as the gate dielectric. A FET transfer measurement, or "transfer sweep," refers to the electrical measurement of a FET in which the source and drain electrodes are held at a constant bias V_{DS} (in all of our measurements, this value is 100 mV) and the gate potential V_G is varied across a voltage window while currents at the gate and drain electrodes are monitored. Instead of V_G, the specific type of gate electrode will often be indicated (as it is in this work) by type (V_{BG} for back-gate, V_{SG} for side-gate).

A representative back gated graphene transfer measurement is shown in Figure 3.2 (a). Plotted along the y-axis, the drain current, or the electrical current measured at the drain electrode (I_D), functions as a measure of the electrical current passing through the device channel from source to drain. Plotted along the x-axis, the back-gate (silicon substrate) was variably biased in a double sweep starting from -30 V, increasing to 30 V, and reversing to -30 V, all at a constant voltage rate of change (or sweep rate) of ± 1.2 V/s. Transfer sweeps such as shown in Figure 3.2 (a) are usually conducted as a double sweep in which the gate electrode is biased from the negative limit of the V_{BG} window to the positive limit and back. Typically, the two halves of a double sweep measurement (bisected by the sign of the sweep rate) are referred to as the forward (towards positive V_{BG}) and reverse (towards negative V_{BG}) sweeps.

It can often be difficult to distinguish the plot of the forward sweep from the reverse sweep, as is the case in Figure 3.2 (a). This is indicative of a small hysteresis, or the lagging of changes to a physical property (in this case, the change in I_D) behind changes to the inducing effect (the change in V_{BG}). Hysteresis can be avoided by decreasing the sweep rate of the measurement; however, the extent to which the hysteresis can be mitigated may be limited in some FET materials, as will be demonstrated in Section 5.1. The presence of large hysteresis suggests some manner of transport, mobility, or phase change limitation in the system of the device. It is expected of a typical graphene FET that the hysteresis measured during back-gating be small ($\leq 3\%$ of the gate window size) at the sweep rate shown here, and Figure 3.2 is consistent with these expectations.

Another significant feature worth identifying in Figure 3.2 (a) is the Dirac point voltage. A characteristic particular to graphene, the Dirac point refers to the energy level in the band structure where the valance and conduction bands meet. In a FET transfer characteristic measurement, the minimum of the drain current is also referred to as the "Dirac point voltage" or sometimes just "Dirac point," as this state of minimum channel conductivity arises as a result of the physical phenomenon. This is because gating the graphene channel shifts its Fermi level. When the Fermi level is above the Dirac point, the channel conductivity increases due to an excess of electrons. When the Fermi level is below the Dirac point, the channel conductivity increases due to an excess of holes. When combined, these phenomena

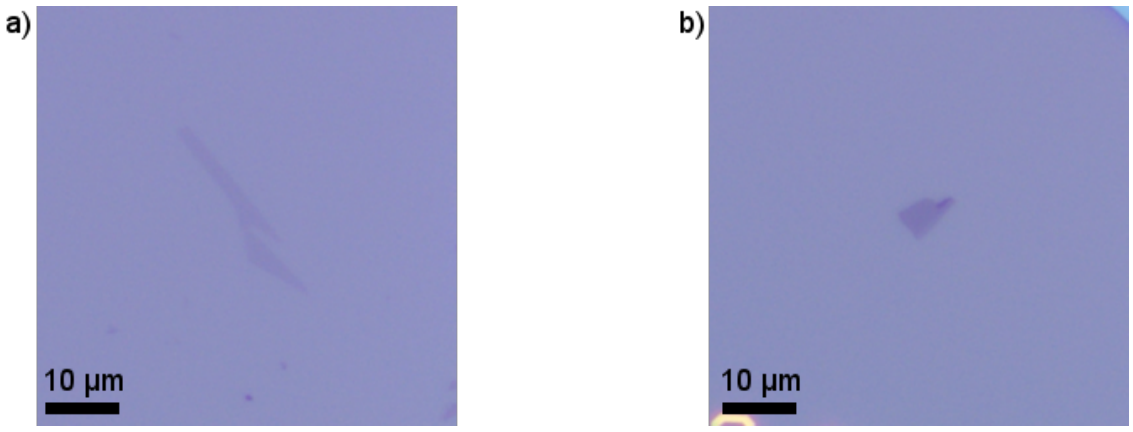


Figure 3.1: Optical Images of Graphene Flakes. Optical image comparison of (a) a graphene flake at 2 layers and 2 µm wide channel and (b) a graphene flake at approximately 8 layers and 7 µm wide channel. The larger volume present in (b) due to its increased thickness presents a more suitable candidate flake for investigating lithium intercalation.

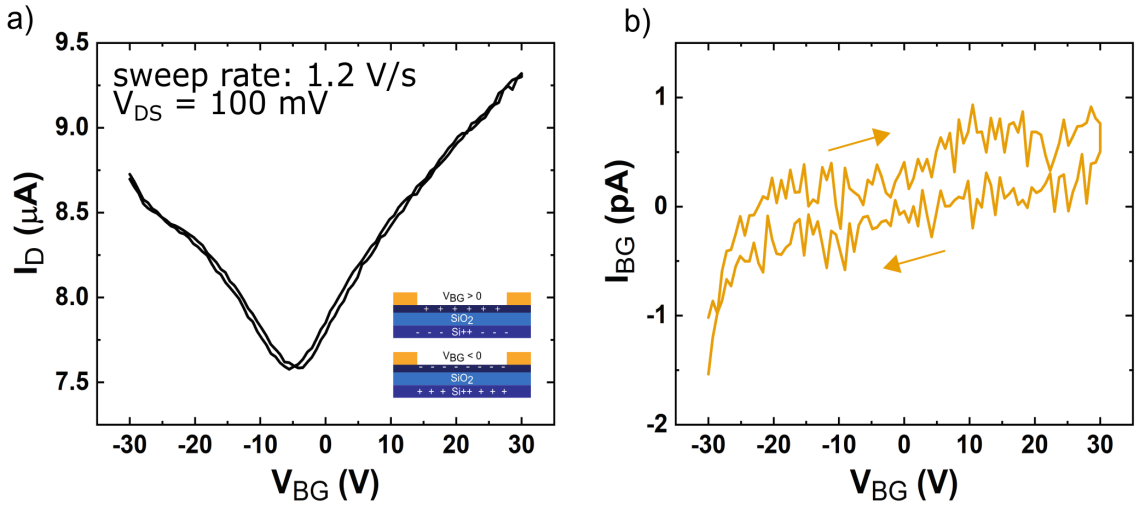


Figure 3.2: Transfer Characteristics of a Back-Gated FET Sample. Transfer characteristics of back-gated FET sample divided into (a) drain current (I_D, source to drain) (inset: cartoon of back-gated FET) and (b) back-gate current (I_{BG}, source to gate).

result in a minimum in graphene conductivity as the Fermi level equals the Dirac point. Even at the Dirac point voltage, graphene FETs often show relatively high minimum conductivity when compared to most semiconductor FETs (on the order of µA compared to pA), so many would argue that a graphene channel FET technically does not have an OFF-state.

The positioning of the Dirac point on the x-axis of a transfer sweep expresses the doping of the channel in a graphene FET. A perfect, undoped graphene channel would be symmetrical about 0 V V_{BG}, but this is difficult and uncommon to produce. Impurity doping from lab-grown graphene, adsorbates on the channel, films of photo- or e-beam resist from the fabrication process, and even interactions from the substrate can push the Dirac point of a device to be more negative (n-type) or more positive (p-type) relative to 0 V gate bias[42, 43, 44, 45, 46]. The devices produced in this research were treated to minimize any of these confounding contaminates by oxygen plasma cleaning the substrate before graphene exfoliation, minimizing sample exposure to ambient atmosphere, and thorough cleaning of the sample with organic solvent washes and nitrogen jet drying. Despite these efforts, the positioning of the Dirac point at about -5 V versus V_{BG} indicates n-type doping. We speculate that this results from e-beam resist residue, as has been demonstrated in other works[47, 46]. This doping also explains the seemingly higher current reached on the positive side of the gate bias; we would expect to reach a similar drain current at a more negative gate bias than was measured here. The presence of this dopant was not met with concern, as there was no speculation that the resist would inhibit the FETs' operation nor their electrochemical reactivity.

Figure 3.2 (b) depicts the back-gate current (I_{BG}) of this device during its transfer sweep. There is a very small amount of current that is passed from the source through the dielectric to the gate; this current is referred to as the gate current or "leakage current." Unlike the I_D, the leakage current reverses direction as the gate bias is reversed. Leakage current through the gate of a functional device is typically at least 2 orders of magnitude lower than the drain current; otherwise, it is frequently assumed that the device has developed an electrical short between the source and the gate (or the substrate had poor oxide growth in production) and is said to have undergone dielectric breakdown. This device has clearly not undergone a dielectric breakdown, as (seen in Figure 3.2(b)) the current is measured in pA as opposed to µA.

The work detailed here demonstrates the functionality of the graphene FETs developed and defines relevant features of a typical graphene FET's transfer characteristics. These features continue to be relevant in reviewing the results of side-gating the devices through a PEO:$LiClO_4$ polymer electrolyte as the dielectric. More relevant concepts will be introduced in the upcoming chapter regarding the implementation of quasi-reference electrodes in these same devices.

4.0 Designing and Conditioning Silver Quasi-Reference Electrodes for FET Geometries

This chapter focuses on work undertaken to incorporate a reference electrode into a graphene-based EDL FET. The goals of this work were (a) to identify a reference electrode material and implementation that would function with 2D EDL FET geometry and traditional FET measurement techniques, and (b) to evaluate the stability of the resulting electrode potential. We addressed these goals using open-circuit voltage measurements comparing potential drift between two reference electrodes at varying distances and by attempting to mitigate said drift with a conditioning method. Resulting from the open-circuit voltage measurements, it was concluded that the attempted conditioning method was ultimately unnecessary. Instead, a measurement protocol involving three initial transfer sweeps within the smallest measured gate window of -2.5V $\leq V_{SG} \leq$ 2.5 and 30-minute rest periods between all transfer sweeps with no additional reference electrode treatments was found to be sufficient for maintaining reference electrode potential.

4.1 On Silver Quasi-Reference Electrodes for Electrochemical Investigations of Graphene FETs

The design constraints of applying a reference electrode to a planar, vacuum-isolated FET system strains the practicality of classical electrochemical approaches. The primary limitation of traditional electrochemical analysis is its use of liquid electrolytes; in fact, essentially all commercial reference electrodes are designed to be submersed in aqueous solutions[48, 49]. However, EDL FET devices, including the devices fabricated for this work, are (1) often measured under vacuum in order to isolate the devices from atmospheric contaminates, and (2) use electrolyte as a layer or thin film in the solid state device[50, 51, 52, 53]. Incorporating a macroscopic, liquid-filled electrode into a ultra-high vacuum probe station while minimizing damage risk to the vacuum itself and simultaneously fully immersing the electrode in a

thin film becomes impractically expensive and difficult. Furthermore, we hoped to develop a reference electrode that could be incorporated in the 2D EDL FET design and fabrication workflow simply and without need of new measurement equipment; otherwise, it is highly unlikely that our peers and collegues will attempt to address the question of electrochemical reactivity in EDL FETs. Particularly, I expect the ability to lithographically define and fabricate such an electrode will go a long way to encourage those already familiar with this fabrication methodology to attempt electrochemical measurements in their research. Identifying the components and characteristics of a typical reference electrode will illuminate the framework by which we addressed this difficulty.

Figure 4.1 schematizes the geometry of most commercial reference electrodes as compared to the design we adopted for our reference electrode. The most common commercial reference electrodes are termed full half cells, and they are made up of four components: the body, top seal, junction, and active component[48]. The body and top seal isolate the filling solution of the reference electrode from the electrolyte of the electrochemical cell. Similarly, the junction of a reference electrode facilitates very slow ion transfer between the inside and outside of the electrode body, thereby protecting electrode's local chemical environment from that of the electrochemical cell. None of these components are inherently necessary in our design; simply using a solid polymer electrolyte already restricts ionic conductivity beyond that of a liquid electrochemical cell. Instead, we will focus on the active component.

Active components are a necessary part of any reference electrode (even in nonaqueous, solid-state, or thin-film systems), as they work together to establish the electrode's potential. In an Ag/AgCl reference electrode, for example, a silver wire and an AgCl salt coating make up the redox couple and are active components of the full half cell. However, approaches in nonaqueous or solid-state systems will frequently favor redox couple depositions over a couple shared between a metal wire and corresponding salt. For example, a study from Xiong et al. demonstrates lithium intercalation in MoS_2 using a lithium pellet as both a reference electrode and a Li^+ reservoir. This deviates from our goal of streamlined fabrication, as lithium metal is pyrophoric and must be handled with significant caution. Several other recently developed methods rely on the lithium iron phosphate (LFP) redox couple (particles incorporated into an ink or solution, deposited, and monitored with a contacting electrode)

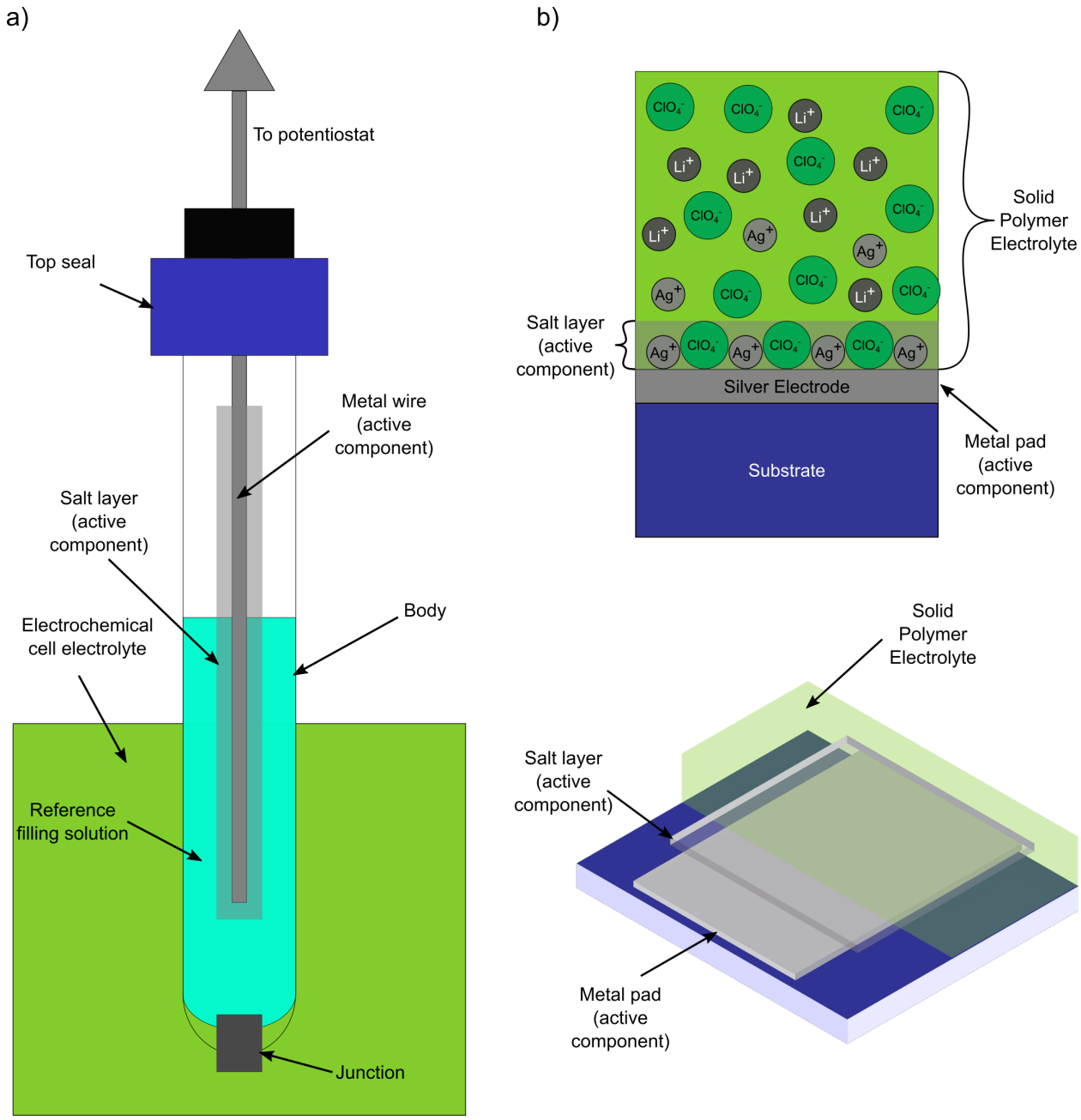


Figure 4.1: Reference Electrode Anatomy Diagrams. (a) Schematic breaking down the various components of a commercial reference electrode in analyte solution. (b) Cross-sectional (top) and isometric view (bottom) schematics of a 2D reference electrode for EDL FET implementation including hypothetical salt layer beneath solid polymer electrolyte.

as a reference electrode and have been used in thin-film planar systems[54, 18]. These efforts demonstrate excellent potential stability and may reflect a direction for future work in our project. However, in our first approach we desired to develop a methodology that reduced the number of new materials introduced into the device and utilized the familiar fabrication technique of lithography.

Therefore, motivated mainly by the desire for a simple, reproducible fabrication procedure, we chose to implement a bare Ag pad as a reference electrode. This approach is based on a common practice in analytical electrochemistry where bare Ag wires are used as "quasi-reference" electrodes in nonaqueous electrolytes. Quasi-reference electrodes are solid metal electrodes that, despite the absence of a surface coating containing the oxidized form of the redox couple, maintain relatively stable equilibrium potentials under measurement conditions. However, quasi-reference electrodes are prone to potential drift over long measurement times and high potential biases[48, 49]. Potential drift over time for quasi-reference electrodes can vary, with reports broadly differing from 2 mV per 5 hours to 7 mV per 7 days[55, 56, 57, 58, 59, 60, 61, 62]. Despite this, the stability of a quasi-reference electrode is still suitable for many measurements, and certainly presents a worthy first approach to easily fabricated electrochemical monitoring in FETs.

Among active materials for quasi-reference electrodes, silver presents a compelling material in the context of this work despite potential drawbacks. Silver electrodes can easily be integrated into the planar design of these FET devices and fabricated directly on the device substrate using the same lithographic processes as the gate, source, and drain electrodes. It is also noted, however, that silver has been shown previously to electromigrate across silicon surfaces, lending the material a level of physical instability that is not ideal for devices on our substrate of choice here[63]. Ultimately, we faced the decision between choosing a metal that is well understood in electrochemistry or searching for the perfect material for simple FET implementation. As a first look at electrochemistry in FETs, we elected to explore the possibilities provided by silver as the reference electrode's active material with an eye towards replacing silver with a more stable material in the future.

We also hypothesized that, in our electrolyte of choice, the stability of a silver reference electrode may be slightly improved from its as-fabricated state. In an Ag/AgCl reference

electrode, for example, the silver active component of the electrode is coated in a layer of AgCl salt; this salt layer ensures that the local environment of the Ag metal electrode always contains Ag^+, the second half of the Ag/Ag^+ redox couple, to maintain the electrode's potential. It was our hypothesis that, following electrolyte deposition, the surface of the silver electrode will react to form a layer of $AgClO_4$ salt to serve as the oxidized form of the Ag/Ag^+ redox couple and further stabilize the potential of the electrode:

$$2\,LiClO_4 + Ag_2O \rightleftharpoons 2\,AgClO_4 + Li_2O \tag{4.1}$$

To explore this possibility, we needed to evaluate the native potential drift of the silver electrode in PEO:$LiClO_4$. We also decided to investigate whether the stability under applied potential could be improved with a conditioning process to encourage a salt layer buildup on the surface of the electrode.

4.2 Open-Circuit Voltage Measurement of Silver Quasi-Reference Electrodes in a Solid Polymer Electrolyte

In a preliminary effort to observe the behavior of a silver quasi-reference electrode in contact with a solid polymer electrolyte, we made a set of open-circuit voltage (OCV) measurements of silver electrodes on SiO_2 with a PEO:$LiClO_4$ film on top. We fabricated the electrodes using an MLA lithographic fabrication process and electron beam metal evaporation to deposit 10 µm square silver pad pairs of varying distance apart on a substrate identical to the substrate used for the devices in this work. The pairs were designed at distances of 10 µm, 100 µm, and 1000 µm in order to compare voltage stability relative to electrode separation distance, as depicted in Figure 4.2 (a). Ultimately, the intention was to determine how much the electrochemical potentials of the silver pads would vary over time. In this OCV measurement method, the potentials of both silver pads were measured relative to ground while maintaining zero current to ground. Figure 4.2 (b), (c), and (d) depict representative potential versus time data for Ag electrodes at each inter-electrode distance. If the reference electrode potentials were completely stable, we would expect the difference

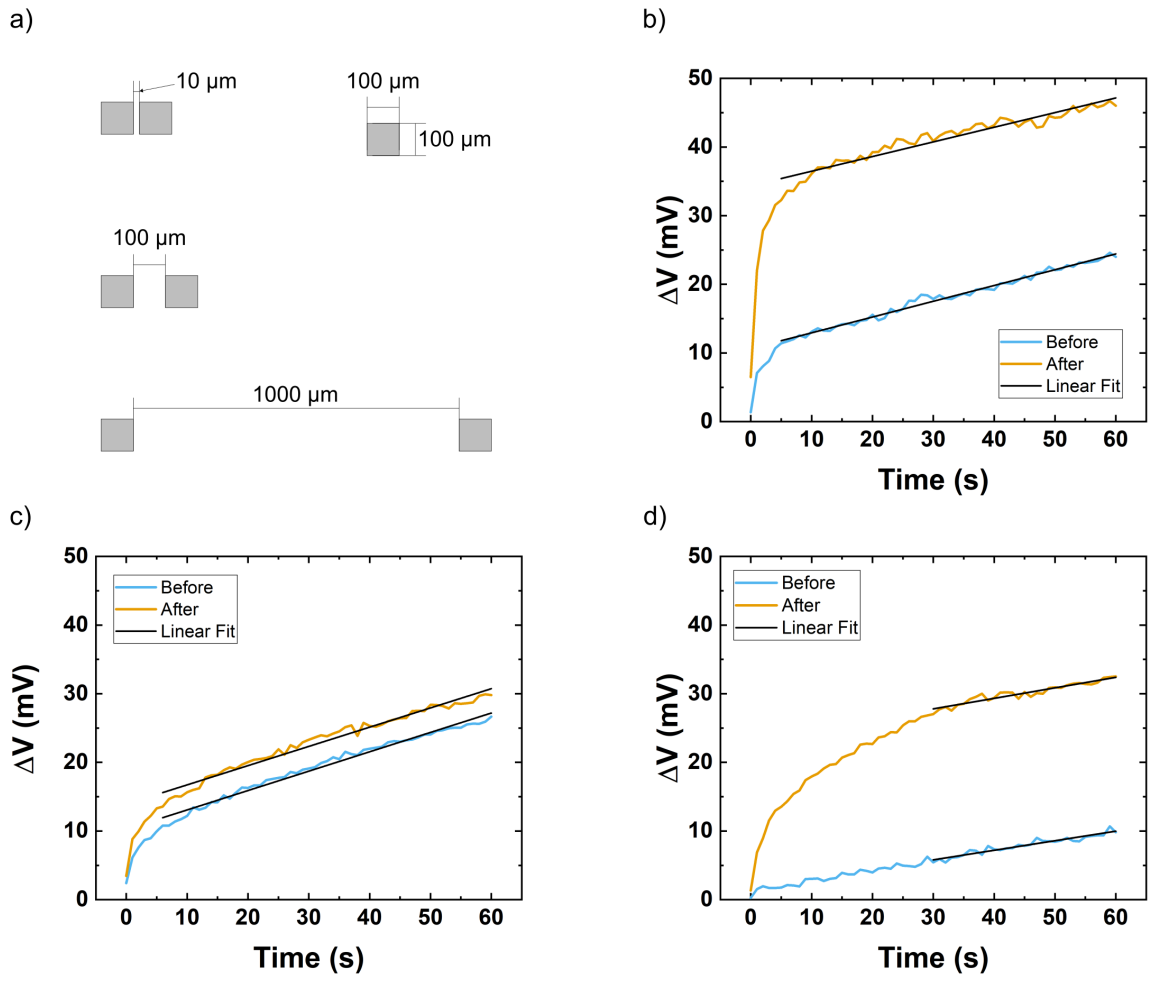


Figure 4.2: Open-Circuit Voltage (OCV) Ag Reference Electrode Measurements. (a) Schematic of reference electrode pads at given distances. (b, c, d) Representative OCV measurements from quasi-reference electrode pads beneath a PEO:$LiClO_4$ film; OCV data from pads pre-conditioning ("Before") and post-conditioning ("After") procedure at electrode distances of (b) 10 µm, (c) 100 µm, and (d) 1000 µm.

measured between each pad to vary no more than the noise floor of the equipment's potentiometer. However, the initial measurements from this experiment clearly show that a polarization emerges between the two electrodes in all cases. These results regularly reveal a sharp difference in the potentials of the paired electrodes (tens of mV over the first five seconds, as seen in Figure 4.2 (b) and (c)) followed by a predominately linear increase that continues to the end of the measurement. Best fit lines can be drawn from the 5 second marks through the end of the experiment. The slopes of linear best fits to the "Before" lines in (b), (c), and (d) after the first five seconds are 0.28 mV/s, 0.23 mV/s, and 0.15 mV/s, with y-intercepts at 10 mV, 11 mV, and 1 mV, respectively.

We needed to improve our reference electrodes' potential stabilities beyond what the OCV measurements suggested in our first measurements before embarking on FET transfer measurements. Although the polarization did not exceed 65 mV over the course of 60 seconds in any measurement, we expected our FET transfer measurements to take anywhere from 0.5 to 1.5 hours, which would allow drifts of several volts during each measurement. This amount of potential drift was unacceptable for our purposes, as it would eliminate any realistic ability to identify electrochemical phenomena by measured electrochemical potential. However, it is common to "condition" a fresh reference electrode by forcing current through the electrode[48, 49]. Alternating a bias against the reference electrode at above and below the redox potential of the reference electrode metal releases cations into the local environment to ionically bond with nearby anions:

$$\mathrm{LiClO_4 + Ag\ (s) \rightleftharpoons AgClO_4 + Li^+ + e^-} \tag{4.2}$$

$$\mathrm{Li^+ + e^- + PEO \rightleftharpoons PEO : Li} \tag{4.3}$$

This process coats the electrode with a salt layer and incorporates the oxidated part of the redox couple at the interface between electrode and the electrolyte, improving stability of the electrode's potential. With the hope of developing a $\mathrm{AgClO_4}$ coating on the electrodes, it was worthwhile to experiment with the electrode pads and see if the potential stability could be improved with a similar conditioning method. The conditioning method (described in detail in the Appendix) required holding one pad at ground while raising and lowering

the potential of the other pad by ± 0.5 V in a square wave (either ON or OFF). The bias between pads was designed as high as 0.5 V in order to ensure reduction and oxidation at each pad regardless of any electrochemical variation between the local environment of each electrode.

Unexpectedly, the conditioning process resulted not in improved stability, but instead a larger voltage offset between each two electrodes, as can be seen in the "After" data in Figure 4.2 (b, c, d). This is reinforced by the y-intercepts of linear best fit lines of the last 55 seconds of "After" data in Figure 4.2 (b), (c), and (d), which are 14 mV, 34 mV, and 23 mV, increasing as compared to the "Before" data by 4 mV, 24 mV, and 22 mV, respectively. The slopes of the lines, on the other hand, were remarkably consistent. Before and after conditioning, the slope of the 10 µm distant pads remained constant and the slope of the 100 µm distant pads decreased by 0.02 mV/s to 0.21 mV/s. The 1000 µm distant pads, not portraying the same sharp potential increase in the first five seconds of measurement as the other two samples, took a longer period of time (approximately 30 seconds) to reach a linear trend after conditioning. However, a linear best fit line taken from the last 30 seconds of the measurement provides a slope of 0.14 mV/s, decreasing by 0.01 mV/s from the "Before" slope.

Naturally, an increase in polarization between reference electrodes was the opposite of the intended effect of the conditioning process and requires further interpretation. Polarization between reference electrodes could be indicative of current flow between the two. In that case, it is possible that the conditioning sweeps increased the electrical resistance between the two electrodes, which would increase the polarization of the electrodes as a current flowed. The possibility of such a feedback loop can be investigated in the circuit diagram of these measurements in Figure 4.3 (a). It is necessary to pass some small amount of current in order to measure the voltage in a circuit; by measuring two pads simultaneously, it is altogether possible that our pads became biased as a result of the measurement feedback. In order to avoid this trouble in the future, we can redesign the measurement as depicted in Figure 4.3 (b). Rather than attempting to measure both pads simultaneously, grounding one pad and measuring the other will eliminate feedback from the measurement itself and simply measure the potential drift of the reference electrode vs. ground. Ultimately, this should yield a more accurate OCV measurement for stability assessment.

Despite the severe drift observed in these OCV measurements, the consistency of potential change over time slope before and after conditioning attempts left hope that the reference electrode potentials may be more stable than what the OCV measurements implied. Even so, this experiment ultimately left us uncertain regarding how we were affecting the local chemical environment of our reference electrodes and, subsequently, their potential stability. Fortunately, after a series of initial transfer sweep measurements on our FET devices while measuring the reference electrode potentials, we discovered an effective method of conditioning the electrodes and reducing potential drift to acceptable levels.

4.3 Conditioning Reference Electrodes with Small Gate Window FET Transfer Sweeps

Early measurements of the quasi-reference electrodes in the FET devices during FET transfer sweeps yielded a rather unexpected result. At first, devices were measured over a gate voltage window limited between -2.5 V $\leq V_{SG} \leq$ 2.5 V. The purpose of this was

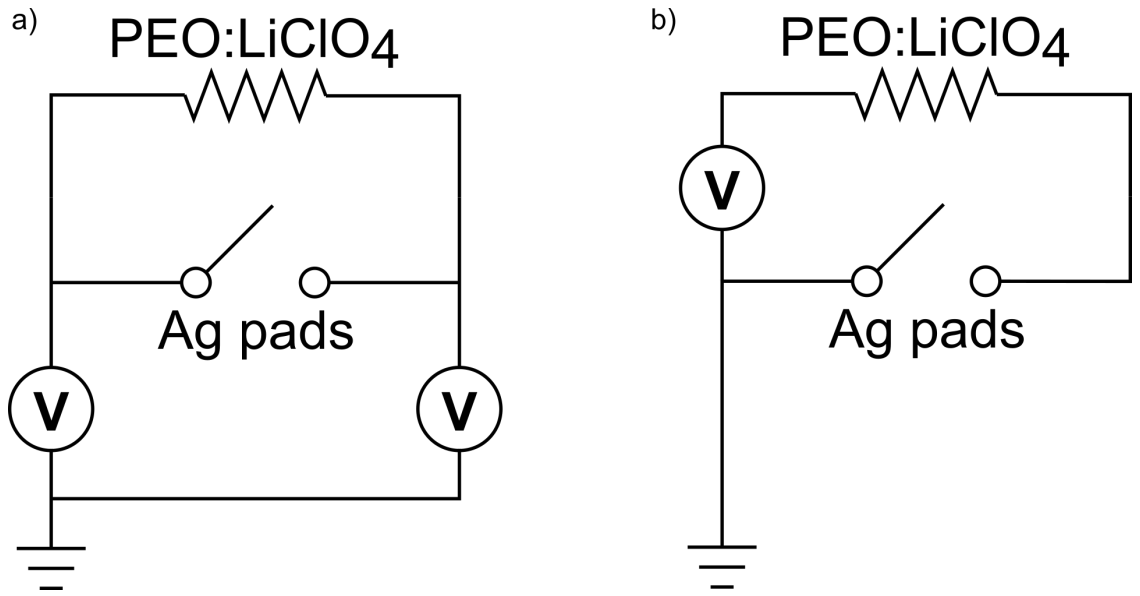


Figure 4.3: Circuit Diagrams of Open-Circuit Voltage (OCV) Ag Reference Electrode Measurements. (a) Circuit diagram of OCV measurement conducted in this work. Two source measurement units (SMUs) were used to measure voltage at two Ag pads separated by differing distances of PEO:$LiClO_4$. (b) Circuit diagram of a theoretical redesigned OCV measurement intended to reduce measurement feedback due to multiple simultaneous voltage measurements.

to minimize the possibility of electrochemical reactivity during these measurements while also gathering data from a large enough gate window that would show all of the relevant features in the transfer sweep: the Dirac point as well as the n- and p-branches. Sweeps were initiated by holding the gate bias at -2.5 V for one minute, and then the gate electrode potential was modulated from -2.5 V to 2.5 V and back. The sweeps were only separated in measurement by the 1-minute gate biasing and were otherwise measured continuously. It is also important to note that during these measurements, the back-gate was allowed to float (i.e., not connected to the measurement apparatus).

During these measurements, we noted a monotonic increase in the measured potential of the quasi-reference electrodes of 20 mV per sweep that would eventually saturate at about 400 mV higher than the original measurement. However, we found that after a 24-hour hiatus (during which the device was completely disconnected from the measurement equipment), the measured potential would recover to near its original state as shown in Figure 4.4 (a). Although the recovery was incomplete (the reference electrode potential remained $\sim$100 mV more positive than its initial value after the 24-hour hiatus), it led us to consider whether it would be possible to stabilize the reference electrode potential by introducing an extended rest period between each sweep.

Following this evidence, we took transfer measurements with a window of -2.5 V $\leq V_{SG} \leq$ 2.5 V across several devices, incorporating a 30-minute rest period between each measurement during which no bias was intentionally held on the devices. Ultimately, introducing this rest period between each individual sweep led to measurements in which the initial reference electrode potential drifted by less than 2 mV per sweep, as shown in Figure 4.4 (b). In addition, we found that, after 24-hours, the potentials of the quasi-reference electrodes would return to within $\pm$ 20 mV of the reading from the previous day. Accordingly, we decided that the 30-minute rest period gave the best trade-off between voltage stability and total measurement time, so we incorporated the rest period into the protocol we adopted for all FET measurements. That is, we included a 30-minute rest period between each measurement in transfer sweep experiments with consecutive sweeps.

Although the exact reason why this reference electrode stabilization method works so effectively is uncertain, we have several hypotheses. Particularly intriguing is the rever-

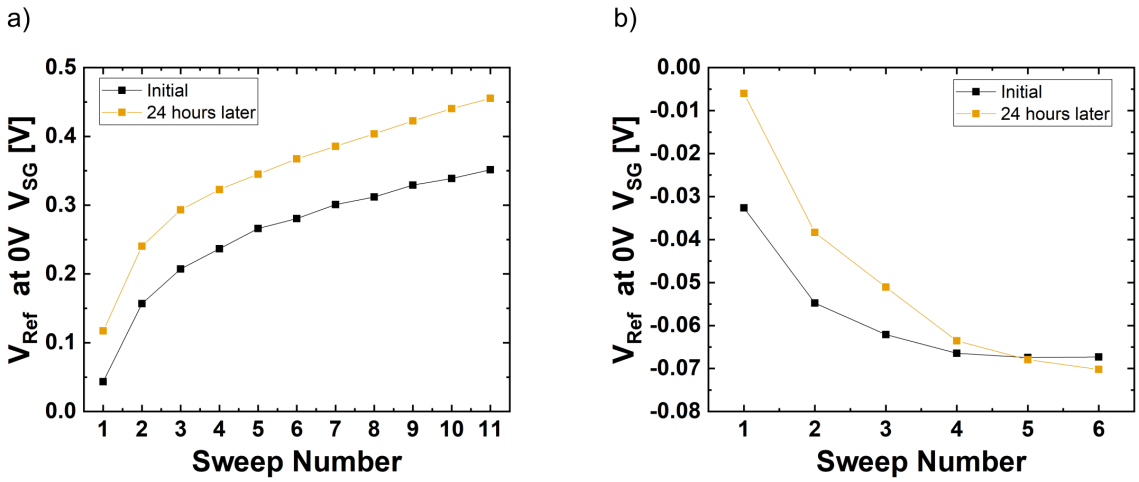


Figure 4.4: Reference Electrode Drift During FET Measurements with or without Rest Intervals. Representative data comparing reference electrode measured potentials across consecutive sweeps with (a) no rest interval between sweeps, and (b) 30-minute rest intervals between each sweep. Data shown also compares measurement series before and after a 24-hour rest period during which contact probes were completely disconnected from devices. Data shown in (a) and (b) are notably from different devices.

sal of the measured potential change between sweeps when comparing measurements with and without rest periods. This suggests that, during the sweeping of the device and the measurement of the quasi-reference electrode, either the channel experiences a net negative electrochemical bias during the sweep, or the quasi-reference electrode becomes increasingly positively charged during the measurement process. It is true that the gate electrode must be biased negatively for a period of time (1-minute in this work) prior to each measurement in order to allow anions to populate near the FET channel; however, the anions should be inducing a positive charge in the channel as opposed to a negative charge. Because the quasi-reference electrode is measured versus ground, and the source electrode is grounded, we would expect the measured reference potential to decrease with each sweep as a result of this measurement; however, it does not do this in the non-resting procedure. Instead, it seems more likely that quasi-reference electrode becomes increasingly positively charged as a result of the measuring process taking place during the experiment.

5.0 Modulating FET Gate Potential while Monitoring Reference Electrode Potential

As this reference electrode and conditioning method together provided acceptably stable reference potential measurements using PEO:$LiClO_4$ electrolyte, we used it to similar effect under higher side-gate voltage conditions. This tool to measure the system's electrochemical potential relevant to Ag/Ag^+ during FET measurements provided an opportunity to learn more about reactions that could be happening at the FET channel under different gate biases. However, without further information about the gate biases at which these reactions might occur, we required a combination of experiments. The first experiment implemented a progressively increasing gate potential range (a dynamic gate potential window) to identify as precisely as possible the gate potential at which any changes to the graphene channel began to occur. The second cycled over a single gate potential range (a fixed gate potential window) to isolate any transfer characteristic changes caused by reaching a reaction potential from those caused by opening the gate window.

5.1 Dynamic and Fixed Gate Potential Window Measurement Experimental Conditions

Both the dynamic and fixed V_{SG} window experiments were designed with the expectation of lithium intercalation in mind. As a result, all measurements in both experiments started and ended at -2.5V V_{SG}. This value enabled us to consistently capture the Dirac point of the transfer characteristics while reducing measurement times; lithium intercalation was expected to occur at the negative electrochemical biasing of the channel, or (equivalently) the positive electrical biasing of the gate electrode. All measurements were conducted with a sweep rate of 5mV/s and a V_{DS} of 100 mV. This is a relatively slow sweep rate as compared to the back-gated graphene FET device measurements in Figure 3.2 and was selected to reduce the hysteresis of each sweep, reflective of the slow ion mobility in PEO:$LiClO_4$. As

an example, a transfer sweep of -2.5 V $\leq V_{SG} \leq$ 7 V would take approximately 1.5 hours including the 30-minute wait, resulting in total experiment times of over 17 hours. The dynamic V_{SG} window experiment was designed to show how the transfer characteristics of the device changed as the maximum V_{SG} increased, so after a change in the device transfer characteristics had been observed the experiment was ended upon reaching time constraints. The fixed V_{SG} window experiment was designed after the results of the dynamic V_{SG} window experiment were reviewed; its upper-bound gate potential was selected so as to surely encompass the estimated onset V_{SG} potential of transfer characteristic changes observed in the first experiment, so an additional 2V V_{SG} were added to the identified onset potential as a maximum.

All experimental steps following the fabrication of the devices and the reference electrodes were conducted in one of two environments: an argon glovebox and a high-vacuum probe station. The PEO:$LiClO_4$ electrolyte was deposited according to a standard procedure (detailed in the Appendix) inside of the argon glovebox, including an anneal step during which excess solvent was evaporated off of the sample. The sample was then enclosed in a pressure-sealed, stainless steel transport case while still in the argon environment, and the case was transported from the glovebox to the probe station. The sample chip was transferred from the case to the probe station under high-vacuum conditions and subsequently sealed inside of the probe station before measurements. Based on the reference electrode conditioning experiments detailed in Section 4.3, we concluded that three conditioning sweeps would be sufficient to prepare the reference electrodes immediately before initiating either experiment. As in the reference electrode conditions experiments, the back-gate was allowed to float throughout these measurements.

5.2 On Interpreting Electrochemical Potential from Reference Electrode Measurements

Ultimately, the goal in this work is to evaluate observed changes in the graphene FET transfer characteristics as a result of increasing the V_{SG}, relate those changes to relevant po-

tentials as measured against the potential of the reference electrode, and evaluate candidate substances or contaminates in the graphene FET system that may have electrochemically reacted to cause said changes. The approach we took with these measurements involved monitoring the reference electrode potential alongside what was otherwise a series of standard FET transfer sweeps. Accordingly, the source was grounded in these measurements, and all other electrodes were either maintained or measured with respect to the potential of the source electrode. As a result, all reference electrode potential measurements in this device are recorded as non-constant values. Despite this, we assume that the reference electrode's absolute potential is unchanging, just as it would be in a more traditional solid-state electrochemical measurement[48, 49]. This assumption asserts that the changing potential measured on the reference electrode could only be a reflection of the changing potential of the ground of the measurement; that is, the changing potential of the source (and, subsequently, the drain and gate) electrode. Interpreted in this manner, we are able to compare the electrochemical potential of the graphene channel as it changes versus the relatively constant potential of the quasi-reference electrode.

5.3 Broad Trends in the Dynamic V_{SG} Window Measurements

Again, our aim with the dynamic V_{SG} window series of measurements was to explore the impact of increasing the gate window size in the positive direction on the FET transfer characteristics on a step-by-step basis. Each opening allowed for the careful observation of any new features or changes to previously existing features. The initial hypothesis for these measurements was to find evidence of lithium intercalation at a gate bias closer to 3 V, and this is reflected in the design of the experiment. Ultimately, we had to increase the V_{SG} window size to 5 V V_{SG} before observing significant changes. As seen in Table 5.1, the first three measurement windows were only increased by 0.5 V from each previous measurement window. However, due to time constraints, it became necessary to increase the window step size to 1 V per sweep.

Table 5.1: Sweep Number and Maximum V_{SG} of Dynamic Gate Potential Window Measurements

Sweep Number	Maximum V_{SG}[V]
1, 2, 3, 13	2.5
4	3
5	3.5
6	4
7	5
8	6
9	7
10	8
11	9
12	10

Figure 5.1 shows the data collected during the V_{SG} window expansion portion of the experiment(Sweeps 3 - 12). Due to an over 370% increase in maximum I_D from Sweep 3 (V_{SG} upper-bound of 2.5 V) to Sweep 12 (V_{SG} upper-bound of 10 V), the I_D data are split across Figure 5.1 (a) and Figure 5.1 at Sweep 7 (V_{SG} upper-bound of 5 V, plotted on both (a) and (b) for continuity) to prevent conflicting scaling.

The most striking change in the I_D is the evolution of a ramping current increase as the maximum V_{SG} increases. The sweeps up to 3.5 V V_{SG} (part of Figure 5.1 (a)) demonstrate relatively little I_D change as the V_{SG} window is increased. This is consistent with side- and top-gated graphene EDL FETs in research literature, as they are frequently pushed only to or just past 3 V V_{SG}[24, 25, 26]. However, upon pushing the V_{SG} to the 4.0 V maximum V_{SG} measurement, we begin to see a change evolve as the I_D increases slightly in the reverse sweep. This I_D increase becomes more evident with each subsequent measurement, notably in the very next sweep to a V_{SG} upper-bound of 5.0 V as plotted in Figure 5.1 (a). By the 5.0 V V_{SG} maximum sweep, the maximum I_D has increased from that of the initial 2.5 V

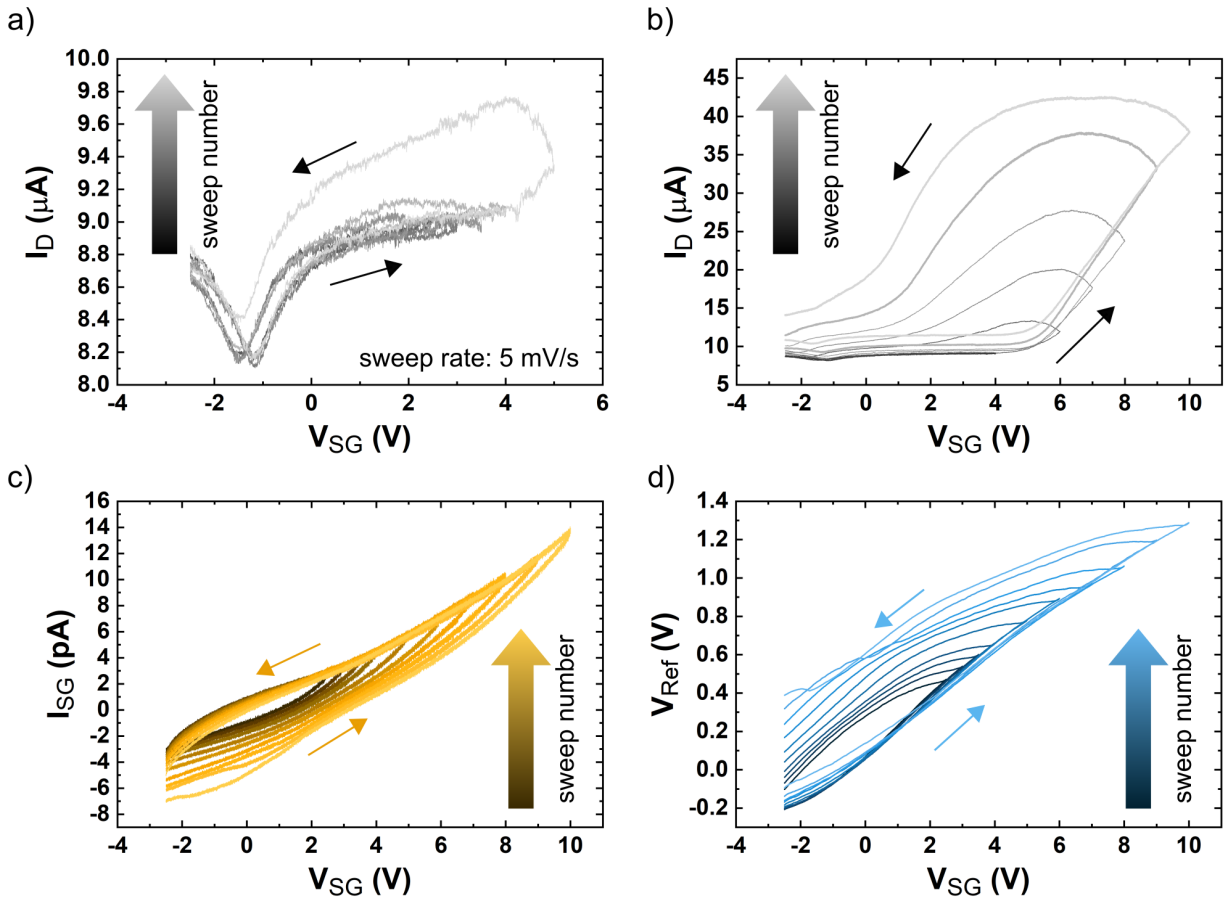


Figure 5.1: Dynamic V_{SG} Window Transfer Characteristics. Complete set of window expansion sweeps (Sweeps 3 - 12) from the dynamic V_{SG} window experiment. All measurements taken at sweep rate of 5 mV/s and V_{DS} of 100 mV. Sweep directions marked with arrows. Increasing sweep number indicated by dark-to-light color gradients. (a) I_D transfer characteristics from Sweeps 3 - 7 (plotted separately to prevent conflicting scaling). (b) I_D transfer characteristics from Sweeps 7 - 12. (c) I_{SG} transfer characteristics. (d) V_{Ref} measured reference potential.

V_{SG} maximum sweep by 8%, although the I_D at the Dirac point remains unchanged on the forward sweep; this proves that some potential 4.0 V $\leq V_{SG} \leq$ 5.0 V causes the increase in I_D. By the final measurement (which pushes the V_{SG} maximum to 10.0 V), the maximum current has increased by 371.8%. and the forward sweep Dirac point current has increased by 26.4% from the initial 2.5 V V_{SG} maximum sweep.

With increased V_{SG} maximums, we see changes in other features of the I_D transfer measurements for this device. For example, it is apparent from Figure 5.1 (b) that the reverse sweeps consistently display an increase in I_D, reach a maximum, then decrease. Particularly interesting is the continued increase in current after the V_{SG} sweep direction has reversed. This may suggest that the sweep rate is too fast to accurately reflect the maximum I_D for a given V_{SG} due to the slow movement of ions. However, it may also suggest that the graphene channel is being reversibly doped as a result of an electrochemical reaction. Both of these hypotheses are reinforced as, by the final measurement, the Dirac points of the forward and reverse sweeps have shifted n-type by different magnitudes; the forward sweep Dirac point has moved by -0.5 V, while the reverse sweep Dirac point has moved by -1 V.

Between the increased I_D and negatively shifted Dirac points in these electrical transfer characteristics, it is evident that there have been changes to the graphene channel of the device. However, with only the dynamic V_{SG} window measurement in hand, it is difficult to distinguish between changes attributable to a specific electrochemically active voltage versus changes that are attributable to the increasing V_{SG} upper-bound. In order to do so, we must also measure and observe any changes over a series of measurements that maintain a consistent V_{SG} window yet still operates comfortably on both sides of the 4–5 V V_{SG} potential of the observations made in this experiment.

5.4 Broad Trends in the Fixed V_{SG} Window Measurements

The fixed V_{SG} window measurements were designed after the dynamic V_{SG} window measurements were taken and used some of the information gathered from the earlier experiment in the design process. By cycling a device at a fixed gate potential window, we ensured that

any collected data reflects changes caused specifically as a result of the device being in a state of gating between 2.5 V and 7.0 V V_{SG}. The bounds of the fixed gate window were chosen to ensure that the 4–5 V V_{SG} range noted as containing a possible electrochemical reaction potential in the dynamic V_{SG} window experiment was included in the measurement. For this experiment, we used a fresh device that had been previously measured only in the range from -2.5 V $\leq V_{SG} \leq$ 2.5 V. As shown in Table 5.2, this experiment was comprised of 12 total measurements: 3 conditioning sweeps, 8 sweeps with the V_{SG} window of -2.5 V $\leq V_{SG} \leq$ 7.0 V, and a final sweep mimicking the conditioning sweeps.

Table 5.2: Sweep Number and Maximum V_{SG} of Fixed Gate Potential Window Measurements

Sweep Number	Maximum V_{SG}[V]
1, 2, 3, 12	2.5
4, 5, 6, 7, 8, 9, 10, 11	7

Figure 5.2 depicts the relevant transfer characteristics for the fixed window sweeps (Sweeps 4 - 11). Similar to the dynamic V_{SG} window experiment, I_D (depicted in Figure 5.2 (a)) shows a trend of increasing I_D current; however, unlike in the dynamic V_{SG} window experiment, we can attribute the changes observed in these data to the limited V_{SG} window alone. Notably, Sweep 4 (the first experimental sweep in this series) stands out very clearly in the I_D curves; the current does not begin to sharply increase until about 4.5 V V_{SG}; after this, the I_D increases similarly to the that from the dynamic V_{SG} window experiment. The trend continues as each new sweep leads to an overall increase in I_D current, although the magnitude of I_D change is shown to approach saturation in both the maximum and minimum I_D values in Figure 5.2 (b). The minimum I_D of the fixed V_{SG} window device does not decrease to its original state when the V_{SG} window is reduced to -2.5 V $\leq V_{SG} \leq$ 2.5 V in Sweep 12, demonstrating that although the maximum V_{SG} value is a feature of channel doping through high V_{SG} potential, the channel itself has also undergone a lasting decrease in resistivity.

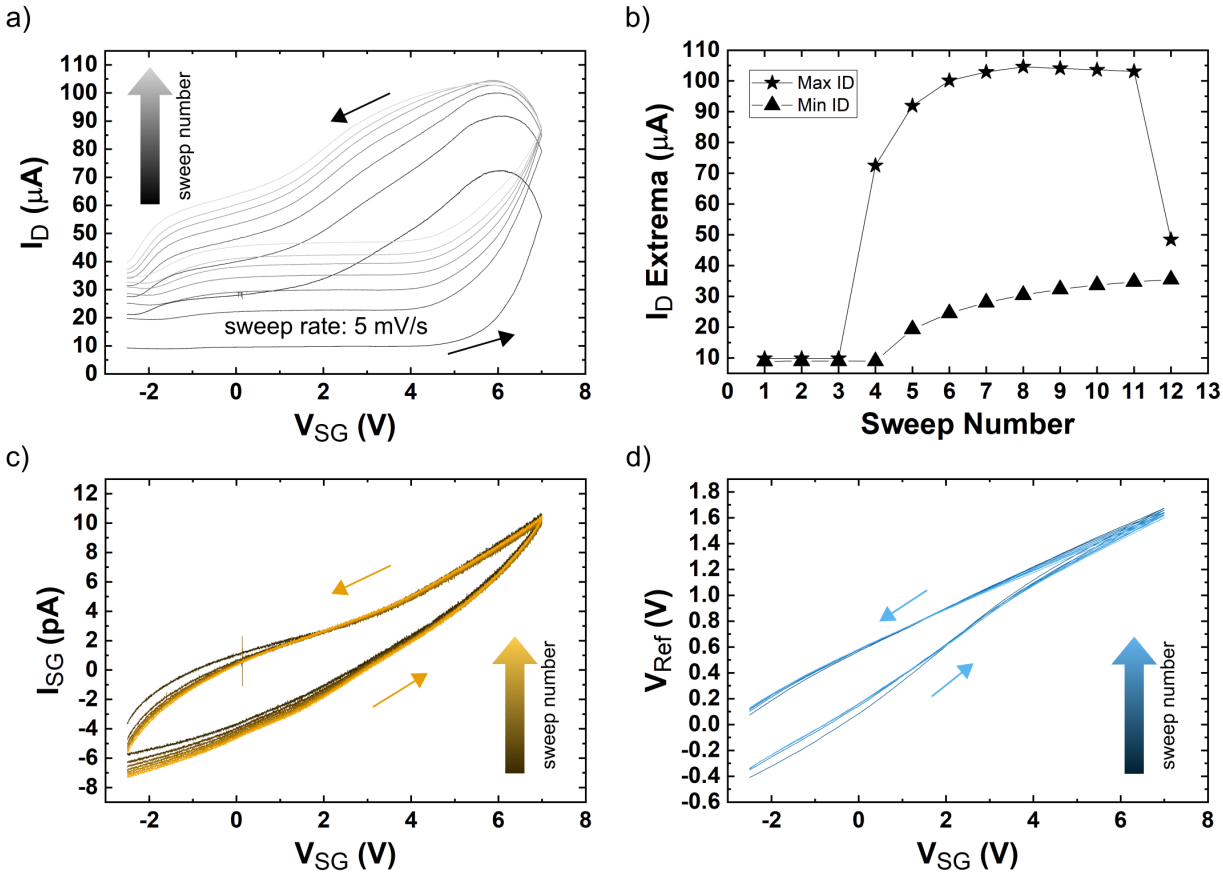


Figure 5.2: Fixed Gate Window Transfer Characteristics. Set of fixed window sweeps (Sweeps 4 - 11) from the fixed V_{SG} window experiment. Sweep 10 has been excluded due to poor contact during measurement. All measurements taken at sweep rate of 5 mV/s and V_{DS} of 100 mV. Sweep directions marked with arrows. Increasing sweep number indicated by dark-to-light color gradients. (a) I_D transfer characteristics. (b) Comparing trends of maximum (stars) and minimum (triangles) I_D values across all 12 sweeps. (c) I_{SG} transfer characteristics. (d) V_{Ref} measured reference potential.

The fixed V_{SG} window experiment also provided the best opportunity to observe the performance of the silver reference electrode. As previously described, many quasi-reference electrodes show potential drift over the course of multiple measurements and extended periods of time. The fixed V_{SG} window experiment provides insight into reference electrode's stability under experimental conditions, as the V_{Ref} can be compared across 8 subsequent measurements of the same V_{SG} window. As seen in Figure 5.3, we can sample V_{Ref} data points from identical V_{SG} potentials present in all experimental sweeps to observe reference potential stability. In the dynamic V_{SG} window experiment (Figure 5.3 (a)), the reverse sweep V_{Ref} data points increase to reflect the increasing V_{SG} maximum on each subsequent sweep. This is demonstrative of polarization of either the reference electrode or the device ground due to the influence of the V_{SG}. The forward sweep data points, not having been exposed to the new V_{SG} maximum since the last experiment, show greater consistency, with standard deviations of less than 40 mV. Contrastingly, the static V_{SG} experimental V_{SG} data shows consistency, reporting a standard deviation of less than 20 mV. These values provide a sense of the voltage drift of our reference electrodes, and both are acceptable for the purposes of our measurements; a < 100 mV potential variation over the course of the full experiment is close enough to distinguish electrochemical reaction potentials.

5.5 Comparing Changes Observed in both FET Transfer Characteristics

As shown in Figure 5.4, most changes to the transfer characteristics of a graphene FET can be identified as one of six transformations: an increase or decrease to the drain current of the device (Figure 5.4 (a)), an increase or decrease in the ON/OFF ratio of the device (Figure 5.4 (b)), or a shifting of the Dirac point resulting from either an n- or p-type doping (Figure 5.4 (c)). In graphene FETs that are carefully isolated from contaminants or exogenous chemical reactions before or during measurements, it is unlikely to observe any of these characteristics as "changes"; instead, the device measured will likely show consistent transfer characteristics throughout the measurement, even if it is already deviating from the "ideal" graphene characteristics outlined in gray in the figure. However, because we are looking for

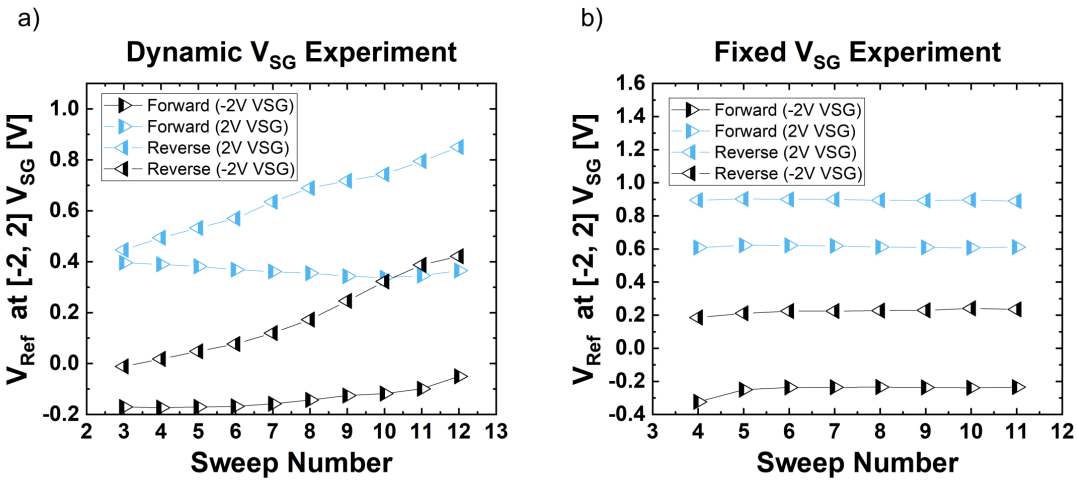


Figure 5.3: Analysis of V_{Ref} Drift in Dynamic and Fixed V_{SG} Window Experiments. Data points sampled at -2 V and 2 V V_{SG} in both the forward (right-pointing arrows) and reverse (left-pointing arrows) sweeps. (a) Dynamic V_{SG} window experiment V_{Ref} data samples from all window-expansion sweeps (Sweeps 3 - 12). (b) Fixed V_{SG} window experiment V_{Ref} data samples from all -2.5 V $\leq V_{SG} \leq$ 7.0 V V_{SG} sweeps (Sweeps 4 - 11).

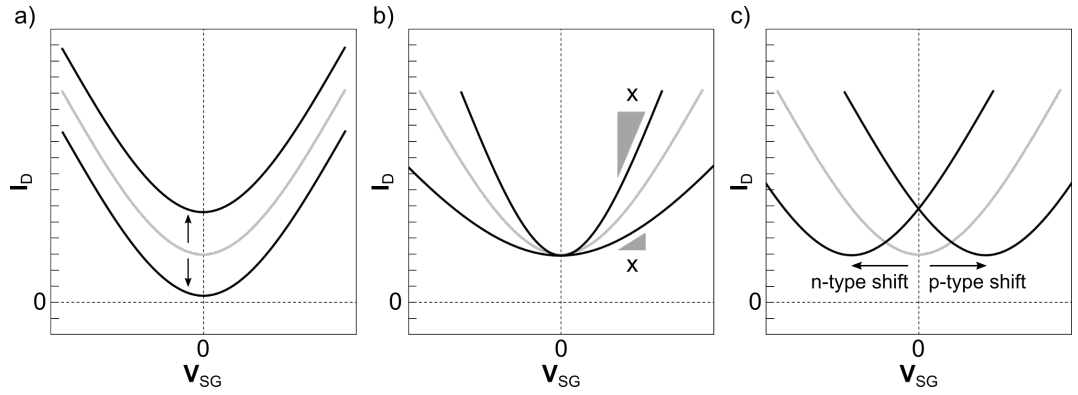


Figure 5.4: Graphene FET I_D Transfer Characteristic Changes Resulting from Physiochemical Phenomena. Cartoon of FET I_D transfer characteristic transformations resulting from chemical or physical changes to the channel. "Ideal" (native or unreacted) graphene I_D curve outlined in gray. (a) Increase or decrease of the I_D.(b) Increase or decrease of the ON/OFF ratio. (c) Dirac point shift resulting from an n-type (left) or p-type (right) doping.

a physical or chemical change in the graphene channel due to lithium intercalation (or any other electrochemical phenomenon), we are expecting to see a change in the transfer characteristics of the graphene FET that reflects those changes. In order to address the changes to the graphene channel, it is necessary to compare data from two equivalent experimental conditions; that is, with two measurements from the same V_{SG} window, sweep rate, and V_{DS}. This was taken into consideration in both experimental designs, as in both experiments a final measurement was conducted at the same V_{SG} bounds as the conditioning sweeps.

The plots shown in Figure 5.5 depict the final conditioning sweep (Sweep 3) from each experiment as the initial state of the FET transfer characteristics, and an identical sweep conducted immediately after both series were concluded (Sweeps 13 and 12 from the dynamic and fixed V_{SG} window experiments, respectively). Four particular changes from the before and after measurements that are identical in direction (if not magnitude) across the two experiments can be identified:

1. Increased average drain current
2. Negative V_{SG} shifted Dirac points in both forward and reverse sweeps
3. Increased ON/OFF ratio
4. Negative-shifted and higher slope side gate current

Note that the V_{SG} range in both sets of measurements is identical for each sweep. The implication of these changes (being altered device transfer characteristics from before and after electrical stressing via the V_{SG}) is that an electrochemical reaction has occurred. Identifying possible electrochemical reactions in our experiments relies on the answers of two questions:

1. At what electrochemical potential do observed changes to the graphene FET's transfer characteristics occur?
2. What compounds and contaminates participating in reactions near that potential may be present in the device and its system?

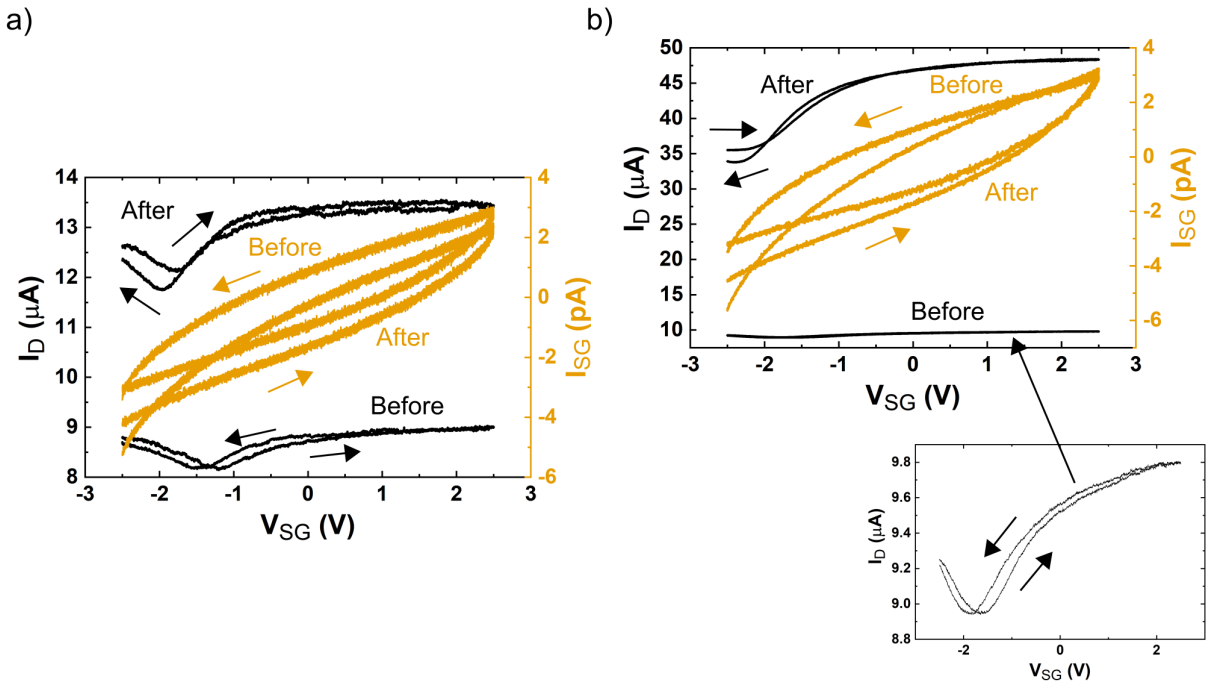


Figure 5.5: Graphene FET Transfer Measurements Before and After Experiments. The final conditioning sweep (Sweep 3) and the final sweep overall (Sweeps 13 and 12, respectively) from the dynamic and fixed V_{SG} window experiments. All measurements taken at sweep rate of 5 mV/s, V_{DS} of 100 mV, and V_{SG} window of -2.5 V $\leq V_{SG} \leq$ 2.5 V. I_D outlined in black, I_{SG} outlined in gold. Final conditioning sweep labeled "Before," final overall sweep labeled "After." Sweep direction indicated with arrows. (a) "Before" and "After" sweeps from the dynamic V_{SG} window experiment. (b) "Before" and "After" sweeps from the fixed V_{SG} window experiment. (inset) Smaller I_D window to depict "Before" fixed V_{SG} window experiment with appropriate scaling.

5.6 Identifying a Likely Electrochemical Reaction Potential

In hopes of confirming and identifying an electrochemical reaction, we returned to the previously identified potential of near 4 V V_{SG} the voltage at which the first apparent change in the I_D curves in both experiments occurred. We will refer to this potential as the "onset potential." The early sweeps from each experiment support this assertion.

Figure 5.6 (a) shows Sweeps 3 - 6 of the dynamic V_{SG} window experiment. Of particular note in these measurements is the consistency of the Dirac point potentials and the I_D across the measurements. The most noticeable change from measurement to measurement arises in the reverse sweep of Sweep 6 at about 2 V V_{SG} where a maximum peak just barely begins to surface, evidence of the earliest changes to the I_D slope. More noticeable is the apparent change in I_D magnitude that occurs after Sweep 4 of the fixed V_{SG} window experiment. Figure 5.6 (b) shows the fixed V_{SG} window potential Sweeps 4 and 5, the first and second non-conditioning sweeps of the experiment. The I_D of Sweep 4 remains within 1 µA of the maximum I_D from the conditioning sweeps until, shortly after crossing the onset potential, it begins increasing, ultimately reaching nearly 8 times the maximum I_D of the conditioning sweeps. Most importantly, the I_D does not recover before the next sweep, indicating that a change to the graphene channel has occurred.

To further evaluate the onset potential as a possible electrochemical reaction potential, we compared the onset potential across both experiments to explore its consistency. The plots in Figure 5.7 depict (in black) drain currents from individual sweeps from each experiment. Figure 5.7 (a) and (b) depict the 5 V V_{SG} and 7 V V_{SG} maximum sweeps from the dynamic V_{SG} window experiment, respectively. Figure 5.7 (c) depicts the 7 V V_{SG} maximum sweep from the fixed V_{SG} window experiment. The y-axes have been adjusted to maintain visibility of the inflection of the I_D curves, but with identical y-axis window size to maintain scaling across each plot. Comparing the onset potentials from Figure 5.7 (a) and (b), two sweeps from the same experiment, shows that it is remarkably consistent within a single device, with the onset potentials lying at 4.3 V and 4.5 V V_{SG} respectively. The consistency between devices is somewhat weaker, as in Figure 5.7 (c) we can see an onset potential of 3.9 V V_{SG}. Ultimately, we can conclude that the gate bias at which the channel becomes markedly more

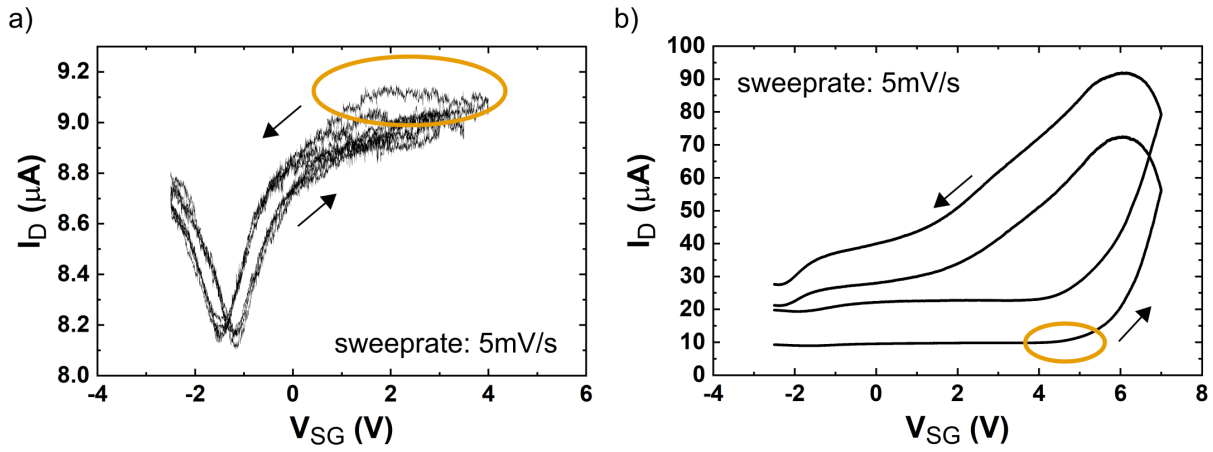


Figure 5.6: Evidence Supporting the Onset Potential as a Reaction Potential. Early measurements from both dynamic and fixed V_{SG} window experiments highlighting I_D changes occurring as a result of passing the onset potential. All measurements taken at sweep rate of 5 mV/s and V_{DS} of 100 mV. Sweep direction indicated with arrows. (a) Sweeps 3 - 6 of the dynamic V_{SG} window experiment. First observation of I_D current increasing on the reverse sweep circled in gold. (b) Sweeps 4 and 5 of the fixed V_{SG} window experiment. First observation of I_D slope change resulting in subsequent I_D increase across all points circled in gold.

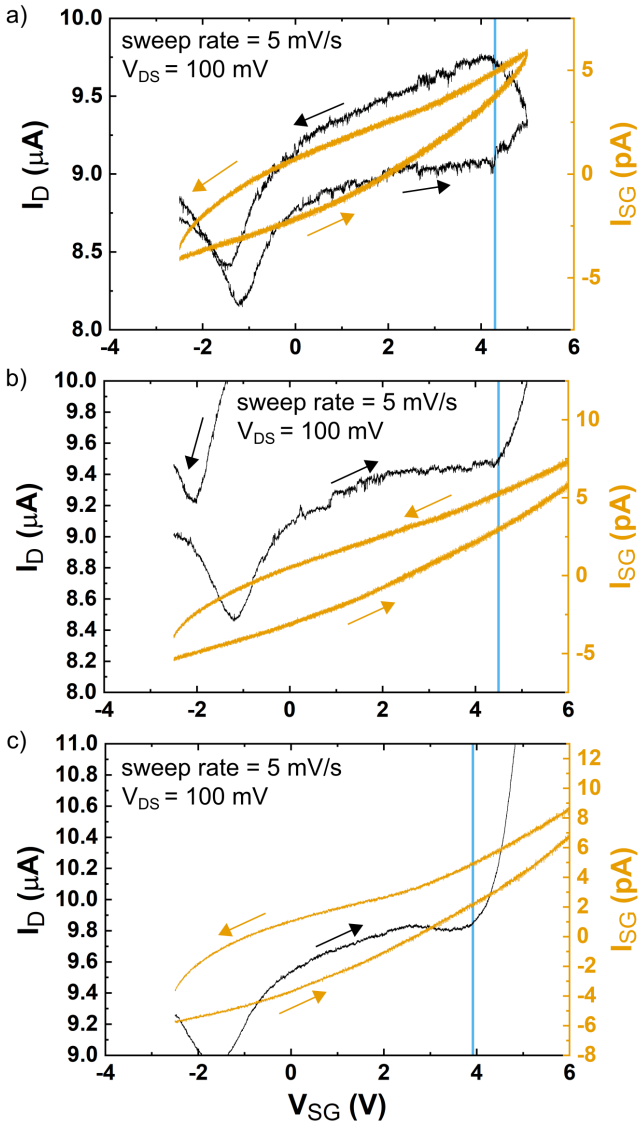


Figure 5.7: Onset Potential vs. V_{SG}. Individual measurements from each experiment compared to evaluate the consistency of the onset potential as related to V_{SG}. All measurements taken at sweep rate of 5 mV/s and V_{DS} of 100 mV. Sweep direction indicated with arrows. Onset potential indicated by blue vertical line. (a) Sweep 7 of the dynamic V_{SG} window experiment, the first sweep of the experiment to reach 5 V V_{SG}. Onset potential: 4.3 V V_{SG}. (b) Sweep 9 of the dynamic V_{SG} window experiment, the first sweep of the experiment to reach 7 V V_{SG}. Onset potential: 4.5 V V_{SG}. (c) Sweep 4 of the fixed V_{SG} window experiment, the first sweep of the experiment to reach 7 V V_{SG}. Onset potential: 3.9 V V_{SG}.

conductive is indeed consistent on the order of ± 600 mV with respect to each onset potential. However, it does not specifically show that an electrochemical reaction is occurring, nor what that reaction might be. Monitoring the side-gate current and the reference electrode potential, respectively, can provide this information.

Like any other FET transfer characteristic feature, the onset potential is natively observed with reference to V_{SG}; however, in order to properly relate it to any other electrochemical reaction, it must also be correlated to some point of reference. Plotted in Figure 5.8 (a), (b), and (c) depict the exact same sweeps as shown in Figure 5.7. However, instead of plotting the I_D from each measurement versus V_{SG}, the I_D is plotted versus negative V_{Ref}. Similarly, the I_{SG} is negated to reflect the current flowing to the channel. Because the V_{Ref} is measured instead of controlled like V_{SG}, the window size of the x-axes of these plots vary according to the maximum and minimum potentials reached by the reference electrodes.

The I_{SG} data can provide tentative further evidence of establishing the onset potential as a chemical reaction potential. In electrochemical analysis, current measured in the counter electrode is used to evaluate if a chemical reaction has occurred; if the current increases, that is evidence of an ongoing chemical reaction causing the current increase. The situation in our FET devices is somewhat different. There is always a leakage current flowing through the electrolyte between the source, drain, or channel and the gate, and this leakage current can mask current driven by an electrochemical reaction. However, what we can observe is the mild I_{SG} slope change that occurs near the onset potentials. This is most clearly seen in Figure 5.8 (c). The steeper slope reflects an increase of electrons flowing away from the gate, which is exactly what would occur during a reduction reaction at the channel.

In the same manner of plotting, we are able to interpret the electrochemical potential of the source (the ground of the original measurement) as it changes versus the potential of our reference electrode. Figure 5.8 (a), (b), and (c) depict onset potentials of -0.7 V, -0.7 V, and -1.1 V vs Ag/Ag^+, respectively. Here, we see a ± 400 mV variation in onset potential between experiments, once again an acceptable reference variation for our purposes. More importantly, this time we can actually relate the potential (through an approximation versus Ag/Ag^+) to potentials of electrochemical reactions possibly present in these experiments.

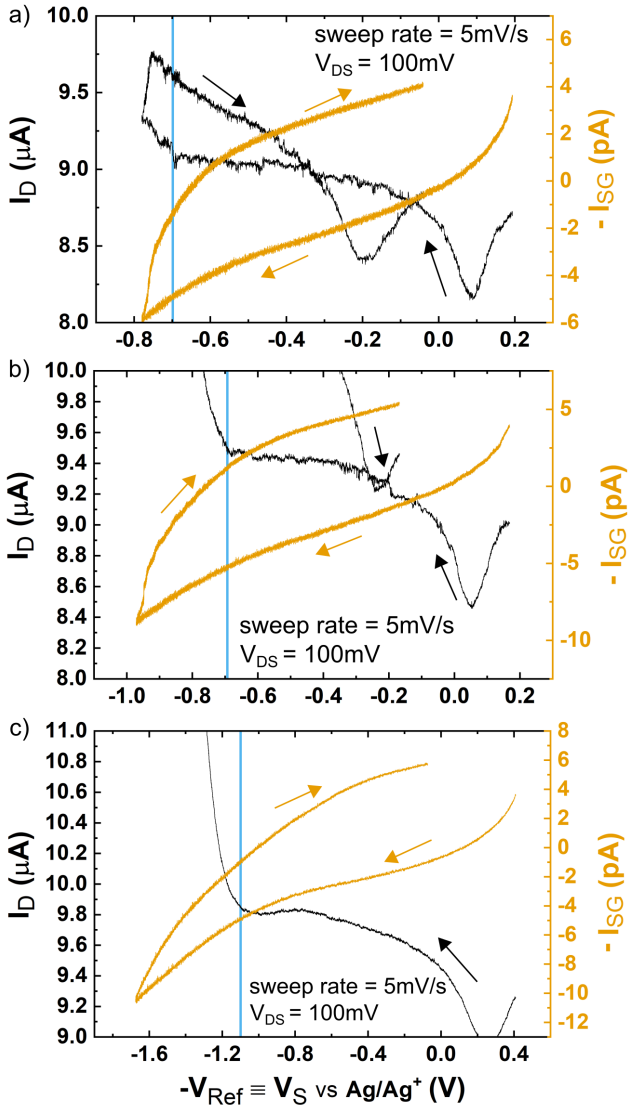


Figure 5.8: Onset Potential vs. -V_{Ref}. Individual measurements from each experiment compared to evaluate the consistency of the onset potential as related to -V_{Ref}. All measurements taken at sweep rate of 5 mV/s and V_{DS} of 100 mV. Sweep direction indicated with arrows. Onset potential indicated by blue vertical line. (a) Sweep 7 of the dynamic V_{SG} window experiment, the first sweep of the experiment to reach 5 V V_{SG}. Onset potential: -0.7 V vs. Ag/Ag^+. (b) Sweep 9 of the dynamic V_{SG} window experiment, the first sweep of the experiment to reach 7 V V_{SG}. Onset potential: -0.7 V vs. Ag/Ag^+. (c) Sweep 4 of the fixed V_{SG} window experiment, the first sweep of the experiment to reach 7 V V_{SG}. Onset potential: -1.1 V vs. Ag/Ag^+.

5.7 Exploring Possible Electrochemical Reactions

The evidence described in this section suggests that our hypothesis about lithium intercalation (and the popular claim made in the device community) is false. Figure 5.9 outlines electrochemical potentials either of compounds possibly present in the device environments (top, blue) or of observations from the experiments (bottom, yellow) as plotted against Ag/Ag^+, an estimate of the reference electrode potential in these devices. Given uncertainty of the exact reference potential of reference electrodes (and noting a $\sim$0.4 V difference between the onset potentials from each experiment), we would expect any notable electrochemical potentials, if attributable to the onset potential of changes to the transfer characteristics of the graphene FETs, to at most fall within $\pm$ 1 V of the onset potential from each experiment.

Based on this theory, we can eliminate several suspect compounds. Our original hypothesis of lithium intercalation is refuted here; by our measurements, lithium intercalation in graphene was at closest nearly 3 V off from the nearest onset potential, and nearly 2 V away from the closest bound of the potential range of the experiments. A relevant electrochemical phenomena referred to as the formation of the solid electrolyte interphase (SEI) in lithium-ion batteries is also shown to occur well outside of our experimental range[66]. Interestingly, the electrochemical stability window of the electrolyte, although not correlated with the onset potential in these experiments, was crossed by the Ag/Ag^+ metric during the course of this experiment; in fact, it was actually crossed during the conditioning sweeps of the experiment. However, the high stability of the reference potential during the conditioning sweeps suggests that oxidative degradation of the electrolyte is unlikely to be the culprit.

Of particular interest shown here is the equilibrium potential of the hydrogen evolution reaction (HER),

$$2\,H^+ + 2\,e^- \rightleftharpoons H_2 \tag{5.1}$$

which has (by estimation of the Nernst equation) been calculated to vary roughly in the region depicted in Figure 5.9. It can clearly be seen that this range operates very closely to the onset potentials of both experiments; however, before any sort of conclusion can be drawn, the changes to the graphene channel must be identified and compared to impacts

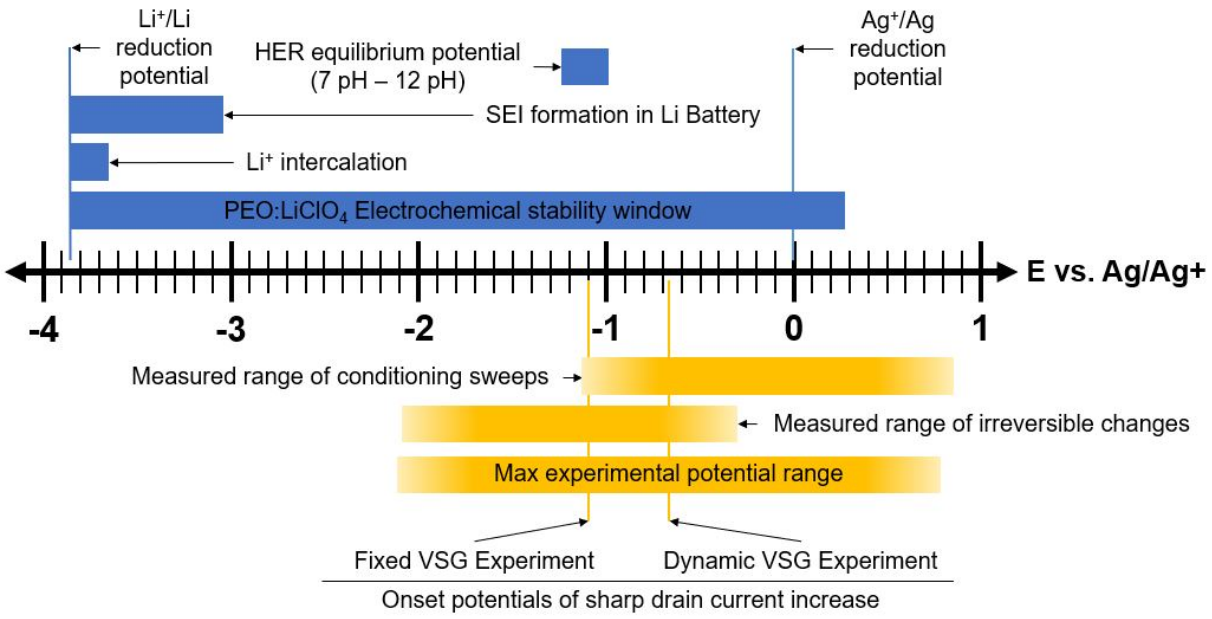


Figure 5.9: Relevant Electrochemical Potentials. Compilation of relevant experimental potentials (below number line, yellow) and relevant hypothetically related electrochemical potentials (above number line, blue) plotted with reference to Ag/Ag^+. Blue potential ranges are plotted exactly to appropriate Ag/Ag^+ ranges [64, 65, 33, 66]. Yellow potential ranges are plotted with $\pm$ 400 mV (indicated by dark-to-light gradient) to note the variation of onset potentials between experiments, as the reference electrode potentials may also vary.

on the channel by products or reactants of the hydrogen evolution reaction. Water, for example, can serve as the oxidation half-reaction for HER. Multiple reports demonstrate that the introduction of water to a graphene channel will decrease resistance of the channel as water is adsorbed on the graphene surface, resulting in an increase in I_D magnitude as we see in our experiments[67, 68]. However, these reports indicate resistance decreases on the order of 1-3%, while we see current increases of 30% and 400%, respectively, across the two FETs we studied. In addition, these reports show p-type doping of the channel with the introduction of water, which is contrary to the results we find in our work.

PMMA is a well known contaminant in many 2D FETs, as it is a very commonly used electron beam lithography resist in the fabrication process and notoriously difficult to remove completely[44, 45, 46]. One study breaks down the effects of PMMA on graphene FETs, attempting to anneal the devices to remove the PMMA, then reintroducing it and remeasuring the devices[47]. Chan et al. demonstrate that the removal of PMMA leads to an n-type doping of the device and an increase in conductivity. Although it is not addressed in the paper, some of the plotted data from Chan et al. suggests an increase in ON/OFF ratio upon the removal of PMMA as well. However, the electrochemical stability window of PMMA does not closely align with the onset potential from our experiments, as several groups report an electrochemical stability window for a PMMA based gel-polymer electrolyte of up to 4.9 V vs. Li/Li^+. This range completely envelopes the entire range of measured electrochemical potential of our experiments[69, 70, 71]. This demonstrates that, for PMMA to be the major contributor to the changes to the graphene channel, the potential of our quasi-reference electrodes would have to be at least 2 V more positive versus Ag/Ag^+ than currently assumed. By comparison to other Ag/Ag^+ reference electrodes with $LiClO_4$ as a supporting electrolyte[59], we expect that the reference electrode will vary from Ag/Ag^+ no more than 80 mV, so this seems unlikely.

Interference of the measurement by means of silver contamination is possible in this work, but unlikely. One recent study by Iqbal et al. has reported that the introduction of silver nanoparticles leads to n-type doping of graphene FETs as well as an increase in conductivity[72]. However, the increase in conductivity reported does not show an increase across all data points of the measurement V_{SG} window as shown in our work, nor do the

reports show consistent increases to the ON/OFF ratio as seen in our results. In addition, although the Ag/Ag^+ reduction potential was crossed during measurement, the crossing occurred as early as the conditioning portion of both experiments, reducing the likelihood of silver contamination causing the features observed as a result of the onset potentials. Future work to evaluate this possibility could do so by simply replicating this work without the presence of silver reference electrodes to investigate if the transfer characteristic changes were replicated.

All of the previously addressed reactions assume that a component or contaminant in the device is the reaction culprit, but it is possible that the electrochemical reaction could involve graphene itself. One example of this is the reduction of oxidized defects in the graphene channel. Graphene oxide is reported to reduce to graphene at -0.948 V versus Ag/Ag^+, lying between the onset potentials from both experiments[73]. It has also been demonstrated to increase in conductivity by an order of magnitude after reduction, similar to our results[74]. While it is unlikely that the I_D increase we observed was caused entirely by graphene oxide reduction (as we used graphene flakes and not graphene oxide flakes for our channels), it is quite likely that a similar reaction would have contributed to our observations.

Ultimately, this analysis does not not yield wholly conclusive evidence, nor is it able to do so without additional investigations. In fact, it is entirely possible that several of the compounds described here are impacting the graphene FET transfer characteristic changes simultaneously. What we are able to do conclusively is eliminate candidates as major contributors to the results we observed. In this manner, it is clear that our original hypothesis—that lithium intercalation in the graphene channel caused changes to the FET transfer characteristics seen at higher V_{SG}— is highly unlikely.

6.0 Conclusions and Future Work

Understanding the electrochemical reactions of EDL FETs is crucial for the development of the field and its future technologies. Knowledge of electrochemical action in EDL FETs may reveal interesting and useful chemistry for devices comprised of different channel materials and electrolytes. Some researchers already claim that observed increases in channel conductivity result from electrochemistry, yet use no analytical techniques to identify specific reactions at play[13, 14]. A more complete understanding of electrochemistry in these systems will allow us to develop the EDL FET field faster as a result of intentional design, as well to avoid the pitfalls of unintentional and interfering electrochemistry.

In the work presented here, the electrochemical potentials that we observed alongside lasting changes in FET transfer characteristics are inconsistent with lithium intercalation in graphene. This begs the question: what electrochemical reaction or reactions are happening in the devices? To answer this question more completely, more research is necessary. Future work in identifying electrochemical reactions in EDL FETs will most heavily rely on optimization of the reference electrode. Particularly, the noted difference of approximately 0.4 V between the onset potentials from each experiment calls the consistency of reference potentials between devices into question. A consistent onset potential between multiple devices is necessary to confirm if the same chemical reaction is occurring in each device, and, given that both of these devices were fabricated at the same time, from the same graphene exfoliation, on the same substrate, it is unlikely that the onset potentials measured result from two entirely different reactions. As discussed in Section 5.7, this suggests that the difference in onset potentials between devices is instead the result of variation between reference electrodes. In the same line of thought, I have two hypotheses for the difference between onset potentials observed in this work.

This first is that the varying positions of the gate, source, and drain electrodes relative to the reference electrodes resulted in different polarizations of the reference electrodes. Other researchers have shown that, in solid electrolyte cells, electrode geometric orientation and positioning (relative to other electrodes) can have result in polarization of reference

electrode[75, 76, 77]. In the same vein, it is possible that our reference electrodes are polarizing versus the gate, source, or drain electrodes, resulting in an inconsistent V_{Ref} between different devices due to their differing electrode layouts necessitated by graphene flake size and shape. We could explore this possibility by fabricating graphene EDL FETs from near-identical CVD-grown graphene channels[78], although it should be noted that these would introduce unique electrochemical features of their own[42, 43]. Such channels would allow the gate, source, drain, and reference electrodes to all be produced with identical positioning across multiple devices; whether the static V_{SG} window experiment produces similar onset potential data from device to device or not, we will know confidently if the electrode positioning impacted these results.

My second hypothesis regarding the difference in onset potentials between devices is that it results from a PEO:$LiClO_4$ deposition in which $LiClO_4$ concentration varies across grain boundaries in the solid polymer electrolyte. Quasi-reference electrodes are frequently sensitive to ion concentration[48, 49], so it would be unsurprising to observe this occurrence if there is in fact ion concentration variation across grain boundaries. By fabricating multiple devices close enough together to rely on the same reference electrode, we could maintain the exact same local chemical environment for the reference electrode. I believe EDL graphene FETs like those used in this work could likely fit within 500 µm apart with relatively little fabrication difficulty and still rely on the same reference electrode in between the devices. We could then replicated the fixed V_{SG} window measurement on the device pairs and compare the onset potentials in each device. If the onset potential varies between device pairs but not between paired devices, we will have demonstrated that varying ion concentration across grain boundaries of the electrolyte affects reference electrode potential.

However, fabricating a silver quasi-reference electrode in the EDL FET design is just the first step in developing this understanding. As mentioned in Section 4.1, silver has drawbacks[63] when implemented in FET devices, and it would be ideal to identify a reference electrode material that has similarly simple and familiar implementation. An ideal reference electrode material in this sense would lend itself to typical 2D FET fabrication techniques (e-beam lithography, metal deposition, etc.) and possess a resistance to electromigration. I have not yet identified a material that will fit this ideal, but I am interested in attempting

to implement lithium iron phosphate (LFP) with 2D crystal EDL FETs similar to its use in the work of Sharbati et al[18]. Although LFP is deposited as a film rather than a metal electrode, it has been shown to hold remarkable potential reproducibility ($\pm$ 3 mV) across multiple identical experiments. Depending on LFP's likelihood of ion contamination in PEO:$LiClO_4$ (which could be tested by replicating the fixed V_{SG} window experiment with an LFP reference electrode instead of a silver quasi-reference electrode and comparing the results to those shown in Figure 5.5 (b)), it may provide the best step forward for this work.

In regards to identifying the electrochemical reaction present in this study, I have found more evidence to refute possible reactions than to corroborate them. It is my belief that a sort of ill-defined electrochemical reaction (possibly a graphene defect being reduced, for example) is occurring in these samples, and, unless such a reaction is identified in other graphene research, I do not expect anyone else in the 2D EDL FET community to seek out the answer any time soon. In order to identify the reaction occurring in these (or new, similarly constructed devices), I propose to conduct in situ Raman measurements through the duration of the fixed V_{SG} window experiment. In situ Raman measurements may reveal chemical composition changes to corroborate reference electrode measurements and, when Raman, transfer characteristics, and reference potentials are compared across the onset potential, we will have a sense of the chemical changes occurring in the device before and after the onset potential. We could also use the Raman data from subsequent sweeps to observe the buildup of chemical changes that I expect to see due to the increasing I_D observed with each new sweep in the fixed V_{SG} window experiment. For example, Raman shifts have been observed as a result of the reduction of graphene oxide[79] that we could compare our results against. It is possible that the reactions we would seek to observe are occurring in different key locations along the device— at the Au contacts, in the bulk of the channel, or along the channel edges, particularly— so I would suggest targeting these locations. Previous research has shown that Raman can be performed on a working FET coated with PEO:$LiClO_4$[80, 81], so the measurement should be able to be taken during operation even in the presence of the solid polymer electrolyte.

Note that the onset potentials identified in this research are specific to this EDL FET system; that is, attempting the same measurements with devices made from a different chan-

nel material, a different electrolyte, or both, may result in different changes in the transfer characteristic at different onset potentials. This is because changing these components of the EDL FET fundamentally changes the reactants that are available to undergo irreversible electrochemical reactions. In order to identify and use (or avoid) the onset potential of any electrochemical reaction in an EDL FET, it will likely be necessary to identify onset potentials of reactions for each combination of channel material and electrolyte. Moreover, each new combination of reference electrode and electrolyte will require calibration with some known electrochemical potential.

A thorough understanding of how to execute electrochemical measurements of 2D EDL FETs will provide both the opportunity to discover interesting new material properties as well as the ability to better understand what happened to a device when things have gone wrong. Learning more about the chemistry of graphene or any other 2D crystal channel is an obvious benefit, but the ability to chemically alter a channel's chemistry will provide an all-new knob with which we can tune a device's properties even after fabrication. As an example, the increased conductivity and ON/OFF ratio observed in this work would benefit a device aiming for low-energy applications; it is likely that many application-centric device design principles could incorporate post-fabrication electrochemical preparation steps if only the electrochemistry in the devices were more completely understood. With a reference electrode integrated in EDL FET design, the research question eventually changes from "What exactly is driving the changes?" to "How can we use that information to design better EDL FETs?"

Appendix A Experimental Protocol and Conditions

The intention of this appendix is to provide a description of each step of the device fabrication and measurement methods with representative protocol. My hope and goal with these descriptions is (1) to provide a clear understanding of the various details of my efforts specific to the research detailed in this thesis, and (2) to create a useful reference for some of the basic methods I have used in my device research experience.

A.1 Si/SiO_2 Substrate Preparation

A 100 mm diameter, p-doped, $\langle 100 \rangle$ oriented silicon substrate with a 90 nm SiO_2 top-layer from University Wafer was diced into sample chips approximately 1 cm square. The chips were cleaned with a 10 second rinse in acetone followed immediately (before the acetone dried) with a 10 second rinse with isopropyl alcohol (IPA). The IPA was then immediately blown off with a N_2 gun. I have previously cleaned chips with a final step in deionized water, but I have not had any indication that the water has aided the removal of any contaminants and subsequently discontinued this practice.

The chips were then O_2 plasma cleaned with a South Bay Technology PC 2000 RF Plasma Cleaner to eliminate any remaining organic contaminants on the surface of the substrates. The specifications for the cleaning were as follows: power, 50 W; O_2 flow rate, 10 sccm; time, 1 minute; pressure, 200 mTorr. This process was not strictly necessary for these chips. The Fullerton lab has since developed a method for marker deposition that significantly reduces electron beam lithography time by depositing a less-dense marker field using a maskless aligner process; however, the maskless aligner process requires the substrate to be plasma cleaned due to its use of photoresist that does not remove easily with solvents. I included the plasma cleaning step with my sample chips with the expectation that, by the time the new method was developed, I would still need to exfoliate more graphene and wanted a consistently treated substrate. Ultimately, this was unnecessary.

A.2 Fabricating Sample Reference Electrode Pads for Open-Circuit Voltage Measurements

To observe the potential stability of silver in PEO:$LiClO_4$ solid polymer electrolyte, I fabricated pairs of 100 µm square silver pads at distances of 10 µm, 100 µm, and 1000 µm distances apart. I designed the pads in KLayout and used photolithography and metal deposition to fabricate them. For devices that can be fabricated with an approximately 1 µm resolution and can be either plasma cleaned post-fabrication or will not be significantly affected by contaminant photoresist, a maskless aligner (I used the Heidelberg MLA 100) offers a very fast lithographic step when compared to EBL or standard UV mask exposure methods. After the MLA step, I used a PLASSYS Electron Beam Evaporator MEB550S to deposit 5 nm of Ti followed by 150 nm of Ag. The purpose of the 150 nm thickness was to protect the pads from landing probes before measurement; the thickness can be reduced to as low as 100 nm or perhaps even 50 nm depending on the material, but the pad becomes much more susceptible to damage from probe landing as a result. After the fabrication of these pads, the deposition procedure from Section A.8 was followed to embed the silver pads in PEO:$LiClO_4$.

A.3 Open-Circuit Voltage Measurements on Sample Reference Electrodes and Conditioning

I have already noted that the open-circuit voltage measurements I attempted with silver pads in PEO:$LiClO_4$ were likely impacted by a feedback loop due to the measurement configuration. To be specific, each measurement was conducted with a probe landed on each of a pair of silver pads. Each of the probes was connected to a separate SMU channel, and each channel was designated to measure voltage versus ground for 60 seconds.

Following these measurements, I attempted to electrochemically condition the silver pads with the goal of building a robust layer of $AgClO_4$ salt on the surfaces of the pads. This was done by biasing the pads against each other in a square wave pattern centered about 0 V.

The idea was to drive reduction and oxidation reactions of Ag on each pad symmetrically with the expectation that the two pads would develop similar chemical environments and subsequently similar potentials. This conditioning process was attempted with pairs of pads, denoted here as Pad 1 and Pad 2. The voltage pulse cycle is outlined in Table A1 and was repeated for 10 cycles.

Table A1: Ag Pad Conditioning Attempt Cycle

Step	Pad 1	Pad 2	Time
1	0.5 V	0 V	10 s
2	-0.5 V	0 V	10 s
3	0 V	0.5 V	10 s
4	0 V	-0.5 V	10 s

A.4 Few-Layer Graphene Mechanical Exfoliation

We store the majority of our 2D crystal sources inside of an argon glovebox in order to reduce source contact with oxygen and water. From within the Ar glovebox, a small sample of graphene was removed from a source crystal with wafer dicing tape. The tape sample was removed from the glovebox via a petri dish, and another piece of 18074 tape was used to remove a small flake of the sample graphene.

This final sample tape was folded onto itself, with each fold contacting the opposing side of the tape and transplanting graphene from one side of the tape to the other. The process was repeated until the graphene was barely visible to the human eye on both sides of the sample tape, presenting itself as a cloud on the tape. The sample tape was then placed on a clean silcon chip (from Section A.1), and the back of the tape was gently rubbed with a pencil eraser. The tape was slowly removed from the substrate, leaving behind a field of exfoliated graphene flakes. There are many types of tapes that can be used for this process, and I have found that different tapes have different efficacies for different types of 2D crystals. Graphene, in particular, has shown good flake density yields from 18074 Blue Medium Adhesion standard dicing tape, and so I used this tape here.

The sample chip was placed under an optical microscope, and suitable flakes were identified by color approximation (see Figure A1). Typically, with this substrate, graphene flakes will show optical coloration changes related to their relative thicknesses (in terms of layers), and this can be used to approximate flake suitability for devices by coloration. I have found that nearly translucent gray flakes are 1 or 2 layers thick, gray flakes are 2 - 5 layers thick, and dark gray flakes are 5 - 10 layers thick. Approximate positions of gray and dark gray flakes of suitable length and width were noted.

Access time and cost limitations during electron beam lithography for marker field deposition (described in Section A.5) required that I identify the areas of the sample chip with the highest density of candidate channel flakes. As a part of the optical imaging process, I noted a general sense of where the graphene flakes were closest to each other. I limited the marker field to an approximately 4 mm square area, giving me the ability to capture about a quarter of my sample chip's surface area in a marker field that could be used to align electrode placement to a candidate channel.

A.5 Designing and Depositing Alignment Markers and Marker Field

A candidate channel crystal flake cannot accurately be fabricated into a device without some sort of alignment grid for the electron beam lithography (EBL) step. There are multiple

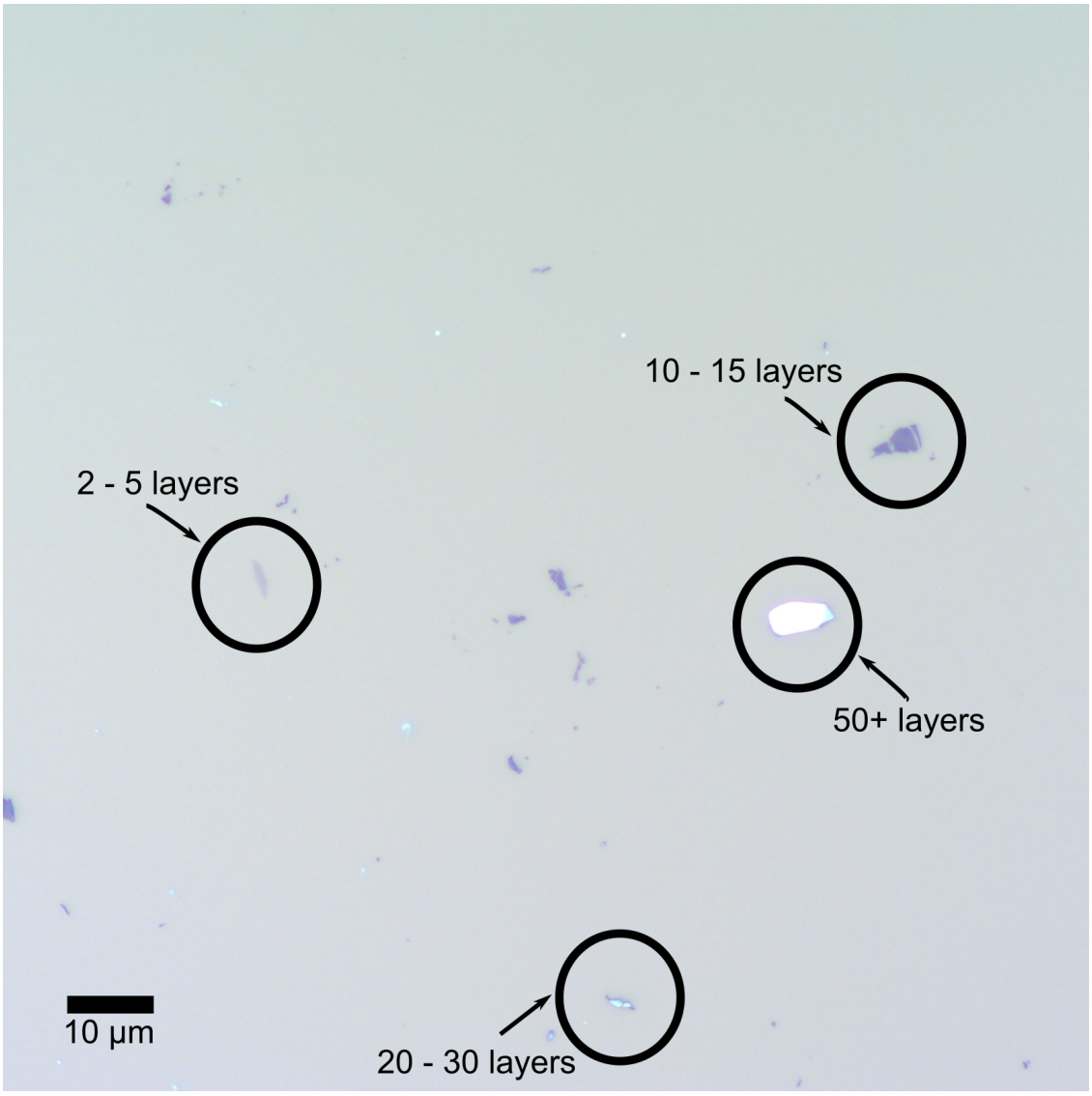


Figure A1: Estimating Graphene Flake Thicknesses. Shown is a 20x optical microscope image of graphene flakes mechanically exfoliated on Si/SiO_2 substrate. Circled in black are examples of graphene flakes and an estimation of their thicknesses based on coloration.

ways to do this, but the method I chose for this work— due to my familiarity and consistency of results— was to use EBL after flake exfoliation to make a field of markers for flake location and electrode design alignment. The sample chip was spin-coated with 950 PMMA A4 e-beam resist and annealed on a hotplate at 180 °C for 3 minutes in atmospheric conditions to ensure the resist held tightly to the sample. The sample chip was then loaded into a Raith e-LiNE (EBL) station. The coordinate placement of the alignment field was chosen to cover the region of the sample chip containing the highest number of suitable graphene flakes. The pattern was written with a beam dosage of $150\,\mu\mathrm{A\,s\,cm^{-2}}$.

After the writing step, the sample chip was removed from the EBL station and loaded into a PLASSYS Electron Beam Evaporation System. At 8×10^{-7} mbar, a 5 nm thick film of Ti was deposited to serve as an adhesion layer to the SiO_2 top-layer of the substrate. 45 nm of Au was then deposited to cap the field and alignment markers of the sample chip.

The sample chip was then removed from the evaporator and placed overnight in an acetone bath for liftoff. The following day, the chip was suspended in the acetone with a pair of tweezers while a micropipette was used to generate a gentle pressure in the acetone bath to remove or "lift off" the excess Ti/Au plating, leaving Ti/Au markers behind.

A.6 Designing and Depositing Gate, Source, Drain, and Reference Electrodes

The sample chip with its alignment marker field was viewed under an optical microscope, and optical images were taken at 20x zoom of each identified candidate graphene flake such that the centers of the surrounding four Au field markers were visible. These images were used with KLayout software to design contacting electrodes (the source and drain electrodes) overlaid across candidate graphene flakes such that the electrode ends were parallel to each other and crossed the entire flake across the flake's narrowest dimension (see Figure A2). The ends of each electrode were 10 µm long and 2 µm wide. 100 µm square pads (intended for landing probes during measurements) were positioned at distances of at least 150 µm away from the graphene flake, and the pad was connected to the electrode ends. During this design step, care was taken to avoid connecting the source and drain electrodes to each other (or, later, to the gate or reference electrodes) by graphene or a Au marker.

The gate electrodes were positioned such that the electrode ends were 3 µm away from the source and drain electrodes and on the opposite side of the channel unless markers or other graphene flakes forced the source or drain to be positioned on opposite sides of the channel. The gate electrode ends were designed to be as wide as the device channel and 2 µm long. Similarly to the source and drain electrodes, the gate electrode ends were connected to 100 µm square pads.

Following the same procedures from Section A.5 (with the exception of depositing 150 nm of Au instead of 45 nm), the gate, source, and drain electrodes were deposited. The devices were then re-imaged using the same optical microscope process described previously, and reference electrodes were designed for each device (see Figure A3). These electrodes were positioned equidistant from the source and drain, with similarly designed ends placed 10 µm from the channel. The reference electrodes were deposited in the same manner as the procedures described in Section A.5, except using Ag instead of Au.

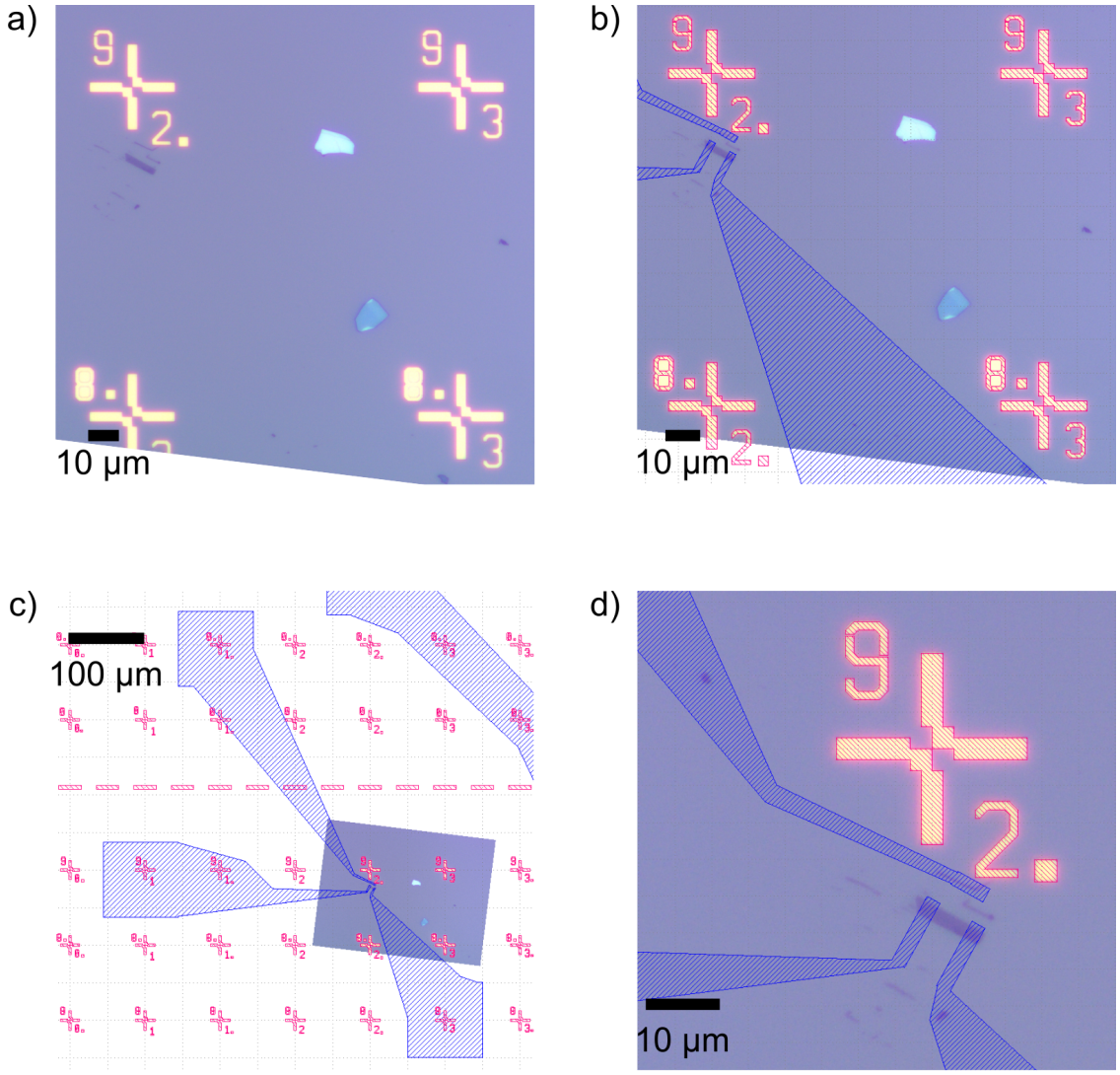


Figure A2: Laying Out Gate, Source, and Drain Electrodes for Graphene FET. Images demonstrating the electrode designing process for a single device. (a) Optical image of candidate channel flake with surrounding alignment markers. (b) KLayout overlay matching alignment markers to the coordinate system and showing electrodes designed around graphene flake. (c) KLayout overlay zoomed out to show electrode pad orientations and designs. (d) KLayout overlay zoomed in to show source and drain electrode positioning across graphene flake and gate electrode avoiding alignment marker.

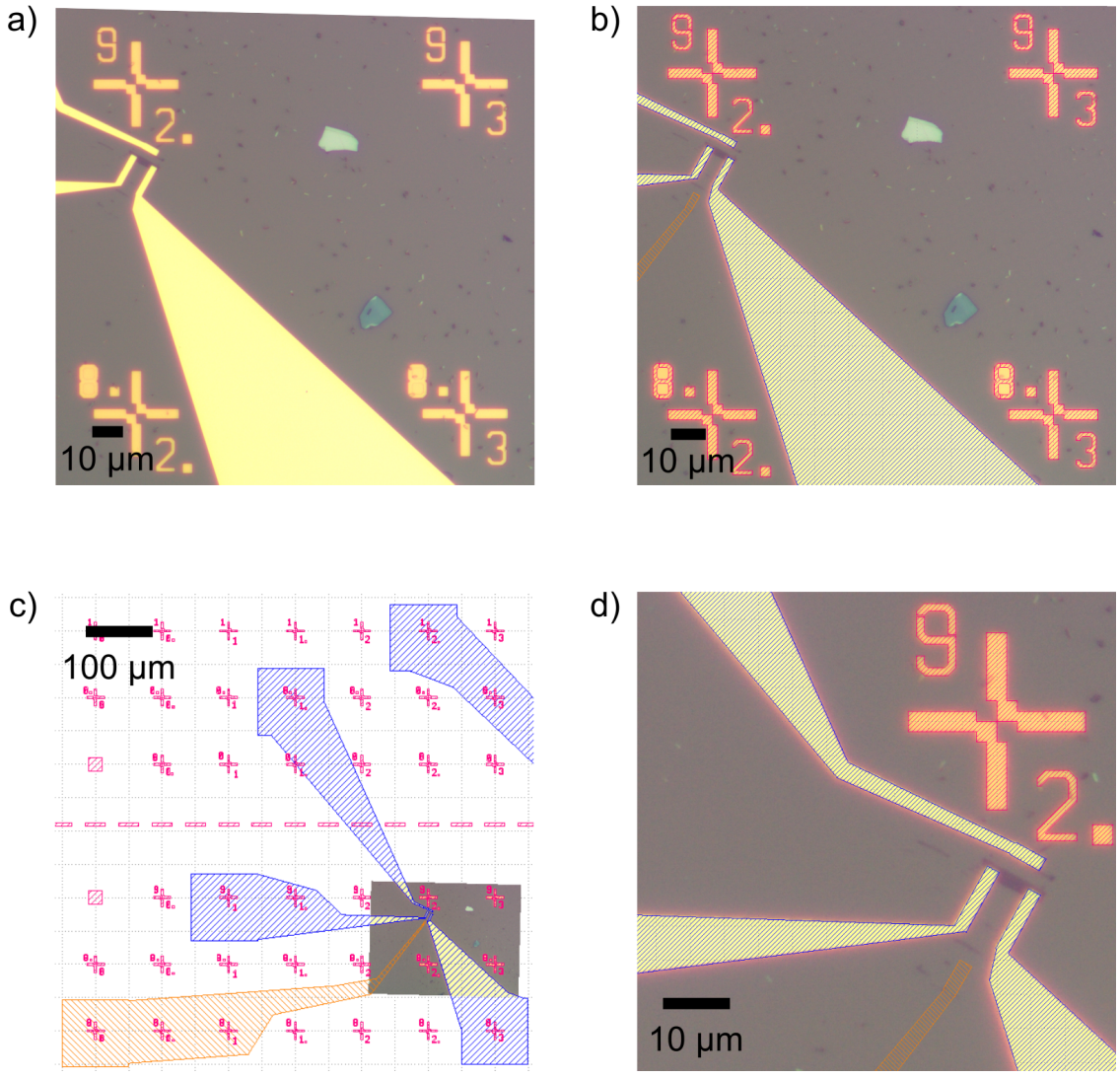


Figure A3: Laying Out Reference Electrode for Graphene FET. Images demonstrating the electrode designing process for a single device. (a) Optical image of graphene FET with surrounding alignment markers. (b) KLayout overlay matching alignment markers and gate, source, and drain electrodes to the coordinate system and showing reference electrode (in orange) electrode designed between source and drain electrodes. (c) KLayout overlay zoomed out to show electrode pad orientations and designs. (d) KLayout overlay zoomed in to show reference electrode end positioning between source and drain electrodes and distance from the graphene channel.

A.7 Preparing Device Sample Chip Inside Glovebox for Transport to Probe Station

Securing a sample chip to a probe station sample chuck from inside the glovebox requires some preparatory steps. The first of these is the preparation of Kapton tape slivers to secure the chip to the sample chuck. Kapton tape slivers were prepared by unrolling a section of 5 mm tape onto a desk surface and slicing approximately 2 - 3 mm wide slivers with a razor blade. The tape slivers are usually stuck on the inside surface of a small petri dish. I also frequently use a permanent marker to mark a large O on the outside surface of the petri dish bottom and a large X on the petri dish top. This allows the glovebox user to note, at a glance, if a selection of tape slivers is unused (from the O dish), and provides a receptacle for used and ready-to-be-disposed tape slivers (the X dish). The petri dish was then loaded into the glovebox. When ready to be measured, the sample chip was attached to the sample chuck with two tape slivers crossing the corners of the chip. The sample chip and chuck were then loaded into a LakeShore CRX-VF Probe Station via a transfer case and loadlock to eliminate atmospheric contamination.

A.8 Preparing and Depositing PEO:$LiClO_4$ Solution

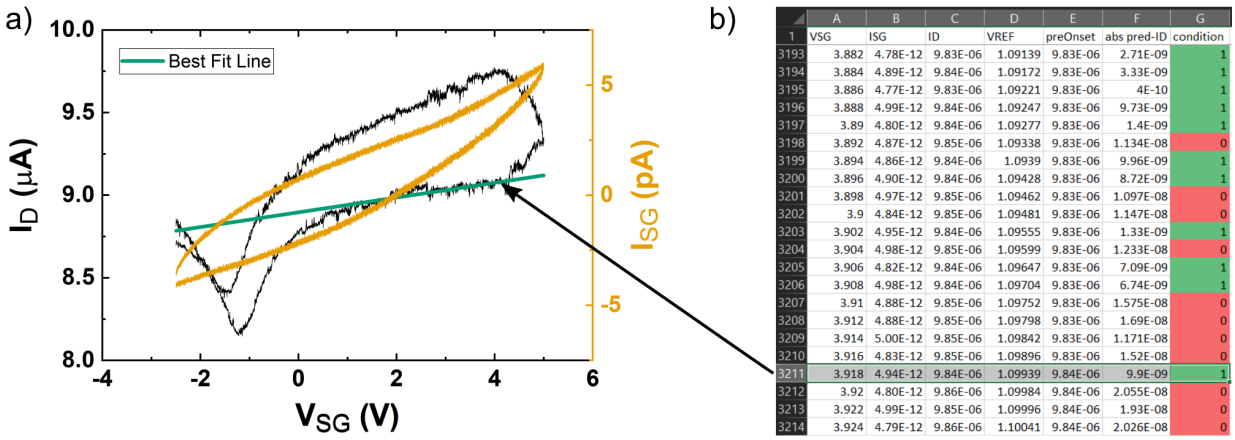
The goal was to prepare a 1 wt.% solution of PEO:$LiClO_4$ in acetonitrile (ACN) with a 20:1 ether oxygen to Li^+ ratio from within the Ar glovebox. Anecdotally, I have been told that this electrolyte can be tempermental during deposition outside of this weight percent and ether oxygen ratio combination, so I was willing to be flexible with the exactness of these values as long as the deposition (on a spare chip to test first) went smoothly. With perfect measurements, this would require 100 mg of PEO, 12.1 mg of $LiClO_4$, and 11.21 g of ACN. An example preparation proceeded as follows: using a Mettler Toledo 104 TS mass balance inside the argon glovebox, I tared a 100 mL vial, added 98.8 mg of PEO powder, tared the balance, added 12.7 mg of $LiClO_4$, and tared the balance once more to add 11.2176 g of ACN. This resulted in a 0.98 wt.% solution of PEO:$LiClO_4$ in ACN with an 18.8:1 ether

oxygen to Li^+ ratio. I would have considered making a new solution if the ether oxygen to Li^+ ratio were lower than 10:1.

To deposit the electrolyte on the sample inside of the Ar glovebox, the Si substrate was placed on a room temperature hot plate and 35 µL of the polymer electrolyte were dropcasted on the surface of the chip with a micropipette. The ACN was allowed to evaporate from the chip for 10 minutes before the chip was removed from the hot plate; then the hot plate was set to 80 °C, allowed to come to temperature, and the chip was replaced on the hot plate for 3 minutes of annealing. Samples prepared in this manner were transferred to the probe station via a hermetically-sealed transfer case and a vacuum-enabled load-lock to prevent atmospheric exposure before and during measurement.

A.9 Onset Potential Identification Protocol

The onset potentials from the dynamic and fixed V_{SG} window experiments can be evaluated qualitatively, but to quantify their values, I created a methodology for pinpointing the onset potential data point (see Figure A4). I first used OriginPro data analysis and plotting software to make a line of best fit of the region of the data after the Dirac point and before the onset potential in the forward sweep. I took the absolute value of the difference between each experimental data point and its predicted value from the line of best fit. Naturally, since the line of best fit was targeted for the linear region of each sweep between the Dirac point and the onset potential in the forward sweep, the value of this metric was highest before the linear region and after the onset potential. Using Microsoft Excel, I then parsed the data for the first data point at which the difference was less than 10 nA and was followed by at least 1000 data points at which the difference was greater than 10 nA. This condition is how I have defined onset potential in this system. In the example in Figure A4, the onset potential is 3.918 V.



	A	B	C	D	E	F	G
1	VSG	ISG	ID	VREF	preOnset	abs pred-ID	condition
3193	3.882	4.78E-12	9.83E-06	1.09139	9.83E-06	2.71E-09	1
3194	3.884	4.89E-12	9.84E-06	1.09172	9.83E-06	3.33E-09	1
3195	3.886	4.77E-12	9.83E-06	1.09221	9.83E-06	4E-10	1
3196	3.888	4.99E-12	9.84E-06	1.09247	9.83E-06	9.73E-09	1
3197	3.89	4.80E-12	9.84E-06	1.09277	9.83E-06	1.4E-09	1
3198	3.892	4.87E-12	9.85E-06	1.09338	9.83E-06	1.134E-08	0
3199	3.894	4.86E-12	9.84E-06	1.0939	9.83E-06	9.96E-09	1
3200	3.896	4.90E-12	9.84E-06	1.09428	9.83E-06	8.72E-09	1
3201	3.898	4.97E-12	9.85E-06	1.09462	9.83E-06	1.097E-08	0
3202	3.9	4.84E-12	9.85E-06	1.09481	9.83E-06	1.147E-08	0
3203	3.902	4.95E-12	9.84E-06	1.09555	9.83E-06	1.33E-09	1
3204	3.904	4.98E-12	9.85E-06	1.09599	9.83E-06	1.233E-08	0
3205	3.906	4.82E-12	9.84E-06	1.09647	9.83E-06	7.09E-09	1
3206	3.908	4.98E-12	9.84E-06	1.09704	9.83E-06	6.74E-09	1
3207	3.91	4.88E-12	9.85E-06	1.09752	9.83E-06	1.575E-08	0
3208	3.912	4.88E-12	9.85E-06	1.09798	9.83E-06	1.69E-08	0
3209	3.914	5.00E-12	9.85E-06	1.09842	9.83E-06	1.171E-08	0
3210	3.916	4.83E-12	9.85E-06	1.09896	9.83E-06	1.52E-08	0
3211	3.918	4.94E-12	9.84E-06	1.09939	9.84E-06	9.9E-09	1
3212	3.92	4.80E-12	9.86E-06	1.09984	9.84E-06	2.055E-08	0
3213	3.922	4.99E-12	9.85E-06	1.09996	9.84E-06	1.93E-08	0
3214	3.924	4.79E-12	9.86E-06	1.10041	9.84E-06	2.026E-08	0

Figure A4: Process for Identifying the Onset Potential. (a) A depiction of the line-fitting of the region between the Dirac point and onset potential of Sweep 7 from the dynamic V_{SG} window experiment. The line was fit from 1.5 V V_{SG} to 2.5 V V_{SG}. (b) Screenshot from the Excel spreadsheet used to identify the onset potential. Column E contains the data point values predicted by the line of best fit in the region before the onset potential. Column F contains the absolute value of the data point values predicted by the line of best fit (Column E) minus the measured values from the drain current (Column C). Data point 3211 is the first point to satisfy the condition that this difference is $\leq$ 10 nA and is followed by at least 1000 data points for which the difference is $\geq$ 10 nA. This condition is how I have defined onset potential.

A.10 Nernst Equation Estimation for Hydrogen Evolution Reaction in this System

In Figure 5.9, I used a calculated range for the Hydrogen Evolution Reaction (HER). This value was estimated for the EDL FET system under vacuum during measurement and following the Nernst equation,

$$\mathrm{E} = \mathrm{E}^0 - \left(\frac{RT}{2F}\right) \ln\left(\frac{[\mathrm{H_2}]}{[\mathrm{H^+}]^2}\right) \tag{A.1}$$

The values were taken as follows:

$\mathrm{E}^0 = 0$ V vs. RHE

$\mathrm{T} = 298.15$ K

$\mathrm{R} = 8.314\,\mathrm{J\,K^{-1}\,mol^{-1}}$

$\mathrm{F} = 96\,485.33\,\mathrm{C\,mol^{-1}}$

$[\mathrm{H_2}] \approx \frac{P_{H_2}}{P_{H_2,\mathrm{ref}}} = \frac{8 \times 10^{-7}\,\mathrm{Torr}}{760\,\mathrm{Torr}}$ where 8×10^{-7} Torr is the pressure in vacuum chamber

$[\mathrm{H^+}] = 10^{-7}$ for 7 pH, 10^{-12} for 12 pH

The $\mathrm{H_2}$ concentration is approximated by the assumption that, by generating $\mathrm{H_2}$, the background $\mathrm{H_2}$ pressure will very quickly approach the background pressure of the instrument vacuum. The pH range shown here is roughly estimated as the range for the steady-state local concentration of protons under continuous HER conditions.

Appendix B Paper Insert

ACS APPLIED MATERIALS & INTERFACES

Research Article

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Electric Double-Layer Gating of Two-Dimensional Field-Effect Transistors Using a Single-Ion Conductor

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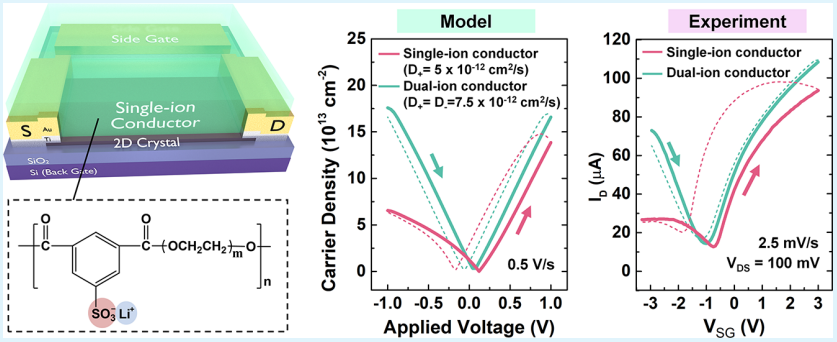
Supporting Information



ABSTRACT: Electric double-layer (EDL) gating using a custom-synthesized polyester single-ion conductor (PE400-Li) is demonstrated on two-dimensional (2D) crystals for the first time. The electronic properties of graphene and $MoTe_2$ field-effect transistors (FETs) gated with the single-ion conductor are directly compared to a poly(ethylene oxide) dual-ion conductor ($PEO:CsClO_4$). The anions in the single-ion conductor are covalently bound to the backbone of the polymer, leaving only the cations free to form an EDL at the negative electrode and a corresponding cationic depletion layer at the positive electrode. Because the cations are mobile in both the single- and dual-ion conductors, a similar enhancement of the n-branch is observed in both graphene and $MoTe_2$. Specifically, the single-ion conductor decreases the subthreshold swing in the n-branch of the bare $MoTe_2$ FET from 5000 to 250 mV/dec and increases the current density and on/off ratio by two orders of magnitude. However, the single-ion conductor suppressed the p-branch in both the graphene and the $MoTe_2$ FETs, and finite element modeling of ion transport shows that this result is unique to single-ion conductor gating in combination with an asymmetric gate/channel geometry. Both the experiments and modeling suggest that single-ion conductor-gated FETs can achieve sheet densities up to 10^{14} cm^{-2}, which corresponds to a charge density that would theoretically be sufficient to induce several percent strain in monolayer 2D crystals and potentially induce a semiconductor-to-metal phase transition in $MoTe_2$.

KEYWORDS: *electric double layer, ion gating, two-dimensional, single-ion conductor, field-effect transistor, EDLT, iontronics*

INTRODUCTION

Similar to conventional semiconductor materials such as silicon,[1,2] the electrical and optical properties of two-dimensional (2D) crystals can be strongly influenced by strain. For example, strain can transform 2D semiconductors from indirect to direct band gap materials with enhanced radiative efficiencies[3] or tune the emission wavelength of the 2D crystals.[4,5] In addition, monolayer 2D transition-metal dichalcogenides (TMDs) such as Mo- and W-dichalcogenide van der Waals crystals are predicted to undergo a complete phase change from the semiconducting 2H phase to the metallic 1T′ under strain.[6,7] Experimentally, phase transitions in $MoTe_2$ have been demonstrated by inducing local strain using an atomic force microscope (AFM) tip[8] and more recently, by inducing global strain via an electric field applied to a ferroelectric substrate in contact with $MoTe_2$.[9] Dynamically tuning the band gap in 2D crystals is not only fundamentally interesting but could be useful for applications such as low-voltage transistors[10−12] and flexible electronics.[13,14] For these applications, it would be desirable to create a gate dielectric that can be deposited at low temperatures, achieve large gate capacitance (e.g., 1−4 $\mu F/cm^2$),[15,16] and induce strain locally via field effect.

To address this need, we propose a new concept: a single-ion conductor electric double-layer transistor (EDLT) based on 2D crystals. Our approach is unique compared with EDL gating with dual-ion conductors (i.e., those with mobile cations and anions), which are commonly used for electronic and

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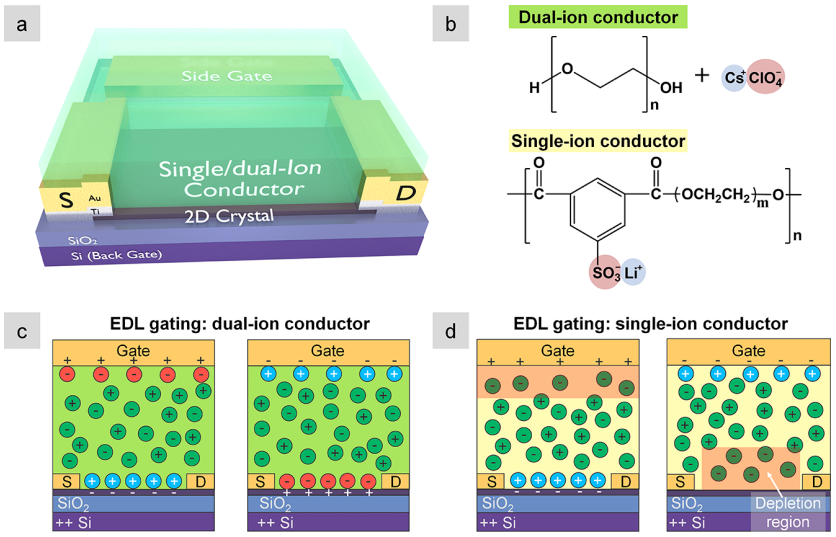

Figure 1. (a) Schematic of a 2D crystal FET (either graphene or $MoTe_2$) that can be operated by using a back gate or a single/dual-ion conductor using a metal side gate. (b) Chemical structures of the dual- and single-ion conductors: PEO:$CsClO_4$ (top row) and the ionically functionalized polyester (PE400-Li) (bottom row), respectively. Anions are shaded in red and cations are shaded in blue. Schematics of the (c) dual-ion conducting and (d) single-ion conducting FETs under two polarities. In the single-ion case, only cations are mobile while the anions are bound to the polymer backbone and therefore fixed. This immobility leads to cationic depletion regions (shaded in pink) at either the gate/single-ion conductor ($V_G > 0$) or single-ion conductor/semiconductor interface ($V_G < 0$), depending on the polarity of the applied field.

optoelectronic device studies.[17−21] Moreover, a wide variety of EDLTs have been demonstrated on 2D crystals.[15,16,22−25] Dual-ion conductors can induce charge densities on the order of ~10^{14} cm^{-2} for electrons and holes.[26,27] This corresponds to a capacitance density up to 10 $\mu F/cm^2$ and a large electric field strength of ~V/nm at the interface, allowing access to regimes of transport in semiconductors that cannot be achieved with conventional gate dielectrics.[25,28,29] In contrast to a dual-ion conductor, the anions of a single-ion conductor, or ionomer, are covalently bound to the backbone of the polymer, leaving only the cations free to move in response to an applied field. When polarized, an EDL consisting of densely packed cations is created at the negative electrode, but there is no corresponding anionic EDL at the positive electrode. In response to this imbalance, one side of the single-ion conductor (near the negative electrode) undergoes longitudinal expansion. The mechanism to induce strain using single-ion conductors has been well investigated for ionic polymer metal composites (IPMCs), which are useful for biomimetic actuators and artificial muscles.[30] In electronics, single-ion conductors have been used previously to gate organic transistors[31−33] where the motivation for immobilizing one ion over the other was to avoid electrochemical reactions within the organic channel. To our knowledge, there has been no report directly comparing single- and dual-ion conductors with similar chemistries in the same 2D crystal FETs or distinguishing the electrostatic gating effects between cationic EDLs and cationic depletion layers on 2D crystals.

We present the first demonstration of a single-ion conductor multilayer 2D crystal EDLT and lay the groundwork for demonstrating flexible 2D FETs with new functionalities induced by an EDL via strain. Experimentally, we used an ionically functionalized polyester (created via the condensation of poly(ethylene glycol) oligomers with dimethyl 5-sulfoisophthalate salt[34]) to electrostatically gate both graphene and $MoTe_2$ FETs. Compared with back gating through SiO_2, transfer characteristics using a side gate to control the location of the ions within both the single- and dual-ion conductors reveal a comparable enhancement of the n-branch current (e.g., 20-fold improvement of subthreshold swing and two orders of magnitude increase in on/off for $MoTe_2$ FETs). The dual-ion conductor gating results agree well with previous reports.[16,25,26,35] However, unlike the dual-ion conductor, the single-ion conductor quenches the p-branch in graphene and $MoTe_2$ FETs, which has not been reported before. Finite element modeling of ion transport in response to an applied field shows that the p-branch quenching is unique to single-ion conductor gating via the formation of a cationic depletion region (as opposed to an anionic EDL) in combination with an asymmetric gate/channel geometry. Both the experiments and modeling suggest that single-ion conductor-gated FETs can achieve sheet densities up to 10^{14} cm^{-2}, which could possibly induce sufficient strain to access the strain-induced electronic and optoelectronic properties described above.[36,37]

RESULTS AND DISCUSSION

The EDL-gated multilayer 2D crystal FETs use a side-gate geometry, as shown in Figure 1a. Graphene and $MoTe_2$ were mechanically exfoliated onto a p-doped Si substrate with 90 nm SiO_2 (used as a back gate). The source/drain and gate contacts (Ti/Au) were patterned by electron beam lithography (EBL) with the side gate located 10 μm away from the channel. The solid-state single-ion conductor is poly(ethylene glycol benzene-1,3-dicarboxylate-5-sulfoisophthalate lithium), abbreviated as PE400-Li, and the solid-state dual-ion conductor is poly(ethylene oxide), abbreviated as (PEO):C-sClO_4. The chemical structures of the dual- and single-ion conductors are similar and shown in Figure 1b. The PE400-Li is a polyester with each repeat unit consisting of the ionic group, namely, dicarboxylic 5-sulfoisophthalate, and a spacer of poly(ethylene glycol) 400, which provides the same repeat unit as PEO.[34] Unlike PEO:$CsClO_4$ where the anion, ClO_4^-, is free to respond to the applied field, the negatively charged functional group (SO_3^-) in PE400-Li is covalently bound to

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the polymer backbone, while the cation Li^+ is free to move under an applied field. The ether oxygen to cation molar ratios are 76:1 for the dual-ion conductors and 9:1 for the single-ion conductors. Differential scanning calorimetry (DSC) shows that the single-ion conductor has a markedly higher glass transition temperature (T_g = 14.5 °C) than the PEO:$CsClO_4$ electrolyte (T_g = −31.5 °C) (Figure S1, Supporting Information), which is consistent with the single-ion conductor having a larger salt concentration.[38] This difference in T_g suggests that the single-ion conductor will have lower ionic conductivity than the dual-ion conductor.

When no voltage is applied, cations and anions are homogeneously distributed throughout the electrolyte for both the single- or dual-ion conductors. The steady-state locations of cations and anions under $V_G > 0$ and $V_G < 0$ are illustrated in Figure 1c,d for the dual-ion conductor and single-ion conductor, respectively. When a positive gate bias is applied to a dual-ion conductor (Figure 1c, left), cations (Cs^+) are driven to the channel where they induce image charges (in this case, image charges are electrons) forming a cationic EDL at the channel/electrolyte interface. An analogous anionic EDL will form as anions (ClO_4^-) accumulating at the electrolyte/gate interface. When the polarity of the applied bias is reversed, an anionic EDL forms at the channel and a cationic EDL forms at the gate (Figure 1c, right).

For a single-ion conductor, shown in Figure 1d, a positive gate bias does not result in an anionic EDL at the gate/electrolyte interface; instead, there exists a cationic depletion layer (Figure 1d, left). When the polarity is reversed, the cation depletion layer forms at the channel/electrolyte interface (Figure 1d, right). Crucially, the negative charge stored by anions in the cationic depletion layer equals the positive charge in the cationic EDL, while the volumetric charge density of anions in the depletion layer is fixed and smaller than the volumetric charge density of the closely packed cations in the EDL. Thus, the depletion layer requires larger thickness (or volume when considered in 3D) than the EDL to store the same amount of charge. The presence of such a thick depletion layer also suggests that the device geometry will affect the interface capacitance of devices gated by the single-ion conductor because the depletion layer thicknesses will depend on the areas of both channel and gate. In contrast, the EDL thickness is always the distance between the ion and channel surface (i.e., <1 nm) and is independent of the channel size. Nonetheless, a depletion layer, albeit significantly thicker than the EDL, will still serve as a capacitor just with a smaller capacitance density than the EDL.[31]

To understand how the ion and voltage distributions differ under an applied voltage in a single-ion conductor compared to a dual-ion conductor and how their distributions will change with respect to the device geometry, we modeled ion transport using finite element analysis via COMSOL Multiphysics. A modified Nernst−Planck−Poisson system of equations[39,40] was solved for both single-ion and dual-ion conductors in two parallel plate capacitor geometries: one with electrodes of equivalent sized and another where one electrode is 10 times larger than the other (i.e., modeling the FET scenario where the channel is smaller than the gate). Figure 2 shows the resulting steady-state voltage distributions for applied voltages of equal and opposite polarities; the voltage is applied to the right electrode with the left electrode grounded. We first consider the scenarios where the electrodes have equivalent size (Figure 2a,b). In the case of a dual-ion conductor, anions and cations accumulate adjacent to their respective electrodes, producing EDLs of equal charge and thickness. The result is a symmetric voltage profile across the thickness of the capacitor where half of the applied voltage drops on each EDL regardless of the voltage polarity (Figure 2a), and the voltage drop through the bulk of the electrolyte is nearly zero.

In the case of the single-ion conductor, the majority of the voltage always drops across the depletion layer, regardless of polarity. The voltage drop is approximately 3 times larger across the depletion layer than the EDL, and the depletion layer is also approximately 3 times thicker than the EDL (Figure 2b). This result is sensible when considering conservation of charge across the parallel plate capacitor. Charge (Q) is expressed as $Q = V_{int}C_{int} = V_{int}\varepsilon_0\varepsilon_r\frac{A}{d}$, where V_{int} is the voltage across the interface, C_{int} is the interface capacitance, A is the area of channel, and d is the thickness of the interface capacitive layer (i.e., thickness of EDL or the depletion layers). Thus, the thicker depletion layer has lower interface capacitance and therefore requires a larger voltage drop to balance the charge.

For the scenario of equal sized electrodes discussed above, the voltage distribution across the single-ion conductor differs from the dual-ion conductor because the depletion region in a single-ion conductor requires the majority of the voltage drop. However, when the electrodes are unequal in length, similar to what would exist between the channel and the gate in a side-gated EDLT geometry, the voltage profiles between the single- and dual-ion conductors are remarkably similar because the geometry induces the majority of the voltage drop. Specifically, the length of the left (grounded) electrode decreased to one-tenth of the right electrode, and for the dual-ion conductor, 90% of the voltage drop across the EDL occurs adjacent to the shorter electrode, regardless of the voltage polarity (Figure 2c). The asymmetric voltage drop again results from charge conservation: the shorter electrode requires a larger voltage drop to compensate for its smaller capacitance.

In the case of the single-ion conductor (Figure 2d), the majority of voltage drop is also adjacent to the shorter electrode for the reason mentioned above, but the details of the ion and voltage distributions are more complicated. For $V > 0$ applied to the longer electrode, ∼85% of the voltage drop is distributed across the ∼0.5 nm-thick cationic EDL at the shorter electrode. When the polarity is reversed to $V < 0$, almost all of the applied voltage (97%) falls within the ∼1.5 nm-thick depletion layer near the shorter electrode (Figure 2d). This result is significantly different from Figure 2b where the electrode sizes are equal. To understand this difference, we focus on the voltage distributions near the grounded electrode only because the shorter grounded electrode is similar to the channel in the transfer measurements where $V_S = 0$ V and $V_{DS} \ll V_{GS}$ (see parts 2 and 6 in the Supporting Information). Focusing on the inset of Figure 2d, the depletion layer is ∼3 times thicker than the EDL even though the voltage drop is only 14% larger. This occurs because the grounded electrode is 10 times smaller and requires the majority of the potential drop regardless of the polarity of V. Even though the depletion layer thickness is 3 times larger, it is not possible for this layer to have 3 times larger potential drop than the EDL at the same electrode, and therefore, the charge at the grounded electrode will be lower for $V < 0$ compared to $V > 0$. This result suggests that the single-ion conductor in a side-gated EDLT geometry will exhibit weaker p-type doping compared to n-type doping.

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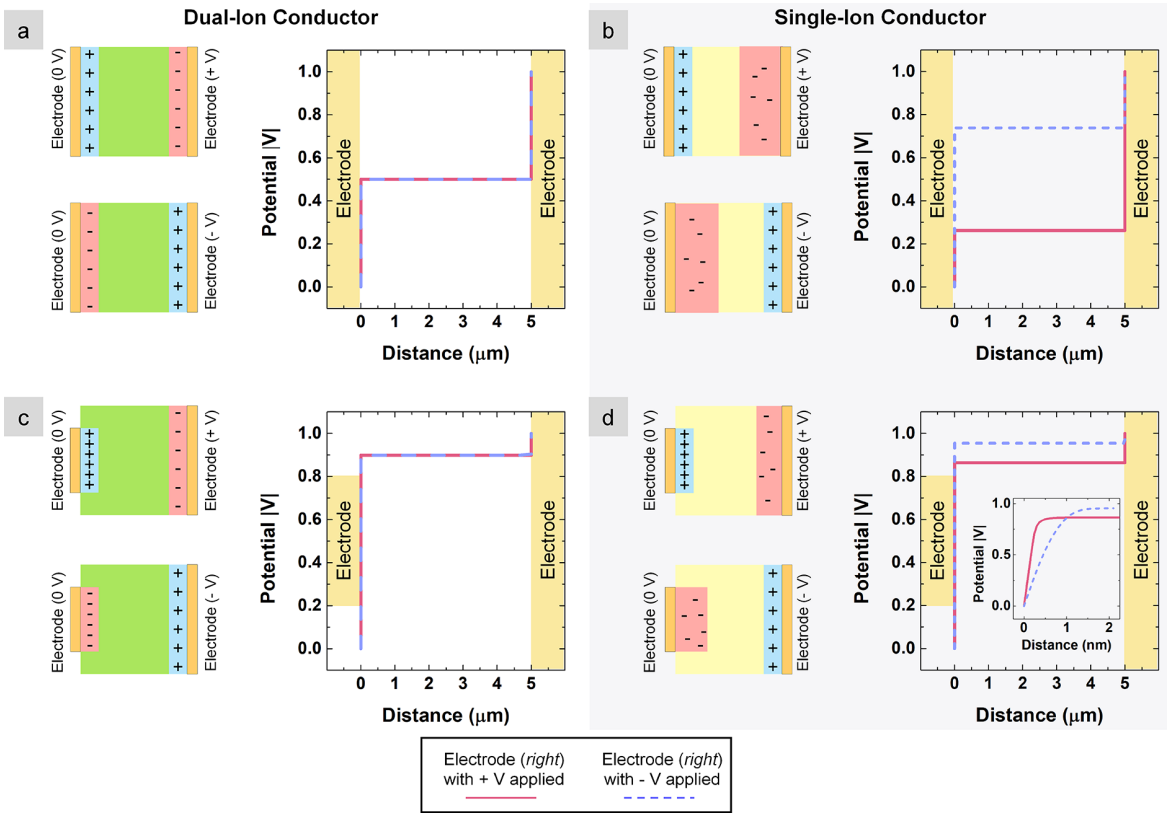

Figure 2. Steady-state voltage distributions from COMSOL Multiphysics and the corresponding device schematics showing ion positions for both (a, c) dual-ion and (b, d) single-ion conductors in two parallel plate capacitor geometries: electrodes of equal size (upper row) and electrodes of unequal size where the right electrode is 10 times larger than left (bottom row). Note that the schematics are not drawn to scale. Either ±1 V is applied on the right-side electrode. Cation and anion layers are highlighted in blue and red, respectively. The anion EDL (dual-ion) or cationic depletion layer (single-ion) thickness differences are illustrated qualitatively. Specifically, for the dual-ion conductor, the anionic EDL layer thickness is similar to the cationic EDL layer thickness; while for the single-ion conductor, the cationic depletion layer thickness is larger and influenced by the electrode size. The steady-state potential distributions under positive and negative voltages are highlighted in the red solid and dashed blue lines, respectively.

To test these predictions experimentally, we chose graphene as the first 2D material for two reasons. First, because it is a semi-metal, graphene is highly conductive and ambipolar with an intrinsic charge neutrality point at zero gate voltage, making it ideal for sensing both p- and n-type changes in conductivity. Second, EDL gating of graphene FETs using a dual-ion conductor has been widely demonstrated,[26,35] making it straightforward to benchmark against previously published results.

Graphene FETs with side gate geometry were fabricated by EBL as depicted above in Figure 1a. After device fabrication and before the single-ion conductor deposition, the channel surface was cleaned using an AFM in contact mode to remove e-beam resist residue.[41] Preparing a residue-free surface is essential to achieve the maximum gating effect because the EDL forms within a few nanometers of the surface, similar to the typical thickness of the EBL residue.[41] Figure 3a shows the AFM images of a graphene device after AFM cleaning. The root mean square roughness (R_q) of the channel surface was reduced from ∼1.30 nm before cleaning to ∼0.37 nm after cleaning, which is close to the reported value for freshly exfoliated graphene on SiO_2 (∼0.32 nm).[42] Note that all R_q are reported for a 400 × 400 nm area. The line scan indicates a flake thickness of 1.5 nm, corresponding to ∼5 layers of graphene.

The transfer characteristics of the graphene FETs (without electrolyte) were first measured with a back gate (Figure 3b, blue line), and the devices show a Dirac point around V_{BG} = 0 V, suggesting that there is negligible intrinsic doping in the exfoliated flakes. Under V_{DS} = 100 mV, the transfer curve exhibits highly symmetric n- and p-branches with a current maxima of ∼100 μA (25.4 μA/μm) at $|V_{BG}|$ = 30 V. The output characteristics of the bare graphene FET (Figure 3c, blue lines) also indicate that I_D is a linear function of V_{DS}, suggesting good ohmic contact at the source/drain terminals. These results on the bare graphene FETs are in good agreement with prior reports.[35,43,44]

After deposition of the single-ion conductor, the transfer and output measurements were repeated with EDL gating using the side gate 10 μm away from the channel. A sweep rate of 2.5 mV/s was used, which is 2000 times slower than that of the bare FET to allow sufficient time for the ions to respond to the field. This relatively slow sweep rate is consistent with the high T_g of the single-ion conductor that reflects slow ion mobility. Compared to the bare FET, the maximum I_D increased in the n-branch (V_{SG} > 0 V) by 50% to ∼152 μA at V_{SG} = 3 V. The increased current is expected for the EDL gating because of the large interfacial capacitance (1−4 μF/cm^2) induced by EDLs.[15,16] However, unlike conventional EDL gating with dual-ion conductors where the current is enhanced in both the

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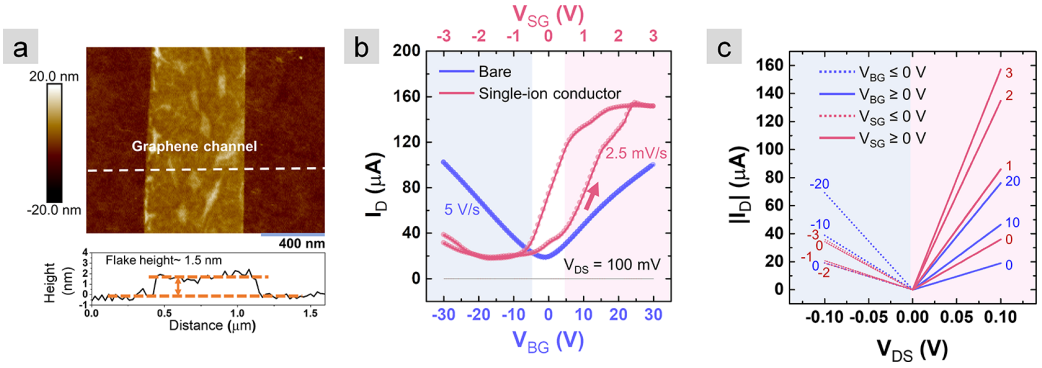

Figure 3. (a) AFM topography scan of a bare graphene FET channel (before electrolyte deposition). The location of the line scan is indicated by the white dashed line. (b) Transfer characteristics of the graphene FET: the blue data corresponds to the back-gated measurement of a bare FET while the red corresponds to a side-gated measurement on the same FET with the single-ion conductor. (c) Output characteristics of the back-gated (blue) and side-grated (red) graphene FETs.

n- and p-branches of an ambipolar FET, the single-ion conductor-gated FET shows a suppressed p-branch (V_{SG} < 0 V). The maximum I_D for the p-branch decreased by 65% to ~35 μA at V_{SG} = −3 V. This observation agrees well with the predictions from Figure 2d. The channel current, $I_D = \mu\varepsilon_0\varepsilon_r\frac{A}{d}(V_{int} - V_T)\frac{W}{L}V_{DS}$, where V_{int} is the interface voltage, d is the interface capacitive layer thickness, and $A/W/L$ is the area/width/length of the channel. When V_G is negative (corresponding to the p-branch), the depletion layer thickness next to the channel is expected to be much larger than the EDL thickness next to the channel when V_G is positive (corresponding to the n-branch). However, we learned from Figure 2d that the voltage drop across the depletion layer at the short electrode (i.e., channel) is only slightly larger than that across the EDL; thus, the channel current should be lower in the p-branch than in the n-branch.

Output characteristics as a function of side gate voltages are shown in Figure 3c (red lines). Compared with the back-gated data, the maximum I_D under positive (negative) side gate voltages are higher (lower), which is congruent with the transfer characteristics. Note that the results shown in Figure 3c are double sweeps, including the single-ion conductor-gated results, and the overlap of the forward and reverse sweeps indicates that the single-ion conductor gating is stable at each measured gate voltage, as long as adequate time is provided for the ions to respond to the field.

Thus far, the electrical characteristics of the single-ion conductor-gated FETs qualitatively agree with our predictions; however, it is essential to benchmark the single-ion conductor gating performance against a commonly used dual-ion conductor. To do this, we removed the single-ion conductor by solvent washing (dimethylformamide, DMF) and AFM cleaning. After the two-step cleaning process, the root mean square roughness (R_q) of the graphene channel is close to the value of freshly exfoliated flakes (Supporting Information, Figure S8).[42] Then, we redeposited a dual-ion polymer electrolyte, PEO:$CsClO_4$, on the same device and repeated the transfer measurements. Figure 4 shows the transfer curves for two such FETs (device 1 and 2) with (1) Si/SiO_2 back gate (no electrolyte), (2) EDL side gate using the single-ion conductor, and (3) EDL side gate using the dual-ion polymer electrolyte, PEO:$CsClO_4$. The solid lines correspond to the forward sweeps, and the dashed lines correspond to the reverse sweeps. For the transfer curves obtained using PEO:$CsClO_4$

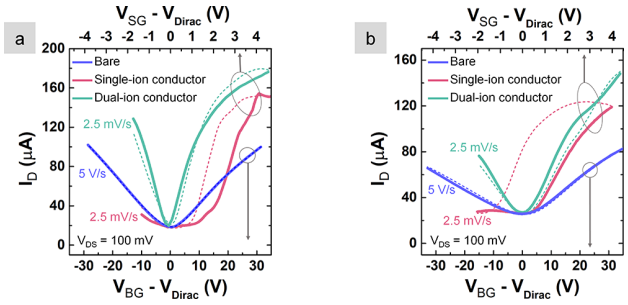

Figure 4. (a, b) Transfer characteristics of two graphene FETs. Back-gated bare devices (blue), side-gated with single-ion conductor (red), and side-gated with dual-ion conductor (green). Solid and dotted lines indicate scans from negative to positive gate voltages and from positive to negative gate voltages, respectively. Note that the gate voltages were normalized with respected to V_{Dirac} to facilitate comparison between n- and p-branches currents using different gating methods. The original data are provided in Supporting Information, Part 3.

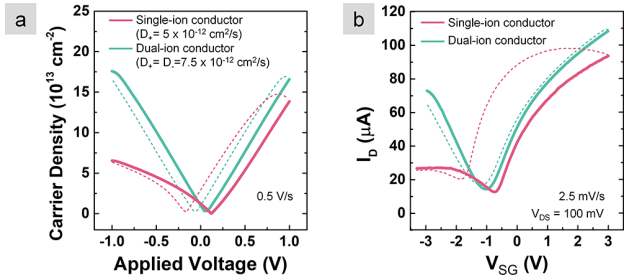

Figure 5. (a) COMSOL simulations of corresponding charge carrier densities within the grounded electrode in a parallel-plate capacitor geometry with the single-ion conductor (red) and the dual-ion conductor (green). (b) Transfer characteristics of both ion conductors on one graphene FET (device 3): the single-ion conductor is red and the dual-ion conductor (PEO:$CsClO_4$) is green. In both (a) and (b), the voltage is swept from negative to positive (solid lines) and then reversed (dotted lines).

(green), both the n- and p-branches are clearly observable and show increased current compared to the bare, back-gated devices. Overall, for the n-branch, EDL gating with either dual- or single-ion conductor shows enhanced on current (~80 and 60% for dual- and single-ion conductors, respectively) over back gating through SiO_2. This improvement is attributed to

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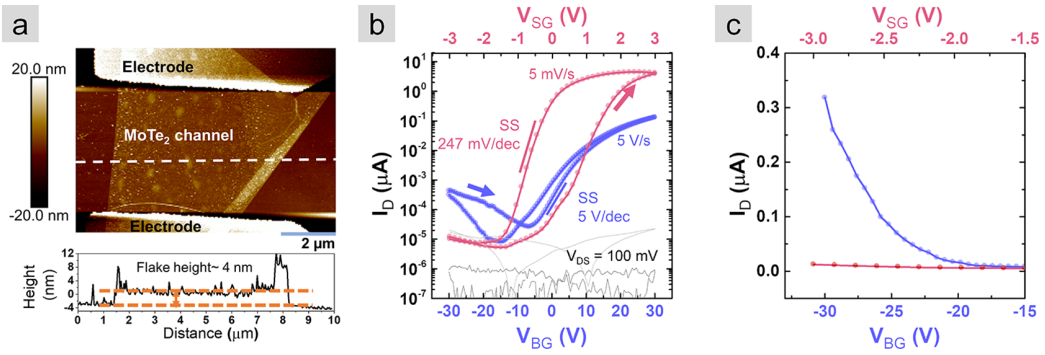

Figure 6. (a) AFM topography scan of a bare $MoTe_2$ FET channel (before electrolyte deposition). The location of the line scan is indicated by the white dash line. (b) Transfer characteristics of the $MoTe_2$ FET in log scale with back-gated transfer measurements from $V_{BG} = -30$ to 30 V on the bare FET in blue and side-gated transfer of the same FET from $V_{SG} = -3$ to 3 V with single-ion conductor in red. (c) Zoomed transfer curves on a linear y axis over a negative range of V_{BG} to highlight the suppressed p-branch when using the single-ion conductor.

the larger EDL capacitance and agrees with previous reports.[15,16] For the p-branch, the enhancement of on current is again observed for the dual-ion conductor but is suppressed for the single-ion conductor. Note also that the Dirac point location in the transfer measurements shifts to negative V_{SG} after the deposition of the single-ion conductor and does not return to zero after removing the electrolyte with solvent and AFM cleaning (Supporting Information, Figure S5). However, this shift is commonly observed in EDL gating of graphene FETs using dual-ion conductors[23,35] and reflects that the electrolyte induces doping of the graphene channel even in the absence of a gate voltage. The original data and discussion of the differences between devices are provided in Supporting Information, Part 3.

The successful ambipolar modulation of the channel current using a dual-ion conductor indicates that the single-ion conductor did not change the graphene channel in a way that would prevent hole conduction. This further supports the understanding that suppressed p-branch current in the single-ion conductor is caused by the cation depletion layer having weaker gate modulation compared to the EDL. This effect can be captured by modeling the dynamic response of single- and dual-ion conductors in response to a voltage sweep. A time-dependent Nernst–Plank–Poisson equation was used with a geometry identical to Figure 2c,d. The voltage is applied to the right electrode, and the ion distribution near the left (grounded) electrode is monitored. The ion mobility of the single-ion conductor is lower than that of the dual-ion conductor (as mentioned above and in Figure S1), and we therefore set the diffusion coefficient of the dual-ion conductor to be 1.5 times larger than that of the single-ion conductor.

Figure 5a shows the predicted carrier density in response to a voltage sweep in the range of ±1 V. For the dual-ion conductor, anions and cations accumulate at the electrodes identically, resulting in a symmetric carrier density with respect to the applied voltage polarity. In contrast, for the single-ion conductor, the carrier density at the grounded electrode is lower under a negative voltage corresponding to the cation depletion region, compared to positive voltage corresponding to a cationic EDL. These results agree with the smaller capacitance at the depletion layer, as discussed above regarding Figure 2.

If we consider only EDL gating of the single- and dual-ion conductors (i.e., $V_G > 0$), the maximum predicted carrier densities are similar (15×10^{13} cm^{-2} and 17×10^{13} cm^{-2} for single and dual-ion conductors, respectively). The similarity is also reflected in the steady-state modeling results in Figure 2c,d where the voltage dropped across the grounded electrode is similar for single-ion (0.85 V) and dual-ion conductors (0.89 V). The EDL thicknesses are also similar (~0.5 nm), and therefore, the charge densities are expected to be similar.

To compare directly between modeling and experiments, Figure 5b shows the transfer curves measured experimentally on a third device (device 3) using both single- and dual-ion conductors (see also Figure S5, Supporting Information). The experimental results of all three devices shown in Figures 4 and 5 exhibit similar trend and match closely with simulations.

The similar n-type doping performance between the single- and dual-ion conductors is encouraging because it suggests the possibility of using the single-ion conductor to induce high charge density similar to dual-ion conductors, which is up to 10^{14} cm^{-2} as measured experimentally[25,26] and also predicted in simulations in Figure 5a. Note that a higher applied voltage is required experimentally to achieve the same carrier density as the simulation because of the geometry differences and imperfect ion packing. In addition, we measured the EDL capacitance induced by the single-ion conductor by a series of V_{SG} transfer measurements under various V_{BG} (Figure S6, Supporting Information). The EDL capacitance of the single-ion conductor (1.66 μF/cm^2) is very similar with the reported value of dual-ion conductors (1–4 μF/cm^2),[15,26,45] which also implies the possibility of achieving similar n-type gating. The ability to pack ion densely is critical for creating electrostatic imbalance in the single-ion conductor, which can lead to mechanical bending of the electrolyte if it is placed on a semirigid support (i.e., a suspended 2D flake).

Lastly, to make sure that the gating performance of the single-ion conductor is not unique to graphene and can also be observed in 2D crystals, $MoTe_2$ FETs were fabricated with the same device geometry as the graphene FETs. We choose $MoTe_2$ because one potential use for single-ion conductor gating is to explore the strain-induced semiconductor-to-metal transition for which $MoTe_2$ is predicted to have one of the smallest strain requirements (i.e., <3%).[6] Moreover, the transition has been experimentally demonstrated in $MoTe_2$.[8,9] The AFM scans of one $MoTe_2$ FET are shown in Figure 6a, and the line scan shows the channel thickness to be 4 nm (~6 $MoTe_2$ layers). The majority of the flake is in uniform thickness, and therefore, we expect minimal impact from thickness variations on the electrical properties.[46] Back-

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gated transfer characteristics were measured on bare devices, as indicated by the blue transfer curve in Figure 6b. The bare $MoTe_2$ FET is ambipolar with a minimum current of $\sim 10^{-5}$ μA at V_{BG} of ~ -15 V. The on/off ratio of the n-branch from $-5 < V_{BG} < 30$ V is $<10^4$, and the p-branch from $-30 < V_{BG} < -17$ V is <100.

Using the single-ion conductor, the maximum current through $MoTe_2$ at V_{SG} = 3 V is ~32 times larger compared to the maximum current of the bare FET at V_{BG} = 30 V (Figure 6b). Output characteristics also show effective gate control of the channel current using the single-ion conductor (Figure S9). The on/off ratio of the n-branch increases from 10^4 for the bare FET to $\sim 10^6$ with the single-ion conductor. Also, the subthreshold swing (SS) of the n-branch decreases with the single-ion conductor (from 5000 mV/dec by back-gating the bare device to 247 mV/dec). The strong current modulation and the enhanced on/off ratio further confirm the strong EDL modulation by the single-ion conductor. Similar to the graphene FETs, the I_D of the p-branch remains suppressed, in this case, at the off level of 10^{-5} μA. The suppressed p-branch is highlighted in a linear plot in Figure 6c.

CONCLUSIONS

EDL gating using a custom-synthesized single-ion conductor is demonstrated for the first time on both graphene and $MoTe_2$ FETs. Transfer characteristics for all the FETs show an enhanced n-branch using the single-ion conductor and a suppressed p-branch compared with back-gated measurements of bare FETs. Finite element modeling of ion transport in response to an applied field shown that the p-branch suppression results from the combination of using a single-ion conductor and an asymmetric gate/channel geometry. In addition, the two ion conductors compared on the same FETs both show similar performance in the n-branch (i.e., on/off ratio and maximum ion current), suggesting that the single-ion conductor can achieve cationic ion densities similar to the well-studied dual-ion conductor (i.e., up to 10^{14} cm^{-2}). This achievable carrier density is also predicted by modeling and would be theoretically sufficient to induce several percent strain in a 2D crystal. This is the first demonstration of a single-ion conductor-gated multilayer 2D crystal FET, and the results lay the groundwork for inducing strain in 2D materials locally via field effect and for demonstrating the 2H to 1T′ phase transition. These features are potentially useful for creating an electronic switch with a low turn-on voltage and steep subthreshold swing and for 2D flexible electronics with functionality controlled by strain.

EXPERIMENTAL SECTION

Device Fabrication and Electrical Characterization. Freshly cleaved few-layer graphene and $MoTe_2$ flakes (1.5 nm–5 nm-thick) were mechanically exfoliated from their bulk sources (2D semiconductors) to p-doped silicon substrate with 90 nm SiO_2 (Graphene Supermarket, resistivity of 0.001–0.005 ohm·cm). The flake topography and thickness were measured by AFM (Bruker Dimension Icon, ScanAsyst mode). Source/drain electrodes and side gates were patterned by EBL (Raith e-LINE). Also, Ti (3 nm)/Au (120 nm) metals were deposited by e-beam evaporation (Plassys MEB550S electron beam evaporator) at a base pressure of $<10^{-6}$ Torr. After liftoff, FETs were transferred to a cryogenic vacuum probe station (Lakeshore, CRX-VF) for vacuum annealing (400 K, 4 h at a pressure of 2×10^{-6} Torr) and initial electrical measurements. After annealing, FETs were transferred from the probe station to an Ar-filled glovebox using an Ar-filled load lock without exposure to ambient air for electrolyte deposition, before transferring back to the probe station for electrical measurements. The electrical measurements were conducted using a Keysight B1500A semiconductor parameter analyzer at a constant temperature of 300 K.

Single-Ion Conductor Synthesis. The polyester single-ion conductor was synthesized by a two-step melt condensation between poly(ethylene glycol) (PEG) 400 (M_w = 400 g mol^{-1}) and dimethyl 5-sulfoisophthalate sodium salt.[34] The resulting polyester Na was then sealed in semipermeable dialysis membranes and exposed to an excess of LiCl (0.5 M) in deionized water to exchange Na^+ for Li^+.[34] The final product, polyester Li (PE400-Li), was dissolved in dimethylformamide (DMF) inside an Ar-filled glovebox to obtain a 3 wt % solution. The solution was drop-cast on graphene and $MoTe_2$ FETs (8 μL on the 1 cm^2 chip), and the DMF was removed by evaporating naturally in the glovebox overnight. The FETs coated with the single-ion conductor were transferred back to the probe station using the load lock for subsequent measurements.

Dual-Ion Conductor. The dual-ion conducting polymer electrolyte (PEO:$CsClO_4$) was prepared similarly to previously published work.[15] PEO (Polymer Standards Service, M_w = 94600 g mol^{-1}) and $CsClO_4$ (Sigma-Aldrich, 99.9%) were dissolved in anhydrous acetonitrile (Sigma-Aldrich) to make a 1 wt % solution with an ether oxygen to Cs molar ratio of 76:1. Twenty-five microliters of the solution was drop-cast onto the 1 cm^2 sample of graphene FETs in the glovebox, dried at room temperature until the majority of the solvent evaporated, and then annealed at 80 °C for 3 min.

Modeling. The time-dependent, modified Nernst–Planck–Poisson relationship was used in COMSOL Multiphysics to predict ion accumulation in response to voltage. Ion migration was modeled using a modified version of the Nernst–Plank equation: $\frac{dc}{dt} = \nabla(D_{\pm}\nabla c_{\pm} + \frac{D_{\pm}F}{RT} z_{\pm} c_{\pm} \nabla V + \gamma$, where c is the ion concentration, D is the ion diffusion coefficient, F is faraday's constant, RT is the thermal energy, γ is the steric repulsion term, and V is the electrolyte potential. The potential is coupled to Poisson's equation $\nabla^2(-\varepsilon V) = F\sum_{i=1}^{2}(z_i c_i)$, where ε is the permittivity of the electrolyte ($\sim 10\ \varepsilon_0$)[36] and z is the ion charge number (+1 for cations, −1 for anions). A stern layer, defined by $\nabla^2(-\varepsilon V) = 0$, was used directly adjacent to the electrode and SiO_2 boundaries and set to equal 2 Å. The bulk concentration of ions corresponds to an ether oxygen to lithium ratio of 20:1, and the density of the polymer is assumed to be 1 g/cm^3.

For all four geometries, a 50 μm-long by 5 μm-thick electrolyte was used; electrodes were modeled as boundary conditions with the appropriate potentials. In the models involving geometries of equal-sized electrodes, the electrode surfaces constituted the entire 50 μm boundary. A zero charge boundary condition (defined as $n \cdot D = 0$, where n is the surface normal vector and $D = -\varepsilon \nabla V$ was used for the nonelectrode boundaries). The mesh size near the electrode interfaces was decreased until the EDL concentrations remained within 1% of its previous value.

In the models involving unequal electrodes, boundary conditions for nonelectrode boundaries were defined to mimic SiO_2 by using a modification of the previous boundary condition: $n \cdot D = -\frac{\varepsilon_{SiO2}\phi}{t}$, where ε_{SiO2} is the permittivity of SiO_2, ϕ is the local electrolyte potential at the interface, and t is the oxide thickness (90 nm). This modification allowed for a nonzero electric flux through the nonelectrode boundaries (i.e., 90 nm oxide) and therefore allowed ions to accumulate near the oxide surface. To determine the carrier density in ions/cm^2 through the electrolyte, the volumetric charge density was integrated using trapezoid approximation along a cutline taken across the electrolyte perpendicular to the center of the grounded electrode beginning at the electrode surface and terminating at the center of the electrolyte.

DSC Measurements. The DSC samples were prepared inside the Ar-filled glovebox. PE400-Li (8.7 mg) and PEO:$CsClO_4$ (7.1 mg) were hermetically sealed in aluminum DSC pans. Measurements were made on TA 250 calibrated with an indium standard. To measure T_g (glass transition temperature) and T_m (melting temperature), samples were heated to 100 °C to erase the thermal history, cooled to −70 °C at 3 °C min^{-1}, and heated to 100 °C at 5 °C min^{-1}.

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ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.9b11526.

DSC measurements; 2D potential profiles from COMSOL modeling; transfer measurements on device 3; estimation of EDL capacitance in the single-ion conductor-gated FET; impact of device geometry on charge density from COMSOL simulations; effective gate size; and output characteristics of single-ion conductor-gated $MoTe_2$ FETs (PDF)

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‖K.X. and J.L. contributed equally to this work. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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