Active Power Distribution Node Enhanced Reconfigurable Grids and their Effects on Distributed Energy Resource Availability

by

Alvaro Cardoza

Bachelor of Science in Electrical Engineering, University of Pittsburgh, 2012

Master of Science in Electrical Engineering, University of Pittsburgh, 2016

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This dissertation was presented

by

Alvaro Cardoza

It was defended on

July 16, 2021

and approved by

Luke Solomon, PhD, Principal R&D Electronics Engineer
Hitachi ABB Power Grids

Robert Kerestes, PhD, Assistant Professor,
Department of Electrical and Computer Engineering

Brandon Grainger, PhD, Assistant Professor,
Department of Electrical and Computer Engineering

Zhi-Hong Mao, PhD, Professor,
Department of Electrical and Computer Engineering

Dissertation Advisor: Alexis Kwasinski, PhD, Associate Professor,
Department of Electrical and Computer Engineering

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Alvaro Cardoza, PhD

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As interest for using more DC distribution systems increase, there is a need for developing effective DC-DC interfacing power electronic devices for managing power flow and power quality levels among a system's increasingly diversified array of sources and loads. Some of the applications in which DC-DC power electronic interfaces are gaining increased attention include the information and communication technologies (ICT), electric vehicles, and renewable generation industries. There is a growing interest in these fields related to the integration of distributed generation (DG) technologies in electrical networks to ensure that DG power supply availability is increased.

This dissertation explores the use of a multiple-input, multiple-output (MIMO) DC-DC modular multilevel converter (MMC) topology as nodes within a distribution network for managing power flow and power quality levels. Each power electronic node is referred to as an active power distribution node (APDN) and a network of these nodes creates a reconfigurable distribution grid architecture. This alternative and modular approach to designing distribution networks provides selective increased power supply availability to strategic loads within the structure, and in turn provides an increased utilization of renewable generation sources, which inherently have intermittent generation profiles. A DC test system was chosen as the focus for this work to reflect the prevalence and increased penetration of both DC generation and loads within electrical networks. The performance of the APDN converter will be evaluated individually for its

general input and output characteristics and as part of a network of interacting APDNs. Key focus areas for assessing the APDN's functionality include its MIMO power routing and power buffering abilities, its stability performance, and its ability to increase the availability of connected sources and loads. The results of this work aim to demonstrate the benefits of creating a reconfigurable distribution network and how it can more effectively meet the needs of the dynamically changing landscape of distribution network power generation and load profiles.

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Acknowledgements

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1.0 Introduction

As distribution-level power systems throughout the world continue to utilize more DC infrastructure, effective DC-DC interfacing power electronic devices must be developed for managing power flow and power quality levels between a system's increasingly diversified array of sources and loads [1]. DC-DC power electronic interfaces are continuing to gain increased attention throughout many distribution applications, including the information and communication technology (ICT) [2], electric vehicle [3], and renewable generation [4] industries. It is important to look at new ways to integrate the growing penetration of distributed generation (DG) throughout electrical networks and rethink the way that electricity is distributed to ensure the maximum availability for DG power supplies.

Electricity markets continue to utilize more distributed generation to meet the rising global electricity demand. Global demand for energy in 2015 was 575 quadrillion BTUs (17.26 TWh) and projections for 2040 estimate a rise up to 736 quadrillion BTUs (24.62 TWh) – an increase of 28% from 2015 levels [5]. Figure 1 shows these projections made by the U.S. Energy Information Administration (EIA) for the growth of this energy demand over a 50-year time period from 1990 projected into 2040; each year's data is broken down into energy consumed by either developed or developing nations. Most of the growth in energy demand between 2015 and 2040 is expected to come from developing nations with quickly growing populations, growing economies, and access to the energy market [5].

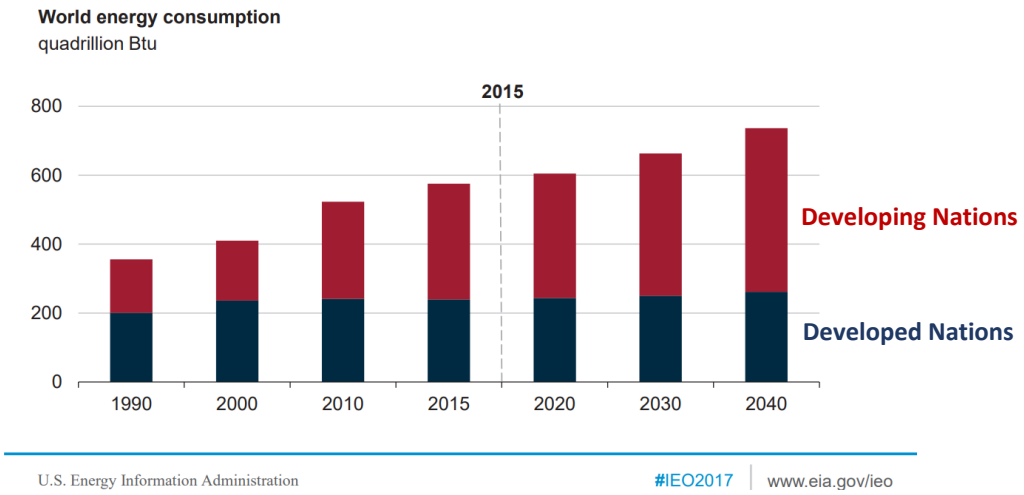

Figure 1. World energy consumption as of 2017 over a 50-year period including projections into 2040 [5]

With the inclusion of additional DG, generation profiles are diversifying to meet this growing demand as older power plants are retiring. Distributed generation installations of renewable generation sources, such as solar and wind, are filling this growing electricity generation and demand gap. Government incentivized programs like the Department of Energy SunShot program have helped to stimulate further adoption of solar in the United States as an economically viable generation source -- increasing solar's generation capacity from 3 GW to 47 GW over just 6 years. The SunShot program collaborates with universities, national laboratories, private companies, non-profit organizations, as well as local and state governments to foster the technological, policy, and economic development of solar in the United States and remove critical barriers for greater deployment. SunShot continues to stay aggressive with setting future economic goals for solar and aims to bring the cost of solar to record lows by 2030: utility-scale solar power to $0.03 per kWh, commercial-scale solar to $0.04 per kWh, and residential-scale solar to $0.05 per kWh [6]. At $0.03 per kWh, utility-scale solar would then be one of the most affordable power generation options available – lower than most fossil-fuel based generation – fueling the continued growth of solar installations across the world.

As renewable generation sources continue to become more cost-effective solutions, their increased adoption across all sectors will undoubtedly follow. Energy storage will play a large role in utilizing this growing supply of generation by storing the energy (i.e. during the daytime for solar and nighttime for wind) and discharging it as needed across a daily load profile [7]. Large scale energy storage technology has been prohibitive in the past due to its high-cost and the limited state policies, wholesale market rules, and retail rates that govern its use. However, as battery costs continue to decline and batteries According to the EIA, the United States reportedly has 1.4 GW of operational large-scale battery capacity as of the end of 2020 with another 4 GW of battery capacity scheduled for installation in 2021 [8]. These numbers are projected to grow substantially over the next several decades with energy storage capacity substantially rising above 20,000 MW by 2030 and reaching around 40,000 MW by 2050, as seen in Figure 2. Projections for solar photovoltaic capacity are expected to roughly quadruple between 2020 and 2050, while wind generation capacity sees more modest gains. The increased adoption of renewable generation sources and energy storage installations demonstrate a changing electric grid infrastructure that must be met with new approaches for handling the new power flow through distributed grid networks.

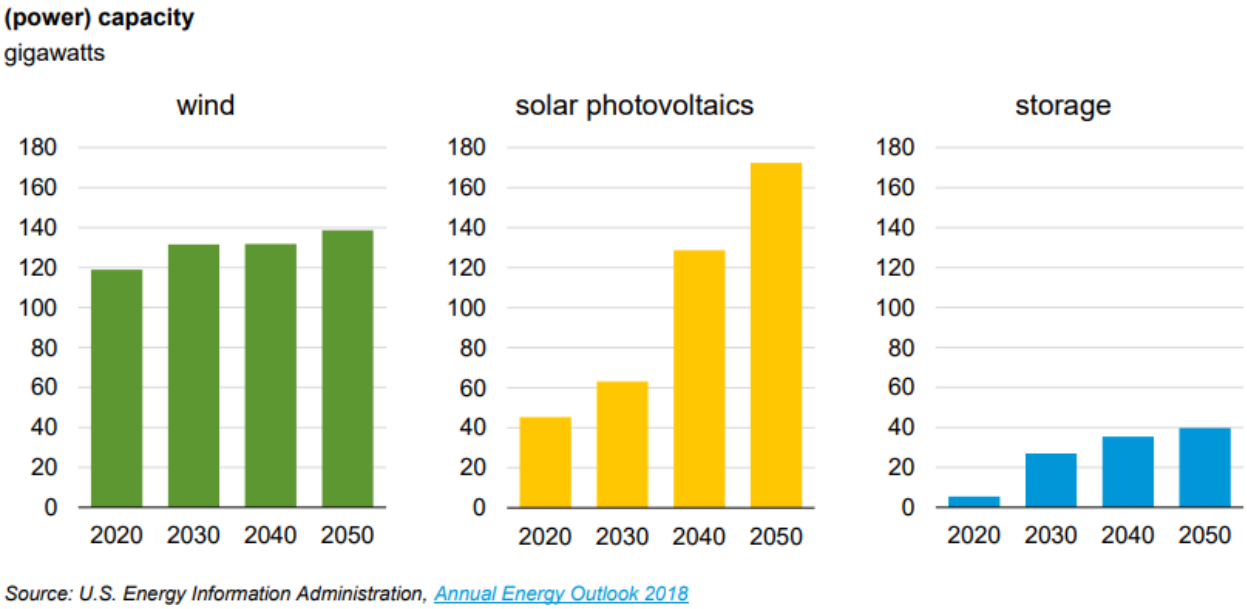

Figure 2. United States wind, solar, and battery storage capacity projections, 2020-2050 [9]

With DC infrastructure increasingly adopted on both generation- and load-sides, DC-DC power electronic interfaces can be utilized within distribution networks in order to improve power supply availability to strategic loads and provide an increased utilization of renewable generation sources. Potential power electronic interfaces should be rated to handle system DG and loads and be robust solutions in case of component failure. Conventional DC/DC converter topologies like the boost and the flyback converters suffer power limitations inherent to their use of a single semiconductor switch. Their single switch design limits their ability to process higher power ratings to the voltage and current ratings of their individual semiconductor switch. Furthermore, these fundamental converter topologies are vulnerable to high losses and ringing when operated at high conversion ratios regardless of their operating power range. The operational shortcomings associated with conventional DC/DC converter topologies shift the investigation towards

alternative solutions that can handle higher power ratings and conversion ratios. Overcoming these limitations can be achieved by either manufacturing larger, higher-rated semiconductor components or by considering alternative converter topologies.

Due to the increased cost associated with higher-rated components, industry and researchers alike have explored the stacking of conventional converter topologies as modules -- reducing the voltage and current stress on each module's components proportional to the number of stacked modules. These lower-rated stacked modules are more cost effective and accommodate higher power and higher conversion ratio applications, all the while reducing the size of output filtering without increasing switching frequency [10]. This family of power electronic devices are referred to as modular multilevel converters (MMC). The MMC has proved to be a versatile and efficient topology used widely in high voltage direct current (HVDC) transmission systems, medium voltage variable speed drives, dynamic braking choppers, and STATCOMs [11]–[13].

Herein research efforts utilize the DC-DC modular and multi-port interfacing topology known as the triangular modular multilevel converter (TMMC) [14]. The TMMC uses stacked capacitor voltages from synchronous buck-boost derived modules in order to effectively step-up or step-down the voltage depending upon the direction of current flow. Input and output ports can be placed between any of the modules to meet source and/or load system requirements making this an ideal converter interface topology. This work investigates the design, implementation, and testing of the TMMC topology within the context of active power distribution nodes (APDN), which serve as nodes within a distribution network and provide network capabilities of power routing, power buffering, and improved DG availability.

1.1 Objective

This work aims to explore the use of power electronic converters within DC distribution network architectures to provide additional power flow control, power quality, and power supply availability to the operation of the network. The scope of the work and methodology is inherently application agnostic and can be applied to various DC distribution-level network architectures such as DC microgrids, electric ships, cell networks, and data centers. Ultimately, this project provides a discussion pertaining to the selection of a suitable APDN converter, works through the design and simulation of a modular converter solution for application flexibility, explores the converter's printed circuit board (PCB) hardware realization, and studies the APDN's impact on DER availability within a system. Strengths and weaknesses of the system testbed will be evaluated throughout each step of the research scope to serve as a reference for future work.

1.2 Dissertation Organization

The dissertation is structured into three main research categories: TMMC-APDN converter investigation, and the design and testing of a TMMC-APDN module prototype, and an investigation of the TMMC-APDN's impacts on DER availability. The APDN investigation includes a topological analysis of the selected converter, simulation results of the design, an examination of averaged modeling techniques for improved simulation performance, and a study of the converter's stability around a defined operating point. The printed circuit board (PCB) design and testing results for a TMMC-APDN module will be detailed, compared to simulations, and discussed. Lastly, an analysis of power supply availability within distribution networks will

be defined and investigated outlining the approach for evaluating the performance of an APDN controlled distribution network. After each section has been described, the dissertation will conclude with a discussion of results and an outline of future work.

2.0 Background on Active Power Distribution Node (APDN)

Distributed energy resources are a hot topic for research institutions and industry alike due to their rising adoption globally and the technical challenges with reducing grid instabilities through DG's growing use in traditional grids, especially with renewable energy resources. Despite these challenges, the distribution of generation sources is considered to hold many benefits in terms of its technical, economical, and environmental impacts on power systems [15]. It is important to look at new ways to integrate the growing penetration of DG throughout electrical networks and rethink the way that electricity is distributed and ensure the availability of DG power supplies is maximized.

Historically speaking, AC power has been the standard for both transmission and distribution power systems with the exception of telecommunication power systems, which operates on low power DC systems. This held true for over a century mostly because of the disparity between DC power and AC power's abilities to reach higher power levels and transmit that power over long distances. DC generators operated at 110 Vdc, were generally lower powered, and had to be relatively close to the load base. On the other hand, higher-powered AC generators and motors combined with the AC transformer's abilities to step voltage up and down allowed for the transmission of much larger amounts of power over long distances. In recent decades, however, the rise of DC power electronic technologies has reintroduced the relevance of DC technologies at both the transmission and distribution power levels. In many respects, DC distribution networks nowadays are considered more proficient at interfacing with a diverse array of both DC and AC sources and loads without sacrificing reliability or availability [16]. Power electronics enable

more flexible control of connected generation and loads through their control and PWM schemes, and DC networks enable a simpler integration for inherently DC technologies such as PV and energy storage.

Typical distribution networks are designed with either radial cabling, ring-type cabling, ladder-type cabling, or meshed cabling -- with radial designs being the most popular approach [15], [17]. Network designs can offer a higher level of availability to their systems by adding lines and incorporating circuit redundancy for back-up power flow in the instance of a fault or large loading. Simplified examples of each type of network can be found in Figure 3, Figure 4, Figure 5, and Figure 6, respectively. While radial networks are quite common and often serve as the focus for many microgrid studies, they offer the worst flexibility and availability of generation and storage resources on the grid due to their lack of redundant paths. Ring-type and ladder-type schemes offer a better availability of resources through their redundant parallel paths, and meshed networks offer the most diverse collection of redundant power paths and circuits. As being the most complex of network topology, meshed networks are also the most expensive to implement and are mostly used when a project prioritizes fault tolerant architectures with higher availability and/or needs to supply a critical load like a hospital [16]. However, power supply availability and network reconfigurability are the two core focuses of this dissertation work, and therefore, the benefits of meshed networks outweigh their drawbacks and they will serve as the network topology foundation of this work.

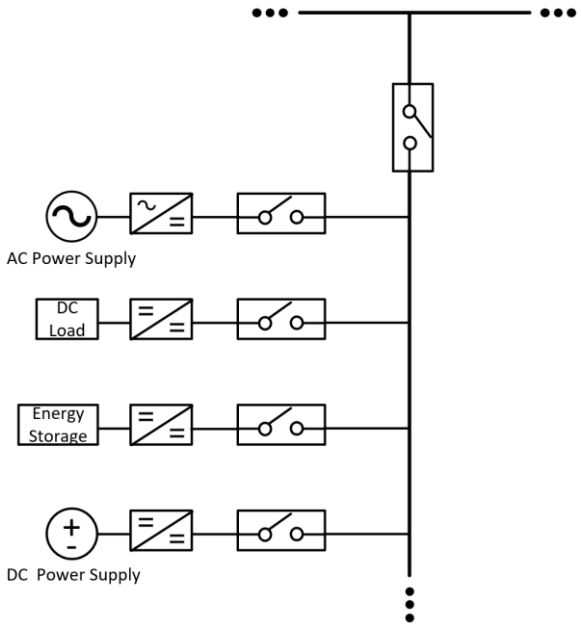

Figure 3. Radial Distribution Network Example

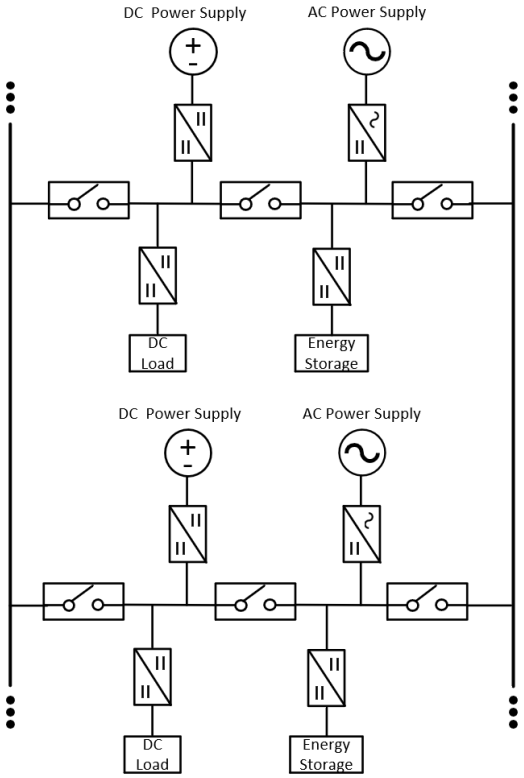

Figure 4. Ladder Distribution Network Example

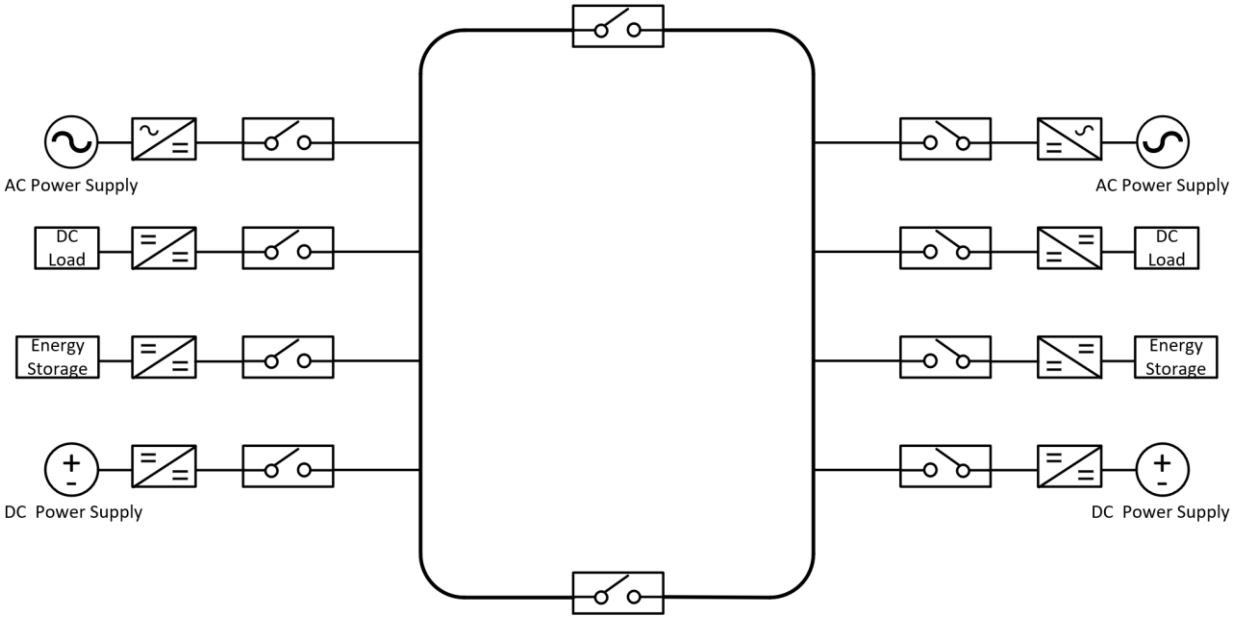

Figure 5. Ring Distribution Network Example

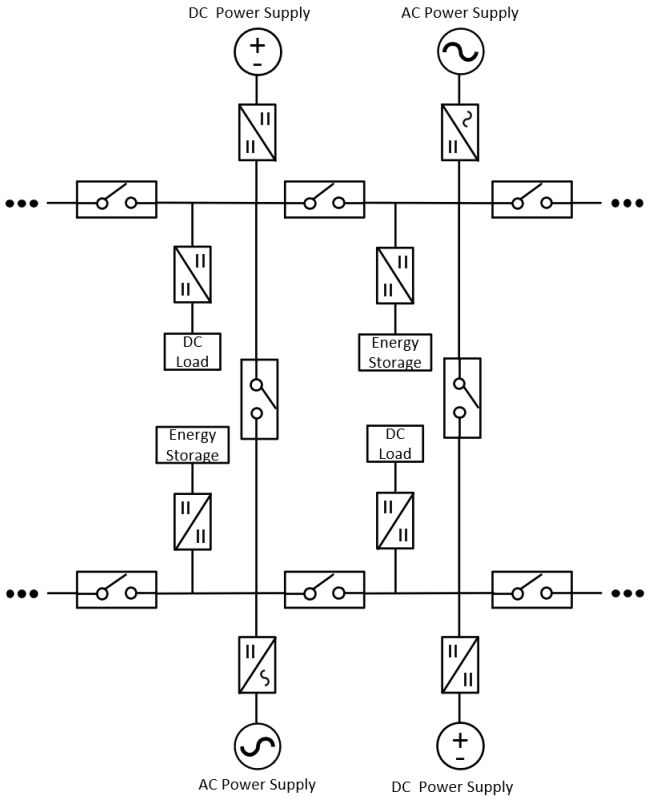

Figure 6. Meshed Distribution Network Example

Previous works have shown the technical planning and demand-cost benefits of installing energy storage as a distributed source for critical loads that are sensitive to power availability issues [18], [19]. Studies performed in [20] explore the relationships between a wide-range of downtime costs and different circuit interfaces like power converters and circuit breakers. Results demonstrate that the higher initial cost for power electronic interfaces with embedded energy storage -- like the designs explored in this dissertation -- can be offset when integrating these power electronic solutions into high availability demanding applications with large downtime costs. These costs can be quite expensive based on the application, such as those in highly sensitive ICT systems. According to an industry-funded economic study in 2013, the average downtime cost for a data center is about $474,480/hour [21], which serves as a big motivator for improving system availability and reducing these costs. The relationship between microgrid design, converter

selection, and availability is investigated in [22] providing an extensive framework for evaluating availability in different distribution network designs. Furthermore, systems incorporating multi-port converters were found to promote source diversity and increase overall system availability and resiliency [23].

There are few examples investigating reconfigurable distribution networks in the literature. Early approaches began with the use of switches between branches in a radial network that can be switched on and off to transfer load with minimal losses helping to balance the overall load profile. The technique transforms radial networks into temporary ring loops with the switch selection and operation chosen according to two power flow approximation algorithms for optimal branch power exchange. These loops then open back up into new radial branches and provide an added level of flexibility and redundancy to the network in cases of high load [24], [25]. At the time this technique provided an innovative solution using existing distribution network design, however, it struggled to converge to the global optimal solution, especially as the system grew larger. A more modern approach to developing reconfigurable grids utilizes the hierarchical control of microgrids [26]. Intersecting control layers operate as a form of redundancy and communicate the status of different source and load branches across the microgrid. The distribution network can then make use of power electronic interface converters – to operate akin to the aforementioned switches – to facilitate a similar technique as earlier works with switching the radial network into a temporary ring loop configuration assisting with clearing faults and balancing loads.

This dissertation expands on the previous works of developing reconfigurable DC distribution networks by utilizing Active Power Distribution Nodes (APDN) to manage power flow and load exchange per Figure 7. APDNs utilize bi-directional MIMO DC/DC power electronic converters to enable power-routing and power-buffering functionality, which ultimately

function to improve the power supply availability of a network [27]–[30]. This alternative and modular approach to designing distribution networks provides selective increased power supply availability to strategic loads within the structure, and in turn provides an increased utilization of renewable generation sources, which inherently have intermittent, variable generation profiles [16], [20], [31]–[33].

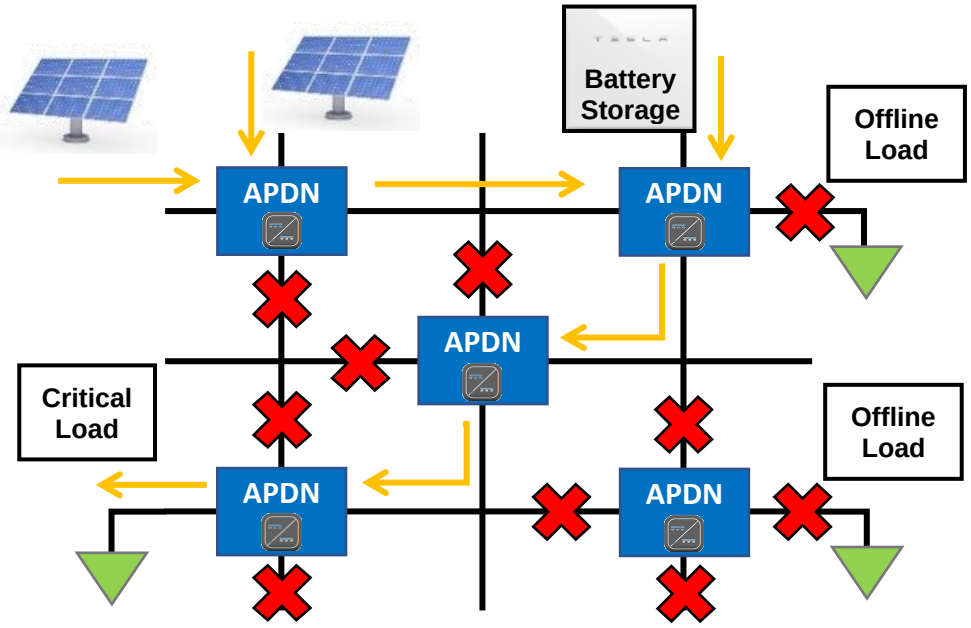

Figure 7. Active power distribution node reconfigurable distribution structure with example power flow scenario (where yellow arrows indicate power flow, red x's indicate closed I/O ports, and green triangles indicate loads)

A suitable APDN converter topology must demonstrate the ability for bi-directional MIMO functionality and may contain an energy storage element for power-buffering between its inputs and outputs. The Triangular Modular Multilevel Converter (TMMC) was selected as the core topology for this work for its stability robustness and reconfigurable MIMO design flexibility [14]. To enable power-buffering, a hybrid battery-and-ultracapacitor-based energy storage system (ESS) version of the TMMC-APDN is investigated—expanding the work from [34]. By utilizing

a hybrid approach, the energy density and power density benefits of each energy storage technology can be utilized, while mitigating their respective weaknesses. Ultracapacitors operate for transient dynamic response over a range of milliseconds to minutes, while batteries provide a power-deficit compensation over a range of minutes to hours. Additionally, the embedded energy storage helps promote the expansion of new generation and loads added to the distribution network by power-buffering potential new power imbalances that may arise [16]. Studies demonstrate the effectiveness of using ultracapacitor ESSs for transient load-leveling and power-buffering applications with both DC and modular multilevel converter topologies [35]–[37]. Additionally, the embedded energy storage can help promote the expansion of new generation and loads being added to the distribution network by power-buffering through new power imbalances that may arise during connection and disconnection transients. For instance, APDNs' power-buffering feature can decouple the dynamics between sources and loads with the energy storage rapidly discharging to feed a load of interest so that the performance of the load isn't affected by source dynamics (such as the intermittence associated with PV and wind). Similarly, this dynamic puts less strain on generation sources when the load shifts throughout the day.

The TMMC topology is an expandable (n+1)-level, bi-directional modular multilevel DC-DC converter topology with a triangular form factor of *n* rows of synchronous buck-boost converter modules plus one additional row for the addition of an input/output for a full converter conversion ratio of *n+1*, as shown in Figure 8. The dedicated input and output of Figure 8 are purely representative and each can operate as either an input or an output. With its modular structure and bidirectional functionality, the TMMC can operate as the reconfigurable APDN and can be modified to act as a SISO, MISO, SIMO, or MIMO converter. Between each row of modules, a source or load can be attached, demonstrating the TMMC's versatility and

reconfigurable MIMO functionality. Voltage distribution between rows can be uniform or non-uniform based on the needs of sources and loads; however, stability is most easily achieved with a balanced distribution of voltages across the MMC layout. The use of embedded row energy storage helps to support the converter's stability of non-uniform voltage distribution. Due to the triangular form factor of the multilevel converter, voltage and current sharing can be achieved for each TMMC module, benefitting the converter's modularity and ease of controllability. Voltage and current sharing are most easily achieved when operating in a single-input, single-output configuration; however, a well-designed controller can accommodate adequate levels of voltage and current sharing for MIMO applications [38].

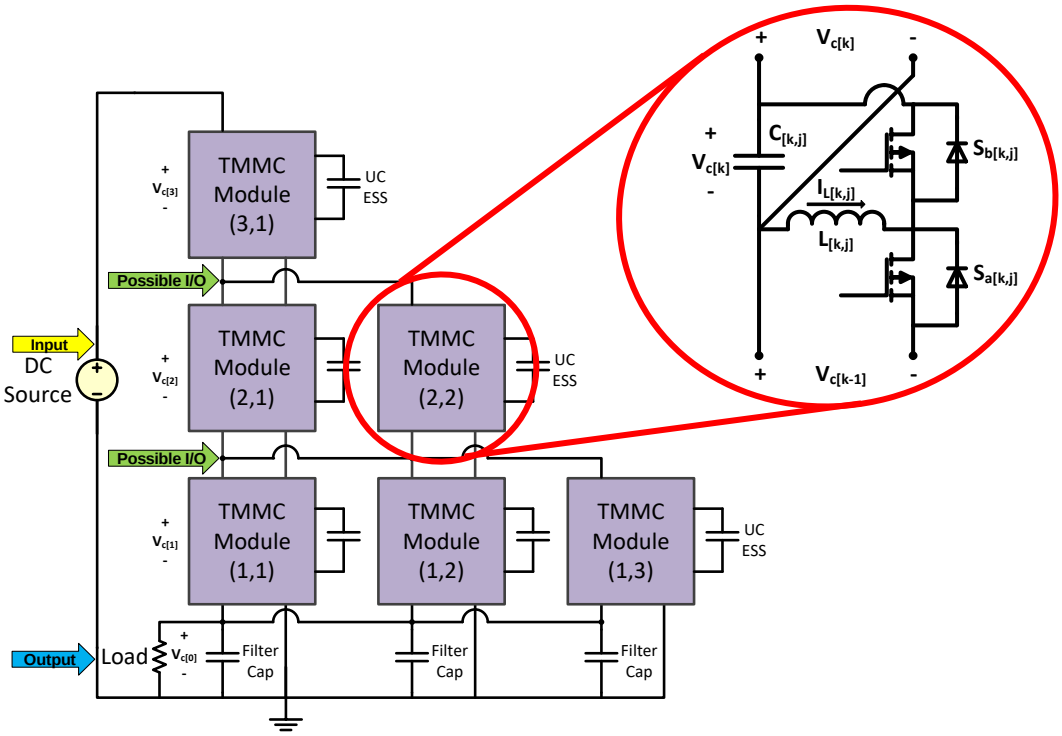

Figure 8. Three-level multiple input, multiple output triangular modular multilevel converter with an ultracapacitor energy storage system demonstrating potential input and/or output ports labeled in green, dedicated output resistive load in blue, and input DC source in yellow

Equations (2-1) and (2-2) show the capacitor and inductor dynamics of a MIMO step-down TMMC-APDN, where *n* is the number of module rows, *k* is the particular row being evaluated, *b* refers to the number of parallel modules per evaluated row, i_k is the current flowing from or to a connected input or output, respectively, $i_{ESS(k)}$ is the current flowing from or to the embedded energy storage, and R_L is the inductor resistance of an individual module. Each row's capacitor voltage dynamics is a function of all adjacent rows' inductor currents, the voltage of the adjacent *k+1* capacitor, and the currents of any connected inputs or outputs placed at the node above the module row. Examining the capacitor and inductor dynamics show that a high level of coupling exists between adjacent rows of the converter—demonstrating that the loss of a module row would negatively affect the performance of adjacent rows. This coupling must not only be accounted for to adequately control the converter, but also for the analysis of the converter's availability as the loss of a converter row will negatively impact converter operation. Negative impacts of the dynamic inter-row coupling are lessened by the converter's cascaded voltage-current controller design as well as each module's embedded energy storage. Inductor current dynamics are expressly derived from a row *k*'s capacitor voltage and the capacitor voltage from the previous row, *k-1*, as well as the voltage across the module's inductor.

$$b_k C \frac{d\dot{\bar{v}}_{c(k)}}{dt} = \begin{cases} \sum_{j=1}^{b_{k+1}} \bar{\imath}_{L(k+1,j)} - \sum_{j=1}^{b_{k+2}} \bar{\imath}_{L(k+2,j)}\left(1 - d_{(k+2,j)}\right) - b_{(k+1)} C \dot{\bar{v}}_{c(k+1)} - i_k \,, \\ k = 0 \\ -\sum_{j=1}^{b_k} \bar{\imath}_{L(k,j)} d_{(k,j)} + \sum_{j=1}^{b_{k+1}} \bar{\imath}_{L(k+1,j)} - \sum_{j=1}^{b_{k+2}} \bar{\imath}_{L(k+2,j)}\left(1 - d_{(k+2,j)}\right) - b_{(k+1)} C \dot{\bar{v}}_{c(k+1)} + \sum_{j=1}^{b_k} i_{ESS(k,j)} - i_k \,, \\ k \in \{1, \dots, n-2\} \\ -\sum_{j=1}^{b_k} \bar{\imath}_{L(k,j)} d_{(k,j)} + \sum_{j=1}^{b_{k+1}} \bar{\imath}_{L(k+1,j)} - b_{(k+1)} C \left(\dot{v}_i - \sum_{l=0}^{n-1} \dot{\bar{v}}_{c(l)}\right) + \sum_{j=1}^{b_k} i_{ESS(k,j)} - i_k \,, \\ k = n-1 \end{cases} \tag{2-1}$$

$$Note: \dot{\bar{v}}_{c_3} = \dot{v}_i - \sum_{l=0}^{n-1} \dot{\bar{v}}_{c(l)}$$

$$L \frac{d\bar{\imath}_{L(k,j)}}{dt} = \begin{cases} \bar{v}_{c(k)} d_{(k,j)} - \bar{v}_{c(k-1)}(1 - d_{(k,j)}) - \bar{\imath}_{L(k,j)} R_L \,, \\ k \in \{1, \dots, n-1\} \\ \left(v_i - \sum_{l=0}^{n-1} \bar{v}_{c(l)}\right) d_{(k,j)} - \bar{v}_{c(k-1)}(1 - d_{(k,j)}) - \bar{\imath}_{L(k,j)} R_L \,, \\ k = n \end{cases} \tag{2-2}$$

The capacitor and inductor state equations of each row of the MIMO-TMMC in a step-up configuration are represented by Eqs. (2-3) and (2-4). The dynamics differ from the step-down configuration and are somewhat simpler to navigate through. Each row's capacitor voltage dynamics are a function of the current module's inductor currents, the inductor current of the above row, and the currents of all connected inputs or outputs placed at all nodes above the module row. The inductor current dynamics comprise the voltages of the below row, row *k*, and module's inductor current.

$$b_k C \frac{d\bar{v}_{c(k)}}{dt} = \begin{cases} -\sum_{j=1}^{b_k} \bar{i}_{L(k,j)}\, d_k + \sum_{j=1}^{b_{k+1}} \bar{i}_{L(k+1,j)}\left(1 - d_{(k+1,j)}\right) - \sum_{j=k}^{n} i_j\,, \\ k \in \{1, \dots, n-1\} \\ -\sum_{j=1}^{b_k} \bar{i}_{L(k,j)}\, d_k - i_k, \\ k = n \end{cases} \tag{2-3}$$

$$L \frac{d\bar{i}_{L(k,j)}}{dt} = \begin{cases} -v_i(1 - d_{(k,j)}) + \bar{v}_{c_k} d_{(k,j)} - \bar{i}_{L(k,j)} R_L\,, \\ k = 1 \\ \bar{v}_{c_k} d_{(k,j)} - \bar{v}_{c(k-1)}(1 - d_{(k,j)}) - \bar{i}_{L(k,j)} R_L\,, \\ k \in \{2, \dots, n\} \end{cases} \tag{2-4}$$

2.1 TMMC Controller Design

Each row of modules is controlled by a cascaded two-stage voltage and current controller, which must account for the previously described capacitor and inductor dynamics. For each row of the TMMC, a singular voltage controller is utilized to regulate all parallel modules to promote voltage sharing; however, each module of the converter has its own dedicated current controller as seen in Figure 9. This one-to-one ratio of modules to current controllers is to ensure quick dynamic regulation of the module switches, overcurrent protection of semiconductors, and overall stability of each module in the face of transient events. The current controller is designed to operated much faster than the voltage controller in order to provide such features. During normal steady state operation, each current controller within a row should ideally operate uniformly. The voltage PI controller is fed by the difference of a specified reference voltage and the summed voltages between the controlled module row and the previous row. As mentioned previously, voltage and current sharing across rows is best promoted when the voltage levels between rows are identical; however, the controller can still operate effectively when this is not the case. The

subtracted reference voltages between the controlled row and the previous row helps to establish a voltage controller interdependency helping to enhance the dynamic performance of the converter. The output of each row's voltage and each row's voltage PI block is sent into a transformation block that provides a relevant reference inductor current value, which is then similarly subtracted by the actual inductor current of the module of interest. This reference inductor current value is established from the relationships drawn by Eqs. (2-1, 2-2, 2-3, 2-4). A second PI block would then process this current difference and provide an output switching signal for its respective module switches, with the design consideration that it must operate much faster (>10 times) than the voltage controller, so that inductor current dynamics are much faster than capacitor voltage dynamics. As mentioned earlier, it is much more desirable for the capacitor voltage be relatively stiff and change more slowly than the current flowing across in the inductors to promote greater converter stability and more dynamic control of the module switches.

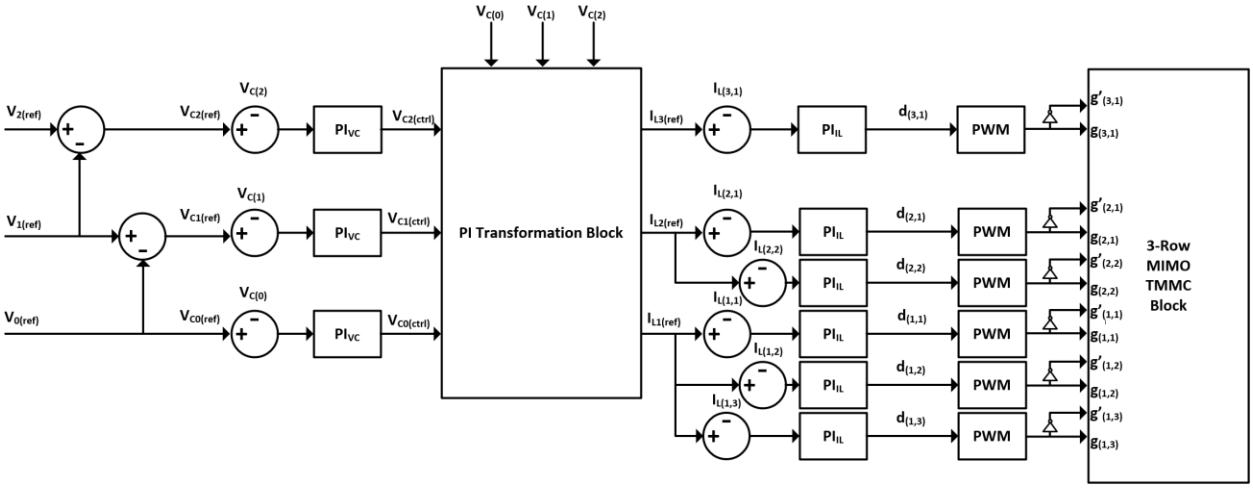

Figure 9. 3-row MIMO TMMC control diagram

2.1.1 State-Space Derivation of Transformation Block

The controller transformation block shown in Figure 9 that connects the voltage control outer-loop and the current control inner-loop is a very important component of the control system and must be derived based on the number of TMMC converter rows and parallel modules. For the 3-level step-down model used in this work, the transformation block can be derived from the converter's capacitor dynamic equations in (2-1). These equations are first transformed into their state-space representation to simplify the derivation. As a reminder, the top row of the converter (row 3) will be ignored in these equations as its dynamics are directly linked to the relationship of the input voltage and the voltages of the row voltages 0, 1, and 2 per

$$\dot{\bar{v}}_{c_3} = \dot{v}_\iota - \sum_{l=0}^{n-1} \dot{\bar{v}}_{c_{(l)}} \ . \tag{2-5}$$

Transformation Block Derivation using State-Space Representation of Dynamic Equations

Note: The effect of parallel capacitors is shown via b_k – the integer number of parallel modules

$$\begin{bmatrix} b_1 C \dot{\bar{v}}_{c_0} \\ b_1 C \dot{\bar{v}}_{c_1} \\ b_2 C \dot{\bar{v}}_{c_2} \end{bmatrix} = \begin{bmatrix} \sum_{j=1}^{b_1} \bar{\iota}_{L_{1,j}} - \sum_{j=1}^{b_2} \bar{\iota}_{L_{2,j}}(1 - d_{2,j}) - b_1 C \dot{\bar{v}}_{c_1} - i_0 \\ -\sum_{j=1}^{b_1} \bar{\iota}_{L_{1,j}} d_{1,j} + \sum_{j=1}^{b_2} \bar{\iota}_{L_{2,j}} - \sum_{j=1}^{b_3} \bar{\iota}_{L_{3,j}}(1 - d_{3,j}) - b_2 C \dot{\bar{v}}_{c_2} + \sum_{j=1}^{b_1} i_{ESS_{1,j}} - i_1 \\ -\sum_{j=1}^{b_2} \bar{\iota}_{L_{2,j}} d_{2,j} + \sum_{j=1}^{b_3} \bar{\iota}_{L_{3,j}} - b_3 C \left(\dot{v}_\iota - \sum_{l=0}^{n-1} \dot{\bar{v}}_{c_{(l)}} \right) + \sum_{j=1}^{b_2} i_{ESS_{2,j}} - i_2 \end{bmatrix}$$

Create Matrix, W_m, from b_k terms, which indicate the number of parallel modules per rows (v_{c0}, v_{c1}, v_{c2})

$$\begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix}\begin{bmatrix} C\dot{\bar{v}}_{c_0} \\ C\dot{\bar{v}}_{c_1} \\ C\dot{\bar{v}}_{c_2} \end{bmatrix} = \begin{bmatrix} \sum_{j=1}^{b_1} \bar{\imath}_{L_{1,j}} - \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}}(1-d_{2,j}) - b_1 C\dot{\bar{v}}_{c_1} - i_0 \\ -\sum_{j=1}^{b_1} \bar{\imath}_{L_{1,j}} d_{1,j} + \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} - \sum_{j=1}^{b_3} \bar{\imath}_{L_{3,j}}(1-d_{3,j}) - b_2 C\dot{\bar{v}}_{c_2} + \sum_{j=1}^{b_1} i_{ESS_{1,j}} - i_1 \\ -\sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} d_{2,j} + \sum_{j=1}^{b_3} \bar{\imath}_{L_{3,j}} - b_3 C\left(\dot{v}_i - \sum_{l=0}^{n-1} \dot{\bar{v}}_{c_{(l)}}\right) + \sum_{j=1}^{b_2} i_{ESS_{2,j}} - i_2 \end{bmatrix},$$

$$where\ W_m = \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix}$$

Extract Disturbance Terms (Source, Loads, ESS) and Adjacent Capacitor Terms ($b_{k+1}C\dot{\bar{v}}_{c_{k+1}}$), and form own Matrices:

Note: Sources/Loads only impact disturbance terms hence why they should be separated

$$\begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix}\begin{bmatrix} C\dot{\bar{v}}_{c_0} \\ C\dot{\bar{v}}_{c_1} \\ C\dot{\bar{v}}_{c_2} \end{bmatrix}$$

$$= \begin{bmatrix} \sum_{j=1}^{b_1} \bar{\imath}_{L_{1,j}} - \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}}(1-d_{2,j}) \\ -\sum_{j=1}^{b_1} \bar{\imath}_{L_{1,j}} d_{1,j} + \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} - \sum_{j=1}^{b_3} \bar{\imath}_{L_{3,j}}(1-d_{3,j}) \\ -\sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} d_{2,j} + \sum_{j=1}^{b_3} \bar{\imath}_{L_{3,j}} \end{bmatrix} - \begin{bmatrix} b_1 C\dot{\bar{v}}_{c_1} \\ b_2 C\dot{\bar{v}}_{c_2} \\ -b_3 C\sum_{l=0}^{n-1} \dot{\bar{v}}_{c_{(l)}} \end{bmatrix} + \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 3 & 0 & 0 \\ 0 & -C & 0 & 0 & -1 & 0 & 2 & 0 \end{bmatrix}\begin{bmatrix} v_i \\ \dot{v}_i \\ i_0 \\ i_1 \\ i_2 \\ i_{ESS_1} \\ i_{ESS_2} \\ i_{ESS_3} \end{bmatrix}$$

Extract duty cycle relationships and create matrix, M_d, from them:

Note: Duty cycles of parallel modules are assumed to be equal, and therefore, $d_{k,j} = d_k$

$$\begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix} \begin{bmatrix} C\dot{\bar{v}}_{c_0} \\ C\dot{\bar{v}}_{c_1} \\ C\dot{\bar{v}}_{c_2} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix} \begin{bmatrix} \sum_{j=1}^{b_1} \bar{\imath}_{L_{1,j}} + \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} \\ \sum_{j=1}^{b_1} \bar{\imath}_{L_{1,j}} + \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} + \sum_{j=1}^{b_3} \bar{\imath}_{L_{3,j}} \\ \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} + \sum_{j=1}^{b_3} \bar{\imath}_{L_{3,j}} \end{bmatrix} - \begin{bmatrix} b_1 C\dot{\bar{v}}_{c_1} \\ b_2 C\dot{\bar{v}}_{c_2} \\ -b_3 C \sum_{l=0}^{n-1} \dot{\bar{v}}_{c_{(l)}} \end{bmatrix}$$

$$+ \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 3 & 0 & 0 \\ 0 & -C & 0 & 0 & -1 & 0 & 2 & 0 \end{bmatrix} \begin{bmatrix} v_i \\ \dot{v}_i \\ i_0 \\ i_1 \\ i_2 \\ i_{ESS_1} \\ i_{ESS_2} \\ i_{ESS_3} \end{bmatrix}, \qquad where\ M_d = \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix}$$

Add $b_{k+1} C\dot{\bar{v}}_{c_{k+1}}$ terms to both sides:

$$\begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix} \begin{bmatrix} C\dot{\bar{v}}_{c_0} \\ C\dot{\bar{v}}_{c_1} \\ C\dot{\bar{v}}_{c_2} \end{bmatrix} + \begin{bmatrix} b_1 C\dot{\bar{v}}_{c_1} \\ b_2 C\dot{\bar{v}}_{c_2} \\ -b_3 C \sum_{l=0}^{n-1} \dot{\bar{v}}_{c_{(l)}} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix} \begin{bmatrix} \sum_{j=1}^{b_1} \bar{\imath}_{L_{1,j}} + \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} \\ \sum_{j=1}^{b_1} \bar{\imath}_{L_{1,j}} + \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} + \sum_{j=1}^{b_3} \bar{\imath}_{L_{3,j}} \\ \sum_{j=1}^{b_2} \bar{\imath}_{L_{2,j}} + \sum_{j=1}^{b_3} \bar{\imath}_{L_{3,j}} \end{bmatrix} + \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 3 & 0 & 0 \\ 0 & -C & 0 & 0 & -1 & 0 & 2 & 0 \end{bmatrix} \begin{bmatrix} v_i \\ \dot{v}_i \\ i_0 \\ i_1 \\ i_2 \\ i_{ESS_1} \\ i_{ESS_2} \\ i_{ESS_3} \end{bmatrix},$$

$$where\ M_d = \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix}$$

Create Matrix, Q_m, from added $b_{k+1}C\dot{\bar{v}}_{c_{k+1}}$ terms:

$$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ -\frac{b_3}{b_1} & -\frac{b_3}{b_1} & \frac{b_2-b_3}{b_2} \end{bmatrix}\begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix}\begin{bmatrix} C\dot{\bar{v}}_{c_0} \\ C\dot{\bar{v}}_{c_1} \\ C\dot{\bar{v}}_{c_2} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix}\begin{bmatrix} \sum_{j=1}^{b_1}\bar{\imath}_{L_{1,j}} + \sum_{j=1}^{b_2}\bar{\imath}_{L_{2,j}} \\ \sum_{j=1}^{b_1}\bar{\imath}_{L_{1,j}} + \sum_{j=1}^{b_2}\bar{\imath}_{L_{2,j}} + \sum_{j=1}^{b_3}\bar{\imath}_{L_{3,j}} \\ \sum_{j=1}^{b_2}\bar{\imath}_{L_{2,j}} + \sum_{j=1}^{b_3}\bar{\imath}_{L_{3,j}} \end{bmatrix} + \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 3 & 0 & 0 \\ 0 & -C & 0 & 0 & -1 & 0 & 2 & 0 \end{bmatrix}\begin{bmatrix} v_i \\ \dot{v}_i \\ i_0 \\ i_1 \\ i_2 \\ i_{ESS_1} \\ i_{ESS_2} \\ i_{ESS_3} \end{bmatrix},$$

$$where\ Q_m = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ -\frac{b_3}{b_1} & -\frac{b_3}{b_1} & \frac{b_2-b_3}{b_2} \end{bmatrix}$$

Remove summation signs and create [3x3] i_L matrix:

Note: According to the assumption that each parallel module shares the same current: $i_{L_{k,j}} = i_{L_k}$

$$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ -\frac{b_3}{b_1} & -\frac{b_3}{b_1} & \frac{b_2-b_3}{b_2} \end{bmatrix}\begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix}\begin{bmatrix} C\dot{\bar{v}}_{c_0} \\ C\dot{\bar{v}}_{c_1} \\ C\dot{\bar{v}}_{c_2} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix}\begin{bmatrix} b_1 i_{L_1} & b_2 i_{L_2} & 0 \\ b_1 i_{L_1} & b_2 i_{L_2} & b_3 i_{L_3} \\ 0 & b_2 i_{L_2} & b_3 i_{L_3} \end{bmatrix} + \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 3 & 0 & 0 \\ 0 & -C & 0 & 0 & -1 & 0 & 2 & 0 \end{bmatrix}\begin{bmatrix} v_i \\ \dot{v}_i \\ i_0 \\ i_1 \\ i_2 \\ i_{ESS_1} \\ i_{ESS_2} \\ i_{ESS_3} \end{bmatrix}$$

Define/isolate I_{Lref} terms per row by extracting matrix, Z_m – the number parallel modules per I_{Lref} row

Note: This can be performed according to the assumption that each module's inductor current equals its inductor current reference in equilibrium: $i_{L_k} \approx i_{L_k}^{ref}$. Furthermore, $\frac{di_{L_k}^{ref}}{dt} \approx 0$. To facilitate controller design, the outer loop (voltage controller) is designed to be much slower than the inner loop (current controller) by at least >10x. This makes the outer loop see the inner loop as infinitely fast and decouples their operation. The inner loop system can be approximated as an ideal current source with a magnitude of $i_{L_k}^{ref}$

$$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ -\frac{b_3}{b_1} & -\frac{b_3}{b_1} & \frac{b_2 - b_3}{b_2} \end{bmatrix} \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix} \begin{bmatrix} C\dot{\vec{v}}_{c_0} \\ C\dot{\vec{v}}_{c_1} \\ C\dot{\vec{v}}_{c_2} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix} \begin{bmatrix} \boxed{\boldsymbol{b_1 i_{L_1}}} & b_2 i_{L_2} & 0 \\ b_1 i_{L_1} & \boxed{\boldsymbol{b_2 i_{L_2}}} & b_3 i_{L_3} \\ 0 & b_2 i_{L_2} & \boxed{\boldsymbol{b_3 i_{L_3}}} \end{bmatrix} + \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 3 & 0 & 0 \\ 0 & -C & 0 & 0 & -1 & 0 & 2 & 0 \end{bmatrix} \begin{bmatrix} v_i \\ \dot{v}_i \\ i_0 \\ i_1 \\ i_2 \\ i_{ESS_1} \\ i_{ESS_2} \\ i_{ESS_3} \end{bmatrix}$$

$$= \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix} \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_2 & 0 \\ 0 & 0 & b_3 \end{bmatrix} \begin{bmatrix} i_{L_1}^{ref} \\ i_{L_2}^{ref} \\ i_{L_3}^{ref} \end{bmatrix} + \begin{bmatrix} 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 3 & 0 & 0 \\ 0 & -C & 0 & 0 & -1 & 0 & 2 & 0 \end{bmatrix} \begin{bmatrix} v_i \\ \dot{v}_i \\ i_0 \\ i_1 \\ i_2 \\ i_{ESS_1} \\ i_{ESS_2} \\ i_{ESS_3} \end{bmatrix},$$

$$where\ Z_m = \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_2 & 0 \\ 0 & 0 & b_3 \end{bmatrix}$$

Remove Disturbance Terms as their dynamics cannot be controlled by the controller

Note: Connected sources/loads/ESS affect only the disturbance terms and cannot be controlled by the converter controller; and therefore, are neglected from the I_L-V_C relationship derivation

$$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ -\frac{b_3}{b_1} & -\frac{b_3}{b_1} & \frac{b_2 - b_3}{b_2} \end{bmatrix} \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix} \begin{bmatrix} C\dot{\vec{v}}_{c_0} \\ C\dot{\vec{v}}_{c_1} \\ C\dot{\vec{v}}_{c_2} \end{bmatrix} = \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix} \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_2 & 0 \\ 0 & 0 & b_3 \end{bmatrix} \begin{bmatrix} i_{L_1}^{ref} \\ i_{L_2}^{ref} \\ i_{L_3}^{ref} \end{bmatrix}$$

Rearrange the equation to isolate $\boldsymbol{i_L^{ref}}$ terms

$$\begin{bmatrix} \bar{i}_{L_1}^{ref} \\ \bar{i}_{L_2}^{ref} \\ \bar{i}_{L_3}^{ref} \end{bmatrix} = \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_2 & 0 \\ 0 & 0 & b_3 \end{bmatrix}^{-1} \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix}^{-1} \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ -\frac{b_3}{b_1} & -\frac{b_3}{b_1} & \frac{b_2-b_3}{b_2} \end{bmatrix} \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix} \begin{bmatrix} C\dot{\bar{v}}_{c_0} \\ C\dot{\bar{v}}_{c_1} \\ C\dot{\bar{v}}_{c_2} \end{bmatrix},$$

$$where\ T_{dm}^{-1} = M_d^{-1} Q_m = \begin{bmatrix} 1 & -(1-\widehat{d_2}) & 0 \\ -\widehat{d_1} & 1 & -(1-\widehat{d_3}) \\ 0 & -\widehat{d_2} & 1 \end{bmatrix}^{-1} \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ -\frac{b_3}{b_1} & -\frac{b_3}{b_1} & \frac{b_2-b_3}{b_2} \end{bmatrix}$$

Therefore, the equation is simplified to:

$$\begin{bmatrix} \bar{i}_{L_1}^{ref} \\ \bar{i}_{L_2}^{ref} \\ \bar{i}_{L_3}^{ref} \end{bmatrix} = \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_2 & 0 \\ 0 & 0 & b_3 \end{bmatrix}^{-1} T_{dm}^{-1} \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix} \begin{bmatrix} C\dot{\bar{v}}_{c_0} \\ C\dot{\bar{v}}_{c_1} \\ C\dot{\bar{v}}_{c_2} \end{bmatrix}$$

The capacitor dynamics of each row are directly linked to the output of the outer-loop voltage controller as well as the corresponding $\boldsymbol{i_L^{ref}}$ term, and therefore, $\boldsymbol{C\dot{\bar{v}}_{c_k} \approx v_{c_k}^{ctrl}}$:

$$\begin{bmatrix} \bar{i}_{L_1}^{ref} \\ \bar{i}_{L_2}^{ref} \\ \bar{i}_{L_3}^{ref} \end{bmatrix} = \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_2 & 0 \\ 0 & 0 & b_3 \end{bmatrix}^{-1} T_{dm}^{-1} \begin{bmatrix} b_1 & 0 & 0 \\ 0 & b_1 & 0 \\ 0 & 0 & b_2 \end{bmatrix} \begin{bmatrix} v_{c_0}^{ctrl} \\ v_{c_1}^{ctrl} \\ v_{c_2}^{ctrl} \end{bmatrix}$$

… which equals the desired Transformation Block relationship

$$\boxed{\begin{bmatrix} i_{L_1}^{ref} \\ i_{L_2}^{ref} \\ i_{L_3}^{ref} \end{bmatrix} = Z_m^{-1} T_{dm}^{-1} W_m \begin{bmatrix} v_{c_0}^{ctrl} \\ v_{c_1}^{ctrl} \\ v_{c_2}^{ctrl} \end{bmatrix}}$$

2.2 Development of TMMC-APDN Simulation Model

The traditional single-input, single-output (SISO) TMMC is transformed into a two-input, two-output MIMO TMMC via an additional output resistor – identical to the output row resistor – placed below the top row of modules, and an additional controlled current source input – equal to current flowing through the second row – placed above the bottom row of modules. With the addition of a robust control system (a PI voltage controller per row fed into a PI current controller per module) and an ESS power buffering solution, the TMMC's power sharing attribute can be maintained for multiple inputs and/or outputs. Applications incorporating energy storage within MMC topologies for high power applications have already been explored [37], [39] with battery technologies in order to help meet a growing need for load leveling and power buffering. Within the proposed circuit design, power buffering is achieved by attaching an ultracapacitor to each of the TMMC's modules via an interfacing dual-quadrant Type-C Chopper circuit. With the intermittency of renewable generation sources like solar, it is preferable to utilize an energy storage solution that provides quick discharges of power while subsequently recharging quickly. Ultracapacitors are a good fit for such an application with a high-power density profile to compensate for deficits in power output, the capability for quick charge and discharge cycling, and a long lifespan. Future designs of this APDN topology would benefit from a hybrid energy storage solution with ultracapacitors handling power deficits in the seconds to minutes range and batteries mitigating power deficits in the minutes to hours range. This hybrid approach would extend the power buffering capabilities of the converter and allow for both temporary and long-term losses of power within a distribution network.

All modeling and testing of 3-level TMMCs is performed in MATLAB Simulink with the step-down configuration of the converter. This configuration was selected to replicate the converter's connection to a 380 Vdc system. The TMMC requires one of its sources to serve as a "slack bus" for all other connected inputs and outputs, and for this work, this "bus" is selected as the 380 V connection to represent a use case in ICT and other DC distribution systems. The high-side input voltage of 380 V is selected for its adopted use in DC distribution networks, with each *n* row holding one-fourth of that voltage, 95 V, roughly twice the common DC voltage of 48 V. This topology could be expanded by adding more rows to more closely achieve 48 V per row, but the overall principles of the converter remain the same regardless of the number of rows.

With the hybrid energy storage solution enabling power buffering, a DC-DC interface between the ESS and the TMMC modules is required. This converter must operate as a two-quadrant device with bi-directional current flow in order to both charge and discharge the ultracapacitor, as well as be easily controllable to allow for the simple selection between charging and discharging operations. A Type-C chopper DC-DC Converter, also referred to as a Buck and Boost converter, can achieve both functionalities and was selected as the interfacing topology between the ultracapacitor and the TMMC modules. Chopper circuits interface sources and loads and are static power electronic devices used to convert fixed DC power to variable DC power by means of high-speed switches connecting and disconnecting from a specified load. Their operation allows for connected sources and loads to operate in both single-quadrant or multi-quadrant regions based on the configuration of switches and their impact on the flow of power. The four quadrants are denoted by voltage (y-axis), current (x-axis), and their respective polarities as shown in Figure 10, which ultimately dictate the directional flow of power. There are five types of choppers, labeled A through E, but the main focus of this research focuses on the Type-C chopper,

which combines the functionality of both the Type-A chopper (unidirectional, first quadrant) and the Type-B chopper (unidirectional, second quadrant), in order to achieve bi-directional, dual quadrant power flow (first and second quadrant). The Type-C chopper topology connected to an ultracapacitor is shown below in Figure 11.

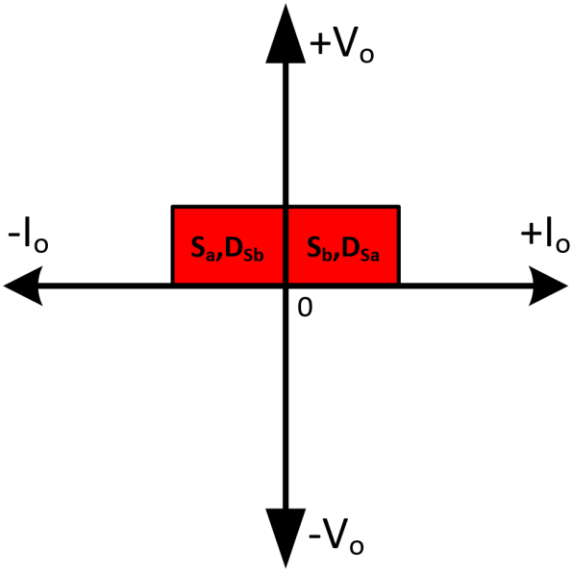

Figure 10. First and second quadrant operation of the Type-C chopper with depicted switching states of MOSFETs and body diodes

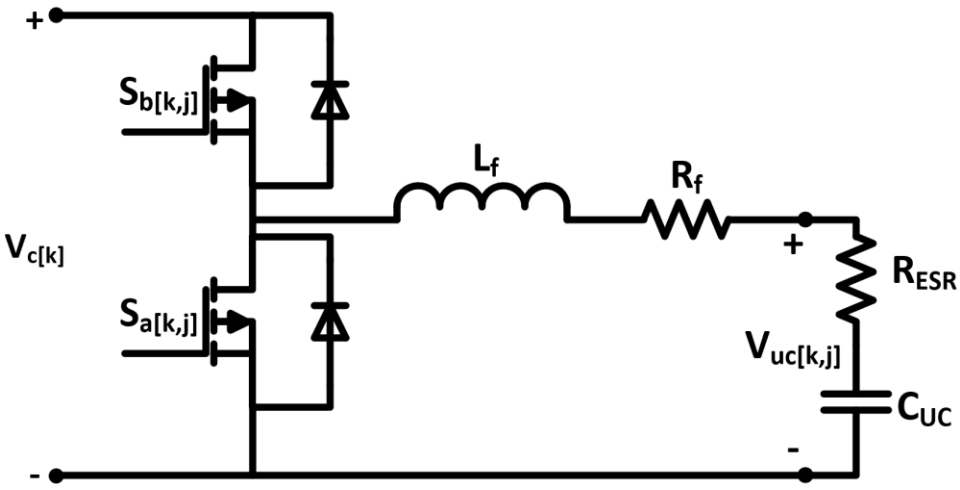

Figure 11. Type-C chopper bidirectional dc-dc converter connected to an ultracapacitor

For the Type-C chopper's proper interfacing of the module and the ESS, the module capacitor voltage, V_C, must always be greater than the voltage across the ESS, V_{ESS}. This voltage bias ensures the proper flow of current from high side to low side, and vice versa. As such, with an average module capacitor voltage of 95 V, the ESS voltage was designed for 48 V – a roughly 2:1 ratio of voltages. The Type-C chopper can effectively operate as both a buck converter and a boost converter based on proper switch activation. Each switch utilizes a body or freewheeling diode for when it is not actively in operation. By controlling the bottom switch, S_a, and keeping the top switch, S_b, open, the converter is in "boost" or "discharging" mode with power flowing from the ESS to the connected module; conversely, by controlling the top switch, S_b, and keeping the bottom switch, S_a, open, the converter is in "buck" or "charging" mode with power flowing from the connected module to the ESS. Both operating modes are depicted in Figure 12 and Figure 13, respectively.

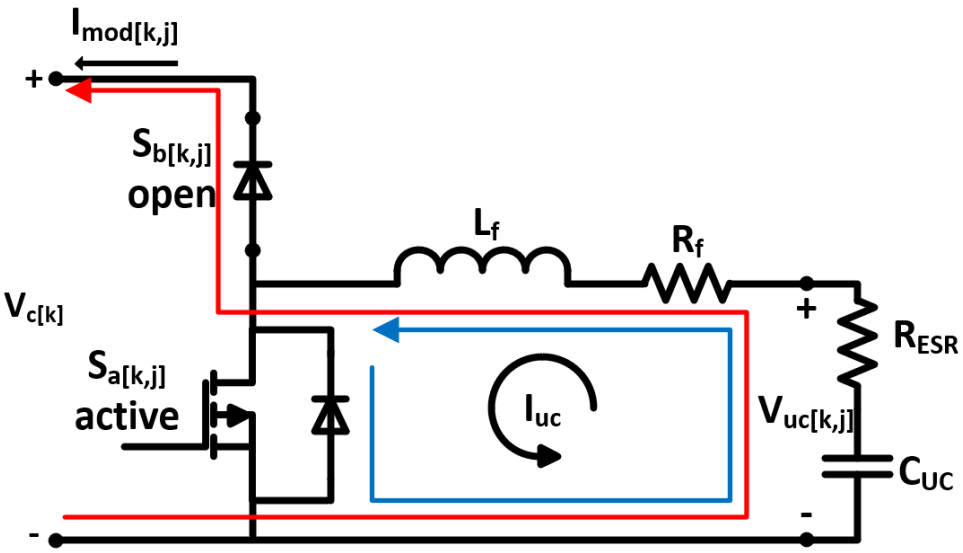

Figure 12. Boost or Discharging Mode Operation of the Type-C Chopper
Red line: Switch Sa open; Blue line: Switch Sa closed

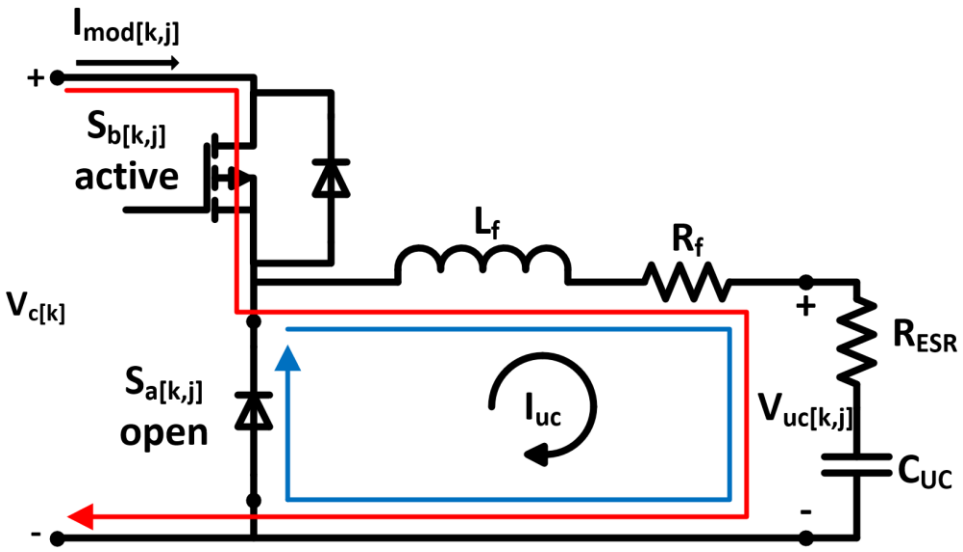

Figure 13. Buck or Charging Mode Operation of the Type-C Chopper
Red line: Switch S_b closed; Blue line: Switch S_b open

Per the state machine Simulink diagram in Figure 14 and Figure 15, the chopper circuit begins in a neutral mode of operation with the voltage of the module capacitor falling in between two defined thresholds of 94.5 V and 95.5 V. Neither of the two switches in the interfacing chopper converter are triggered in this state. In the event of a system perturbation leading to the TMMC module voltage crossing either threshold, the state machine shifts modes from the neutral state to either the buck state or the boost state in order to regulate the voltage and bring it back between the thresholds more quickly. If the module voltage drops below the lower threshold, the interface converter enters its discharging (boost) state, effectively raising the voltage of the module capacitor by discharging the attached ESS per Figure 12. The bottom switch of the interface converter is triggered for this state. Similarly, if the voltage exceeds the upper threshold, the converter enters its charging (buck) state, effectively lowering the voltage of the module capacitor by charging the ESS per Figure 13. The upper switch of the interfacing converter is triggered for this state. The state machine's cycle of operation is demonstrated by the algorithm's flow chart in Figure 16.

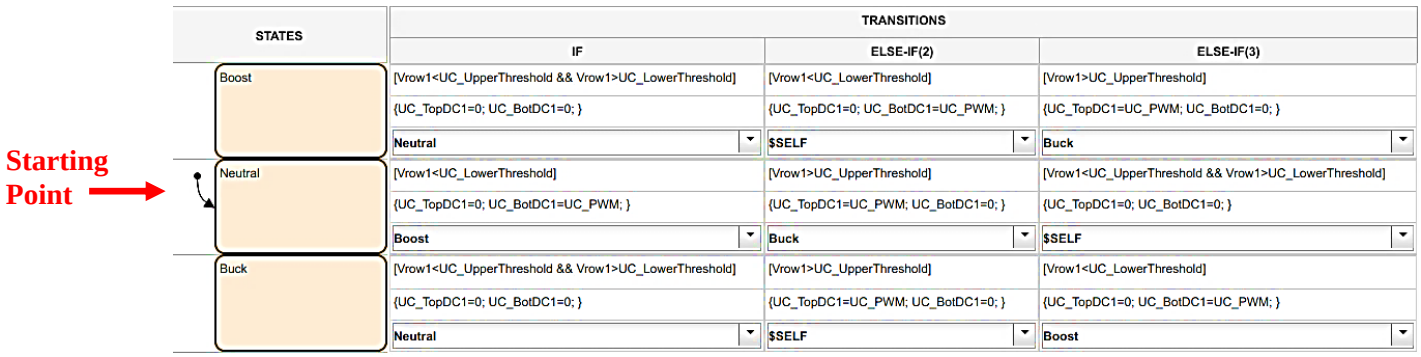

Figure 14. ESS Row Voltage Threshold Balance Algorithm

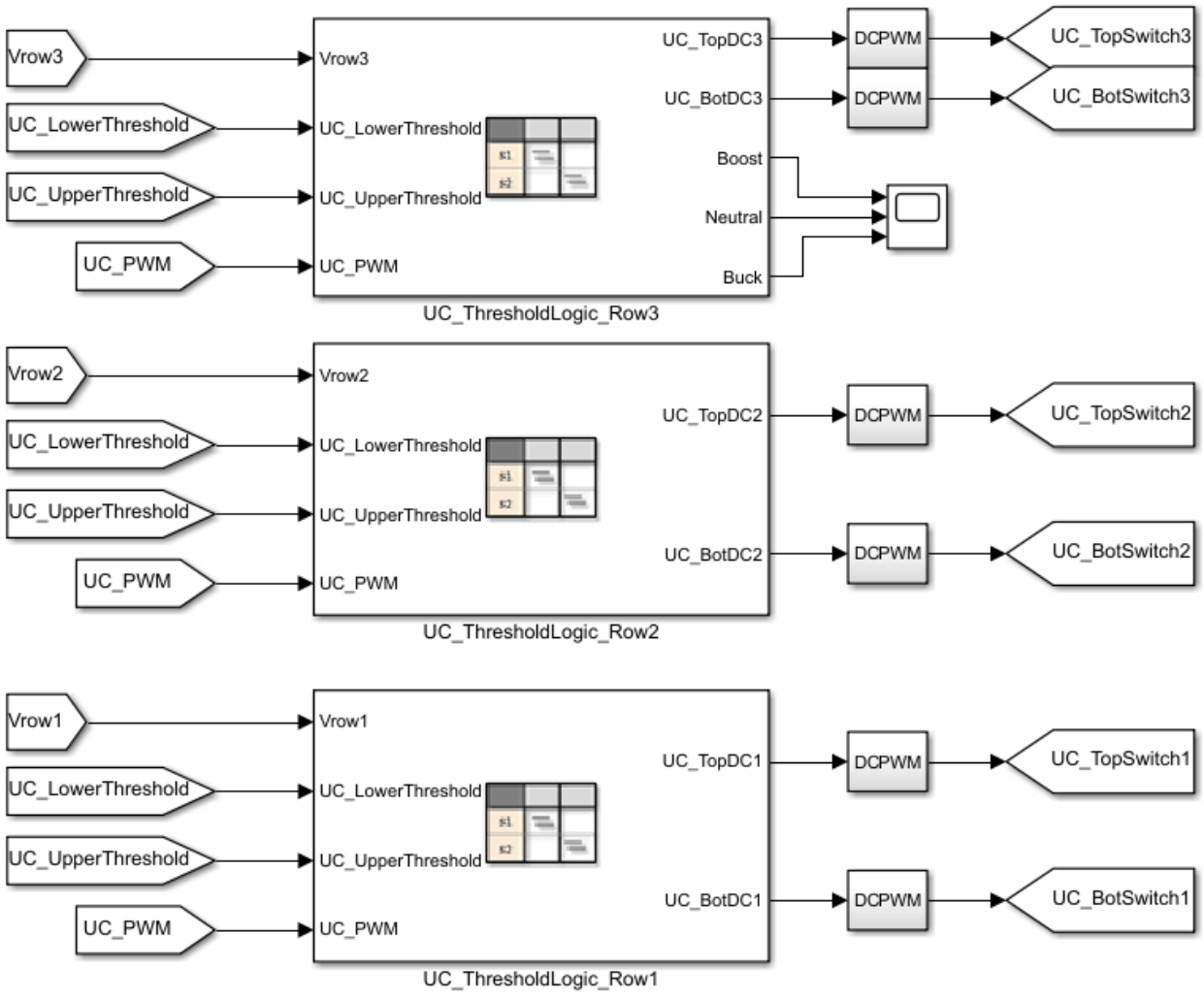

Figure 15. ESS Control Structure including Algorithm

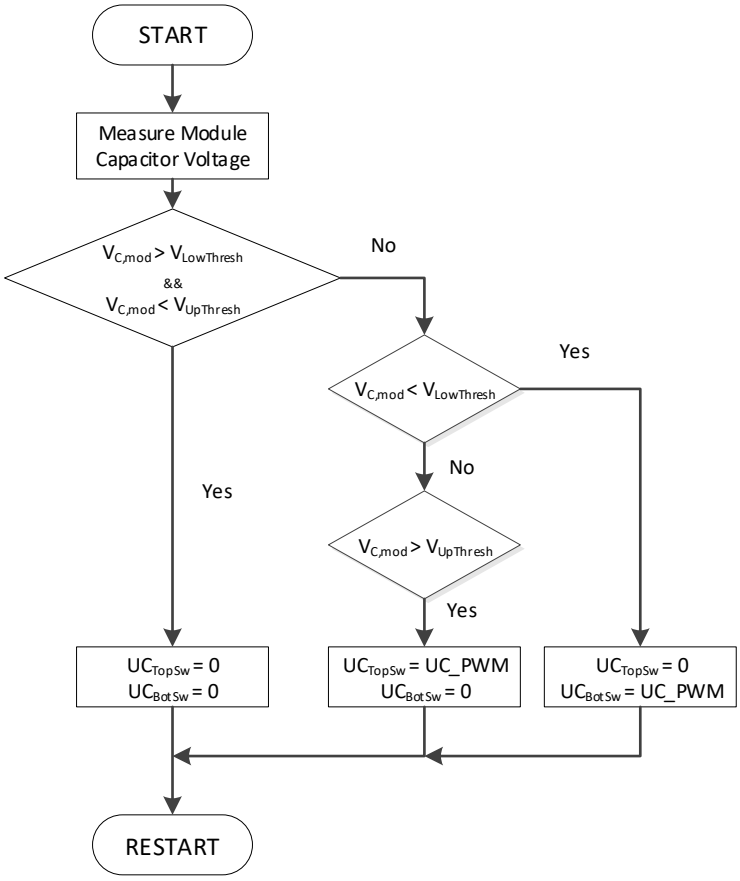

Figure 16. ESS Row Voltage Threshold Balance Algorithm Flow Chart

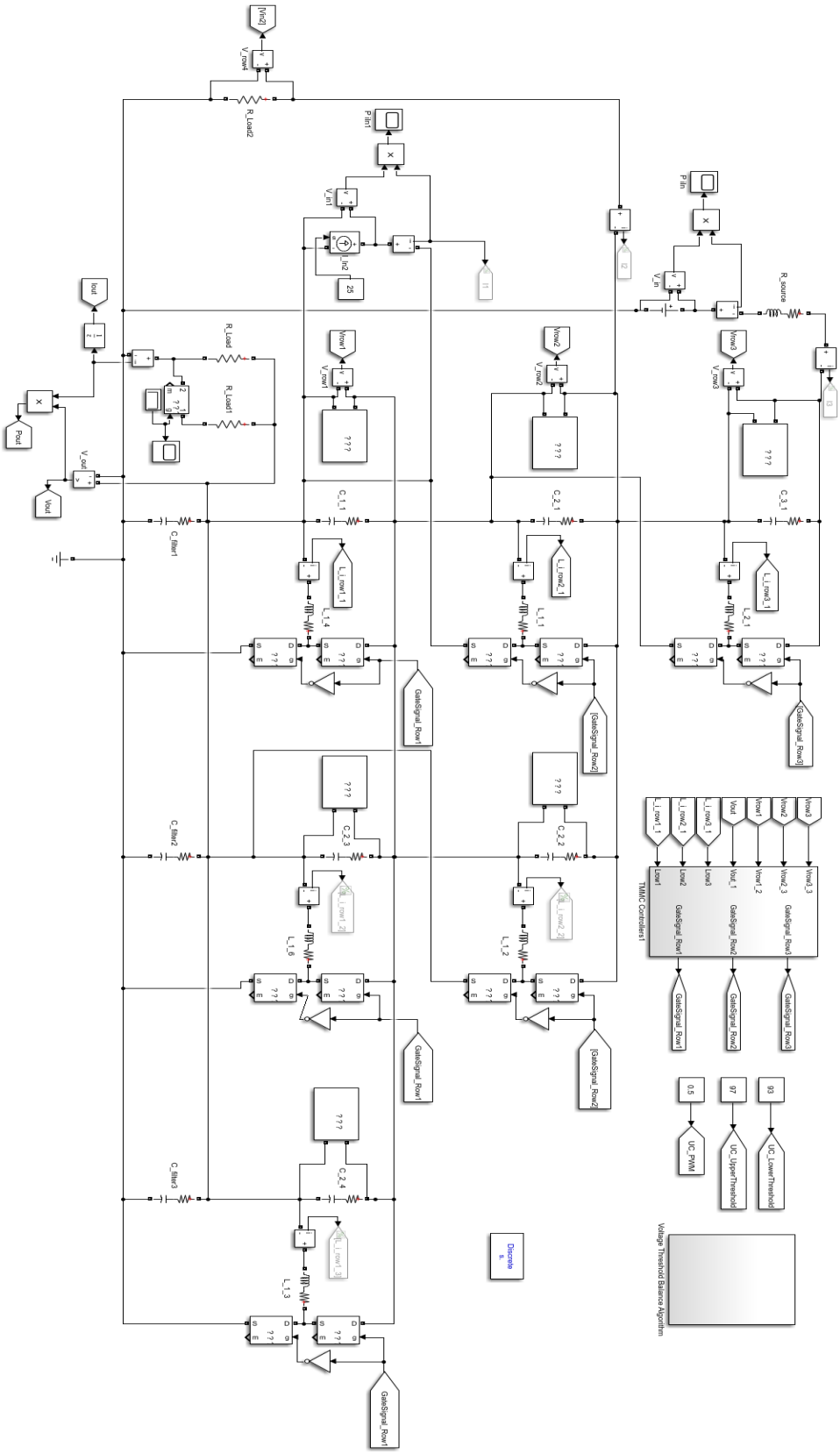

Figure 17. MIMO TMMC-APDN Simulink Simulation Model

Figure 18 showcases results of a 500 ms simulation of the three-row MIMO TMMC-APDN seen in Figure 17. At 167 ms and 333 ms, respectively, the bottom-most output load power demand is doubled from 1128 W to 2256 W and then subsequently returned to its nominal value. The simulation results demonstrate stability across all (*n+1*) rows of the converter with voltages of all three module rows and the bottom-most output row close to the desired 95 V. However, the total simulation described takes 8107 s (2 hours and 15 minutes) to complete. The simulation time is expected to grow linearly as more APDNs are placed on the test system, which could prove difficult to simulate efficiently. As an exercise to explore alternative ways to cut down on the computational load, two averaged modeling techniques were used to simulate a TMMC, while retaining each converter's dynamic performance.

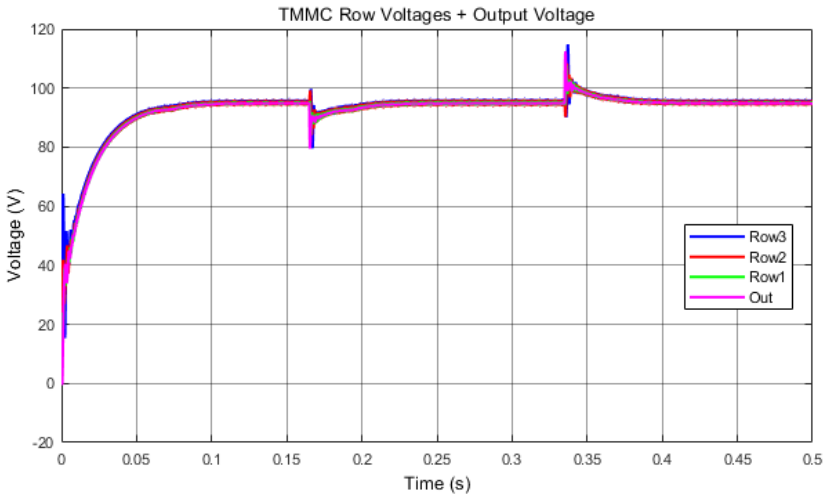

Figure 18. Three-level MIMO TMMC switched electrical model results with ultracapacitor energy storage providing transient support – TMMC row and (bottom) output voltages

2.3 Averaged Modeling of the TMMC Topology

The bulk of the model complexity and computational load stems from the cascaded switching model dynamics between the TMMC modules and their dedicated controllers' pulse-width modulators (PWM), and the interfacing bi-directional buck-and-boost converters used for controlling the ultracapacitors connected to each module. Each converter switching model solves differential equations at a specified simulation time step, incurring switching ripple and a heavy simulation time burden. Literature demonstrates that by deriving averaged equivalents of each converter, both the switching ripple and computational load is significantly reduced, benefitting system simulation time [40], [41]. Two main approaches for averaging the dynamics of the TMMC buck-boost modules are investigated: 1) a purely mathematical state-space representation of buck-boost converter dynamics [42], and 2) a hybrid equivalent circuit model using controlled current sources [43]. Each technique is used to reconstruct the TMMC with averaged buck-boost modules in place of their electrical component-derived counterparts and each is compared to a switched electrical model of the converter. As the full ESS-enhanced MIMO TMMC is computationally intensive, all three simulations will comprise a three-row SISO TMMC without ESS. These results will give a reference frame for the performance of each converter modeling technique. Additionally, the damping Q-factor of the parallel RLC circuit of each approximated model is tuned to the switched electrical model, facilitating direct comparisons, by adjusting the source inductance of the system input per

$$Q = R\sqrt{\frac{C}{L}}. \tag{2-6}$$

The state-space averaged buck-boost converter derivation follows the traditional switched state analysis in continuous conduction mode (CCM) with the averaging of the A and B state-space matrices. The procedure is detailed more thoroughly in [42]. The state-space matrices describe the averaged input and output dynamics of the buck-boost converter relative to their duty cycle and circuit elements as shown in Eqs. (2-7) and (2-8),

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \end{bmatrix} = \begin{bmatrix} 0 & 1 - d/L \\ -1 - d/C & -1/RC \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \frac{d}{L} \\ 0 \end{bmatrix} V_{in} \tag{2-7}$$

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{in} . \tag{2-8}$$

The full state-space model shown in Figure 20 utilizes Simulink state-space blocks per Figure 19 with the dynamics from (2-7) and (2-8) and consists of three TMMC converter rows plus one output row. Each row can be equipped with a separate input and/or have its output, R, adjusted to replicate MIMO behavior. As a purely mathematical representation of the converter topology, the Q-factor of the converter was tuned with an added "source inductor" summed to the inductance of the top row's state-space block.

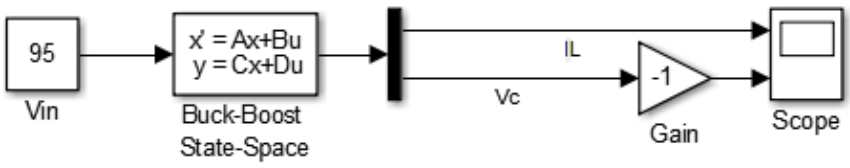

Figure 19. State-Space Averaged Model of TMMC Buck-Boost Module

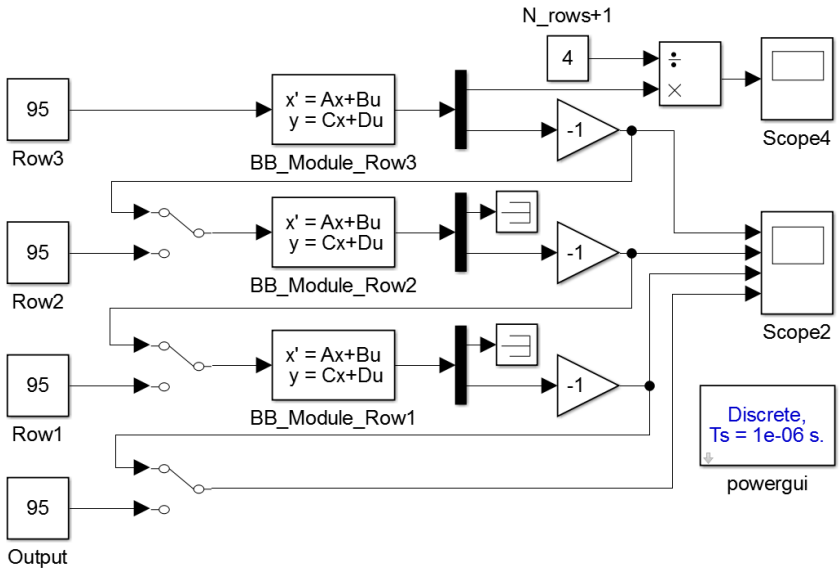

Figure 20. Three-level TMMC sate-space model with adjustable inputs to the each state-space block and adjustable outputs within each state-space block

The development of the state-space TMMC model comes with the benefit of having a reduced simulation time, however, this model is unable to inherently operate bi-directionally nor directly interface with an electrical system. Therefore, the next goal is to pursue the hybrid equivalent circuit model for the TMMC following the approach described in [43], which utilizes controlled input and output current sources in place of converter switches as shown in Figure 21. This model utilizes the state-space analysis described previously to develop the CCM averaged nonlinear large-signal models in Eqs. (2-9) and (2-10),

$$\begin{aligned} \overline{i_L} &= I_{ref} - \frac{1}{2}DT\left(2m + \frac{v_{in}}{L}\right) \\ \overline{i_L} &= I_{ref} - \frac{1}{2}\left(\frac{\overline{v_c}}{v_{in} + \overline{v_c}}\right)T\left(2m + \frac{v_{in}}{L}\right) \end{aligned} \tag{2-9}$$

$$\begin{aligned} \frac{d\overline{v_c}}{dt} &= \frac{1}{C}(1 - D)i_L - \frac{\overline{v_c}}{RC} \\ \frac{d\overline{v_c}}{dt} &= \frac{1}{C}\left(\frac{v_{in}}{v_{in} + \overline{v_c}}\right)i_L - \frac{\overline{v_c}}{RC}, \end{aligned} \tag{2-10}$$

where *m* is the slope of the controller's current compensation ramp. This equivalent circuit method replicates the performance of the fundamental DC-DC converters (buck, boost, and buck-boost) by segmenting them into their input and output current stages governed by averaged controlled current sources. By eliminating all current control elements (switches and inductors) in favor of emulating their dynamics mathematically, the computation time related to switching dynamics is greatly reduced.

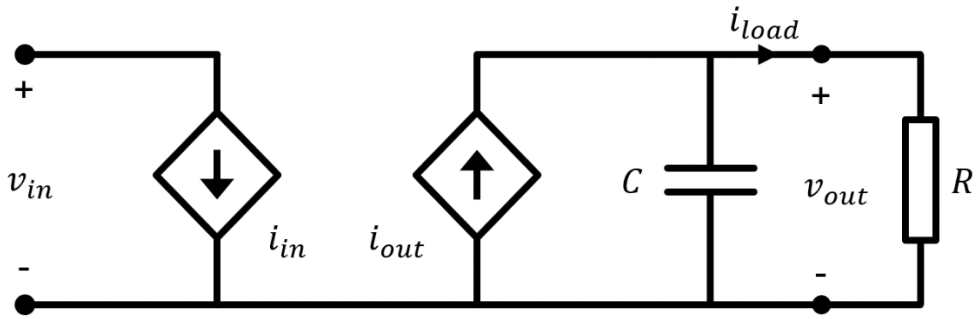

Figure 21. Equivalent circuit TMMC buck-boost module topology

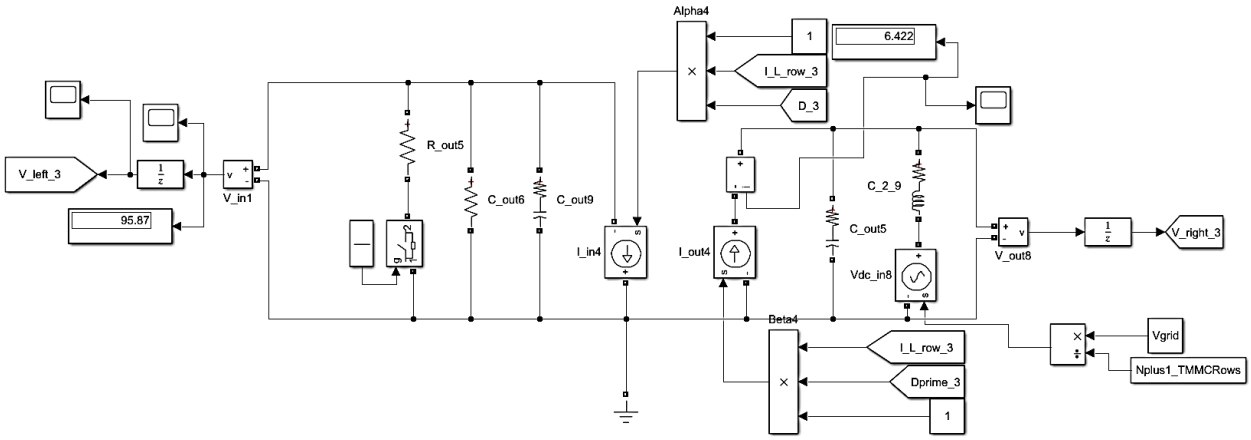

Figure 22. Equivalent circuit TMMC buck-boost module Simulink Model

Recreating the TMMC using the equivalent circuit model extends the design principle of the state-space TMMC model. Each row of the converter is modeled individually with the required number of parallel modules per row connected via their output stage's positive rail with an example

of the Simulink model seen in Figure 22. Each row is connected to an adjacent row indirectly using controlled voltage sources fed with the voltage signal of the higher or lower adjacent row based on the direction of current flow in the TMMC. Each row of modules utilizes a form of current programmed control with the controlled current sources dynamically updated per the calculated inductor currents in (9) and gain values, α and β, determined by (2-11) and (2-12),

$$\alpha = \frac{\overline{v_c}}{v_{in} + \overline{v_c}} \tag{2-11}$$

$$\beta = \frac{v_{in}}{v_{in} + \overline{v_c}} \tag{2-12}$$

The gains, α and β, are then multiplied by the calculated inductor current to control the input and output current sources, respectively. The I_{ref} term is the upper threshold for the inductor value in (6) and is dynamically updated based on the difference of the reference voltage (95 V) and the controlled row's output voltage. If this difference is greater than +1 V, the I_{ref} term is incremented by 0.5 A. If the difference is less than -1 V, the I_{ref} term is decremented by a 0.5 A. The interdependent relationship between row voltage difference and the updated inductor current reference ensures a stable and dynamic inductor current.

For each method of modeling the SISO TMMC, a 500 ms simulation in MATLAB Simulink is performed at a 1 µs simulation time step and a 100% load step occurring at 250 ms. The load step is achieved by altering the output resistance of the converter from 8 Ω to 4Ω via switching in an additional parallel 8 Ω resistor. The dynamic voltage and current response for all three converter models and the simulation times to completion are evaluated as performance

metrics. Specifically, the voltage and current waveforms for each of the three TMMC module rows and the voltage waveform across the output load are plotted and compared. Each simulation was performed six times with the average simulation time per model configuration calculated for analysis.

Figure 23 contains the voltage waveforms for each modeling technique with all three sets of signals matching closely. The load step's increased power demand dips the worst-case voltage for each model to 47.86 V, 49.46 V, and 41.84 V, respectively. The electrical model has its largest voltage dip on row 3, while its other rows incur a dip closer to the other models around 50 V. As expected, the state-space model resembles the most idealized version of the waveform without losses nor switching dynamics present. The equivalent circuit model showcases more nonlinearities than the state-space while still following the same trajectory. Resistive losses in the output stage of each module and the dedicated output stage at the bottom of the equivalent circuit TMMC are manifested in the form of the output voltage waveform being slightly offset from the rest of the voltage waveforms. Lastly, the switched electrical model showcases the most non-linearities, most notable around the switched load step. The steady state row voltages of each waveform closely match each other and the 95 V target voltage at 95 V, 94.85 V, and 94.90 V, respectively. The output voltages differ more drastically, however, which reflect the way the output row of each converter is simulated with steady state output voltages of 95 V, 94.23 V, and 94.86 V, respectively. The equivalent circuit model's output voltage is farthest from the target voltage due to the placement of the total converter's resistive losses on the output, which are summed together and placed in series along the dedicated output stage of the TMMC.

Figure 24 showcases the inductor current waveforms for each model along each of the three module rows. These plots show more variation and disparity between modeling techniques. The

state-space model continues to demonstrate the idealized mathematical representation of the inductor current dynamics, while the equivalent circuit and the switched electrical models experience the effects of the switched load transient on each module inductor. A much larger transient is evident for the switched electrical model, reflective of dynamics present with stored inductor energy upon switching in the additional load. The steady state inductor currents for each model are 5.94 A and 11.87 A for the state-space model, 5.93 A and 11.89 A for the equivalent circuit model, and 5.94 A and 11.86 A for the switched electrical model – all of which closely match the calculated target values of 5.94 A and 11.88 A. Peak switching transient currents are negligible for the state-space model; however, the maximum transient current is 11.07 A for the equivalent model and 13.66 A for the switched electrical model. Additionally, the switched electrical model incurs a transient dip unlike the other two models and falls to 0.30 A before recovering to a nominal current value.

After performing several simulations runs of each modeling technique at a 1 μs time step, the average simulation times for each model are 5.99 s, 67.96 s, and 98.02 s, respectively. The greatest simulation time improvement comes from the state-space model with a 1536.4% improvement over the switched electrical model, while the equivalent circuit model boasts a 44.2% improvement. Furthermore, the state-space and equivalent circuit models can be run at a larger time step of 10 μs without a loss of dynamic fidelity, unlike the switched electrical model, for additional simulation time savings. At this increased time step, the average simulation times reduce to 4.13 s and 18.46 s, respectively – increasing the improvements to 2273.4% and 430.9%. A summary of all test parameters and results can be found in Table 1.

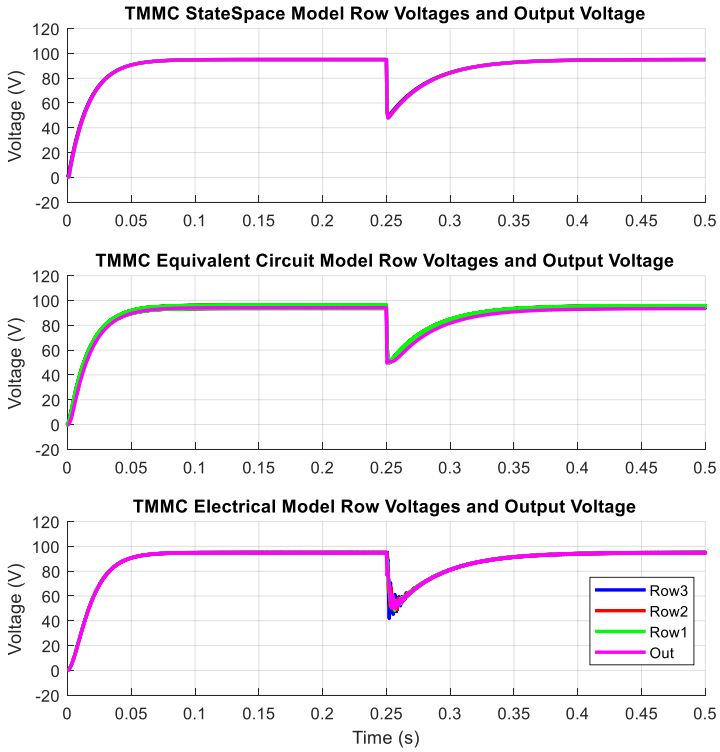

Figure 23. 1 µs time step simulation row / output voltage results (top to bottom: state-space, equivalent circuit, switched electrical)

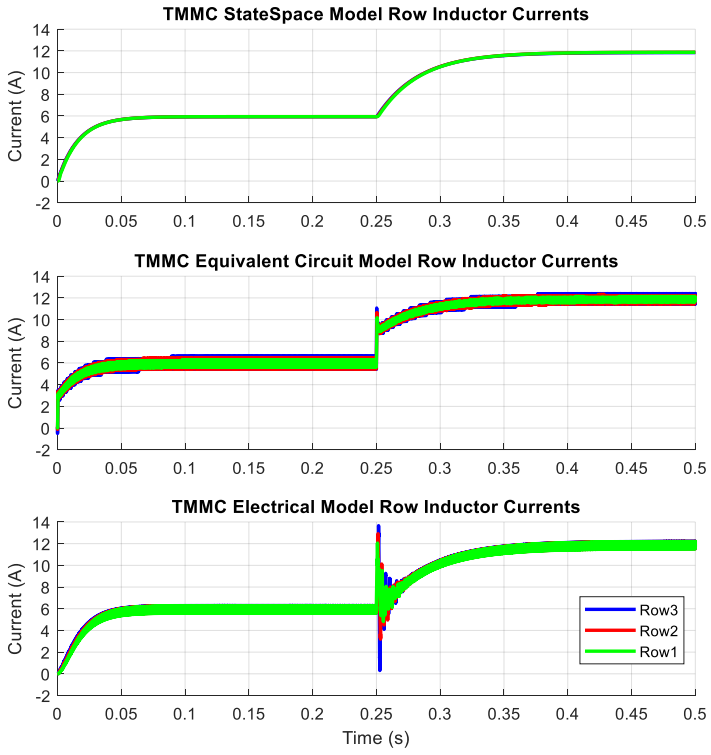

Figure 24. 1 µs time step simulation row inductor current results (top to bottom: state-space, equivalent circuit, switched electrical)

Table 1. Averaged TMMC model test parameters and results

Averaged Steady State Values	State-Space Model	Equivalent Circuit Model	Electrical Model
$\mathbf{L_{src}}$	0.0325 H	0.269 H	2.50 H
$\mathbf{R_{src}}$	0.01 Ω	0.01 Ω	0.01 Ω
L	560 µH	560 µH	560 µH
C	60 µF	60 µF	60 µF
$\mathbf{R_{load}}$	8 Ω (with step change to 4 Ω)		
$\mathbf{V_{C1,2,3}}$	95 V	94.85 V	94.90 V
$\mathbf{V_O}$	95 V	94.23 V	94.86 V
$\mathbf{I_L}$	5.94, 11.87 A	5.93, 11.89 A	5.94, 11.86 A
$\mathbf{T_S}$**,sim**	1 µs, 0.1 µs	1 µs, 0.1 µs	1 µs, 0.1 µs
$\mathbf{f_S}$	100 kHz	100 kHz	100 kHz
t,sim,avg (1 µs)	5.99 s	61.96 s	98.02s
t,sim,avg (10 µs)	4.13 s	18.46 s	--

Using averaged techniques for state-space and equivalent circuit converter modeling speeds up simulation time and allows for high fidelity simulated studies of larger APDN systems. The state-space approach provides the fastest solution for simulating converter performance, albeit while sacrificing true switching transient dynamics and the ability to directly interface with other electrical systems. The equivalent circuit averaging modeling technique provides a good compromise between improving simulation performance while maintaining more of the converter dynamics during transient phenomenon as well as the ability to directly interface with external electrical circuitry. These findings reinforce the benefits of using averaged models for simulation to cut down on simulation time. These techniques can be used as a modeling option while exploring a larger test case of a distribution network utilizing APDNs.

2.4 Stability Analysis of the TMMC-APDN

To evaluate the stable operation of the converter design, the local stability of the TMMC-APDN is investigated around defined equilibrium points. By analyzing the TMMC-APDN voltage and current dynamics with respect to its PI controller loop equations, the converter's eigenvalues and poles are derived. Both step-down and step-up configurations of the TMMC are analyzed to account for different node locations of the slack bus, which in turn, analyzes the TMMC-APDN's stability with different arrangements of connected sources and loads. Capacitor and inductor dynamic equations for the step-down configuration, described in (2-1) and (2-2), are noticeably more complicated than the step-up configuration in (2-3) and (2-4). This difference in complexity can largely be attributed to the location of the slack bus and how that affects adjacent module row relationships.

For the step-down TMMC-APDN, the controller states, disturbance terms, and control inputs are as follows. The states comprise capacitor voltages, inductor currents, and their respective control PI control variables denoted by α – derived and defined for the outer loop voltage controller in (2-13)-(2-15) and the inner loop current controller in (2-16)-(2-18). The disturbance terms refer to variables that cannot be regulated via controller such as source input voltage(s), output load(s), and energy storage current(s). Control inputs include each row of module's capacitor voltage reference. For completion, each state and control input is listed below, but realistically, the number of terms can be reduced by making the assumption that each row of modules shares the same inductor current value; and therefore, only one inductor current term would be required per row of modules for analysis.

States (x):

$$v_{C_0}\ v_{C_1}\ v_{C_2}\ i_{L_{1,1}}\ i_{L_{1,2}}\ i_{L_{1,3}}\ i_{L_{2,1}}\ i_{L_{2,2}}\ i_{L_{3,1}}$$

$$\alpha_{v_{c_0}}\alpha_{v_{c_1}}\alpha_{v_{c_2}}\alpha_{i_{L_{1,1}}}\alpha_{i_{L_{1,2}}}\alpha_{i_{L_{1,3}}}\alpha_{i_{L_{2,1}}}\alpha_{i_{L_{2,2}}}\alpha_{i_{L_{3,1}}}$$

Disturbance Terms (w):

$$v_i\ \dot{v_i}\ i_0\ i_1\ i_2\ i_{ESS_{1,1}}\ i_{ESS_{1,2}}\ i_{ESS_{1,3}}\ i_{ESS_{2,1}}\ i_{ESS_{2,2}}\ i_{ESS_{3,1}}$$

Control Inputs (u):

$$v_{c_0}^{ref}, v_{c_1}^{ref}, v_{c_2}^{ref}$$

For the step-up TMMC-APDN, the controller states, disturbance terms, and control inputs are as follows. The step-up states are identical to their step-down equivalents with the main differences being the disturbance term current values and the control input row capacitor voltages.

States (x):

$$v_{C_1}\ v_{C_2}\ v_{C_3}\ i_{L_{1,1}}\ i_{L_{1,2}}\ i_{L_{1,3}}\ i_{L_{2,1}}\ i_{L_{2,2}}\ i_{L_{3,1}}$$

$$\alpha_{v_{c_1}}\alpha_{v_{c_2}}\alpha_{v_{c_3}}\alpha_{i_{L_{1,1}}}\alpha_{i_{L_{1,2}}}\alpha_{i_{L_{1,3}}}\alpha_{i_{L_{2,1}}}\alpha_{i_{L_{2,2}}}\alpha_{i_{L_{3,1}}}$$

Disturbance Terms (w):

$$v_i\ i_1\ i_2\ i_3\ i_{ESS_{1,1}}\ i_{ESS_{1,2}}\ i_{ESS_{1,3}}\ i_{ESS_{2,1}}\ i_{ESS_{2,2}}\ i_{ESS_{3,1}}$$

Control Inputs (u):

$$v_{c_1}^{ref}, v_{c_2}^{ref}, v_{c_3}^{ref}$$

$$v_{c_k}^{ctrl} = K_{p_v}\left(v_c^{ref} - v_{c_k}\right) + K_{i_v}\int\left(v_c^{ref} - v_{c_k}\right) \tag{2-13}$$

$$\alpha_{v_c} = K_{i_v}\int\left(v_c^{ref} - v_{c_k}\right) \tag{2-14}$$

$$\dot{\alpha}_{v_c} = K_{i_v}\left(v_c^{ref} - v_{c_k}\right) \tag{2-15}$$

$$d_k = K_{p_c}\left(i_{L_k}^{ref} - i_{L_k}\right) + K_{i_c}\int\left(i_{L_k}^{ref} - i_{L_k}\right) \tag{2-16}$$

$$\alpha_{i_L} = K_{i_c}\int\left(i_{L_k}^{ref} - i_{L_k}\right) \tag{2-17}$$

$$\dot{\alpha}_{i_L} = K_{i_c}\left(i_{L_k}^{ref} - i_{L_k}\right) \tag{2-18}$$

Due to the non-linearities of the converter and control designs, the discussed closed loop systems must be linearized around a defined equilibrium point before investigating the local stability. The dynamics of each configuration can be defined using a combination of their states, disturbance terms, and control inputs as follows,

$$\dot{x} = f(x, w, u)\,. \tag{2-19}$$

This dynamic expression can then linearized around a defined equilibrium point as denoted by (2-20)-(2-22) for the step-down configuration, where $V_{C_k} = V_{C_k}^{ref}$, $I_{L_k} = I_{L_k}^{ref}$, $\mathrm{A}_{v_{C_k}} = V_{c_k}^{ctrl}$ per (2-13), and $A_{i_{L_k}} = D_k$ per (2-16). This same process is repeated for the step-up function,

$$X = \left[V_{C_0}\, V_{C_1}\, V_{C_2}\, I_{L_{1,1}}\, I_{L_{2,1}}\, I_{L_{3,1}} \mathrm{A}_{v_{c_0}} \mathrm{A}_{v_{c_1}} \mathrm{A}_{v_{c_2}} \mathrm{A}_{i_{L_{1,1}}} \mathrm{A}_{i_{L_{2,1}}} \mathrm{A}_{i_{L_{3,1}}}\right]^T \tag{2-20}$$

$$W = \left[V_i\, \dot{V}_i\, I_0\, I_1\, I_2\, I_{ESS_{1,1}}\, I_{ESS_{1,2}}\, I_{ESS_{1,3}}\, I_{ESS_{2,1}}\, I_{ESS_{2,2}}\, I_{ESS_{3,1}}\right]^T \tag{2-21}$$

$$U = \left[V_{c_0}^{ref}\, V_{c_1}^{ref}\, V_{c_2}^{ref}\right]^T. \tag{2-22}$$

The state matrix, *A*, of each linearized system can then be calculated using the Jacobian matrix between the relationship of (2-19) and the linearized terms of the system per (2-20)-(2-22).

$$A = \left[\frac{\partial f(X, W, U)}{\partial X}\right] \tag{2-23}$$

The eigenvalues of the equilibrium point operation are calculated to determine local stability performance of both a step-down and step-up TMMC-APDN. These stability calculations are performed according to system parameters in Table 2 and PI controller gains in Table 3. The test results are shown in Figure 25, Figure 26, Figure 27, and Figure 28. The first two showcase the local stability results of the step-down converter and the latter two show the local stability results of the step-up converter. Figure 26 and Figure 28 present a zoomed-in view of the tightly packed voltage controller poles for each configuration to showcase the spread of the poles. Each configuration's testing shares the same stepped output power levels relative to their output voltage of 2850 W, 2137.5 W, 1425 W, and 712.5 W.

The eigenvalues of both converter arrangements consistently lie on the left-half of the complex plane indicating local asymptotic stability around the defined equilibrium points. As desired, there is a clear separation of the 6 voltage controller eigenvalues and the 12 current controller eigenvalues demonstrating the decoupling of the controller inner- and outer-loops. The method used to evaluate the stability can be found in Appendix A.

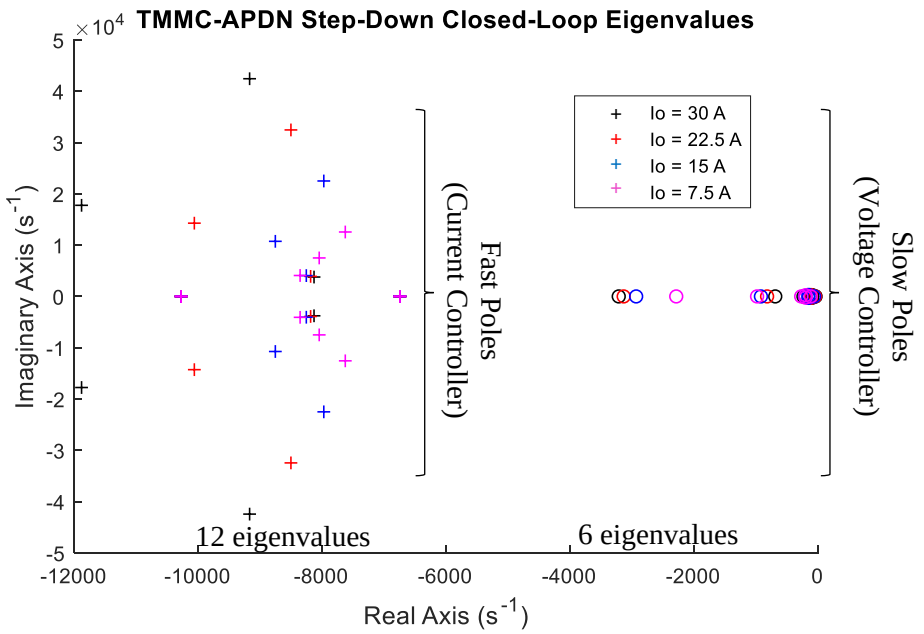

Figure 25. Step-Down TMMC-APDN Closed-Loop Eigenvalue results derived from controller loops showing a separation between voltage controller and current controller poles (+ indicates fast poles; o indicates slow poles)

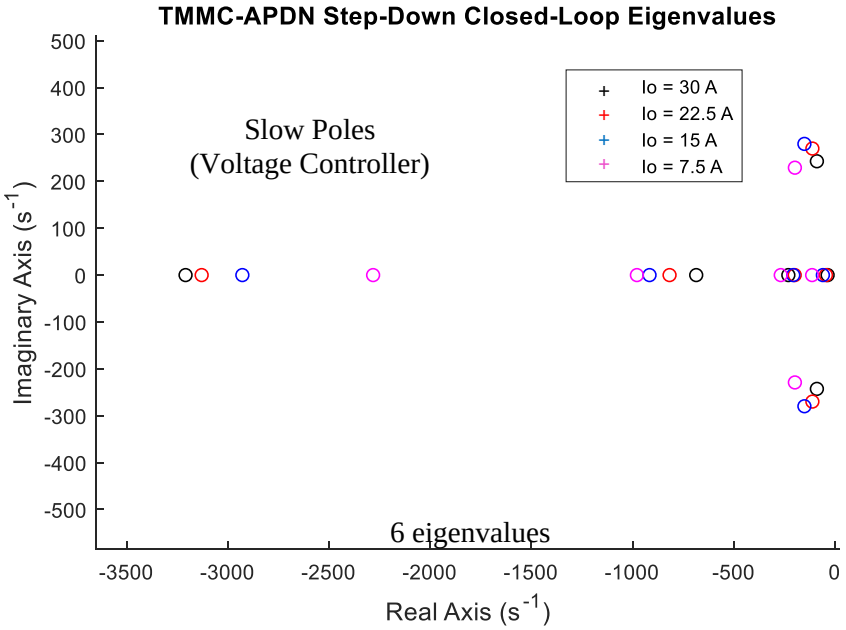

Figure 26. Zoomed-In view of Step-Down TMMC-APDN Closed-Loop Voltage Controller Eigenvalue results

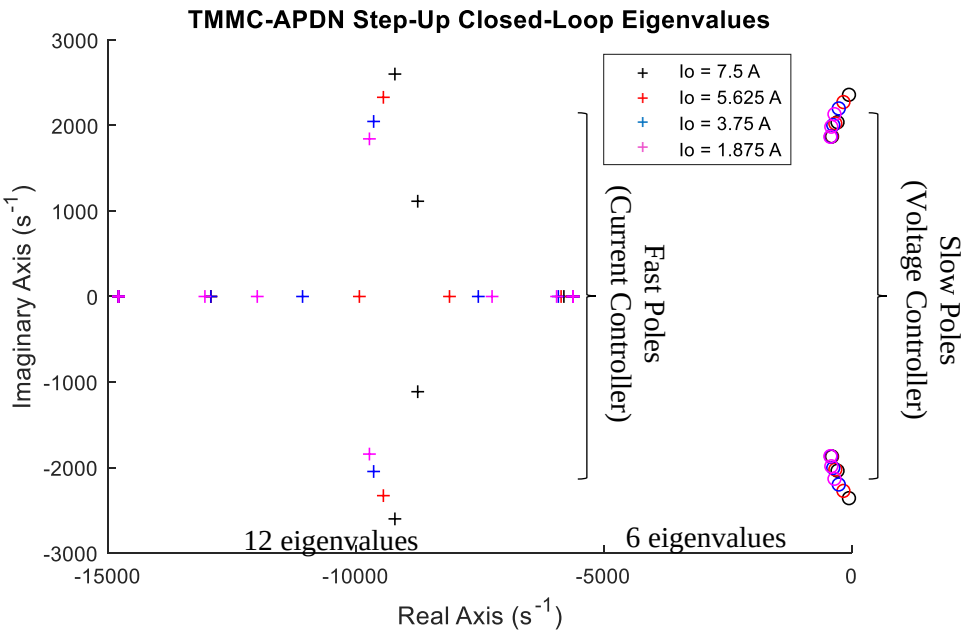

Figure 27. Step-Up TMMC-APDN Closed-Loop Eigenvalue results derived from controller loops showing a separation of voltage controller poles from current controller (+ indicates fast poles; o indicates slow poles)

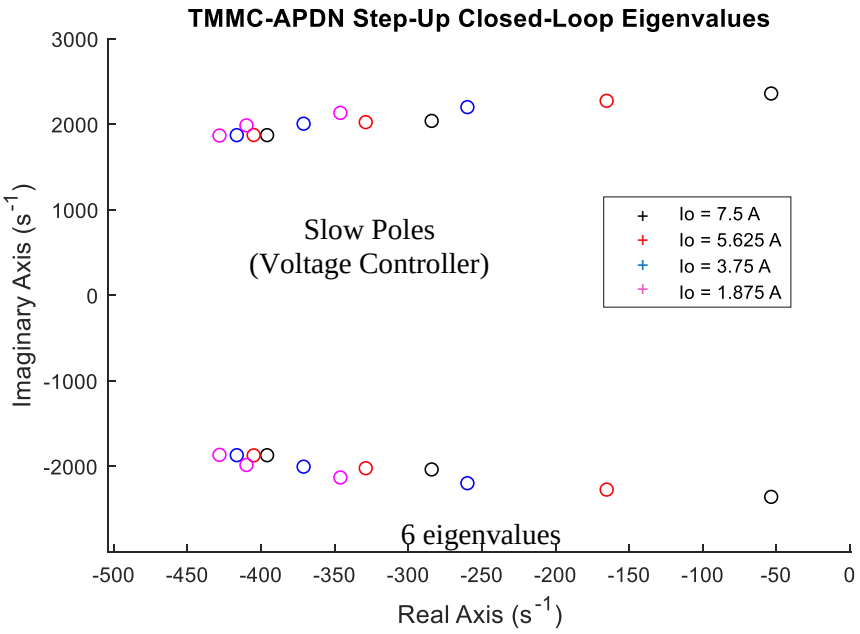

Figure 28. Zoomed-In view of Step-Up TMMC-APDN Closed-Loop Voltage Controller Eigenvalues results

Table 2. Stability Test Parameter Values

Parameter	Value (units)
Step-Down Source Voltage	380 V
Step-Up Source Voltage	95 V
Module Voltage	95 V
Module Capacitance	60 μF
Module Inductance	560 μF
Step-Down Output Current Range	30 A, 22.5 A, 15 A, 7.5 A
Step-Up Output Current Range	7.5 A, 5.625 A, 3.75 A, 1.875 A

Table 3. Stability Test Controller Variables

Configuration	Parameter	Value (units)
Step-Down	Kpv	0.01
	Kiv	5.2
	Kpc	0.05
	Kic	204
Step-Up	Kpv	0.05
	Kiv	260
	Kpc	0.06
	Kic	244.8

3.0 Hardware Implementation of TMMC-APDN

The TMMC-APDN hardware prototype was designed in Altium according to the parameters and components specified in Table 4 and Table 5. Given the modularity of the TMMC-APDN converter, the full PCB design is divided into individual module boards. This design choice encourages the flexible construction of different sized TMMC-APDNs with a different number of module rows relative to the source and load requirements of a specific network node. For instance, three module boards can be used for a two-row converter, six module boards for a three-row converter, and so on. The board design is distributed across four-layers with designated layers for ground and power in the middle of the board per Figure 29. Each module board design contains a single synchronous buck-boost converter with electrical input/output connection ports on the top and bottom sides of the board.

Table 4. APDN Converter Module PCB Component Ratings

Parameter	Rating
Module Power Rating	0.750-1.1 kW
Switching Frequency	100 kHz
Input Voltage	95 V_{DC}
Output Voltage	95 V_{DC}
Module Capacitance	60 µF
Module Inductance	560 µH

Table 5. PCB Design Components

Component	Rating
Infineon MOSFET IPP200N25N3G	250 V, 64 A, 20 mΩ
TI Isolated Gate Driver UCC5320	4.3 A, 3000V_{rms} isolation
EPCOS Film Capacitor B32678G	60 µF, 300 V_{dc}
CWS Power Inductor HF5712-561M-25AH	560 µH, 25 A, 25 mΩ, 790 kHz
Allegro Current Sensor ACS770ECB-200B-PFF-T	200 A, AC/DC

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.01mm	3.5	
1	Top Trace		Signal	1oz	0.036mm		
	Dielectric 2	PP-006	Prepreg		0.122mm	4.2	0.02
2	Ground Plane		Signal	1oz	0.035mm		
	Dielectric5	FR-4	Dielectric		1.15mm	4.2	
3	Power Plane		Signal	1oz	0.035mm		
	Dielectric 3	PP-006	Prepreg		0.122mm	4.2	0.02
4	Bottom Trace		Signal	1oz	0.036mm		
	Bottom Solder	Solder Resist	Solder Mask		0.01mm	3.5	
	Bottom Overlay		Overlay				

Figure 29. 4-Layer Stack-Up of TMMC-APDN Module

3.1 PCB Design of TMMC-APDN Modules

The Infineon IPP200N25N3G MOSFET, capacitor, and inductor were selected according to work performed in [14]. A 200 A Allegro hall effect current sensor is used to measure the module inductor current with nominal operation running around 20 A. Additional board components include the two-channel gate driver with built-in isolation and one isolated DC/DC converters per gate driver channel for supplying the gate driver with isolated power supply voltage

signals. The Texas Instruments gate driver [44] is configured to output a 0 V to 12 V potential to the MOSFET gate in order to reach the turn-on gate-to-source threshold voltage of 3 V. This gate driver voltage range rests well within the V_{GS} of the MOSFET [45] (±20 V) and is large enough to minimize on-state losses and prevent false $\frac{dV}{dT}$ turn-on. Input and output RLC filters in combination with snubber circuitry for each MOSFET was designed to reduce ripple on the output of the converter module. The tested PCB design is shown in Figure 30 with a zoomed-in view of the gate driver circuitry in Figure 31. The top and bottom of the boards are seen 3D-modeled in Altium in Figure 32 and Figure 33, respectively. The experimental test board top and bottom layers and the test setup are shown in Figure 34, Figure 35, and Figure 36, respectively. The Altium schematics are shown in Figure 37 through Figure 40.

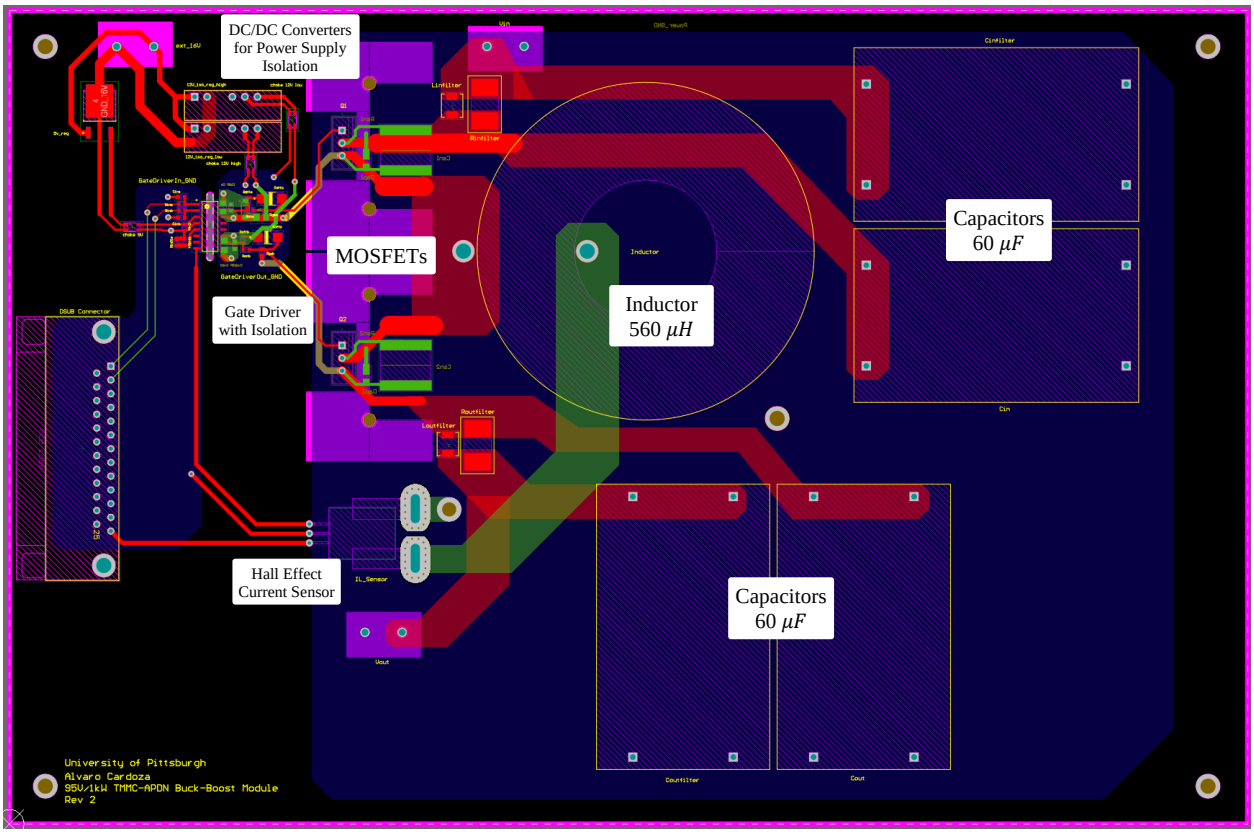

Figure 30. 4-Layer PCB Design of Single TMMC-APDN Module

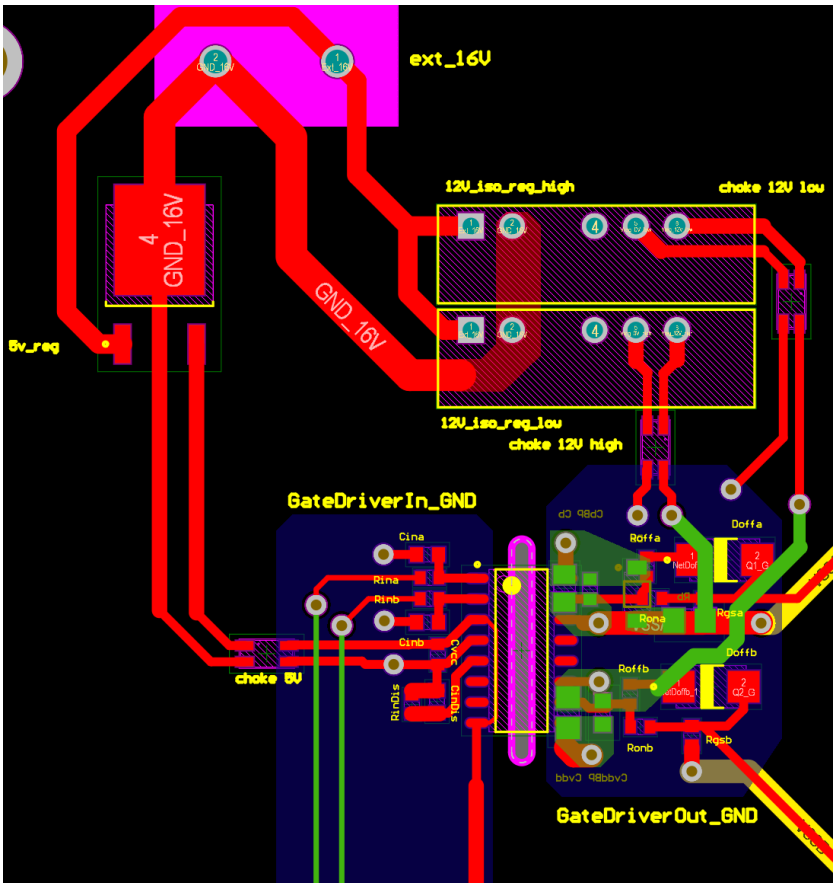

Figure 31. TMMC-APDN Module Gate Driver Circuitry

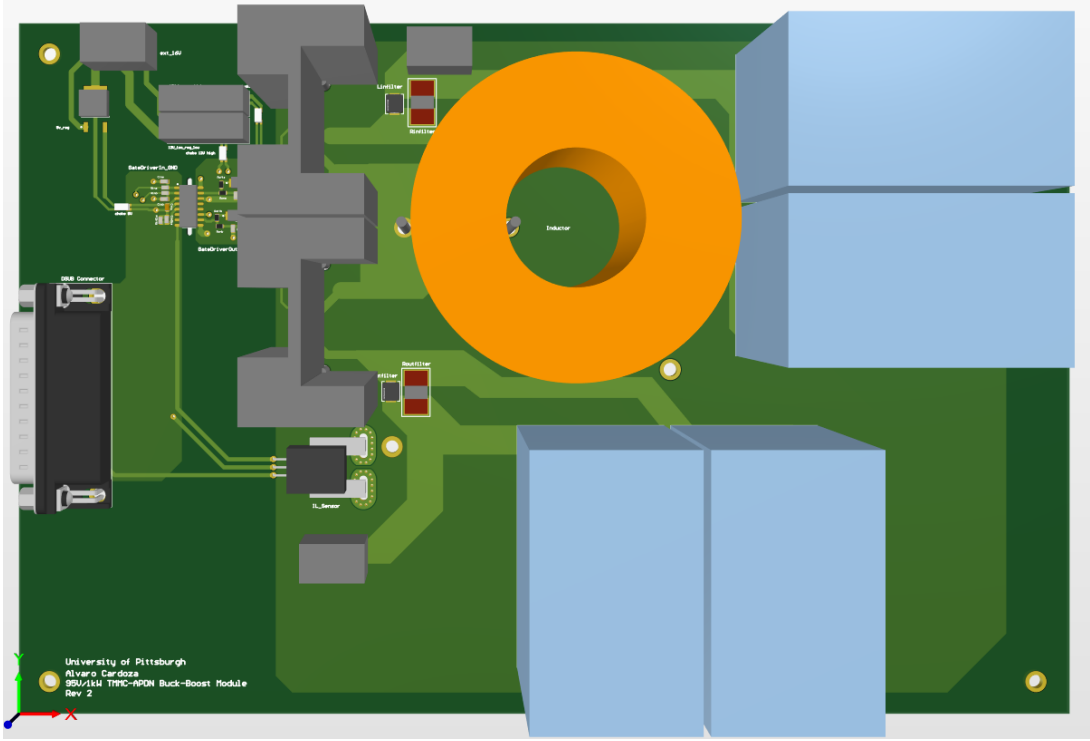

Figure 32. Top Layer of Altium 3D-model TMMC-APDN Module Board

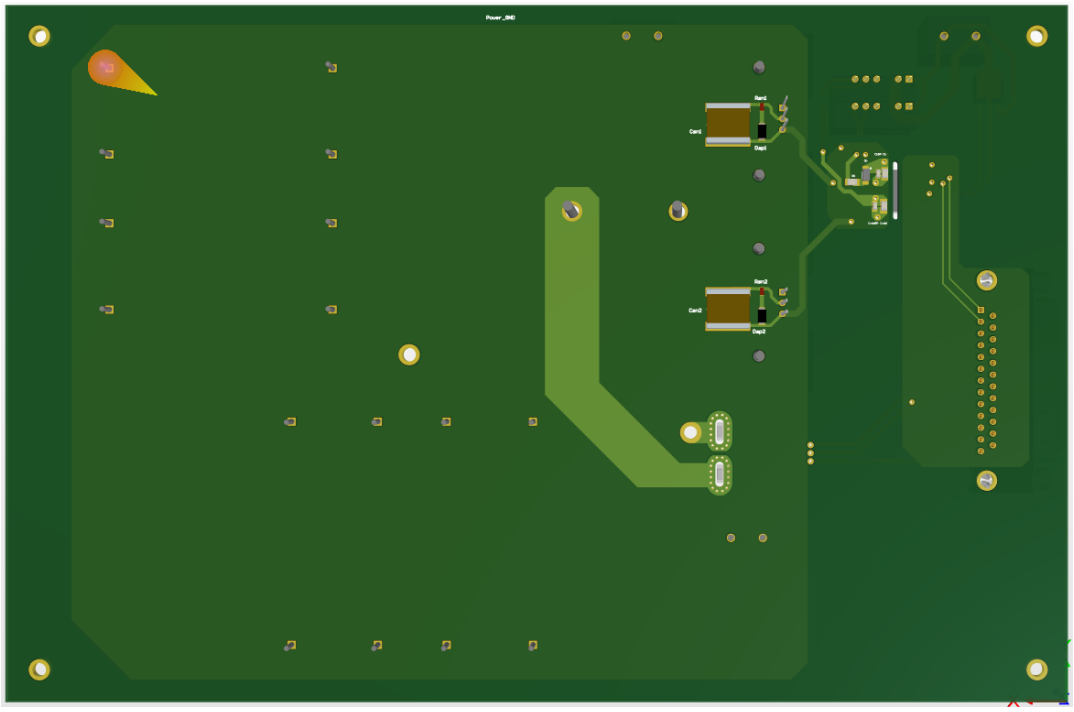

Figure 33. Bottom Layer of Altium 3D-model TMMC-APDN Module Board

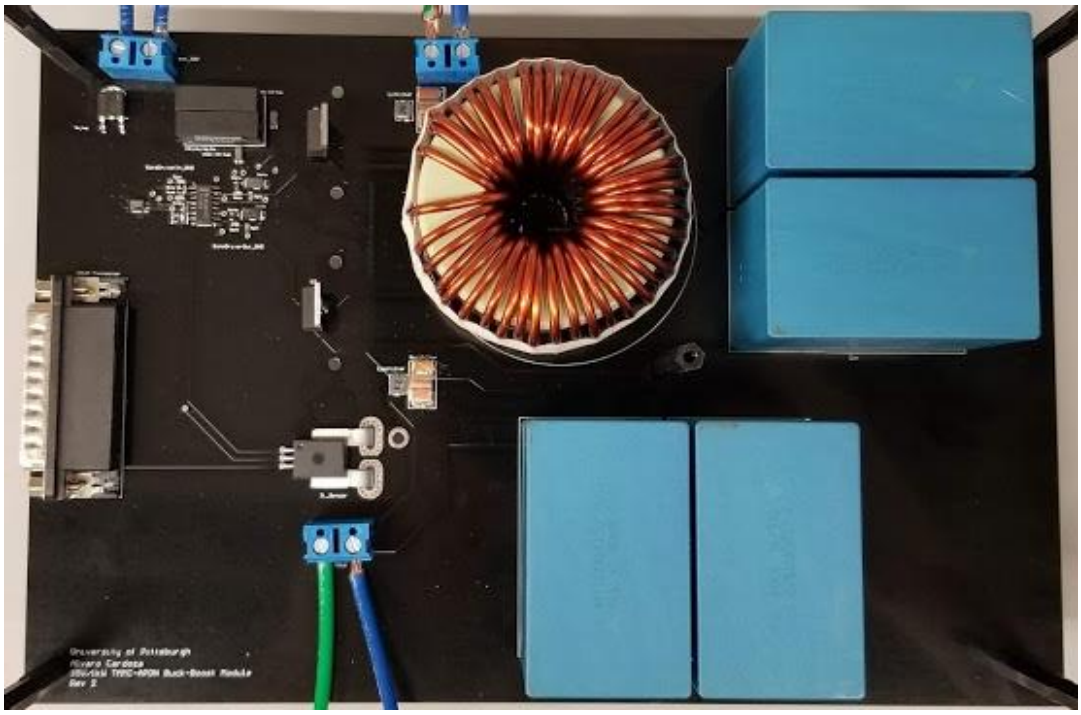

Figure 34. Top Layer of Soldered TMMC-APDN Prototype Module Board

Figure 35. Bottom Layer of Soldered TMMC-APDN Prototype Module Board

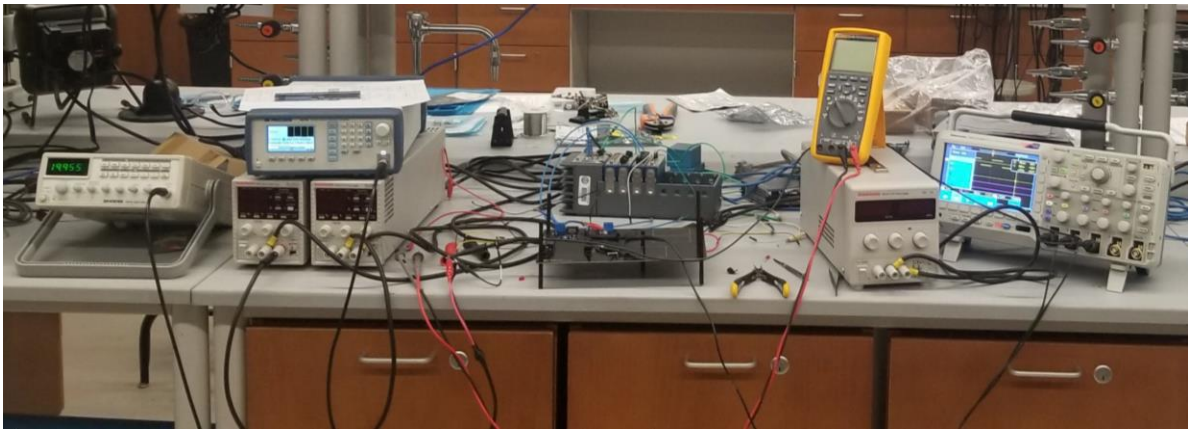

Figure 36. Laboratory Test-Setup

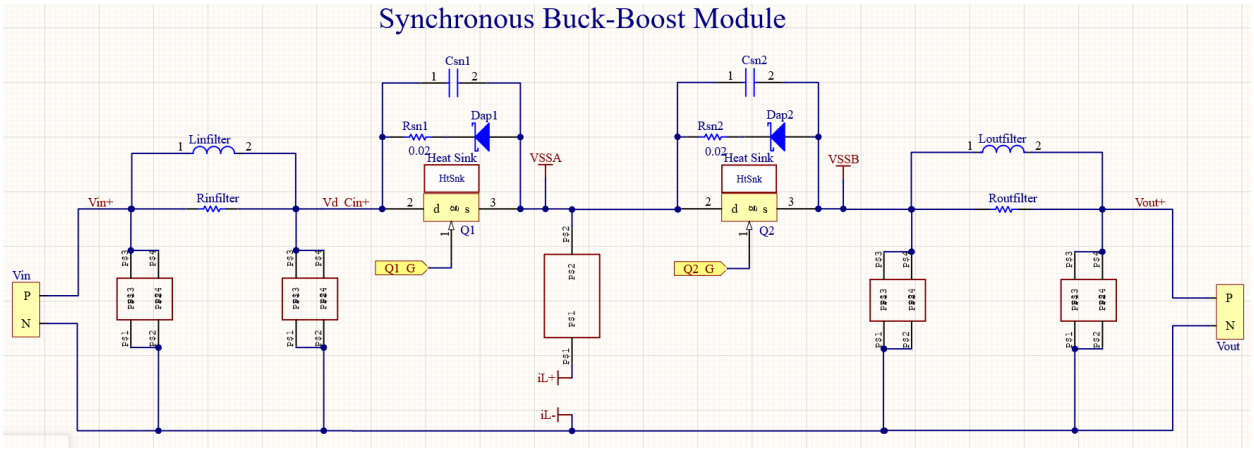

Figure 37. Altium Schematic of Synchronous Buck-Boost TMMC-APDN Module

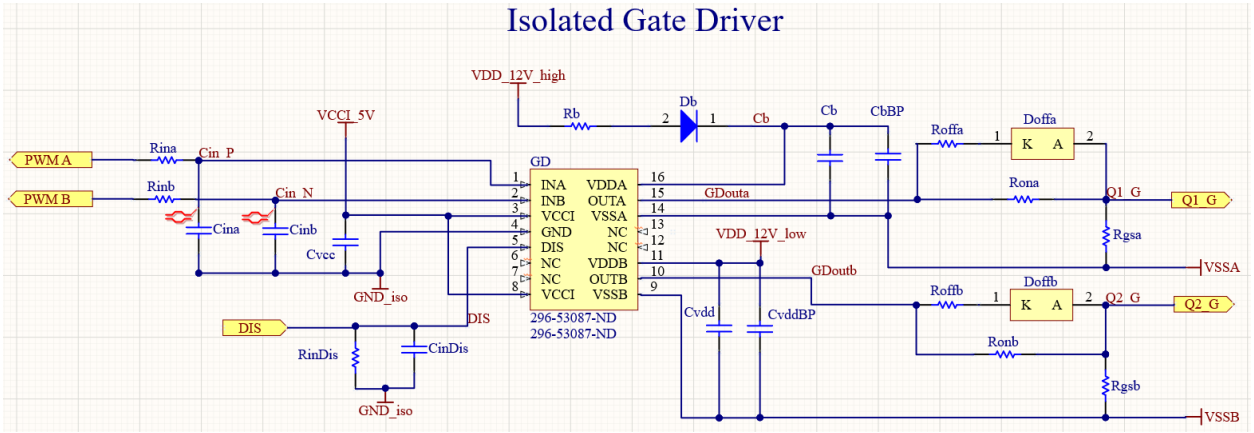

Figure 38. Altium Schematic of Isolated Gate Driver Design

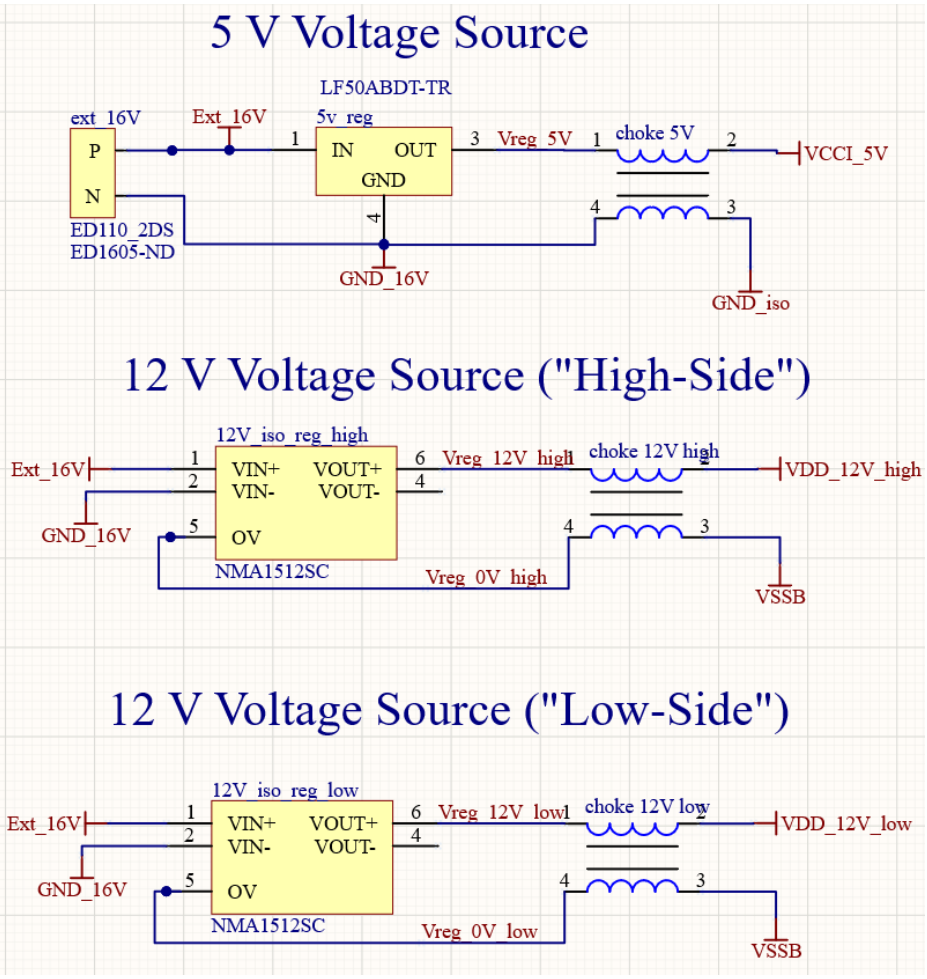

Figure 39. Altium Schematic of 5 V and 12 V Gate Driver Input and Output Voltage Regulators (5 V regulator powers the input signals and 12 V isolated converters power the two gate driver output channels)

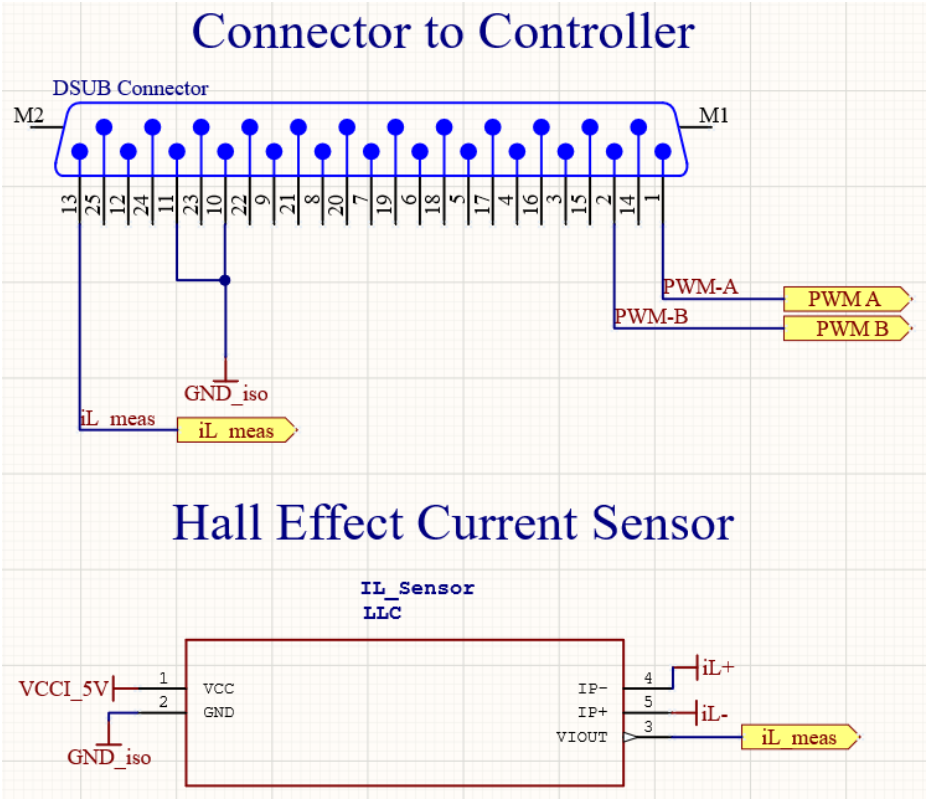

Figure 40. Altium Schematic of the Signal D-SUB Connector for External Controller Connections (PWM signals A and B, current measurement) and Hall Effect Current Sensor Designs

3.2 LTspice Simulation Validation of TMMC-APDN Module Design

To verify the proper selection of circuit components and design operation, the TMMC-APDN synchronous buck-boost module is simulated using LTspice. Every component used in the Altium schematic and design is referenced in LTspice to replicate the performance of the converter as possible as closely. A dead time delay of 250 ns is programmed between the two switching signals entering the gate driver to mitigate the potential of shoot-through. Additionally, a boot

strap circuit is designed for the “high-side” output channel of the gate driver to ensure that the “high-side” N-Channel MOSFET with its low on-resistance is biased sufficiently with a V_{gs} signal larger than its drain voltage to consistently turn on as desired.

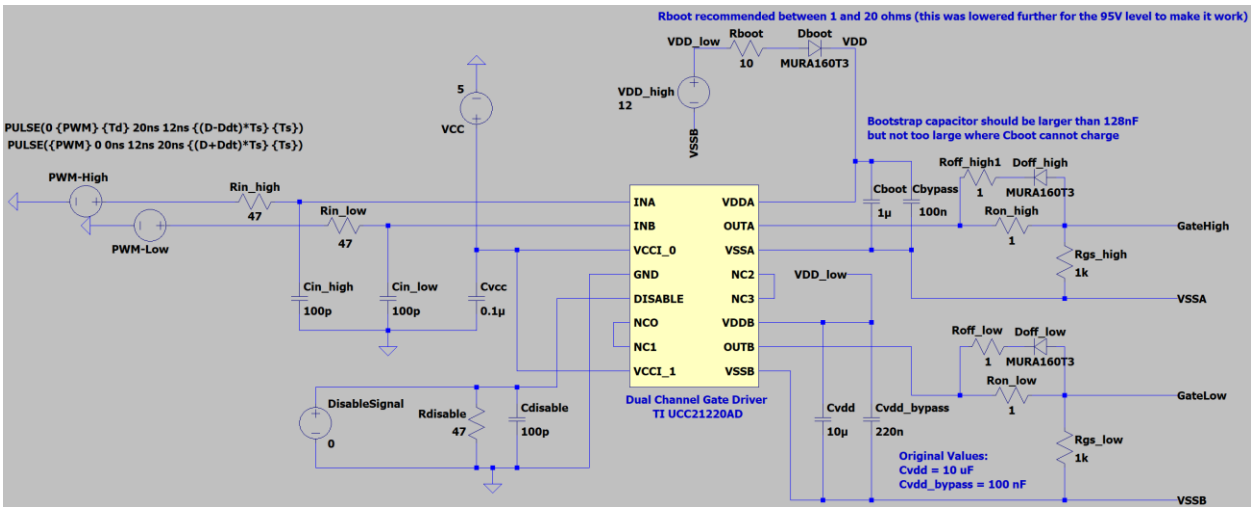

Figure 41. The LTspice gate driver simulation design

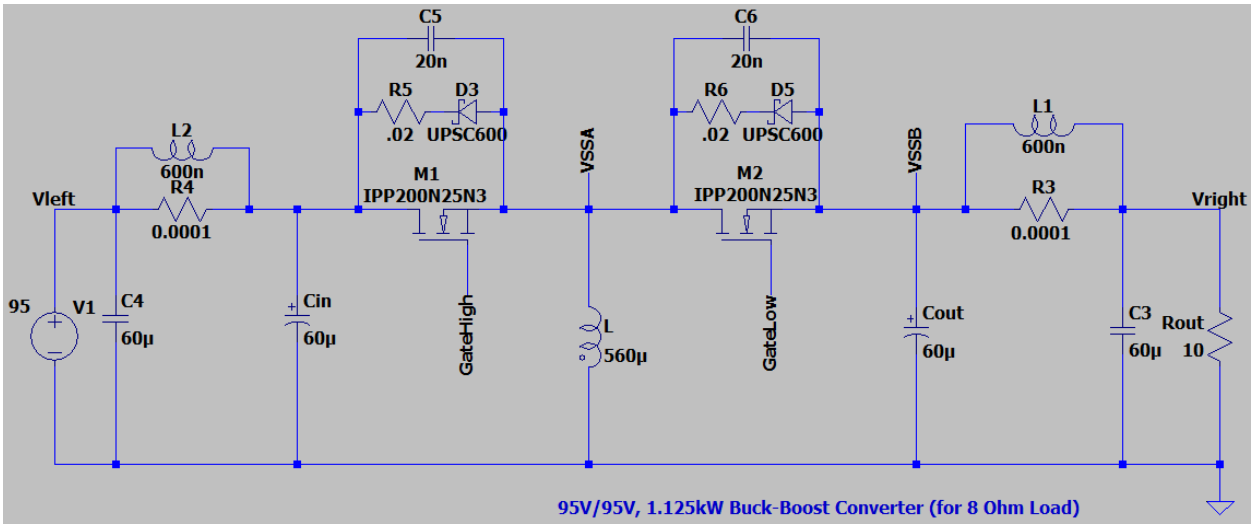

Figure 42. The LTspice Synchronous Buck-Boost Converter Module Simulation Design

```
.model MURA160T3 D(IS=1.11356e-09 RS=0.283217 N=1.57799 EG=1.22127 XTI=0.05 BV=600 IBV=5e-06 CJO=2.2552e-11 VJ=0.4 M=0.356372 FC=0.5 TT=9.47851e-08 KF=0 AF=1
.lib UCC21220AD_TRANS.lib
.param D=0.51 Ts=0.00001 PWM=5 Td=150ns Ddt=0.015
.tran 0 10ms 0 startup uic
.ic V(Vleft)=0 V(Vright)=0 I(L)=0
```

Figure 43. The LTspice Test Parameters

Running the LTspice simulation provides the results shown in Figure 50, Figure 51, and Figure 52. The desired results should produce an output voltage close to the input voltage of 95 V, and inductor current equal to roughly the output current divided by (1-D), and square waves with minimal over- and under-shoot switching between 0 V and 12 V with a clear dead zone between switching both signal switch cycles. These results in both figures demonstrate performance close to the desired metrics with an average inductor current of 20.76 A, an output current of 9.6 A, and an average output voltage of 96.42 V. The switching waveforms display defined square waves with negligible over- and under-shoot as well as an active dead zone with both MOSFETs close to 0 V before one of them switches high to ~11-12 V.

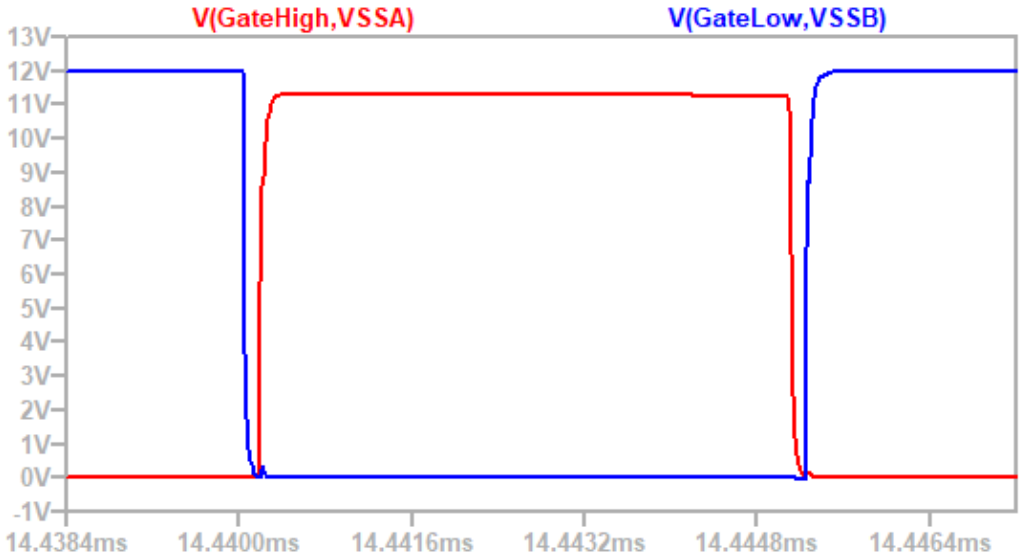

Figure 44. LTspice simulation of TMMC-APDN module gate driver switching signal outputs (12 V and 11.28 V)

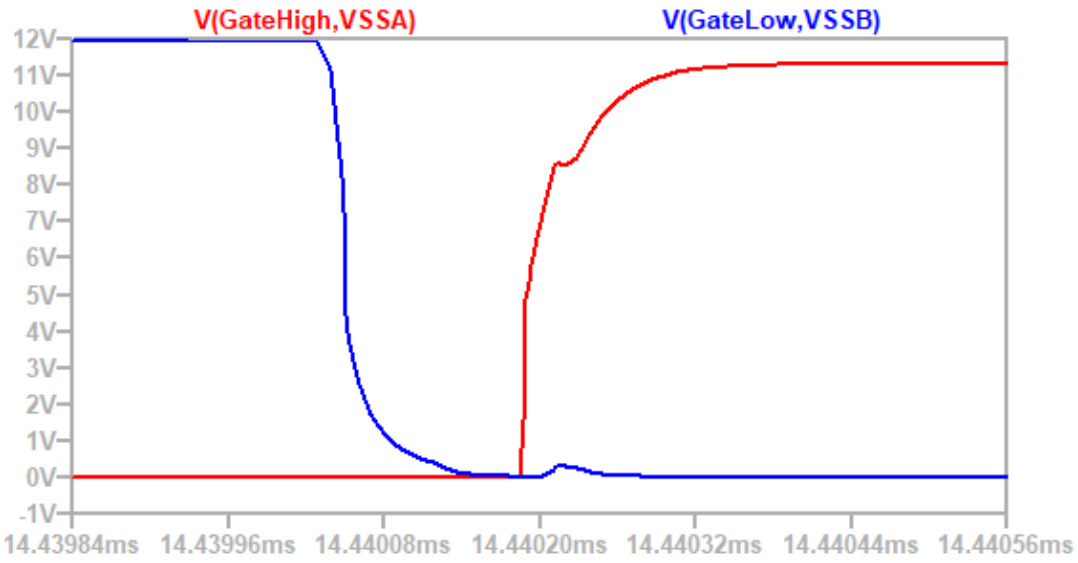

Figure 45. LTspice simulation of TMMC-APDN module dead time between switching signals (44.808 ns)

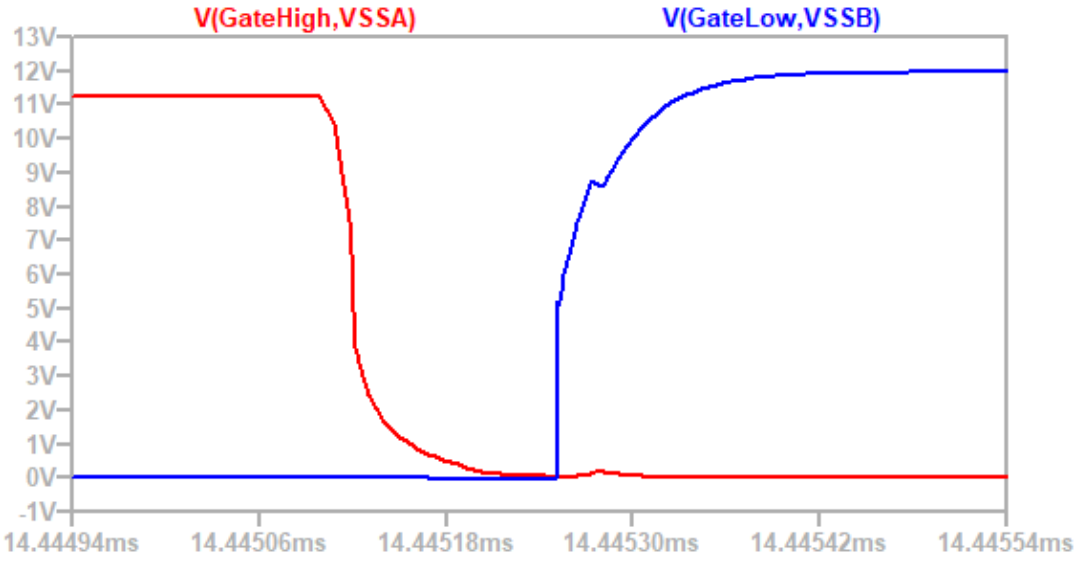

Figure 46. LTspice simulation of TMMC-APDN module dead time between switching signals (45.398 ns)

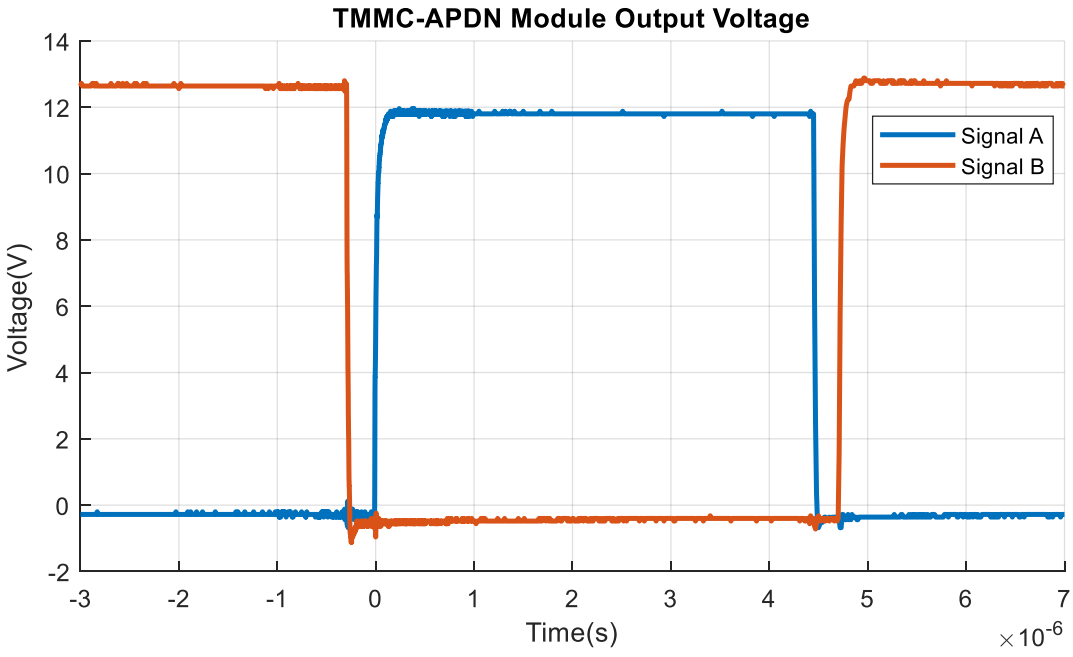

Figure 47. PCB experimental results of TMMC-APDN module dead time between switching signals (250 ns)

The output voltage and main inductor current results Figure 48 and Figure 49, respectively, demonstrate a reduced overshoot, reduced ripple, and improved response time with an increase in output power. All four load sizes achieve steady-state stability at the defined operating points. However, the converter's selected inductor described in Table 5 has a current rating of 25 A, and therefore, would saturate for the 6 Ω, 1500 W load, which has an average steady-state inductor current of 32.72 A. As such, the higher resistance loads are the focus for testing the module board moving forward with the next highest load of 8.2 Ω producing an average steady-state inductor current of 24.65 A. Combined views of the simulated output voltage, inductor current and switching waveforms are shown in Figure 50, Figure 51, and Figure 52.

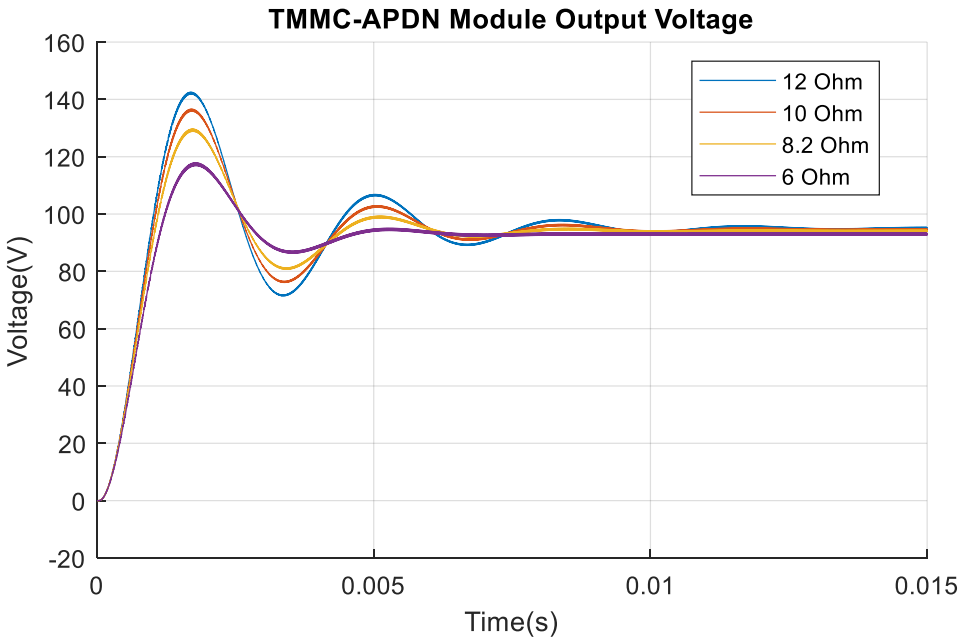

Figure 48. LTspice simulation of TMMC-APDN module output voltage across loads of 12 Ω, 10 Ω, 8.2 Ω, and 6 Ω

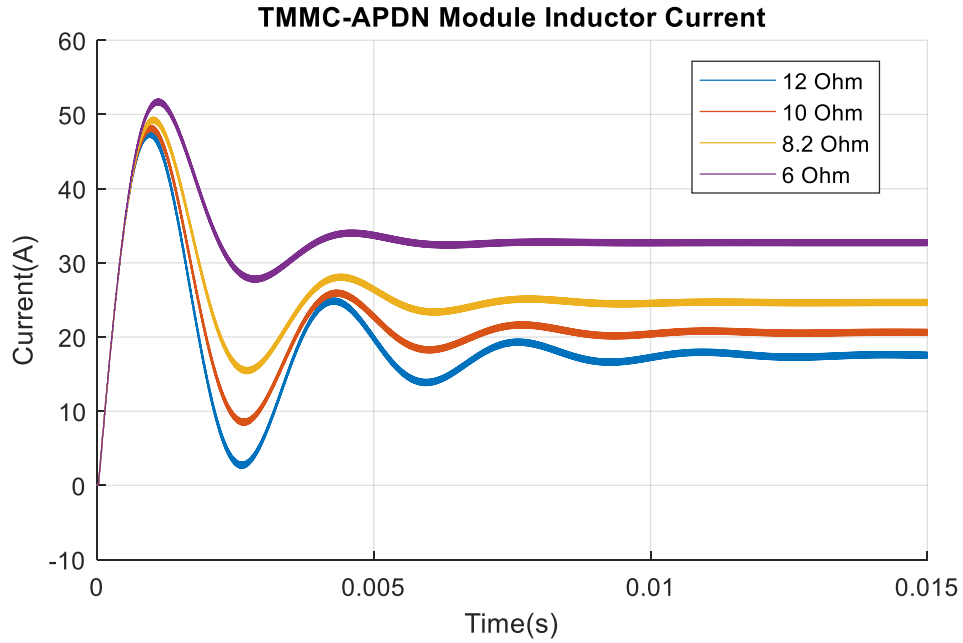

Figure 49. LTspice simulation of TMMC-APDN module inductor current across loads of 12 Ω, 10 Ω, 8.2 Ω, and 6 Ω

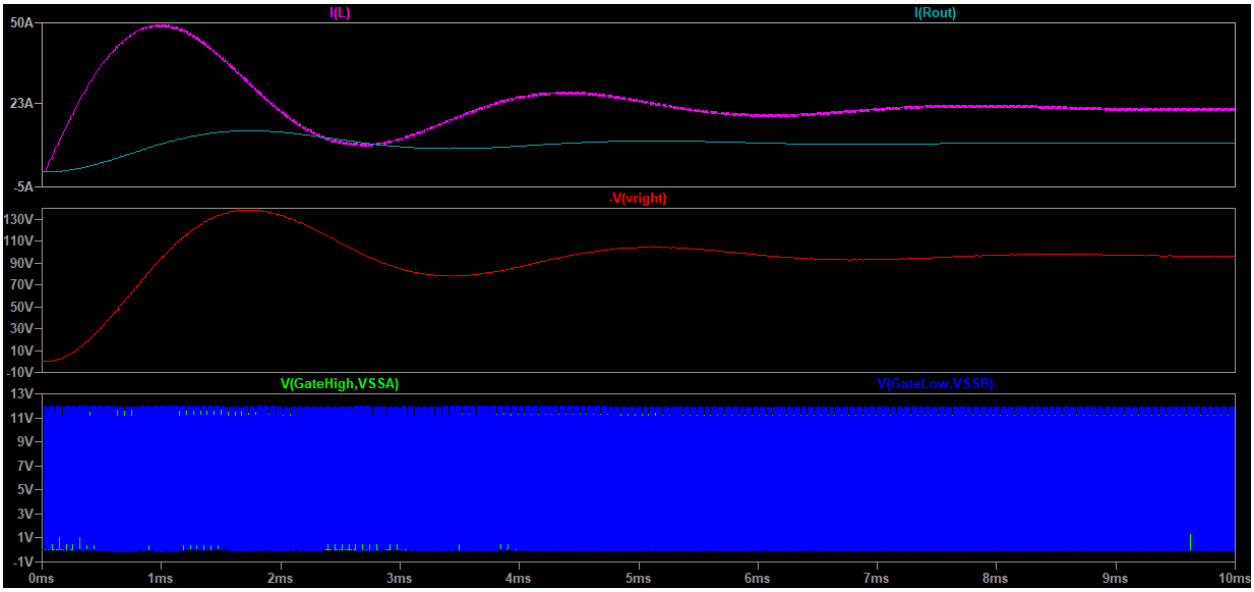

Figure 50. Zoomed-out LTspice Simulation Results of TMMC-APDN Module (from top to bottom: inductor current, output resistor current, output capacitor voltage, and both gate switching signals)

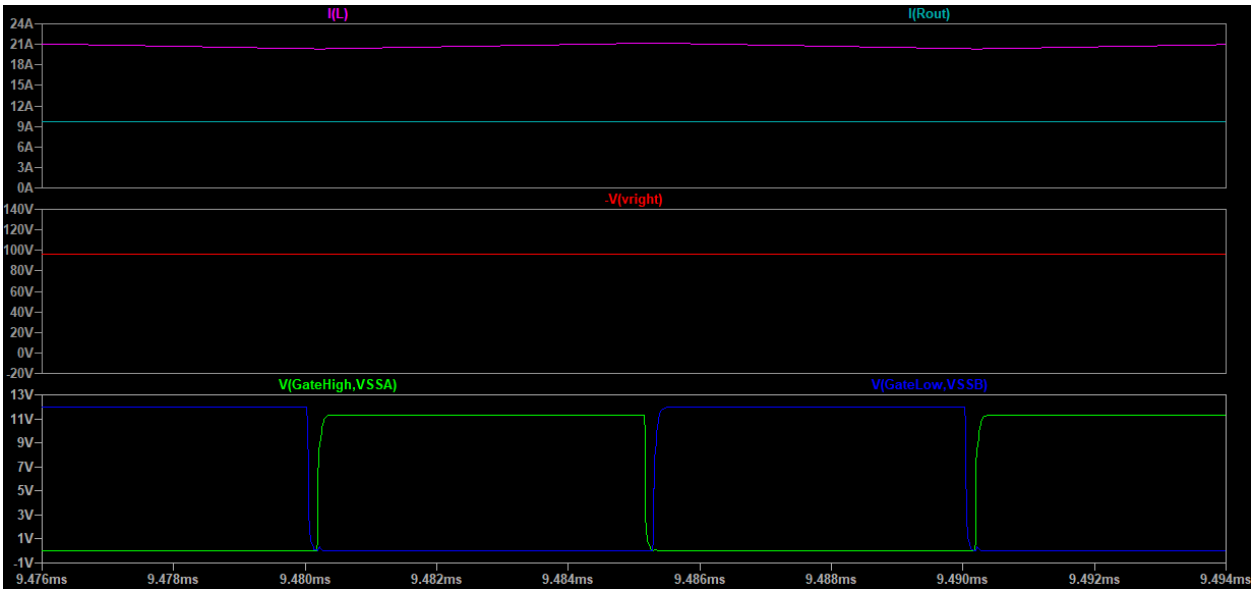

Figure 51. LTspice Simulation Results of TMMC-APDN Module (from top to bottom: inductor current, output resistor current, output capacitor voltage, and both gate switching signals)

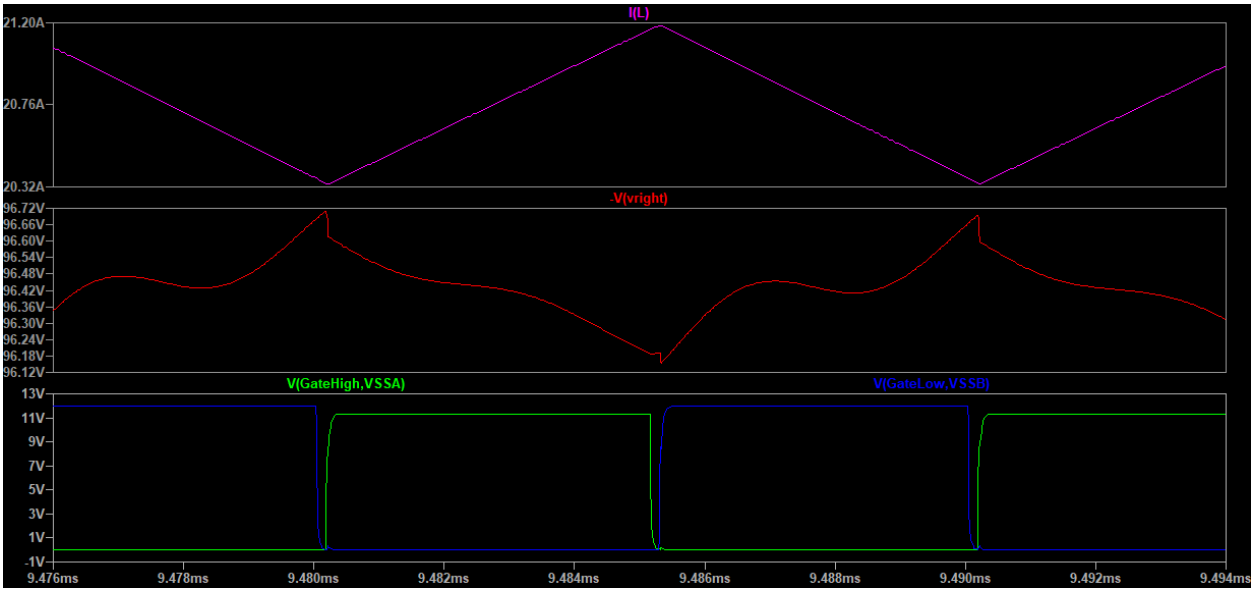

Figure 52. Zoomed-in LTspice Simulation Results of TMMC-APDN Module (from top to bottom: inductor current, output capacitor voltage, and both gate switching signals)

4.0 TMMC-APDN Benefits for Availability

Availability is a metric used to describe a repairable system and its likelihood to be fully operational given the possibility of components failing and coming back online. A more formal definition within the context of this work describes availability as either 1) the probability that a grid will provide full power to a load at any given time, t, or as 2) the expected period of time where a grid functions in its desired manner [22]. A large motivation of this dissertation work is to develop a means to augment distribution networks via power electronics to improve the availability and utilization of renewable forms of DG and distributed energy storage. By studying their availability, it can be determined how effectively APDN enable the energy potential of these technologies to be utilized by an electrical grid or network.

Mathematically availability can be defined as (4-1) where A is the availability of a system or a repairable component, μ and λ are the repair and failure rates, respectively, and T_U and T_D are the mean up time (MUT) and mean down time (MDT), respectively. It should be noted that μ and λ are the inverse terms of MDT and MUT, respectively. The mean time between failures (MTBF) is given by the sum of the mean up and down times, i.e. the relationship of $T_U + T_D$. Modular designs such as the TMMC-APDN excel at reducing MDT by offering redundant pathways for critical loads and should be used when feeding critical loads in a distribution network.

$$A = \frac{\mu}{\lambda + \mu} = \frac{T_U}{T_U + T_D} \tag{4-1}$$

4.1 Distributed Generation (DG) and Availability Investigation

Previous works have shown the technical planning and demand-cost benefits of installing energy storage as a distributed source for critical loads that are sensitive to power availability issues [18], [19]. Studies performed in [20] explore the relationships between a wide-range of downtime costs and different circuit interfaces like power converters and circuit breakers. Results demonstrate that the higher initial cost for power electronic interfaces with embedded energy storage -- like the designs explored in this paper -- can be offset when integrating these power electronic solutions into high availability demanding applications with large downtime costs. These costs can be quite expensive based on the application, such as those in highly sensitive ICT systems. According to an industry-funded economic study in 2013, the average downtime cost for a data center is about $474,480/hour [21], which serves as a big motivator for improving system availability and reducing these costs. The relationship between microgrid design, converter selection, and availability is investigated in [22] providing an extensive framework for evaluating availability in different distribution network designs. Furthermore, systems incorporating multi-port converters were found to promote source diversity and increase overall system availability and resiliency [23].

This chapter presents and analyzes a method for evaluating energy resource availability using minimum cut set probability of a DC distribution network integrated with modular DC-DC converter interfaces with embedded energy storage and discusses the advantages of using such a system layout. Analytic tools are required to understand key characteristics of these technologies and need to accompany such development to better understand how to design, operate, and use them.

Examining the capacitor and inductor dynamics show that a high level of coupling exists between adjacent rows of the converter—demonstrating that the loss of a module row would negatively affect the performance of adjacent rows. This coupling must not only be accounted for to adequately control the converter, but also for the analysis of the converter's availability as the loss of a converter row will negatively impact converter operation. Negative impacts of the dynamic inter-row coupling are lessened by the converter's cascaded voltage-current controller design as well as each module's embedded energy storage.

As previously mentioned, the modular design of the TMMC provides redundancy to any connected system enhancing the overall availability of network operation. It is important to take advantage of the TMMC-APDN's modularity for integrating sensitive sources and loads. Each converter row with parallel modules lowers the probability of row failure relative to the number of parallel modules. Past studies demonstrate the effectiveness of using ESSs for transient load leveling and power-buffering applications with both DC and modular multilevel converter topologies [35]–[37]. To enable power-buffering, a hybrid battery-and-ultracapacitor-based energy storage system (ESS) version of the TMMC-APDN is investigated—expanding the work from [34]. By utilizing a hybrid approach, the energy density and power density benefits of each energy storage technology can be utilized, while mitigating their respective weaknesses. Ultracapacitors operate for transient dynamic response over a range of milliseconds to minutes, while batteries provide a power-deficit compensation over a range of minutes to hours. Additionally, the embedded energy storage helps promote the expansion of new generation and loads added to the distribution network by power-buffering potential new power imbalances that may arise [16].

This alternative and modular approach to designing distribution networks provides selective increased power supply availability to strategic loads within the structure. In turn, APDNs provide an increased utilization of connected generation (especially renewable generation sources, which inherently have intermittent, variable generation profiles). The chosen test system shown in Figure 53 investigates a 380 V DC system—comprising a DC generation source and a load, connected to an AC grid. Two parallel APDNs jointly function as interfaces between the DC bus' generation and loads, and the AC bus' upstream generation. These interfaces boost the network's availability and resiliency with their multi-port design, converter modularity, and embedded energy storage. A DC test system was chosen to reflect the prevalence and increased penetration of DC generation and loads within ICT networks, such as datacenters. Power distribution systems enable simple integration of distributed energy resources (DER), such as PV arrays, and distributed storage (DS), such as batteries. Use of distributed generation sources is considered to hold many benefits in terms of its technical, economical, and environmental impacts [15]. However, it is important to explore new ways to integrate the growing use of DG and rethink the way that electricity is distributed and ensure the availability of DG power supplies is maximized.

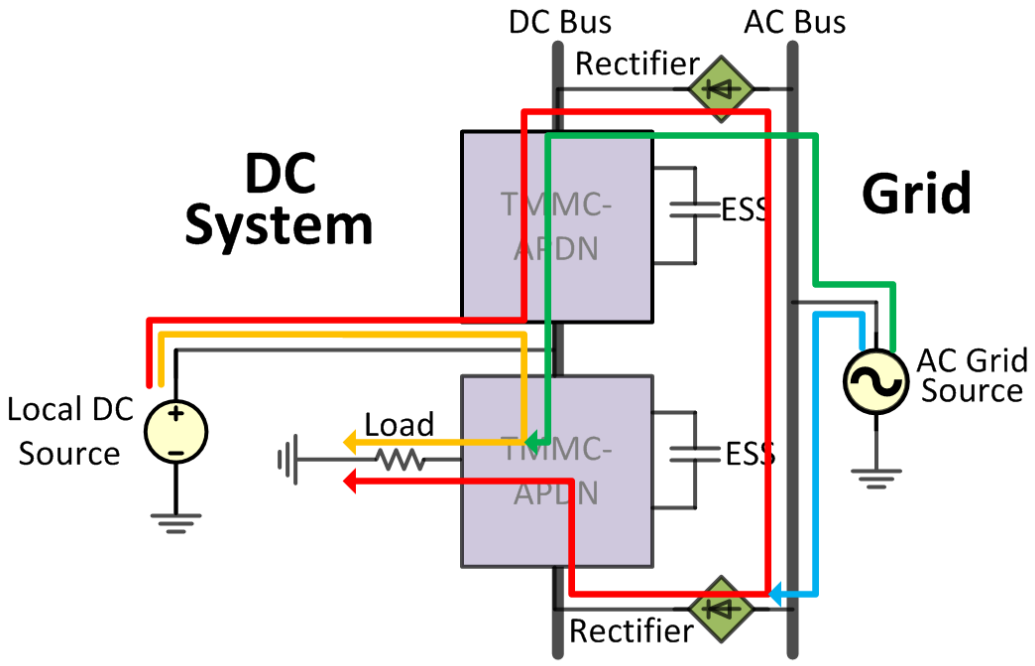

Figure 53. Two TMMC-APDN test system with four potential power flow pathways indicated by the colored arrows

4.2 TMMC-APDN Availability Analysis

Evaluating availability has many practical uses for system operation, such as: a useful quantitative analytical approach for system planning and configuration, risk assessment when selecting expensive technology solutions, and as an input for microgrid controllers [22]. Studying the availability of an APDN system showcases how effectively APDNs maximize the energy potential of DER for the utilization of an electrical grid or network. The higher the availability, the more effectively the DER is being utilized and the more consistently load(s) are being supplied with power and/or returned to power. Emphasis is placed on evaluating the availability effects of the APDN's modularity and embedded energy storage.

Modular designs such as the TMMC-APDN excel at reducing MDT by offering diverse pathways for sources and loads, and excel at feeding critical loads in a distribution network. Each APDN module's failure rate is determined by

$$\lambda_{PE} = \sum_{i} \lambda_i, \tag{4-2}$$

where λ_{PE} is the failure rate of the power electronic interface and λ_i is the failure rate of the i^{th} component of the interface. This approach operates on the assumption that an interface circuit is in an operational state only when all electrical components are functional and healthy. Equation (4-2) sums the failure rate data acquired from manufacturer data sheets as well as technical reliability data handbooks to provide an estimated failure rate for a power electronic circuit [46], [47]. These sources compile their data based on general component quality, device ratings, electrical stress, and environmental conditions.

Collecting failure rates provides sufficient information to analyze the reliability of a specific circuit component or collection of components; however, reliability metrics do not look at the repair rates of system components, and therefore do not do a great job of evaluating system performance. Availability, on the other hand, looks at both failure and repair rates and assesses system performance more effectively and holistically. A conservative MDT estimate of roughly one-week (166.6 hours) is assumed and used to determine the APDN repair rate, μ [22]. This time estimate is surmised from the time needed for replacement part acquisition and circuit restoration of the interface. The repair rate is the inverse of the MDT and calculated as such. In order to compare each converter module and circuit on an equal basis, it is assumed that each circuit is equally stressed. This assumption is reinforced by the TMMC's ability for voltage and current sharing. Additionally, it is important that the APDNs are controlled via decentralized controllers

so as to avoid requiring availability data for communication links that can act as single points of failure, as shown in [26], [48], [49]. The remainder of the reliability data used in the example testcases is found in Table 6.

Table 6. Test Case Reliability Data

Component/System	Failure Rate (10^{-7}/hr)	Repair Rate (10^{-7}/hr)	References
MOSFET	0.79	Non-repairable	[7], [20]
Capacitor	0.60	Non-repairable	[7], [20]
Inductor	1.13×10^{-3}	Non-repairable	[7], [20]
Rectifier	20.0	0.006	[9], [20]
Power Electronics	λ_{PE}	0.006	-
U.S. Electric Grid	4098	0.481	[9], [27]
Control System	3.03	0.006	[9]

Although availability and resiliency analysis is an essential assessment for ensuring the integration of TMMC-APDNs into systems powering critical loads, it is difficult to analyze the chosen test system's availability with conventional methods. For the chosen testbed, the inclusion of two modular converters and two generation sources produces a more complex model for analysis with a large number of possible component states. Techniques like Markov Chain analysis prove practically ineffective for dealing with a large number of states. An efficient alternative method utilizes the studied system's minimal cut sets (MCS) of a Markov chain model as shown in Figure 54. These MCS define the set of components and devices that act as the collective point(s) of worst-case failure and best-case repairability for a system. Minimal cut sets can be associated to minimal cut states representing a system failed condition. However, if any one of the failed components in a minimal cut state is repaired the system returns to operation.

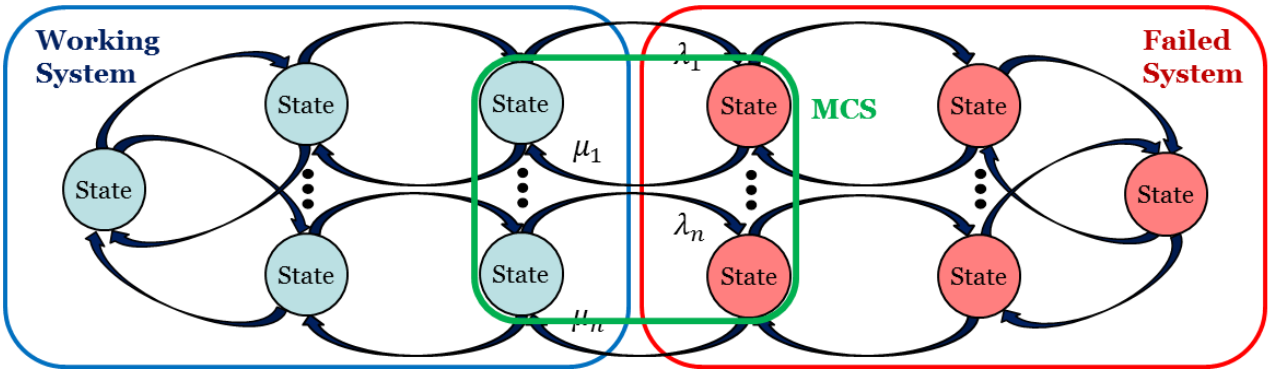

Figure 54. Minimal cut set flowchart between system working states and failed states

The technique referenced in [22], [50] uses the sum of all MCS probabilities in a defined system to approximate the availability of a system relative to its unavailability, U, $(1 - A)$ as indicated by

$$\underbrace{\sum_{i=1}^{M_C} P(K_j) - \sum_{i=2}^{M_C}\sum_{j=1}^{i-1} P\left(K_i \bigcap K_j\right)}_{\text{Lower Bound}} \leq U_{sys} \leq \underbrace{\sum_{j=1}^{M_C} P(K_j)}_{\text{Upper Bound}}, \quad \text{Error Term} \tag{4-3}$$

where M_C is the total number of MCS, K_j represents the MCS, and P(K_j) is the MCS probability. The lower bound comprises an error term relative to two MCS occurring simultaneously as the occurrence of a component failure may not be a mutually exclusive event, and the upper bound contains a singular MCS. While the error term can often be neglected when using highly available electrical components, this paper focuses on the scenario where the error term is not neglected due to the simultaneous influence of parallel converter module MCS and module embedded energy storage MCS.

The availability analysis for this research is focused on the operation of the previously described test system with two parallel TMMC-APDN placed within a DC network connected to an AC grid. Three test cases are evaluated via (4-3) and verified experimentally with Monte Carlo simulation, as described in

Table 7 and , respectively, each test case changing the row location of the load resistor on APDN #2 to explore the impact of parallel modules per load-connected row – three, two, and one module(s), respectively. Each test case will also evaluate four subcases to explore the four potential power pathways of source to load, represented by the colored arrows in Figure 53. Each power pathway is evaluated with MCS to determine the different best-case and worst-case availabilities of the system per test case. The process of determining a power pathway's module MCS and ESS MCS is demonstrated for test case 1.1 in Table 7. Each module of the MCS comprises a point of failure/repair for the testbed, while each ESS MCS comprises the collective functioning modules' ESS and their pathways to serve the load in the test case source's absence. The last ESS MCS is zero as energy storage cannot supply power to the load when the load's module row has simultaneously failed.

Table 7. Subcase 1.1 MCS Configurations

MCS #	Module MCS Configuration Details	ESS Configuration Details	
1	DC Source	**APDN #1**: (6) Module ESS	**APDN #2**: (6) Module ESS
2	**APDN #1**: Row 1 - (3) Parallel Modules	**APDN #1**: (3) Module ESS	**APDN #2**: (6) Module ESS
3	**APDN #1**: Row 2 - (2) Parallel Modules	**APDN #1**: (4) Module ESS	**APDN #2**: (6) Module ESS
4	**APDN #1**: Row 3 - (1) Parallel Module	**APDN #1**: (5) Module ESS	**APDN #2**: (6) Module ESS
5	DC Bus-to-AC Bus: Rectifier	**APDN #1**: (6) Module ESS	**APDN #2**: (6) Module ESS
6	AC Bus-to-DC Bus: Rectifier	**APDN #1**: (6) Module ESS	**APDN #2**: (6) Module ESS
7	**APDN #2**: Row 3 - (1) Parallel Module	**APDN #1**: (6) Module ESS	**APDN #2**: (5) Module ESS
8	**APDN #2**: Row 2 - (2) Parallel Modules	**APDN #1**: (6) Module ESS	**APDN #2**: (4) Module ESS
9	**APDN #2**: Row 1 - (3) Parallel Modules	0	

Table 8. Testbed Load Configurations

Case	Configuration Details
1	Load on Row 1, Local Gen on Row 1, Grid Gen across all rows
2	Load on Row 2, Local Gen on Row 1, Grid Gen across all rows
3	Load on Row 3, Local Gen on Row 1, Grid Gen across all rows

The remaining eleven subcases are performed similarly, and each subcase availability is calculated using the lower bound of (4-3). Reliability data is pulled from industry accepted values detailed in [46] and summarized in Table 6. Using this information, preliminary availability data using the upper bound of (4-3) for the different segments of the APDN is shown in Table 9. Row 1 of the APDN has the highest availability at thirteen 9's due to its 3 parallel modules providing the highest level of redundancy. Other than row 2's two parallel modules providing eight 9's, most of the other converter portions and/or combinations of portions have availability values of four 9's, which correlates to roughly an hour of service downtime per year. A Monte Carlo simulation is performed for a single module to account for converter component reliability variance with a normal distribution of 100,000 component failure rate inputs and a ±50% standard deviation.

Table 9. TMMC-APDN Module Availability Data

Component/System	MUT (hrs)	MDT (hrs)	Availability
TMMC-APDN Module	4.58×10^{6}	166.6	0.999996366369457
TMMC-APDN row 1	3.47×10^{15}	166.6	0.999999999999995
TMMC-APDN row 2	1.26×10^{11}	166.6	0.999999998679 67
TMMC-APDN row 3	4.58×10^{6}	166.6	0.999996366369457
TMMC-APDN + Ctrl	1.92×10^{6}	166.6	0.999991318007430
ESS Interface Converter	6.32×10^{6}	166.6	0.999997365906806
Hybrid ESS + Interface	8.44×10^{6}	166.6	0.999998027260240
Control System	3.30×10^{6}	166.6	0.999994951770010

4.3 Availability Results

For all three test cases, the availability results are presented in Table 10. The highest availability results are identified in subcases 1 and 2 (for all test cases) where the DC source is supplying the power. Subcase 2 consistently has the highest availability as it has the shortest path between generation and load, and therefore has the fewest points of potential failure. Furthermore, test case 1 demonstrates the highest availability potential, which can be attributed to the load being placed on the TMMC-APDN's bottom row with three parallel modules. The Monte Carlo simulation histogram shown in Figure 55 demonstrates the availability probability density function for a single module of TMMC-APDN and has a range of 0.999919 to 0.999998. This simulation is performed using the distribution of failure rate designated in Figure 56. These results reinforce the results found through MCS calculation.

Table 10. Test Case Availability Results

Load Row	Test Case	Subcase Results	
Row 1	1	DC Source — Case 1.1:	0.99995302734910885
		Case 1.2:	0.99999999999998723
		AC Source — Case 1.3:	0.99912478072557376
		Case 1.4:	0.99912478072558653
Row 2	2	DC Source — Case 2.1:	0.99995302734910885
		Case 2.2:	0.99999999945360452
		AC Source — Case 2.3:	0.99912478017919104
		Case 2.4:	0.99912478072559929
Row 3	3	DC Source — Case 3.1:	0.99995302789549156
		Case 3.2:	0.99997662516922248
		AC Source — Case 3.3:	0.99910140534842629
		Case 3.4:	0.99912478127198201

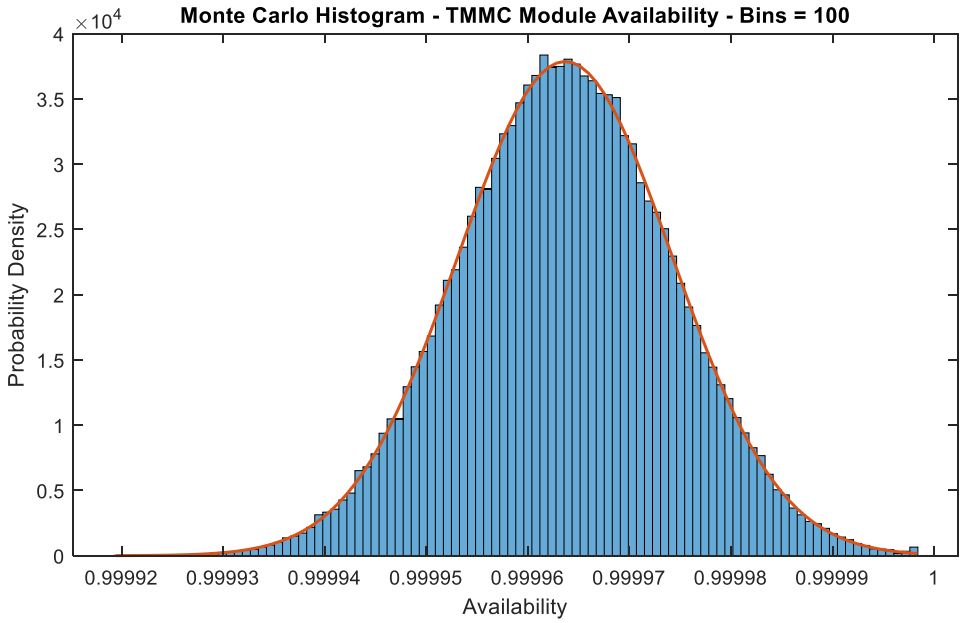

Figure 55. Monte Carlo histogram for a TMMC-APDN converter module's availability over 100 bins

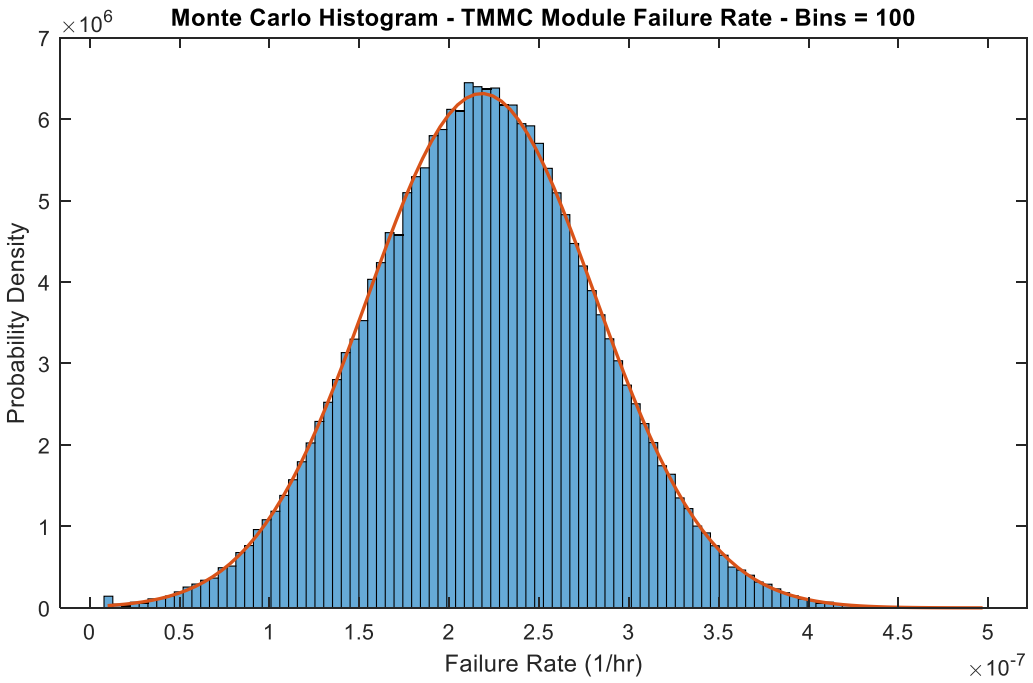

Figure 56. Distribution of TMMC-APDN converter module failure rates over 100 bins used for Monte Carlo analysis

4.4 Availability Test System Simulation

The performance of the two TMMC-APDN test system is verified with simulations of three test scenarios using the parameters in Table 11. Each converter module is controlled to operate at 95 V, with each 3-row n+1 stack of TMMC modules achieving a combined voltage of 380 V, a DC voltage growing in popularity for the design of modern data centers [51]. The local DC generation source is simulated as a controlled current source producing 10 A and connected to the bottom row of 95 V modules. The AC grid connection is designed to supply the 380 V across the entire TMMC-APDN. The ratio of power supplied by the local source relative to the grid source is ~5:1 with the majority of the load being supplied by the local source.

The three test scenarios are described in Table 8 with the changing load positions shown in Fig. 6. Each scenario tests the performance of the system by placing the output load on each row of the APDN #2 (one at a time). Only one APDN is simulated with a load, as both APDNs are identical in design and are in parallel with one another – i.e. the results would be identical for a load placed on APDN #1, row 2 as they would be for a load placed on APDN #2, row 2. The other changed test parameter between tests is the local generation connection.

Table 11. Test System Parameter Values

Parameter	Value (units)
Local source	95 V, 10 A
Grid Source	380 V
APDN Module Voltage	95 V
APDN Capacitance	60 μF
APDN Inductance	560 μF
Energy Storage Type	12 Ah Li-ion Battery; 83 F Ultracapacitor
Energy Storage Voltage	48 V
Load Resistance	8 Ω
Load Power Demand	1128 W
Switching Frequency	100 kHz

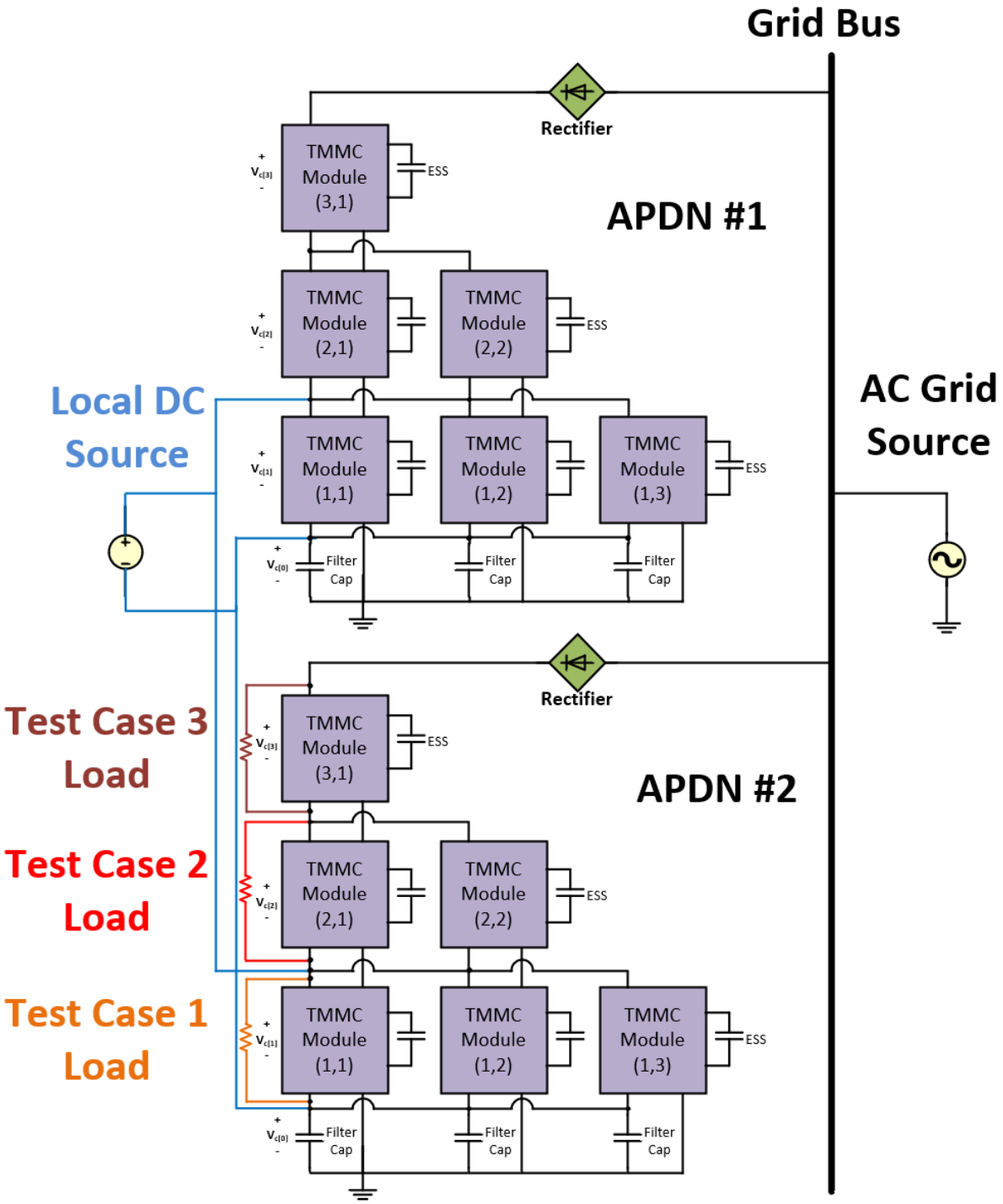

Figure 57. Testcases 1,2,3: Load on row 1, 2, and 3 of APDN #2 (95 V), respectively; local source connected to row of both APDNs (95 V); and grid source connected across all rows of both APDNs (380 V)

As mentioned previously, each APDN is controlled via its own decentralized PI controller with no direct control communication between the two APDNs. Each row of modules is controlled by a cascaded two-stage voltage and current controller, which must account for the previously described capacitor and inductor dynamics. For each row of the converter, a singular voltage controller is utilized to regulate all parallel modules to promote voltage sharing; however, each module per converter row has its own dedicated current controller. Equal voltage and current sharing between all modules of the TMMC is established when the reference voltage is set equal between row voltage controllers. Moreover, the summed voltage between the controlled row and the previous row helps to establish an interdependency of voltage controllers helping to enhance the dynamic performance of the converter. Each APDN module contains its own ESS, and each converter row has its own dedicated ESS control algorithm. The algorithm charges and discharges its energy storage units based on the voltage of the connected module with the objective of achieving a voltage between 94 V and 96 V. Ultracapacitors provide support for transient voltage drops lasting up to 5 minutes; events longer than 5 minutes are transferred to the battery for support.

For each test scenario, the power is disconnected between the DC local generation source and APDN #2 at 0.075 s, and then reconnected at 0.15 s. These tests evaluate the transient response of the energy exchange between the two APDNs and the two connected generation sources. The parameters of interest include the voltage across each row of the APDN (including the bottom output row, which sits below the first row of the converter); the power levels of the local generation source, the grid generation source, and the load resistor; and lastly, the current response of the ultracapacitors across both APDN's top rows, where the grid generation is connected.

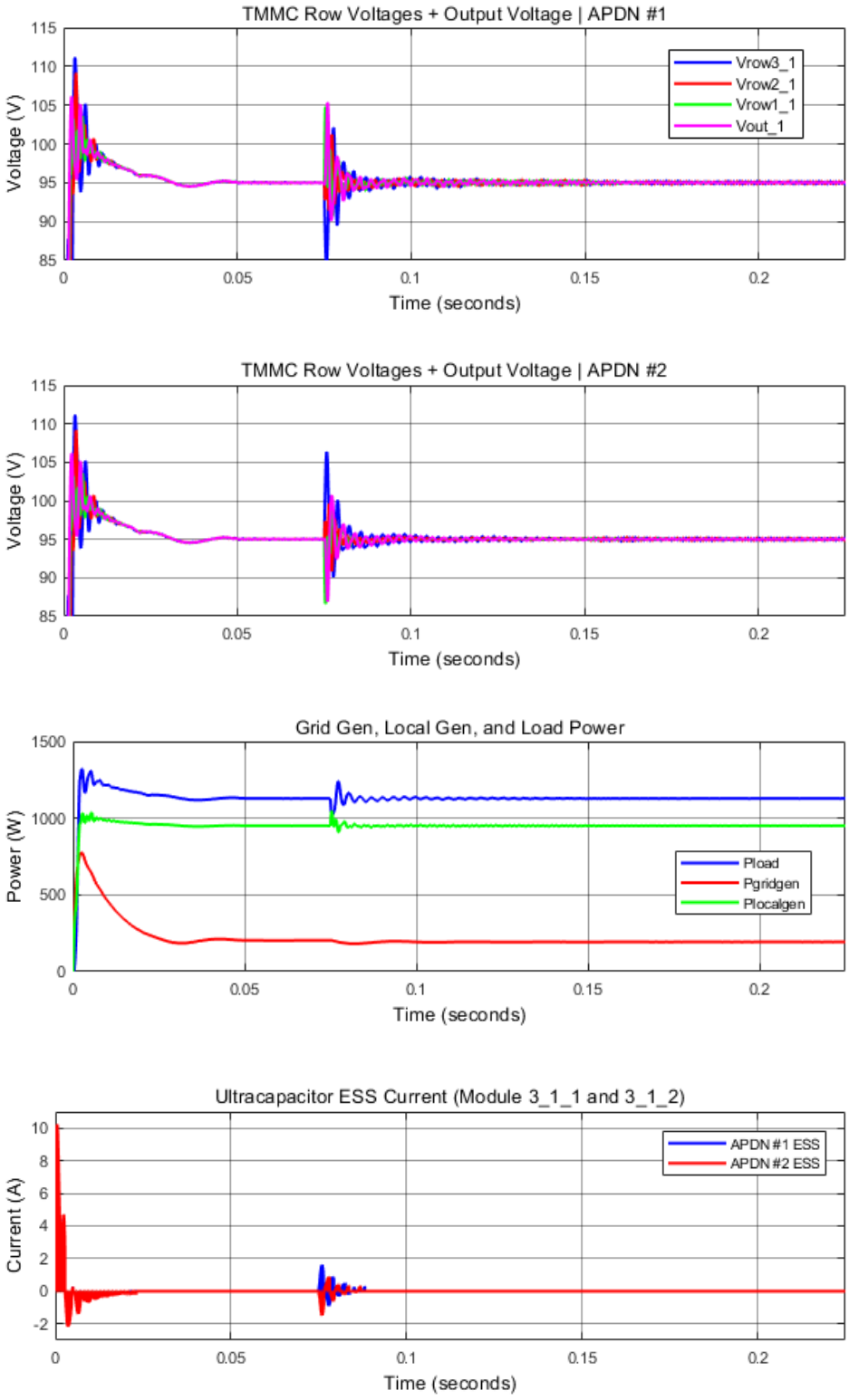

Figure 58. Case 1 Results: (from top to bottom) APDN Row Voltages; Load, Local, and Grid Powers, and Row 3 ESS Currents for both APDNs

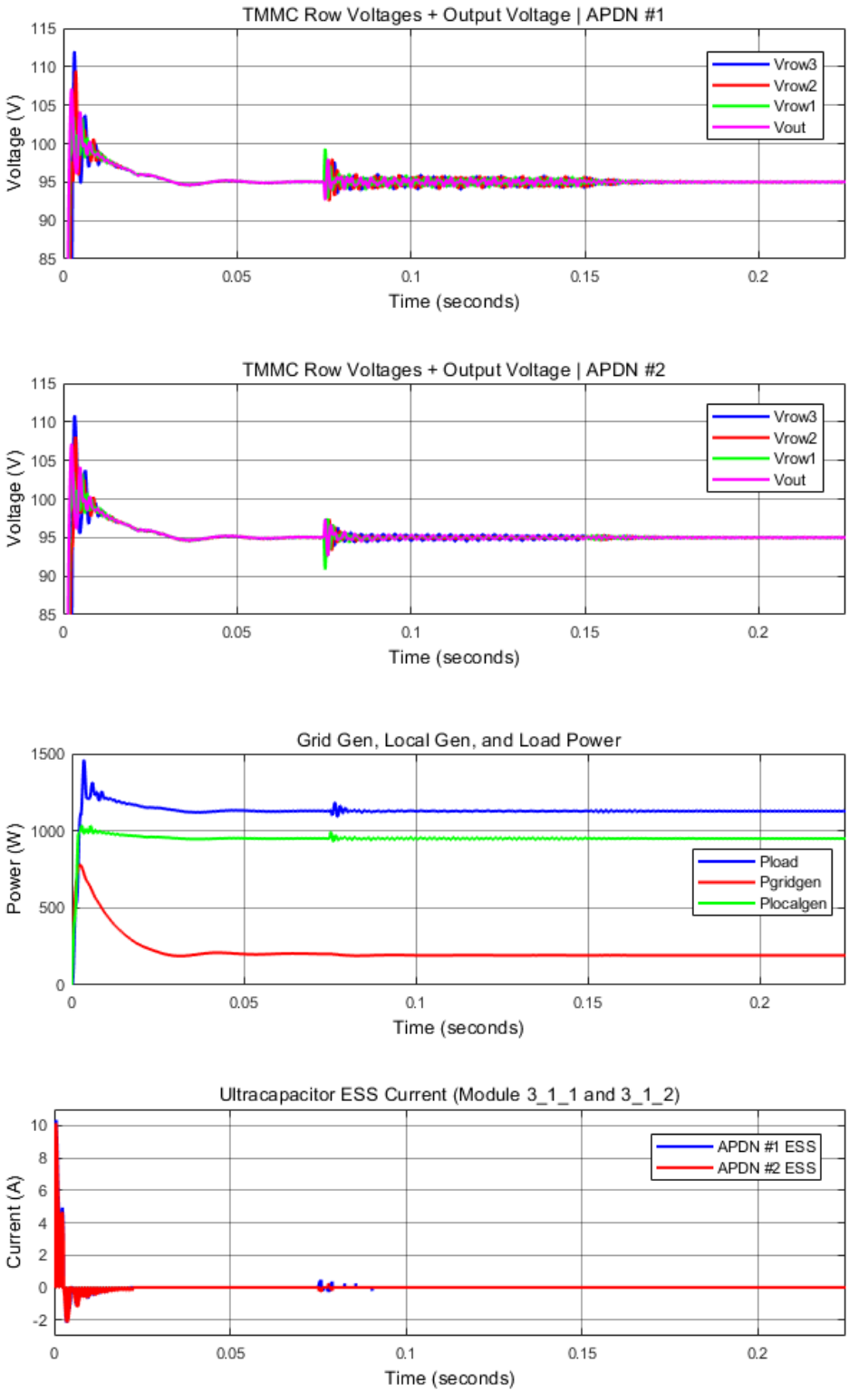

Figure 59. Case 2 Results: (from top to bottom) APDN Row Voltages; Load, Local, and Grid Powers, and Row 3 ESS Currents for both APDNs

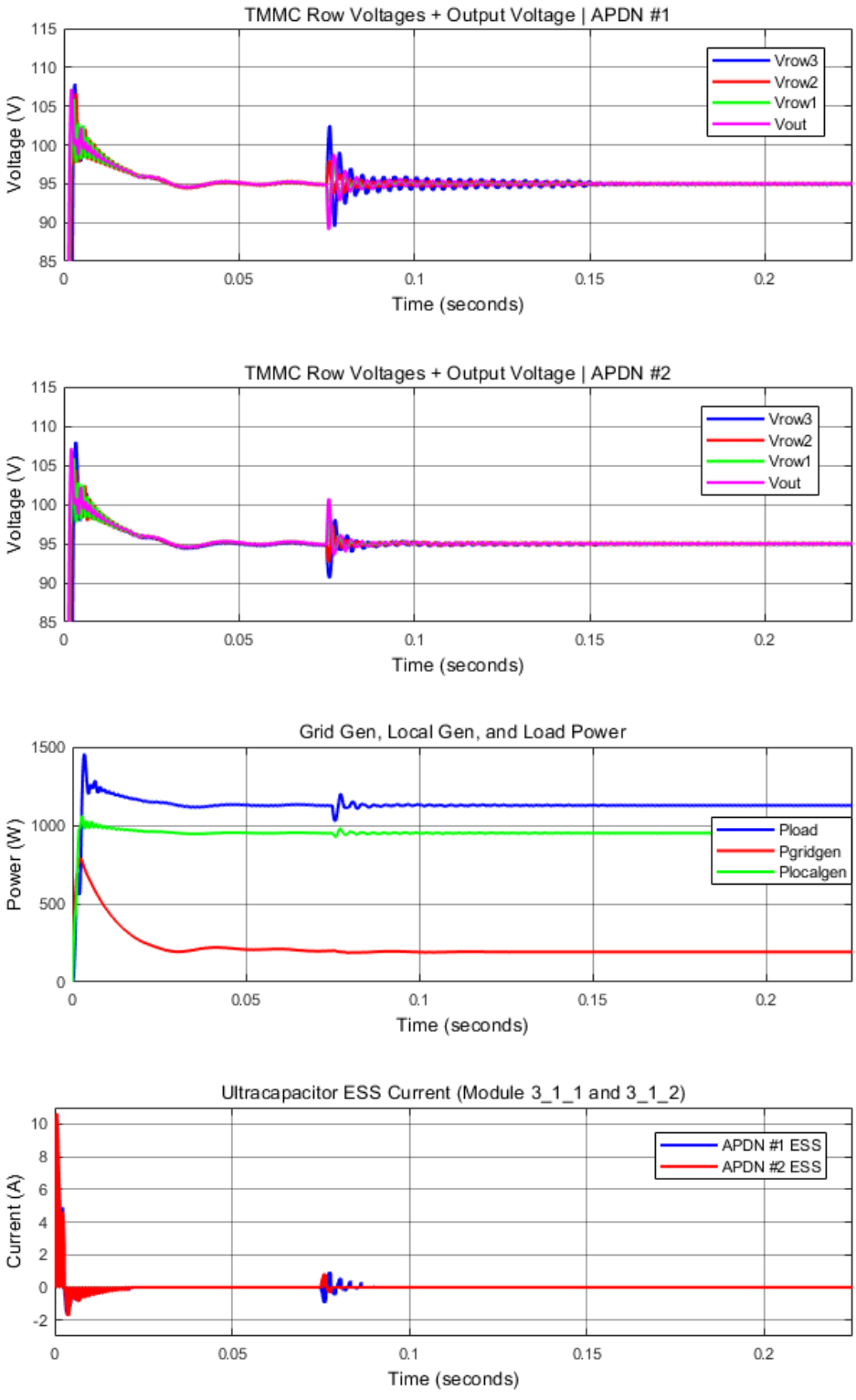

Figure 60. Case 3 Results: (from top to bottom) APDN Row Voltages; Load, Local, and Grid Powers, and Row 3 ESS Currents for both APDNs

Results for the three testcases resemble each other to varying degrees of magnitude. Each simulation sees a voltage overshoot at start-up with the worst-case example being case 1 around 115 V (121% of nominal voltage) and the best-case being case 3 around 107.5 V (113% of nominal voltage). This overshoot can be attributed to the ESS ultracapacitors responding to a perceived transient loss of power and attempting to achieve a module capacitor voltage between 94 and 96 V by injecting upwards of 10 A into each module. The next phenomenon occurs when APDN #2 disconnects from a direct connection to the local generation source at 0.075 s. The switched transient ΔV ranges from ~5 V for case 2, to ~15 V for case 1. The ultracapacitors once again respond to the voltage variance and rapidly discharge and charge opposite to the transient voltage ripple. The transient ripple then dissipates over the next 0.05 to 0.075 s based on the case before the local generation is reconnected to APDN #2. The dissipating ripples per case fall between the 94 V and 96 V voltage window and the ESS does not participate in the voltage regulation. Consistently between cases, APDN #2's voltage waveforms have a smaller transient ripple than those of APDN #1, which may be attributed to the purely resistive load on APDN #2 damping out the ripples. The load power has the largest power ripple across each case with case 3 having the largest load peak ripple of 174 W. The local generation for case 3 has a 55.3 W ripple and the grid generation appears mostly unaffected, which is to be expected as the grid would be the stronger source of the two.

The transient responses for the voltage waveforms of each APDN appears to have a mirrored response. When one APDN row of modules spikes high relative to the switched event, the other APDN's corresponding row of modules dips low. This dynamic is reflective of the current flowing through the two APDNs in opposite directions. APDN #1 is operating in step-up mode with the current flowing upward through the module rows supplied from the local generation

source, while APDN #2 is operating in step-down mode with current flowing downward through its module rows supplied from the grid generation and the local generation that just flowed through APDN #1. Throughout the simulation cases, the load power is visibly the summation of the local generation source, the grid generation source, and the summed ESS ultracapacitor currents. Relative to the ESS responses across the three cases, each case achieves stability within the 94 to 96 V range ($\pm$1.05%) for all but the 15 ms of the transient switched event.

Ultimately, each simulation shows that the APDN test bed model has a stable operating point and that the circuit returns to its nominal steady state voltage regardless of the location of the load or a potential load step change. The embedded energy storage helps to mitigate transients and support the system when either more power is requested from a load or when there is a surplus of power during a negative load step.

4.5 Availability Conclusions

This chapter evaluates an approach for calculating power supply availability using simultaneous minimal cut sets for a DC distribution system and explores the benefits of using this method. This approach can be performed with the incorporation of modular converter interfaces with embedded energy storage, referred to as APDNs. The embedded energy storage of these devices enables the system to ride through traditional system failures, such as the loss of a row of module(s) in the case of TMMC-APDNs, for a specified period of time, and therefore, produce a simultaneous second MCS for availability calculations. These availability results are compared to results where the second MCS are ignored to determine the availability calculation benefits of incorporating this second term. Industry accepted reliability data is used to perform the

calculations including a Monte Carlo analysis of the availability of each converter module over a distribution of defined converter component failure rates. These simulated results support the findings found in the availability calculations.

A testbed utilizing parallel APDNs, a “local” DC source, and an AC “grid” source is investigated to demonstrate the usefulness of the MCS availability calculation and the TMMC-APDN topology. The converter’s modularity promotes diverse power flow pathways minimizing single points of failure in the connected system. Moreover, the TMMC-APDN boasts a high-level of reliability and improved system availability due to its stacked and parallel module design. Based on the required use-case, the TMMC-APDN topology can be expanded to incorporate any number of rows of modules, and more importantly, any number of parallel modules per row to leverage the higher availability associated with parallel modules.

Using MCS theory and Monte Carlo analysis, the availability benefits of the converter’s design are quantified and validated within the defined test system across twelve test cases. Simultaneous MCS of APDN modules and ESS are accounted for providing further enhanced availability results. The test distribution network demonstrates an availability range of 3- to 13-nines based on the flow of power and system configuration—with the DC source subcases consistently producing better results. With the inherent availability of the APDN due to its redundant and diverse circuitry, critical and sensitive systems with large downtime costs that utilize a large DC-based infrastructure like data centers would benefit greatly from this effective availability-enhancing solution.

5.0 Dissertation Conclusions and Future Work

This dissertation has presented a method of redesigning DC distribution networks by exploring the use of MIMO DC-DC APDNs for managing power flow and power quality levels. These APDNs form a network of nodes enabling a reconfigurable distribution grid architecture with power routing and power buffering capabilities. The work performed above analyzes the performance of the TMMC-APDN topology through the simulation of the converter individually and as part of a network of APDNs, the experimental testing of the modules design through hardware realization, and the investigation of the availability benefits the topology provides to connected sources and loads. Methods were crafted and compared for reducing the computational burden of simulating a large system of APDNs using an averaged model of the TMMC and will be considered for future work. Aside from the investigation of simulation modeling approaches, an investigation into the controller design to understand how to best make use of the two-loop control design was performed and supported by stability analysis around defined operating points. The stability analysis demonstrated that all system poles were on the left-hand plane with a distinct separation of "fast" and "slow" poles relative to the inner-loop current controller and outer-loop voltage controller, respectively. From a hardware perspective, TMMC-APDN module PCBs were designed, tested, and compared to their simulation results. This work can be expanded to test multiple module boards connected in different TMMC-APDN configurations to further demonstrate the merits of the topology. Looking at the impact of APDNs upon a larger system, availability analysis of a two TMMC-APDN system was explored validating the improvements to the availability of connected sources and loads. These benefits can be attributed to the converter's modularity providing redundant pathways for power to flow between multiple inputs and outputs.

At the conclusion of each component of this work, the results reinforce the benefits of creating a reconfigurable distribution network and how it can more effectively meet the needs of the dynamically changing landscape of distribution network power generation and load profiles. Work must be continued to explore more multi-port designs and how reconfigurable grids can strengthen the operation of distribution networks across various industries.

Appendix A

Matlab Script – 3-Level Step-Down TMMC-APDN Closed-Loop Model Stability Analysis

```
% Alvaro Cardoza
% 3-Level Step-Down TMMC-APDN Closed-Loop Model and Stability Analysis

clear;
close all;
clc;

format short

% Symbolically Initialize System Variables
syms vin dvin io
syms vc0 vc1 vc2 iL11 iL12 iL13 iL21 iL22 iL31 avc0 avc1 avc2 aiL11 aiL12
aiL13 aiL21 aiL22 aiL31
syms vc0ref vc1ref vc2ref d11 d12 d13 d21 d22 d31
syms kiv kic kpv kpc C L RL

%% 3-Level Step-Down TMMC Dynamics%%

% System States -> vc0, vc1, vc2, iL11, iL12, iL13, iL21, iL22, iL31, avc0,
avc1, avc2, aiL11, aiL12, aiL22, aiL21, aiL22, aiL31
% First the general form equation for Jacobian is found, then based on the
computed equilibrium points, the Jacobian at the equilibrium is computed

% Approximate Duty Cycle Calculation (Based on Row Cap Voltages)
d1apx = vc1/(vc0+vc1);
d2apx = vc2/(vc1+vc2);
d3apx = (vin-(vc0+vc1+vc2))/(vin-(vc0+vc1));

% Voltage Control Loop - PI Output Calculation (Voltage Control Signal)
vc0Ctrl = avc0 + kpv*(vc0ref - vc0);
vc1Ctrl = avc1 + kpv*(vc1ref - vc1);
vc2Ctrl = avc2 + kpv*(vc2ref - vc2);

% Current Control Loop - Inductor Current Reference Framework (Vc - IL
relationship)
Z = [3 0 0; 0 2 0; 0 0 1];                                  % IL - # Parallel
Modules per Row (1,2,3)
W = [3 0 0; 0 3 0; 0 0 2];                                  % Vc - # Parallel
Modules per Row (0,1,2)
Md = [1 -(1-d2apx) 0; -d1apx 1 -(1-d3apx); 0 -d2apx 1];     % Duty Cycle
Relationships per row (1,2,3)

Qm = [1 1 0; 0 1 1; -1/3 -1/3 1/2];                         % Adjacent Row
Capacitor Dynamic Relationship (dvc/dt)
Td = Qm\Md;                                                 % Step-Down
Configuration Transition Matrix
```

```
% Inductor Current References Calculation
iLrefM = Z\Td\W*[vc0Ctrl; vc1Ctrl; vc2Ctrl];
iL1ref = iLrefM(1);
iL2ref = iLrefM(2);
iL3ref = iLrefM(3);

% Current Control Loop - PI Output Calculation (Duty Cycle)
d11 = aiL11 + kpc*(iL1ref - iL11);
d12 = aiL12 + kpc*(iL1ref - iL12);
d13 = aiL13 + kpc*(iL1ref - iL13);
d21 = aiL21 + kpc*(iL2ref - iL21);
d22 = aiL22 + kpc*(iL2ref - iL22);
d31 = aiL31 + kpc*(iL3ref - iL31);

% Capacitor Dynamic Equations per Row (dvc/dt)
dvc0 = (1/(3*C))*((iL11 + iL12 + iL13) - (iL21*(1-d21) + iL22*(1-d22)) - io);
dvc1 = (1/(3*C))*(-(iL11*(d11) + iL12*(d12) + iL13*(d13)) + (iL21 + iL22) -
iL31*(1-d31));
dvc2 = (1/(2*C))*(-(iL21*(d21) + iL22*(d22)) + iL31);

% Inductor Dynamic Equations per Row (diL/dt)
diL11 = (1/L)*(vc1*d11 - vc0*(1-d11) - iL11*RL);
diL12 = (1/L)*(vc1*d12 - vc0*(1-d12) - iL12*RL);
diL13 = (1/L)*(vc1*d13 - vc0*(1-d13) - iL13*RL);
diL21 = (1/L)*(vc2*d21 - vc1*(1-d21) - iL21*RL);
diL22 = (1/L)*(vc2*d22 - vc1*(1-d22) - iL22*RL);
diL31 = (1/L)*((vin-(vc0+vc1+vc2))*d31 - vc2*(1-d31) - iL31*RL);


%% Integrator State Equations %%

% Capacitor Voltage Integrator States
davc0 = kiv*(vc0ref - vc0);
davc1 = kiv*(vc1ref - vc1);
davc2 = kiv*(vc2ref - vc2);

% Inductor Current Integrator States
daiL11 = kic*(iL1ref - iL11);
daiL12 = kic*(iL1ref - iL12);
daiL13 = kic*(iL1ref - iL13);
daiL21 = kic*(iL2ref - iL21);
daiL22 = kic*(iL2ref - iL22);
daiL31 = kic*(iL3ref - iL31);

% Closed-Loop System States (and their Derivatives)
x_cl = [vc0; vc1; vc2; iL11; iL12; iL13; iL21; iL22; iL31; avc0; avc1; avc2;
aiL11; aiL12; aiL13; aiL21; aiL22; aiL31];
dx_cl = [dvc0; dvc1; dvc2; diL11; diL12; diL13; diL21; diL22; diL31; davc0;
davc1; davc2; daiL11; daiL12; daiL13; daiL21; daiL22; daiL31];


%% Jacobian Calculation of System States %%
% Linearize the Closed-Loop System by taking the Jacobian of the State
Derivatives (dx_cl) with respect to the States (x_cl)
```

```
% Jacobian Calculation in Terms of System Variables (General Form)
jacob_dx = jacobian(transpose(dx_cl), transpose(x_cl));


%% Equilibrium Point System Values %%

% Test Parameters to Find Better Results
% Voltage Loop PI Parameters
Kpv = 0.01;       % Original Value: 0.1/0.162
Wz_PI_V = 520;      % Original Value: 220/1200
Kiv = Kpv*Wz_PI_V;

% Current Loop PI Parameters
Kpc = 0.05;        % Original Value: 0.03/0.17/0.025
Wz_PI_C = 4080;        % Original Value: 580/9000/400
Kic = Kpc*Wz_PI_C;

% Module Circuit Parameters
Ceq = 60e-6;
Leq = 560e-6;
RLeq = 25e-3;
% RLeq = 0;

% System Parameter Values
Vin = 380;
Vo = 95;
Po = 1000;
Io = Po/Vo;

% Control Input - Capacitor Voltage Reference Values
Vc0ref = 95;
Vc1ref = 95;
Vc2ref = 95;

% In Equilibrium -- Capacitor Voltages = Reference Voltage Values
Vc0 = Vc0ref;
Vc1 = Vc1ref;
Vc2 = Vc2ref;

% Duty Cycle Calculation (Based on Capacitor Voltages)
D11 = Vc1/(Vc0+Vc1);
D12 = D11;
D13 = D11;
D21 = Vc2/(Vc1+Vc2);
D22 = D21;
D31 = (Vin-(Vc0+Vc1+Vc2))/(Vin-(Vc0+Vc1));


%% Iteratively Solve for Inductor Current Values over a Range of Input/Output
Values (Disturbance Terms) %%

% Range of Disturbance Terms (Choose Range of Values to Solve)
```

```
% Io_array = -30:7.5:-7.5;
% Io_array = -30:15:30;
% Io_array = [-30 -15 15 30];
Io_array = [-30 -22.5 -15 -7.5];
% Io_array = [30 22.5 15 7.5];
% Io_array = [7.95 9.49 11.51];
% Io_array = [-7.5];

I1_array = zeros(length(Io_array));
% I1_array = -3:1:3;
% Io_array = zeros(length(I1_array));
I2_array = zeros(length(I1_array));
IESS1_array = zeros(length(I1_array));
IESS2_array = zeros(length(I1_array));
IESS3_array = zeros(length(I1_array));

% Initialize Arrays of Non-Io Disturbance Terms
j = 0;
k = 0;
l = 0;
m = 0;
n = 0;

% Iteratively Solve for Inductor Current Steady State Values
for i = 1:length(Io_array)

    % Iterate through range of other disturbance values (i.e. i(1,2),
IESS(1,2,3))
    j = j + 1;
    k = k + 1;
    l = l + 1;
    m = m + 1;
    n = n + 1;

    % Use One Current Value at a Time from the Corresponding Disturbance Term
Array
    Io = Io_array(i);
    I1 = I1_array(j);
    I2 = I2_array(k);
    %     IESS1 = 3*IESS1_array(l);
    %     IESS2 = 2*IESS2_array(m);
    %     IESS3 = 1*IESS3_array(n);

    % Assuming Equilibrium -- Kpc(ILref-IL) = 0 and therefore, D (Current PI
Output) = AiL (Current PI Integrator State)
    AiL11 = D11;
    AiL12 = D12;
    AiL13 = D13;
    AiL21 = D21;
    AiL22 = D22;
    AiL31 = D31;

    % Create Symbols for System of Inductor Current Equations
    syms IL11 IL21 IL31
```

```
    % Solve the System of Inductor Current Equations (3 Equations, 3
Unknowns)
    eqns = [IL31 == (Io - 3*(IL11)*(1-D11)) / (D31),...
        IL21 == (1/2)*(Io - 3*IL11*(1-D11) + IL31*(1-D31)) / (D21),...
        IL11 == (1/3)*(Io + 2*IL21*(1-D21))];
    vars = [IL31, IL21, IL11];

    [ILrow3, ILrow2, ILrow1] = solve(eqns, vars);

    % Assume Parallel Modules Have Identical Inductor Current Values
    IL31 = ILrow3;
    IL21 = ILrow2;
    IL22 = ILrow2;
    IL11 = ILrow1;
    IL12 = ILrow1;
    IL13 = ILrow1;

    % In Equilibrium -- Inductor Currents = Reference Current Values
    IL3ref = IL31;
    IL2ref = IL21;
    IL1ref = IL11;


    %% Compute Td matrix (Defined at the Top in Terms of Voltages) %%

    % Substitute Equilbrium Voltage Terms
    Td_equib = subs(Td, [vin, vc0, vc1, vc2], [Vin, Vc0, Vc1, Vc2]);

    % Capacitor Voltage Control Signals Calculation
    VcctrlM = W\Td_equib*Z*[IL1ref; IL2ref; IL3ref];
    Vc0ctrl = VcctrlM(1);
    Vc1ctrl = VcctrlM(2);
    Vc2ctrl = VcctrlM(3);

    % Assuming Equilibrium -- Kpv(Vref-Vc) = 0 and therefore, VcCtrl (Voltage
PI Output) = Avc (Voltage PI Integrator State)
    Avc0 = Vc0ctrl;
    Avc1 = Vc1ctrl;
    Avc2 = Vc2ctrl;


    %% Jacobian Calculations (Subbed and Solved at the Defined Equilibrium
Point(s)) %%

    jacob_dx_solve = subs(jacob_dx, ...
        [vin, io, vc0, vc1, vc2, iL11, iL12, iL13, iL21, iL22, iL31, avc0,
avc1, avc2, ...
        aiL11, aiL12, aiL13, aiL21, aiL22, aiL31, vc0ref, vc1ref, vc2ref,
d11, d12, d13, d21, d22, d31, kiv, kic, ...
        kpv, kpc, C, L, RL], ...
        [Vin, Io, Vc0, Vc1, Vc2, IL11, IL12, IL13, IL21, IL22, IL31, Avc0,
Avc1, Avc2, ...
        AiL11, AiL12, AiL13, AiL21, AiL22, AiL31, Vc0ref, Vc1ref, Vc2ref,
D11, D12, D13, D21, D22, D31, Kiv, Kic, ...
        Kpv, Kpc, Ceq, Leq, RLeq]);
```

```
    %% Eigenvalue Calcuations (System Poles) %%

    EigenVals = eig(jacob_dx_solve);

    %% Plot Results %%

    if i == 1
        figure('NumberTitle', 'off', 'Name', 'Closed Loop Eigenvalues');
        set(gca, 'fontsize', 10);
        xlabel('Real Axis (s^{-1})', 'FontSize', 12);
        ylabel('Imaginary Axis (s^{-1})', 'FontSize', 12);
        title('TMMC-APDN Step-Down Closed-Loop Eigenvalues', 'FontSize', 12);
        %         xlim([-40000 0]);
        %         ylim([-4000 4000]);
        hold on;
    end

    color = ["black" "red" "blue" "magenta" "green" "cyan" "yellow"];
    EigenSort = sort(double(EigenVals),'ComparisonMethod','real');

    for n = 1:length(EigenSort)
        if n <= 12
            symbol = '+';
        else
            symbol = 'o';
        end

        scatter(real(EigenSort(n)), imag(EigenSort(n)), symbol, color(i));
        legend('Io = 30 A', 'Io = 22.5 A', 'Io = 15 A', 'Io = 7.5 A', [-90, -
100, 850, 650]);
        set(gcf,'position',[250,250,600,400])


    end

end
hold;
```

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