Flying Capacitor Multilevel Flyback Converter

by

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This work analyzes and justifies the capabilities of the flying capacitor multilevel flyback converter (FCMFC) structure for DC-DC power conversion. The proposed converter has been analyzed mathematically for theory of operation and simulated extensively in the process. Furthermore, the theoretical and simulation backed efforts have been proven using a series of hardware prototypes to ensure the analysis. This new converter utilizes the very commonly used flyback converter as its core structure. The secondary side filter has been replaced with a series of switch-diode-capacitor (SDC) cells that cycle the flying capacitors for improved overall converter performance. Major improvements are seen for converter efficiency and voltage gain capability, making the FCMFC a promising candidate as a DC converter, that expands the capabilities and thus applicability of the flyback converter. Use of the FCMFC structure gives a designer more variability in the design and expands the range of use for commercial off-the-shelf (COTS) flyback transformers. This can be very useful for a designer by eliminating the need to venture into the magnetic design of a new transformer, which can be very time consuming and complicated. Magnetic component companies also have limited selection range for magnetic components, especially for transformers because of the expense involved to design and test. FCMFC balances energy between the core transformer and flying capacitors, allowing it to handle more power with a lower input ripple current. The input MOSFET switch, that is core to the flyback converter and FCMFC, experiences a reduced stress of operation because of the proposed structure. The secondary side SDC components distribute voltage gain which lowers their voltage stress. Many

other multilevel structures have been designed with great success for this reason, however, none of those structures see the same voltage gain benefit that FCMFC has, making it particularly unique. For this reason, the FCMFC has been the research focus and is the proposed topology. This work will analyze and exemplify the validity of FCMFC to justify the contribution to the field of power electronics.

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Acknowledgments

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I would like to give my advisor, Dr. Brandon Grainger, a very well-deserved acknowledgement. I've been advised by Dr. Grainger since 2016 upon starting a master's degree. The first class I had with Dr. Grainger, power electronics, inspired me to pursue this field of study for all my graduate work. Until this point in my education I had never learned so much so quickly on such a challenging and mathematically rigorous topic. Dr. Grainger's dedication to students and their education made this possible. His teaching style for this subject was matched very well. He would provide the class with slides that were partially filled out. He would use this to guide the class through the lecture step-by-step, writing along with the students. This was invaluable given the mathematical complexity of the material.

It was months after the class occurred that I found out he prepares for each of his lectures ahead of time; sometimes spending hours to rehearse material and equations to ensure a smooth lecture. This is something I had never seen or heard of a professor doing. Over the years of working with Dr. Grainger I also saw how he applies his research experience in the classroom which is what inspired me to pursue my current field of study. Professors like Dr. Grainger are very rare. Typically, a research professor will care more about research than teaching or a dedicated teaching professor won't know much about academic and industrial research. Dr. Grainger has positioned

himself inside and outside the classroom to blend the two areas and inspire students like myself to pursue intense and rewarding fields of study. I felt well-equipped after his course to pursue power electronics and in my time at the university have published five research articles on the subject under his guidance. Dr. Grainger accompanied me across country for my first conference paper which I defended in Portland, Oregon. I was very nervous to get up in front of the elite researchers, but he assured me of my work and presentation skills.

In my graduate research time, I realized how lucky I am to have such a helpful and involved professor. I never felt alone in the PhD process which I learned is quite common for the average graduate student, but not for Dr. Grainger's. My time and experience with Dr. Grainger has led me to a position with Eaton Research Labs. My career path is now underway, and I am very grateful for his role as an inspiring educator.

A special thanks to Eaton and the Power Systems Experience Center (PSEC) team. As an intern working for Dan Carnovale, I was able to learn an invaluable amount of industry information from technical details to marketing and business skills that are not available in academia. This work kept me motivated and gave real-world perspective to my academic studies. Also, the PSEC was used for all converter testing which I am very thankful for. Different voltage and configurations were at my disposal in the testing process.

I would like to thank Dr. Reed for his efforts in the creation of the Electric Power Systems Lab and the Energy Grid Institute. It has been an honor to work for these institutions and I am grateful for all I have been able to learn and accomplish. My colleagues in the lab have been supportive throughout my graduate years and I'm grateful for the friendships I've made along the way. My good friend Thomas "Thom" Cook was a great friend to go through this experience with inside and outside the lab. His advice and guidance in the PCB design process within this work

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1.0 Directive I. Capability Analysis

This directive proposes the flying capacitor multilevel flyback converter (FCMFC) for isolated, high-gain, DC-DC power conversion. This first step is to analyze and then prove what this structure is capable of in steady-state. This directive will prove that the proposed converter topology is worth further research consideration, leading to the latter directives. Three converters, one flyback as a control and the two proposed FCMFCs, have been designed and tested to prove gain and efficiency improvements. The FCMFC converters prototypes achieve higher gain and efficiencies relative to a flyback design using the same components. The stress of the input and output switches is reduced because of the fractioning of the output voltage across multiple output stages. A bootstrap circuit was used for the FCMFC converters to maintain a key flyback converter benefit, the primary to secondary isolation. The operating parameters are 5V to 40V boosting for a 10W load at 250kHz. Utilizing the same transformer, the flyback converter control prototype achieves 78% efficiency while the proposed FCMFC converters reach 85% and 82% efficiency, even with the added isolated power, gate drive and bootstrap circuitry. Duty cycle sweeps were done to show the FCMFC converters have double and triple the gain of the flyback and still increase near the 90% duty cycle flyback threshold. Additional testing was done at 100kHz, 250kHz, 452kHz, and 500kHz. This effort also proves that FCMFC achieves natural voltage balancing across flying capacitors.

1.1 Literature Review & Motivation

Direct current (DC) is a staple of the modern world. Not only are most of our loads powered with direct current but harnessing renewable energy, photovoltaic in particular, is achieved using DC. The power is processed using power electronics that can convert one DC voltage to another and then eventually invert that into usable AC power. A significant portion of that AC power will be rectified back to DC for use in consumer electronics such as a television, gaming station, cell phone or even LED lighting. It was only recently that one of the top gaming consoles managed to incorporate its DC power supply into the console and not as a large brick shape converter attached to a power chord. Power conversion using DC-DC converters is an expanding field that continuously demands smaller and more efficient products.

1.1.1 DC Power Conversion

Solar energy has been one of the leading sources of added power capacity in the recent years. It has held steady at about 30% of the added capacity year over year since 2015. Photovoltaic solar produces DC at around $40V_{DC}$ per panel which then needs boosted to around $400V_{DC}$ where it can be inverted to the $120/240V_{AC}$ required for a home in the United States. Pairing energy storage with solar power is required to have stable grid operation. The energy storage acts as an immediate buffer for times of cloud cover to prevent large and frequent power transients on the local utility. Electric vehicles also come into play as energy storage and added load on the system which require DC power converters. The energy infrastructure is changing to include significant increase of generation and loads that utilize DC power. Along with this the demand grows for highly efficient and reliable DC power converters. Other applications for DC converters span from

small implantable medical devices, to microgrids, all the way up to industrial power supplies and transportation [1,2]. The energy world is evolving to include these more complicated devices and so grows the field of power electronics to meet this challenge.

1.1.2 The Flyback Converter and the Need for Isolation

One popular converter that was invented in 1932 by Alan Blumlein for resonant electron beam scanning for televisions. The circuit required a linearly ramping current (input) that could flyback and repeatedly scan, hence the name. The flyback has since been adapted for DC power conversion where it sees many benefits including but not limited to: isolation, high gain, and simplicity.

Flyback topologies are widely utilized for their low cost and high versatility in power conversion, boasting a wide input and output voltage range of operation [8, 9]. The flyback converter is a good candidate for high step-up voltage conversion that has the added benefit of magnetic isolation. The flyback is a popular isolated converter for renewable applications but can suffer significant switch and diode stress, limiting its use [10]. Active clamp switching schemes are utilized to lower the stress on the primary switch that require advanced control techniques to achieve zero-voltage/current switching for example [11, 12]. These active circuits work well to reduce primary FET stress but FCMFC does this inherently by utilizing the secondary flying capacitor voltage cells to reduce the primary reflected voltage. Utilization of the proposed multilevel flying capacitor variation expands the power potential of this converter because of the decreased stress and increased efficiencies. The flyback converter has not been explored for multilevel operation and is the proposed topology.

To achieve high voltage gain using flyback converters, designers utilize a high turns ratio [13, 14]. This requires detailed custom magnetic design and still yields high stress ratings for the primary FET and secondary output diode. Transformers are often custom made for a particular purpose, but many off-the-shelf options exist and can be utilized in an FCMFC structure to cover a broader application range than what a simple flyback could cover. This is made possible by the increased voltage gain and reduced primary FET stress of the proposed topology. Modifications to the flyback converter using boost converters and other voltage multipliers are also common in this space [15-19]. Modified boost converters are also utilized [20] but with limited gain. All the modified flyback converters will use a moderate turns-ratio and get the remaining gain from a separate converter stage, increasing control system complexity. The FCMFC can achieve high voltage gain using a phase shifted pulse width modulation scheme for the switch-diode-capacitor (SDC) secondary side stages. FCMFCs have the benefit of increased voltage gain, which is not common amongst other flying capacitor topologies such as [3,4]. This work proves that adding one flying capacitor stage will double the available voltage gain of the standard flyback converter, two will triple the gain and this trend continues for higher order FCMFCs which also allows the main input switch to operate at lower duty cycle and stress. This work seeks to extend the capability of the flyback converter by increasing voltage gain and efficiency.

1.1.3 Multilevel Converters

High frequency multilevel converters have been developed to meet the stringent requirements of voltage boosting applications by maximizing power density and efficiency. Flying capacitors (FC) have been used to enhance the capabilities of basic power electronic topologies such as the multilevel boost converter [3]. The multilevel structure spreads voltage gain across

individual switching cells containing the FC and the benefits include increased efficiency, lower device stress, and higher power density [4]. Multilevel structures have also been implemented for the buck [4,5] and buck-boost [7] converters with correspondingly high efficiencies.

Challenges arise with multilevel converters, particularly balancing the FC voltages. Voltage imbalance comes from variance in component values and gate triggering time delays, an issue that is exacerbated with higher level converters. While some converters experience some natural balancing, any variation directly hinders the lower component stress requirements. Control methods have been developed to solve this issue and prevent the premature failure of an individual stage. Natural balancing has been achieved by varying the switching scheme [21]. Active balancing has been achieved through value valley current detection and a constant effective duty cycle to account for the light load condition [22]. This work presents the FCMFC and shows that it achieves natural flying capacitor voltage balance, which is key to the reduced voltage stress seen by the semiconductor devices.

1.1.4 FCMFC Introduction

A generalized FCMFC is shown in Figure 1 with a single SDC stage outlined. Multiple converters can be derived from this general form for N levels where (N-1) is the number of capacitors of a given converter. The double wound inductor ("transformer") provides for higher gain capability but is not the focus of this work. The FCMFC achieves higher output voltages because of the significant gain increase provided by flying capacitors, while maintaining high efficiencies.

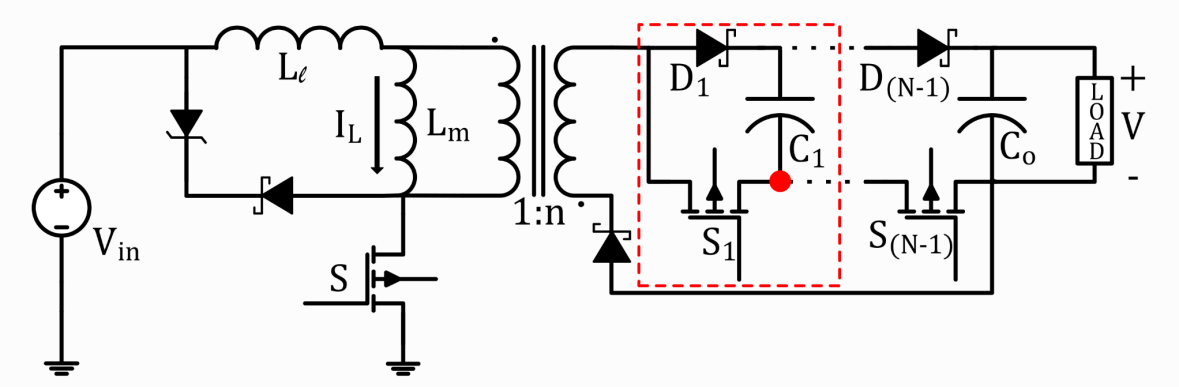


Figure 1. Flying Capacitor Multilevel Flyback Converter General Form

From this work emerges a new DC power converter that can reach higher efficiency and voltage gain than the very popular flyback converter. The contribution of this work is successful operational analysis and implementation of the first functioning FCMFC for DC-DC power conversion. It proves the steady state operating equations hold true and that natural voltage balance is achieved which allows for lower device voltage stresses. Section 1.2 will layout the switching operation of the new topology and steady-state equations. Section 1.3 explains the design of the two FCMFC prototypes and the one flyback converter used as a control group for comparison. This allows direct verification that using the same active and passive devices improves the gain capability and efficiency of the converter which can be seen with a corresponding duty cycle decrease for the proposed design of 5V to 40V. Section 1.4 presents the results and compares to theoretical values. Section 1.5 will conclude research Directive I with a brief discussion of implications and justification to continue research into a comprehensive loss model for the new topology.

1.2 Theory of Operation

Switching of FCMFC is done using phase shifted pulse width modulation (PSPWM) in continuous conduction mode. This mode is where the gain, stress, and efficiency benefits lie. Discontinuous conduction is not as advantageous but will be explored later in this work.

1.2.1 Switching States and Charging Action

The operation of the flying capacitor multilevel flyback converter is shown in Figure 2, Figure 3, and Figure 4. Note that this is the simplest FCMFC, $N = 3$ (or N3) voltage levels (2 capacitors: 1 flying and 1 output) but the operation would be the same for higher level devices. Higher level devices add 2 switching states per flying capacitor, one to charge the magnetizing inductance and another to discharge into the extra flying capacitor. The primary MOSFET (*S*) sets the pace of the switching for the FCMFC. The converter is controlled using PSPWM shown in Figure 5. When the input primary switch is OFF, (*N*-2) of the secondary switches will conduct to charge a flying capacitor stage.

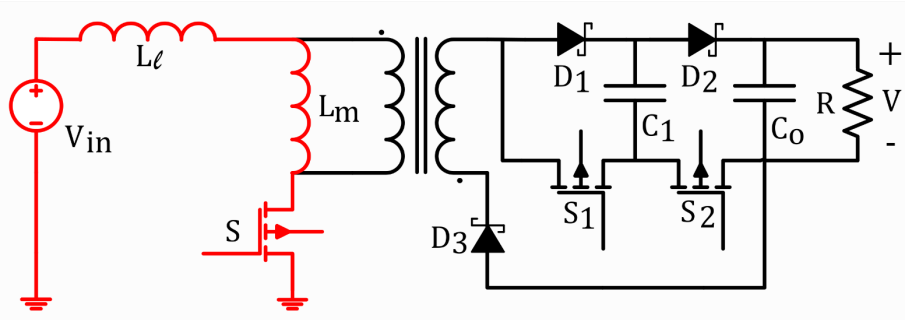


Figure 2. States 1 and 3 of FCMFC Operation: Charging L_m

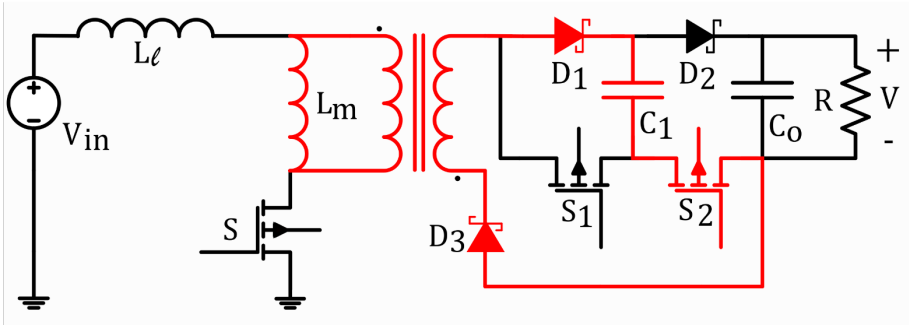


Figure 3. State 2 of FCMFC Operation: Charging C_1

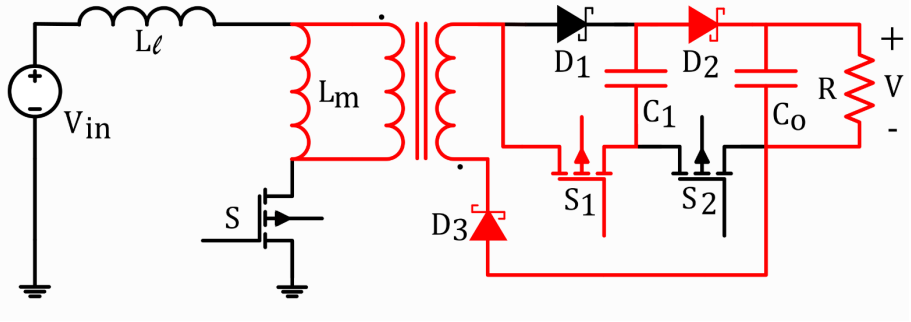


Figure 4. State 4 of FCMFC Operation Output Stage: Charging C_O

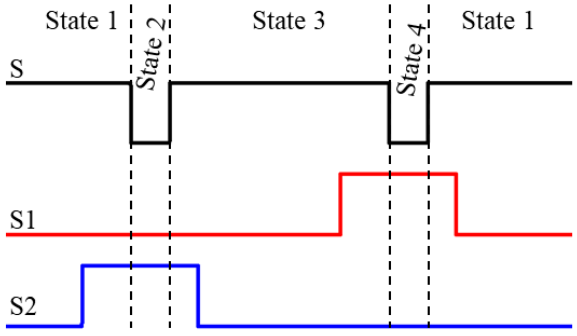


Figure 5. Phase Shifted Pulse Width Modulation

With *S* ON, the magnetizing inductance of the double wound inductor will charge for DT_s shown in Figure 2, where *D* is the duty cycle of input switch *S*, and T_s is the switching period or inverse of the switching frequency f_s. During this stage, secondary conduction through the body diode of the FETs is prevented by the addition of diode D_3. This diode could later be removed with

the addition of GaN and forced OFF states of the FETs. Next, *S* turns OFF and S_2 turns ON with S_1 OFF, shown in Figure 3. In this stage the inductor solely charges the flying capacitor C_1 through D_1, S_2, and D_3. The next state is the same as the first and shown in Figure 2, where the inductor charges again. Finally, the output stage happens in Figure 4 where *S* and S_2 are OFF and S_1 is ON. In this state notice the current flowing up through the negative end of C_1 and through D_2 into the output capacitance and then back through D_3. The energy of the output capacitor is boosted by the inductor and flying capacitor. A simplified charging circuit is shown in Figure 6, where the inductor and flying capacitor energy are being used to charge the output capacitance and supply the load power. This is the energy multiplication effect that leads to higher gains as shown in (1.1), the voltage conversion ratio derived using inductor volt-second balance. Note that the flyback converter is the simplest FCMFC (the N2 case) and this equation becomes the same as the conversion ratio for a flyback converter. For a higher *N* level structure this process would happen with each flying capacitor charging the next until the output capacitor is charged as shown in Figure 6, where the flying capacitor would be $C_{2,3,4, \text{ etc.}}$

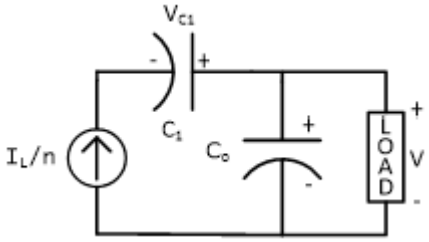


Figure 6. FCMFC Output Charging Circuit Diagram

$$M(D) = \frac{V}{V_{in}} = \frac{n(N\text{-}1)D}{1\text{-}D} \qquad (1.1)$$

To further illustrate the charging states for higher level converters, Figure 7 shows PLECs simulation waveforms of a N = 5 level converter, which has four capacitors. Notice the inductor current shown charging and discharging with each switching sub-cycle. Each charging state is labeled a-d which corresponds to the simplified charging circuit diagrams shown in Figure 8. Each SDC stage in series with the inductor will charge the following SDC stage until the output is reach and recharged. These four sub-cycles make up one complete switching cycle of the FCMFC.

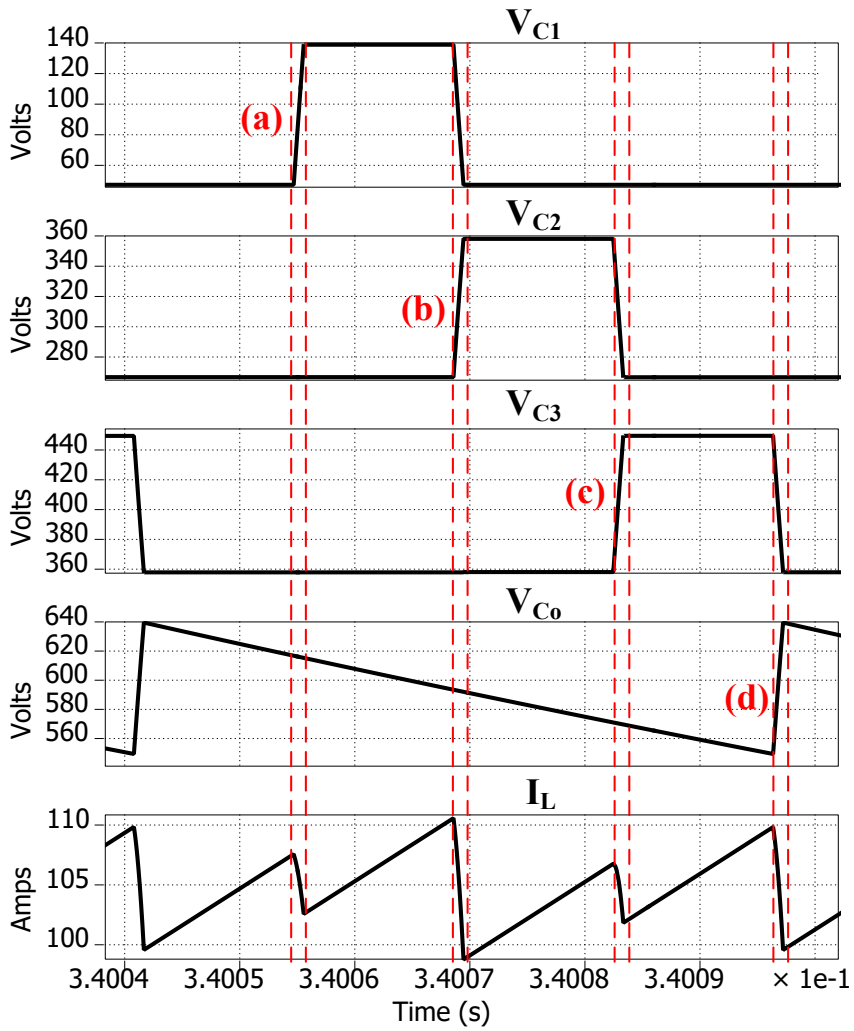
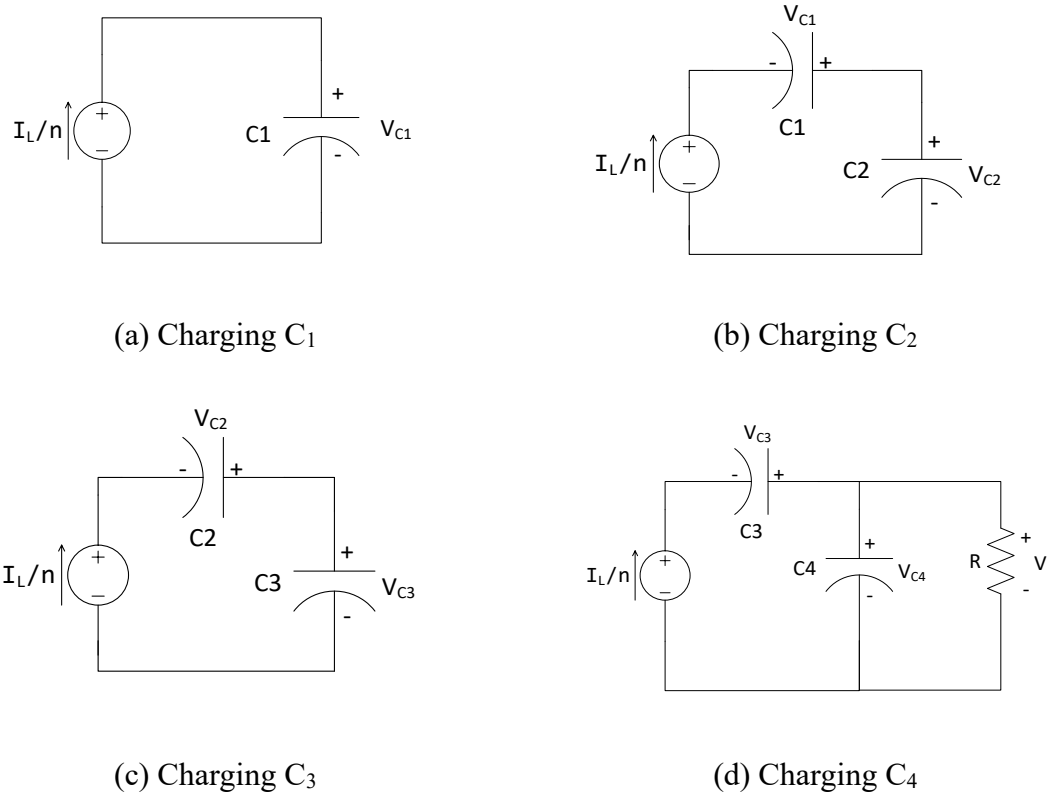


Figure 7. Stage Voltages and Inductor Current; N = 5 Case



(a) Charging C_1 (b) Charging C_2

(c) Charging C_3 (d) Charging C_4

Figure 8. FCMFC (5x1) Capacitor Charging States

1.2.2 Voltage Analysis and Gain Benefit

Plotted in Figure 9 is the ideal gain shown in (1.1) with a transformer turns ratio of $n = 5/3$ for all converters. It is apparent that FCMFC has higher gain for any given duty cycle. Mathematically, each flying capacitor has a multiplicative effect on the voltage conversion ratio, *"(N-1)"* term in (1.1). One flying capacitor doubles the gain of a flyback converter, two flying capacitors will triple the gain, and so on for higher level converters. This relationship is apparent in Figure 9, where voltage gain is shown for the flyback and two FCMFC converters. Hardware conditions are not ideal however, and thus this ideal gain curve gives insight on absolute capabilities.

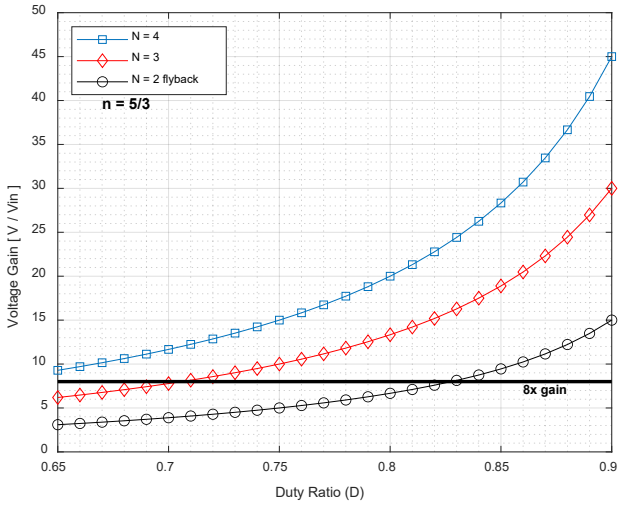


Figure 9. Ideal voltage gain vs duty cycle for flyback and FCMFC

Upon constructing a hardware version of the flyback and FCMFC, the losses reduce the achievable gain. A more accurate predictor of voltage gain is shown in Figure 10. These curves account for the major loss elements of a converter. The analysis for this is done in a later section of this work. The non-ideal gain curves shown are a much more accurate predictor of hardware implementation behavior. The flat line at eight times gain is included to show what duty is required for the application of this work. Notice that in Figure 9 the required duty cycles are much lower in the ideal case than in the loaded case shown in Figure 10. Near 90% duty notice, there is a crossover point where the N3 converter exhibits higher gain than the N4 converter due to conduction losses which illustrates the eventual tradeoff with a multilevel structure. Higher *N* level structures are not necessarily less efficient, but this comparison is based around proof of operation and not optimization. Higher order multilevel converters, ten levels or more, can be very efficient [23] for the same reasons explained in this work. The FCMFC secondary FETs have a reduced blocking voltage rating of: V/(N-1), which facilitates the use of lower rated FETs that have a lower on resistance, as seen in the previous reference. [23] In the case of this plot and prototype, all switches

were chosen at the same 100V rating to account for the significant gain increase that FCMFC experiences. Note that even under load, the FCMFCs both have significantly higher gain that the flyback converter.

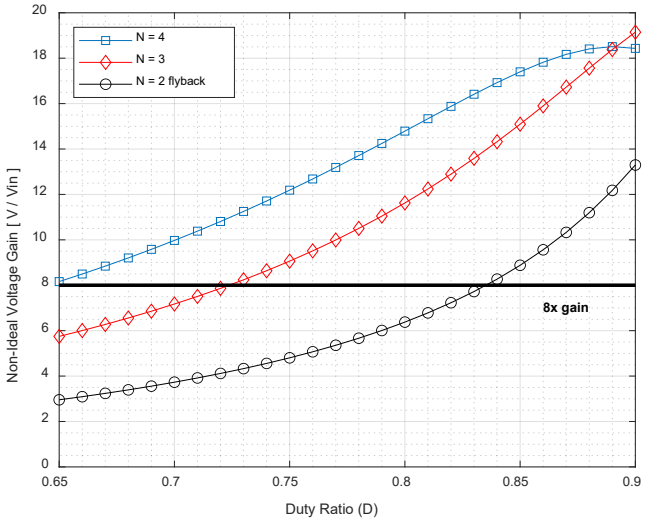


Figure 10. Non-Ideal voltage gain for flyback and FCMFC for 160Ω load

The flying capacitor voltage ripple, ΔV_C, and output capacitor voltage ripple, ΔV, which are derived as (1.2) and (1.3) respectively, were found using voltage ripple analysis as per [24]. Notice that they are dependent on the switching frequency, f_s and converter stages N. Because of the delay in charging multiple SDC stages, the output and flying capacitor voltage ripples increase for higher level converters. This is important to keep in mind for hardware design but the voltage ripple is also easily reduced by increasing the capacitance in question.

$$\Delta V_C = \frac{(N-1)^3 V_{in}\left(\frac{D}{1-D}\right)n}{2Rf_sC} \tag{1.2}$$

$$\Delta V = \frac{n(N-1)^2 D V_{in}\left(\frac{(N-1)}{1-D} - 1\right)}{2Rf_s C} \qquad (1.3)$$

1.2.3 Current Analysis

The average magnetizing inductor current is shown in (1.4) and was derived using capacitor-charge balance. The resultant equation is the same as a flyback converter with an added (*N*-1) term in the numerator to account for flying capacitors. Magnetizing current in the inductor does not directly double or triple because of a portion of the voltage boost is accomplished in the multi-level capacitor stage. In Figure 11 the average magnetizing current is calculated as expected for the three converters designed in this paper. The average magnetizing currents for N2,3,4 level devices are 2.42A, 2.83A, 3.25A respectively. The duty cycle of the input switch decreased from 82.76%, 70.59%, to 61.54% respectively due to the gain increase shown in (1.1). Because of this decrease in primary side conduction, the average input current of each converter is the same at 2A, shown in Figure 11.

$$\mathrm{I_L} = \frac{\mathrm{n(N\text{-}1)V}}{\mathrm{R(1\text{-}D)}} \qquad (1.4)$$

$$\mathrm{L_m} = \frac{\mathrm{V_{in}D}}{2\mathrm{f_s}\Delta\mathrm{i_{L_m}}} \qquad (1.5)$$

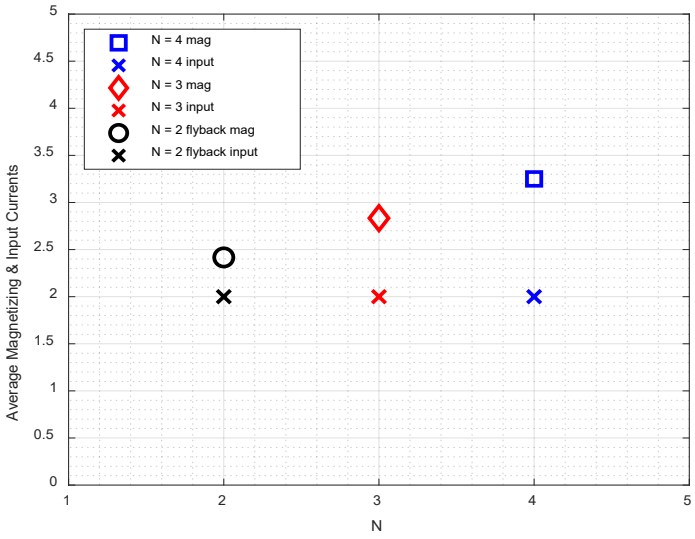


Figure 11. Magnetizing and Input Currents

Ripple current, (1.5), varies for magnetizing inductance L_m, input voltage V_{in}, duty cycle D, and switching frequency f_s. The only variance shown in this equation that would occur for multilevel structures is in the operating duty cycle for the desired conversion ratio. A higher-level converter requires a lower duty cycle and thus will result in a lower ripple current value on the primary inductor. The average magnetizing current is still higher for higher-level devices and shown in Figure 12 is the calculated peak current that would occur through the MOSFET before turn OFF.

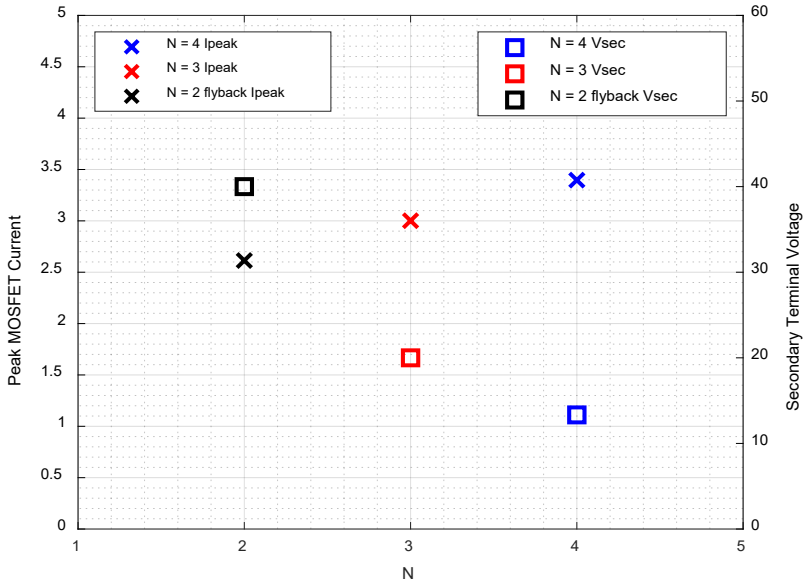


Figure 12. Peak MOSFET Currents and Secondary Terminal Voltage

1.2.4 Zener Snubber Power Consumption

Leakage inductance on the primary winding will cause large voltage spikes at turn OFF of the primary FET. This is one drawback of the flyback converter that is solved with various types of snubber circuits. The most robust of which is the Zener snubber which is suitable for this exercise and shown in Figure 1. A Schottky and Zener diode are placed in series from the switching node of the FET to the positive input voltage node. When the FET turns off the peak current flowing is now stored in the leakage inductance of the "transformer" and this results in a very large voltage spike across the FET. When this happens the Zener diode will conduct at its Zener voltage and regulate the voltage at the switching node, passing the leakage current back to the source. The derived power consumption for this snubber circuit is shown in (1.4), [25]. There is one modification made to account for the FCMFC, the *(N-1)* term. This represents the fact that only a fraction of the converter output voltage is reflected through the transformer during the OFF state

of the primary FET, due to the voltage distribution across the flying capacitors on the secondary of the circuit. This relationship is shown in Figure 12, where the secondary terminal voltage is shown, *V/(N-1)*, for N2,3,4. Although the peak FET current will be higher for higher-level converters, the reflected voltage will be significantly reduced, cut in half for a N3 converter and cut to one third for a N4. The predicted loss in the voltage clamp snubber for these converters is significantly reduced, calculated using (1.6), and shown in Figure 13. Going from the flyback (N2) converter to a N3 FCMFC, the reduction in power loss is significant, 67%, because of the reduced blocking voltage, 1.20W for the flyback down to 0.39W for the N3 FCMFC. However, notice that for a N4 device there is a slight increase in power loss, 0.39W (for N3) to 0.40W (N4), because of the output voltage fraction of one half compared to one third and also the peak current increase, shown in Figure 12. The 0.4W loss for the N4 device is still 66% less than the 1.2W loss of the flyback converter. There is a rise in power loss through the Zener clamp snubber circuit for higher-level devices, but it would take a 12-level device or higher to see the 1.2W snubber loss seen by the flyback.

$$P_{clamp} = \frac{1}{2} L_{lk} I_{max,S}^2 \frac{V_{clamp}}{V_{clamp} - \frac{V}{n(N-1)}} f_s \qquad (1.6)$$

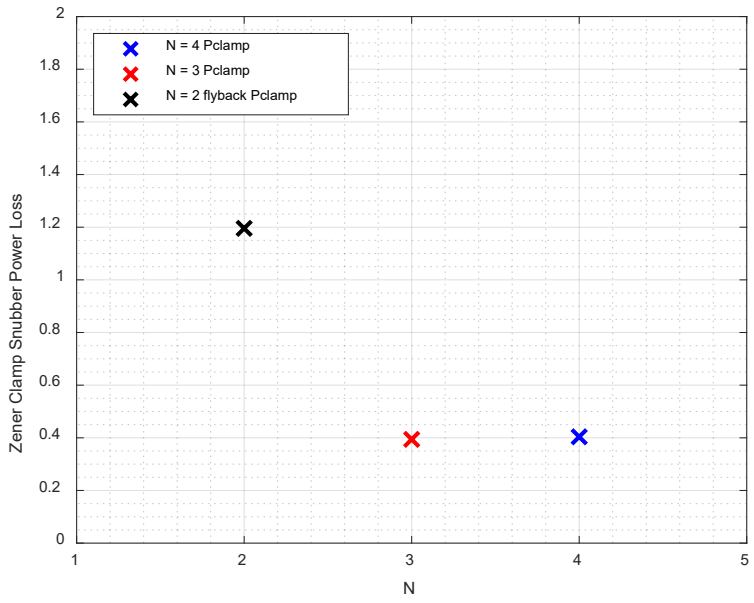


Figure 13. Zener Snubber Power Loss

1.3 Hardware Prototype Design

The goal of this design was a robust prototype testbed. Components were selected to account for a wide range of operation to ensure safe and reliable testing of this new multilevel converter topology. To validate theory of operation previously discussed, hardware prototypes of three converters were developed using the same components, listed in Table I. The flyback converter will serve as a control group or basis of comparison for the two multilevel FCMFC converters. The flyback design is considered a N2 FCMFC. N3 and N4 converters were also designed which have 2 and 3 capacitors on the secondary, respectively.

Table I.
Component List

Component	Brand	Part number
Planar Transformer	Coilcraft	NA5871-AL 42µH, 3:5
Flying Capacitors	TDK AVX	CGA6M2X7R2A105K200AA – 1uF 22201C106MAT2A – 10uF X7R, 100V
MOSFETs	Infineon	IPD30N10S3L-34 100V, 30A
Diodes	Diodes Inc.	PDS5100 100V, 5A
Bootstrap Diode	Nexperia	PMEG10010ELR 100V, 1A, 50Apk, 3.7ns
Gate Driver	Texas Instruments	UCC27512
Isolated Gate Driver	Texas Instruments	UCC21220A
Isolated Power	Analog Devices	LTM8067
Controller	Texas Instruments	C2000 F28335

1.3.1 Control Sensing

A Texas Instruments C2000 F28335 Delfino control development board was used to provide the PSPWM control signals for the primary FET and floating FETs for the flying capacitors on the converter secondary. PLECs coder was used to program the board. A rate of rise ramp was programmed for the primary FET to slowly energize the double wound inductor and avoid a high inrush current that results because of the uncharged output capacitance. This scheme prevents magnetic saturation and protects future iterations which will utilize FETs with lower voltage ratings. Open-loop control was used to run the FETs at a range of duty ratios for testing. A feedback circuit was designed using a voltage divider and op-amp buffer. This circuit allows for the output voltage signal to be safely fed into the F28335 ADC.

1.3.2 Isolated Auxiliary Power, Floating Gate Drive, Bootstraps

One challenge in multilevel structures is floating voltages at the source node of the transistors. In the case of FCMFC converter this challenge is met with the additional challenge of maintaining primary to secondary isolation.

An Analog Devices LTM8067 isolated power chip was chosen to provide auxiliary power. This chip was set to boost the input 5V supply up to 8V and drive the MOSFETs on the secondary side. This chip, being a flyback converter itself, retains primary to secondary isolation for the main converter with a 2kV rating. It provides a selectable voltage output, tuned with a resistor, to allow FETs to be driven at higher voltages if necessary. For this work 8V and 12V can be used on the Infineon FETs which are limited to 20V gate drive. Input and output capacitance are 2μF and 30μF respectively for adequate voltage regulation. A 20mΩ resistor was placed in series with the input of the auxiliary converter to dampen a potential resonant tank circuit that can arise between the inductance of the supply and the input capacitance.

Texas instruments UCC21220A isolated gate driver chips were chosen to reference the floating voltage nodes as a virtual ground. They also provide 4kV isolation from their logic level controller input side to the secondary high voltage side that drives the flying capacitor MOSFETs.

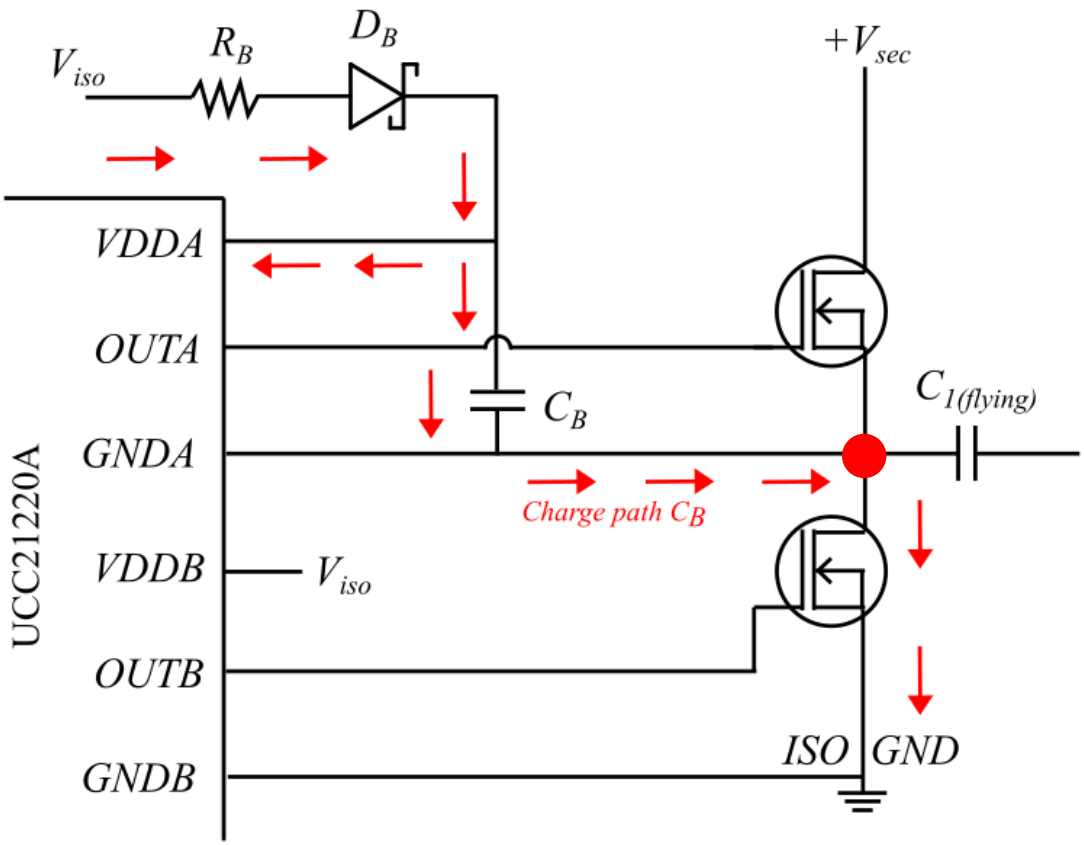


Figure 14. Bootstrap Circuit for N3

Bootstraps are required to drive each floating voltage node which corresponds to the flying capacitors. In the N3 FCMFC there is one bootstrap circuit and there are two in the N4 converter. Each bootstrap circuit consists of a resistor (R_B) diode (D_B) and capacitor (C_B). Isolated 8V DC supply feeds the resistor is in series with the diode and then the capacitor which finally connects to the floating source node of which, is the negative side of a flying capacitor, indicated in Figure 1 on C1, by a red dot and re-emphasized by the red dot in the bootstrap circuit diagram shown in

Figure 14. The positive polarity of CB is connected to the input voltage node of the isolated driver chip. In this configuration the bootstrap circuit charges to the secondary ground of the transformer using the isolated power supply with all latter switch(es) ON. When the latter

switch(es) turn OFF the voltage across CB is now Viso – VDB + VC1. This allows the effective floating FET gate-to-source voltage to be equal to the isolated power supply voltage minus the voltage drop that occurs across the bootstrap diode. The bootstrap capacitor is sized so that it can charge fast enough and have enough stored energy to bias the FET for its required ON-time per cycle. For higher level converters, like the N4 in this work, the first bootstrap capacitor (closest to coil) will have to charge through multiple FETs. The PSPWM must be set such that there is adequate charge time for the bootstrap capacitor. The balance between charging and discharging time must be met and considered for the bootstrap circuit when varying the switching frequency, as done in this work.

The chosen bootstrap diode has a reverse recovery time of 3.7ns which is less than the effective turn-on time of the FET. This is done to prevent excessive current from damaging the auxiliary power supply. The FETs effective turn on time includes the time it takes the drain-to-source voltage to drop once the gate has been charged plus the time it takes the drain-to-source voltage to start dropping when the gate voltage begins to rise. The bootstrap diode was chosen to handle maximum average current of charging the capacitor which occurs when the primary duty cycle is at its lowest point, 50%. The diode can handle peak current during startup conditions which is the supply voltage minus the diode voltage drop divided by the bootstrap resistance, approximately 2A.

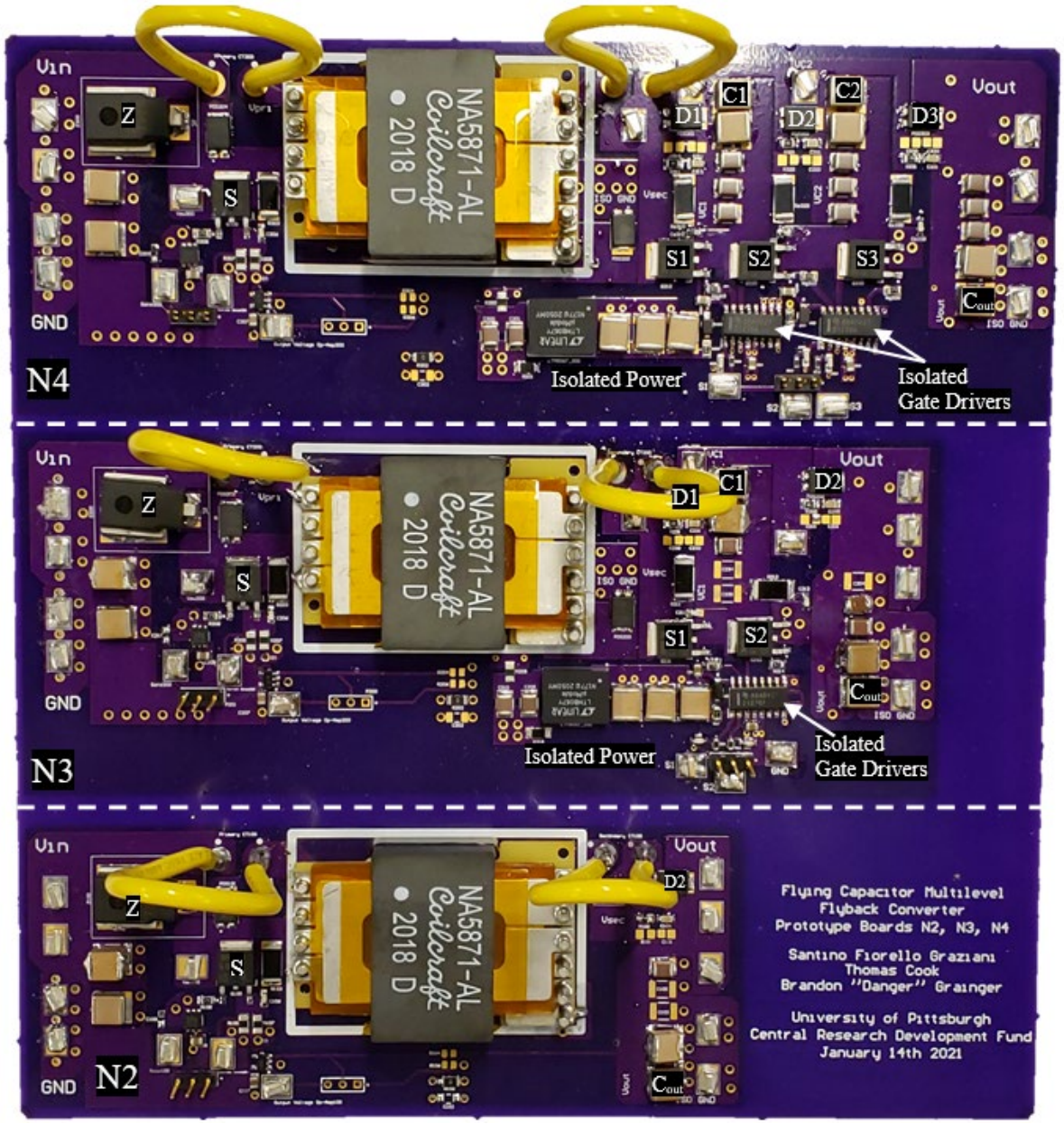


Figure 15. Printed Circuit Board N2 (bottom), N3 (middle), N4 (top)

1.3.3 Printed Circuit Board Layout

Figure 15 is a picture of the three converters with input on the left and output on the right. The three converters are included on one PCB. From top to bottom: N4, N3, and N2 (flyback) are provided. The yellow wires are 14AWG current jumpers for a current transformer testing point to measure primary and secondary current. There is no electrical connection between any of the three converters. Major components are labeled: diodes, switches, capacitors, isolated power and drivers and the Zener diode for the primary switch snubber. A 4-layer board was chosen to efficiently route this circuit topology. The layers include power and signal routing, primary side input ground, secondary side output ground, various power and signal routing. The bottom layer was used to get the primary +5V input to the isolated gate driver chips on the secondary side. This voltage is used on the logic side of the gate driver chips for the control signal inputs.

For the output and flying capacitors, multiple pads were added to easily scale their effective value. Two pads for 10μF and three pads for 1μF allow for finer tuning of the capacitance. The surface mount style capacitors are also stackable to further increase the capacitance for testing. In a similar way, multiple RC pads were added for snubber circuitry for each active semiconductor device.

1.3.4 Snubber Circuits

The primary FET has two snubber circuits. The Zener snubber circuit clamps the voltage overshoot at the switching node that rises because of the leakage inductance energy present at turn OFF. The Zener voltage is set to 27V to protect the FET. Figure 16 shows the Zener clamp snubbing the voltage to a maximum of 32.03V before leveling off to the regulated voltage, well

below the 100V FET rating. The voltage scale is 5V/div and time scale is 2µs/div. The primary FET and other active devices have series RC snubbers to reduce voltage ringing. These are designed to work for all cases in the wide frequency operating range. For example, Figure 16 at 500kHz has little visible ringing.

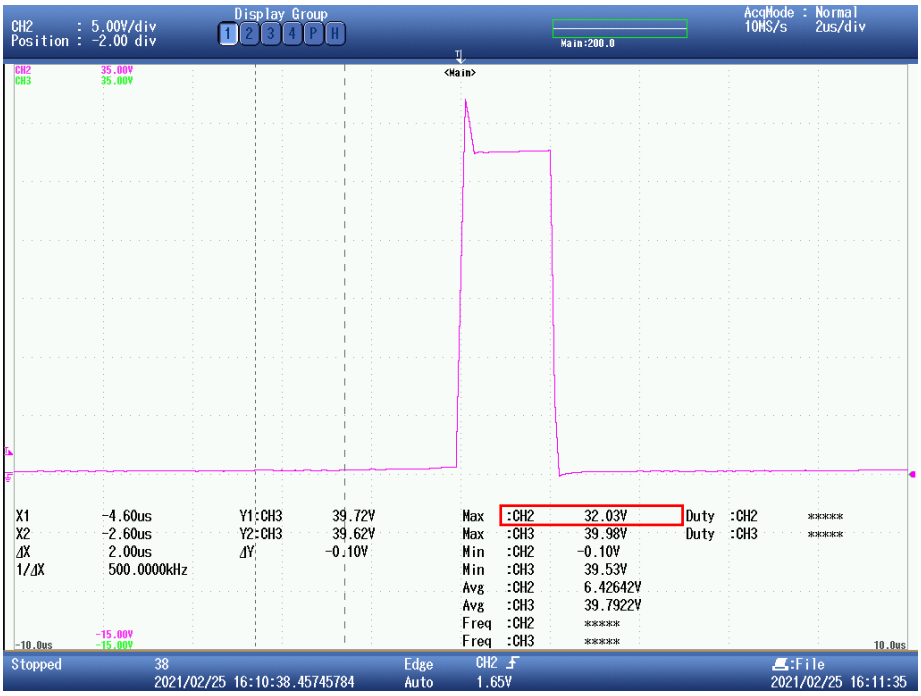


Figure 16. Primary FET switching Node Voltage with Zener Snubber Clamp

1.4 Prototype Testing and Results

Each converter was tested at 100kHz, 250kHz, 452kHz and 500kHz for an increasing constant current load with a 5V input fixed duty cycle and 1µs blanking time. Starting from a very small load (<10mA) and increasing in 50mA increments up to a maximum load of 15W. Input and output voltage and current were measured at each point along with the flying capacitor voltages.

1.4.1 Operation and Voltage Balance

One primary contribution of this work is to ensure operation of the FCMFC. The oscilloscope used was a 50Mhz Yokogawa DL850E with probes: Yokogawa 700929 and Rigol PVP2150. The 5V to 40V, 250kHz case was recorded for the N4 converter and shown in Figure 17. The primary FET gate drive signal is shown on top in blue with the two flying capacitor voltages shown in pink (C_1) and green (C_2) with the output voltage in red. Note that these are not differential measurements but are measured from flying capacitor positive node to the isolated secondary side ground. The time scale is 5µs/div and the voltage scale is 10V/div for the flying capacitors. When the blue gate signal drive goes low, the secondary side flying capacitor charging action will take place. The magnetizing inductor will first charge C_1 which is illustrated by a black arrow on the blue gate drive signal. Because the voltage ripple is ~1V the charging of C_1 is not visible but does take place as indicated. The next cycle is the inductor in series with C_1 to charge C_2. This is apparent on the C_1 (pink) voltage waveform because the measured voltage is pulled up to that of C_2. Next is the output stage where the inductor with C_2 charges the output capacitor. Now the green measurement matches the output voltage of 40V seen in red. Again, the actual ripple

voltage of each capacitor is about 1V and what is shown in the figure is measurements to ground so the changes shown are changes in switching states. There is a change in voltage when the secondary switches change state and then a change when the primary FET switches ON or OFF as indicated in Figure 17.

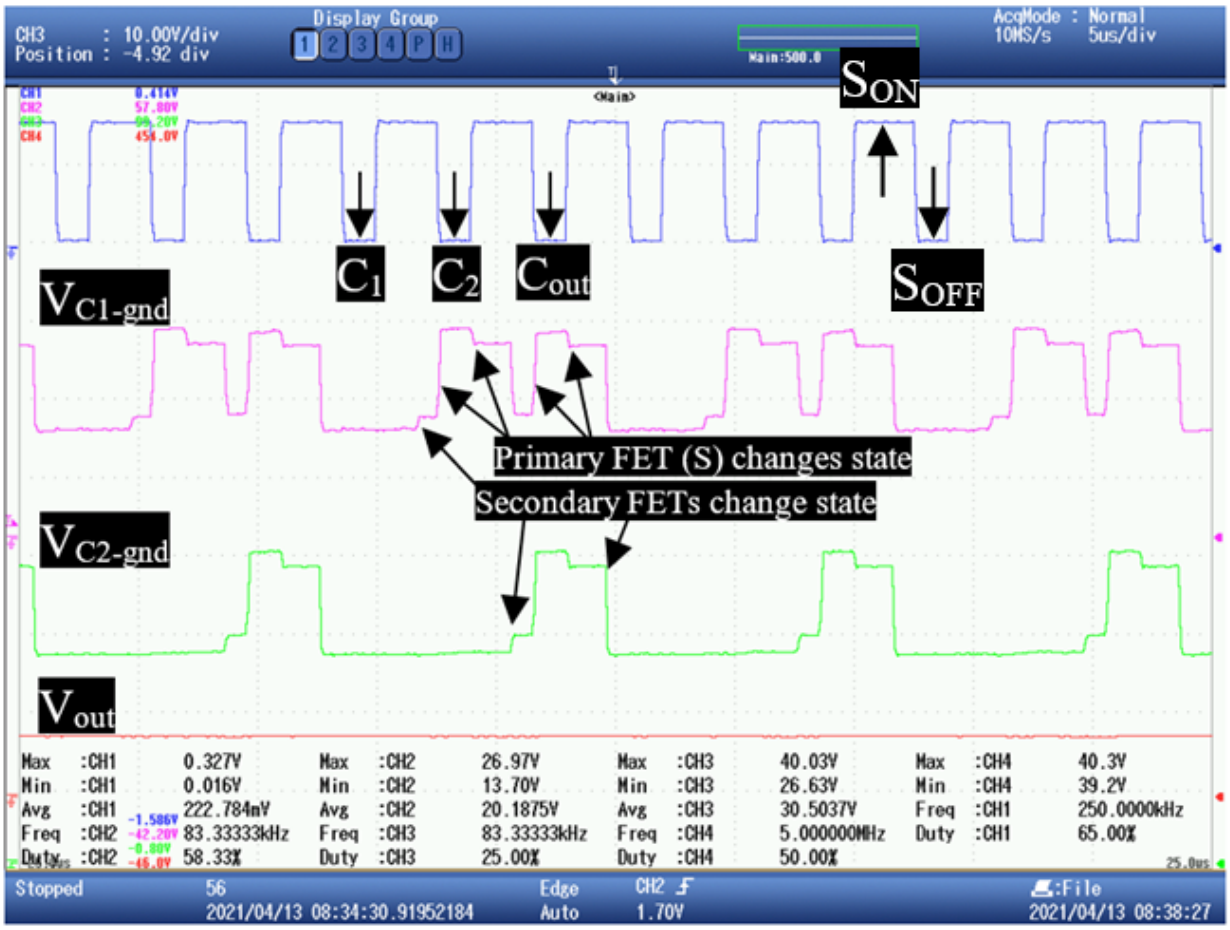


Figure 17. N4 Flying Capacitor Charging Action

The flying capacitor voltages were measured at each state to verify the charging action and voltage balance. Figure 18 is a voltage plot for the N4 converter which has two flying capacitors (C_1 & C_2) and the output capacitor (C_{out}). The voltages were measured at each 50mA increment

up to a 14W power output. At each point the voltage across the flying capacitors hold at one third and two thirds of the output voltage. For example, at the 9W point, the voltages for C_1, C_2, and C_{out} are 20V, 40V, and 60V, respectively. C_1 is closest to the secondary coil and in this case maintains the primary reflected voltage that is cut to one-third of the output voltage when compared to the flyback converter.

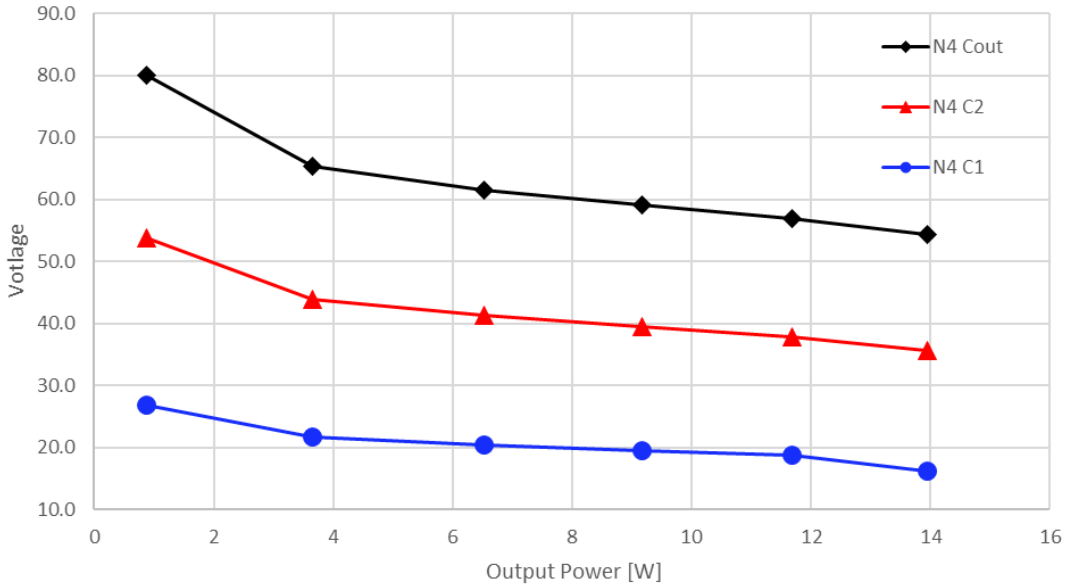


Figure 18. N4 Flying Capacitor Charging Action and Natural Voltage Balance

1.4.2 Voltage Gain

To check the gain potential of each converter, a duty cycle sweep was performed from 50% to 90% under no-load with 5V input, shown in Figure 19. The theoretical prediction of equation (1.1) and Figure 9 are correct. The N3 converter holds at about double the voltage gain of the flyback converter and the N4 is about triple. Take duty of 85% for example, the flyback has a gain of 10 and the N2 is 20 while the N4 is 32. Also of note here is that the typical switching limit of

the flyback converter is around 90%. The flyback voltage gain drops off after 85%, going from 10 down to 8 at 90%. Both FCMFC converters maintain a gain increase from 85% to 90% with the N4 device being more significant. The N2 increases from 20 to 21 while the N4 increases from 32 to 37. Note that even with a higher turns ratio the FCMFCs would still double and triple the voltage gain that a flyback can realize.

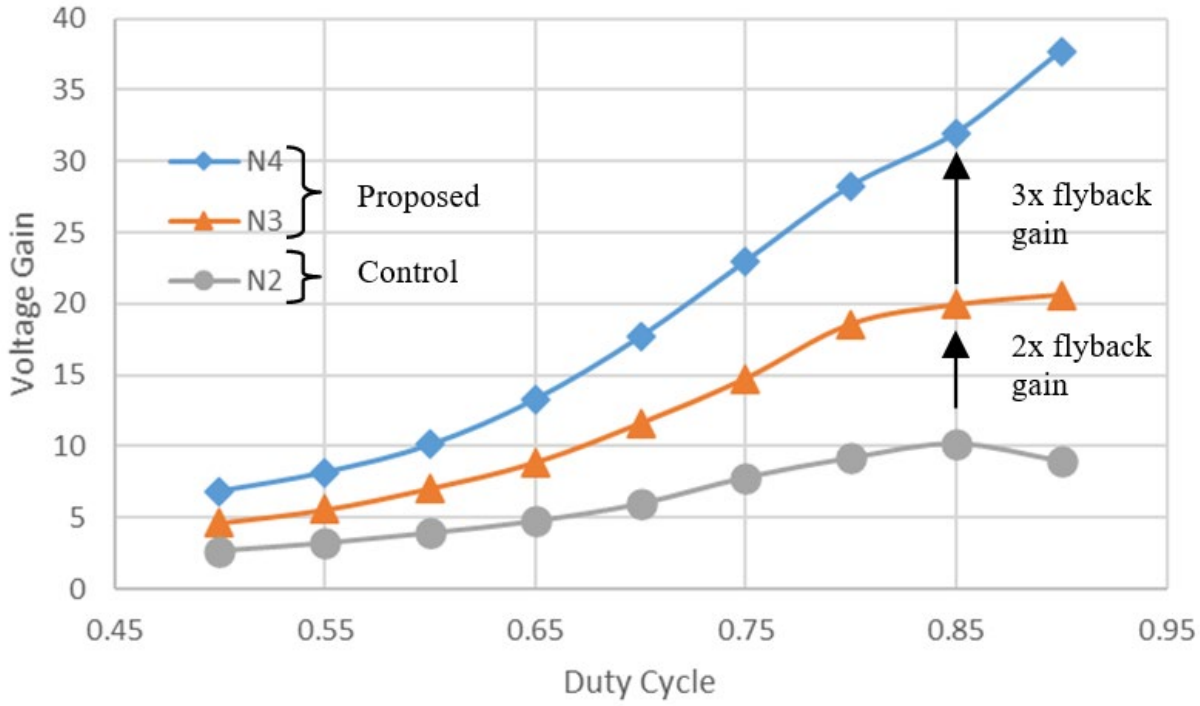


Figure 19. Un-loaded Voltage Gain

To show the effects of loading on voltage gain, Figure 20 shows a plot of output power verses voltage gain. The switching frequency is held fixed at 250kHz and the effective duty cycle is 72.5% for each converter with an input voltage of 5V. The flyback gain holds at 4 while the N3 is double at 8 and the N4 is tripled to 12, as expected. The FCMFC voltage gain is more sensitive upon loading but still holds significantly higher than the flyback converter.

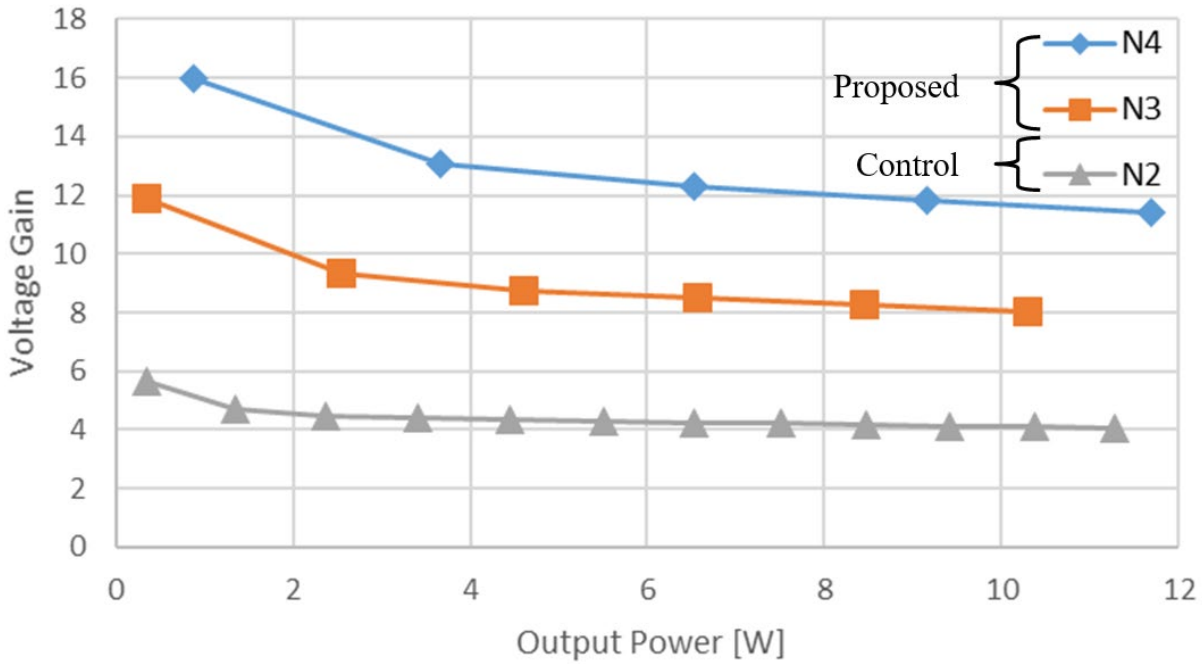


Figure 20. Loaded Voltage Gain

1.4.3 Zener Snubber Loss

As predicted in Section II C, the FCMFC converters will have about one-third the Zener snubber loss as the flyback converter. To illustrate this point, the N2 and N3 converters were run at an 8W load until a stable temperature was reached and thermal images are shown in Figure 21. In both images the Zener diode is the hottest (white) area. For the flyback converter, the temperature rises to 156F while the N3 only reaches 86F. This result is similar for the N4 converter. The flying capacitor connected directly to the secondary coil has a voltage that is half of the steady state voltage across the output capacitor on the flyback converter. This voltage is reflected to the primary during the OFF state of the FET and increases the loss of the Zener.

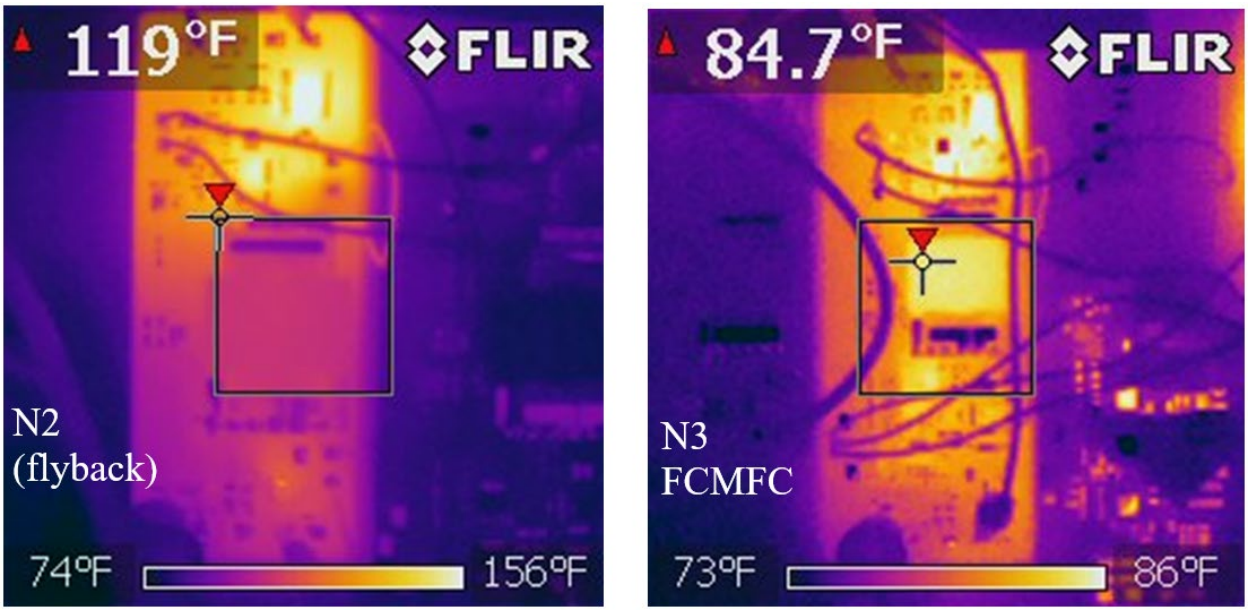


Figure 21. Thermal Images of N2 and N3 at 8W Load

1.4.4 Efficiency

Figure 22 shows the converter efficiencies when operating with 5V to 40V at 250kHz. The efficiency calculation includes all onboard circuitry: auxiliary power, primary gate driver, isolated gate drivers, etc.

The only power consumption unaccounted for is that of the microcontroller, which is similar for each of the three converters. Over the load range both FCFMC converters are more efficient than the flyback converter. The flyback efficiency peaks at 75.6% and the N3 peaks at 85.0% while the N4 peaks at 85.5%. The FCMFC converters are achieving higher efficiencies while having more switching devices and supporting circuitry. Overall, these efficiencies are not high compared to other works referenced herein. A robust approach was taken to prove circuit

functionality and directly compare a flyback converter to the proposed converters and prove the relative efficiency increase. Semiconductors were chosen with significant voltage and current rating margins and used across all converters. Careful consideration can now be taken to design an FCMFC around an existing flyback design and result in high efficiency by using semiconcutors with lower voltage ratings and conduction resistances. FCMFC converters (N3 and N4) can also maintain higher gain range with the lower duty cycle of operation. For the 100kHz, 452kHz, and 500kHz operation, similar efficiency behavior was observed. Higher frequency operation results in higher switching losses and thus a slight degradation in efficiency.

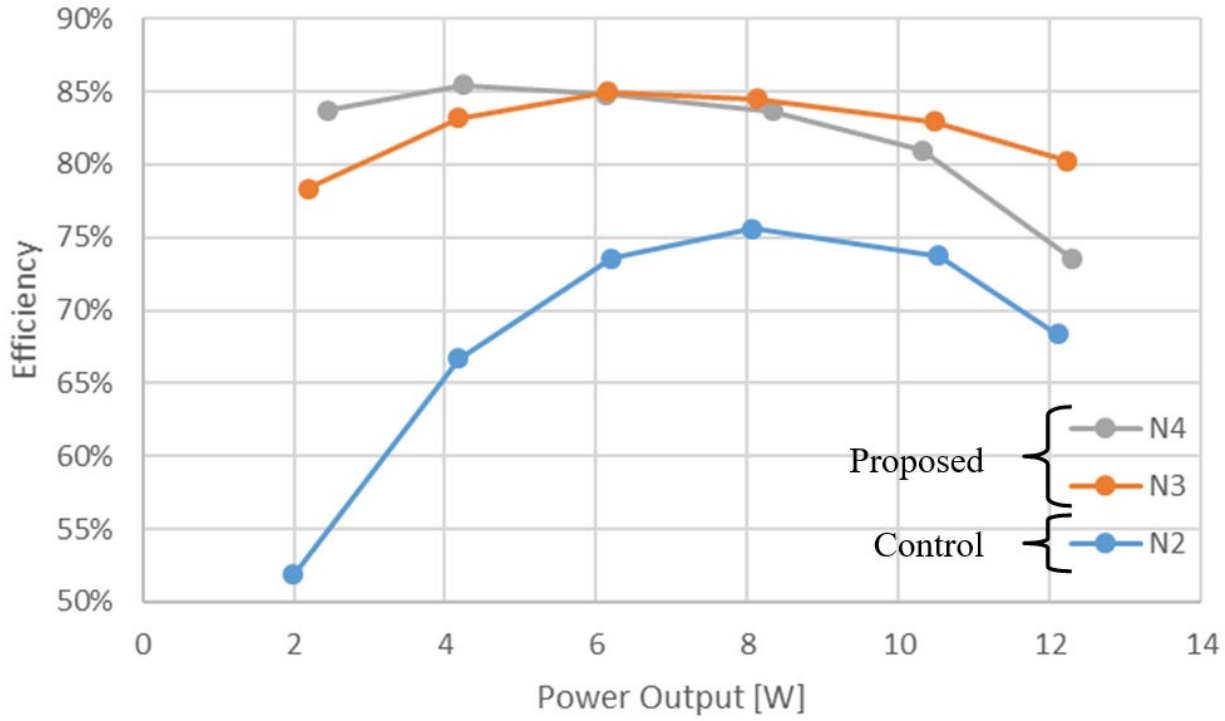


Figure 22. Efficiency vs Output Power N2, N3, N4

Table II.
Efficiency at 5V to 40V, 10W Load, 250kHz

N	Duty Cycle	Efficiency
2	82.5%	77.72%
3	72.5%	84.74%
4	66.0%	81.57%

To compare application capability, the duty cycles were tuned so that the converters achieve 40V, 10W output at 250kHz and results are shown in Table II. The flyback efficiency 77.72% and the N3 converter reaches 84.74%. The Zener snubber loss reduction predicted in Section II C and shown thermally in Figure 21 makes the FCMFC more efficient because of the reduction in the secondary coil voltage caused by the flying capacitor. The same benefit is found for the N4 converter, but the efficiency is lower at 81.57% because of the added conduction and switching losses associated with the extra flying capacitor stage. Further iterations of this converter can take advantage of lower rated FETs and further reduce conduction losses, which will significantly increase their efficiency.

1.5 Comparative Analysis

Given that the FCMFC hardware prototypes worked successfully, and the high voltage gain has been proven, it is worth comparing to other prototype converters in the IEEE literature. Each of the nine converters shown in Table III are compared for: voltage gain, MOSFET voltage stress, number of MOSFETs and number of diodes. The proposed has a low number of diodes compared to the others while having only one more MOSFET. Looking at both voltage gain and stress it is apparent that the proposed converter has the added benefit of the *N* variable, where (*N*-1) is the number of capacitors. Voltage gain will double, triple, etc. as flying capacitors are added. The voltage stress on the FETs is likewise reduced. Notice that the proposed converters have two variables to work with while FCMFC utilizes this N variable in the design process to tune the gain or voltage stress. This gain capability increase allows for lower duty cycle on the primary switch and thus greater efficiency of operation.

Table III. Comparative Analysis of the High Voltage Gain Converters

Converter	Voltage Gain	Voltage Stress on MOSFET(s)	# of MOSFETs	# of Diodes
Converter in [26]	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{V(1-D)}{3+2n-D(3+n-D)}$	2	5
Converter in [27]	$\frac{n(3D+2)-(2-D)}{2(1-D)^2}$	$\frac{V(2+D(n-1))}{n(3D+2)-(2-D)}$	1	6
Converter in [28]	$\frac{1+n}{(1-D)^2}$	$\frac{V}{1+n}$	1	5
Converter in [29]	$\frac{1+nD}{(1-D)^2}$	$\frac{V}{1+nD}$	1	5
Converter in [30]	$\frac{1+n-D}{(1-D)^2}$	$\frac{V(1+n)(1-D)}{1+n-D}$	1	5
Converter in [31]	$\frac{1+n}{(1-D)^2}$	$\frac{V}{1+n}$	1	5
Converter in [32]	$\frac{1+D+2n(1-D)}{(1-D)^2}$	$\frac{V(1\pm D)}{1+D+2n(1-D)}$	2	4
Converter in [33]	$\frac{2+(1+n)D}{(1-D)^2}$	$\frac{V(1-D)}{2+(1+n)D}; \frac{V}{2+(1+n)D}$	2	5
Converter in [34]	$\frac{2(1+n)}{1-D}$	$\frac{V}{2(1+n)}$	2	6
Proposed Converter	$\frac{n(N-1)D}{1-D}$	$(1-D)(V_{in}+\frac{V}{n(N-1)}); \frac{V}{N-2+D}$	3-4	3-4*

1.6 Conclusions and Implications

This directive has derived and demonstrated the operation of the FCMFC for two cases, N3 and N4, with a N2, or flyback, for comparison. All converters were designed using the same active and passive devices. FCMFC converters are more efficient using the same componentry as the flyback converter even with the added circuit due to their inherent stress distribution. The FCMFC converter can also exhibit significantly higher voltage gain while maintaining higher efficiencies. This work extends the benefits of FCML converters to an isolated topology while minimizing the impact losses from transformer leakage which have historically limited the power levels of flyback converters. Use of FCMFC has been proven and justified to be promising for DC power conversion for high gain and efficiency. The next step of this work is to delve into the detailed operation of this device and develop an operation and efficiency model.

2.0 Directive II. Efficiency Analysis and Model Characterization

The FCMFC topology has shown promise with its prototype design and an accurate model of loss components is needed to predict its capability for other applications. This directive establishes an efficiency model for the new flying capacitor multilevel flyback converter (FCMFC) topology. The FCMFC has shown that with multiple output flying capacitors (FC) it establishes high gain while maintaining high system efficiency. The converter is suitable for efficient DC-DC power conversion in continuous conduction mode. Herein, the converter is first explored in the *N*-FC generalized case to derive the CCM/DCM boundary with a static loss model. This is critical to ensure that a design will operate in CCM. It is shown that the FCs widen the available duty cycle range for boosting the input voltages, and how the FCs can achieve comparable efficiencies to a flyback design while exhibiting significantly lower switch stress and reduced inductor size. A theoretical 40V to 400V, 200W, conversion study is presented to show the significant decrease in stress experienced by transistor switches and efficiency effects of the FCs. The added N stages lower the required duty cycle for the same gain which opens the range of boosting capability, while also incurring lower losses in the Zener snubber circuit which is required to dissipate the leakage energy of the couple inductor. The added stages do not drastically affect overall device efficiency. Textbook and publication materials are used to further develop a wholesome theoretical model which is verified using LTSpice and multiple hardware prototypes. Accounting for all loss mechanisms, the model developed can predict hardware efficiency within 0.51% accuracy tolerance for FCMFCs. This advanced model does not exist yet in the literature and is a critical tool for predicting the viability of designing future FCMFC iterations.

2.1 Literature Review and Motivation

Increased photovoltaic (PV) penetration presents many design challenges. PV modules in the 100W to 300W power range pose a maximum power point (MPP) in the range of 15V to 40V [35]. This voltage range is low compared to the input voltage requirement of inverters and thus makes achieving high efficiency difficult. A solution to this problem was the development of microinverters that exist on each PV module [36]. Non-isolated converters, similar to [35,37,38, 39], are desired for this microinverter topology to reduce size and cost. A limitation of non-isolated topologies arises with voltage gain, particularly when a module is shaded [40], that does not allow the converters to operate in the universal grid range of 85-265Vac [36].

One converter that can be used for high DC conversion ratios is the basic flyback converter which boasts high gain and offers electrical isolation, a requirement for system protection. Because of stress limitations, much work has been done in recent years to extend the use of basic converters. Many of the basic power electronics topologies have been utilized in a multi-level fashion to bolster efficiencies, even the buck converter [41]. Multi-stage power conversion is attractive because the design distributes voltage gains across multiple device switching cells and, thus, lowers voltage stress. Flying capacitors are not new in the field of power electronics. They have been used to modify boost, buck and buck-boost converters to promote higher efficiency operation. [42, 43, 44] Their use in the flyback converter is new however and has shown useful for not only promoting higher efficiency, but also higher voltage gain; as seen with the first operating FCMFC herein.

Flyback topologies are widely utilized for their low cost and high versatility in power conversion; boasting a wide input and output voltage range of operation [36]. In continuous conduction mode (CCM), a larger inductance to support a steady-state current and thus energy

storage is necessary but results in smaller ripple values than seen in the discontinuous conduction mode (DCM). DCM will require a smaller inductor that may have less conduction loss but the RMS currents through the MOSFET will be much higher than CCM, hence, more efficient designs tend to operate in CCM [36, 45]. CCM will however result in higher voltage stress on the secondary diodes leading to higher reverse recovery losses. The FCMFC shown in Figure 1 aims to reduce this by spreading the gain across multiple switched-diode capacitor (SDC) stages (or FC) to achieve (*N*-1) voltage stages in its output [46]. A single SDC stage is outlined in red. This will reduce the stress on the main MOSFET, S, by reducing the blocking voltage it will see.

The FCMFC utilizes a varying number of these stages. The one shown has two stages and would be considered an *N=3*, or just *N3,* level device. This would make a flyback converter an *N2* level device, having only an input and output voltage stage.

The FCMFC utilizes a flyback transformer in conjunction with flying capacitors at the output stage to significantly increase available voltage gain which distributes voltage across the flying capacitor stages. Steady-state secondary winding voltage is now a fraction (½, ⅓, ¼, etc.) of what it is for a flyback converter. This means the primary reflected voltage is proportionally reduced. This effect is paired with a lower duty cycle of operation for the input switch because of the inherent gain benefit of the FCMFC as seen in Figure 19 This figure shows the un-loaded voltage gain potential of three hardware prototype converters: one flyback (*N2*) and two FCMFC converters (*N3* & *N4*). Notice that the voltage gains are double and triple that of the flyback converter with respect to the number of flying capacitors.

The FCMFC increases the gain potential of a flyback converter with no modification necessary to the flyback transformer turns ratio. The application range of flyback converters is expanded with the use of existing commercial flyback transformers in an FCMFC structure. This

work will expand upon the operation of a FCMFCs by proposing an efficiency model. The contribution of this directive is to first derive the CCM/DCM boundary of the FCMFC and then investigate the impacts of additional SDC stages on switch stress, efficiency, and available duty cycle range for CCM operation, where greater voltage conversion ratios can be achieved. This will serve as the basis for a holistic efficiency analysis that requires an accurate duty cycle prediction, derived from the former analysis.

Section 2.2 will analyze the general N-level case and discuss the preference of CCM for boosting voltage in PV applications. DCM is analyzed as well to fully characterize FCMFC operation range. Section 2.3 will derive the design constraints to ensure CCM operation of the FCMFC. Section 2.4 will derive the non-ideal voltage conversion ratio and efficiency function of FCMFC for static loss components to show the effects of adding multiple output stages. Section 2.5 derives the stress curves for the main MOSFET, S. Section 2.6 presents a simulation study to compare efficiency and stress of three multi-level structures using the flyback converter as a reference.

Now with a partial loss model the non-ideal gain and duty cycle can be predicted, and a holistic efficiency model can be derived as described in Section 2.7. Section 2.8 will briefly cover FCMFC operation and then give a detailed description of the various loss mechanisms from Sections 2.9 to 2.12. Section 2.13 will explain the prototype design and then compare the model predictions to experimental hardware results. Section 2.15 will use the theoretical model in conjunction with LTSpice to verify and present a loss breakdown. Section 2.16 will close this directive with a discussion on how this model will be utilized for optimization.

2.2 CCM / DCM Boundary of the FCMFC

The steady-state analysis for the FCMFC leads to a voltage conversion ratio, *M(D)*, that shows inherent benefits because of the additional FC. Equation (2.1) shows that the voltage gain for the FCMFC is the same as a flyback converter with the added multiplier of (*N*-1) SDC stages. Adding one FC will double the available gain of the FCMFC and increases for higher *N* values. Further analysis shows that despite the higher steady-state inductor current shown in (2.2), the inductor size required, (2.3), will be reduced as a result of the FC. This is in part a result of the innately higher gain but also the increased switching frequency used to operate multiple stages. The converter also benefits from lower secondary side switching stress shown by (2.4). Because of the higher gain, a larger *D'* will be incurred for a given application so increasing the stages serves to decrease the stress on the individual switches. This will be addressed more formally in the forthcoming sections.

$$M(D) = \frac{V}{V_{in}} = \frac{n(N-1)D}{1-D} \tag{2.1}$$

$$I_L = \frac{n(N-1)V}{R(1-D)} \tag{2.2}$$

$$L_m = \frac{V_{in}D}{(N-1)f_{\mathrm{FCMFC}}\Delta I_{L_m}} \tag{2.3}$$

$$S_{1,2,..(N-1)} = \frac{P_{LOAD}}{\sqrt{D'}} \tag{2.4}$$

Next, we derive the DCM condition for the FCMFC. This is the case when the inductor current, I_L, returns to exactly zero every switching cycle but for the FCMFC this will be every sub-cycle; where a sub-cycle refers to the primary side inductor charging and discharging once as

shown in Figure 23. In the ideal case, the input power equals the output power leading to (2.5). The output power is consumed by the load resistor while the input power is calculated using the energy stored in the inductor, $E_L = 0.5L_mI_{Lpk}^2$. The input voltage V_{in} is applied across L_m for the time of DT_s reaching a peak current, I_{Lpk}. This energy value, E_L, is then averaged over the secondary side switching period of the converter, T_{FCMFC}, which equals (N-1)T_s, with T_s being the input switch, S, switching period. This period distinction comes from the added charging states necessary for each SDC stage. Every additional stage requires one more inductor sub-cycle. There are (N-1) sub-cycles resulting in a device period of $T_{FCMFC} = (N\text{-}1)T_s$. This power cycle happens for (N-1) stages leading to this scaling factor found in (2.5). Equation (2.5) is rearranged algebraically to give the DCM conversion ratio shown as (2.6). Here, it is apparent that the root of the number of stages works to reduce the overall gain of the converter. K is explicitly showing that the voltage conversion ratio is now dependent on more than just the duty cycle but now the number of SDC stages added on the secondary side of the FCMFC. Also note that now the FCMFC does not depend on the turns ratio, n, of the transformer as was the case for CCM operation shown by (2.1).

$$P_{in} = \left[\frac{L_M}{2}\left(\frac{DT_SV_{in}}{L_m}\right)^2 \frac{1}{T_{FCMFC}}\right] \times (N-1) = \frac{V^2}{R} = P_{out} \qquad (2.5)$$

$$M(D) = \frac{V}{V_{in}} = \frac{D}{\sqrt{K(N-1)}}, \qquad where\ K = \frac{2L_m}{RT_s} \qquad (2.6)$$

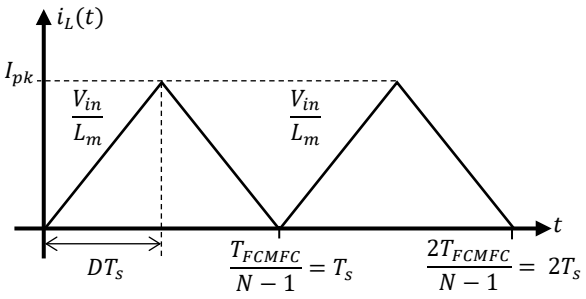


Figure 23. Boundary Conduction Mode of FCMFC

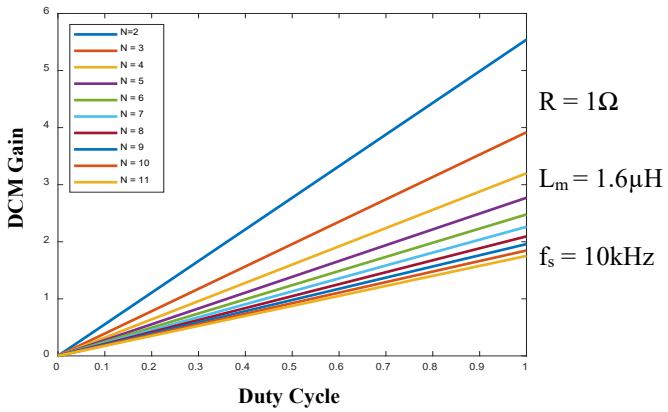


Figure 24. DCM Gain of Novel Converter

The DCM gain for higher *N* order cases is plotted in Figure 24. The case is taken for arbitrary component values shown to the right of the plot and is meant to show how the gain decreases for higher *N*. Note that the case for *N* = 2 is for a standard flyback converter design and is as expected when substituting *N*=2 in (2.5). To ensure operation in CCM for PV output voltage boosting applications, the boundary between CCM and DCM is defined next.

2.3 SDC Stage and Transformer Turns Ratio Impacts on the CCM/DCM Boundary

To take advantage of the high gain operation in CCM, the steady-state inductor current, I_L, must be greater than the ripple current, ΔI_L, (2.7). The steady-state current is shown in (2.2) and the ripple current is half of the peak current (I_{pk}) shown in Figure 23. Inserting the analytical expressions for the steady-state current and ripple current into (2.7) yields (2.8) which can then be rearranged to give (2.9). Taking (2.1) and inserting into (2.9) yields the final inequality to guarantee CCM operation, listed as (2.10).

$$I_L > \Delta I_L \tag{2.7}$$

$$\frac{n(N-1)V}{R(1-D)} > \frac{V_{in}DT_s}{2L_m} \tag{2.8}$$

$$\frac{2L_m}{RT_s} > \frac{V_{in}}{V}\frac{D(1-D)}{n(N-1)} \tag{2.9}$$

$$K > \left[\frac{(1-D)}{n(N-1)}\right]^2 = K_{crit}(D,n,N) \tag{2.10}$$

To illustrate the constraint between modes, Figure 25 shows the CCM/DCM boundaries, found with (2.10), for certain N given arbitrary parameters of R = 1Ω, L_m = 10μH, f_s = 10kHz, and n = 1. It is critical to understand how the addition of FC affects the boundary line for the proposed topology. If the K_{crit} curves are above the K value the converter is in DCM and when the curves are below the K value, at higher duty cycles, the converter will be in CCM. For example, the N = 2, standard flyback design, will crossover from DCM into CCM at a duty cycle of about 0.57. By adding one FC to the flyback design (N = 3), the converter only requires a duty cycle of 0.1 to operate in CCM. The addition of a FC will drive the converter into CCM operation quicker, which is a useful result due to the higher achievable gain in this mode. For all higher N cases, the

converters are in CCM for all D. The transformer turns ratio also affects the curves proportionally as can be seen in (2.10). Increasing the turns ratio from $n = 1$ in Figure 25, to $n = 2$ in Figure 26, has the effect of shifting the K_{crit} curves down and increasing the likelihood of CCM operation of the converter. The duty cycle required for CCM is reduced by an increase in turns ratio. The observations in this section are critical to ensure FCMFC designs operate within CCM to utilize the achievable higher gains, described by (2.1), inherent to the FCMFC topology.

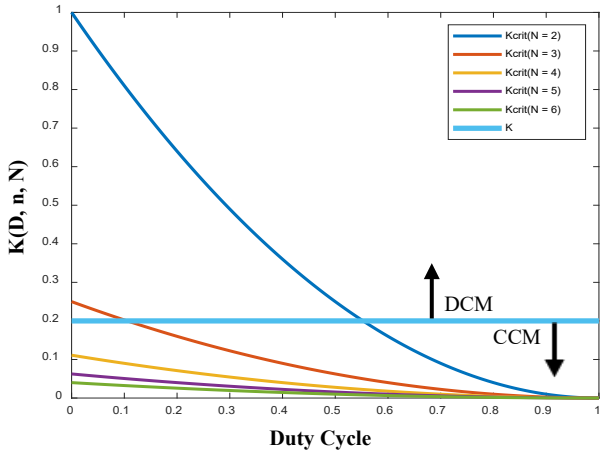


Figure 25. SDC Stage Effects on Boundary

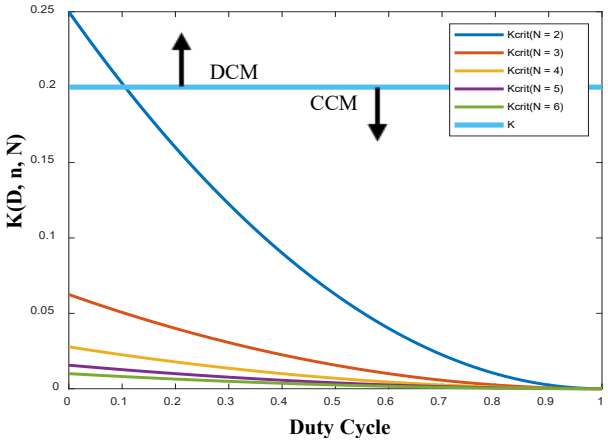


Figure 26. Effect of Turns Ratio on Boundary

2.4 Analytical Efficiency Expression for the FCMFC

This section will analyze the converter for static loss components stemming from the inductor copper windings (R_L), transistor ON resistances, diode ON resistances (R_D) and diode voltage drops (V_D), and capacitors ESR (R_C) to give the best-case efficiency (η) possible. The input transistor (S) will have ON resistance denoted as R_S and the output switch (S_1 through $S_{(N-1)}$) loss will be designated with R_{ON}, because input and output switches will require different ratings. Flyback transformers have more loss mechanisms that are not considered here, such as those associated with leakage inductance, which requires careful design [43]. The loss mechanisms would be similar for the N-level cases considered in this work and are thus simplified for explanation purposes, to a winding loss to account for changes in average inductor currents.

Performing an inductor volt-second balance on the magnetizing inductance for the general (N-1) level case and rearranging terms will result in the final, non-ideal gain (2.11). Note that if all loss terms are zero than (2.11) simply becomes the ideal gain listed as (2.1). Efficiency is calculated by dividing the output power by the input power. Cancelling like terms and substituting in the non-ideal gain results in an analytical expression for efficiency, (2.12). One simplification is made for the first FC charging cycle. Mathematically, capacitor C_1 will have a resistance that is $2R_C$. This will allow that term to simplify with all subsequent charging cycles where there are two capacitors in series.

$$\frac{V}{V_{in}} = \left[\frac{n(N-1)D}{(1-D)}\right]\left[1 - \frac{(1-D)V_D}{nDV_{in}}\right]b \qquad (2.11)$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{VI_L\left(\frac{(1-D)}{n(N-1)}\right)}{DV_{in}I_L} = \left[1 - \frac{(1-D)V_D}{nDV_{in}}\right]b \qquad (2.12)$$

where,

$$b = \left[1 + \frac{R_L + DR_S + \dfrac{(1-D)(R_D + 2R_C + (N-2)R_{ON})}{n^2}}{R\left(\dfrac{(1-D)}{n(N-1)}\right)^2}\right]^{-1}$$

Figure 27 and Figure 28 show the curves for (2.11) and (2.12) respectively for multiple *N*-level instances. The loss component and operational values used for the two figures are as per Table 1 in Section VI. In Figure 27, it is apparent that for higher *N* level converters, the duty required to achieve a gain of 10 is significantly lower.

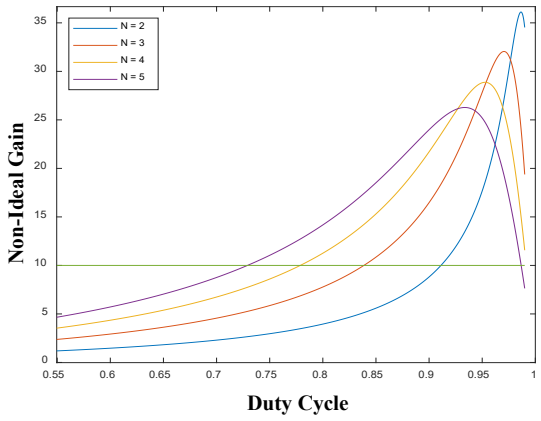


Figure 27. Non-Ideal Gain of FCMFCs

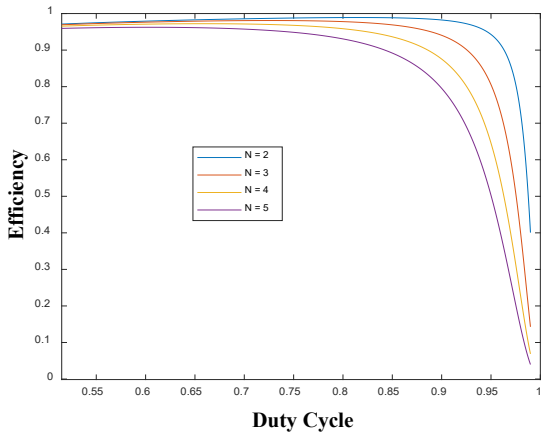


Figure 28. Efficiency of Flyback and FCMFCs

Figure 27 will be used to select the duty cycles required for each converter to achieve a 10x the input voltage at the output in a case study to be described. Figure 28 shows that the number of stages, N, decreases efficiency. This is expected because of an increased number of loss components (R_C, R_D, V_D, R_{ON}) that corresponds to an increase in N. For this paper, the loss component values were held equal to analyze only the effect of increased stages resulting in a worst-case efficiency. This means that the same semiconductors were assumed for each converter. In the final hardware design, the loss values for each N stage added will be less to account for lower stress levels that result from the inherent gain distribution amongst higher N designs. Figure 28 shows the worst-case effects of increasing N. Note that the peak gains are reduced for higher order devices, but this will change significantly with the variation in loss components. The takeaway here is the increased gain range that the flyback converter exhibits with FCs and can do so at significantly lower duty cycles. The hardware loss realized for FCMFC will be less than the flyback converter and will be further analyzed and shown in subsequent sections. This serves as a basis for efficiency analysis that is expanded.

2.5 Switching Stress

The active switching stress of the FCMFC is analyzed to provide insight on the switching loss as a result of higher order (N) devices. The switching stress is defined as the blocking voltage multiplied by the RMS current during the ON state. The output switching stress can be shown to be (2.13). Note that more stages will result in a lower stress on each switch due to the blocking voltage distribution between stages. For the same voltage requirements, a higher N device requires a smaller D, and results in a higher (1-D), reducing stress.

The input switching stress can be compared to the basic flyback converter. Equations (2.13) and (2.14) show the input switch stress for an FCMFC and a flyback design. For the same application, the duty cycle will be different between the two devices. Dividing (2.14) by (2.13) gives the relative input switching stress between the FCMFC and a flyback converter, (2.15). A plot of the ratio is shown in Figure 29. For the standard flyback (N=2), notice that the relative stress is a flat line at 1, which will serve as the reference for all comparisons. For all higher order N notice that the relative stress on the input switch is reduced as the gain increases. Each line approaches a horizontal asymptote at a value equal to 1/(N-1). For example, adding 1 FC, (N = 3), will result in an input switching stress that is half of the stress experienced by the input switch for a flyback converter. Switching stress values are reduced both on the input switch and secondary side switches as a result of adding stages to the FCMFC.

$$S_{1,2,..(N-1)} = \frac{V}{N-1}\frac{I_L\sqrt{(1-D)}}{n} = \frac{P_{LOAD}}{\sqrt{(1-D)}} \quad (2.13)$$

$$S_{FLYBACK} = (V_{in} + \frac{V}{n})I_L\sqrt{D_{fly}} \quad (2.14)$$

$$S_{FCMFC} = \left(V_{in} + \frac{V}{n(N-1)}\right) I_L\sqrt{D_{FCMFC}} \quad (2.15)$$

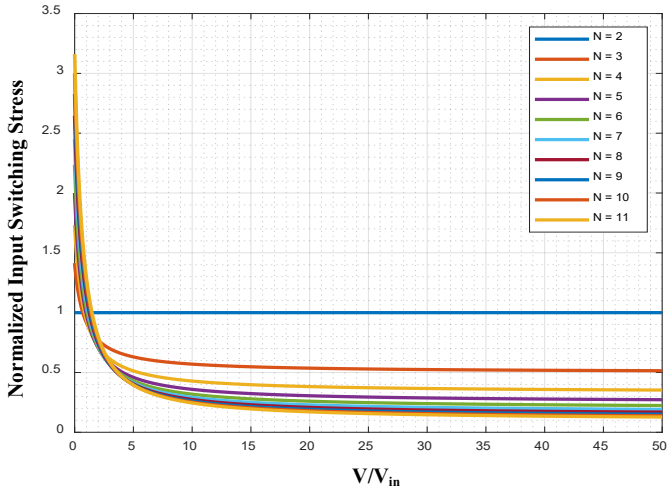


Figure 29. Input Switching Stress Relative to Flyback Converter

2.6 Results Comparison for 40V to 400V Voltage Boosting

Previous analysis has shown promising capabilities of FCMFC because of increasing the number of SDC stages. To show stage effects, four converters were simulated in PLECS to compare current (I_L), stress (S), and efficiency (η). Photovoltaic voltage boosting at 40V to 400V was chosen for light load (200W), and heavy load (1000W). Table IV contains all the converter design values and loss elements as defined in Section 2.4.

Table IV. Converter Component and Loss Element Values

V_{in}	n	L_m	C	f_s	R_S	V_D	R_D	R_{ON}	R_C	R_L
40V	1	1mH	10μF	10kHz	70mΩ	1.2V	10mΩ	35mΩ	10mΩ	50mΩ

Table V. Stage Comparison for 40V to 400V DC Boosting for 200W and 1000W

200W Case

N	D	I_L [A]	V_{block} [V]	S [W]	η [%]
2	0.910	5.5	437	2297	98.0
3	0.840	6.4	247	1437	97.0
4	0.780	6.8	173	1045	96.2
5	0.730	8.0	147	1001	95.6

1000W Case

N	D	I_L[A]	V_{block} [V]	S [W]	η [%]
2	0.918	30.8	445	13116	90.0
3	0.850	32.9	237	7189	87.3
4	0.800	37.5	192	6450	84.4
5	0.760	42.3	152	5587	80.2

Table V shows that for 200W power conversion the efficiency decreases by roughly 1% for each SDC stage added, as predicted in Figure 28. The average inductor current increases with added stages but the blocking voltage on the main switch is significantly decreased resulting in lower switching stress for the higher *N* cases. Also note that all converters were simulated using the same loss values, but for a final design, the converters with higher *N* would require semiconductors with lower ratings and thus lower ON resistances. The FCMFC is achieving the same 10 times gain for each case but duty cycles required are decreasing for higher order *N* cases, $D = 0.91$ for $N = 2$ and $D = 0.73$ for $N = 5$ for example. This result was predicted in Figure 27. Looking at Figure 27, it is apparent that the higher *N* cases have a larger duty cycle range that can be utilized to achieve 10x the output voltage compared to the flyback design, whose available duty cycle range is between 0.90 and 0.97. In the case of heavy cloud coverage for PV applications where the input voltage can drop drastically, the FCMFC can take advantage of this available duty cycle range for each added SDC stage to maintain high output voltage into the inverter system. The losses are more significant at heavy load, losing roughly 3% in η for each added SDC stage, but note the drastic decrease in switching stress.

For the $N = 3$, case the efficiencies are close to that of the flyback converter but still boast a significant stress decrease, so this converter was chosen to test the turns ratio effects on efficiency. Table VI shows that increasing the turns ratio from 1 to 2 to 4 reduced the efficiency by 0.3% and 1.1%, respectively while significantly reducing the switching stress by 41.9% and 55.5%, respectively.

Table VI. Transformer Effects on Efficiency for N = 3 Level FCMFC for 200W

Turns Ratio	D	I_L [A]	V_{block} [V]	S [W]	η [%]
n = 1	0.840	6.36	246.5	1436.9	97.0
n = 2	0.720	7.10	138.5	834.4	96.7
n = 4	0.568	9.31	91.15	639.6	95.6

The CCM/DCM boundary has been derived for the FCMFC, which is impacted by the number of SDC stages. The DCM gain was found and does not have a high voltage gain benefit. The inherent benefit of the FCMFC is that the available duty cycle range for boosting input voltages becomes wider for each SDC stage added to the output. Note that the loss components for semiconductors are kept constant across all iterations of *N*. Predicting the variations in resistances based on the variation in stress would prove too cumbersome for an insightful analysis. The FCMFC converters can achieve comparable efficiencies to a flyback converter while exhibiting significantly lower switch stress. This affect was seen in Directive I with the significantly more efficient Zener snubber circuit. FCMFC also lowers the required duty cycle for 10 times gain and does so with an increase in achievable gain of the device in the case of PV shading, for example. The non-ideal duty cycle can now be predicted for the FCMFC and CCM can be verified in the design process. The efficiency model developed will now be expanded upon to included active and other hardware related losses.

2.7 Complete Efficiency Modeling of the FCMFC

Now that a cohesive model with a single equation has been developed and tested, the efficiency model can progress to include each element in the hardware design. This approach will discretize the loss of each component of the FCMFC prototypes and present a holistic efficiency model of FCMFC. This directive will further establish an efficiency model for the new flying capacitor multilevel flyback converter (FCMFC) topology operating in continuous conduction mode. Textbook and publication materials are used to develop the theoretical model which is verified using LTSpice and multiple hardware prototypes. Accounting for all loss mechanisms, the model developed can predict hardware efficiency within 0.51% accuracy tolerance for FCMFCs.

The proposed converter has similar loss mechanisms to the flyback, such as: static losses from conduction through device resistances, active losses of the semiconductors, and transformer leakage inductance and core loss. In addition, this multilevel structure requires isolated power and gate drive to be on the secondary side of the transformer. This section will derive the general operating and loss mechanism equations for FCMFCs.

2.8 FCMFC Operation and Duty Cycle Estimation

Phase shifted pulse width modulation is used for the secondary side FETs (S_1-S_x) in conjunction with the primary PWM driven input FET (S). The magnetizing inductance charges the first flying capacitor stage (C_1) and then subsequent stages are charged with the inductance in addition with the previous flying capacitor. The ideal conversion ratio is as follows in (2.1), which is identical to a flyback ($N = 2$) converter with the additional (N-1) term, representing the number

of capacitor stages. The turns ratio is represented by n and duty cycle is D. Similarly, the average and ripple inductor currents are expressed in (2.2) and (2.3), respectively, where R is the effective load resistance, f_s is the switching frequency and L_m is the magnetizing inductance. To more accurately predict the duty cycle required by a converter for a certain voltage gain, the non-ideal gain equation is shown in (2.11) using similar methods from [38]. This equation accounts for the diode voltage drop loss (V_D) and static conduction loss in the diode (R_D), capacitors (R_C), inductor winding (R_L), and FETs (R_S, $R_{S1\text{-}Sx}$). With (2.11), an accurate duty cycle estimate can be found and then used in (2.2) and (2.3) to get average and ripple inductor currents.

2.9 Double-Wound Inductor

2.9.1 Conduction Loss

Using (2.2) and (2.5), the average primary inductor current can be found. The secondary current is found using the turns ratio. Using the winding resistance, R_L, and conduction time, the resistive winding loss can be calculated (2.16).

$$P_w = DR_L{I_L}^2 + (1-D)R_L\left(\frac{I_L}{n}\right)^2 \qquad (2.16)$$

2.9.2 Core Loss

The magnetic component, or double wound inductor, has conduction, core, and leakage losses. Tabulated experimental data for the core loss was provided by the manufacturer. Core loss polynomial equations were generated using the curve fit function in Excel for the provided

operating frequencies. The core loss is calculated for a given excitation with the peak flux density (2.17), where K is a series factor provided by the manufacturer and n_{pri} is the number of primary turns.

$$B_{pk} = \frac{K*V_{in}*D}{f_s*n_{pri}} \qquad (2.17)$$

2.9.3 Leakage Energy and Snubber Circuit

Next is the loss associated with the leakage inductance of the primary coil which is dissipated in a Zener snubber circuit shown in Fig. 1. This circuit regulates the primary FET drain to source voltage which will spike very high and destroy the FET in the absence of a snubber regulator. The power loss associated with this circuit is estimated using equation (2.18), where V_{clamp} is the Zener voltage plus the series diode forward voltage drop. L_{lk} is the leakage inductance and the max current prior to primary FET turn OFF is $I_{max,S}$. The total leakage energy is dissipated through the snubber circuit every switching cycle and at a ratio of the Zener voltage to the primary side reflected voltage.

$$P_{clamp} = \frac{1}{2} L_{lk} I_{max,S}^2 \frac{V_{clamp}}{V_{clamp} - \frac{V}{n(N-1)}} f_s \qquad (2.18)$$

2.10 Diodes

The Schottky diodes were chosen for their minimal reverse recovery loss, but they still have forward conduction and capacitive charge losses. The data sheet provides a forward conduction loss curve for a given average forward current. This curve was tabulated and then fit in Excel using

a polynomial. Now using the average current calculation, the diode power dissipation is estimated. In addition, there is a charge loss every switching cycle due to the inherent junction capacitance (2.19). The number of diodes does increase for higher *N* order FCMFC converters where the flyback only has a single output diode. However, because the output side switching is at a pace of $\frac{f_s}{N-1}$ the resulting loss does not increase. For the functionality of the current prototypes however there is an extra diode in series with the secondary coil to prevent secondary FET body diode conduction during primary coil charging. This extra diode loss is included for this work but could later be removed using GaN FETs that can be forced to prevent body diode conduction. Also note that the diode blocking voltage is a function of flying capacitor stages. A flyback converter output diode has to block the full output voltage rating *V* while FCMFC converter output diodes only block a fraction (*N*-1) of that rating.

$$P_{Dq} = f_s C_j \frac{V}{(N-1)} \qquad (2.19)$$

2.11 MOSFETs

A flyback converter has one distinct FET, the primary input FET. [47] This device also exists and functions in the same way for FCMFC, however, there are also output or secondary FETs to cycle the flying capacitors stages of FCMFC. All FETs suffer from conduction, switching and gate charge losses. The primary input FET is driven with the input 5V and will thus have a corresponding ON resistance that results in a power loss for the calculated average current. This calculation can also be done for the output FETs that are driven by the 8V isolated power supply. This power supply was used to maintain overall primary to secondary isolation of the converter. Switching losses for the FETs occur during an ON or OFF transition period when the drain voltage

and current overlap. This loss happens once for each transition per switching cycle for the primary FET and is estimated as per the generalized integral in (2.20) which is simplified to a piecewise linear function in (2.21) and (2.21) for the input FET. The peak drain current before turn ON/OFF can be calculated using (1.2) and (1.3). The output FETs experience the same loss but have a drain to source voltage of $\frac{V}{N-1}$ for turn ON and turn OFF and the peak drain current is calculated in a similar way.

$$P_{sw} = f_s \int_0^t i_d(t) v_{ds}(t)\, dt \mathrm{M(D)} = \frac{\mathrm{V}}{\mathrm{V_{in}}} = \frac{\mathrm{n(N\text{-}1)D}}{\mathrm{1\text{-}D}} \qquad (2.20)$$

$$P_{sw,\,ON} = \frac{1}{2} f_s t_r \left(V_{in} + \frac{V}{n(N-1)}\right)(I_L - \Delta i_{Lm}) \qquad (2.21)$$

$$P_{sw,\,OFF} = \frac{1}{2} f_s t_f (V_Z + V_S)(I_L + \Delta i_{Lm}) \qquad (2.22)$$

2.11.1 Gate Drivers

The primary FET gate driver chip has negligible internal power loss. The isolated gate driver chip(s) on the FCMFC secondary side can run two FETs each and have a quiescent power loss (2.23) associated with internal function for both logic primary and driving secondary sides of the chip. Supply voltage for the logic primary side of the chip is 5V and the quiescent current is 2.5mA. Supply voltage for the driving secondary side of the chip is 8V and the quiescent current is 1.5mA. This loss varies depending on how many flying capacitors and thus SDC stages in operation. The N3 prototype has one isolated gate driver running both secondary FETs while the N4 has two isolate gate drivers to run the three secondary FETs.

$$P_{iso,gd} = V_{supply} I_{quiescent} \qquad (2.23)$$

2.11.2 Charge Loss

Driving the FET gates results in a loss that is a function of the required gate charge Q_G multiplied by the driving voltage and switching frequency (2.24). This equation is the same for all the FETs but the frequency and driving voltage vary as discussed.

$$P_Q = Q_G V_{GS} f_s \qquad (2.24)$$

2.11.3 Isolated Power

The isolated auxiliary power supply has a quiescent loss estimate provided in the date sheet for a given loading that is approximately 200mW.

2.12 Capacitor ESR

In addition, the flying capacitors have an equivalent series resistance that results in another conduction loss for a calculated average current (2.25). The output capacitor is always conducting and then two capacitors conduct for (*1-D*) except for the first flying capacitor which conducts on its own. The full capacitor ESR loss can be shown in (2.26). This equation works for any FCMFC.

$$P_{Cx,ESR} = R_{ESR} I_{c,avg}^2 \qquad (2.25)$$

$$P_{T,ESR} = 2(1-D) R_{ESR} \left(\frac{I_L}{n}\right)^2 - \frac{1-D}{N-1} R_{ESR} \left(\frac{I_L}{n}\right)^2 + \left(1 - \frac{1-D}{N-1}\right) \left(\frac{V}{R}\right)^2 R_{ESR} \qquad (2.26)$$

2.13 Loss Model Equation Summary

This section outlines all portions of the FCMFC loss model with equations shown in Table VII. The MOSFET equations are used for primary and secondary FETs with respective blocking voltages.

Table VII. Summary Table of FCMFC Loss Mechanisms

transformer winding	$P_w = DR_L{I_L}^2 + (1-D)R_L\left(\frac{I_L}{n}\right)^2$	(2.16)
core loss using peak flux density for use with manufacturer measured data	$B_{pk} = \frac{K * V_{in} * D}{f_s * n_{pri}}$	(2.17)
Zener snubber clamp for primary FET	$P_{clamp} = \frac{1}{2}L_{lk}I_{max,S}^2 \frac{V_{clamp}}{V_{clamp} - \frac{V}{n(N-1)}} f_s$	(2.18)
diode capacitive	$P_{Dq} = f_s C_j \frac{V}{(N-1)}$	(2.19)
MOSFET switch-ON	$P_{sw,ON} = \frac{1}{2}f_s t_r (V_{in} + \frac{V}{n(N-1)})(I_L - \Delta i_{Lm})$	(2.21)
MOSFET switch-off	$P_{sw,OFF} = \frac{1}{2}f_s t_f (V_Z + V_S)(I_L + \Delta i_{Lm})$	(2.22)
isolated gate driver chip operating	$P_{iso,gd} = V_{supply} I_{quiescent}$	(2.23)
isolated power	200W	-
MOSFET gate charge	$P_Q = Q_G V_{GS} f_s$	(2.24)
capacitor ESR conduction for all stages	$P_{T,ESR} = 2(1-D)R_{ESR}\left(\frac{I_L}{n}\right)^2 - \frac{1-D}{N-1}R_{ESR}\left(\frac{I_L}{n}\right)^2 + \left(1 - \frac{1-D}{N-1}\right)\left(\frac{V}{R}\right)^2 R_{ESR}$	(2.26)

2.14 Model Verification with Hardware Results

The prototype converters shown in Figure 15 from Directive I were designed and built to verify the accuracy of the proposed efficiency model. The loss mechanism equations were programmed into Matlab in order to get quick iterations of test cases. Shown here are the results for the rated 5V input at 250kHz.

Table VIII. Efficiency at 5V to 40V, 10W Load, 250kHz

N	Predicted Efficiency	Hardware Efficiency	% Tolerance
2	79.58%	77.72%	↑2.34%
3	84.9%	84.74%	↓0.20%
4	81.99%	81.57%	↑0.51%

Table I shows the predicted efficiency values compared to the experimentally measured hardware values at the rated output. The hardware prototypes from Directive I. and shown in Figure 15 were used for this comparison. The flyback converter efficiency is 2.34% higher than experienced in hardware. The *N3* and *N4* converter predicted efficiencies are respectively 0.20% lower and 0.51% higher than predicted.

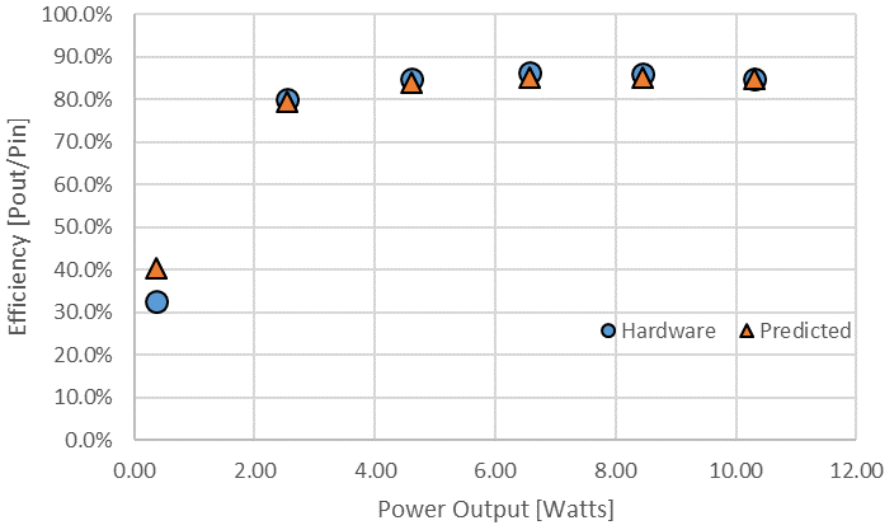


Figure 30 and Figure 31 show the predicted efficiencies for the *N3* and *N4* converters over the rated load range up to 10W, with fixed duty cycle. In this scenario the rated duty cycle for 40V at 10W was used to sweep over the load range. For lower power outputs the converters are at higher voltages and the voltage drops upon loading. It is apparent that the model and measurements are in agreement. Figure 31 shows that predictions start to stray from hardware results beyond the rated load of 10W of the N4 converter. The converter was tested at 17.5W peak where the predicted efficiency is 80% but the hardware yields 66.5%. This is to be expected as the semiconductor devices are being overloaded and heating up causes increased losses. As the rated load is exceeded the accuracy of the model degrades.

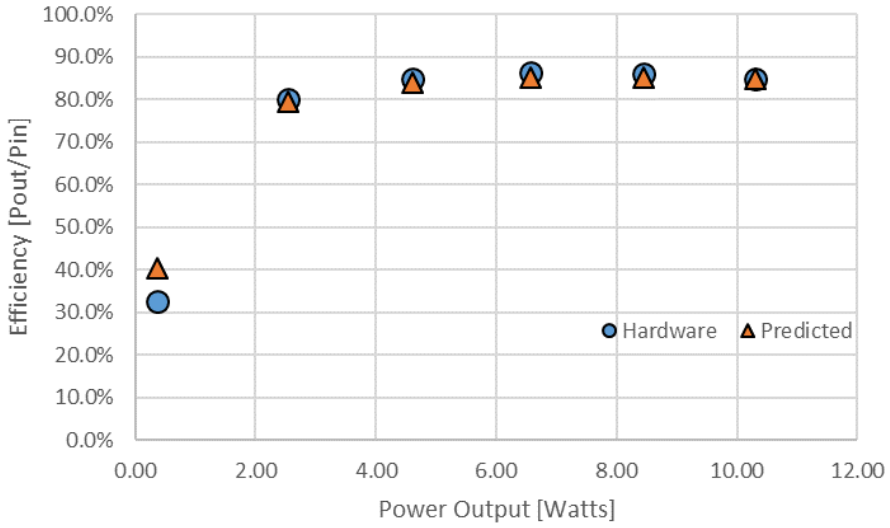


Figure 30. Model vs Hardware Efficiency Comparison for N3

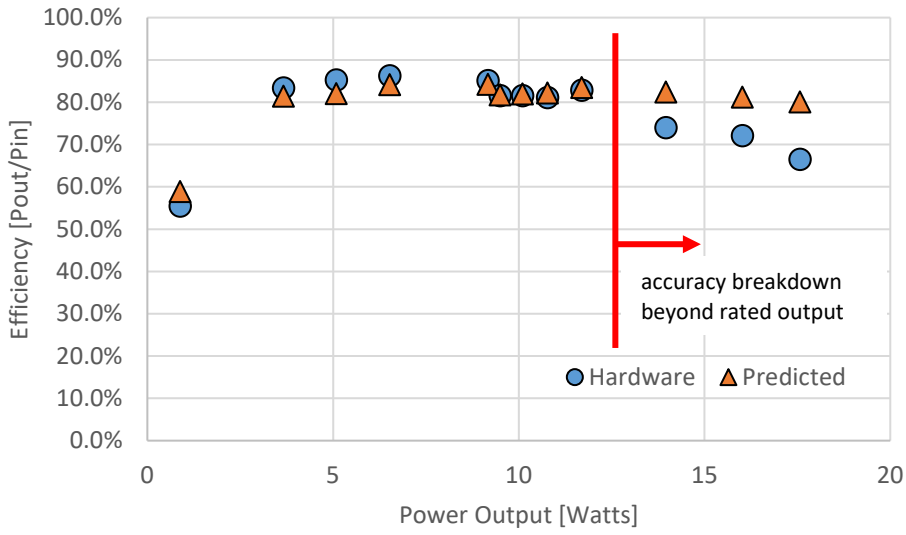


Figure 31. Model vs Hardware Efficiency Comparison for N4

2.15 Loss Breakdown

The new topology can now be characterized by its loss components. This section shows loss breakdowns for the FCMFCs to illustrate how each component affects the converter efficiency. The transformer loss is broken up into its core, leakage, and winding loss contributions. The primary (input) and secondary (output) FETs are separated as well because they experience different voltages and currents. These include the conduction and switching losses. The gate charge loss is included in the gate drive loss portions.

Figure 32 shows the loss breakdown for the N3 converter for the rated case illustrated in Table VIII. At a predicted efficiency 84.90% for 10W load the total loss is 1.8325W and is broken down by percentage in the pie chart. The diodes and the Zener snubber (leakage) loss are the largest loss mechanisms for this converter both at 28%.

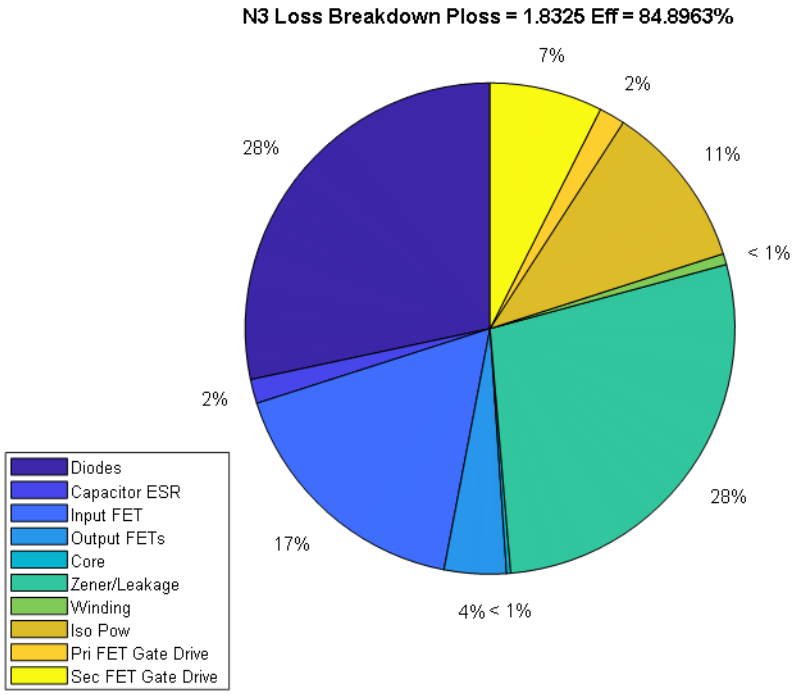


Figure 32. N3 Loss Breakdown (5V to 40V, 10W output, 250kHz)

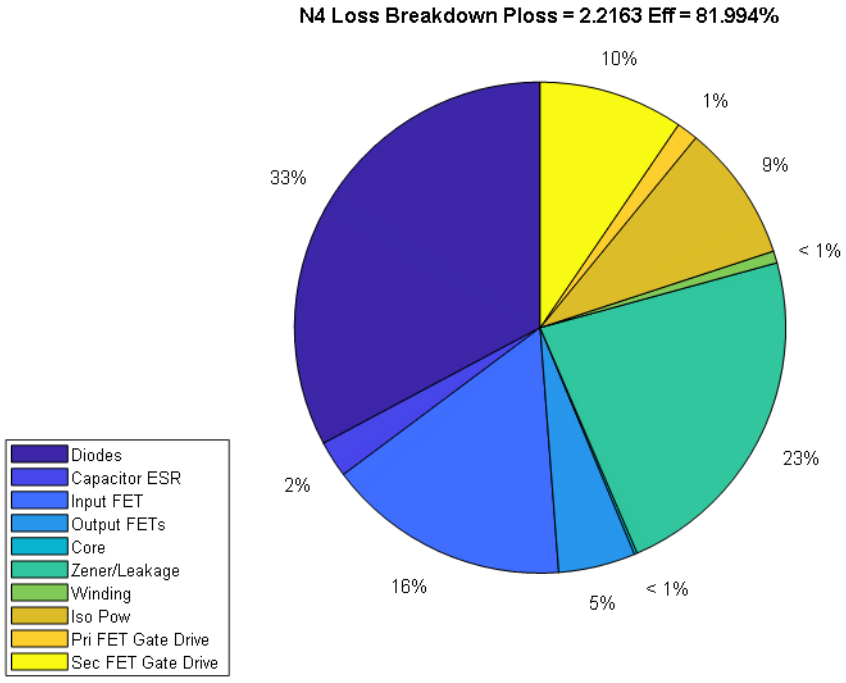


Figure 33. N4 Loss Breakdown (5V to 40V, 10W output, 250kHz)

Figure 33 is the loss breakdown for the N4 FCMFC. At an estimated efficiency 81.99% for 10W the total loss is 2.2163W and is broken down by percentage in the pie chart. The diode and secondary FET and driver losses are increased as a portion of the loss. This is sensible because of the additional SDC stage for the N4 converter.

2.16 Conclusions and Implications

This dissertation analyzed the FCMFC structure for discontinuous conduction mode and found that the gain is decreases with increased number of flying capacitors. Moreover, the DCM to CCM boundary equations were found so that CCM can be verified for future designs. This is critical to ensure that the significant gain improvements are realized. This directive also presents an accurate efficiency model for the novel FCMFC that can be used to predict power loss. The effort was a deep analytical dive into textbook and publication literature. Each loss component of proposed topology has been analyzed and verified individually using LTSpice. The totality of the model was verified using hardware prototypes. The accuracy of the model has been verified using hardware prototypes and is withing a 0.51% accuracy tolerance which is excellent for such a low power prototype where small losses are hard to predict. Currently the model exists in Matlab code and can be used to iterate any potential design given the electrical and component specifications. This model can now be used to design and optimize future FCMFCs, improving on flyback and multilevel performance. This model is key to the third and final research directive of this dissertation: optimization of converter levels.

3.0 Directive III. Optimizing Capacitor Stages

Directive I analyzed and proved the capability of the FCMFC structure. Directive II expanded on these findings with a holistic and accurate efficiency model of the converter. The models can now be used to optimize FCMFC designs for the number of flying capacitors. As was seen in the previous work, there are significant improvements that are seen using this multilevel topology. However, there is a diminishing return where the added conduction losses of higher-level converters (more flying capacitors) start to degrade the overall efficiency. This directive proposes an efficiency optimization process in which the FCMFC will be designed for the highest efficiency based on component selection and number of flying capacitors.

The application of interest is a front-end voltage boosting converter that is part of a solar microinverter. The converter will need high gain and high but also high efficiency over a large gain range due to the variable input voltage supplied by the output of the solar panel. The electrical specifications are 40V to 400V conversion for 200W load, however the input voltage and load power are subject to variability.

3.1 Introduction and Motivation

Photovoltaic (PV) solar power as a resource is discussed and presented as it relates to necessary efficiency improvements. Microinverter resilience improvements are then discussed to justify why central and string inverters are not optimal. Next the FCMFC will be compared to other converters for high voltage boosting and then more specifically to front end boost converters that

exist on microinverters. Optimization as a science in the field of power electronic design is presented and analyzed for this directive. Finally, an explanation of the conduction resistance of semiconductors is presented as it relates to the voltage rating.

3.1.1 Solar Grid Parity

About 36% of all new electricity generating capacity additions in 2019 were from solar power. Solar power has been holding quite steady since 2013 by being about 30% of all added electric power capacity in the United States year over year. The typical installation operates at a capacity factor of 18%, meaning that only about one fifth of maximum solar output is utilized, due to cloud cover and nighttime. Grid parity is the point at which solar power will become economically feasible compared to the other forms of generation like nuclear, coal, and natural gas. The comparison however is not direct because of the distributed nature of solar generation due to the capacity factor and other issues. Microinverters provide panel-by-panel control which can increase total energy production by 25% in a smaller installation, like residential for example. [48] Some installations have limited area, such as rooftop commercial solar. In this case they cannot spread the panels out enough to reduce the effects of shading. With microinverters the panels can be close together and achieve ~33% more energy production because of the individual power control on each panel. ACPV panels have been the most disruptive as they include the microinverter integrated into the solar panel. This cuts down on installations costs significantly. High reliability power electronics have been allowing for this technology to become feasible. Grid interaction requirements are a key challenge, of which isolation is not always required but can be very beneficial. Switch count can increase reliability of the converter but with increased cost. Single phase inversion that can manage the double-frequency ripple of the power output is a

challenge. The converters also need robust power up/down sequences that have local shutdown. Lightning and grounding issues also must be taken into account. Two relevant regulations for inverters and distributed energy resources (DERs) are IEEE 1547 and UL 1741. The power electronics need to meet certain expectations like: match panel life, facilitate installation, improver energy delivery, plug and play design, maximize panel energy, minimal maintenance, support utility operations, meet aforementioned standards.

3.1.2 Microinverter Resilience Analysis

Conversion of sunlight directly into electricity is done with a photovoltaic solar cell. The photons of light strike a silicon lattice structure which excites electrons that conduct towards a lower potential. [49] This creates a direct current and thus and voltage potential is established across the cell terminals that is inverted to AC power for utility grid consumption. Solar power is an integral part in the widespread adoption of microgrids which in turn are being used to improve power resilience to end users. In 2017 solar power comprised 55% of all added renewable energy capacity. [50] The peak power demand in the US is 500,000MW and current installed solar capacity is 69,000MW. With over 13.8% of demand potentially coming from solar power, the resilience of this resource is crucial. With conventional US grid resilience in normal conditions at 99.9% (provided mostly by thermal Rankine cycle type generation sources) it is vital that solar power installations improve their availability to allow for their widespread adoption over conventional fossil fuels. Solar also offers the benefit of local power generation to increase system resilience during an extreme natural disaster scenario.

The first commercially successful microinverter was released in 2008 by Enphase. This M175 module is capable of providing 175W of peak AC power when connected to a single 24V

photovoltaic (PV) panel. Microinverters provide DC to AC power conversion onboard each individual PV panel. Because of their recent widespread adoption, there is no study into the effect of microinverters on solar installation resilience, especially when compared to conventional string and central inverters. This is likely due to IEEE1547 requiring that most inverters turn off when the grid goes down to prevent islanding and hazards for utility and emergency personnel. With increased PV penetration this loss of generation could prove useful to the utility in emergency scenarios if managed properly. Analysis into the resilience of PV installations is critical to their adoption during emergencies to help support the utility and more immediately, their local load. This work will analyze microinverters and their effects on solar power resilience. It will establish a quantitative method to measure the resilience of a PV installation. For perspective this work will compare PV installation inverter layouts in terms of theoretical resilience during extreme events.

3.1.2.1 Resilience Formulation

Defining resilience in this section is critical to understand the effectiveness of microinverters to improve on the metric. Resilience can be hard to quantify because of the data it requires but a useful method is developed here to analyze the resilience of a PV installation.

In (3.1) resilience is defined as the time a vertex is in service (T_U) divided by the total duration of the extreme event (T_e). [51]

$$R_{SL} = \frac{T_U}{T_e} \tag{3.1}$$

This metric shows the internal resilience of the installation to provide power and thus be considered online. For extreme events like tornados, hurricanes, or other natural disasters this number would be calculated after the fact using mean up time and mean event duration. For many

events over the lifespan of an installation this resilience metric would be calculated but for the sake of this paper that data is not available for comparison. This metric also is very vague for now and depends on past data. A new realization of the uptime is needed to make for a useful metric to analyze the resilience of microinverters.

The power from a PV installation is variable depending on solar irradiance. For night time and cloudy days little to no energy is produced form the solar array regardless to its ability to function properly. The intermittency of solar power is not considered in this work as it is always a problem, whether or not panels or inverters have been damaged and rendered out of service. The uptime (T_U), will herein refer to the installation being in service, whether or not there is power available because of varying solar irradiance during the day. Uptime defines a solar installation as being functional during the day. For night hours the solar installation is out of service of course. This variable is what determines the resiliency directly whereas the event duration (T_e) is dependence on the external factors of the hazardous environment that caused the event.

A solar installation is comprised of many individual PV panels. In a natural disaster there are many points of failure for a PV installation. For this work, consider the panels themselves and the inverter or inverters used to convert the DC output of the panels to the usable AC power. Damage of a panel limits the power production of the entire installation. For a typical panel this means the loss of ~200-400W of power [52]. This will not constitute downtime because the installation is still operational but limited in its power output. The uptime (T_U) of the installation is determined by its ability to support the local load. This means that a certain percentage (x) of the installation power (P_{PV}) needs to be available to keep the load up and running. Uptime is now more specifically defined as the ability of the PV source to supply x percent of its rate power output P_{PV}.

$$T_U = time\ that\ x(P_{PV})\ is\ available\ during\ event$$

Energy storage is being used to increase the energy utilization of solar power. In the case of energy storage paired with the PV installation the resilience of the local load is (3.2).

$$R_{ES} = 1 - (1 - R_{SL})e^{-\frac{T_A}{T_e}} \qquad (3.2)$$

Where (T_A) is the time the battery buffer can supply power to the load autonomously when the solar fails.

3.1.2.2 Photovoltaic Installation Layouts

There are three types of inverters: central inverters, string inverters, and microinverters. A central inverter takes in a series of solar strings which consist of multiple panels in series and then inverts that DC into AC. This method has increased hazards and expenses related to the DC power transfer to the panel and is also very susceptible to efficiency degradation caused by individual panel performance [53]. Shown in Figure 34, the loss of one panel affects the entire installation and the loss of the inverter renders the entire installation out of service.

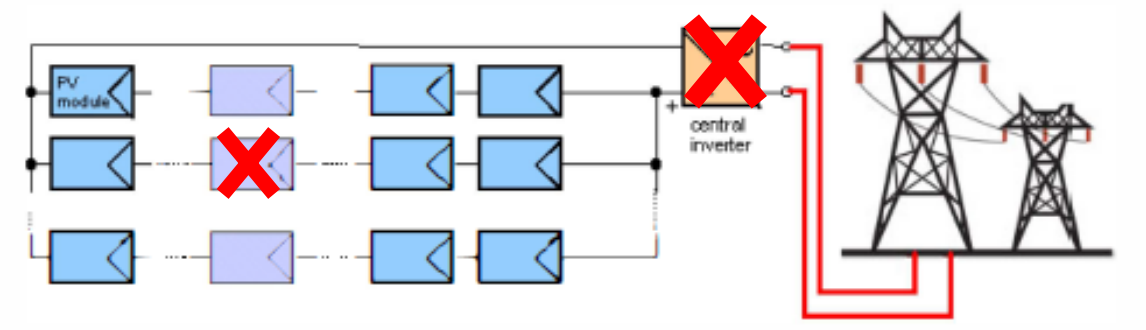


Figure 34. Central Inverter Layout [5]

String inverter layouts consist of multiple panels in series feeding into multiple inverters which are then tied in parallel on the AC side. String inverters are the most commercially viable and widespread due to increased efficiency. If a single panel is shaded or damaged, Figure 35, then only one string will suffer in efficiency rather than the entirety of the solar installation as in the case of a centralized inverter [54]. Note however that the loss of one inverter removes the entire string of panels from service. The resilience of solar power is improved by string inverters because a single inverter is no longer a single point of failure.

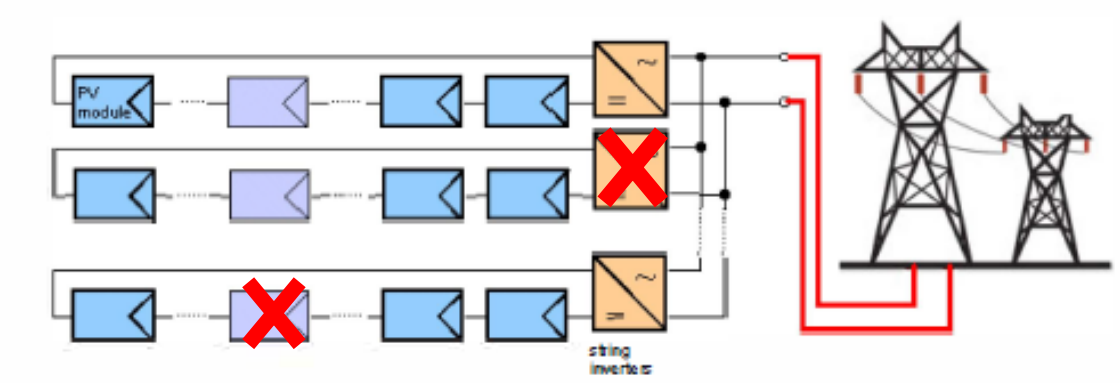


Figure 35. String Inverter Layout [5]

Microinverter systems take the inverter down to the level of each panel and connect in parallel at the AC side, shown in Figure 36. These systems limit the need for excess and hazardous DC wiring. The maximum power point of each panel is now achieved on an individual basis and this increased resolution for maximum power point tracking (MPPT) boosts efficiency of the system [55]. System resilience potential is also greatly improved because a single panel failure due to damage of the panel or inverter (red 'x') or shading does not affect any of the other panels but simply reduces the power output of the overall system by a few hundred watts. The challenge in this scenario is balancing the power produced with the power consumed and schemes have been developed, [56], to achieve this. With this work only the percent power demand required to sustain the load in the emergency scenario (x) as mentioned in the previous section.

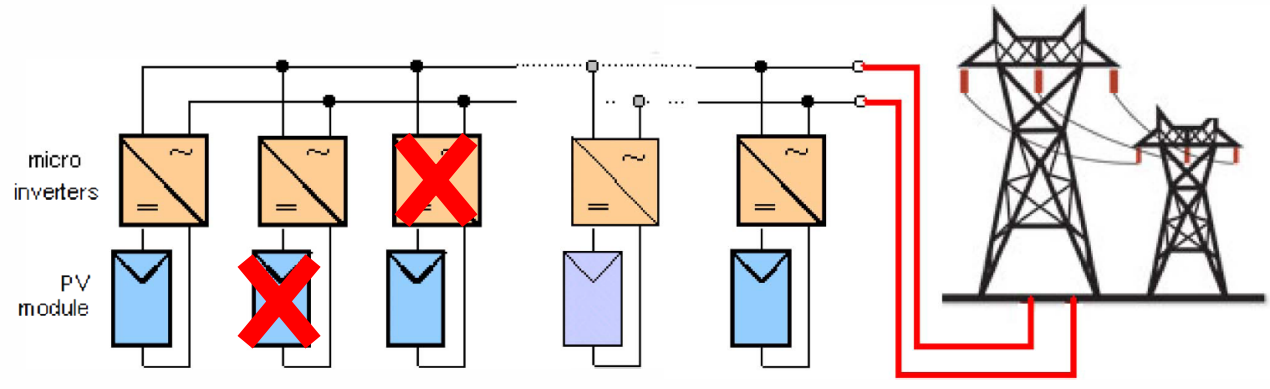


Figure 36. Microinverter System Grid Tie [5]

3.1.2.3 Scenario Analysis and Quantitative Framework

Two components of the PV system are considered, the panels and the inverters which can either operate or fail because of physical damage caused by a natural disaster. The panels and inverters have binary states of failed (0) and working (1) designated by (p_n) panels and (i_n) inverters. The rated panel power output will be (r). For a given system comprised of microinverters the available power is (3.3).

$$P_{micro} = (p_1 * i_1 + p_2 * i_2 + \cdots p_n * i_n) * r \qquad (3.3)$$

Because each panel has its own inverter assume that if one component fails the other will fail. For example, if a panel is ripped from a roof then it will take the microinverter along with it. One cannot work without the other.

A string inverter system power rating will differ because the loss of one inverter takes out that entire string of panels from service. The variable i is now binary for a given string inverter 1 being functional and 0 being failed. The p_n variables represent the number of working panels in a given string, (3.4)

$$P_{string} = (p_{s1} * i_{s1} + p_{s2} * i_{s2} + \cdots p_{sn} * i_{sn}) * r \qquad (3.4)$$

For a central inverter the equation is similar but with only *i* to represent the failure state of the centralized inverter whereby all working panels (*p*) rely, (3.5).

$$P_{central} = p * i * r \quad (3.5)$$

String series voltage issues are ignored for now to simplify the problem. This is critical to the analysis however because the loss of multiple string panels will drop the DC voltage so low the inverter cannot operate. Failures of a panel in a string assume loss of power from that panel but continued electrical connection through the entire string.

Now comparing the available power rating of a PV installation to the power required by the local load during the disaster scenario we have, (3.6).

$$P_{micro,string,central} \geq xP_{PV} \quad (3.6)$$

This states that to be considered uptime and providing the load power, a certain portion ($0 < x < 1$) of the installed PV is available.

3.1.2.4 Example Case Study

An example scenario of a 30kW PV system is analyzed to compare the results of the proposed method. For this system there is a local load of 20kW that needs powered and thus 10kW is typically sent to the grid at full 30kW PV output. This means that a $x = 2/3$ portion of the PV power is needed to consider the installation running as backup (uptime, T_U). The system layout is 30 panels each rated at 100W. There are 3 strings of 10 panels for the string and central systems. The full sunny days are 12 hours long with nighttime of 12 hours where irradiance is near zero. All PV installations could withstand an entire string of 10 panels being destroyed. They would all still be able to produce the 20kW of power to the load. The resilience of the micro inverter system is exemplified when random panels and or microinverters are destroyed. They can withstand much more complicated damage of their installation. The central inverter system cannot withstand any

failure to its inverter and the string system could only provide necessary power with the loss of one string inverter. The microinverter system can lose up to 10 microinverters and panels and still supply the required percentage of load. For a 72-hour event (T_e) this would lead to a resilience of R_{SL} = 12*3/72 = 0.5. With a battery buffer that can last 24 hours (T_A) for the 20kW required load the resilience would be $R_{ES} = 1 - (1 - R_{SL})e^{-\frac{T_A}{Te}}$ = 0.642.

3.1.2.5 Microinverter Resilience Implications

This section presented a way to quantize the resilience of microinverter solar installations and well as centralized and string types for comparison. It explains how microinverter systems are more robust and have more potential to have a higher resilience in disaster scenarios. A case study is used to walk through the process of calculating the resilience of a PV system with and without energy buffers for autonomy. The work could improve by incorporating the complexities of string systems where a minimum number of panels is needed in a given string to provide a high enough series voltage to operate that strings inverter. In conclusion this method can be used to evaluate a microinverters resilience for certain failure scenarios. It could also take past events and evaluate system resilience for insight on designing more resilient layouts in the future.

3.1.3 Microinverter Capability Analysis

Table IX. Comparative Analysis of the Boost Component of Microinverters

Converter Type	Voltage Gain	Voltage Stress on MOSFET(s)	Voltage Stress on Secondary MOSFET(s) & Diode(s)	# of MOSFETs	# of Diodes
Flyback with bidirectional switches [57]	$\frac{nD}{1-D}$	$\frac{V}{nD}$	$\frac{V}{D}$	3	-
Interleaved Flyback with active-clamping [58]	$\frac{nD}{1-D}$	$\frac{V}{nD}$	$\frac{V}{D}$	4	2
Interleaved Flyback with adaptive-snubber [59]	$\frac{nD}{1-D}$	$\frac{V}{nD}$	$\frac{V}{D}$	4	2
Flyback with dissipative-snubber [60]	$\frac{nD}{1-D}$	$\frac{V}{nD}$	$\frac{V}{D}$	1	2
Flyback converter with voltage multiplier [61]	$\frac{1+2n-nD}{1-D}$	$\frac{V}{1+2n-nD}$	$\frac{nV}{1+2n-nD}$	2	3
Boost-Flyback/Flyback converter [62]	$\frac{1+nD}{1-D}$	$\frac{V}{1+nD}$	$\frac{nV}{1+nD}$	3	1
Flyback converter with Voltage-Doubler [63]	$\frac{n}{1-D}$	$V_{PV}+\frac{V}{n}$ V_{PV} is nominal PV voltage (Vin)	$\frac{nV_{PV}+V}{2}$	2	2
Proposed Converter	$\frac{n(N-1)D}{1-D}$	$(1-D)(V_{in}+\frac{V}{n(N-1)})*$	$\frac{V}{(N-1)D*}=\frac{V}{N-2+D}$	3-4	3-4*

3.1.4 Power Converter Optimization

Optimization for power converters can take on many forms. Single or multi-objective problems can be solved. For example, efficiency itself can be optimized as a single objective but this design will likely not be as power dense as if power density was the design objective. This leads to a multi-objective optimization problem where tradeoffs can be made between efficiency and power density. This work focuses on the single objective problem of efficiency to prove the electrical capabilities of the proposed converter. Power density objective optimization could be

done beyond this work in order to shrink the device down for commercial use. Techniques from all forms of optimization are useful however, in the formulation of this work.

A multidimensional optimization of efficiency, output capacitor current ripple, and core temperature rise of boost and flyback converters was done. [64, 65] Many variables were chosen before doing the optimization such as input and output voltage and load power requirement, whereas some papers leave the optimization more open ended. The optimizations were done in many dimensions for varying f_s and turns (N, this is just core turns but they also do turns ratio which they call gamma). Certain values were varied and then eff was optimized at those various points and then this generated 3D surfaces which could be analyzed for the optimization relationships. They also discuss weighting functions as to what matters more in some cases, cost or efficiency, etc. Another point made was that optimization is not always possible. Sometimes, like in my case with discrete converter levels (*N*), the optimal choice would be unrealizable such as zero or infinity and in these cases the variables will need constrained in order to find a realizable result to the optimization. Again, optimizing two things is not always possible because one will be in contention with the other, for example in the paper they cannot both maximize efficiency while minimizing output capacitor current ripple.

One work detailed an optimization process for a boost converter that was powered with fuel cells for portable military applications. [66] The metrics of optimization are efficiency, switching frequency, capacitance, on resistance of FETs, current density, and inductor ripple. These values were found at which point the mass would be minimum and then the plots were made as a function of mission duration. The paper has useful equations to predict switching and conduction losses for transistors and diodes. It also discusses how to estimate loss components like

gate charge from the data sheet. Other optimizations have been done for the basic converter structures and for varying objectives tied to efficiency. [67, 68]

3.2 Diode Conduction Loss Alternative Model

In Directive II the diode forward conduction loss model was derived using data sheet power loss equations. In some cases, the diode power loss curves are not supplied. Rather, the on-resistance (R_d) and forward voltage drop (V_d) are provided. In which case the optimization routine needs to account for this, and the diode loss model is presented below.

$$P_d = R_d {I_{sec}}^2 + V_d I_{sec} \tag{3.7}$$

3.3 Magnetic Optimization (*n*)

3.3.1 Preface

This section explores the magnetic optimization of FCMFC. This is left out of the overall optimization of the FCMFC as described in this dissertation but was critical to visit as a topic because of how key the magnetic design is too the flyback converter and thus FCMFC. This section will analyze the effects of optimization as they relate to a varying number of converter levels or flying capacitors. A full-scale optimization could not be done without at least visiting this topic as is done herein. The results here are important but in essence will justify why a single off-the-shelf transformer was chosen to do the overall converter optimization.

The flying capacitor multilevel flyback converter (FCMFC) utilizes a flyback transformer in conjunction with multiple switch-diode-capacitor (SDC) stages to improve operation of the basic flyback converter for DC-DC power conversion. This section explores the multi-objective optimization of the double-wound inductor of the 200W FCMFC. The core geometry will be optimized for various multilevel converters to yield the most efficient and lightweight inductor. The optimized inductor design exhibited 0.73W loss and corresponded to a basic flyback two level converter while the lightest design of 35g corresponded to a five level FCMFC. While the flyback inductor was most efficient, it was also the heaviest with an anticipated mass of 186.25g, compared to the 35g inductor that only exhibits a loss of 1.11W. All multilevel converters follow the Pareto optimal front making SDC stages a useful design variable for the magnetic optimization of a flyback converter.

3.3.2 Background and Motivation

To achieve grid parity for cost of power production, microinverters are providing cost effective solutions for distributed photovoltaic (PV) generation. In large PV strings, the absence of one panel due to shading or damage often results in the loss of power production from that entire string. Microinverters offer the ability to have on-panel inversion making each panel an independent AC generating source which can increase total solar energy production but at higher cost, [69]. The challenge arises for small cost yet effective microinverters for on-panel inversion. This research effort focuses on the challenge of boosting the low panel output DC voltage to a level high enough for inversion by modifying the inexpensive flyback converter.

The flyback converter includes a magnetic device commonly referred to as a transformer because of the isolation and voltage transformation from primary to secondary. However, the way

that the magnetic component is operated prohibits the magnetic component from being classified as an ideal "transformer" because it does store energy for a short time between charge and discharge cycles. Some have referred to the component as a mutual inductor, but this terminology is also not precise because there is no current coupling between the two inductors. Instead, the terminology of a double wound inductor, or simply inductor, will be used throughout this work as the flux only exists in the primary winding during the ON time of the main switch and in the secondary winding during the OFF time. Most of the energy is stored in the air gap of the core due to the low reluctance which dominates the effective core permeability and inductance.

Reliability, cost, and grid interaction are the key drivers of microinverter technology. The flyback converter is an inexpensive and basic topology and when modified with flying capacitors the switching stress is significantly decreased for higher reliability. Hence, a potential candidate for meeting these key drivers mentioned for future microinverters is the FCMFC. A generalized FCMFC is shown in Figure 1 with a single switch diode flying capacitor stage outlined. Multiple converters can be derived from this general form for N levels where (N-1) is the number of capacitors of a given converter. The double wound inductor provides isolation and higher gain capability in the event of solar shading to maintain the maximum power point of the downstream inverter, [70, 71]. The FCMFC is an improvement in this area because of the significant increase in its voltage conversion ratio while maintaining high efficiency, [72, 73, 74].

The contribution of this work is to optimize the double wound inductor by minimizing mass and power loss for the FCMFC. The double wound inductor is typically the heaviest and most lossy component of a flyback converter. Mass and power loss of the double wound inductor are minimized over a practical design space and it is shown that flying capacitors, as a variable in the optimization routine, are a useful modification to the flyback converter when optimizing the

double wound inductor. The section is outlined as follows. In Section 3.3.3, the operation and relevant equations for the FCMFC are defined and compared to a flyback converter. In Section 3.3.4, the magnetic model used within the optimization is defined. Section 3.3.5 explains the optimization process with results discussed in Section 3.3.6. Section 3.3.7 will conclude this discussion on magnetic optimization and discuss broader implications as they pertain to complete converter optimization.

3.3.3 FCMFC Operation for Magnetics

The converter is operated using phase shifted pulse width modulation to cycle the individual stages in conjunction with the magnetizing inductance, L_m. Each capacitor on the secondary is charged by the magnetizing inductance in conjunction with the previous capacitor stage, resulting in greater energy transfer per switching cycle, tending the converter towards continuous conduction mode (CCM) where it has higher voltage gain as seen in (3.8), [72]. Where D is the duty cycle of the primary input switch, n is the inductor turns ratio, and $(N\text{-}1)$ is the number of capacitors at the secondary side. Figure 37 shows the anticipated gain of FCMFC converters. Equation (3.9) shows average inductor current for a given load, R, and output voltage, V. Equation (3.10) is the required magnetizing inductance, L_m, for a given current ripple, Δi_{Lm}, and switching frequency, f_s, [26]. The number of stages affects all three values by increasing the converter voltage gain and average current while lowering the inductance requirement as shown in Figure 38. For a N = 3 converter or adding a single flying capacitor to a flyback converter, it is apparent that the inductance value required is reduced by half of the standard flyback converter. Operating duty cycle will decrease for a higher number of stages which also impacts the values below as shown in [73, 74].

$$M(D) = \frac{V}{V_{in}} = \frac{n(N-1)D}{1-D} \tag{3.8}$$

$$I_L = \frac{n(N-1)V}{R(1-D)} \tag{3.9}$$

$$L_m = \frac{V_{in}D}{2f_s\Delta i_{L_m}} \tag{3.10}$$

Also, of note are the switching stress benefits that come with the multilevel structure that distributes voltage to lower effective blocking voltages. Because the voltage gain is spread across (*N*-1) stages, the main switching node at the drain node of *S* will experience a proportional decrease in blocking voltage, V_{BS}, shown in (3.11). The secondary switches benefit similarly as shown in (3.12); each having the same voltage rating of V_{BSS}. Higher stage converters result in lower stress on the input switch and the individual output switches which can be seen in Figure 4, where the stress is normalized to the primary switch on a flyback converter. Again, it is apparent that a single flying capacitor can reduce the stress on the input switch. There is a tradeoff seen for higher level devices with conduction and active device losses. As the levels increase, the conduction and active device losses start to grow and make the converter less efficient. This tradeoff is studied in [74]. For the sake of this work, the magnetic optimization is constrained to a N = 5 level device.

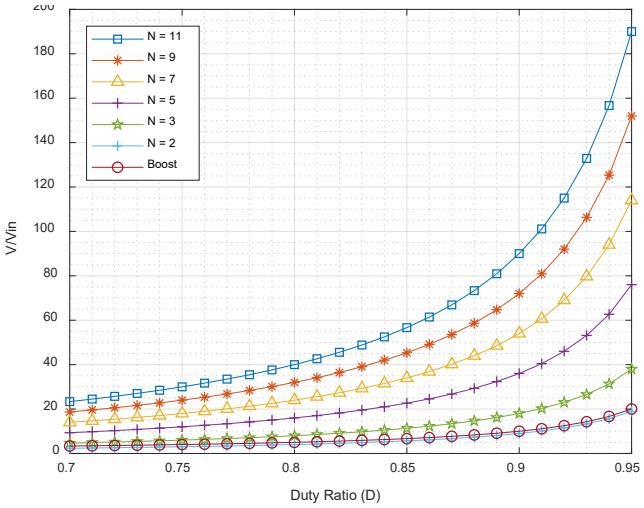


Figure 37. FCMFC Gain Comparison

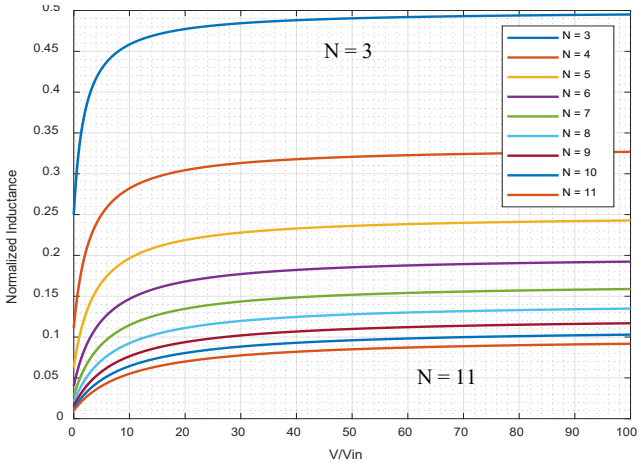


Figure 38. Magnetizing inductance requirement for current ripple normalized to flyback magnetizing inductance.

$$V_{BS} = V_{in} + \frac{V}{N-1} \tag{3.11}$$

$$V_{BSS} = \frac{V}{N-1} \tag{3.12}$$

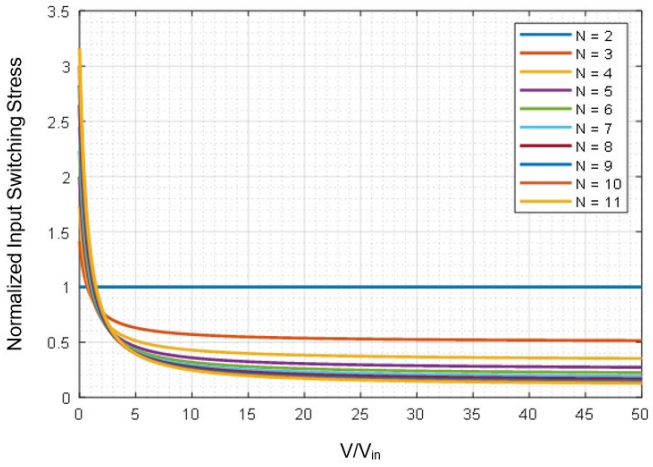


Figure 39. Input switching stress relative to flyback converter.

3.3.4 Modified T-Model Magnetic Equivalent Circuit

The T-model equivalent circuit is a common method and well established, [75]. The equivalent circuit has been modified to function as a double wound inductor for the FCMFC, with an air gap added to prevent magnetic flux saturation, [76, 77]. The air gap has low permeability, μ, resulting in a high reluctance relative to the rest of the magnetic path as can be seen using (3.13) given that $\mu_{air} << \mu_{core}$. Where l_a is the mean free core path length, A_a is the core area, and μ_a is the permeability of the core or air gap. As a result, the energy stored in the magnetic device between switching cycles is primarily stored within the air gap. Higher overall equivalent reluctance, R_x, indicates a greater number of turns, N_x and, thus, winding is required for a particular inductance, L_x, as shown in (3.14). This will impact the conduction mode of the overall converter as shown by the inequality in (3.15), where T_s is the switching period, [74]. If the K_{crit} value is below K then the converter operates in CCM and when K_{crit} is above K, the converter operates in DCM.

$$R_a = \frac{l_a}{A_a \mu_a} \tag{3.13}$$

$$L_x = \frac{{N_x}^2}{R_x} \tag{3.14}$$

$$K > \left[\frac{(1-D)}{n(N-1)}\right]^2 = K_{crit}(D, n, N)\ , \tag{3.15}$$

where, $K = \frac{2L_m}{RT_s}$

Figure 40 shows the toroidal core with air gap and primary and secondary windings where the cross section of the core is constrained to be square. The depth of the core will be defined by w_e and w_s and is fixed for all four inner sides. Other dimensional constraints and free variables are shown in Table X.

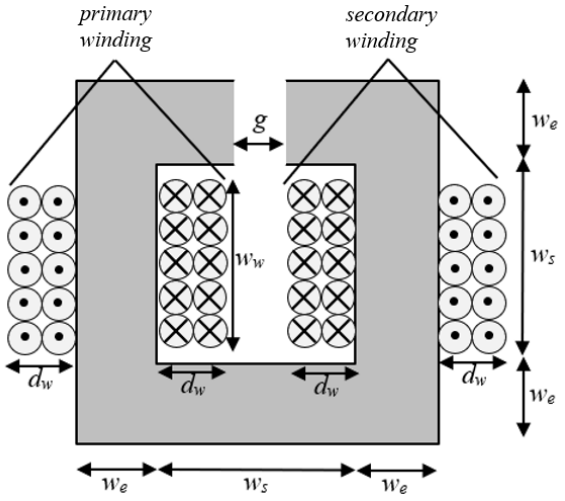


Figure 40. Double wound inductor with air gap.

Table X. Geometric Parameters Associated with Core

Symbol	*Description*	*Type*	*Value*
w_e	core square area side length	free	5mm-20mm
g	air gap length	free	1mm-3mm
μ_r	relative permeability	free	160 or 200
d_w	wire depth	free	$(N*k_{pf}*A_w)/w_w$
$N_{p,s}$	core turns	free	20-1000
w_s	core side length inner	fixed	2.5cm
w_w	core wire length	fixed	2cm

Magnetic materials were chosen to have a linear permeability at the desired switching frequency of 100 kHz. Two materials were assumed from Magnetics®: molypermalloy powder (MPP, $\mu_r = 200$, 8.0g/cm^3) and high flux ($\mu_r = 160$, 7.6g/cm^3), both having a saturation limit of 400mT, shown in Table XI.

Table XI. Core Materials

Name	*Rel. Permeability* (μ_r)	*Density*
MPP	200	8.0 g/cm^3
High Flux	160	7.6 g/cm^3

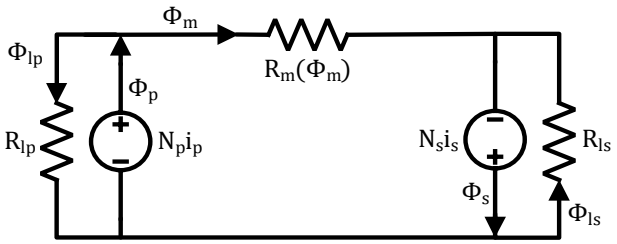


Figure 41. T-Model magnetic equivalent circuit model [4].

The magnetic equivalent circuit, Figure 41, accounts for primary and secondary leakage reluctances as well as core reluctance R_m, which includes the reluctance of the air gap. This model is used to calculate flux through the core when the main switch, *S*, is ON and OFF. Note that because the primary and secondary turns are held the same, the MMF is the same for charging and discharging of the double wound inductor, (3.16). Where Φ_m is magnetizing flux, N_p is primary turns, i_p is primary current, and R_m is magnetizing path reluctance. Calculating exterior adjacent conductor leakage reluctance is done as per the method in [75], using a path shown in Figure 42 Figure 43 and discrete reluctance elements for the leakage path shown in Figure 43. Expressions are adjusted per the modifications to the toroidal core of this work shown in Figure 40. Reference Figure 40 and Table I for dimensional variables shown in (3.17), (3.18), and (3.19). First the

reluctance is calculated associated with the flux flowing around the winding, (10), then the permeance for the flux flowing within the winding, (12), is calculated using the flux path illustrated in Figure 43. These are combined to yield the total leakage reluctance for a winding, (11).

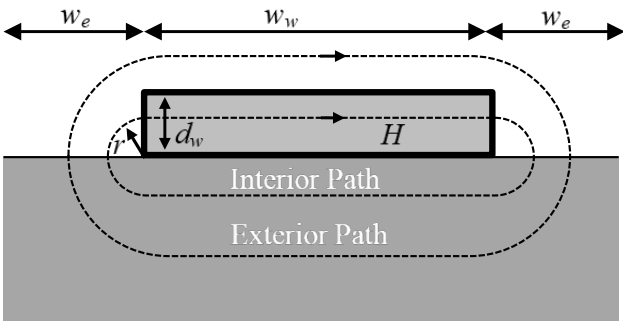


Figure 42. Exterior adjacent leakage flux path [7].

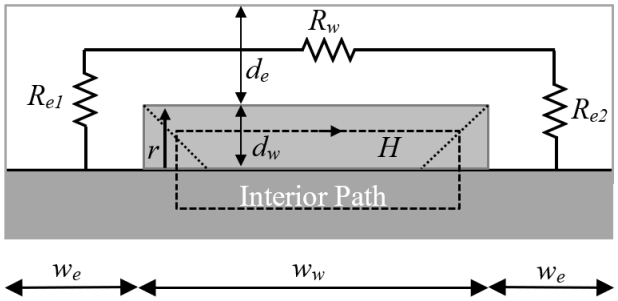


Figure 43. Discrete reluctance elements for exterior adjacent leakage flux path [7].

Using (10) the reluctance can be calculated for the primary and secondary winding and then used to find the primary and secondary leakage inductance for a given design. This inductance using the input and output currents respective to the primary and secondary, leads to an energy loss per switching cycle.

$$\Phi_m = \frac{N_p i_p}{R_m} \tag{3.16}$$

$$R_{eale} = \frac{2d_w w_e + \sqrt{(2w_w + 2w_e)(2{w_e}^3)}}{2\mu_o {w_e}^3} \tag{3.17}$$

$$R_{lp,s} = R_{eale} + \frac{1}{P_{eali}} \tag{3.18}$$

$$P_{eali} = \frac{\mu_o w_e}{256 {w_w}^2 {d_w}^2}[16{k_2}^4 + 16\sqrt{2}k_1{k_2}^3 + 4{k_1}^2{k_2}^2 - 2\sqrt{2}{k_1}^3 + {k_1}^4 ln\left(1 + \frac{2\sqrt{2k_2}}{k_1}\right) \tag{3.19}$$

$$k_1 = |w_w - 2d_w|$$

$$k_2 = \frac{1}{\sqrt{2}}\, min(2d_w, w_w)$$

The equivalent circuit model, shown in Figure 44, includes the magnetizing and the loss components, leakage inductances and winding resistances. For the double wound inductor, only the primary or the secondary winding will conduct with the common magnetizing inductance at a given time. When the switch is ON the primary side charges the magnetizing inductance and when the switch turns OFF the secondary side will conduct using the charged magnetizing inductor. 18AWG magnet wire was chosen with a diameter of 1.024mm and dielectric breakdown of 5130V with a resistance of 0.02139Ω/m and weight of 0.00732kg/m. Primary winding loss is expected to be higher due to the higher current present in that winding. The length of 1 turn is $4w_e$. Providing an extra 2cm on each terminal for mounting yields a resistance for the primary and secondary winding as $0.02139(4Npw_e + 0.02)$ meters.

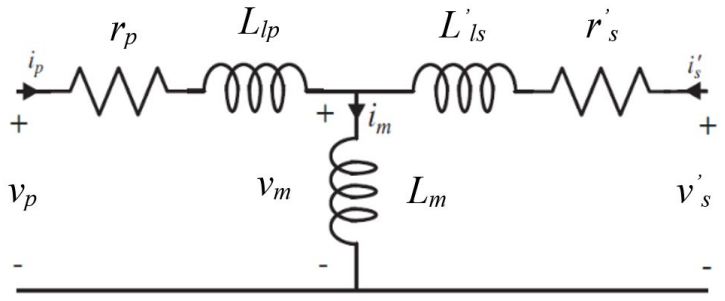


Figure 44. T-Model electrical equivalent circuit model.

3.3.5 Optimization Process and Fitness Functions

This work seeks to achieve multiple low mass and low power loss designs for the magnetic component. Core size, material, and wire arrangement are considered here with the added variability of the converter's flying capacitor stages. This new variable in the tuning process of the optimization expands the design space for the magnetic component, yielding useful results that justify the use of FCMFC. Electrical operating parameters considering photovoltaic panel output voltage boosting applications are as follows: $f_s = 100\text{kHz}$, $V_{in} = 40\text{V}$, $V_{out} = 400\text{V}$, and $P = 200\text{W}$.

The optimization space spans the following free variables: core square area side length (w_e), air gap length (g), magnetic material (μ_r), converter stages (N-1), and turns ($N_{p,\,s}$). Converter levels of $N = 2, 3, 4, 5$ were included; this spans from a flyback converter up to a FCMFC with four capacitor stages, which is three flying capacitors and one output capacitor at the load for the $N=5$ case. Primary and secondary core turns are varied from 20 to 1000 considering the physical-geometrical packing limits. The core permeability and geometric variables varied as per Table X and Table XI. Code was written to calculate the loss and mass components based on wire length, core geometry and provided density values.

MATLAB code was generated to search all possible designs within the space defined by Tables I and II. Nested for loops were used to iterate designs in the following hierarchy: converter level (N-1), core permeability (μ_r), turns ($N_{p,\,s}$), air gap length (g), and core square area side length (w_e).

First, magnetizing and leakage inductances are calculated for the magnetic equivalent circuit defined Section 3.3.4 using equations (3.13, 3.14, 3.17). Constraint checking is done immediately after this step to ensure the design operates in CCM (3.15) and will not saturate the core (3.16); the saturation limit being 400mT. If a design fails, then it is dropped, and the code

starts again on the next increment in the space. If the design passes the constraint check then the code continues to calculate all mass and loss variables.

The final, functional, design space included 192,967 designs which was reduced using an algorithm to check for non-dominated designs. Each design was compared to the rest using for loops and comparators. If the design being reviewed was found to be worse at both loss and mass than another, then that design was not stored for later use. The initial design space of nearly two-hundred thousand is now reduced to 24 candidate designs. Each one of these designs is better than all of the others in one of the two metrics, power loss or mass. These remaining 24 non-dominated designs form the Pareto optimal front shown in Figure 8. Different symbols are used to exemplify the occurrence of all FCMFC converters in the optimal front.

3.3.6 Results and Discussion of Magnetic Optimization

Twenty-four designs with mass ranging from 35.30g to 186.25g and loss ranging from 0.73W to 1.11W form the optimal set within the design results in Figure 45. This is the Pareto front for the magnetic optimization and includes all non-dominated designs; meaning that every design in the front is not bested by another for both power loss and mass. The most efficient double wound inductor was that of a flyback converter (N=2) with a loss of 0.7265W but also the highest mass of 186.25g as shown in Table III highlighted in light grey. The peak current seen through the leakage inductance is lower for the flyback and is the primary driver for this being the converter with the least power loss. In dark grey, a FCMFC converter (N=5) was the least massive at only 35.39g with a loss of 1.1105W. This is significant because the inductor is typically the largest mass component of a flyback (or FCMFC) converter. Highlighted in Figure 45 are four converters that have both low mass and loss and these are further illustrated in Table XII with their component

design values. Looking at other cases shown in the table, a power loss of 0.971W is achieved with a mass of 47.95g. Comparing to the most efficient flyback case in light gray, it is apparent that for an additional 25mW of power loss the mass of the inductor can be drastically reduced by 138.3g or 74%. All four converters included in the design (*N=2,3,4,5*) space result in a design that is in the reasonable trade-off (lower left) zone of the Pareto front.

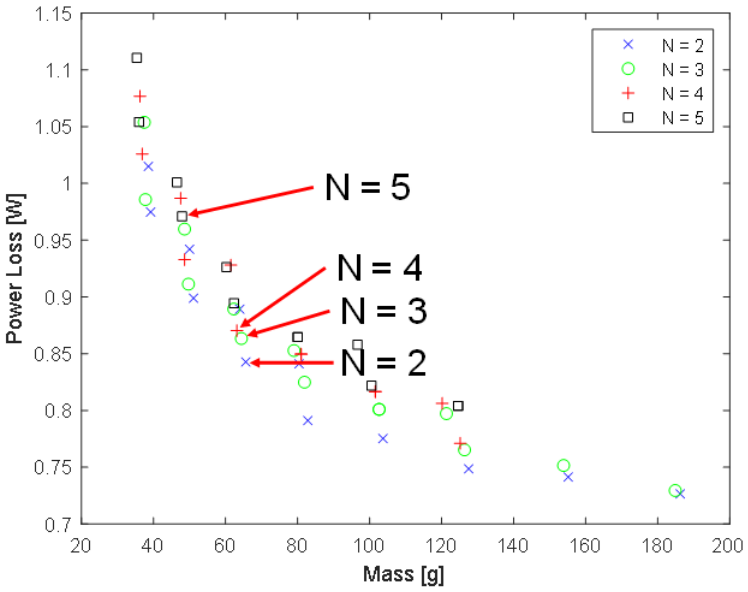


Figure 45. Pareto Optimal Front

Table XII. Optimal Design Results

P_{LOSS} [W]	Mass [g]	Lvl [N]	Perm [μ_r]	Turns [$N_{p,s}$]	w_e [m]	L_m [H]	L_l [H]	I_L [A]	Δi_L [A]
0.8427	65.63	2	200	37	7m	51.6µ	145n	5.5	3.52
0.8633	64.40	3	200	34	7m	43.5µ	132n	6	3.82
0.8702	63.17	4	200	31	7m	36.2µ	119n	6.5	4.25
0.9708	47.95	5	200	34	6m	32.4µ	140n	7	4.41
0.7265	186.25	2	200	22	12m	50.5µ	610n	5.5	3.60
1.1105	35.39	5	160	42	5m	31.8µ	189n	7	4.49

The more efficient magnetic component designs have lower converter levels because they require less peak current to maintain CCM. This effect results in lower leakage loss on the primary

side of the component. However, it is of note that for the entire power electronic converter there are more dynamics to consider that would make the FCMFC more efficient and is currently being proven by the research team. Winding losses are similar at higher stages due to lower required duty cycle and thus similar average input currents. Also note the lower switching stress for higher *N* devices outlined in Section II. The less massive designs, however, are those with more converter stages because more of the energy in the conversion process is stored in the flying capacitors. Note that the higher *N* values shown in Table XII have lower magnetizing inductance values. Both observations can be seen in Figure 45. To further illustrate this point separate Pareto fronts were generated for each of the four converters (*N2*, *N3*, *N4*, *N5*) and are shown in Figure 46, Figure 47, Figure 48, and Figure 49. The current code can generate these separate Pareto fronts if the designer has explicit reasons to choose one of the various FCMFC converters. For example, higher voltage gain could be desirable and thus a higher *N* level device would be fitting, and its Pareto front can be identified and analyzed. The 45 designs shown across all four plots include each of the 24 overall Pareto front (non-dominated designs) in Figure 45. Notice the axes of each plot for power loss and mass. In Figure 46 the flyback converter shows lower loss but higher mass values. Going from Figure 47, Figure 48, and Figure 49, the power losses values trend slightly higher but mass values decrease significantly. This mirrors the results seen when comparing all converter types in Figure 45. If one converter type was desirable for its gain benefit then the optimization could be constrained to only include that level of device (i.e., N=2,3,4,5, etc.).

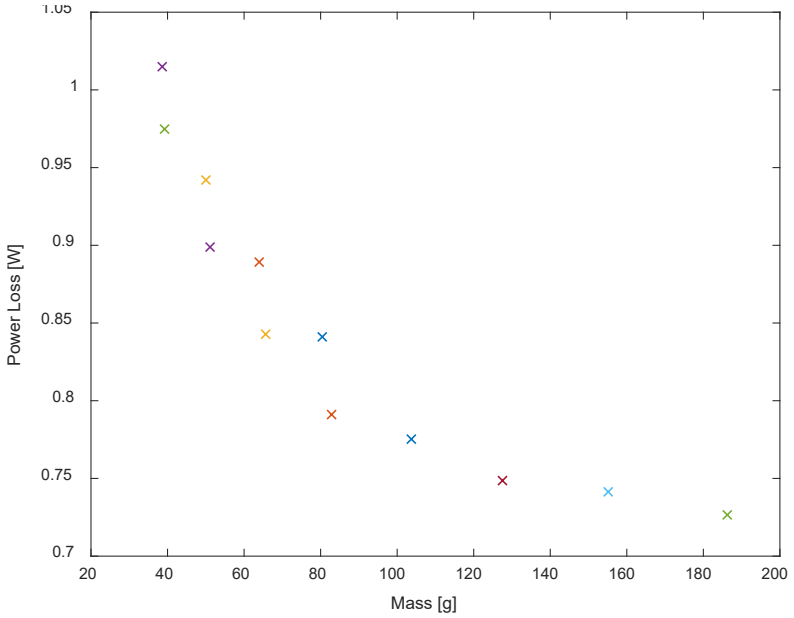


Figure 46. Pareto Front N=2

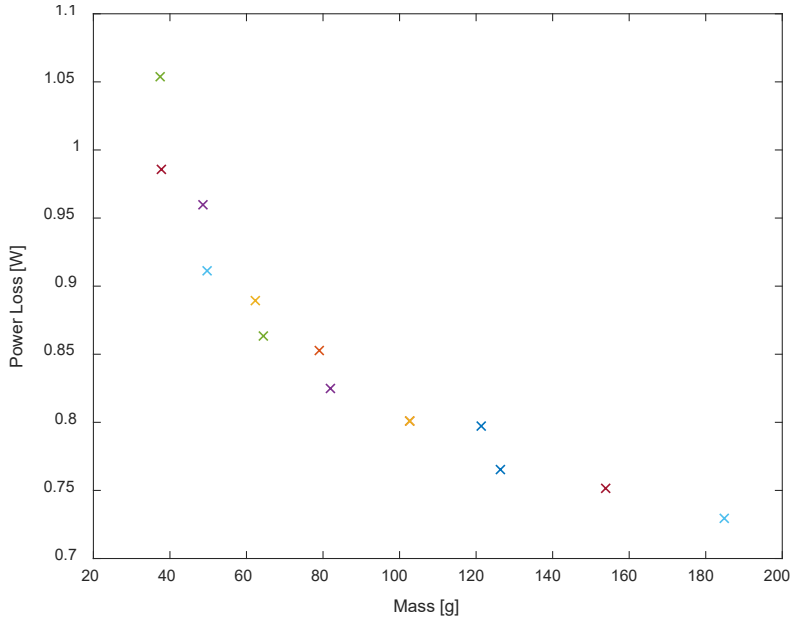


Figure 47. Pareto Front N=3

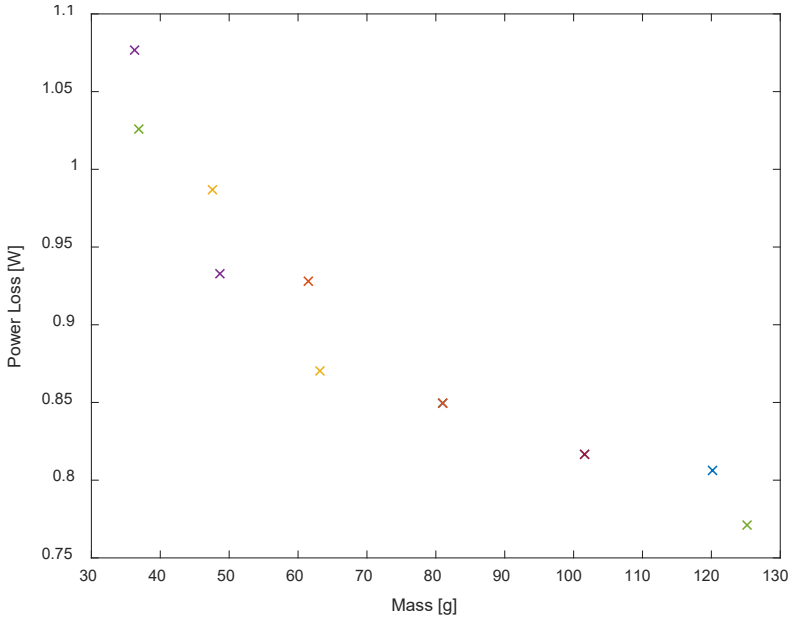


Figure 48. Pareto Front N=4

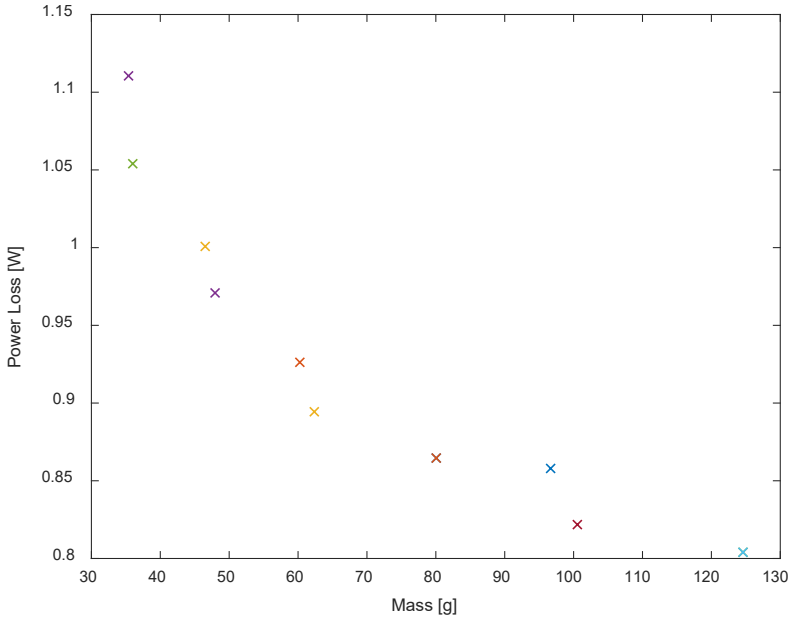


Figure 49. Pareto Front N=5

3.3.7 Implications of Magnetic Optimization

Modifying a flyback converter to support flying capacitors had a positive impact on the operation and design of the double wound inductor that is inherent and key to the flyback converter mass and efficiency performance. The FCMFC has been previously analyzed for efficiency with little detail paid towards the magnetic component design. The goal of this work was to analyze the effect of flying capacitors for FCMFC when optimizing the magnetic component. Optimal designs included converters of each of the 5 levels that were included in the design space. Higher level converter magnetics tend to be lightweight while lower-level converter magnetics tend towards improved efficiency when only considering the efficiency of the magnetics. When considering the overall converter, the efficiency benefits would tend back towards higher level stages but is not the purpose of this work. A trade-off does occur that includes a choice of converter level making it a useful tool in the optimization of a double wound inductor. Further work using this process will expand the design space for multiple core geometries. When designing the magnetic component of a flyback converter, the designer can now consider a new variation in the optimization through the flying capacitor stages.

Flyback transformer optimization has been done before and it could benefit FCMFC but not critical to this work with a multilevel structure and its effect on efficiency. Because FCMFC cycles the transformer so similar to the flyback, a magnetic optimization would not yield justifiable benefit for the overall converter optimization proposed here.

3.4 Component Selection Mechanism

As proven in Directive I, the higher order an FCMFC converter, the lower the voltage stress and thus required rating of semiconductor devices. In the prototype this was not taken advantage of because robust design and reliability were paramount to verify the novel converters functionality. Now that the converter has been proven to operate in a stable matter with open loop control, a component selection mechanism will be used in the optimization process. The key is that lower voltage rating devices have inherently lower on-resistance and will thus experience lower conduction losses and make the converter more efficient. The higher the order (N), or more flying capacitors a device has, the more the voltage is reduced that each stage must withstand. The following subsection will detail how and why this works for semiconductors, MOSFETs, in particular, due to the thinner required epitaxial layer.

3.4.1 Discussion of Power MOSFETs Epitaxial Layer and Voltage Rating vs ON Resistance

The FCMFC is comprised of a multiple power conducting semiconductors components depending on the designed level. This can be as little as 2 MOSFETs and 3 diodes up to 12 MOSFETs and 13 diodes. These components have a conduction loss associated with them during their on-state. Depending on the size of the component there is a specific on resistance. The blocking voltage will vary depending on the N level selected. The higher the level and more flying capacitors, the more the output voltage is distributed and thus lower the blocking voltage required by the semiconductors. Up until now, the same semiconductors were used for each FMCFC for robustness and also design simplicity. This directive will now consider the variation in voltage rating and allow for a more detailed component selection.

It would seem that more FETs and diodes would results in higher conduction losses because of the additional resistances that are added to process the power from input to output. However, this is not the case because on-resistance is a function of blocking voltage. The resistance between source and drain terminals is a combination of many layers of the FET, shown in Figure 50. This includes from top-to-bottom: source (R_s), channel (R_{ch}), access (R_a), parasitic implantation (R_{JFET}), epitaxial (R_n), and drain (R_D) resistances. The layer of concern here is the epitaxial layer which determines the voltage breakdown or "rating" of the device. A higher voltage rating requires a thicker, low-doped, and thus highly resistive (R_n) epitaxial layer. [78] This results in an over increase in drain-to-source on-resistance of the FET. A lower rated FET would thus require a thinner epitaxial layer and have a correspondingly lower on-resistance. A similar relationship exists for diodes. In the case of FCMFC, this means that higher level converters which result in lower voltage ratings allow for semiconductors to be used that have lower conduction losses.

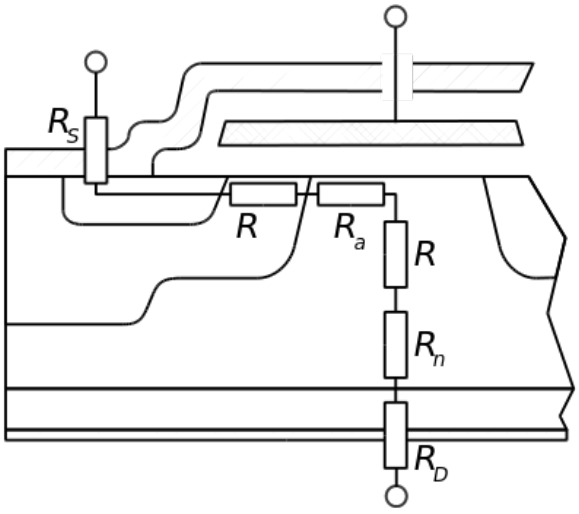


Figure 50. MOSFET Resistance Breakdown [79]

This relationship is further illustrated in the figure of merit plot in Figure 51. It can be seen that for many FETs the specific resistance increases as the breakdown voltage increases. This

relationship will benefit the FCMFC optimization significantly because the voltage ratings are reduced to ½, ⅓, ¼, etc. as the number of flying capacitors is scaled up.

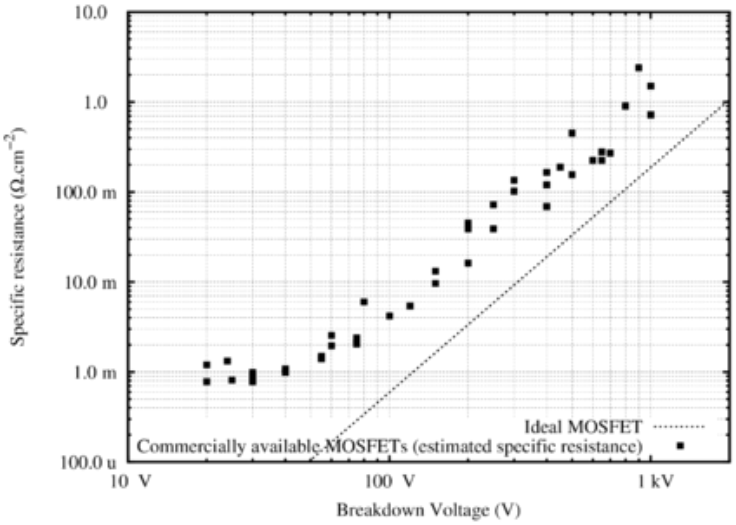


Figure 51. $R_{DS,ON}$ Figure of Merit [79]

3.5 Multilevel Design Process (*N*)

The optimization process for a voltage boosting converter is outlined in Figure 52 where minimal power loss is the objective. This converter is designed to serve as the front end of a microinverter, boosting the PV panel output to adequate levels for inversion into AC power. The components selected for this routine will constrain the problem as well as the electrical operating points shown in Table XIII. The input voltage will vary based upon solar shading as well as the output power depending upon load demand. The switching frequency is a free variable of the optimization within it's given constraint boundary. The output voltage is fixed at 400V with a 5% ripple value.

Table XIII. Electrical Specifications

Input Voltage (V_g)	Output Power (P_{out})	Switching Frequency (f_s)	Output Voltage	Voltage Ripple
20-40V	100-200W	100-600kHz	400V	5%*

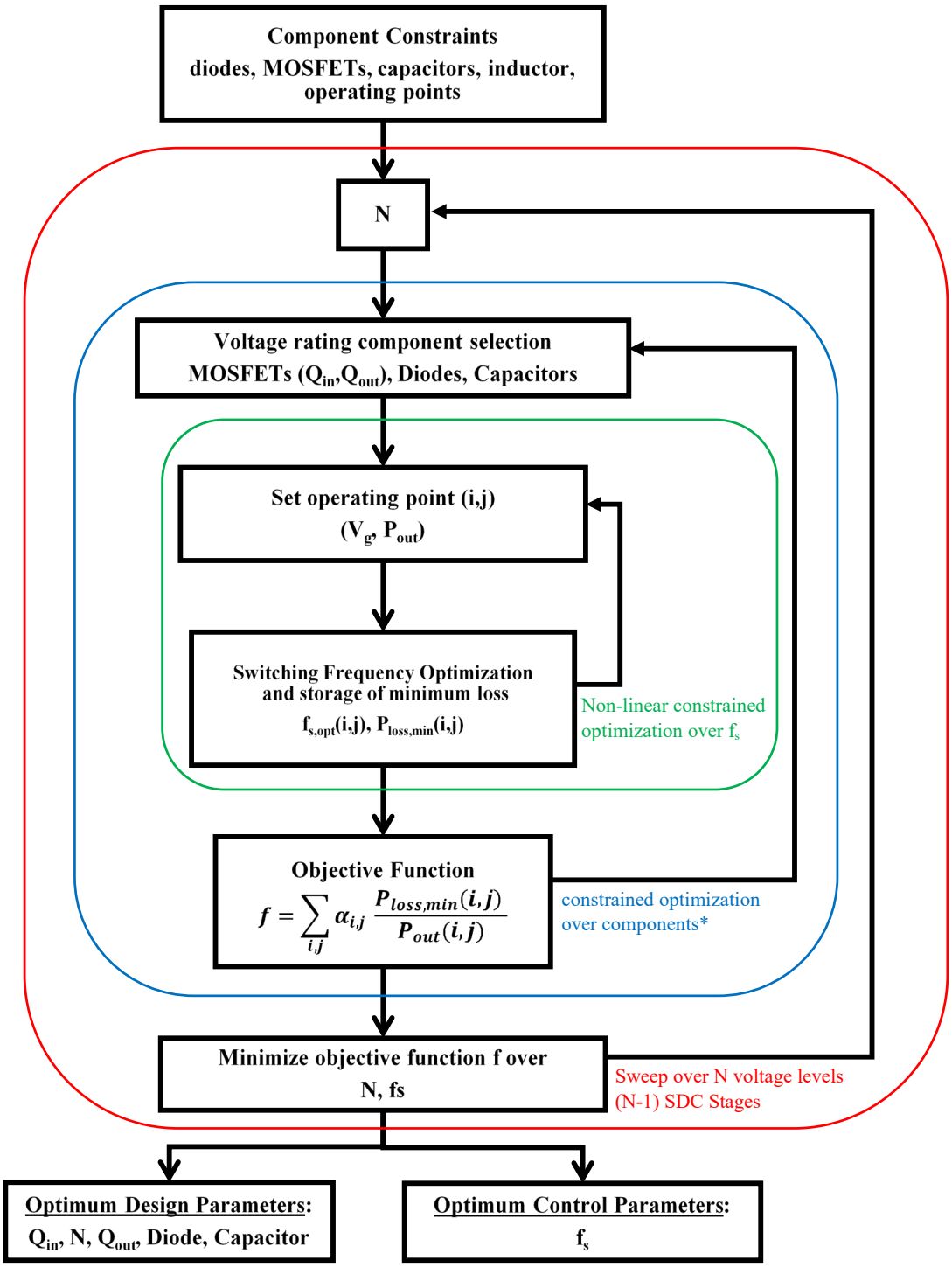


Figure 52. Multilevel Design Process

The outermost loop of the routine is for the number of converters levels (*N*) which equates to the number of flying capacitors (*N-1*). Given this value the estimated voltage ratings of the

components is used to select from the provided components. Lower ratings result in lower conduction resistance for semiconductors as described in 3.4.1. The next inner loop sets the operating point (V_g and P_{out}) and then sweeps to find which frequency results in the least amount of power loss. These values are then fed into the objective function that assigns a weight value (<1) to each operating point. The objective function is now a minimized compiling of the various operating points. The routine continues for all N values specified and will result in one design that is the most efficient. This design will then be built in LTSpice to verify operation and efficiency. Then it will be designed and built using Altium and tested for efficiency.

3.6 Solar Irradiance and Photovoltaic Output

The design process accounts for multiple converter operating points. This is because of the irregularity in voltage and power input into the converter due to solar irradiance varying. [80-85] The PV panel output voltage and power will vary linearly with changes in solar irradiance as shown in the blue curve of Figure 53. PV Panel Output Characteristic Curves [84]The voltage and power operating points will vary as described in Table XIV.

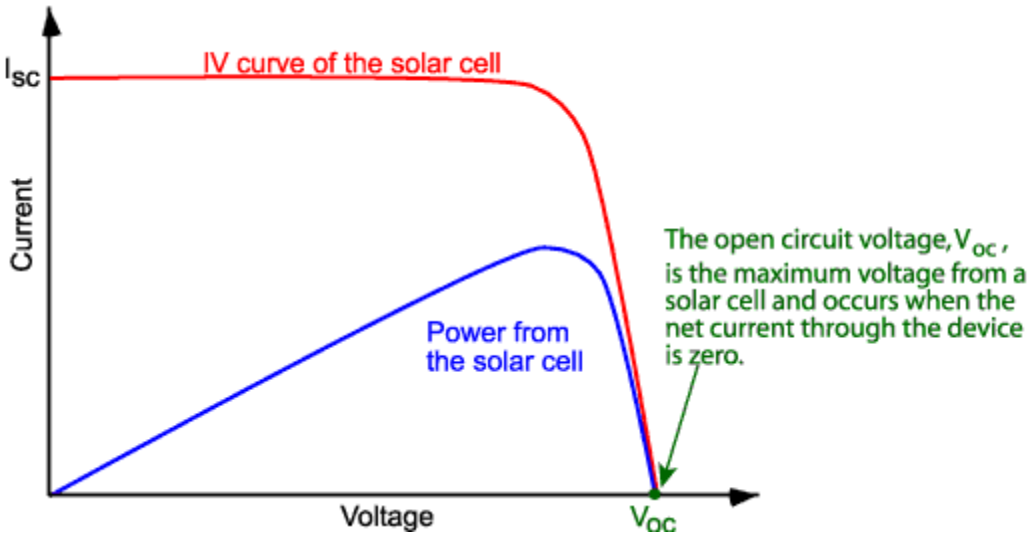


Figure 53. PV Panel Output Characteristic Curves [84]

Table XIV. Voltage and Power Input to Converter

Voltage [V]	40	20	13.33
Power [W]	200	100	66.67

3.7 Reliability Analysis

The 200W power supply will lead to significant losses in each converter analyzed and a reliability study was done to estimate component operating life for each converter. Power loss calculations are derived as an output of the design process previously described. This yields a specific power loss for each component at 200W operating point which is then used in conjunction with data sheet thermal resistances for the semiconductors and heat sinks to estimate steady-state operating temperature. These temperature values are then used in a reliability model to estimate component lifespan for the various converters.

3.7.1 Steady-State Junction Operating Temperatures

Values of 55C/W are listed in the data sheets for junction to ambient thermal resistance. The devices are very small require a heat sink to be attached. In this case a heat sink with thermal resistance of 2.5C/W is assumed for primary FET heat sinks. Secondary FETs assume 35C/W heat sinks and diodes 5C/W. The heat sinks are cooled with natural convection and not forced airflow. That is a combination of junction to sink and sink to ambient thermal resistances and is feasible using the provided calculator. [86-89] The thermal resistance circuit for this calculation is shown in Figure 54. This includes power loss as a current source and the thermal resistances related to the component's semiconductor junction to its case, the case to the heat sink, and the heat sink to the ambient temperature. An ambient temperature of 25C is assumed given the current testing location.

Using this thermal resistance and the junction to case thermal resistance the total can be calculated and the device temperature can be calculated for a given power loss for each component of a given converter.

Heat sink thermal resistances were chosen to ensure components would be in safe operating range (<150C). Values were not based off a specific heat sink but chosen within a rang that is possible for consumer available heat sinks for these package sizes. These are subject to change but will have little effect on these results. Simply put, the flyback components handle much more power and thus have more power loss that results in significantly more components heating. This leads to a higher failure rate relative to FCMFCs. FCMFC could possibly require no heat sinks due to the drastic reduction in component power loss. Not only as a result of the structures more efficient nature but also from the power handling that is shared across stages.

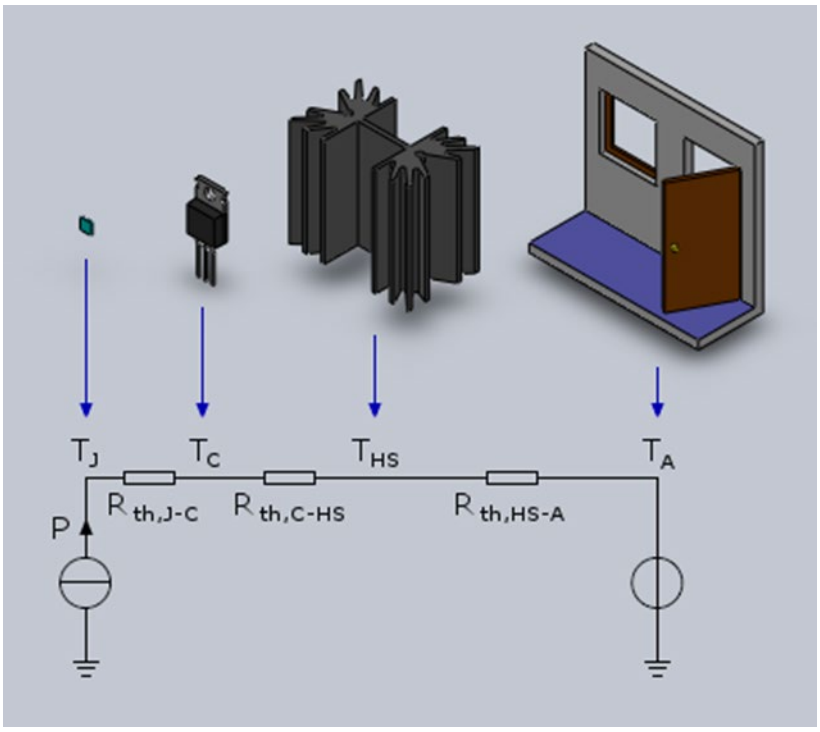


Figure 54. Thermal Resistance Circuit [86]

Table XV. Primary FET Steady-State Operating Junction Temperature

		Max Temp (C)	Max Power Dissipation(W) datasheet	Junction to case thermal resistance (C/W)	Power Dissipation (from MATLAB) (W)	Junction Temperature at SS
Part #	N	Tmax	PD	RJA	PQmin	Tuse
AOB29S50L	2	150		3.300	20.69	145.002
IPB407N30NATMA1	3	175	300	0.500	3.604	35.812
IXTA94N20X4	4	175	360	0.420	2.3435	31.84302
FDB075N15A	5	175	333	0.450	3.144	34.2748
FDB075N15A	6	175	333	0.450	3.0888	34.11196
FDB075N15A	7	175	370	0.450	2.767	33.16265

The flyback being nearly 10x for the primary FET gets near the peak temp of that device of 150C. All FCMFC converter primary FETs will operate under 36C. This is a major benefit because the FCMFC will thus not require as robust of a heat sink, reducing converter volume. Similar results are seen for the secondary power components as shown in

Table XVI. Secondary FETs Steady-State Operating Junction Temperature

		Max Temp (C)	Max Power Dissipation(W) datasheet	Junction to case thermal resistance (C/W)	Power Dissipation (from MATLAB) (W)		Junction Temperature at SS
Part #	N	Tmax	PD	RJA	Pqmin*	Pqmin/(N-1)	Tuse
-	2	-	-	-	-	-	-
IPB407N30NATMA1	3	175	300	0.500	2.2039	0.734633333	51.07948333
IXTA94N20X4	4	175	360	0.420	1.7704	0.4426	40.676892
FDB075N15A	5	175	333	0.450	1.9852	0.39704	39.075068
FDB075N15A	6	175	333	0.450	1.7131	0.285516667	35.12156583
AUIRLS4030	7	175	370	0.400	10.2627	1.4661	76.89994

Table XVII. Secondary Diodes Steady-State Operating Junction Temperature

		Max Temp (C)	Max Power Dissipation(W) datasheet	Junction to case thermal resistance (C/W)	Power Dissipation (from MATLAB) (W)	per diode (flyback has 1 others have N)	Junction Temperature at SS
Part #	N	Tmax	PD	RJA	Pdmin*	Pdmin/(N, N-1)	Tuse
VS-15EWX06FNTR-M3	2	-	-	1.800	13.3555	13.3555	115.8174
RFN10BM3SFHTL	3	175	300	6.00	7.5905	2.530166667	52.83183333
DSA15IM200UC-TRL	4	175	360	2.00	1.7947	0.448675	28.140725
SBR20M150D1Q-13	5	175	333	1.80	4.1246	0.82492	30.609456
V20PWM12HM3/I	6	175	-	2.00	2.9565	0.49275	28.44925
V20PW10-M3/I	7	150	-	2.00	2.8032	0.400457143	27.8032

3.7.2 Reliability Calculations

The Arrhenius High Temperature Operating Life (HTOL) model was used to calculate Failure Rate (λ), and Mean Time to Failure (MTTF) of the converter components. [90-92] This was done given the final optimal operating results of each converter and specific power loss of each component that is presented in later sections. The model is shown in Figure 55 and includes pre-determined testing data that is assumed for all converters components. This is a reasonable assumption given that all components are silicon and in the same general price, quality, and application range.

Using the MicroSemi MicroNote 1002 for reliability calculations the relative reliability between converter components is calculated for the highest 200W power conversion. Using the proposed loss model to estimate component power loss and then calculating the thermal resistance of the component to the ambient from the data sheet the device steady-state operating temperature

can be predicted. This operating temperature is the "T_{use}" for the reliability calculation which is based on the Arrhenius High Temperature Operating Life (HTOL) model. This estimates the standard reliability values Failure Rate (λ), Failures in Time (FIT) and Mean Time to Failure (MTTF). The base values of the equation were kept constant for all devices such as: activation energy, chi-squared, activation energy, etc. This is a fair assumption because the components are all Si and similar in cost and function. The calculated failure rate is shown in equation (3.20).

$$\lambda_{hour} = \frac{\chi^2(\alpha,\nu)}{2 * D * H * A_f} \tag{3.20}$$

Microsemi

Reliability Calculator

MicroNote™ 1004

by Paul Ellerman,
Director of Reliability
pellerman@microsemi.com

Reliability Calculator using Arrhenius HTOL Model

INPUT DATA: Do not use screening data for reliability calculations.

Number of Failures (r)	Number of Devices Tested (D)	Test Hours per Device (H)
0	220	1000
1	450	380

Test Temperature (°C)	Use Temperature (°C)	Established Activation Energy (Ea)
125	55	0.7

Chi-Square (X^2) @ 60% Confidence Level (α)	Acceleration Factor (Af)	Total Number of Failures (r)	Total Number of Device Hours (DH)	Equivalent Device Hours (EDH)
4.045	77.94	1	391,000	30,474,923

Failure Rate (λ_{hour})	6.64E-08
FIT : Failures in Time **(λ per billion hours)**	66

$MTTF_{hours}$: Mean Time to Failure **(θ in hours)**	15,069,338
$MTTF_{years}$: Mean Time to Failure **(θ in years)**	1,720

Indicates Data Entry Point

Indicates Variable Value

Parameters & Constants

r = number of failures or rejects
D = Number of Devices Tested
H = Test Hours per Device
T (Calculation Temperature in Kelvin) = Celsius + 273°
T_{test} = Test Temperature (HTRB or other burn-in temperature)
T_{use} = Use Temperature (standardized at 55°C or 328°K)
E_a = Activation Energy (eV)
$X^2/2$ (Chi-Squared/2) is the probability estimation for number of failures at α and ν)
α (alpha) = Confidence Level for X^2 distribution; reliability calculations use **α = 60% or .60**
ν (nu) = Degrees of Freedom for X^2 distribution; reliability calculations use **ν = 2r + 2**
A_f = Acceleration Factor from the Arrhenius equation
k (Boltzmann's Constant) = **8.617 x 10e-5 eV/°K**
DH (Device Hours) = **D x H**
EDH (Equivalent Device Hours) = **D x H x A_f**
λ_{hour} = Failure Rate per hour
FIT (λ_{FIT}) = Failures in Time = Failure Rate per billion hours
MTTF = Mean Time to Failure

Equations

$$A_f = e^{E_a/k\left(1/T_{use} - 1/T_{test}\right)} \qquad FIT = \lambda_{FIT} = \lambda_{hours} \times 10^9$$

$$\lambda_{hour} = \frac{X^2(\alpha,\nu)}{2 \times D \times H \times A_f} = \frac{X^2(\alpha,\nu)}{2 \times EDH}$$

$$MTTF_{hours} = 1/\lambda_{hours} \qquad MTTF_{years} = 1/\left(\lambda_{hours} \times 24 \times 365\right)$$

Figure 55. Reliability Calculator Model MicroSemi []

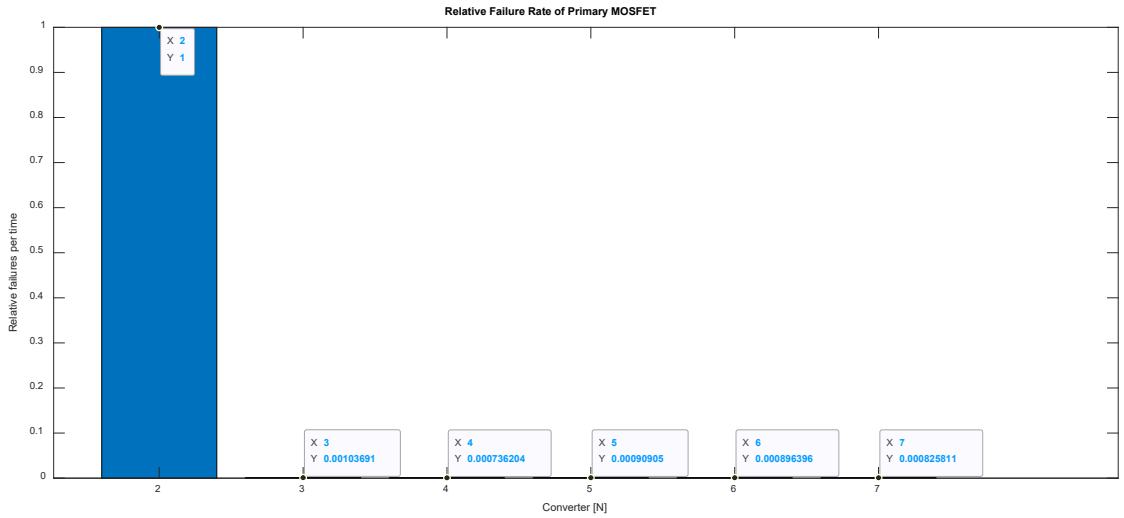


Figure 56. Relative Failure Rate of Primary MOSFETs

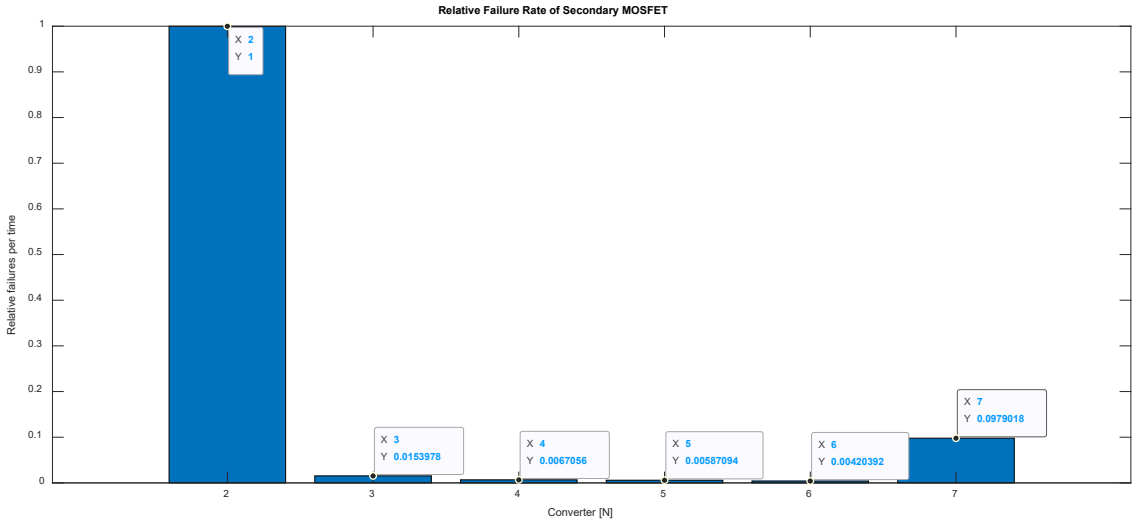


Figure 57. Relative Failure Rate of Secondary MOSFETs

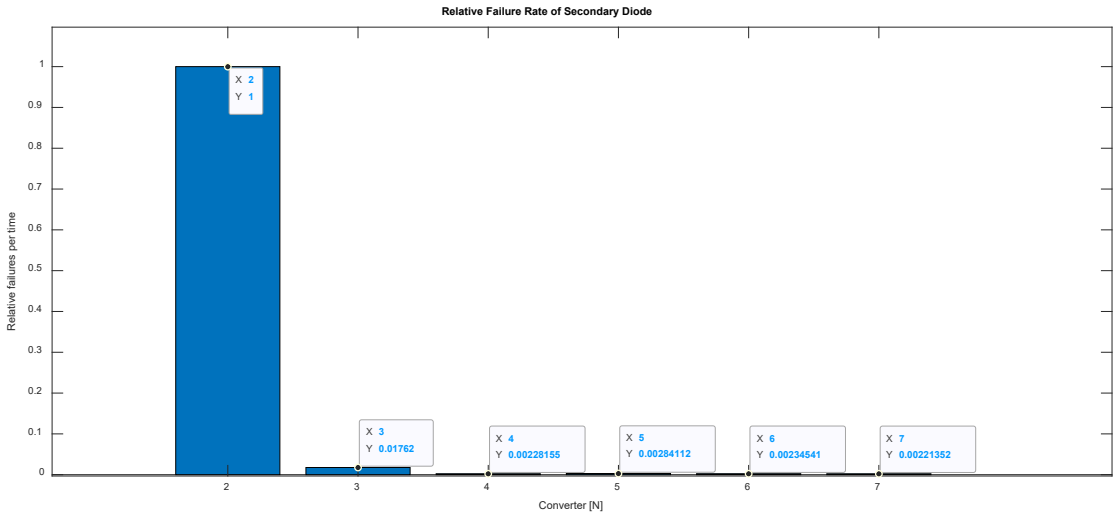


Figure 58. Relative Failure Rate of Secondary Diodes

Figure 56, Figure 57, and Figure 58 show the relative failure rate of converter components normalized to that of the flyback converters failure rate. The component failure rate of the primary MOSFET is reduce to sub 1% values when utilizing any of the FCMFCs. Similarly, for the secondary FETs and diodes, the failure rates are less for the FCMFC converters. This is in line with the power loss and temperature data shown in Table XV, Table XVI, and Table XVII. The FCMFC structure distributes power utilization across multiple stages, allowing each individual component to operate at a lower steady-state temperature and effectively have a longer operating life.

3.8 Component Selection

Converter levels were limited to N = 2-7. This includes the flyback converter for comparison to the new FCMFC topology. Given the supply chain constraints brought about by the

COVID19 pandemic, the component selection process was limited by availability. Semiconductor components were chosen with a 65% voltage derating factor and 55% current derating factor. Table XVIII and Table XIX show the components ratings required for each of the considered converters in this study. These tables were calculated using the steady-state operation equations provided in Directive I and the operating specifications in Table XIII.

MOSFET package size was constrained to a TO-263 surface mount package and diodes were constrained to a TO-252 surface mount package. Higher N level devices require lower blocking voltages which also opens up for higher available drain currents leading to even lower on resistances. This in turn will have a significant efficiency benefit for FCMFC over the flyback converter. In addition when discussing the added components this does not add significant loss because of the conduction time for each component. For example, the flyback suffers the worst diode loss (~40%) even though it only has 1 diode. This is because of the significant voltage that diode must block. The FCMFC converters do have more diodes but each diode conducts for a fraction of time less than the flyback converter and thus doesn't double or triple diode losses. This will have the added benefit of reliability because FCMFC components are under less stress and power loss, thus operating at lower temperatures. Making them last longer than a flyback converter.

Table XVIII. Primary FET

N	Vin	iQ	iQ rating	Vblock Q	Qmin rating
2	40	13A	23A	280	431
3	40	13A	23A	160	246
4	40	13A	23A	120	185
5	40	13A	23A	100	154
6	40	13A	23A	88	135
7	40	13A	23A	80	123

Table XIX. Secondary FETs and Diodes

N	Vout	Iout	"Rout"	Pmax	Vblock	Vmin rating	Isec peak	Imin Rating
2	400	0.5	800	200	400	615	7.8	14.2
3	400	0.5	800	200	200	308	7.8	14
4	400	0.5	800	200	133	205	7.8	14
5	400	0.5	800	200	100	154	7.8	14
6	400	0.5	800	200	80	123	7.8	14
7	400	0.5	800	200	67	103	7.8	14

This data was then used to search Digi-Key and Mouser online catalogues to find MOSFETs with the lowest on resistance and diodes with the lowest forward power dissipation. The components chosen are shown for primary FETs, secondary FETs, and secondary diodes are shown in Table XX, Table XXI, and Table XXII.

Table XX. Primary FET

Required Ratings			Digi-Key	Component Ratings		
N	iQ rating	Q rating	Part #	Rmax [mΩ]	Volts	Amps
2	20-30A	431	AOB29S50L	150.0	500	29
3	20-30A	246	IPB407N30NATMA1	40.7	300	44
4	20-30A	185	IXTA94N20X4	10.6	200	94
5	20-30A	154	FDB075N15A	7.5	150	130
6	20-30A	135	FDB075N15A	7.5	150	130
7	20-30A	123	FDB075N15A	7.5	150	130

Table XXI. Secondary FET

Required Ratings			Digi-Key	Component Ratings		
N	qd rating	iq Rating	Part #	Rmax [mΩ]	Volts	Amps
2	615	14-20A	-	-	-	-
3	308	14-20A	IPB407N30NATMA1	40.7	300	44
4	205	14-20A	IXTA94N20X4	10.6	200	94
5	154	14-20A	FDB075N15A	7.5	150	130
6	123	14-20A	FDB075N15A	7.5	150	130
7	103	14-20A	AUIRLS4030	4.3	100	180

Table XXII. Secondary Diode

Required Ratings			Digi-Key	Data
N	qd rating	iq Rating	Part #	Ploss curve
2	615.3846	14-20A	VS-15EWX06FNTR-M3	yes
3	307.6923	14-20A	RFN10BM3SFHTL	yes
4	204.6154	14-20A	DSA15IM200UC-TRL	yes
5	153.8462	14-20A	SBR20M150D1Q-13	yes
6	123.0769	14-20A	V20PWM12HM3/I	yes
7	103.0769	14-20A	V20PW10-M3/I	yes

3.8.1 Diode Forward Power Dissipation Curves

All diodes selected have forward dissipation curves that are interpolated using Microsoft Excel as shown in Figure 59 for the N4 converter diodes. This data is used with the curve fit function that produces a second order equation. This equation is then used within the MatLab script to interpolate the diode forward dissipation loss for all given operating points.

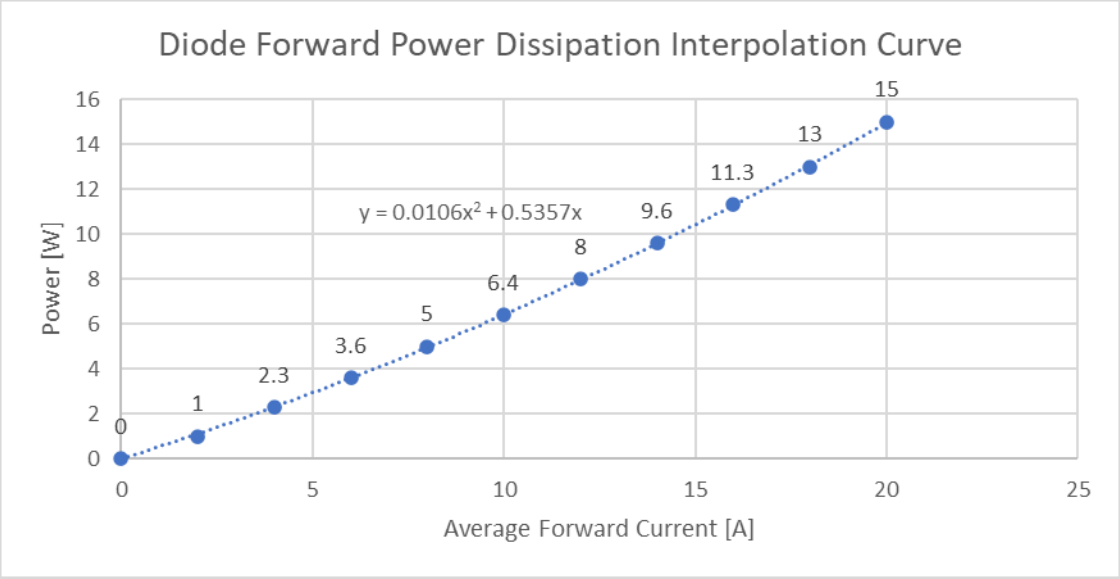


Figure 59. N4 Diode Forward Dissipation Interpolation Curve

3.9 Cost Analysis

The cost for each converter is compiled below based on the advertised Digi-Key prices at the time of selection. This cost in includes all semiconductor components and auxiliary circuitry such as isolated power chips and gate drivers. As expected, the FCMFC converters are more expensive than the traditional flyback (N2) converter by two or three times. The component selection was limited to availability and certain high demand components like the MOSFETs for the N4 converter were significantly more expensive than all the others. This is considering the COVID19 supply shortages. The per component prices are listed in Table XXIII for reference.

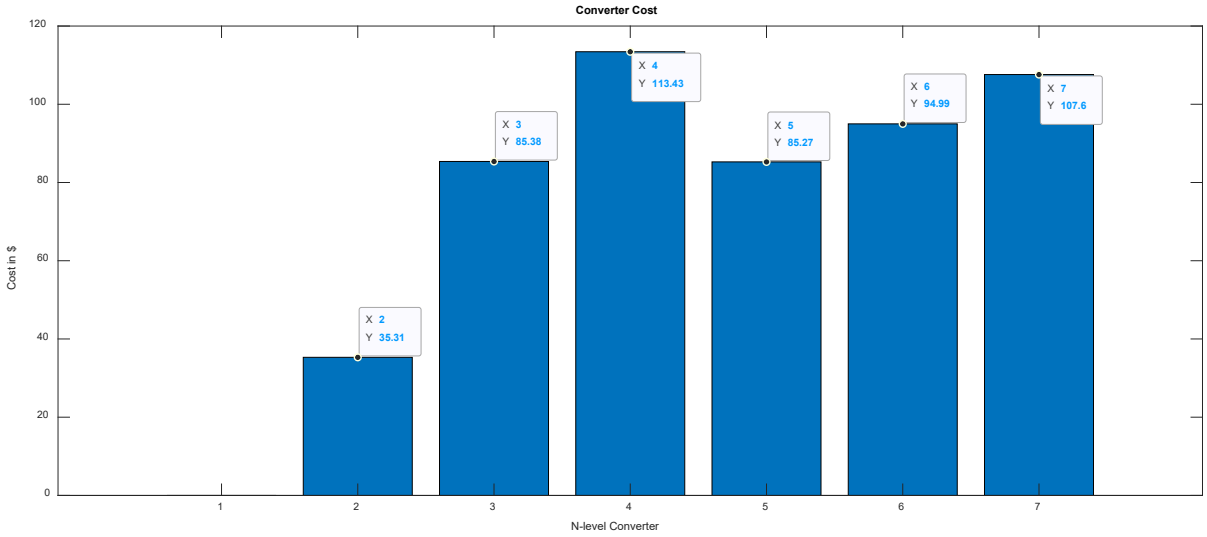


Figure 60. Converter Cost Comparison

Table XXIII. Component Prices [$]

N-level	2	3	4	5	6	7
Primary FET	4.83	10.02	12.92	4.76	4.76	4.76
Secondary FETs	0	10.02	12.92	4.76	4.76	5.95
Diodes	1.36	1.01	1.52	1.07	1.07	1.01

3.10 MatLab Script Design

The optimization routine outlines in Figure 52 was programmed in MatLab using 540 lines of code. This code also includes reliability and cost analysis discussed in later sections. The code is included a .m file with this dissertation document. The electrical operating specifications are set as per Table XIII. Next all the necessary data for components is set using arrays for each operating variable. This includes the transformers, capacitors, and the various MOSFETs and diodes that can be used given each converter's operating limits.

3.11 Design Process Results

3.11.1 Power Loss Comparison

The results of the MATLAB design process are provided in this section. Point plots are shown for the comparison of each converters power loss at the three operating points. Figure 61, Figure 62, and Figure 63 show the 200W, 100W, and 66.67W operating points respectively. They also have each data point selected and displaying the power loss at that point for that particular converter, N2-N7. Figure 64 is a combination of the previous three figures for a comparison of all operating points for all converters. The flyback converter, N2, has the highest losses associated with all three operating points while the N4 FCMFC is the lowest. The N6 converter has a similar loss profile to N4 but due to the added complexity of two additional switching stages this converter is not optimal. Notice that going from N6 to N7 the power losses begin to increase partly because of the added stage but also due to the diminishing return of the voltage distribution benefit associated with multilevel converters. For this design criteria and available components, the optimal converter is an N4.

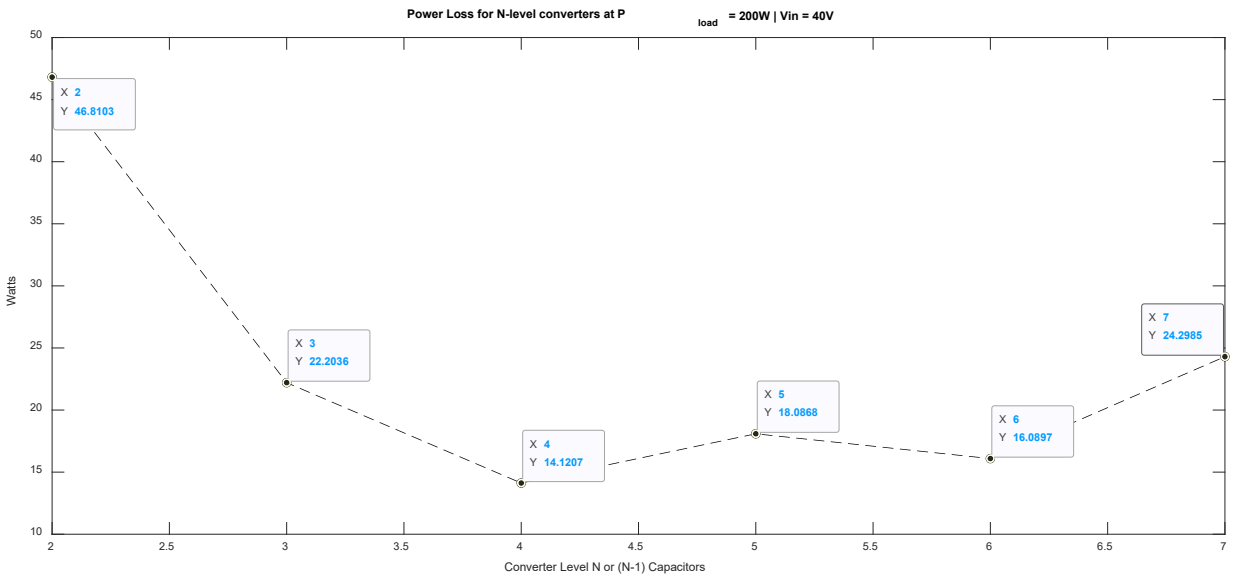


Figure 61. Power Loss Curve 200W 40Vin

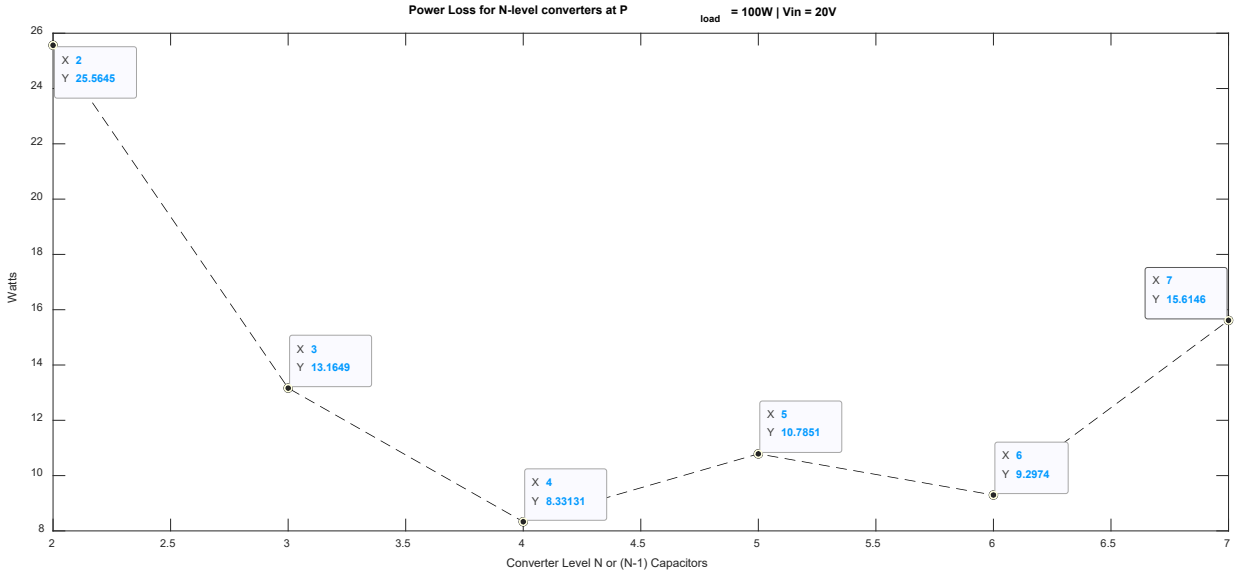


Figure 62. Power Loss Curve 100W 20Vin

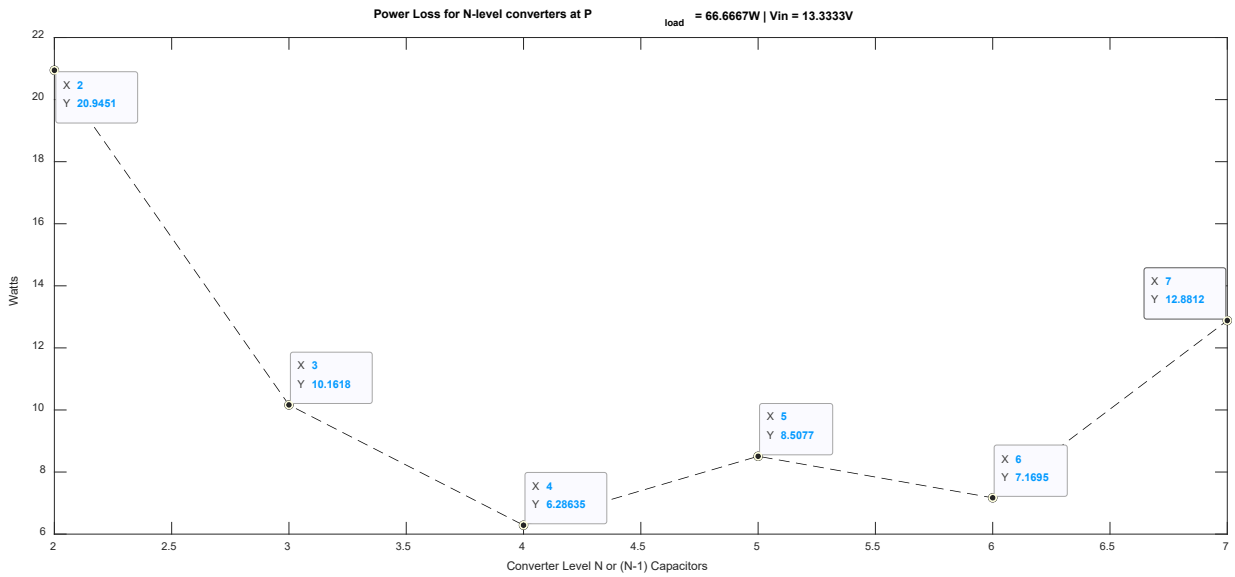


Figure 63. Power Loss Curve 66.67W 13.33Vin

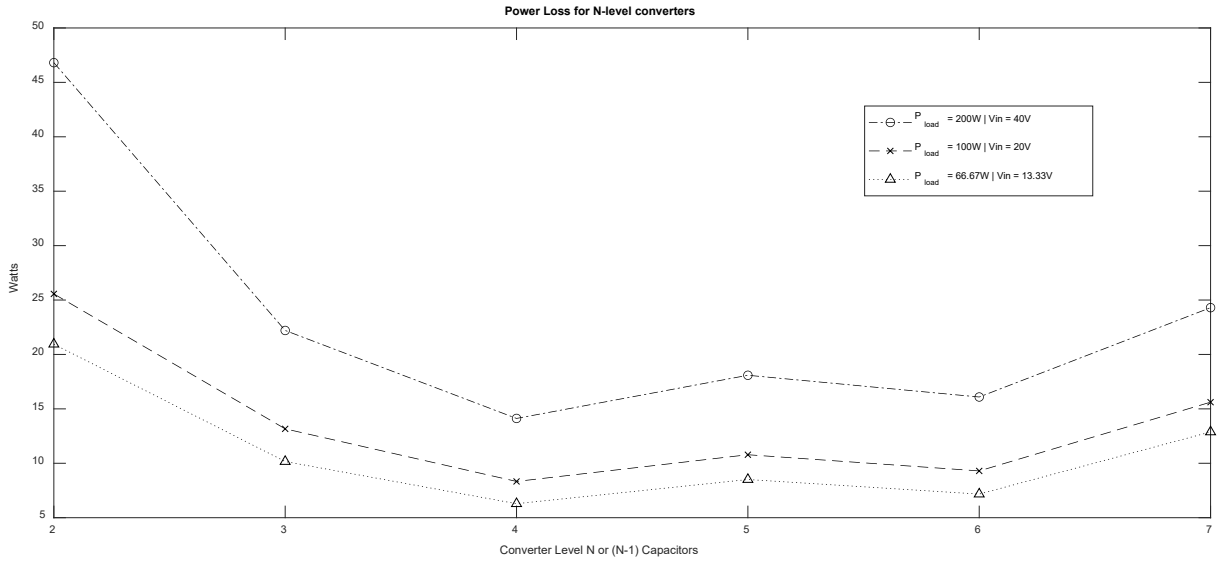


Figure 64. Power Loss Curves at All Operating Points

3.11.2 Power Loss Breakdown Comparison

It is important to understand the power loss mechanisms for these converters and how they influence the optimal design. For each point in Figure 64 the associated power loss breakdown is shown in a pie chart in this section. Six different converters at three different operating points leads to 18 separate loss breakdowns, Figure 65-Figure 82. These charts will help explain the trends seen in the power loss curve shown in Figure 64. The charts are interleaved so that each operating point can be compared easily amongst the converters. The pie charts are a percentage breakdown of the power loss for a particular converter at a particular operating point; with this it is important to understand the percent values in each chart are portions of a different number each time. Trending in this case will be discussed accordingly. For example, when comparing Figure 65 to Figure 66, the diode loss percentage increases from 29% to 34%, but as a portion of a smaller total power loss. This means that diode losses for the N2 make up a smaller portion of total loss but when compared to the N3 the diode losses are much higher. Both the portion of a loss component and its absolute power loss are important in this section when describing the trends of the design process results. Also note that the flyback converter does not have the secondary FETs, gate drivers, and isolated power associated with the FCMFC converters. The optimal designs are chosen to have the lowest total loss which means that each individual component loss is not minimized in every case which can have an effect on trends.

3.11.2.1 First Operating Point 200W 40Vin (N2-N7)

Efficiencies for this power point start at 81% for the N2 flyback and increase up to 93.4% for N4 and then trend down slowly to 89% for the N7. Diode losses are reduced from N2 to N7 even with the addition of multiple diodes for the multilevel converters. The primary reason for this is the reduction in reverse recovery loss due to lower reverse voltage on the diodes. Capacitor ESR is insignificant (<1%) and consistent for all converters. The input primary FET power loss is significantly reduced for FCMFCs, going from 44% for N2 down to 11% for N7, indicating the reduction in voltage stress on that component. The secondary FETs result in a power loss that is increasing for higher level converters. Starting at 10% for the N3 converter and increasing to 43% of the loss for the N7 converter, the secondary FET loss increases because of the increase in FETs present that must handle the secondary current. The diminishing return effect is seen in this instance. As the converter level increases the voltage distribution benefit is counteracted by the sheer increase in power processing components and conductive loss through them, and thus the most efficient converter is not the highest level considered. Core loss ranges between 10-20% of the total loss for all converters. Core loss is driven by the peak flux density and switching frequency. FCMFC converters have lower duty cycles and result in lower peak flux but have varying minimum switching frequencies and thus no trend occurs across converters for core loss in percent terms. In absolute terms the FCMFCs experience lower core loss which will be discuss in the coming sections. Primary FET gate drive loss is similar for all converters as expected. Secondary FET gate drive increases for higher level converters that have more FETs which is expected but also not a significant loss mechanism. The multilevel converters have isolated power components that have a similar trend due to the current they supply to the gate drivers. Winding loss is below 1% for all converters and should be similar because of the same average current

processed by the transformer. Zener leakage is a significant loss component shown to vary amongst the converters in percent terms. The Zener snubber circuit protection level is different for each converter based on the FET protection required due to transformer reflection voltage. The snubbers required from N2-N7 are 336V, 192V, 144V, 120V, and 105.6V respectively. A higher clamping voltage means less current let-through and thus lower power loss, but the voltage reflected from the secondary of the transformer is also critical and in the case of FCMFCs that voltage is reduced two, three, four, etc. times for each level added. This allows for ample protection of the lower rated FET in the FCMFC converters without any increase in snubber power loss. In fact, the FCMFCs will experience a decrease in snubber power loss as a result of this.

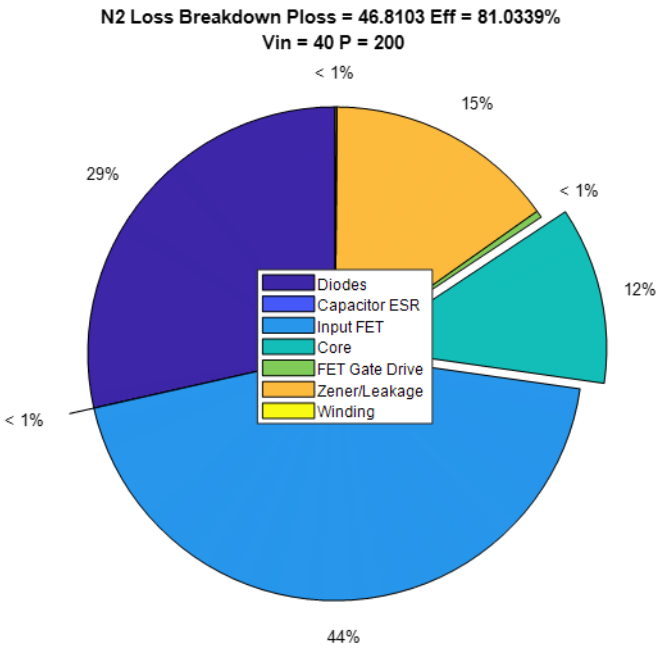


Figure 65. N2 Loss Breakdown 200W 40Vin

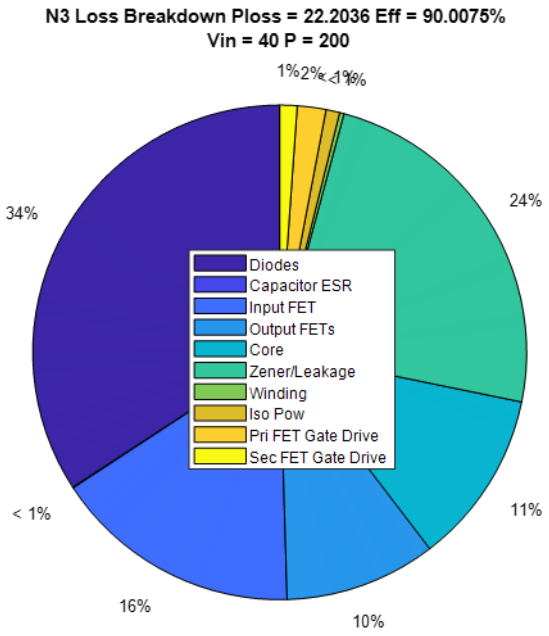


Figure 66. N3 Loss Breakdown 200W 40Vin

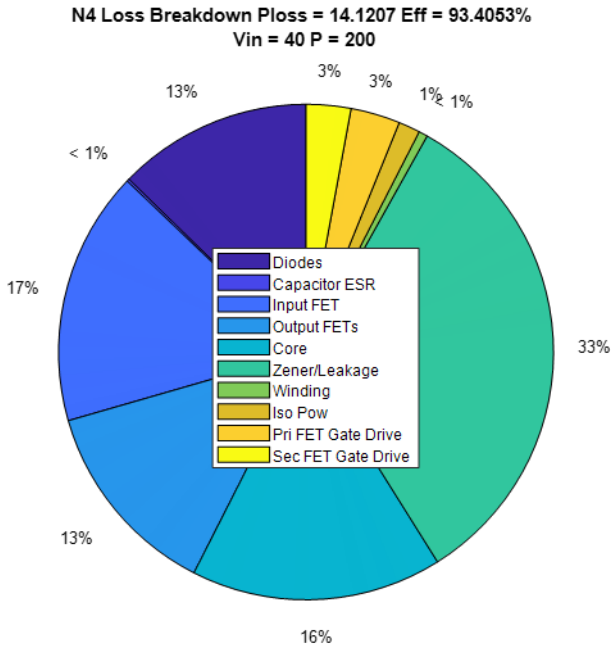


Figure 67. N4 Loss Breakdown 200W 40Vin

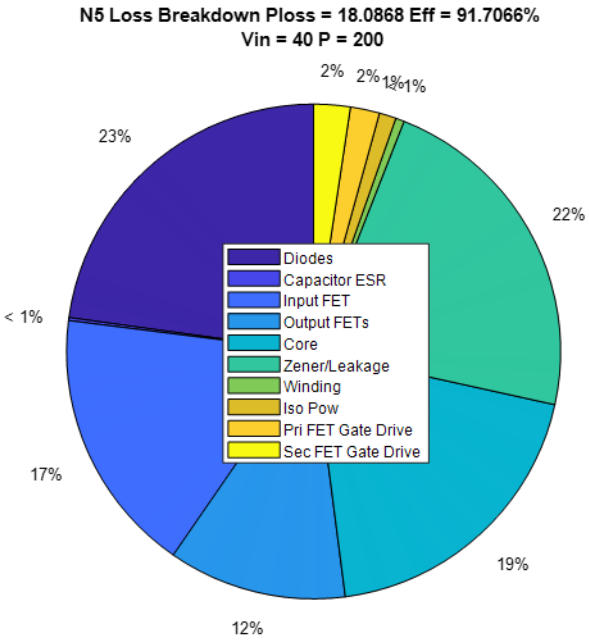


Figure 68. N5 Loss Breakdown 200W 40Vin

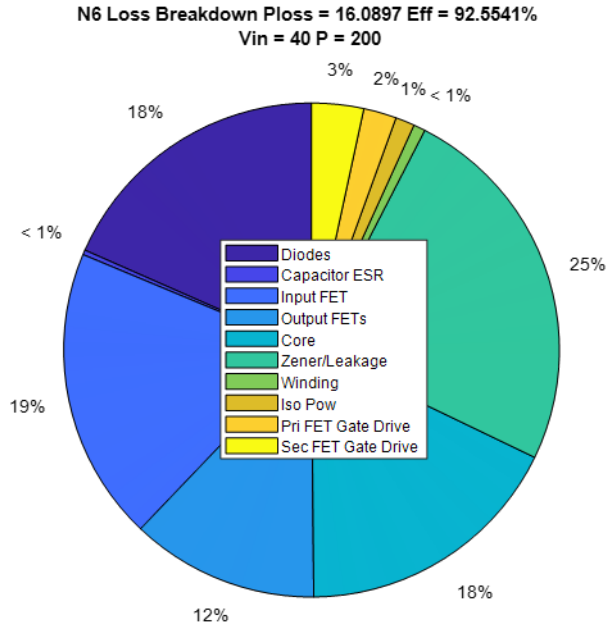


Figure 69. N6 Loss Breakdown 200W 40Vin

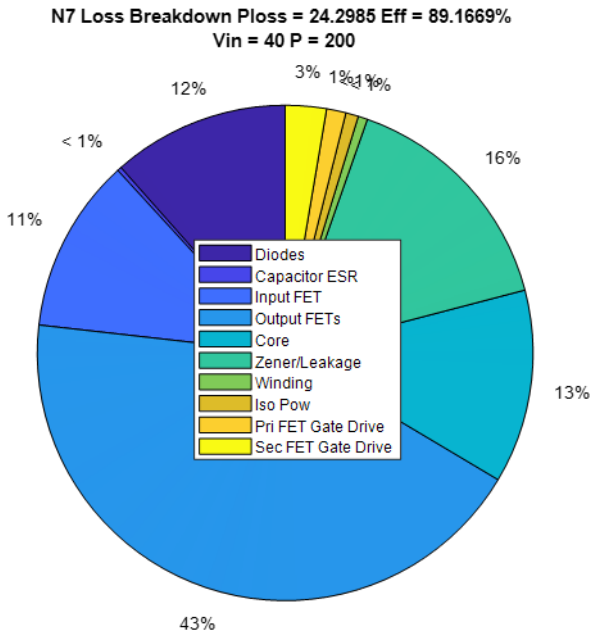


Figure 70. N7 Loss Breakdown 200W 40Vin

3.11.2.2 Second Operating point 100W 20Vin (N2-N7)

For the second operating point the power processing is lower, but the voltage gain is higher. The same trends are seen for the 200W 40Vin operating point as for this operating point of 100W 20Vin shown in Figure 71 to Figure 76. Because the power level is lower the total power losses are lower and the smaller fixed power losses (gate drive and isolated power) start to make up a larger percent of the total power loss.

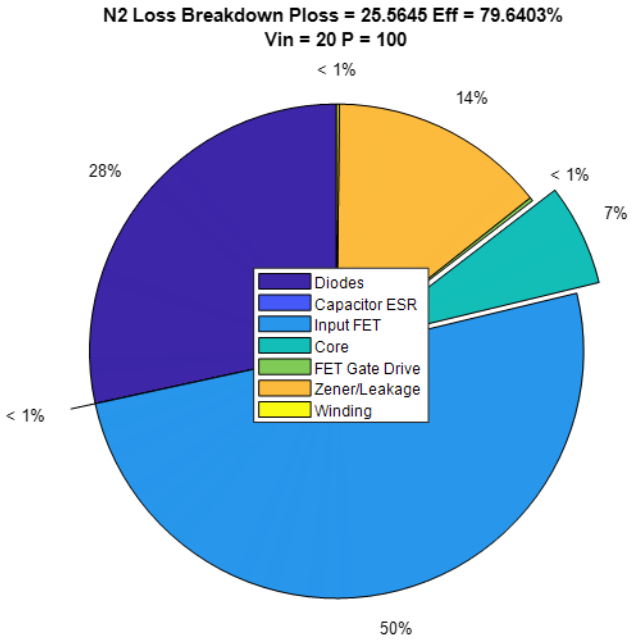


Figure 71. N2 Loss Breakdown 100W 20Vin

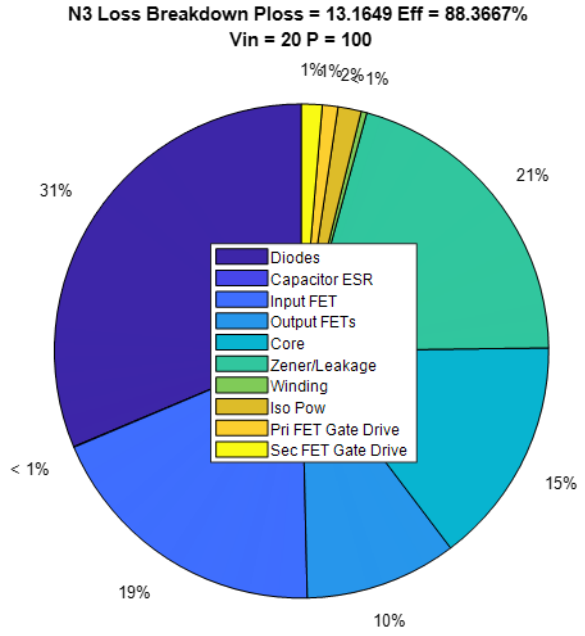


Figure 72. N3 Loss Breakdown 100W 20Vin

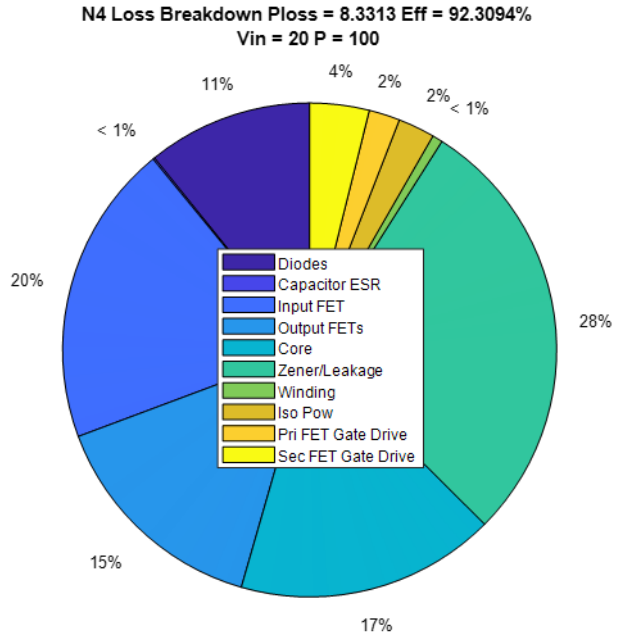


Figure 73. N4 Loss Breakdown 100W 20Vin

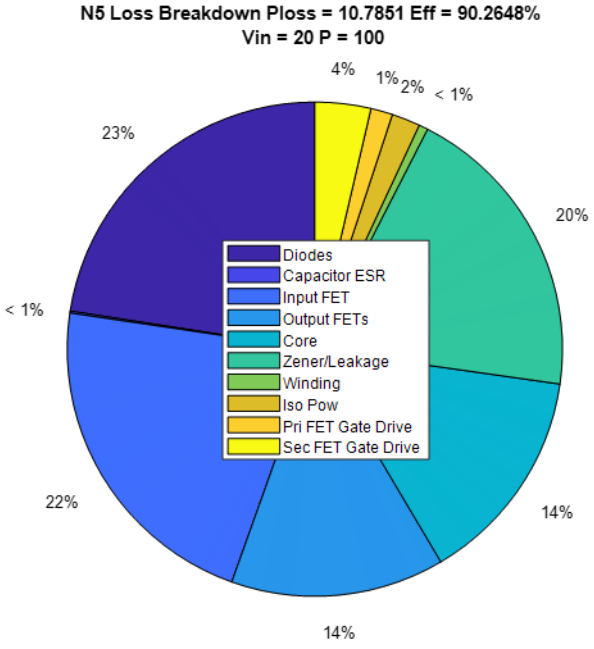


Figure 74. N5 Loss Breakdown 100W 20Vin

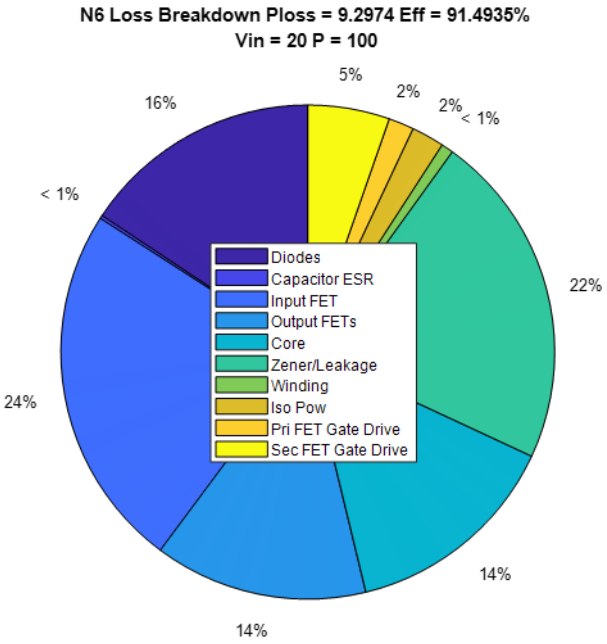


Figure 75. N6 Loss Breakdown 100W 20Vin

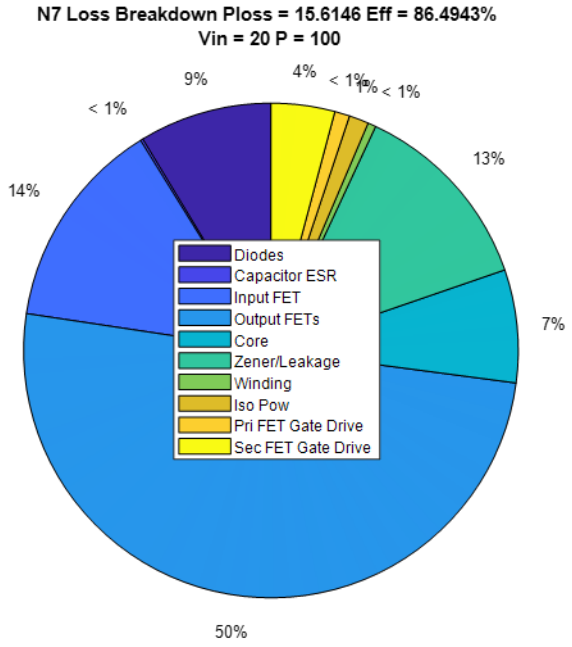


Figure 76. N7 Loss Breakdown 100W 20Vin

3.11.2.3 Third Operating point 66.67W 13.33Vin (N2-N7)

For the third operating point the power processing is even lower, and the voltage gain is even higher. The same trends are seen for the 200W 40Vin operating point as for this operating point of 66.67W 13.33Vin shown in Figure 77 to Figure 82. Because the power level is even lower the total power losses are lower and the smaller fixed power losses (gate drive and isolated power) start to make up an even larger percent of the total power loss. Notice also that the diode loss percentages are falling as they are primarily a function of current.

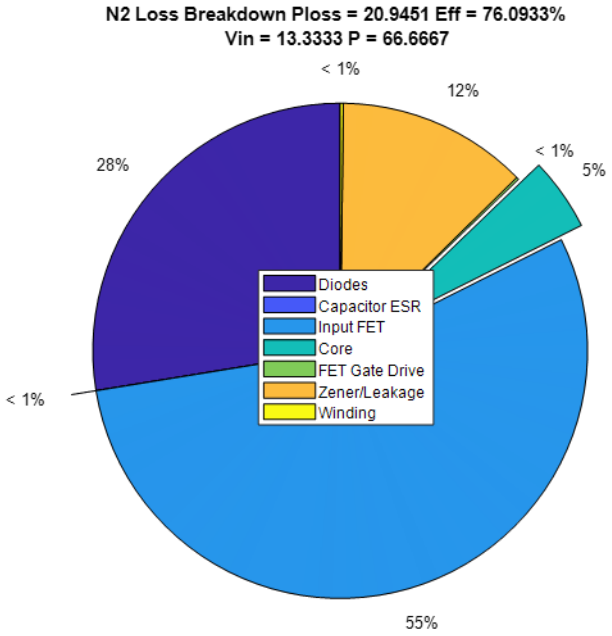


Figure 77. N2 Loss Breakdown 66.67W 13.33Vin

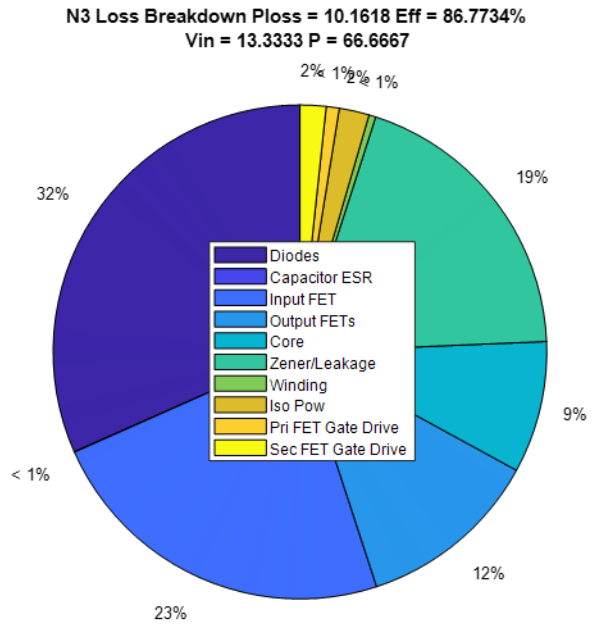


Figure 78. N3 Loss Breakdown 66.67W 13.33Vin

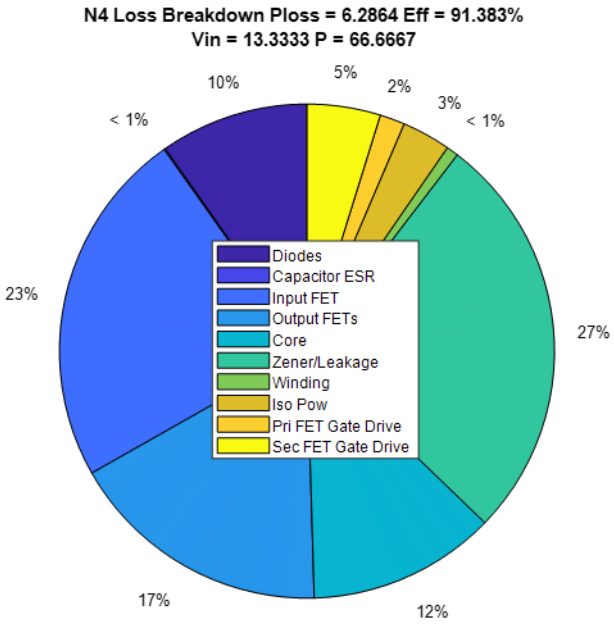


Figure 79. N4 Loss Breakdown 66.67W 13.33Vin

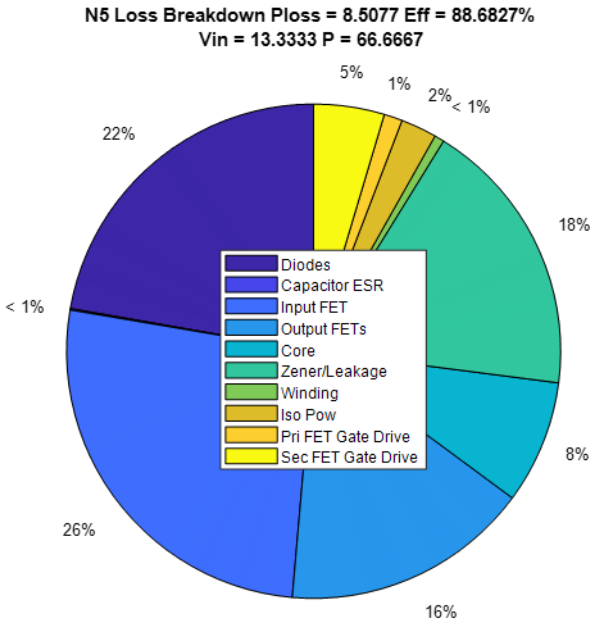


Figure 80. N5 Loss Breakdown 66.67W 13.33Vin

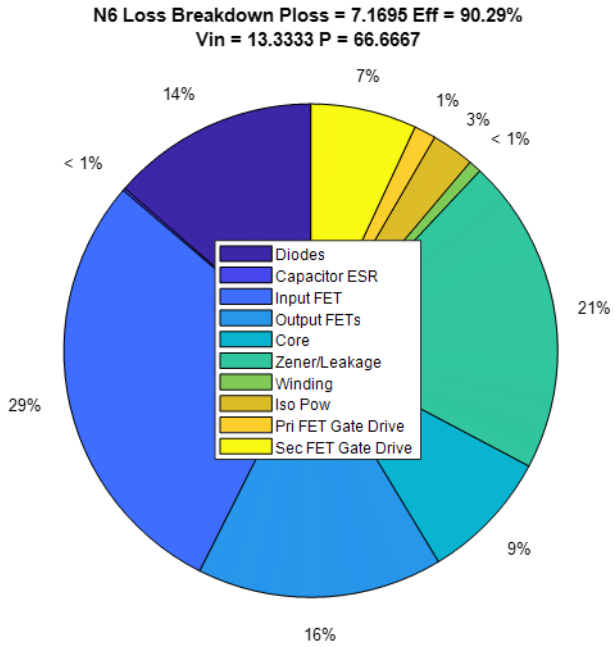


Figure 81. N6 Loss Breakdown 66.67W 13.33Vin

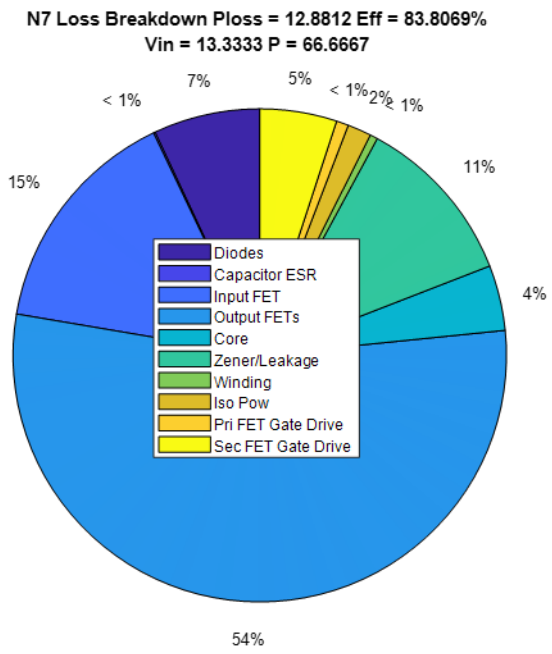


Figure 82. N7 Loss Breakdown 66.67W 13.33Vin

3.11.3 Power Loss Comparison in Absolute Terms

This section summarizes the power loss mechanisms for the six converters in three separate tables corresponding to the three operating points. Trends are important here to compare the multilevel structures to the flyback (N2). In Table XXIV and highlighted in yellow is the diode power loss for the flyback and the lowest level FCMFC. It would be expected that a converter with more diodes would suffer from a higher diode loss. In the case of FCMFC the power is distributed so that more diodes can operate in an overall more efficient manner and thus cut the power loss almost in half. The trend continues for higher level FCMFCs have even lower losses.

Highlighted red is the primary FET power loss that is significantly reduced from 20.69W to 3.60W with the addition of a single flying capacitor stage. This is a reduction of 83% and did not require complex auxiliary sensing and control circuit that is required for zero-voltage switching

schemes. Highlighted in blue is the loss for the secondary output FETs that are significant but do not add more loss than what is saved in the diodes and input FET as previously discussed, justifying their addition. Core loss in green is shown to be reduced in all FCMFC converters compared to the flyback converter. Similar trends are seen in

Table XXV and Table XXVI for the 100W and 66.67W operating points respectively.

Table XXIV. First Operating Point 200W 40Vin Abolute Loss Value Comparison [Watts]

Converter	Diodes	Cap ESR	Input FET	Output FETs	Core Loss	Zener Snubber	Winding Loss	Isolated Power	Pri FET GD	Sec FET GD	Total [W]
N2	13.36	0.004	**20.69**	-	5.43	7.06	0.05	-	0.22	-	46.81
N3	7.59	0.012	**3.60**	2.20	2.53	5.34	0.06	0.20	0.42	0.25	22.20
N4	1.79	0.023	2.34	1.84	2.32	4.65	0.08	0.20	0.46	0.41	14.11
N5	4.12	0.036	3.14	2.11	3.53	4.07	0.10	0.20	0.35	0.43	18.09
N6	2.96	0.050	3.09	1.97	2.85	3.96	0.12	0.20	0.35	0.54	16.09
N7	2.80	0.067	2.77	10.5	3.07	3.77	0.15	0.20	0.31	0.65	24.23

Table XXV. Second Operating Point 100W 20Vin Abolute Loss Value Comparison [Watts]

Converter	Diodes	Cap ESR	Input FET	Output FETs	Core Loss	Zener Snubber	Winding Loss	Isolated Power	Pri FET GD	Sec FET GD	Total [W]
N2	7.26	0.002	12.88	-	1.70	3.62	0.04	-	0.05	-	25.55
N3	4.12	0.005	2.50	1.31	1.96	2.70	0.05	0.20	0.13	0.18	13.15
N4	0.90	0.010	1.64	1.24	1.42	2.37	0.06	0.20	0.17	0.32	8.33
N5	2.43	0.014	2.36	1.51	1.54	2.13	0.06	0.20	0.15	0.39	10.78
N6	1.46	0.020	2.22	1.30	1.33	2.04	0.07	0.20	0.15	0.50	9.29
N7	1.36	0.025	2.15	7.85	1.15	1.99	0.08	0.20	0.15	0.65	15.60

Table XXVI. Third Operating point 66.67W 13.33Vin Abolute Loss Value Comparison [Watts]

Converter	Diodes	Cap ESR	Input FET	Output FETs	Core Loss	Zener Snubber	Winding Loss	Isolated Power	Pri FET GD	Sec FET GD	Total [W]
N2	5.77	0.001	11.5	-	1.00	2.61	0.04	-	0.04	-	20.96
N3	3.21	0.003	2.38	1.22	0.87	1.97	0.05	0.20	0.09	0.17	10.16
N4	0.61	0.006	1.47	1.08	0.77	1.69	0.05	0.20	0.10	0.30	6.28
N5	1.89	0.009	2.24	1.38	0.69	1.55	0.05	0.20	0.10	0.39	8.50
N6	0.97	0.012	2.07	1.15	0.62	1.49	0.06	0.20	0.10	0.50	7.17
N7	0.90	0.015	1.96	7.00	0.55	1.44	0.07	0.20	0.10	0.65	12.89

3.11.4 Power Loss Breakdown Bar Graphs

The graphs in this section are another are another way to visualize the data and trends that were previously discussed using line plots and pie charts. Each of the converters is shown for the ten different loss components with a graph for each operating point. The major loss component of the flyback converter is the primary input FET in Figure 83, Figure 84, and Figure 85 for all operating points. This component is reduced significantly for all FCMFCs for all three operating points. The Zener snubber clamp and diodes tend to be the largest loss component for FCMFCs.

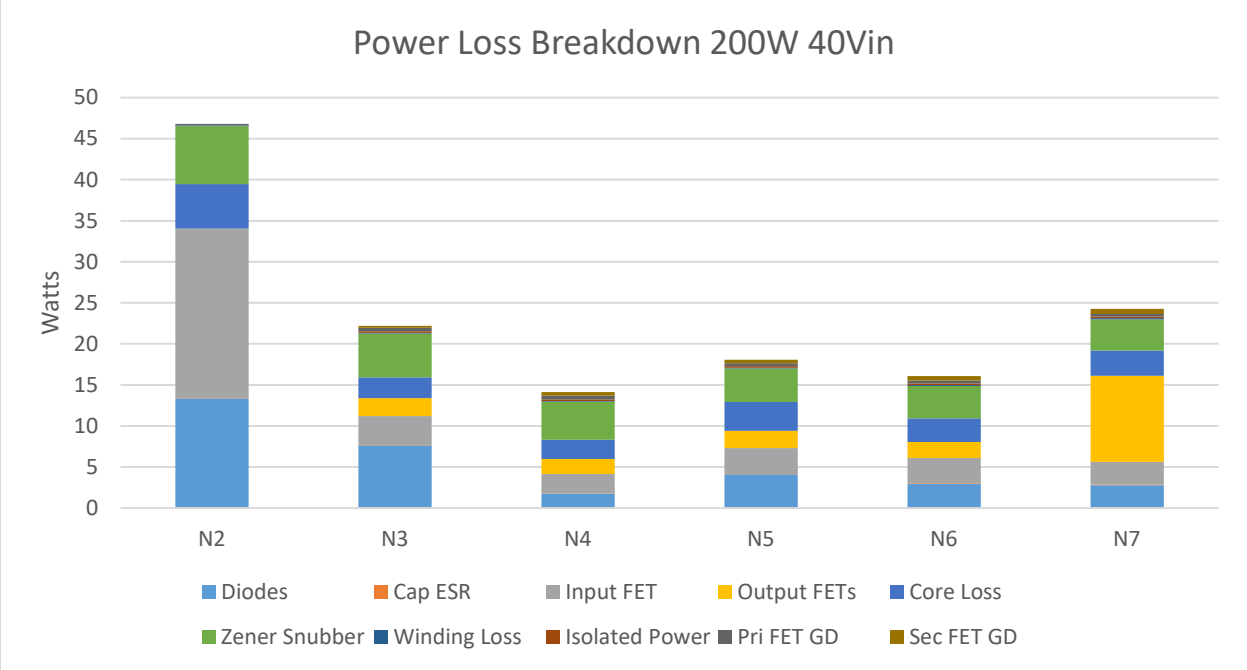


Figure 83. 200W 40Vin Loss Breakdown Bar Graph

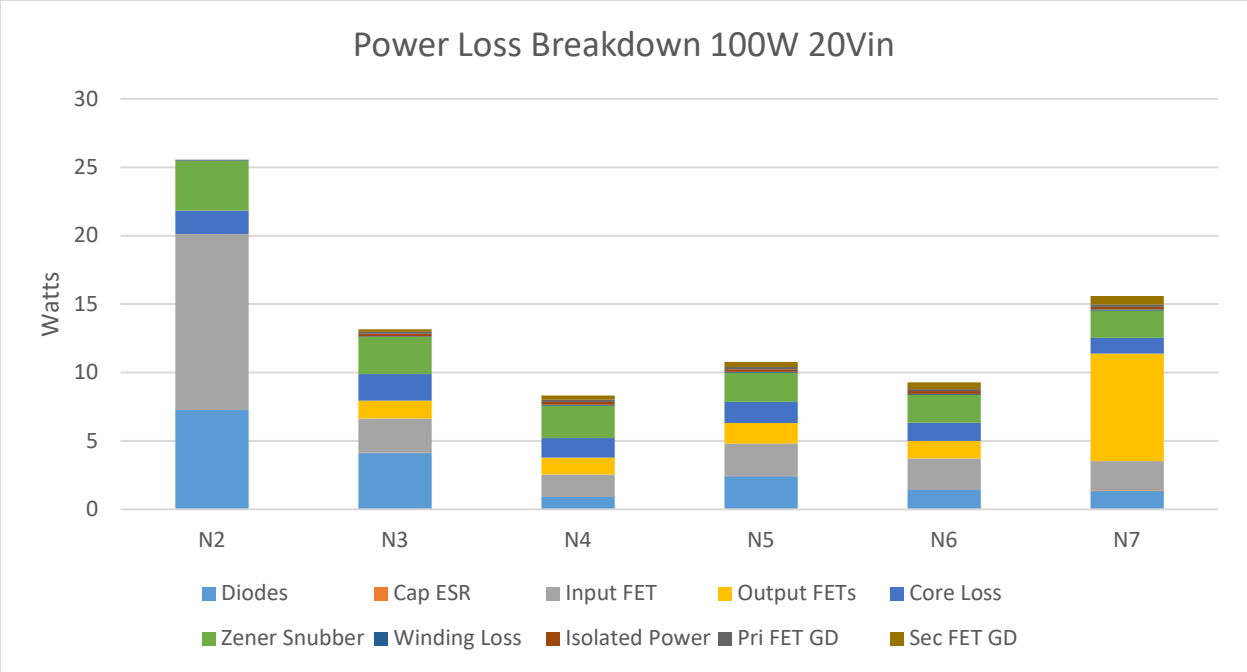


Figure 84. 100W 20Vin Loss Breakdown Bar Graph

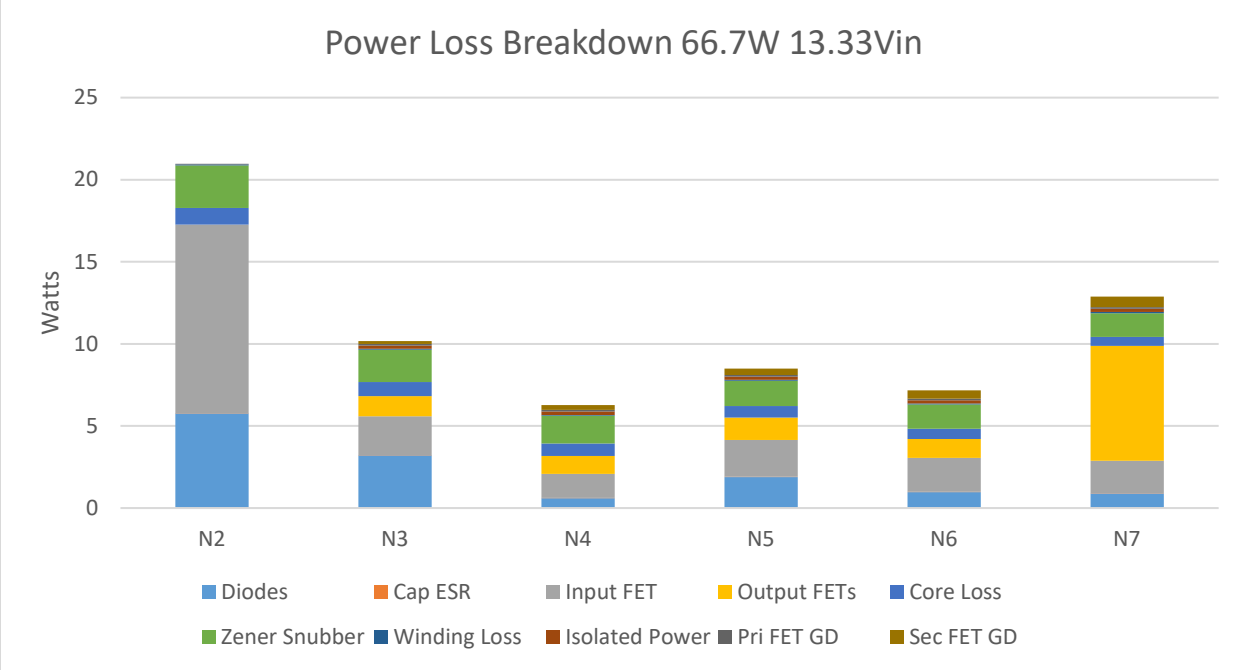


Figure 85. 66.7W 13.33Vin Loss Breakdown Bar Graph

3.11.5 Operating Parameter of Final Designs

Each of the optimal designs from the previous section has an associated duty cycle and switching frequency of operation associated with it. That information is shown in

Table XXVII and will help further explain the power loss trends seen for flyback to multilevel converters.

Table XXVII. Operating Parameters for Final Designs

	200W 40Vin		100W 20Vin		66.67W 13.33Vin	
Converter	Duty	Freq [Hz]	Duty	Freq [Hz]	Duty	Freq [Hz]
N2	0.86	207,387	0.93	117,470	0.95	100,000
N3	0.75	160,070	0.86	103,324	0.90	100,000
N4	0.67	147,943	0.80	109,799	0.86	100,000
N5	0.60	112,270	0.75	100,000	0.82	100,000
N6	0.55	112,316	0.71	100,000	0.79	100,000
N7	0.50	100,000	0.67	100,000	0.75	100,000

From the previous section it was apparent that the FCMFC greatly reduced the power loss associated with the primary FET. Table XXVII shows that the N2 converter is switching at a higher frequency compared to the FCMFC converters. This is partially the reason for its higher loss but also the voltage stress it handles is much higher due to the flybacks operation. These frequencies listed are shown for the converter operating as efficiently as possible for a given operating point so there are tradeoffs between loss mechanisms that lead to these duty cycle and switching frequency values. Note that the duty cycles of operation for the higher-level converters is lower, another reason for higher efficiencies in these converters.

3.12 Final Decision

The results listed in the previous Table XXIV and Table XXVII show that N4 is the most efficient of the six converters considered. N4 values are highlighted in gray to emphasize this being the converter of choice. The N4 is at the cross over point of benefit and trade-offs for the loss mechanisms and less complex to implement than the N6 which is a close second in terms of efficiency. These results are heavily dependent on the devices available and operating parameters of the converter. In Figure 56, Figure 57, and Figure 58 the N4 converter has the lowest relative failure rate for the primary and secondary FETs and also secondary diodes. It is only minimally surpassed in some instances by higher order converters that are more complex to implement.

Cost comparison shown in Figure 60 reveals the N4 to be the most expensive to implement. This cost value is correlated to supply chain constraints due to COVID19. Given a more normalized supply of semiconductors, the higher order converters would scale linearly in terms of expense making the N4 on the lower end of cost, while still likely more expensive than the flyback converter. Cost savings could result for a manufactured product that would need considered before a thorough decision could made on board cost. This section and information serves as an exercise in prototype cost and a basis for a more detailed cost analysis. For example, the FCFMC converters have significantly reduced component loss and would require a smaller and less expensive heat sink.

3.13 LTspice Simulation

An LTspice simulation was developed using circuit component models to check the design and the circuit is shown in Figure 86. This circuit was used to test the auxiliary circuitry loading, the snubber circuit, and the stability of flying capacitor voltages. It was also used to push the design slightly beyond its voltage and power limits to check for weakness in the design.

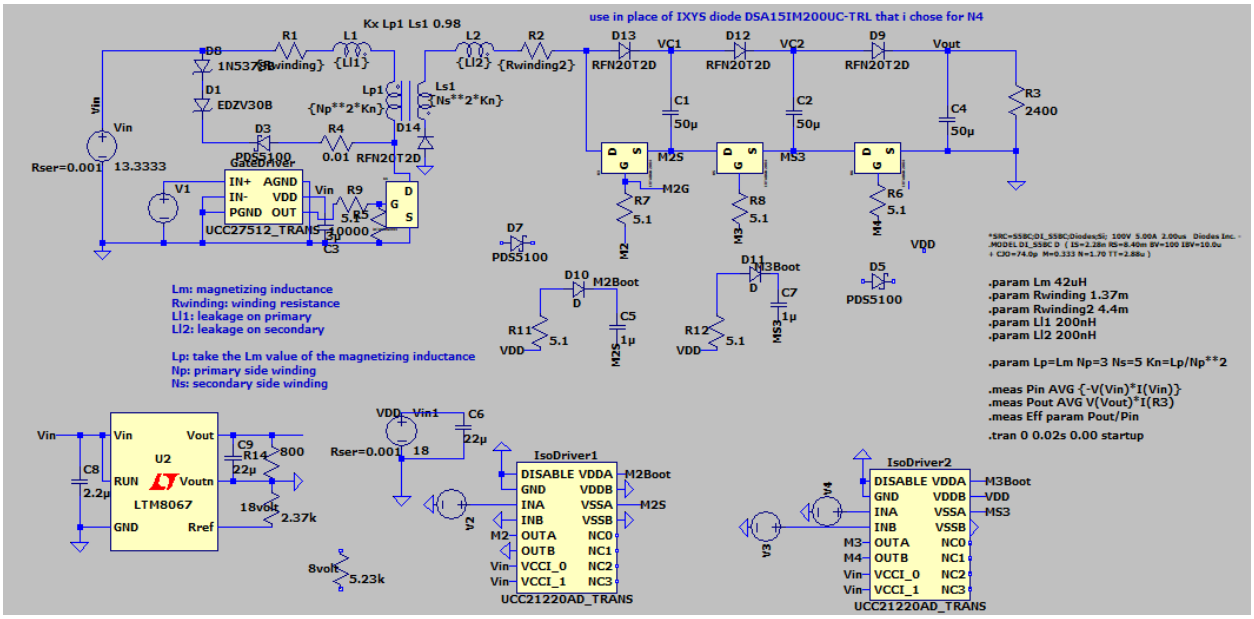


Figure 86. LTspice Circuit

Table XXVIII. LTspice Simulation Results

Operating Point	Duty	Pout [W]	Efficiency	MATLAB Eff
13.33 Vin	86.0%	67	88.4%	93.41%
20.00 Vin	80.0%	100	88.5%	92.31%
40.00 Vin	66.5%	200	91.0%	91.38%

Testing at the three primary operating points was done to check efficiencies were within range of expectations calculated in section 3.11. Figure 87 shows the input and output power waveform for the 13.33Vin and 66W operating point. This waveshape is consistent with the other two operating points. The efficiencies shown in Table XXVIII for LTspice are not expected to

match those from MATLAB because of simulation and hardware differences as well as circuit component substitutions that were made for components which did not have specific circuit models. The IXTA94N20X4 (94A, 10.6mΩ) FETs are represented I the LTspice simulation by the manufacturer circuit model for IXTA86N20X4 FETs which have an 86A max drain current rating and 13mΩ on-resistance. All operating points have efficiencies within 5% of the expected values and provides assurance that there is no major flaw or mistake in the circuit design. PWM duty cycles were also checked against the MATLAB expectations in the previous section.

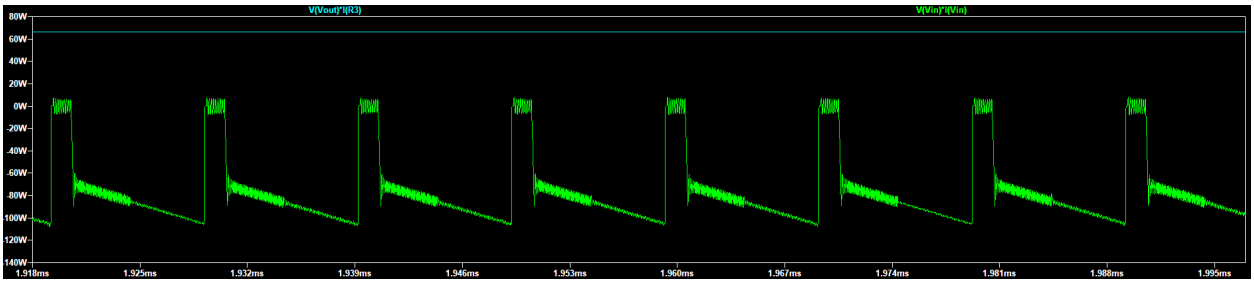


Figure 87. LTspice 13.33Vin 66W Simulation Waveform

3.14 Hardware Design

The component list for the final design is shown in Table XXIX. Semiconductors from the previous design process are included as well as the flying capacitors that are chosen for lowest ESR. The auxiliary component is also shown and has been tested in previous design to work for multilevel operation.

Table XXIX.
200W Component List

Component	Brand	Part number
Planar Transformer	Coilcraft	NA5871-AL 42µH, 3:5
Flying Capacitors	KYOCERA AVX WIMA	2220CC105KAZ2A – 1uF DCP4I051006GD2KSSD – 10uF 600V
MOSFETs	IXYS	IXTA94N20X4 200V, 94A
Diodes	IXYS	DSA15IM200UC-TRL 100V, 15A
Bootstrap Diode	Nexperia	PMEG10010ELR 100V, 1A, 50Apk, 3.7ns
Zener Diodes	Micro Commercial Co	3SMAJ5952B-TP 130V 3W
Heat Sink	Ohmite	BGAH150-125E
Gate Driver	Texas Instruments	UCC27512
Isolated Gate Driver	Texas Instruments	UCC21220A
Isolated Power	Analog Devices	LTM8067
Controller	Texas Instruments	C2000 F28335

3.14.1 Auxiliary Input Power Circuit Design and Snubber Circuit

The input voltage is now varying from 20V to 40V, and an auxiliary input power circuit was designed for 5V to drive primary side gate driver chip logic. Another LTM8067 power circuit was designed to provide an isolated 12V driving voltage for the FET gate drivers. The designs are the same as in 1.3.2 with the exception of the tuning resistor for the 12V circuit being 3.48kΩ. The primary FET snubber circuit voltage was set to 130V per the design process. Five Zener diodes were used in parallel to provide ample current handling at all operating points.

3.14.2 Altium PCB Design

A four-layer board was required to make appropriate circuit routing without interference. Caution was taken to keep the gate driving and logic chips away from higher voltage and current areas that could cause electromagnetic interference with the gate signals. Figure 88, Figure 89, and Figure 90 show the schematic diagram, 2D PCB layout with a combination of the 4-layer selected, and a 3D rendition of the final board. The top red layers show the power and signal routing while the lower three layers are ground and power planes for the main and auxiliary power circuitry. The final board measures in at 325x172mm.

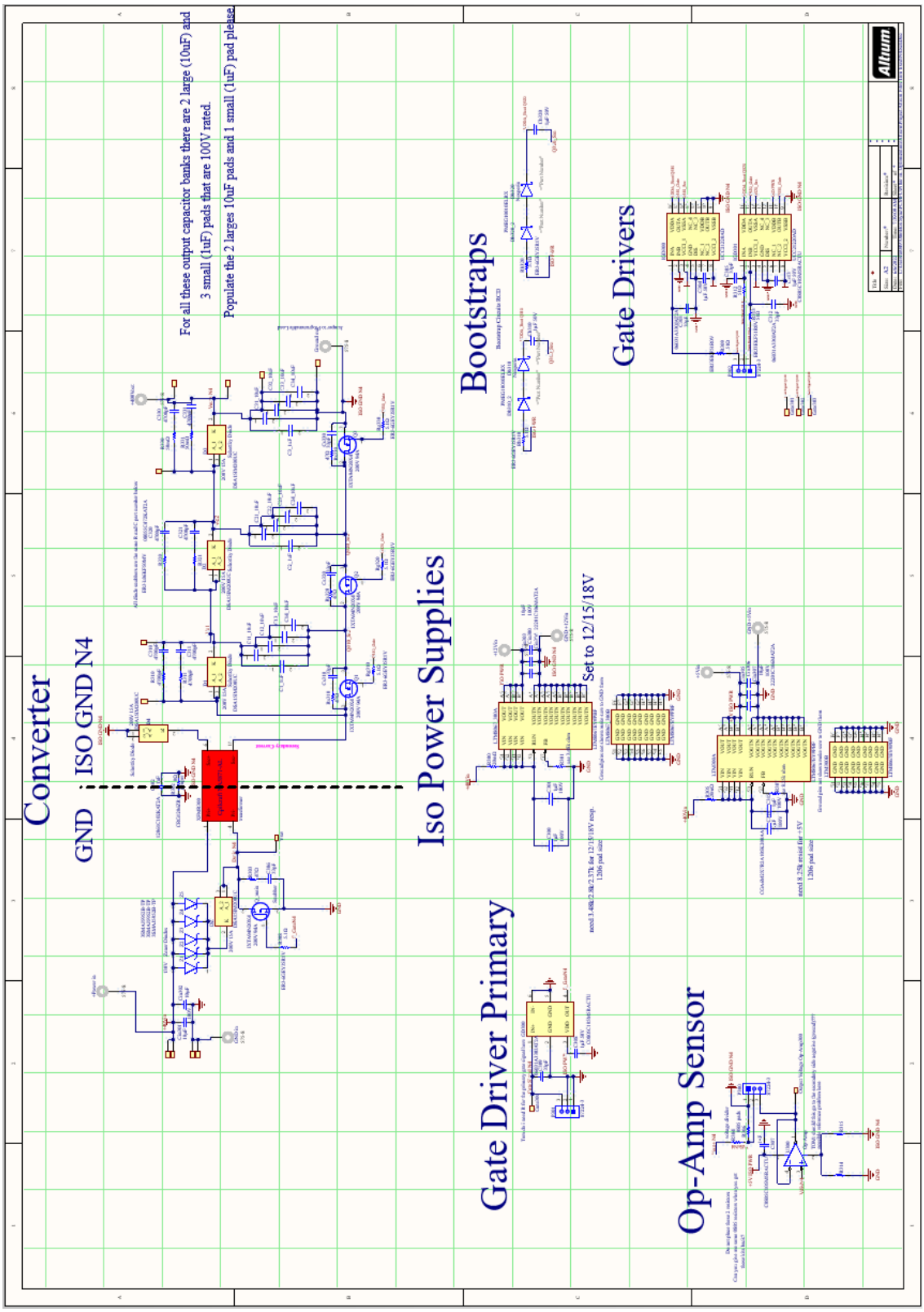


Figure 88. Hardware Schemtic

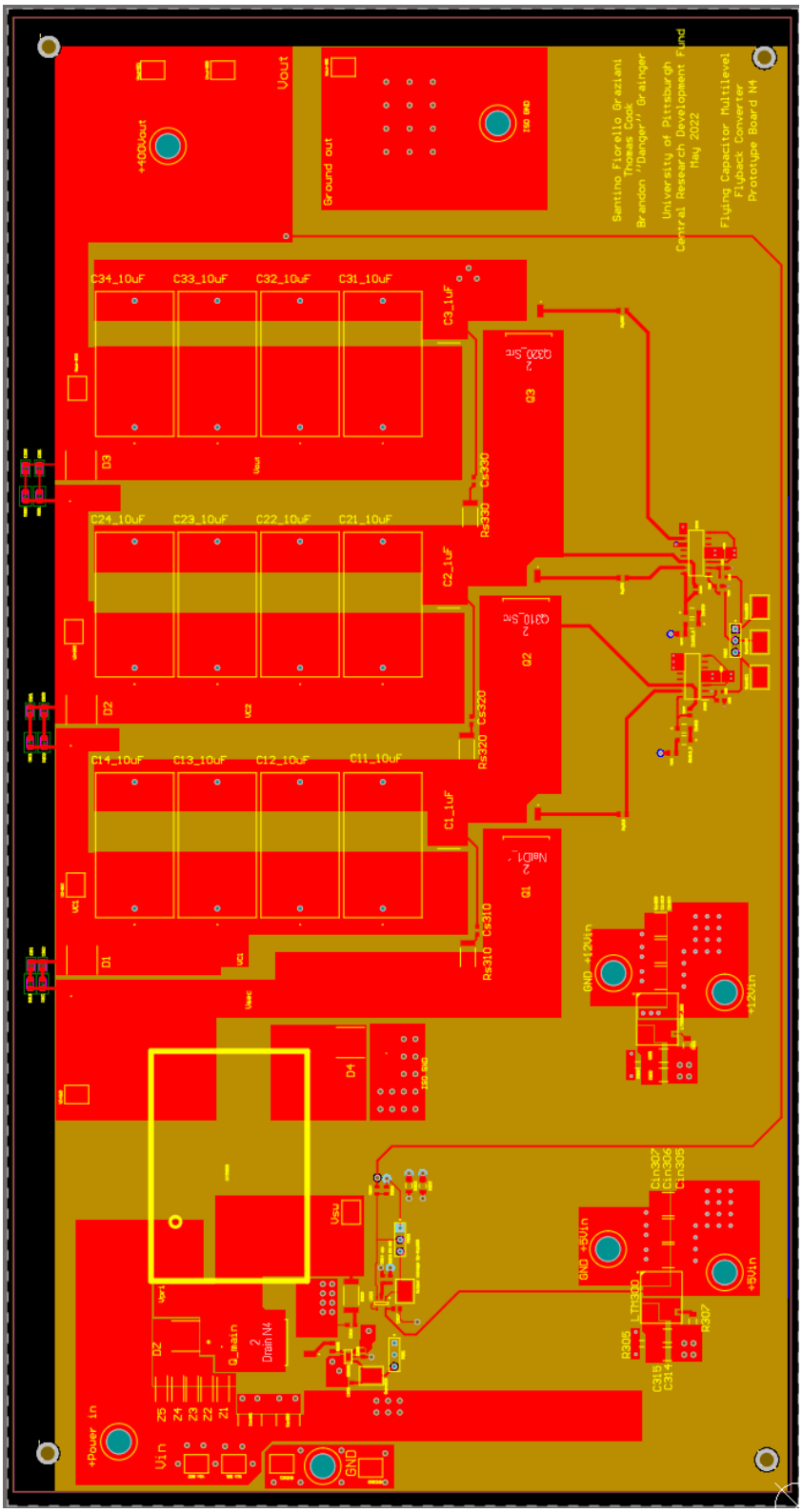


Figure 89. PCB Layout 4-layer Combination

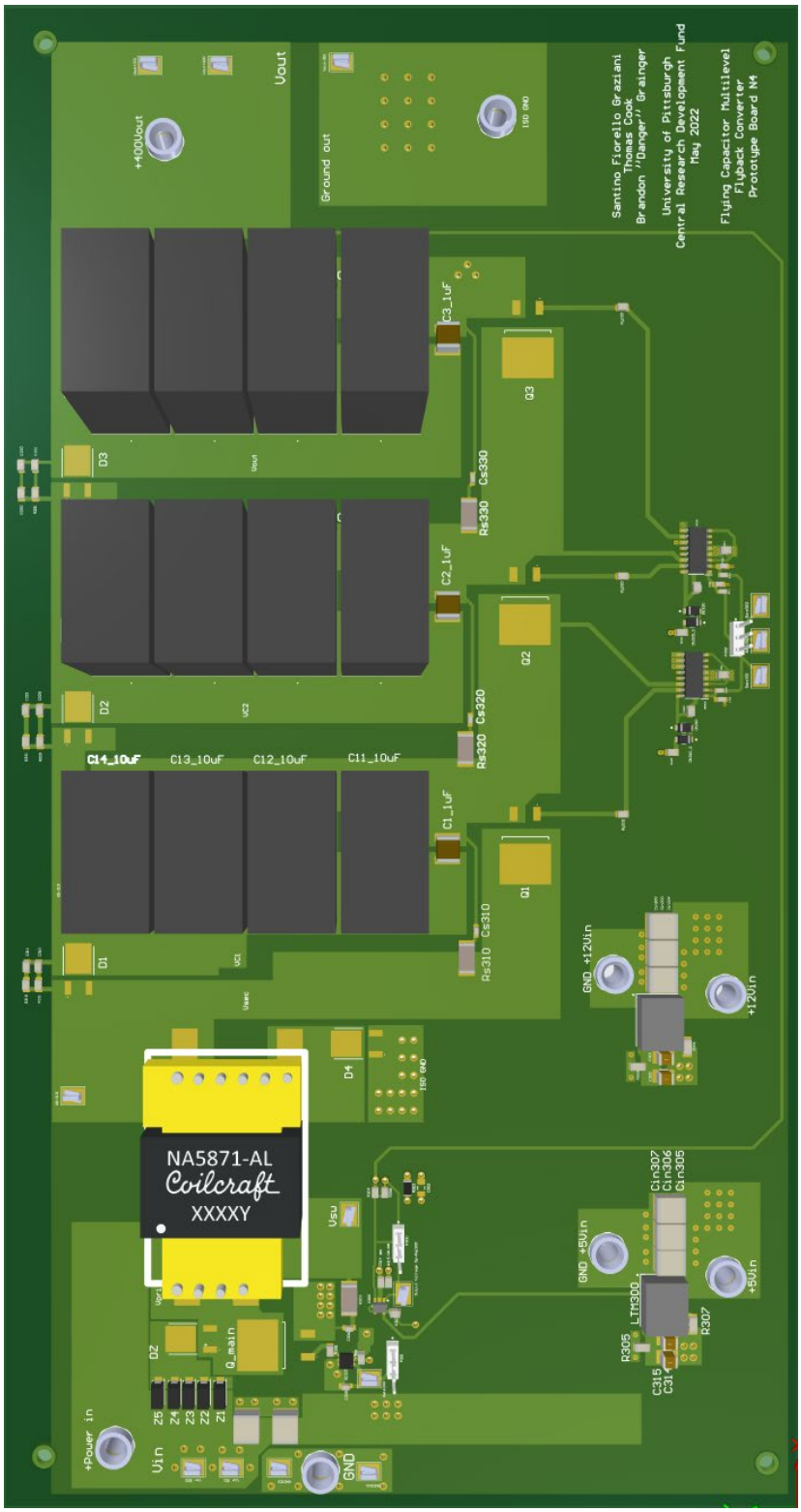


Figure 90. PCB Design 3D Rendition

3.15 Hardware Results

The power converter was tested using a Magna-Power DC power supply (SL500-5.2/208+LXI) and a Sorenson programmable DC load (SLH-300-18-1800). Scope captures were taken using a Yokogawa DL850E. Voltage and current measurements were taken using Fluke 87 multimeters. The hardware testing setup is shown in Figure 91 with equipment outlined. The prototype board is shown in Figure 92.

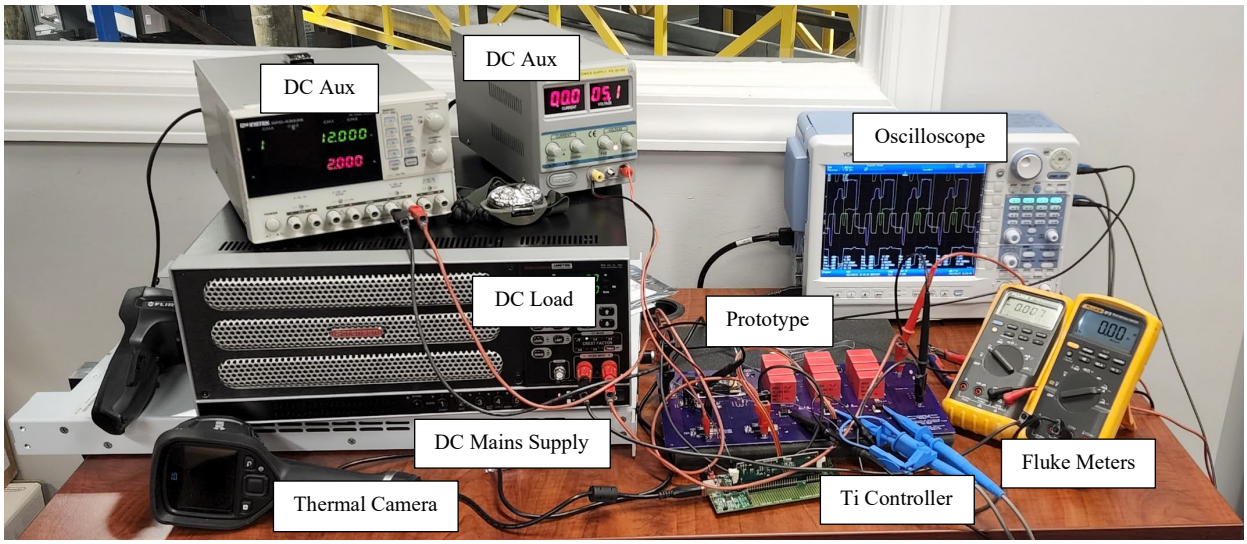


Figure 91. Hardware Testing Setup

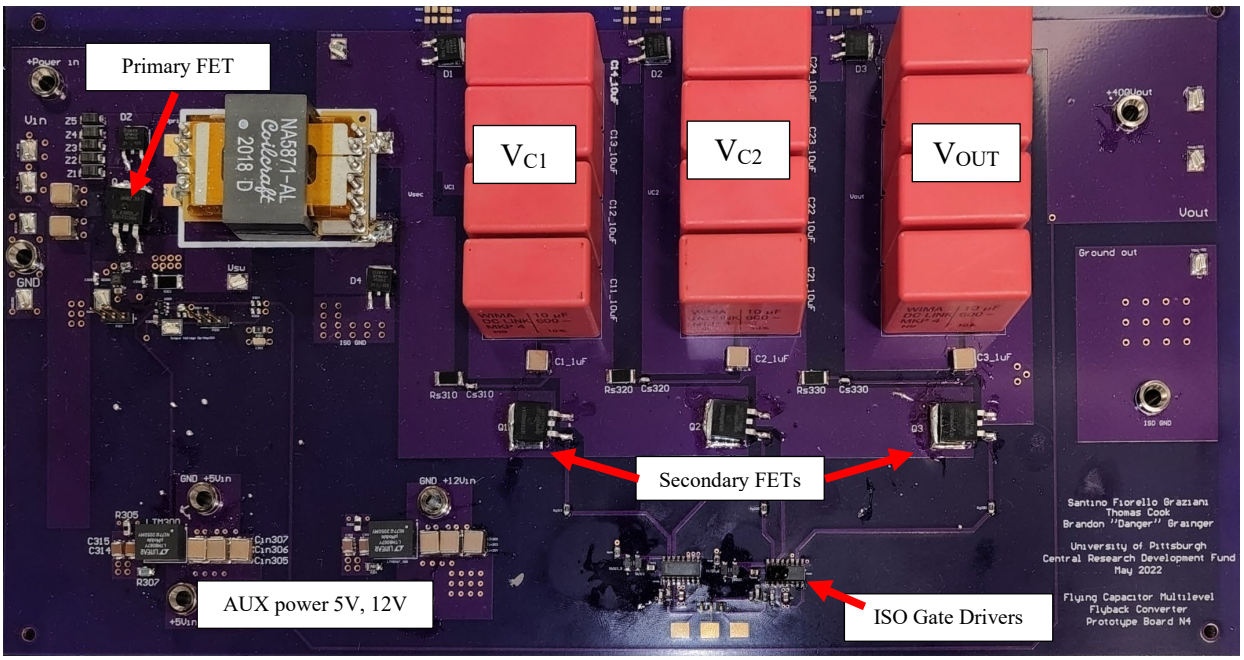


Figure 92. N4 Prototype Board

3.15.1 Voltage Gain and Flying Capacitor Balance

The converter was tested for voltage output capability at light load (~25-50mA). Output voltages are shown in Table XXX. The voltage across the flying capacitors is also shown in this table to verify natural voltage balance occurs. Each operating point achieves the 400V desired voltage and has a natural voltage balance across flying capacitors. This balance is key to maintaining the reduced blocking voltage across the semiconductors chosen for the FCMFC.

Table XXX. Voltage Gain and Balance Testing

Operating Point	Voltage [V]	V_{C2} [V]	V_{C1} [V]
13.33 Vin	417.2	275.2	138.1
20.00 Vin	595	401.5	200.3
40.00 Vin	612	409.7	204.1

3.15.2 Gate Driver PWM and Operation

Gate drive signals are shown for 150kHz and 500khz in Figure 93, Figure 94 respectively. In both figures from top to bottom the gate signals correspond to: the primary FET (yellow), the first flying capacitor FET (cyan), the second flying capacitor FET (pink), and the output capacitor FET (green). The converter was loaded in both cases and the gate drive signals are properly synchronized and phase shifted. Synchronization is critical to stable operation and the voltage balance of the flying capacitors. This ensures that each stage is charged for an equal amount of time by the inductor and precious capacitor stage. In both cases the duty cycle is 85% which corresponds to the yellow gate drive signal for the primary FET. This sets the pace for the converter and the secondary flying capacitor stages follow suit. Notice the secondary FETs have a fixed 60% duty cycle which is necessary to ensure that the secondary FETs are in position when the primary FET turns OFF and supplies current to the secondary side. The secondary switches change during the ON stage of the primary FET when current is not being supplied to the secondary by the transformer. Phase shifting and synchronization makes the three secondary gate drive signals 120º consistently. The secondary FET states determine the charging stage of the flying capacitors as described in section 1.2.1.

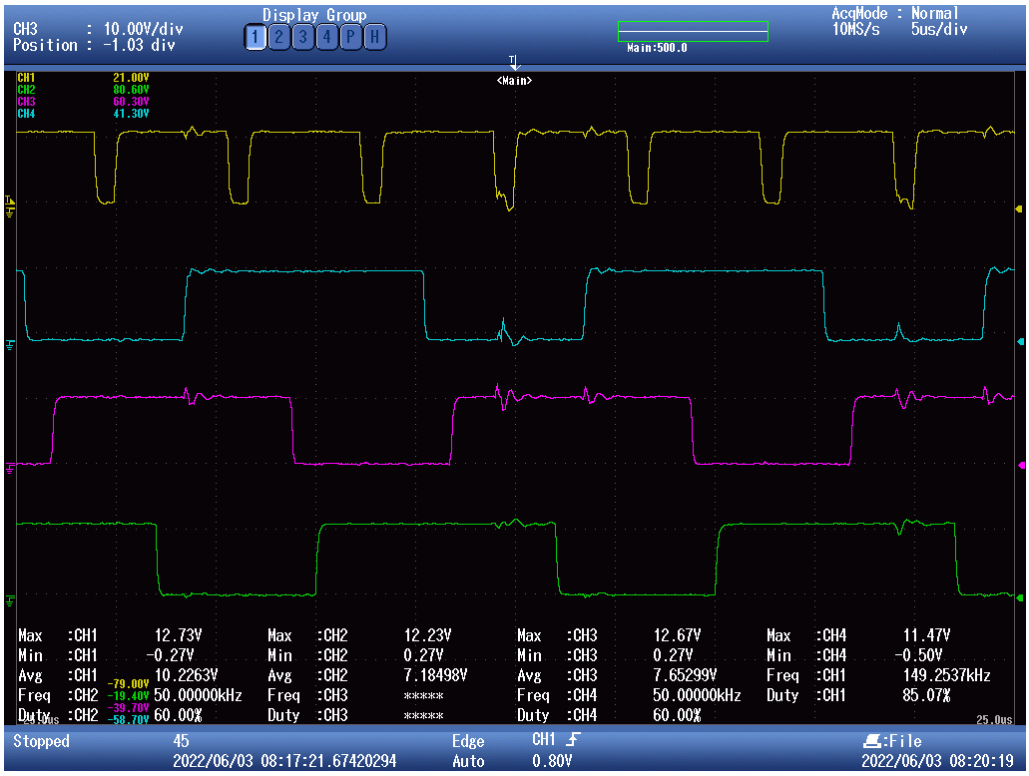


Figure 93. 150kHz Gate Driver Signals PWM Under Load

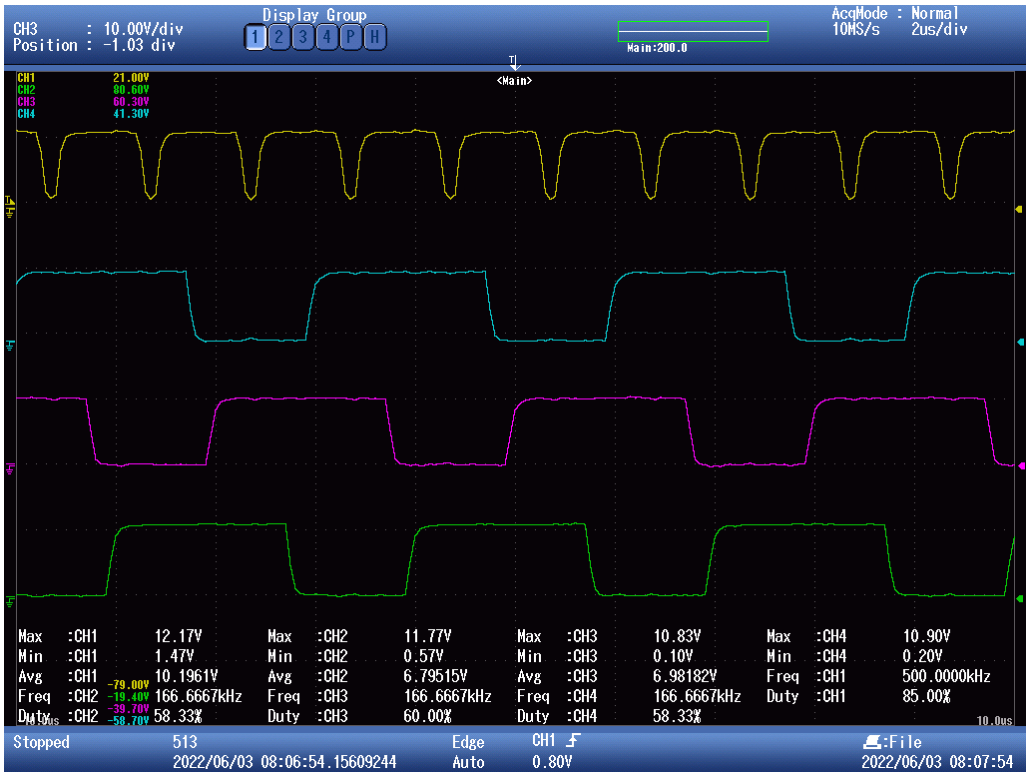


Figure 94. 500kHz Gate Driver Signals PWM Under Load

The primary FET snubber operation was verified and is shown in the scope capture of Figure 95. The yellow waveform on the top is the voltage across the switch node of the primary FET to ground. The secondary PWM gate drive signals are also shown in this capture for timing comparison. The voltage spikes occur when the primary FET turns OFF and there is a voltage rise due to the inductor energy of the transformer's leakage inductance. This energy is re-routed back into the power supply using the Zener snubber circuit and prevents a harmful voltage rise across the primary FET. The snubber circuit is operating as expected and the primary FET is protected for rated operating parameters.

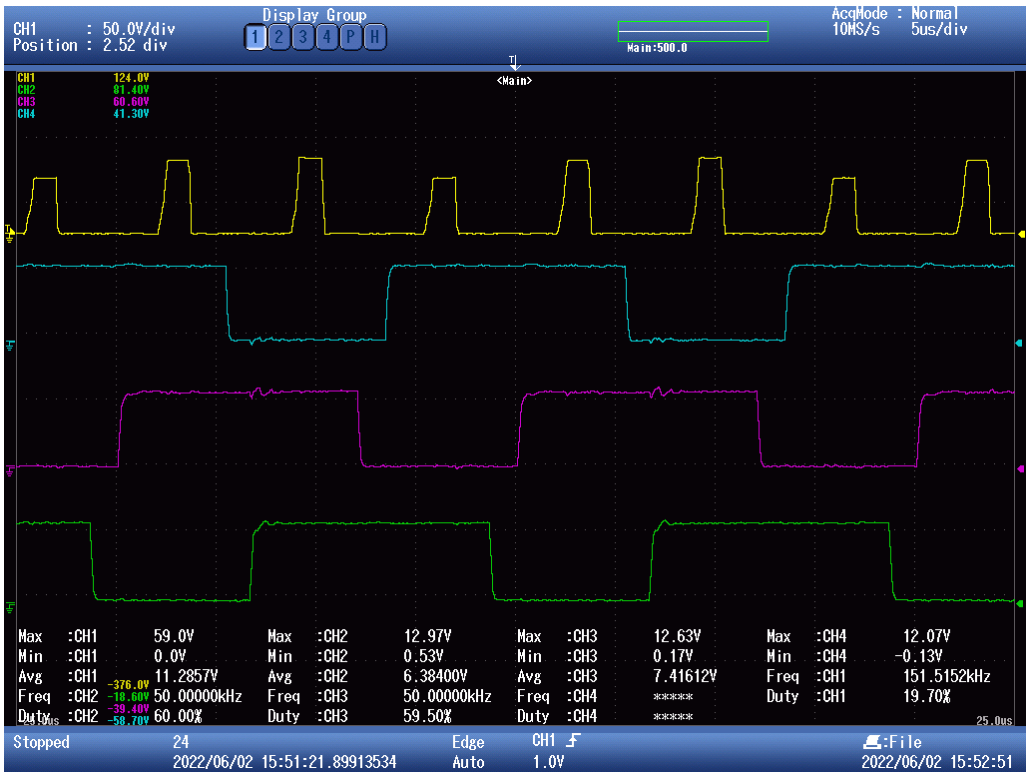


Figure 95. Snubber Circuit Operation

3.15.3 Efficiency Plot Comparison

The predicted theoretical model efficiencies are compared to the hardware design. The supply did not allow enough time to take stable measurements of voltage and current but from iterative testing efficiencies are estimated. The plot below in Figure 96 shows the estimated efficiencies compare to a windowed ranges of operating hardware efficiencies. These windows are based off the iterating testing that was done while reading the measurements from Fluke meters. Data points were not recorded due to supply sinking current into the converter and having to be closely monitoring temperature of the prototype. The efficiency windows are based off of the readings that took place during the testing process of trying to get the board to operate in a stable manner with the DC power supply. Efficiencies trend upwards for higher load as expected.

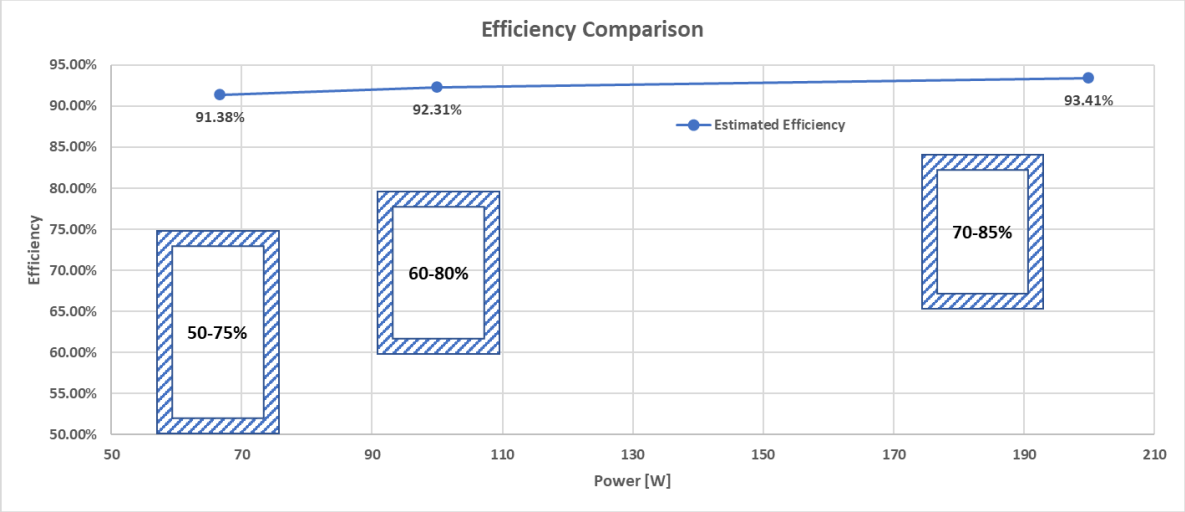


Figure 96. Hardware Efficiency Comparison

Table XXXI. Testing Results

D	Vin	I_{in}	Pin	Vout	I_{out}	Pout	Efficiency	V_{gd}
65%	20	3	60.0	250	0.08	20.00	33.3%	12V
65%	15.5	0.773	12.0	180	0.056	10.08	84.1%	12V
65%	20.1	0.674	13.5	241	0.045	10.85	80.1%	10V
65%	30.8	0.409	12.6	150	0.061	9.15	72.6%	5.1
65%	30.8	0.4	12.32	143	0.061	8.723	70.8%	4.5
65%	41.2	0.593	24.4316	219	0.06	13.14	53.8%	4.5
65%	19.89	3.01	59.8689	230	0.127	29.21	48.8%	10

Table XXXI shows the stable testing results that were acquired. This table is not indicative of the converters peak capabilities but what was able to be recorded given DC supply instability and current limitations. Testing was done at 65% duty cycle with varying input and secondary gate driving voltages in an attempt to reach peak power outputs (67-200W). Peak efficiency of 84.1% was achieved at 10W output with a 48.8% efficiency achieved at the highest recorded 29.21W output.

4.0 Research Implications Conclusions and Future Work

The efforts herein present the flying capacitor multilevel flyback converter to the power electronics field. Multilevel conversion as a sub-field has yet to explore the flyback converter for this topology prior to this dissertation and related publications. A new choice is available now for a power electronics designer to consider when designing a power converter for a new application. This converter, while studied for solar voltage boosting, has capabilities for multilevel inversion electric vehicle charging amongst many others.

Flyback converters are one of the most common used for small consumer electronics. This work has extended the capability of the basic flyback converter by modifying it for multilevel operation. The FCMFC improves upon the voltage gain and efficiency of the flyback converter. The addition of flying capacitors allows a designer to use an existing off-the-shelf flyback transformer and extend its power and voltage range. This has the potential to save significant time in the design process. It also makes the industrial adoption of this converter more attractive.

The FCMFC as a standalone converter is relevant in the space on its own and not as a modified and improved flyback converter. It performs at levels equal to or greater than advanced prototypes in the power electronics academic space. The converter also provides electrical isolation which makes it attractive for certain power applications that require circuit protection. This work has shown that the FCMFC exhibits natural balancing which is key for the use of semiconductors with lower voltage ratings. The converter was able to support 600V output operation using 200V MOSFETs without failing due to the voltage balancing.

There are two functioning prototype boards as a result of this work that can be utilized by future students of the Electric Power Systems Lab. The 10W and 200W prototypes could be used

for further efficiency comparison and feedback control stability. The boards were designed using standard package sizes so they can be modified easily to test various types of semiconductors.

The FCMFC was explored for DCM operation but not designed or tested in this fashion. Another field of design is voltage bucking and the FCMFC has potential in this space for exploration. Also, the field of multilevel inversion could be explored using the existing 200W board to make a full microinverter prototype.

5.0 Related Publications

Table XXXII below shows all related publications in chronological order. It briefly explains the topics and then has a column for which directive the paper is related to and another for status of the paper. Citations are listed below the table to the corresponding entry for easy reference.

Table XXXII. Six Related Publications

Publication	Topic	Related Directive
[1]ECCE2018	pulsed power & some DC-DC operational analysis	I
[2]IECON2018	pulsed power & some DC-DC stress analysis	I
[3]ECCE2019	eff and non-ideal analysis and BCM D prediction	II
[4]PEDG2021	magnetic design optimization	III
[5]OJPEL2022	Hardware capability	I+II+III
[6]COMPEL2021	Efficiency model	II

1. S. F. Graziani, A. Barchowsky and B. M. Grainger, "A Flying Capacitor Multilevel Flyback Converter for Pulsed Power Applications," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 7063-7068.
2. S. F. Graziani, A. Barchowsky and B. M. Grainger, "Design Considerations of a Flying Capacitor Multilevel Flyback Converter for DC-DC and Pulsed Power Applications," IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, 2018, pp. 1140-1145.
3. S. F. Graziani and B. M. Grainger, "Impacts of Switched-Diode Capacitor Stages on the Flying Capacitor Multievel Flyback Converter," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 3737-3741.
4. S. Graziani, P. R. Ohodnicki and B. M. Grainger, "Double Wound Inductor Design Optimization for the Flying Capacitor Multilevel Flyback Converter using a Modified, T-Model Magnetic Equivalent Circuit," 2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2021, pp. 1-7, doi: 10.1109/PEDG51384.2021.9494172.
5. S. F. Graziani, T. V. Cook and B. M. Grainger, "Isolated Flying Capacitor Multilevel Converters," in IEEE Open Journal of Power Electronics, vol. 3, pp. 197-208, 2022, doi: 10.1109/OJPEL.2022.3160049.
6. S. F. Graziani, T. V. Cook and B. M. Grainger, "Efficiency Modeling of the Flying Capacitor Multilevel Flyback Converter," 2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL), 2021, pp. 1-5, doi: 10.1109/COMPEL52922.2021.9646019.

Appendix A Objective Function Minimization

The MATLAB code has the capability to account for more than three operating points and use the power loss model to create a cost or objective function based on weightings for each of the operating points. These ratings are fractions that sum to one and represent the importance or amount of time that a converter would operate at that particular point. This system can account for converters that have complex power profiles to handle, such as solar converters which have a varying power input or a converter with a variable load. The cost function is shown in equation (A.1) and shows that each operating point has a power loss ($P_{x,y}$) and a particular weighting or alpha value ($\alpha_{x,y}$).

$$J(N) = \alpha_{1,1}[P_{1,1}] + \alpha_{1,2}[P_{1,2}] + \alpha_{1,3}[P_{1,3}] + \cdots + \alpha_{3,3}[P_{3.3}] \quad \text{(A.1)}$$

The results of this for the same converter and operation range from the body of this work are shown in Figure 97. The FCMFC converters are less costly in terms of power loss when considering all operating ranges and equally weighting them (1/9). This tool would be useful in future designs for complex load profiles that need consideration in the design process.

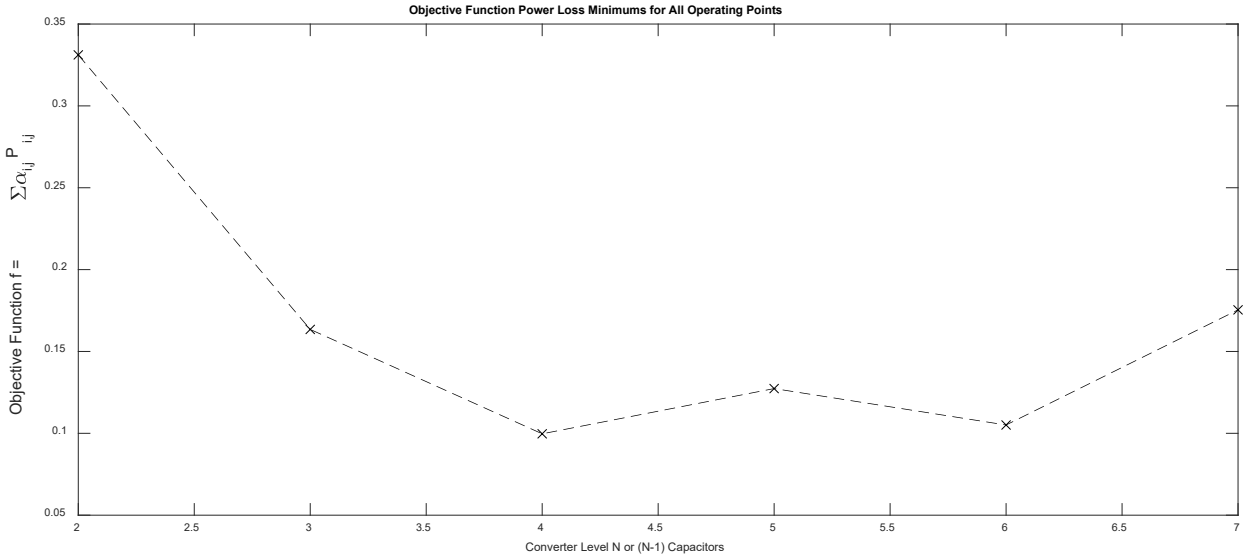


Figure 97. Objective Cost Function Results

Appendix B MATLAB Code for Multilevel Design Process

```
%% %Santino Graziani July 6th 2022
%This script compiles loss components for FCMFC and optimizes converter
%level
close all
clear all
clc
set(0,'DefaultFigureWindowStyle','docked')


%% Constrained Converter Operating Variables
V = 400;                    %output voltage
Vg = 40;                    %input voltage
Pout = 200;                 %output power

%free operating variables
f = 100000:600000;              %switching frequency

Nmax = 7;                       %converter level (flying caps)

%% Transformer Fixed Component Quantities
n  = 5/3;                %turns ratio pri:sec
Lm = 42e-6;              %mag inductance
Ll = 0.2e-6;             %leakage inductance
Rwp = 0.00137;           %winding resistance primary
Rws = 0.0044;            %winding resistance secondary


%%
% Variable Pre-Select Component Quantities using voltage rating
% Each N has it's own set of FETs and Diodes

%% Diodes
    %Reverse Recovery characteristics
    Qr = [0, 37e-9, 0e-9, 0e-9, 0e-9, 0e-9, 0e-9];
%reverse recovery charge [PDS5100 schottky so none listed]
    trd = [0, 20e-9, 22e-9, 1e-9, 24e-9, 1e-9, 1e-9];
%mostly schottky with no RR time or charge at least have 1ns if no listing in
datasheet
    a = [0, 0.0463, 0.0214, 0.0106, 0.0148, 0.0107, 0.0132 ];
%Diode conduction loss coefficients P = ax^2 + bx
    b = [0, 0.9103, 1.412, 0.5357, 0.4576, 0.5496, 0.4177];
    %Cd = [0, 11e-12, 400e-12, 400e-12, 400e-12, 400e-12, 400e-12];
%diode junction capacitance

    %need to estimate this for non-ideal gain D equation        *using
functions for forward power loss
    Vd = [0, 1.9, 1.0, 0.81, 0.71, 0.66, 0.6];
%diode forward voltage drop @6-8A
```

```
    Rd = [0, 0.0270, 2*0.0206, 2*0.0171, 2*0.0121, 2*0.0187, 2*0.0141];
%diode on resistance estimate using slope of conduction V/I curves double for
FCMFC cuz of extra diode



%% MOSFETs
    %Primary
    RQ = [0, 0.130, 0.036, 0.0106, 0.00625, 0.00625, 0.00625];
%MOSFET on-resistance (only input MOSFET 10V Vgs)+ remove current sense R
(10mOhm)
    QG = [0, 26.6e-9, 65e-9, 77e-9, 77e-9, 77e-9, 77e-9];
%MOSFET total gate charge Qg = 24-31nC Ciss = 1976pF
    tr = [0, 39e-9, 9e-9, 9e-9, 37e-9, 37e-9, 37e-9];
%MOSFET rise time (delay times not included)
    tf = [0, 40e-9, 9e-9, 7e-9, 21e-9, 21e-9, 21e-9];
%MOSFET fall time
    QCoss = [0, 88e-12, 281e-12, 750e-12, 516e-12, 516e-12, 516e-12];
%MOSFET ouptut capacitance loss (charges during OFF released at turn-ON)

    %Secondary
    Rq = [0, 0, 0.036, 0.0106, 0.00625, 0.00625, 0.0034];
%MOSFET on-resistance (output MOSFETs 8V Vgs) [IPD30N10S3L-34]
    qG = [0, 0, 65e-9, 77e-9, 77e-9, 77e-9, 87e-9];
%MOSFET total gate charge Qg = 24-31nC Ciss = 1976pF
    qtr = [0, 39e-9, 9e-9, 9e-9, 37e-9, 37e-9, 330e-9];
%MOSFET rise time (delay times not included)
    qtf = [0, 40e-9, 9e-9, 7e-9, 21e-9, 21e-9, 170e-9];
%MOSFET fall time
    qCoss = [0, 0, 281e-12, 750e-12, 516e-12, 516e-12, 670e-12];
%MOSFET ouptut capacitance

%% Capacitors
    Rc = [0, 0.002, 0.002, 0.002, 0.002, 0.002, 0.002];
%capacitor ESR

%% Iso Power
    Viso = 10;          %isolated aux voltage source for secondary FET
driving


%% Reliability Specs for FETs first then diodes/caps?
%update excel sheet when this code is finalized and re-enter temps here
%using a reasonably sized heat sink to bring the operating junction temps
into the usable range (<150C)

Nmax = 7;
    Ttest = 273 + 55;                          %standard base temp

    X2 = 4.045;                               %chi-squared
    Ea = 0.7;                                 %activation energy
    k = 8.617e-5;                             %Boltzmann's constant
    DH = 391000;                              %total device hours
```

```
    %Specific Component Pri FET | Sec FET | Diode  --> these valuse are
calculated in excel 'Component_Temps.xlsx'
    Tuse_pri_fet = 273 + [0, 145.002, 35.812, 31.84302, 34.2748, 34.11196,
33.16265];                          %operating temp
        Af_pri_fet = exp((Ea/k)*(1./Tuse_pri_fet - 1/Ttest));
%Acceleration factor from Arrhenius equation (hotter means fail faster)
        Frate_pri_fet = X2./(2*DH*Af_pri_fet);                    %failures
per hour lambda
        MTTF_pri_fet = 1./Frate_pri_fet;                          %mean time
to failure
      figure
        bar(2:Nmax,Frate_pri_fet(2:Nmax)/Frate_pri_fet(2))
        title("Relative Failure Rate of Primary MOSFET")
        xlabel('Converter [N]');
        ylabel('Relative failures per time');
        %axis([2 7 0 1.1])

        %need to use diode temp to relate sec fets
    Tuse_sec_fet = 273 + [0, 115.8174, 51.07948333, 40.676892, 39.075068,
35.12156583, 76.89994];                         %operating temp
        Af_sec_fet = exp((Ea/k)*(1./Tuse_sec_fet - 1/Ttest));
%Acceleration factor from Arrhenius equation (hotter means fail faster)
        Frate_sec_fet = X2./(2*DH*Af_sec_fet);                    %failures
per hour lambda
        MTTF_sec_fet = 1./Frate_sec_fet;                          %mean time
to failure
      figure
        bar(2:Nmax,Frate_sec_fet(2:Nmax)/Frate_sec_fet(2))
        title("Relative Failure Rate of Secondary MOSFET")
        xlabel('Converter [N]');
        ylabel('Relative failures per time');
        %axis([2 7 0 1.1])

     Tuse_d = 273 + [0,115.8174, 52.83183333, 28.140725, 30.609456, 28.44925,
27.8032];                          %operating temp
        Af_d = exp((Ea/k)*(1./Tuse_d - 1/Ttest));    %Acceleration factor
from Arrhenius equation (hotter means fail faster)
        Frate_d = X2./(2*DH*Af_d);                    %failures per hour
lambda
        MTTF_d = 1./Frate_d;                          %mean time to failure
      figure
        bar(2:Nmax,Frate_d(2:Nmax)/Frate_d(2))
        title("Relative Failure Rate of Secondary Diode")
        xlabel('Converter [N]');
        ylabel('Relative failures per time');
        %axis([2 7 0 1.1])


%% Cost (very affected by semiconductor shortage
Qprice = [0, 4.83, 10.02, 12.92, 4.76, 4.76, 4.76];
qprice = [0, 0, 10.02, 12.92, 4.76, 4.76, 5.95];
dprice = [0, 1.36, 1.01, 1.52, 1.07, 1.07, 1.01];
isopprice = 24.18;
isogdprice = 3.89;
gdprice = 1.05;
```

```
for iter = 2:Nmax
    Cost(iter) = isopprice + gdprice + Qprice(iter) + (iter-1).*(qprice(iter)
+ dprice(iter)) + isogdprice*round((iter-1)/2);
    if iter > 2
        Cost(iter) = Cost(iter) + isopprice;
    end

end
figure
bar(Cost)
xlabel('N-level Converter')
ylabel('Cost in $')
title('Converter Cost')


%% Device Equations
%Set Operating Point with non-ideal gain finder (Outer Control Loop)
d = 0.01:0.0001:0.99;
duty = zeros(1,Nmax);


% %need to check if achieved gain or not otherwise drop it
% plot(d,gain)
% hold on
%gain plot stuff
% [a, b] = size(d);
% g = G*ones(1,b); %desired gain horizontal line
% plot(d,g)
% title("Non-Ideal Gain")
% legend('N = 2','N = 3', 'N = 4', 'N = 5','N = 6','N = 7','N =
8','Location', 'northwest') %,'N = 6', 'N = 7','N = 8', 'N = 9','N = 10', 'N
= 11');
% %fix legen for ideal duty
% xlabel('Duty Cycle');
% ylabel('Non-Ideal Gain');



% DCM check needee???
% operating point of MOSFET needs consideration

%% Power Loss Objective
%figure
%Loop for N level converters starting with flyback
adj = 0.65; %figure out what to do with this (remove it and add device
selection component)
Vc = zeros(1,Nmax); %Zener clamp voltage with series diode drop (it goes
higher in real life cuz time to turn on)
check = string;
c = zeros(Nmax);
cf = zeros(3,3,24);
```

```
for N = 2:Nmax %loop for N

    Vb = Vg + V/(n*(N-1));                %blocking voltage of main Q is Vin +
reflected at turn-ON

    Vds = Vb/n + Vg;
    Vc(N) =  1.2*[40 + V/(n*(N-1))];      %clamping zener voltage design
variable based on design rating
    Vblock(N) = Vb;                       %must be less than Vc (120% as of
now)



    %loop for operating point i = Vg | j = load current (I or R)
    for i = 1:3
        Vin = Vg/i; %set Vin = 40 and vary
        for j = 1:3

            ca = 0; %current adjust for flyback N2
            while ca < 1
                if N > 2 %only loop for N2 flyback
                    ca = 2;
                end


            P = Pout/j;                   %load   output power is linear with
respect to voltage 1:1 slope so assume they scale evenly which is fair
            R = (V^2)/P;                  %load resistance
            G = V/Vin;                    %gain


            %add in extra diode for FCMFC
            Rx = Rd(N) + 2*Rc(N) + (N-2)*Rq(N); %diode cap and output MOSFET
resistances SDC Stage Resistances
            gain = (d - (1-d).*Vd(N)./(n*Vin)).*((R.*(1-d)./(n*(N-
1)))./(R.*((1-d)./(n*(N-1))).^2 + Rwp + d.*RQ(N) + Rx/(n^2))); %RQ primary
FET
            %* this uses diode on resistance which is not in the data
            %sheets so need a good way to estimate this accurately for each
            %diode Hmmmmmmmm
            DUTY(i,j,N) = 0;
            %loop to find all duty cycles at current operating point(i,j)
            for z = 1:length(d)
                if gain(z) > (G - 0.1) && gain(z) < (G + 0.1)
                    duty(N) = d(z);             %find the non-ideal duty
cycle  duty is the current value for N converter in the loop
                    DUTY(i,j,N) = d(z);         %DUTY stores all of the
values for each converter
                    break
                end
            end

            % if one fais to achieve gain the whole converter fails
            if DUTY(i,j,N) == 0
               check(N) = 'fail';
```

```
            c(N) = 1;
        end

        %need to throw a flag is D = 0 becuase it couldn't reach the
        %gain required at this operating point

        %operating points

        I = n*(N-1)*V/(R*(1-duty(N)));        %magnetizing current
*1.155 for RMS value???

        ir = Vin*duty(N)./(f.*Lm);            %ripple current varies with
f

        for k = 1:length(f) %check for crossover into CCM
            if I > 1.5*ir(k)
                cf(i,j,N) = f(k);        %use k later
                CF(i,j,N) = f(k);
                break
            end
        end

        Vblock(i,j,N) = Vb;
        %irip(N) = ir;


        if ca == 1 && N == 2
            I = Inew2;
            ca = 2;
        end

        Iavg(i,j,N) = I;

        %     plot(f, i)    %plott ripple currents vs f
        %     hold on

%% Pcore    Core loss using Coilcraft data NA5871 transformer
    np = 3; %primary turns
    K = 3850;
    Bpk(N,:) = 1000*K*Vin*DUTY(i,j,N)./(f*np); %peak flux density Bpk in mT
for graph in planar_trans_core_loss_coilcraft.pdf

    Pc500kHz(N,:)= [-6e-6*Bpk(N,:).^4 + 0.0041*Bpk(N,:).^3 +
0.3759*Bpk(N,:).^2 - 14.263*Bpk(N,:) + 145.21]/1000;
    Pc400kHz(N,:)= [-4e-6*Bpk(N,:).^4 + 0.0023*Bpk(N,:).^3 +
0.2131*Bpk(N,:).^2 - 8.0856*Bpk(N) + 82.317]/1000;
    Pc300kHz(N,:)= [-2e-6*Bpk(N,:).^4 + 0.0012*Bpk(N,:).^3 +
0.1127*Bpk(N,:).^2 - 4.2757*Bpk(N) + 43.53]/1000;
    Pc200kHz(N,:)= [-9e-7*Bpk(N,:).^4 + 0.0006*Bpk(N,:).^3 +
0.052*Bpk(N,:).^2 - 1.975*Bpk(N) + 20.107]/1000;
    Pc100kHz(N,:)= [-3e-7*Bpk(N,:).^4 + 0.0002*Bpk(N,:).^3 +
0.0169*Bpk(N,:).^2 - 0.642*Bpk(N) + 6.5356]/1000;

    %stitch them together for one coninuous core loss function vs freq
```

```
    Pcore(N,:) = [Pc100kHz(N,1:100000) Pc200kHz(N,100001:200000)
Pc300kHz(N,200001:300000) Pc400kHz(N,300001:400000)
Pc500kHz(N,400001:500001)];

    B = Pcore(N,:) < 0; %find negative core loss values
    Pcore(N,B) = 0;     %set them equal to zero

 %% prob get rid of this section
    %using the 5 data sets for 100-500kHz operation there are 4th order
    %polynomials generated in excel and added here to calculate core
    %loss for given excitation Bpk lump all frequencies to the nearest
    %frequency so 400001Hz --> 400kHz power loss calc

%     if f <= 150000
%         Pcore(N) = Pc100kHz(N);
%     elseif f <= 250000
%         Pcore(N) = Pc200kHz(N);
%     elseif f <= 350000
%         Pcore(N) = Pc300kHz(N);
%     elseif f <= 450000
%         Pcore(N) = Pc400kHz(N);
%     elseif f <= 550000
%         Pcore(N) = Pc500kHz(N);
%     else
%         Pcore(N) = Pc500kHz(N);
%     end

%% Pw
        %Inductor Winding Loss
            Pw(N,:) = (I^2)*Rwp*duty(N) + (1-duty(N))*((I/n)^2)*Rws;
%current only flows on windings while conducting (D = prim (1-D) = sec)

%% Pd
        %Diode Losses
        di = 1;
        if N > 2
            di = 2; %extra diode on FCMFC to prevent reverse conduction
        end
        Pd(N,:) = di.*(a(N)*((1-duty(N))*I/n)^2 + b(N)*((1-duty(N))*I/n) +
f.*((V/(di*(N-1)))*(trd(N)*(I+ir)/n + Qr(N))));   %using data sheet graph for
power dissipation and RR loss (V*Qr + V*i*tr)*fs

%FCMFC has 2 forward conducting diodes that split the blocking voltage in
half which.. so more forward but less RR loss
        %Pd(N,:) = (Vd*I/n + Rd*(I/n)^2)*(1-duty(N)) + (f.*V*Qrr)/(N-1); %for
all diodes %using RR and static model

%% PQ
        %Input MOSFET Loss
        %             |    conduction    |      switch-ON         |
switch-OFF             |          Coss          |
            PQ(N,:) = RQ(N)*duty(N)*I^2  + 0.5*Vb*tr(N)*f.*(I-ir) +
0.5*tf(N)*(Vc(N) + Vd(N))*f.*(I+ir) + 0.5*QCoss(N).*(f)*(Vb^2); %MOSFET
blocks clamp peak voltage at turn off and input voltage + reflected at turn
on
    %need to add gate charge loss Coss each cycle
```

```
%% Pq
        %Output MOSFETs Loss
        if N == 2    %no output mosfet for flyback converter
            Pq(N,:) = zeros(1,length(f));
            Pqsingle(N,:) = zeros(1,length(f));
        else N > 2;
            %         |          conduction           |          switch-ON
|           switch-OFF         |           Coss                |
            Pq(N,:) = (N-2)*Rq(N)*(1-duty(N))*(I/n)^2 + 0.5*(V/(N-
1))*(I/n)*qtr(N).*f + 0.5*(V/(N-1))*(I/n)*qtf(N).*f +
0.5*qCoss(N).*(f)*(V/(N-1))^2;     %share turn ON/OFF, 1 gate charges per
cycle for state change

            Pqsingle(N,:) = Rq(N)*(1-duty(N))*(I/n)^2 + 0.5*(V/(N-
1))*(I/n)*qtr(N).*f + 0.5*(V/(N-1))*(I/n)*qtf(N).*f +
0.5*qCoss(N).*(f)*(V/(N-1))^2;
        end

%% Pz
        %Leakage Loss Into Zener Clamp
            Pz(N,:) = 0.5.*f.*Ll*(n*Vc(N))./(n*Vc(N) - (1/(N-
1))*V).*(I+ir).^2;

%% Pc
        %Capacitor ESR Loss
            Pc(N,:) = 2*(1-duty(N))*Rc(N)*(I/n)^2 - ((1-duty(N))/(N-
1))*Rc(N)*(I/n)^2 + (1-(1-duty(N))/(N-1))*Rc(N)*(V/R)^2; %output cap always
conducts and then 2 conducting for D' all the time except the first cap
charges on its onwn so subtract

%% Pisop
        %Isolated Power Chip
            Pisop(N,:) = 0.200; %using data sheet graph somewhere between
160mW and 600mW same for all N cuz 1 output MOSFET per cycle
            if N == 2
                Pisop(N,:) = 0;
            end

%% Pgd
        %Primary Gate Driver charge loss
            Pgd(N,:) = Vin.*f*QG(N);           %Vdd*f*Qg Qg = 24-31nC Ciss =
1976pF (quiescent loss is neglible according to data sheet)


%% Pigd
        %Secondary Iso Gate Driver charge loss                  Pigd =
Vdd*f*Qg Qg (Gate Charge loss) + Vvcci*Ivcci + Vvdda*Idda + Vvddb*Iddb
(primary power input and then iso driver power inputs on secondary)
            Pigd(N,:) = (N-1)*(Viso*qG(N).*f + Viso*0.0015) + (round((N-
1)/2))*(5*0.0025); %using charts on data sheet
            if N == 2
                Pigd(N,:) = 0;
            end

%% Ploss
```

```
              %Total power loss --> minimize this
              %Pcore = [0,
0.00730307054406291,0.00502998423867712,0.00428103011486400];
                Ploss(N,:) = Pz(N,:) + PQ(N,:) + Pq(N,:) + Pd(N,:) + Pw(N,:)
+ Pc(N,:) + Pcore(N,:)  + Pgd(N,:) + Pigd(N,:) + Pisop(N,:); %Pisop only one
that doesn't vary on f

%% Minimums
            [m, x] = min(Ploss(N,:)); %find minimum of total power loss
            Pmin(i,j,N) = m;
            minfreq(i,j,N) = f(x);
            irip(i,j,N) = ir(x);

            %store all power loss components at the x total minimum
            %store diode min loss for comparison
            Pdmin(i,j,N) = Pd(N,x); %diode loss at chosen frequency
            PQmin(i,j,N) = PQ(N,x);
            Pqmin(i,j,N) = Pq(N,x);
             Pqsinglemin(i,j,N) = Pqsingle(N,x);
            Pzmin(i,j,N) = Pz(N,x);
            Pcmin(i,j,N) = Pc(N);
            Pwmin(i,j,N) = Pw(N);
            Pigdmin(i,j,N) = Pigd(N,x);
            Pgdmin(i,j,N) = Pgd(N,x);
            Pcoremin(i,j,N) = Pcore(N,x);

            %Pqmin

            % revert to minimum frequency if the min is below BCM crossover
point
            if minfreq(i,j,N) < cf(i,j,N)
                Pmin(i,j,N) = Ploss(N,k);
                minfreq(i,j,N) = f(k);
                irip(i,j,N) = ir(k);
                Pdmin(i,j,N) = Pd(N,k); %diode loss at chosen frequency
                PQmin(i,j,N) = PQ(N,k);
                Pqmin(i,j,N) = Pq(N,k);
                Pqsinglemin(i,j,N) = Pqsingle(N,k);
                Pzmin(i,j,N) = Pz(N,k);
                Pcmin(i,j,N) = Pc(N);
                Pwmin(i,j,N) = Pw(N);
                Pigdmin(i,j,N) = Pigd(N,k);
                Pgdmin(i,j,N) = Pgd(N,k);
                Pcoremin(i,j,N) = Pcore(N,k);
            end

            eff(i,j,N) = (V^2/R)/(V^2/R + Pmin(i,j,N));

            %% Current adjust for flyback --> it's major loss components are
not included in Iavg equation from Dragan book (above)
            if ca == 0 && N == 2
                Inew2 = I/eff(i,j,2);
                ca = 1;

            end
```

```
%loop back to adjust current for N2

%             plot(f, Ploss)
%             hold on
            end


        %Pie Chart for all cases 9 for each N level converter Nmax*9 = # of
figures
if i == 1 && j == 1 || i == 2 && j == 2 || i == 3 && j == 3
        if N == 2
            Pflypie(N,:) = [ 100*Pdmin(i,j,N), 100*Pcmin(i,j,N),
100*PQmin(i,j,N), 100*Pcoremin(i,j,N), 100*Pgdmin(i,j,N), 100*Pzmin(i,j,N),
100*Pwmin(i,j,N) ];
            labels = {'Diodes','Capacitor ESR','Input FET','Core','FET Gate
Drive','Zener/Leakage','Winding'};
            explode = [ 0 1 0 1 0 0 0 ];
            figure
            pie(Pflypie(N,:),explode);

        elseif N > 2
            Ppie(N,:) = [ 100*Pdmin(i,j,N), 100*Pcmin(i,j,N),
100*PQmin(i,j,N), 100*Pqmin(i,j,N), 100*Pcoremin(i,j,N), 100*Pzmin(i,j,N),
100*Pwmin(i,j,N), 100*Pisop(N), 100*Pgdmin(i,j,N),  100*Pigdmin(i,j,N) ];
            labels = {'Diodes','Capacitor ESR','Input FET','Output
FETs','Core','Zener/Leakage','Winding','Iso Pow','Pri FET Gate Drive','Sec
FET Gate Drive'};
            explode = [ 0 0 0 0 0 0 0 0 0 0];
            figure
            pie(Ppie(N,:),explode);

        end

        lgd = legend(labels);
        %legend(labels,'Location','southoutside','Orientation','vertical')
        legend(labels,'Position',[0.08 0.1 0.1 0.2])
        title({"N" + N + " Loss Breakdown Ploss = " + Pmin(i,j,N) + " Eff = "
+ 100*eff(i,j,N) + "%" , "Vin = " + Vg/i + " P = " + Pout/j})

end

        end
i = 1;%reset operating points
j = 1;
    end




end %end main loop
%%

%% Failure Checking
%if duty cycle is 0 then the converter could not achieve voltage gain for
```

```
TT = DUTY <= 0;


%Get 1 slice of Pmins to plot and compare N cases
figure
MINS = squeeze(Pmin(1,1,2:Nmax));
plot(2:Nmax,MINS,'k--o','MarkerSize',6)
title("Power Loss for N-level converters at P_{load} = " + Pout + "W | Vin =
" + Vg + "V")
xlabel('Converter Level N or (N-1) Capacitors');
ylabel('Watts');

figure
MINS = squeeze(Pmin(2,2,2:Nmax));
plot(2:Nmax,MINS,'k--o','MarkerSize',6)
title("Power Loss for N-level converters at P_{load} = " + Pout/2 + "W | Vin
= " + Vg/2 + "V")
xlabel('Converter Level N or (N-1) Capacitors');
ylabel('Watts');

figure
MINS = squeeze(Pmin(3,3,2:Nmax));
plot(2:Nmax,MINS,'k--o','MarkerSize',6)
title("Power Loss for N-level converters at P_{load} = " + Pout/3 + "W | Vin
= " + Vg/3 + "V")
xlabel('Converter Level N or (N-1) Capacitors');
ylabel('Watts');


figure
MINS = squeeze(Pmin(1,1,2:Nmax));
plot(2:Nmax,MINS,'k-.o','MarkerSize',6); hold on
MINS = squeeze(Pmin(2,2,2:Nmax));
plot(2:Nmax,MINS,'k--x','MarkerSize',6); hold on
MINS = squeeze(Pmin(3,3,2:Nmax));
plot(2:Nmax,MINS,'k:^','MarkerSize',6);  hold on
title("Power Loss for N-level converters")
xlabel('Converter Level N or (N-1) Capacitors');
ylabel('Watts');
labels = {'P_{load} = 200W | Vin = 40V','P_{load} = 100W | Vin =
20V','P_{load} = 66.67W | Vin = 13.33V'};
legend(labels,'Position',[0.6 0.62 0.3 0.2])
curtick = get(gca, 'xTick');    %set x-axis to integers (FCMFC N-levels are
integers)
xticks(unique(round(curtick)));

%3D plot attempt
% v = [Vg/1, Vg/2, Vg/3];
% p = [Pout/1, Pout/2, Pout/3];
% plot3(v,p,Pmin(:,:,2))



%legend('N2','N3','N4','N5','N6','N7','N8')
```

```
%  x = eff(:,:,1);
%  y = eff(:,:,2);
%  z = eff(:,:,3);
%  figure; plot3(x,y,z,'.-'); %the figure is attached below
%  %what the hell is this plot? wack ass plot imo

 Npass = Nmax;
 for N = 2:Nmax
    if c(N) == 1
        Npass = N - 1;
        break
    end
 end


%loop to find minimum of all operating points
Obj = zeros(1,Nmax); %Npass
Obj(1) = inf;
alpha = (1/9)*ones(3,3);
%alpha = [0 0 1 ; 0 0 0 ; 0 0 0 ]; %can set each weight
for N = 2:Nmax %use Npass once the check logic is fixed
    for i = 1:3
        for j = 1:3
            P = Pout/j;
            Obj(N) = Obj(N) + alpha(i,j)*Pmin(i,j,N)/P;
        end
    end
end

[MIN, Nmin ] = min(Obj);

figure
plot(Obj,'k--x','MarkerSize',9)
title("Objective Function Power Loss Minimums for All Operating Points")
xlabel('Converter Level N or (N-1) Capacitors');
ylabel('Objective Function f = {\Sigma}{\alpha}_{i,j}P_{i,j} ','FontSize',
15);


%%
% figure
% freq = 1000:0.01:300000;
% plot(freq, 0.5*freq*Ll*(n*Vc)/(n*Vc - (1/(N-
1))*V).*(I+(Vin.*duty(N)./(freq.*Lm.*(N-1)))).^2) %leakage loss function vs
frequency (do this for total power and find minimum)
% [m, x] = min(0.5*freq*Ll*(n*Vc)/(n*Vc - (1/(N-
1))*V).*(I+(Vin.*duty(N)./(freq.*Lm.*(N-1)))).^2);
% minfreq = freq(x);

%fmnincon not finding the minimum
% FUN = @(x) 0.5*x*Ll*[(n*Vc)/(n*Vc - (1/(N-1))*V)]*(I+(Vin*duty(N)/(x*Lm*(N-
1))))^2;
% X0 = 1;
% X = fmincon(FUN,X0,[],[],[],[],0,300000);
```

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