

New Architectures and Nonlinear Control Strategy of Dual Active Bridge Converter

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Bachelor of Science in Electrical Engineering, University of Pittsburgh, 2014

Master of Science in Electrical Engineering, University of Pittsburgh, 2021

Submitted to the Graduate Faculty of

Swanson School of Engineering in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

University of Pittsburgh

2022

UNIVERSITY OF PITTSBURGH
SWANSON SCHOOL OF ENGINEERING

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University of Pittsburgh, 2022

This dissertation contains 3 distinct research projects that focus on architectures and control strategies for dual active bridge converters and triple active bridge converters. Objective #1 presents design considerations, performance analysis, and control strategy for a current-fed, triple active bridge converter. This project was verified using a digital signal processor to implement a new control method within both 1) a real time digital simulator, and 2) a triple active bridge prototype. Objective #2 evaluates operational performance improvements to a dual active bridge converter through the use of observers and parameter estimators. The observer tracks the converter current without the need for a current sensor. The quick nature of the presented current observer (less than 1ms) allows the converter controller to compensate quickly to a dc bias current, which should reduce stress on the transformer and extend the lifetime of converter components. The proposed parameter estimator is shown to be suited for use with tunable inductors, allowing the controller to maintain design requirements even with dynamically changing magnetics. Objective #3 presents a finite element analysis of a 3-winding, concentric wound, 50kW, 10kHz ferrite ribbon transformer. This study models the performance of the transformer within a triple active bridge experimental test bed. When possible, these projects have been submitted and/or published within IEEE conferences and journals to further the field of study of dual active bridge converters for use in multiport and medium voltage applications.

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Nomenclature

DAB	Dual active bridge
DC	Direct current
MMF	Magneto motive force
MV	Medium voltage
MVDC	Medium voltage direct current
ZCS	Zero current switching
ZVS	Zero voltage switching
ϕ_x	Switching phase shift angle at port x with respect to port 1
D_x	Duty cycle of switching voltage waveform at port x
f_s	Switching frequency
n_x	Transformer turns ratio at port x
L_{dc}	Self-inductance of mutual inductor
L_M	Mutual inductance of mutual inductor
V_{xDC}	DC bus voltage at port x
v_x	Port voltage at port x
i_x	Port current at port x
v_{Lx}	Transformer leakage inductance voltage at port x
V_{armx}	Square wave peak voltage for arm voltage at current-fed port x
v_{armx-y}	Square wave voltage for arm y voltage at current-fed port x
v_{armx}	Switching voltage waveform for current-fed port x

v_{Tx}	Voltage across transformer winding at port x
v_{xDCh1}	Voltage across high-side mutual inductor 1 at current-fed port x
v_{xDCh2}	Voltage across high-side mutual inductor 2 at current-fed port x
v_{xDCl1}	Voltage across low-side mutual inductor 1 at current-fed port x
v_{xDCl2}	Voltage across low-side mutual inductor 2 at current-fed port x

1.0 Background

The widespread adoption of dc systems for low-voltage applications at the distribution level has spurred further research into even higher power dc networks, including increased system voltages into the medium voltage (MV) range. At this point, many benefits of distributed energy resources (DERs) such as: increased system resilience, reduced transmission and generation capacity costs, and lowered environmental effects, are common knowledge in the industry.

Unfortunately, without proper control, the increasingly dynamic distribution system is more likely to face voltage instability and protection coordination challenges [1]. One possible method of addressing these challenges is to place the DERs on a dc network instead of an ac network. Dc networks have been highly effective in the past at providing continuous, high-quality power to sensitive loads at the LV level by utilizing energy storage and advanced control to quickly respond to system transient events [2]. With the development of wide bandgap semiconductor devices, it is becoming viable to operate at the kilovolt level using solid-state switches [3]. In addition to switching device technology improvements, the increased levels of renewable energy resources entering the grid at the distribution level or naval grid architecture is creating a demand for increased control and safety measures at those levels. Figure 1 shows the key differences between a unidirectional ac network and a bidirectional dc network. Note that shipboard grids typically contain multiple electrical grid zones such as these, which only further increases the complexity of the network [4].

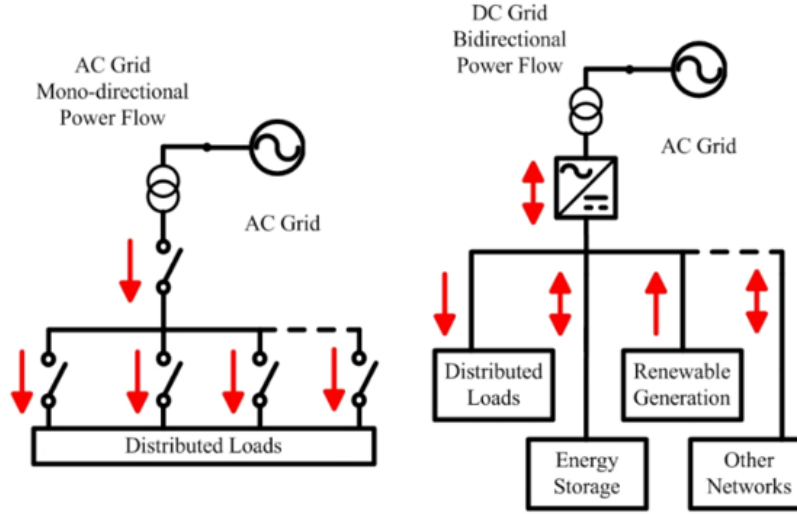


Figure 1: Monodirectional AC Grid (left) and Bidirectional DC Grid (right)

However, as the capacity of dc networks is increased, certain concerns arise. Namely, DERs themselves typically increase the control burden of the network [1], [5], [6]. In addition, the intermittent nature of renewable energy resources usually requires the system designer to include energy storage devices to reduce transient power fluctuation within the network [7]. On top of it all, traditional ac circuit breakers cannot be used within MVDC networks, making fault protection of these networks difficult.

A key component within dc networks that can address many of these issues is the converters that interface with the network. Modern solid-state switches and stacked topologies have recently enabled the possibility of operating at the kilovolt level for connection to the utility grid [8]–[10]. Power electronics can be used to increase flexibility of the dc network and also to respond to DERs [11]–[14].

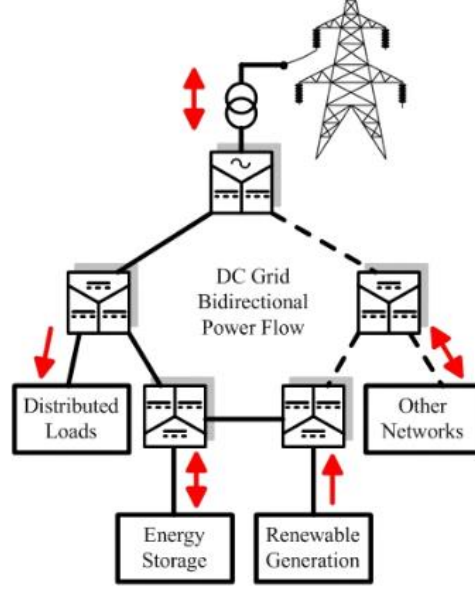


Figure 2: Example dc distribution ring bus network using bidirectional multi-port converters. Note that the distributed loads can receive power at the distribution level without experiencing long transmission losses.

A centralized converter with multiple ports can be used within a dc network to incorporate DERs, storage, and other networks into a grid with minimal conversion steps [15]–[18]. Also, by adding inductance to a converter, fault tolerant operation can be achieved [19]. If these features are combined, the result is a current-fed, multi-port converter that can interconnect multiple MVDC buses within a dc network [20]. The current-fed triple active bridge (CFTAB) converter design containing both of these features will be the basis for the research performed in this article [20]. See Figure 2 for an example of a dc network that makes use of such multi-port converters to create a ring network.

In addition, multi-port converters provide a method to tie in energy storage into the network using centralized control [16], [21]–[23]. At present, there are also at least 6 different categories of fault current limiting power converters available to protect the network from fault events [24].

This rise in microgrid research has opened the possibility of integrating battery energy storage and distributed generation within a shipboard power network. Energy storage has already

proven a reliable method for increasing shipboard power system resilience as well as dispatching energy to pulsed power loads [25]. By leveraging the controllability of power electronics, it is possible to quickly dispatch power to desired electrical zones within the network [25]. This flexibility allows the reduction in size of the on-board generators, which are typically oversized to supply pulsed power loads [25].

A key technology gap within MVDC networks is the lack of a commercially available circuit breaker to interconnect buses and interrupt fault currents. Recently, there have been promising initiatives to develop dc circuit breakers, including a dc breaker for shipboard dc systems [26]. In the absence of a mature product, power electronics can instead be used to control power flow and limit the transient current surge during a fault [24]. Ultimately, in the future it should be possible to improve system resiliency by combining these redundant methods of fault protection for dc systems.

Triple active bridge-based (TAB) converters have been demonstrated to integrate photovoltaics, local dc generation, energy storage, and dc loads within the same system with minimal conversion steps [15], [16]. The addition of inductive components has been shown to provide fault-ride through capability during an extreme voltage collapse or sag event [19]. By incorporating the features of fault tolerance within a TAB converter, the resulting current-fed TAB (CFTAB) converter can interconnect multiple MVDC buses within a dc network [20].

2.0 Research Plan: Objective #1 - Design Considerations, Decoupled Control, and Grid Implementation of a CFTAB Converter

Objective #1 consists of a few distinct projects that focus on a current-fed triple active bridge (CFTAB) converter. The power flow study explores the relationship between the parameters of the magnetic components and the performance of the converter. From the analysis, a controller is proposed which decouples the 2 load ports from one another. The decoupled performance prevents load changes at one port from affecting the performance of the other load port. The controller was implemented within a control hardware-in-the-loop experiment as well as using a prototype 3-port converter. A PLECS model was used to demonstrate two CFTAB converters interconnected and operating in a ring bus configuration.

2.1 Literature Review

The widespread adoption of dc systems for low-voltage applications at the distribution level has spurred further research into even higher power dc networks, including increased system voltages into the medium voltage (MV) range. At this point, many benefits of distributed energy resources (DERs) such as: increased system resilience, reduced transmission and generation capacity costs, and lowered environmental effects, are common knowledge in the industry.

However, as the capacity of dc networks is increased, certain concerns arise. Namely, DERs themselves typically increase the control burden of the network [1], [5], [6]. In addition, the intermittent nature of renewable energy resources usually requires the system designer to

include energy storage devices to reduce transient power fluctuation within the network [7]. On top of it all, traditional AC circuit breakers cannot be used within MVDC networks, making fault protection of these networks difficult.

A key component within dc networks that can address many of these issues is the converters that interface with the network. Modern solid-state switches and stacked topologies have recently enabled the possibility of operating at the kilovolt level for connection to the utility grid [8]–[10]. Power electronics can be used to increase flexibility of the dc network and also to respond to DERs [11]–[14].

In addition, multi-port converters provide a method to tie in energy storage into the network using centralized control [16], [21]–[23]. At present, there are also at least 6 different categories of fault current limiting power converters available to protect the network from fault events [24].

A centralized converter with multiple ports can be used within a dc network to incorporate DERs, storage, and other networks into a grid with minimal conversion steps [15]–[18]. Also, by adding inductance to a converter, fault tolerant operation can be achieved [19]. If these features are combined, the result is a current-fed, multi-port converter that can interconnect multiple MVDC buses within a DC network [20]. The current-fed triple active bridge (CFTAB) converter design containing both of these features will be the basis for the research performed in this article [20]. See Figure 2 for an example dc network that makes use of such multi-port converters to create a ring network.

2.2 Description of Converter

2.2.1 Converter Topology

Traditionally, a dual active bridge (DAB) converter is comprised of a high frequency transformer with both the primary and secondary windings each having a full H-bridge interface to the primary and secondary dc buses [5], [27]–[29]. The primary-side H-bridge will generate a square waveform from the primary dc bus and apply it to the primary windings of the high frequency transformer. Likewise, the secondary-side H-bridge will generate a square waveform from the secondary DC bus and apply that voltage waveform to the secondary windings of the high frequency transformer. This traditional DAB topology can be controlled by adjusting the phase angle delay of the secondary side square wave with respect to the primary. Triple active bridge (TAB) converters are similar, with the addition of a tertiary H-bridge port and a 3-winding high frequency transformer [21], [30].

The current-fed triple active bridge (CFTAB) converter developed in this paper takes a similar design to a TAB converter, with mutual inductor pairs and MMC style arms added to the medium voltage windings of the 3-winding transformer [20]. The topology of the converter is shown in Figure 3. The secondary and tertiary ports are both connected to their respective MV dc buses. The application for the MV dc buses could be a redundant connection to a critical load, or to two separate dc buses altogether with independent load and generation profiles. To operate at MV levels, the secondary and tertiary sides will require switching submodules to be placed in arm configurations as shown in Figure 3. A simplification is made by in this paper by approximating each stacked arm submodule as a single ideal voltage source. This eliminates the need for a

complex and sensitive capacitor balancing scheme when modeling and evaluating the performance of the CFTAB converter.

The winding leakage inductance of the primary, secondary, and tertiary windings are L_1 , L_2 , and L_3 , respectively. The MV ports have mutual inductor pairs, and the naming convention is based on the pattern L_{xDCyz} , where x is the port number, y is either ‘ h ’ for high-voltage side (or closer to the positive dc voltage) or ‘ l ’ for low-voltage side (or closer to the negative dc voltage), and z is either 1 or 2 which identifies which inductor within the mutual inductor pair.

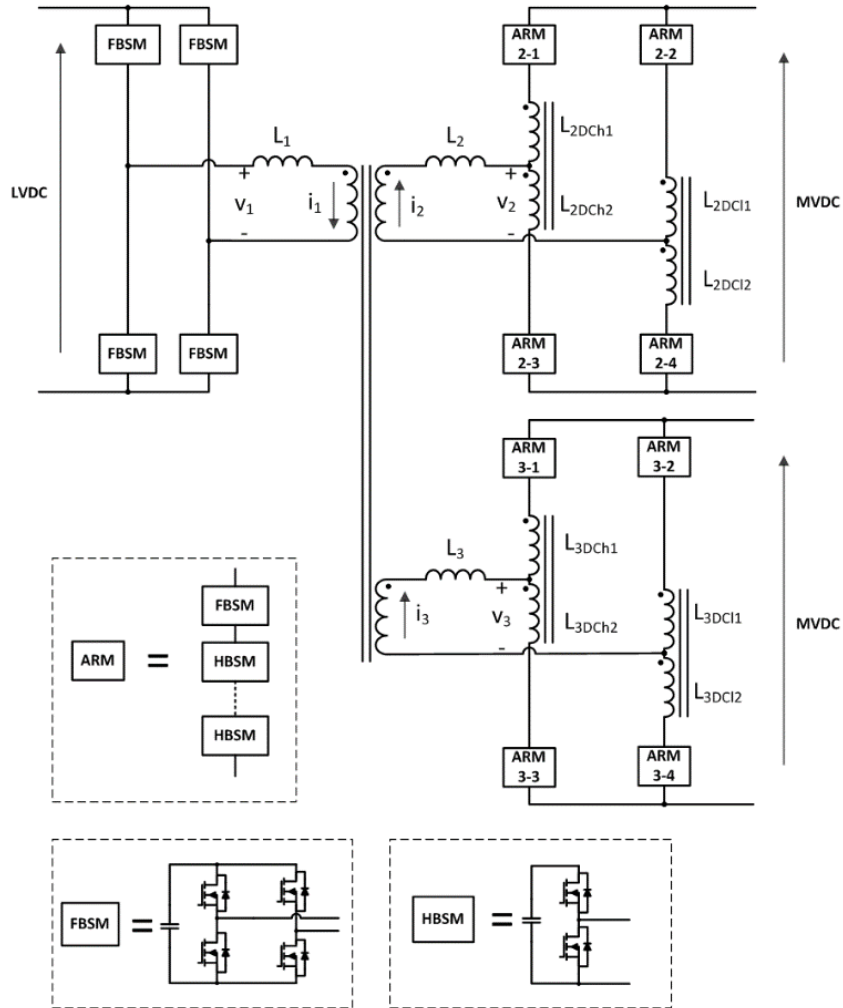


Figure 3: Current-fed triple active bridge topology for the example application of a LV-MV-MV converter.

The MV arms consist of stacked submodules. Each MV port also contains 2 pairs of mutual inductors.

The converter power flow is determined by the voltages v_1 , v_2 , and v_3 and currents i_1 , i_2 , and i_3 which correspond to the primary, secondary, and tertiary transformer windings, respectively. The power flow at any port x can be computed as:

$$p_x = v_x i_x \quad (2-1)$$

Since MMF is shared within an ideal transformer, the overall power flow of the converter can be defined as:

$$p_1 = p_2 + p_3 \quad (2-2)$$

2.2.2 Converter Operation

Traditional single phase shift control is used to regulate the power flow of the converter. As typical for DAB based converters, the average current through the transformer is assumed to be zero under stable operation. The proposed control is phase shift-based and uses average power output as the control reference. Shown in Figure 4 are the square voltage waveforms that are applied at each port of the converter. Note that while the voltage v_1 is directly applied to the primary windings of the transformer, the arm voltage waveforms v_{arm2} and v_{arm3} are not directly applied to the secondary and tertiary MV transformer windings due to the mutual inductors. The voltages across the secondary and tertiary windings of the transformer (v_2 and v_3) can nevertheless be computed from the 3 controlled switched voltage waveforms (v_1 , v_{arm2} , and v_{arm3}). The primary voltage waveform v_1 is used as the reference, and the two controllable parameters are the phase shifts of the secondary (ϕ_2) and tertiary (ϕ_3). In addition to controlling phase shift, it is possible to additionally regulate the duty cycles of each square wave. However, the duty cycles at the ports with mutual inductors are bound by the relationship in (2-3) [31].

$$V_{busDC} = 2DV_{arm} \quad (2-3)$$

In (3), $D = 0.5$ represents an ideal square wave. If this condition is not met, the mutual inductor pairs will experience a dc voltage bias, and a dc bias in the current will result. Therefore, the duty cycles at the secondary and tertiary ports in this application are not freely available to be used as control variables, since they are limited by the voltage ratio of the bus voltages and arm capacitor voltages.

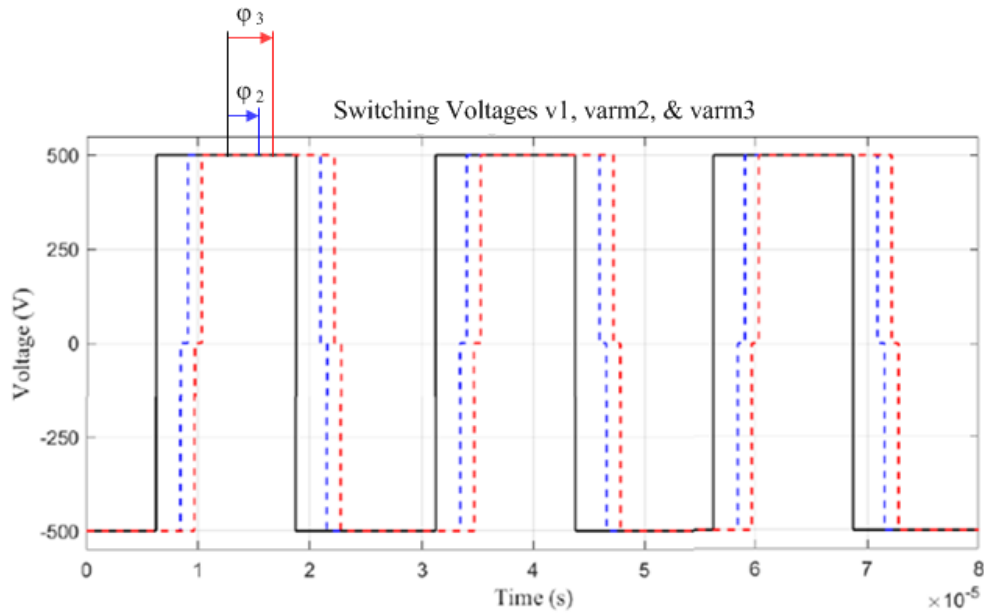


Figure 4: Switching voltage waveforms for each port: v_1 (black), v_{arm2} (blue), and v_{arm3} (red). For this study, the port voltages will all be assumed to be 500V. The phase angles ϕ_2 and ϕ_3 are the control variables and use the primary waveform v_1 as the reference.

2.3 Power Flow Analysis

The average power flow was computed by using a switched circuit model for all 8 possible states. There are potentially more states, but in this application a duty cycle of $D = 0.5$ was

maintained on the secondary and tertiary ports for stability purposes (which reduces the number of possible switched states). To reduce possible states even further to simplify the analysis, the duty cycle of the primary was maintained at 0.5 as well.

A single switching cycle of this converter is expected to be within the kilohertz range (around 1 to 25kHz). This makes it intuitive to assume that the dc bus voltages and submodule voltages will remain constant within a switching cycle. Under this assumption, the current slopes become linear under a constant applied voltage, and a state space representation of the circuit can be constructed.

2.3.1 Decoupling Mutual Inductor Characteristic Equations

One key challenge in the circuit analysis is mathematically decoupling the currents within the mutual inductor pairs. The standard equation for the voltage applied across an inductor with mutual coupling is:

$$v_{\alpha} = L_{\alpha} \frac{di_{\alpha}}{dt} - M \frac{di_{\beta}}{dt} \quad (2-4)$$

Where α denotes the first inductor within the coupled pair and β denotes the second inductor. This equation is unfortunately not a linear state equation due to the two inductor current derivatives. However, it is possible to perform a circuit analysis to substitute for one of the inductor current derivatives. Reducing the equation into a linear form will permit the creation of a state-space model for the circuit for each switch configuration.

Reflecting on the topology in Figure 3, there are 2 mutual inductor pairs on each of the two MV ports. This equates to a total of 8 inductors that have non-linear state equations. Performing

the substitution to a linear form will require 21 equations. The equations can be derived from the circuit diagram in Figure 3 as follows:

Mutual inductor equations from Kirchhoff's voltage loop within one MV port:

$$v_{2dch2} - v_{2dch1} = v_{2dcl1} - v_{2dcl2} \quad (2-5)$$

$$v_{3dch2} - v_{3dch1} = v_{3dcl1} - v_{3dcl2} \quad (2-6)$$

Kirchhoff's voltage loops within each MV port:

$$\begin{aligned} v_{Co2} - v_{Carm2-11} - v_{2dch1} - v_{2dch2} - v_{Carm2-21} \\ = v_{Co2} - v_{Carm2-12} - v_{2dcl1} - v_{2dcl2} - v_{Carm2-22} \end{aligned} \quad (2-7)$$

$$\begin{aligned} v_{Co3} - v_{Carm3-11} - v_{3dch1} - v_{3dch2} - v_{Carm3-21} \\ = v_{Co3} - v_{Carm3-12} - v_{3dcl1} - v_{3dcl2} - v_{Carm3-22} \end{aligned} \quad (2-8)$$

$$v_{Co2} = v_{Carm2-12} + v_{2dcl1} - v_2 + v_{2dch2} + v_{Carm2-21} \quad (2-9)$$

$$v_{Co3} = v_{Carm3-12} + v_{3dcl1} - v_3 + v_{3dch2} + v_{Carm3-21} \quad (2-10)$$

$$v_{Co2} = v_{Carm2-11} + v_{2dch1} + v_2 + v_{2dcl2} + v_{Carm2-22} \quad (2-11)$$

$$v_{Co3} = v_{Carm3-11} + v_{3dch1} + v_3 + v_{3dcl2} + v_{Carm3-22} \quad (2-12)$$

Kirchhoff's current law at ports 2 and 3:

$$\frac{v_{L2}}{L_2} = -\frac{di_{2dch1}}{dt} + \frac{di_{2dch2}}{dt} \quad (2-13)$$

$$\frac{v_{L3}}{L_3} = -\frac{di_{3dch1}}{dt} + \frac{di_{3dch2}}{dt} \quad (2-14)$$

Faraday's law for mutual inductors in ports 2 and 3:

$$v_{2dch1} = L_{dc} \frac{di_{2dch1}}{dt} + M \frac{di_{2dch2}}{dt} \quad (2-15)$$

$$v_{2dch2} = L_{dc} \frac{di_{2dch2}}{dt} + M \frac{di_{2dch1}}{dt} \quad (2-16)$$

$$v_{2dcl1} = L_{dc} \frac{di_{2dcl1}}{dt} + M \frac{di_{2dcl2}}{dt} \quad (2-17)$$

$$v_{2dcl2} = L_{dc} \frac{di_{2dcl2}}{dt} + M \frac{di_{2dcl1}}{dt} \quad (2-18)$$

$$v_{3dch1} = L_{dc} \frac{di_{3dch1}}{dt} + M \frac{di_{3dch2}}{dt} \quad (2-19)$$

$$v_{3dch2} = L_{dc} \frac{di_{3dch2}}{dt} + M \frac{di_{3dch1}}{dt} \quad (2-20)$$

$$v_{3dcl1} = L_{dc} \frac{di_{3dcl1}}{dt} + M \frac{di_{3dcl2}}{dt} \quad (2-21)$$

$$v_{3dcl2} = L_{dc} \frac{di_{3dcl2}}{dt} + M \frac{di_{3dcl1}}{dt} \quad (2-22)$$

Note that the second current slope term is added instead of subtracted as in (2-4). This is simply due to the current direction defined in the other direction in the circuit schematic in Figure 3.

Three-winding transformer turns ratio and current balance equations:

$$\frac{v_1 - v_{L1}}{n_1} = \frac{v_2 + v_{L2}}{n_2} \quad (2-23)$$

$$\frac{v_1 - v_{L1}}{n_1} = \frac{v_3 + v_{L3}}{n_3} \quad (2-24)$$

$$n_1 i_{L1} = n_2 i_{L2} + n_3 i_{L3} \quad (2-25)$$

The final step in preparation to solve the equation is to establish which variables are states within the system and which are controllable inputs. After decoupling the mutual inductor currents, the system can then easily be rewritten into state space form. The state space equation is of the form $\dot{\mathbf{x}} = \mathbf{Ax} + \mathbf{Bu}$ where the arrays \mathbf{x} and \mathbf{u} are:

$$\begin{aligned} \mathbf{x} = [& i_{L1} \ i_{L2} \ i_{L3} \ v_{Co2} \ v_{Co3} \ v_{Carm2-11} \ v_{Carm2-12} \ v_{Carm2-21} \ v_{Carm2-22} \ \dots \\ & \dots \ i_{2dch1} \ i_{2dcl1} \ i_{2dch2} \ i_{2dcl2} \ v_{Carm3-11} \ v_{Carm3-12} \ \dots \\ & v_{Carm3-21} \ v_{Carm3-22} \ i_{3dch1} \ i_{3dcl1} \ i_{3dch2} \ i_{3dcl2}]^T \end{aligned} \quad (2-26)$$

$$\mathbf{u} = [V_1 \ I_{DC2} \ I_{DC3}]^T \quad (2-27)$$

Solving for each state variable is done through MATLAB's symbolic solver toolkit. This solver was used to solve the system of 21 equations to mathematically decouple the mutual inductor currents from their respective pair. The result of the analysis provided a linear equation for the current derivatives for each mutual inductor, which allowed the system to be put into state space form.

2.3.2 State Space Matrix

This section describes the process for computing the average power flow output of the converter. The switching frequency is assumed to be much faster than the time constant of the

capacitors within the dc buses and MV arms. Under this assumption, the inductor currents are the only state variable to change appreciably within one switching cycle, and the currents can be assumed to be linear.

The \mathbf{A} and \mathbf{B} matrices were constructed by using the inductor current derivatives solved in (2-5)-(2-25). The capacitor voltage derivatives were easily computed from Kirchhoff's nodal analysis. Unfortunately, the symbolic representation of the 21-state system has too many terms to fit within this paper, thus the symbolic matrices themselves are not included. Instead, the numeric \mathbf{A} matrix is solved for using the parameters listed in Table I. The switching state that generates positive voltages for v_1 , v_{arm2} , and v_{arm3} is used. The resulting \mathbf{A} matrix is provided in Figure 5.

0	0	0	0	0	0	-156	-156	0	0	0	0	-156	-156	0	0	0	0	0	0
0	0	0	0	0	0	-234	-234	0	0	0	0	78	78	0	0	0	0	0	0
0	0	0	0	0	0	78	78	0	0	0	0	-234	-234	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	-1000	0	-1000	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-1000	0	-1000	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	10000	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	10000	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	69	0	0	117	48	0	0	0	0	-39	-39	0	0	0	0	0	0
0	0	0	69	0	0	-117	-187	0	0	0	0	39	39	0	0	0	0	0	0
0	0	0	69	0	0	-187	-117	0	0	0	0	39	39	0	0	0	0	0	0
0	0	0	69	0	0	48	117	0	0	0	0	-39	-39	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10000	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	10000	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	69	0	-39	-39	0	0	0	0	117	48	0	0	0	0	0	0
0	0	0	0	69	0	39	39	0	0	0	0	-117	-187	0	0	0	0	0	0
0	0	0	0	69	0	39	39	0	0	0	0	-187	-117	0	0	0	0	0	0
0	0	0	0	69	0	-39	-39	0	0	0	0	48	117	0	0	0	0	0	0

Figure 5: State Space \mathbf{A} matrix using the parameters in Table I. Note that this matrix changes with the switched states. This analytical solution for the \mathbf{A} matrix matches the results from the PLECS ‘get’ ‘topology’ function.

Table 1 provides the circuit design parameters for the CFTAB converter. These parameters are based on the design parameters of a previous analysis and are similar to analyses on other multi-port structures [16], [20]. One key feature to note is that the switching frequency of the design has been slowed down from 40kHz to 1kHz to account for performance restrictions within the TI controller and real-time digital simulator (discussed in Section V). To achieve similar output power of the converter, the inductance values are increased by a factor of 40 from the reference design. Note that this limitation of the experimental setup is not in itself a limitation of the speed of the proposed control or converter.

Table 1: CFTAB Converter Circuit Parameters

Variable	Parameter	Value
n_1	Primary Turns Ratio	1
n_2	Secondary Turns Ratio	1
n_3	Tertiary Turns Ratio	1
L_1	Primary Winding Inductance	800 μ H
L_2	Secondary Winding Inductance	800 μ H
L_3	Tertiary Winding Inductance	800 μ H
L_{dc}	Coupled Inductor Inductance	4.0mH
L_M	Mutual Inductance	3.2mH
f_s	Switching Frequency	1.0kHz
D_1	Primary Duty Cycle	0.5
D_2	Secondary Duty Cycle	0.5
D_3	Tertiary Duty Cycle	0.5
V_{1DC}	Primary DC Voltage	500V
V_{2DC}	Secondary DC Voltage	500V
V_{3DC}	Tertiary DC Voltage	500V
V_{arm2}	Secondary Arm Voltage	500V
V_{arm3}	Tertiary Arm Voltage	500V
T_s	Switching Period	1.0ms

One thing to note is that the matrices \mathbf{A} and \mathbf{B} will change with each switch configuration. For simplicity, the duty cycle of all ports is assumed to be 50%. This means that the voltage is positive for half the cycle and negative for the remainder of the cycle. This limits the number of possible states for each port to 2. With 3 ports, the number of possible states is 2^3 , or 8. The matrices \mathbf{A} and \mathbf{B} were computed for each switch configuration.

To confirm the accuracy of the state space matrices, a PLECS circuit schematic of the converter was developed. The results of the PLECS circuit analysis confirmed the accuracy of the state space matrices. The converter model used the circuit parameters in Table 1 match the analytically derived state-space matrices and match the results in Figure 5.

2.3.3 Computation of Steady-State Current Waveforms

Before computing the average power flow, the average current through the transformer inductors must equal zero. Typically, this means that at steady-state, the current values at the start of a switching cycle are non-zero. To determine the correct initial current values, begin with zero initial current within all inductors, and then compute the final current values after the 3rd switched state (halfway through the switching cycle). The initial current is equal to: $i(0) = -\frac{1}{2}i\left(\frac{T_s}{2}\right)$.

As the system is in state-space form, the linear derivatives of currents are known. The change in current during a state is equal to the following equation where φ is the fraction of the total switching cycle that the state is active:

$$\Delta i = \frac{di}{dt} \varphi T_s \quad (2-28)$$

Since all switching signals have a 50% duty cycle, the converter should be exactly halfway through the switching cycle after 3 states.

Once the steady-state initial current values are known, the current waveform for an entire cycle can be computed by applying (2-28) for each of the 6 states. Since there are 6 states, there will be 6 intervals to compute the change in current. The current value at the end of each state can be computed with (29):

$$i_{Lx}(t_{fn}) = \Delta i_{Lx} + i_{Lx}(t_{in}) \quad (2-29)$$

Where x represents the port number, t_{fn} is the final time at the end of state n , and $i_{Lx}(0)$ is the initial current at the beginning of state n .

2.3.4 Computation of Average Power Flow

The voltage during a state is assumed to remain constant. The current changes in a linear trajectory. Therefore, the average power flow at a port during a single state is equal to

$$P_{xn} = v_x \frac{(i_x(0) + i_x(t_{fn}))}{2} \quad (2-30)$$

Where x represents the port number and t_{fn} is the final time at the end of state n . Recall that the current i_x is equivalent to the current flowing through the transformer winding at that port i_{Lx} . The MV voltages can be computed from (2-9) and (2-10), and the primary port voltage is already known. Since the transformer leakage inductor currents are states, the initial and final current at each state can easily be computed using the state space matrices using the method described in (2-28). The average power flow through the converter during an entire switching cycle can be computed by:

$$P_{xavg} = \sum_{n=1}^6 P_{xn} \varphi_{xn} \quad (2-31)$$

Where P_{xn} is the average power at port x during state n , and φ_{xn} is the fraction of the total switching cycle that state n occurs. The phase shift φ can be converted to radians by multiplying by 2π .

2.3.5 Average Power Flow Equations Across All Modes

The average power flow was computed for the entire operating range of the converter ($-0.5 < \phi_2 \leq 0.5$ and $-0.5 < \phi_3 \leq 0.5$). A key feature to note is that the power flow equations are unique to the sequence of the switches. There are 8 possible switching sequences, and each sequence will be called a ‘mode’ of the converter. See Table 2 for the list of possible operating modes of the converter. The resulting power flow equations for each mode are as follows:

MODE 1: $0 < \phi_2 < \phi_3$

$$P_1 \approx L_1^{-1} L_\alpha^{-1} \{ T_s n_1 V_1 [L_2 L_{3\alpha} n_2 V_{Carm2-0} (-2\phi_2^2 + \phi_2) + L_{2\alpha} L_3 n_3 V_{Carm3-0} (-2\phi_3^2 + \phi_3)] \} \quad (2-32)$$

$$P_2 \approx L_\alpha^{-1} \{ T_s n_2 V_{Carm2-0} [-2(L_{3\alpha} n_1 V_1 - L_3 n_3 V_{Carm3-0}) \phi_2^2 + (L_{3\alpha} n_1 V_1 + L_3 n_3 V_{Carm3-0}) \phi_2 + L_3 n_3 V_{Carm3-0} (2\phi_3^2 - \phi_3) - 4L_3 n_3 V_{Carm3-0} \phi_2 \phi_3] \} \quad (2-33)$$

$$\begin{aligned}
P_3 \approx & L_\alpha^{-1} \{ T_s n_3 V_{Carm3-0} [L_2 n_2 V_{Carm2-0} (-2\phi_2^2 - \phi_2) \\
& + (L_{2\alpha} n_1 V_1 + L_2 n_2 v_{Carm2-0}) (-2\phi_3^2 + \phi_3) \\
& + 4L_2 n_2 V_{Carm2-0} \phi_2 \phi_3] \}
\end{aligned} \tag{2-34}$$

Where,

$$\begin{aligned}
L_\alpha = & (L_{dc} - M)^2 n_1^2 + L_2 L_3 (n_1^2 + n_2^2 + n_3^2) \\
& + (L_{dc} - M) (L_2 n_1^2 + L_2 n_2^2 + L_3 n_1^2 + L_3 n_3^2)
\end{aligned} \tag{2-35}$$

MODE 2: $0 < \phi_3 < \phi_2$

$$\begin{aligned}
P_1 \approx & L_1^{-1} L_\alpha^{-1} \{ T_s n_1 V_1 [L_2 L_{3\alpha} n_2 V_{Carm2-0} (-2\phi_2^2 + \phi_2) \\
& + L_{2\alpha} L_3 n_3 V_{Carm3-0} (-2\phi_3^2 + \phi_3)] \}
\end{aligned} \tag{2-36}$$

$$\begin{aligned}
P_2 \approx & L_\alpha^{-1} \{ T_s n_2 V_{Carm2-0} [(L_{3\alpha} n_1 V_1 + L_3 n_3 V_{Carm3-0}) (-2\phi_2^2 + \phi_2) \\
& - L_3 n_3 V_{Carm3-0} (2\phi_3^2 + \phi_3) + 4L_3 n_3 V_{Carm3-0} \phi_2 \phi_3] \}
\end{aligned} \tag{2-37}$$

$$\begin{aligned}
P_3 \approx & L_\alpha^{-1} \{ T_s n_3 V_{Carm3-0} [L_2 n_2 V_{Carm2-0} (2\phi_2^2 - \phi_2) \\
& - 2(L_{2\alpha} n_1 V_1 - L_2 n_2 v_{Carm2-0}) \phi_3^2 + (L_{2\alpha} n_1 V_1 + L_2 n_2 v_{Carm2-0}) \phi_3 \\
& - 4L_2 n_2 V_{Carm2-0} \phi_2 \phi_3] \}
\end{aligned} \tag{2-38}$$

MODE 3: $\phi_3 < \phi_2 < 0$

$$\begin{aligned}
P_1 \approx & L_1^{-1} L_\alpha^{-1} \{ T_s n_1 V_1 [L_2 L_{3\alpha} n_2 V_{Carm2-0} (2\phi_2^2 + \phi_2) \\
& + L_{2\alpha} L_3 n_3 V_{Carm3-0} (2\phi_3^2 + \phi_3)] \}
\end{aligned} \tag{2-39}$$

$$\begin{aligned}
P_2 \approx L_\alpha^{-1} \{ T_s n_2 V_{Carm2-0} [2(L_{3\alpha} n_1 V_1 - L_3 n_3 V_{Carm3-0}) \phi_2^2 \\
+ (L_{3\alpha} n_1 V_1 + L_3 n_3 V_{Carm3-0}) \phi_2 + L_3 n_3 V_{Carm3-0} (-2\phi_3^2 - \phi_3) \\
+ 4L_3 n_3 V_{Carm3-0} \phi_2 \phi_3] \} \quad (2-40)
\end{aligned}$$

$$\begin{aligned}
P_3 \approx L_\alpha^{-1} \{ T_s n_3 V_{Carm3-0} [L_2 n_2 V_{Carm2-0} (2\phi_2^2 - \phi_2) \\
+ (L_{2\alpha} n_1 V_1 + L_2 n_2 v_{Carm2-0}) (2\phi_3^2 + \phi_3) \\
- 4L_2 n_2 V_{Carm2-0} \phi_2 \phi_3] \} \quad (2-41)
\end{aligned}$$

MODE 4: $\phi_2 < \phi_3 < 0$

$$\begin{aligned}
P_1 \approx L_1^{-1} L_\alpha^{-1} \{ T_s n_1 V_1 [L_2 L_{3\alpha} n_2 V_{Carm2-0} (2\phi_2^2 + \phi_2) \\
+ L_{2\alpha} L_3 n_3 V_{Carm3-0} (2\phi_3^2 + \phi_3)] \} \quad (2-42)
\end{aligned}$$

$$\begin{aligned}
P_2 \approx L_\alpha^{-1} \{ T_s n_2 V_{Carm2-0} [(L_{3\alpha} n_1 V_1 + L_3 n_3 V_{Carm3-0}) (2\phi_2^2 + \phi_2) \\
+ L_3 n_3 V_{Carm3-0} (2\phi_3^2 - \phi_3) - 4L_3 n_3 V_{Carm3-0} \phi_2 \phi_3] \} \quad (2-43)
\end{aligned}$$

$$\begin{aligned}
P_3 \approx L_\alpha^{-1} \{ T_s n_3 V_{Carm3-0} [L_2 n_2 V_{Carm2-0} (-2\phi_2^2 - \phi_2) \\
+ 2(L_{2\alpha} n_1 V_1 - L_2 n_2 v_{Carm2-0}) \phi_3^2 + (L_{2\alpha} n_1 V_1 + L_2 n_2 v_{Carm2-0}) \phi_3 \\
+ 4L_2 n_2 V_{Carm2-0} \phi_2 \phi_3] \} \quad (2-44)
\end{aligned}$$

MODE 5: $\phi_2 < 0 < \phi_3; \quad \phi_3 - \phi_2 < 0.5$

$$\begin{aligned}
P_1 \approx L_1^{-1} L_\alpha^{-1} \{ T_s n_1 V_1 [L_2 L_{3\alpha} n_2 V_{Carm2-0} (2\phi_2^2 + \phi_2) \\
+ L_{2\alpha} L_3 n_3 V_{Carm3-0} (-2\phi_3^2 + \phi_3)] \} \quad (2-45)
\end{aligned}$$

$$\begin{aligned}
P_2 \approx L_\alpha^{-1} \{ T_s n_2 V_{Carm2-0} [(L_{3\alpha} n_1 V_1 + L_3 n_3 V_{Carm3-0}) (2\phi_2^2 + \phi_2) \\
+ L_3 n_3 V_{Carm3-0} (2\phi_3^2 - \phi_3) - 4L_3 n_3 V_{Carm3-0} \phi_2 \phi_3] \} \quad (2-46)
\end{aligned}$$

$$\begin{aligned}
P_3 \approx & L_\alpha^{-1} \{ T_s n_3 V_{Carm3-0} [L_2 n_2 V_{Carm2-0} (-2\phi_2^2 - \phi_2) \\
& + (L_{2\alpha} n_1 V_1 + L_2 n_2 v_{Carm2-0}) (-2\phi_3^2 + \phi_3) \\
& + 4L_2 n_2 V_{Carm2-0} \phi_2 \phi_3] \}
\end{aligned} \tag{2-47}$$

MODE 6: $\phi_2 < 0 < \phi_3$; $\phi_3 - \phi_2 > 0.5$

$$\begin{aligned}
P_1 \approx & L_1^{-1} L_\alpha^{-1} \{ T_s n_1 V_1 [L_2 L_{3\alpha} n_2 V_{Carm2-0} (2\phi_2^2 + \phi_2) \\
& + L_{2\alpha} L_3 n_3 V_{Carm3-0} (-2\phi_3^2 + \phi_3)] \}
\end{aligned} \tag{2-48}$$

$$\begin{aligned}
P_2 \approx & L_\alpha^{-1} \{ T_s n_2 V_{Carm2-0} [2(L_{3\alpha} n_1 V_1 - L_3 n_3 V_{Carm3-0}) \phi_2^2 \\
& + (L_{3\alpha} n_1 V_1 - 3L_3 n_3 V_{Carm3-0}) \phi_2 + L_3 n_3 V_{Carm3-0} (-2\phi_3^2 + 3\phi_3) \\
& + 4L_3 n_3 V_{Carm3-0} \phi_2 \phi_3 - L_3 n_2 V_{Carm2-0}] \}
\end{aligned} \tag{2-49}$$

$$\begin{aligned}
P_3 \approx & L_\alpha^{-1} \{ T_s n_3 V_{Carm3-0} [L_2 n_2 V_{Carm2-0} (2\phi_2^2 + 3\phi_2) \\
& - 2(L_{2\alpha} n_1 V_1 - L_2 n_2 v_{Carm2-0}) \phi_3^2 \\
& + (L_{2\alpha} n_1 V_1 - 3L_2 n_2 v_{Carm2-0}) \phi_3 - 4L_2 n_2 V_{Carm2-0} \phi_2 \phi_3 \\
& + L_2 n_2 V_{Carm2-0}] \}
\end{aligned} \tag{2-50}$$

MODE 7: $\phi_3 < 0 < \phi_2$; $\phi_2 - \phi_3 < 0.5$

$$\begin{aligned}
P_1 \approx & L_1^{-1} L_\alpha^{-1} \{ T_s n_1 V_1 [L_2 L_{3\alpha} n_2 V_{Carm2-0} (-2\phi_2^2 + \phi_2) \\
& + L_{2\alpha} L_3 n_3 V_{Carm3-0} (2\phi_3^2 + \phi_3)] \}
\end{aligned} \tag{2-51}$$

$$\begin{aligned}
P_2 \approx & L_\alpha^{-1} \{ T_s n_2 V_{Carm2-0} [(L_{3\alpha} n_1 V_1 + L_3 n_3 V_{Carm3-0}) (-2\phi_2^2 + \phi_2) \\
& + L_3 n_3 V_{Carm3-0} (-2\phi_3^2 - \phi_3) + 4L_3 n_3 V_{Carm3-0} \phi_2 \phi_3] \}
\end{aligned} \tag{2-52}$$

$$\begin{aligned}
P_3 \approx L_\alpha^{-1} \{ & T_s n_3 V_{Carm3-0} [L_2 n_2 V_{Carm2-0} (2\phi_2^2 - \phi_2) \\
& + (L_{2\alpha} n_1 V_1 + L_2 n_2 v_{Carm2-0}) (2\phi_3^2 + \phi_3) \\
& - 4L_2 n_2 V_{Carm2-0} \phi_2 \phi_3] \}
\end{aligned} \tag{2-53}$$

MODE 8: $\phi_3 < 0 < \phi_2$; $\phi_2 - \phi_3 > 0.5$

$$\begin{aligned}
P_1 \approx L_1^{-1} L_\alpha^{-1} \{ & T_s n_1 V_1 [L_2 L_{3\alpha} n_2 V_{Carm2-0} (-2\phi_2^2 + \phi_2) \\
& + L_{2\alpha} L_3 n_3 V_{Carm3-0} (2\phi_3^2 + \phi_3)] \}
\end{aligned} \tag{2-54}$$

$$\begin{aligned}
P_2 \approx L_\alpha^{-1} \{ & T_s n_2 V_{Carm2-0} [-2(L_{3\alpha} n_1 V_1 - L_3 n_3 V_{Carm3-0}) \phi_2^2 \\
& + (L_{3\alpha} n_1 V_1 - 3L_3 n_3 V_{Carm3-0}) \phi_2 + L_3 n_3 V_{Carm3-0} (2\phi_3^2 + 3\phi_3) \\
& - 4L_3 n_3 V_{Carm3-0} \phi_2 \phi_3 + L_3 n_2 V_{Carm2-0}] \}
\end{aligned} \tag{2-55}$$

$$\begin{aligned}
P_3 \approx L_\alpha^{-1} \{ & T_s n_3 V_{Carm3-0} [L_2 n_2 V_{Carm2-0} (-2\phi_2^2 + 3\phi_2) \\
& + 2(L_{2\alpha} n_1 V_1 - L_2 n_2 v_{Carm2-0}) \phi_3^2 \\
& + (L_{2\alpha} n_1 V_1 - 3L_2 n_2 v_{Carm2-0}) \phi_3 + 4L_2 n_2 V_{Carm2-0} \phi_2 \phi_3 \\
& - L_2 n_2 V_{Carm2-0}] \}
\end{aligned} \tag{2-56}$$

2.4 Design Considerations for Mutual Inductors and Transformer Leakage

Inductance

To confirm the accuracy of the characteristic equations, a PLECS simulation was developed. Circuit component values were chosen based upon the values from a reference experiment of a current-fed DAB [32]. Table 2 includes the parameters that were used for both the

calculations and the simulation. Note that these parameters are for an application at a higher switching frequency than the parameters found in Table 1.

Table 2: CFTAB Converter Circuit Parameters for Leakage Inductance Analysis

Variable	Parameter	Value
n_1	Primary Turns Ratio	1
n_2	Secondary Turns Ratio	1
n_3	Tertiary Turns Ratio	1
L_1	Primary Winding Inductance	20 μ H
L_2	Secondary Winding Inductance	20 μ H
L_3	Tertiary Winding Inductance	20 μ H
L_{dc}	Coupled Inductor Inductance	100 μ H
M	Mutual Inductance	80 μ H
f_s	Switching Frequency	40kHz
D_1	Primary Duty Cycle	0.5
D_2	Secondary Duty Cycle	0.525
D_3	Tertiary Duty Cycle	0.525
ϕ_2	Secondary Switching Delay (p.u.)	0.1
ϕ_3	Tertiary Switching Delay (p.u.)	0.15
V_{1DC}	Primary DC Voltage	500V
V_{2DC}	Secondary DC Voltage	525V
V_{3DC}	Tertiary DC Voltage	525V
V_{arm2}	Secondary Arm Voltage	500V
V_{arm3}	Tertiary Arm Voltage	500V
T_s	Switching Period	25 μ s

For the analysis, each arm was treated as a square wave voltage source. Note that arm₂₋₁ and arm₂₋₄ switch as a pair; likewise, arm₂₋₂ and arm₂₋₃ switch as a pair. Also, as the duty cycle of the arms extend beyond 0.5, the voltage difference waveform v_{arm2} will have zero states as if it were operating with a duty cycle below 0.5.

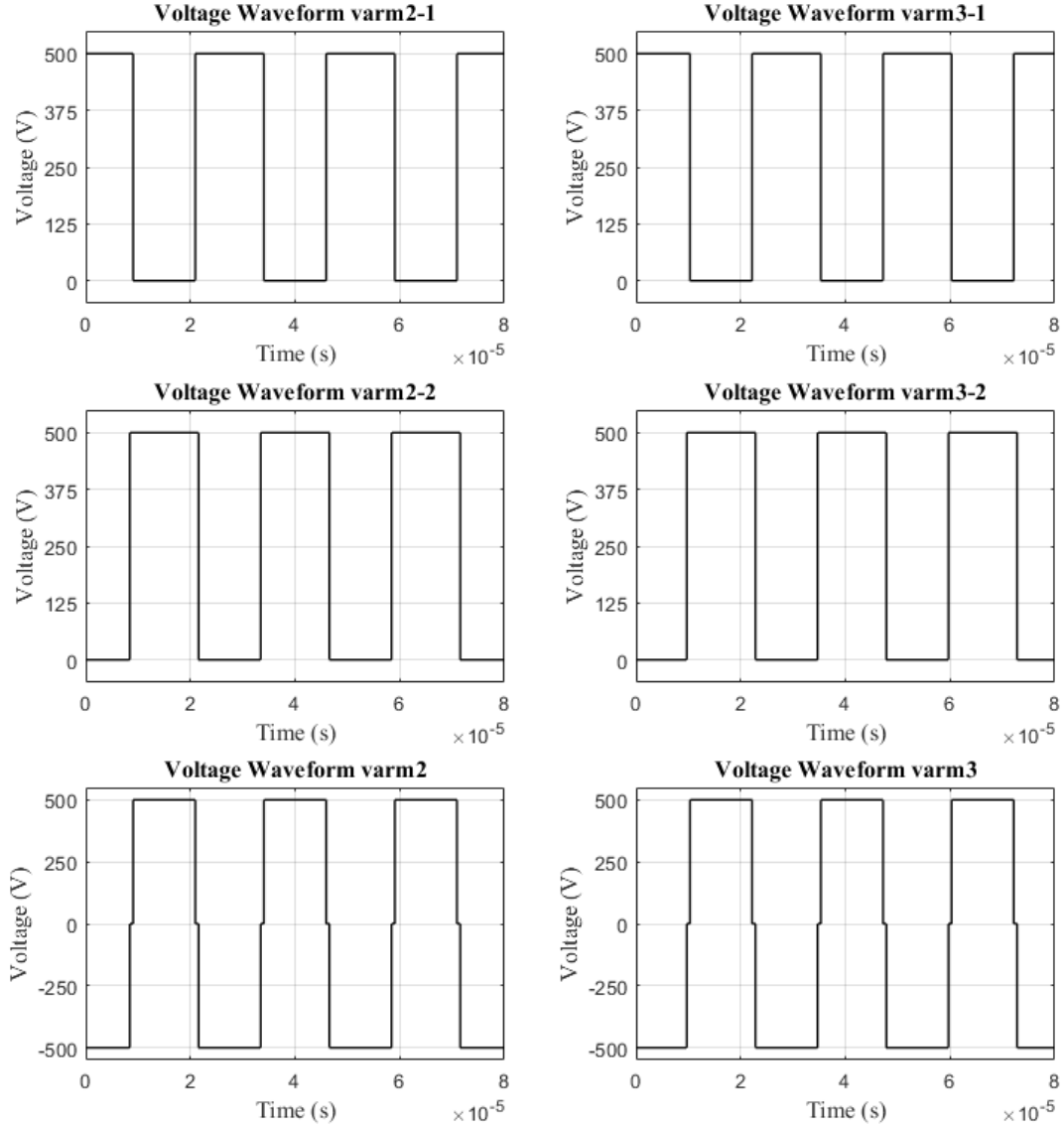


Figure 6. Individual arm voltages for each current-fed port and each port's voltage difference waveform.

Additional assumptions are made for some of the parameters. For instance, an 80% mutual coupling coefficient M was selected to determine the mutual inductance L_M . If a different value of M is chosen, port voltages v_2 and v_3 will be affected because ports 2 and 3 contain mutual inductors. An analysis of converter performance with respect to varying values of M has not been performed in this study.

For simplification of the analysis and to match the parameters with the reference experiment, the turns ratio of the transformer is kept at 1:1:1. Note that in order to maintain stable operation at an arbitrary current fed port x , the arm voltage is related to the DC voltage with

$$V_{xDC} = 2D_x V_{armx}. \quad (2-57)$$

This relationship exists to maintain the coupled inductor Volt-second balance. Deviating from this relationship will impose a DC current bias on the coupled inductors and could possibly lead to instability. In practice, this means the capacitors within the arm submodules will require cell voltage balancing to enforce a constant overall arm voltage.

The switching phase angle delays ϕ_x for the secondary and tertiary ports are selected to be different to conveniently isolate the effects of switching at each port. As shown in Figure 7, a key feature of the converter voltages v_2 and v_3 is that the voltages deviate further from an ideal square wave as the phase angle delays ϕ_x increase. Therefore, the phase angle delays were kept at relatively small values (0.1 and 0.15). This is typically acceptable in applications where the converter has been optimized for high efficiency at full load with a narrower operating range.

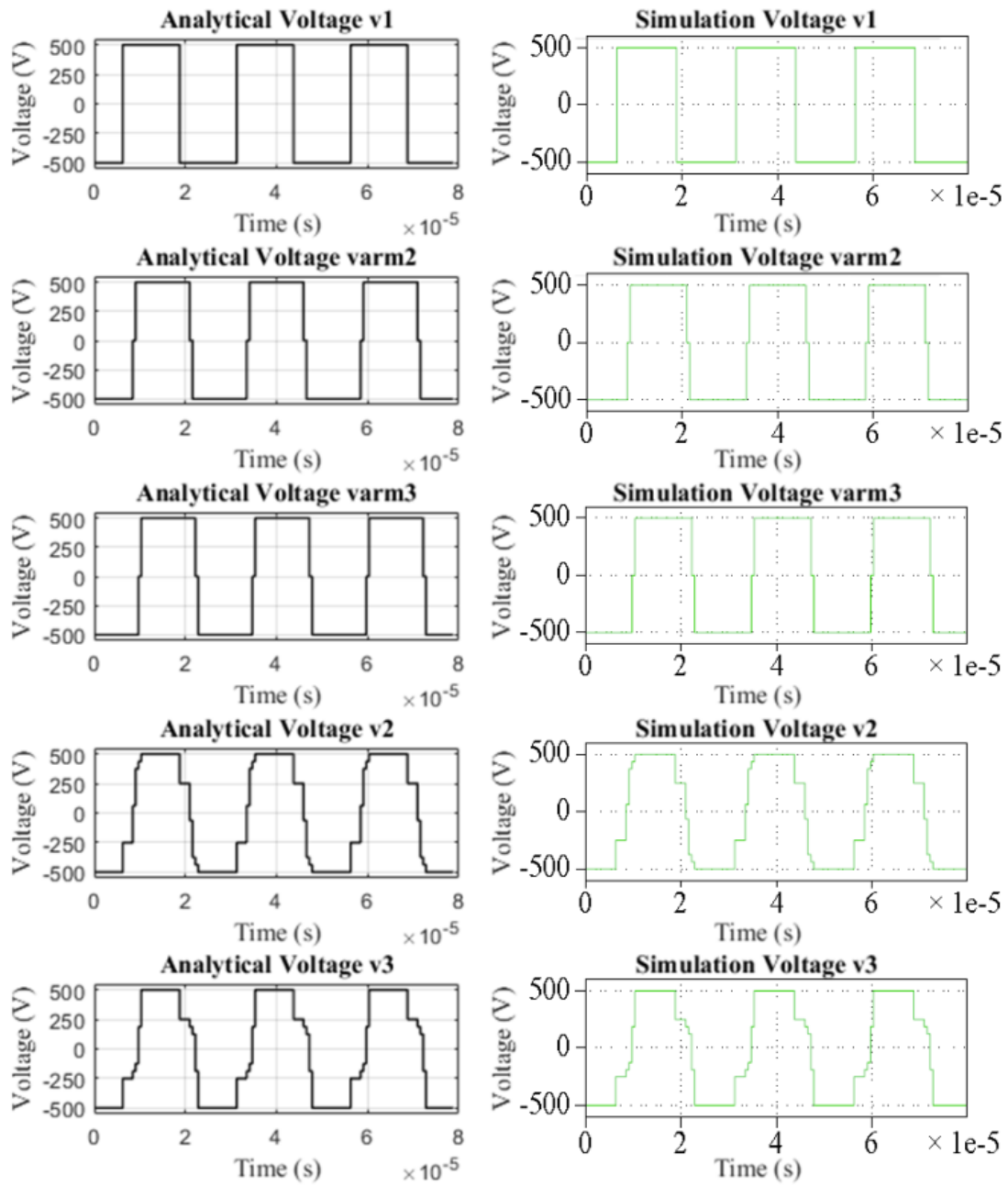


Figure 7. Analytical vs simulation waveforms for port voltages and switching waveforms.

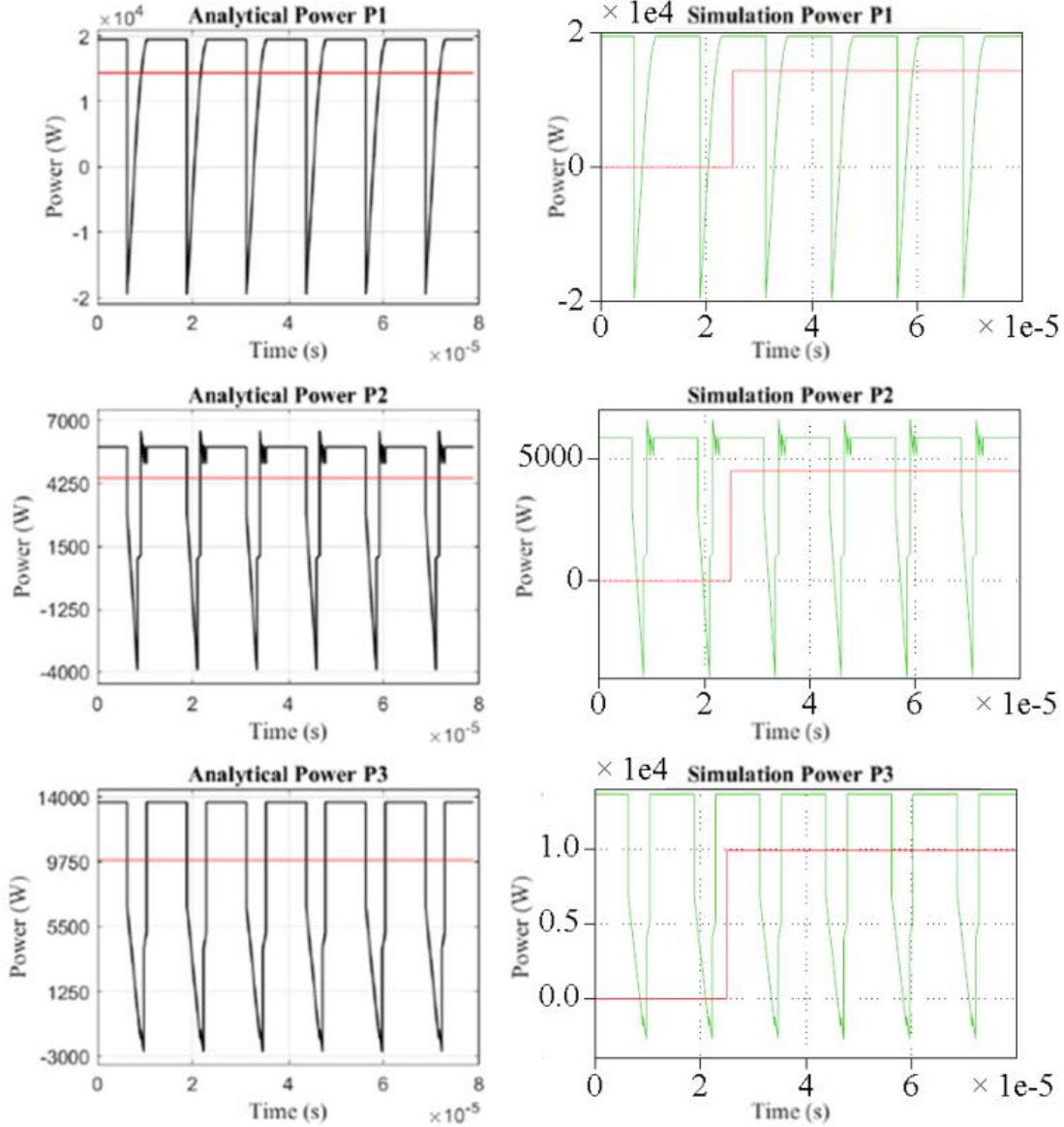


Figure 8. Analytical vs PLECS simulation waveforms for power flow at each port.

Figure 7 shows that the equations from the analyses accurately predict the behavior of the converter. By using the selected parameters, the current-fed port voltages v_2 and v_3 cannot be assumed to be square waveforms when the transformer leakage inductance value is close in magnitude to the mutual inductance values. It is also apparent that port voltages v_2 and v_3 are affected any time switching occurs at another port. Calculation of power flow through the

converter is done by applying the formula in (2-27). The resulting analytical power flow waveforms are shown in Figure 8 and confirmed with the power flow results from the simulation.

2.4.1 Discussions

Looking at the comparison between analytical and simulation voltage waveforms in Figure 7, it is confirmed that the port voltage equations accurately describe the performance of the converter. Similarly, the equations for power flow at each port are confirmed with the simulation results in Figure 8. The peak power values as well as average power (shown in red) are equivalent between the analysis and the simulation. Note that it takes one switching period for the simulation to calculate average power (half a period in this instance, due to symmetry) thus in the case of the simulation, the average power is initially zero before a switching period elapses.

A key result of these analyses is that the current-fed port voltages v_2 and v_3 deviate from an ideal square wave as the mutual inductance values ($L_{dc} - M$) are increased to values similar in magnitude to the transformer leakage inductances L_2 and L_3 . To explore this phenomenon further, the mutual inductance values ($L_{dc} - M$) were varied between 1% and 200% of the transformer leakage inductance values L_2 and L_3 . Figure 9 shows how the selection of inductor values affects the port voltage waveforms and ultimately the performance of the converter.

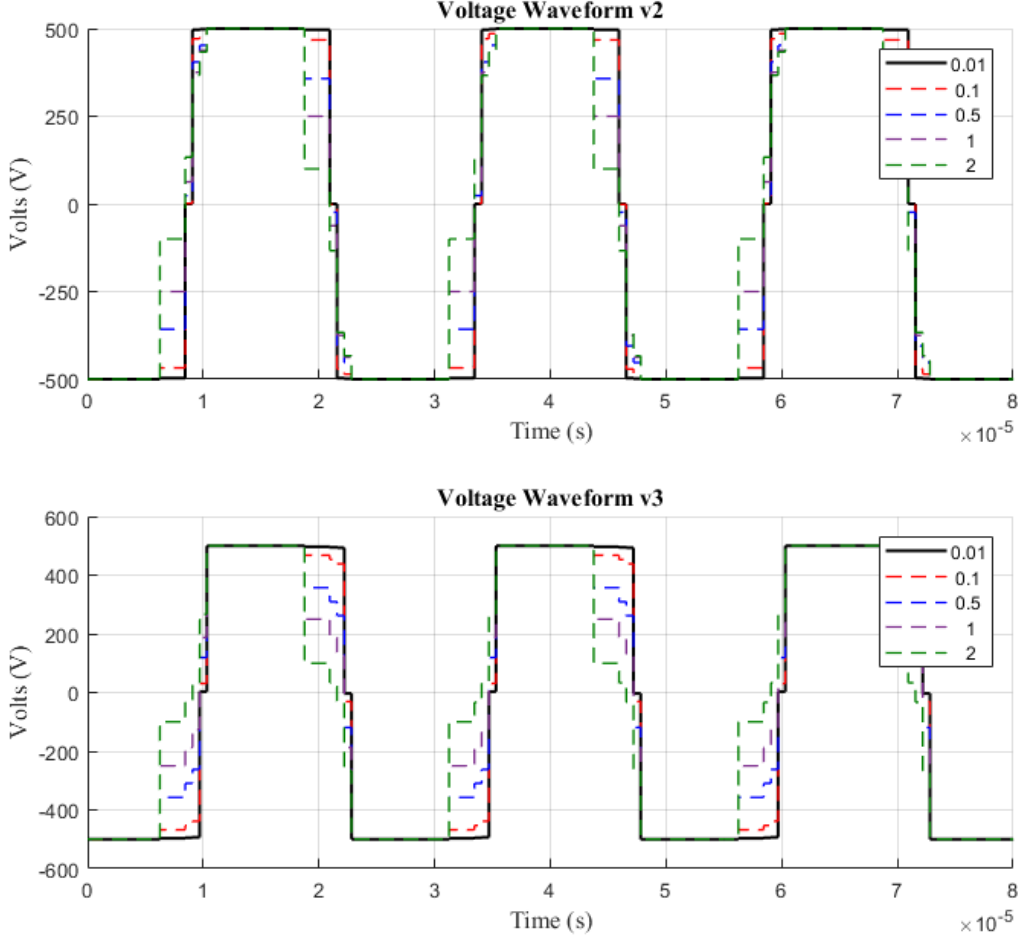


Figure 9: Current-fed port voltage waveforms v_2 and v_3 with inductance ratios $(L_{dc} - M)/L_x$ between 1% and 200% (from simulation).

When the mutual inductance values are 1% of the transformer leakage inductance values, the port voltage waveform is approximately a square wave (with zero states in accordance with the switching duty cycle). Due to the relatively short period of the zero states, each port voltage waveform can be approximated as an ideal square wave when computing power flow.

Therefore, when mutual inductance values are much lower than transformer leakage inductance values, the traditional power flow equations for voltage-fed multi-port converters as listed in [21] can be used. With the parameters listed in Table 2, power flow at the current-fed ports was computed and compared to the expected power flow from the voltage-fed power flow

equations in [21]. The results shown in Figure 10 demonstrate that as the mutual inductance ($L_{dc} - M$) increases, the current-fed ports deliver less power than the “ideal power transfer” computed from the voltage-fed power flow equations.

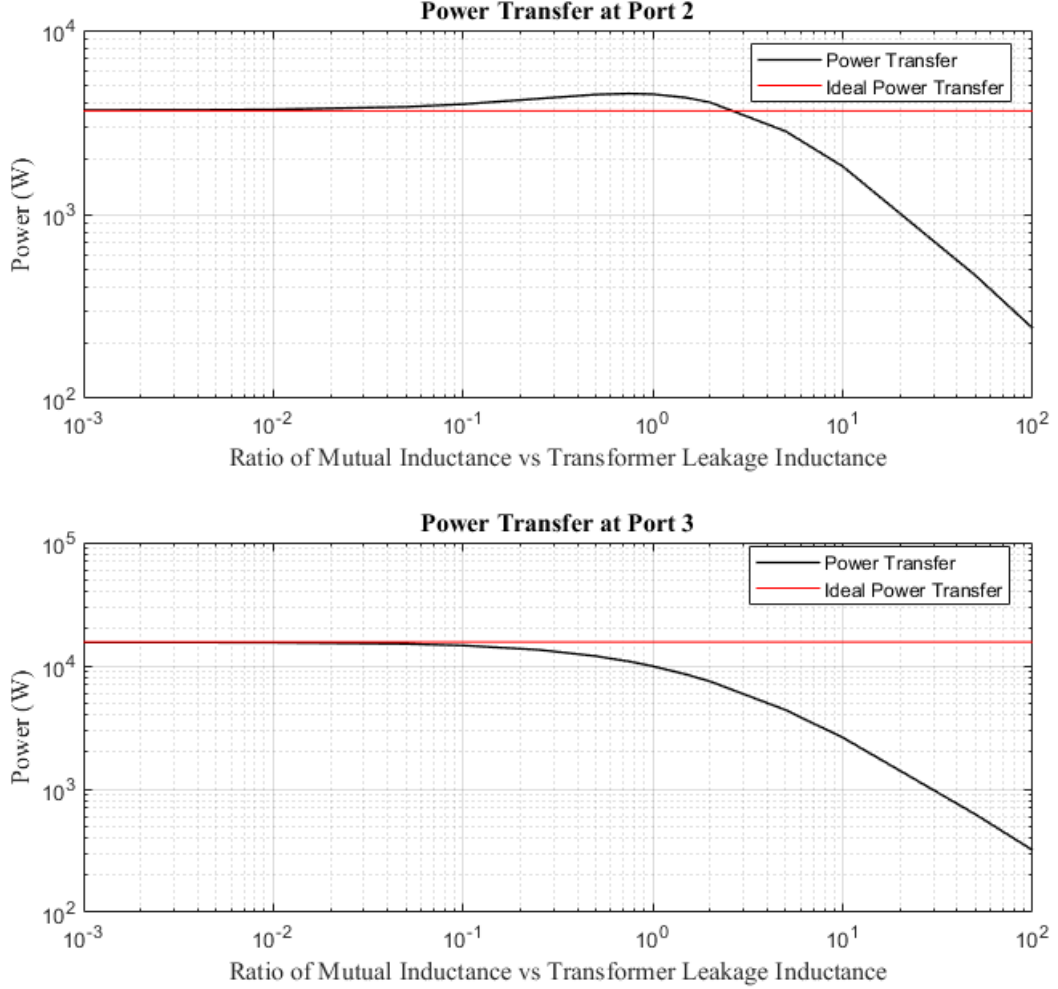


Figure 10: Power transfer at current-fed ports with respect to the inductance ratios $(L_{dc} - M)/L_x$ (from simulation).

The analyses establish characteristic equations for voltage, current, and power flow within a current-fed, multi-port converter. Waveforms were generated from the characteristic equations and confirmed with a PLECS simulation using circuit parameters from a reference experiment. Additionally, the validity of traditional power flow equations for a voltage-fed multi-port converter

were tested against the performance of the current-fed, multi-port DAB converter. The results demonstrate that under certain conditions, a current-fed port's power flow can be controlled in the same manner as a voltage-fed port.

2.5 Decoupled Control

An operational concern with converters containing multi-winding transformers is that the shared flux within the transformer will cause a change in power flow for all 3 ports when the phase shift of a single port is changed. In an IEEE multiport converter seminar in 2021, Dr. Marco Liserre stated that a load change at a first load port creates unintended power fluctuations at a second load port. The aim of this section is to propose a control method that accounts for the coupled port behavior to maintain a constant power output while another port experiences a load change.

The contribution of this section is to harness the results of the power flow analysis to propose a control strategy based on the resulting power flow equations. Since a controller for the CFTAB converter has never been proposed before, this will be a novel controller. The critical feature of the proposed control is that transient power flow conditions at one of the load ports do not affect the power flow performance at the second load port. This is because the coupled flux effects within the multi-winding transformer are predicted from the power flow analysis and compensation is incorporated within the controller. This control compensation is useful when significant load changes can create voltage disturbances at the other 2 dc ports, particularly in the case of weak grid systems like an islanded microgrid [33]. In electric vehicle applications as well, it is an important controller design metric to shield the battery port from transient disturbances

[34]. Traditionally, a decoupling matrix is used to prevent transient disturbances. However, this method requires linearization around an operating point to derive the decoupling gain matrices. The proposed control strategy will be able to achieve decoupled performance without the need to re-calculate the control laws as the operating point changes.

2.5.1 Average Power Flow Control Case Study

Deriving the power flow equations makes it possible to compute the valid operating points of (ϕ_2, ϕ_3) that will deliver a constant power output at one of the ports. Then, a trajectory of these operating points can be discovered to allow the other port to adjust power flow while maintaining constant power at the original port. To demonstrate this concept, a case study will be explored using the parameters in Table 1 for a constant 5kW load at port 3.

The circuit component values in Table 1 were substituted into (2-32)-(2-56) and the resulting power output waveforms at each port are plotted in Figure 11 for the full switching range for $-0.5 \leq \phi_2 \leq 0.5$ and $-0.5 \leq \phi_3 \leq 0.5$. The eight different modes are colored separately in the graphs to clearly show each mode. A key feature to note is that the power output at a port x trends from negative to positive for the range $-0.25 \leq \phi_x \leq 0.25$, regardless of the phase shift at the other port. This is to be expected as a typical control strategy is to independently control each port by increasing its phase shift to increase power flow to that port, and vice versa. A key result of any change in phase shift, however, is a clear change in power output at both ports. For example, if an increase at port 2 power flow is desired and ϕ_2 is increased accordingly, the power output at port 3 will certainly change as a result. The following section of this paper will describe a method of adjusting the power output at one port without affecting the power output at the other

port. As a reminder, the power output at port 1 is simply equal to the sum of the power flow to ports 2 and 3 as described in (2-2). Therefore, the power output at port 1 is also controlled by manipulating ϕ_2 and ϕ_3 .

Note that in Figure 11, the highlighted operating points (dark black) are in a flat plane at 5kW for port 3 output power while the trajectory of port 2 output power can range from approximately -10kW to 10kW. It can also be noted that the control strategy can be simplified further by restricting the operating points to $-0.25 \leq \phi_2 \leq 0.25$ and $-0.25 \leq \phi_3 \leq 0.25$ to force proportional control. This means the power output at port 2 increases as the phase angle ϕ_2 is increased (and vice versa), which makes standard feedback control well-suited to regulating the power output at Port 2 by regulating ϕ_2 . The phase shift ϕ_3 can then be computed from ϕ_2 to achieve a constant 5kW power output at port 3.

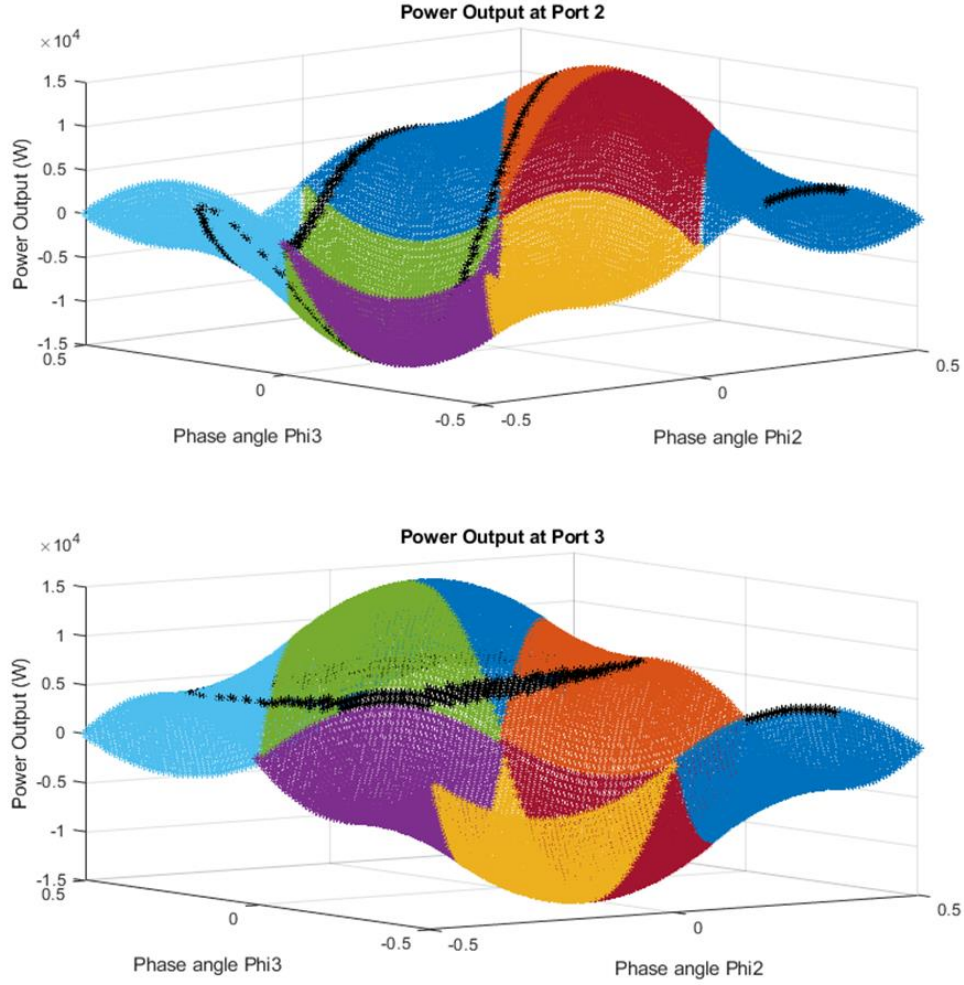


Figure 11: Power output at port 2 across the entire operating range ($-0.5 \leq \phi_2 \leq 0.5$ and $-0.5 \leq \phi_3 \leq 0.5$) (top) and Power output at port 3 across the entire operating range (bottom). Each distinct color corresponds to one of the eight operating modes as described in Table II. Port 2 and port 3 power output with 5kW power reference at port 3. Valid operating points that output 5kW at port 3 are highlighted in dark black. Note that at port 2, the power output can equal zero near the origin with power output increasing or decreasing according to the phase angle ϕ_2 .

Solving for ϕ_3 :

A relationship between the phase shifts ϕ_2 and ϕ_3 can be computed by substituting 5kW into (2-38) for Mode 2 and is given in (2-57).

$$5000 = 78125 \left(-\phi_2^2 - \frac{1}{2}\phi_2 - 3\phi_3^2 + \frac{3}{2}\phi_3 + 2\phi_2\phi_3 \right) \quad (2-58)$$

Then, solving for ϕ_3 :

$$\phi_3 = -\phi_2 \pm \frac{1}{250} \sqrt{125000\phi_2^2 - 125000\phi_2 + \frac{124625}{4}} + \frac{3}{4} \quad (2-59)$$

From (2-58), a constant power output of 5kW is produced at port 3 regardless of the value of ϕ_2 . As ϕ_2 changes, ϕ_3 will be computed accordingly to maintain the desired output of P_3

2.5.2 Control Hardware-in-the-Loop Experiment

For the case study, port 3 was treated as a constant power load of 5kW. The decoupled control strategy that will be described below allows the power at port 2 to swing between 0W and upwards of 7kW. To confirm that the proposed control strategy was viable, a Typhoon HIL 402 real time digital simulator was used to emulate the converter and grid behavior in real time. The converter control was installed onto a TI 28379 controller. A Typhoon DSP180 interface was used to connect the controller input and output signals to the Typhoon HIL 402. This control hardware-in-the-loop (CHIL) experiment successfully demonstrated steady-state stability of the simulated converter when using the external controller. Figure 12 shows the CHIL experimental setup.

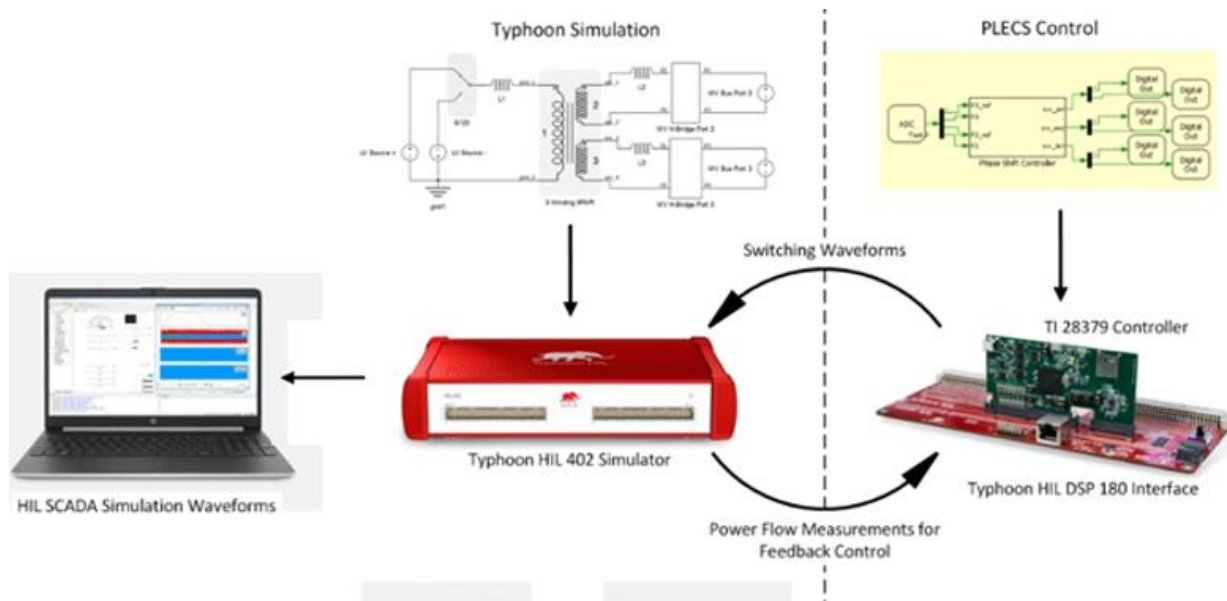


Figure 12: Typhoon HIL Control Hardware-in-the-Loop Experimental Setup

2.5.2.1 Typhoon HIL Schematic and SCADA Panel

The circuit topology in Figure 3 was designed within Typhoon HIL's schematic editor. The Typhoon model is shown below in Figure 13. The component values are designed per the converter parameters in Table 1. Switch S123 generates a square waveform across the primary transformer windings.

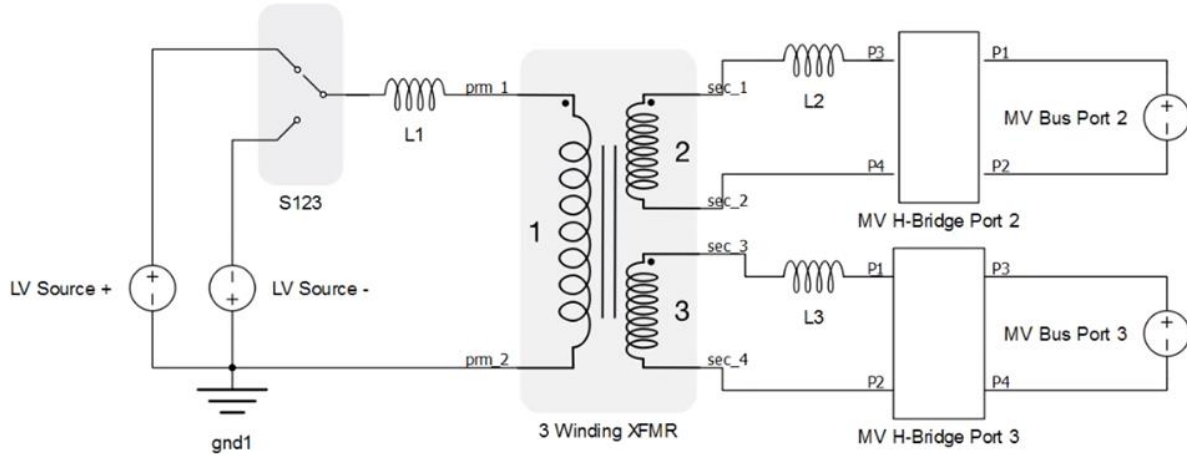


Figure 13: Typhoon HIL model of a 3-bus network (LV-MV-MV) with 3-port interfacing converter. Switch S123 is used to generate a square wave at the primary port, while the MV H-bridges contain the mutual inductor pairs as well as the switching arms.

The MV H-Bridge ports contain the switches and mutual inductor pairs according to Figure 3. The switches are set within the Typhoon HIL simulation software to be controlled by an external digital signal produced by the TI 28379 controller. In the SCADA system the values of P_2 and P_3 are set as analog output reference signals to the controller.

2.5.2.2 Texas Instruments Controller

The controller is programmed by flashing PLECS control blocks onto the controller using the coder compiler software package. The PLECS control blocks are shown below in Figure 14 through Figure 16.

Figure 14 is the overall control system that receives analog inputs from the Typhoon HIL simulation and uses those four signals to generate the phase shift control strategy. The result of the control is 6 digital output signals (2 square wave forms per port) that are sent to the switches at each port. Looking into the Phase Shift Controller block gives Figure 15.

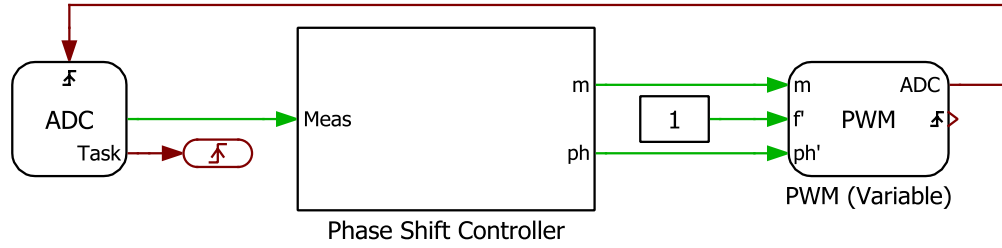


Figure 14: PLECS phase-shift controller using TI C2000 target blocks. The ADC block is the analog power flow measurements coming from the Typhoon HIL simulation. The PWM block sends switching signals back to the simulation.

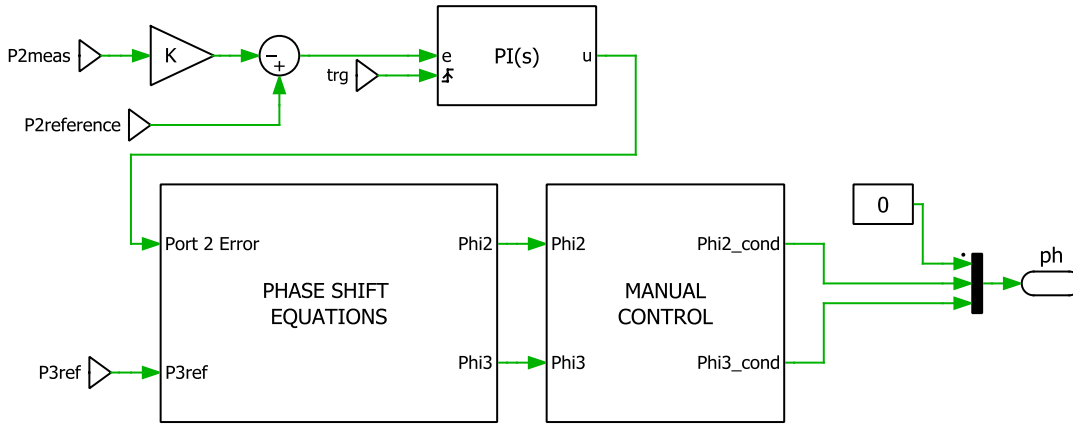


Figure 15: Control logic for phase-shift control. Measured power flow at each port is compared to the desired reference. The error signals are used as an input to the phase shift equations. The output modulation signals are then used to generate the gate switching signals.

Figure 15 compares the reference values set by the user in Typhoon HIL SCADA to the average power output of the Typhoon HIL simulation. The error signals are then passed into a phase shift equations block, which generates modulation values for the secondary and tertiary ports. The modulation signals are passed into standard phase shift PWM blocks, which uses a triangular carrier wave and waveform crossing detection to generate the switching signals for the primary, secondary, and tertiary ports of the converter. The phase shift equations are designed specifically to maintain a power output of 5kW at the tertiary port. Figure 16 shows the details of the phase shift equations block. ϕ_3 is generated from the value of ϕ_2 using (2-58). Note the zero-

order hold blocks throughout this control are put in place to ensure that the phase shift is not updated until a full switching cycle is complete.

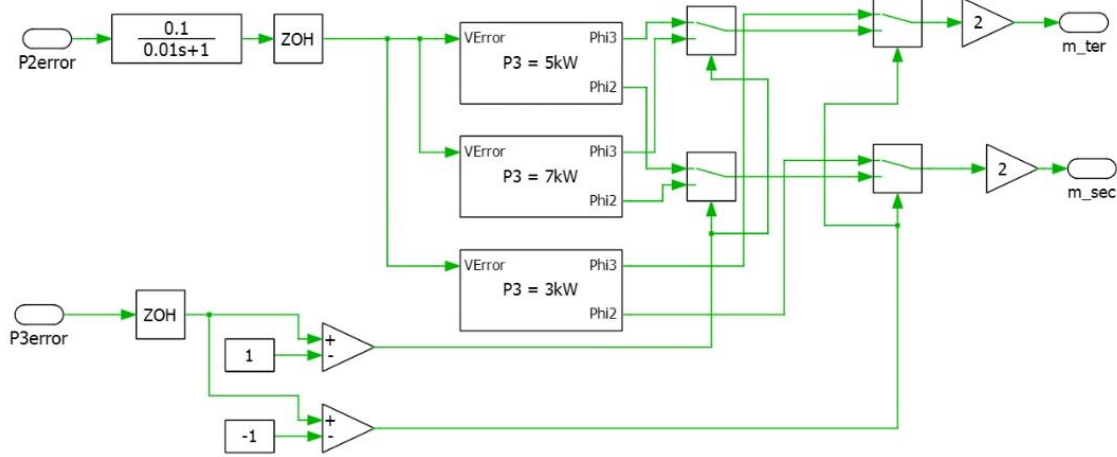


Figure 16: Control blocks for selecting the power output at port 3. The power error signals are used to generate a modulation signal to ramp up, down, or maintain output power at each port.

The controller receives a power reference signal for each port, as well as the measured power signal output from the Typhoon HIL simulation. The controller takes the difference of P_3 from the reference value to determine which equation to use. In this case study, if $P_3 < 5kW$, then the control will attempt to output a higher power (7kW) until 5kW is reached. Likewise, if $P_3 > 5kW$, the control will output a lower power (3kW) until 5kW is reached. Note that this control was limited to only unidirectional power flow. However, the control can be extended to the full range of operation using the computed power flow equations in (2-32)-(2-56). Also, this control strategy can be adapted to instead control the bus voltage or to control the output current at a port instead of the average power.

2.5.2.3 Performance of Real Time Digital Simulation

The results of the C-HIL experiment are shown in Figure 17 and Figure 18. The primary source feeds a continuous 5kW to the constant power load at port 3. Initially, port 2 is disabled. When a 5kW demand is activated at port 2, the power output at port 3 remains unaffected. Figure 11 is provided to 1) verify stable steady-state operation, 2) verify transient load conditions at port 2 do not affect the power flow at port 3 and 3) stable steady-state operation.

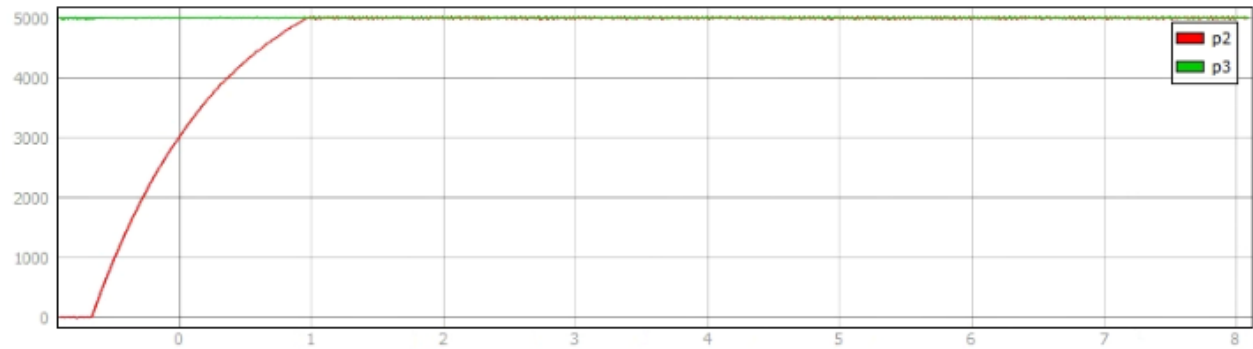


Figure 17: Simulated CFTAB power output waveforms at ports 2 and 3 as the load for port 2 changes from 0kW to 5kW. Note that port 3 power (p3) remains unaffected by the load change at port 2.

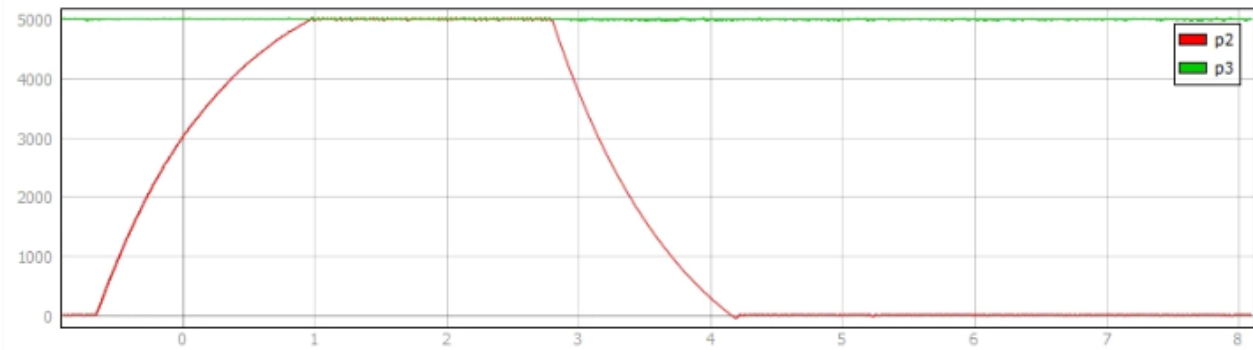


Figure 18: Quick turn-on then turn-off of the load at port 2.

2.6 Experimental Prototype

This section describes the modifications made to an existing triple active bridge converter test bed to verify the proposed control from the earlier sections. The test bed setup is described, as well as the modifications made to perform the hardware experiment. The resulting waveforms conclude this section.

2.6.1 Control Card Setup

The PLECS controller was downloaded to a Texas Instruments F28335 control card using a USB probe interface and the PLECS TI C2000 blockset. The F28335 controller was interfaced with the converter via a TMS320F28335 evaluation board. Digital outputs and analog inputs were buffered using op amps to introduce high impedance between the control card and the converter. This prevents common mode noise generated by the converter from affecting the F28335 control card.

The USB probe interface allowed continuous communication between the F28335 control card and the PC through the PLECS coder external mode. By utilizing the external mode, the PLECS model was able to display the analog input signals as they were read by the control card. This allowed for proper scaling of the analog input signals and easy troubleshooting of the controller during operation.

Figure 19 shows the control card, launchpad, and buffer board. The buffer board circuitry was designed such that a high impedance op-amp network was between the control card and the converter power electronics. The purpose of the buffer board is to prevent common-mode noise from reaching the control card as well as provide an amplified output to condition the gate driver

switching signals. In Figure 19, the power supply delivers the supply voltage to the op-amp circuits. The square wave gate driver signals for all 3 ports can be seen in the oscilloscope. When in operation, the controller will phase shift ports 2 and 3 gate drive signals with respect to port 1 to achieve the desired power output.

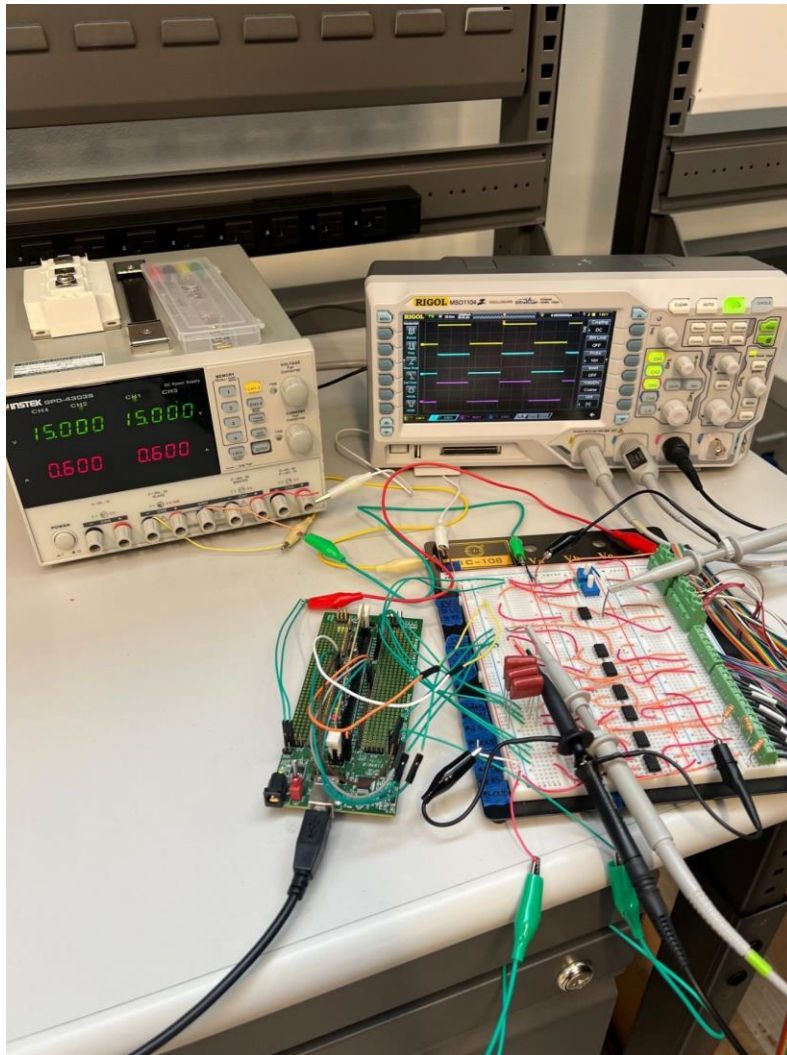


Figure 19: Control Card Launchpad and Buffer Board Circuit

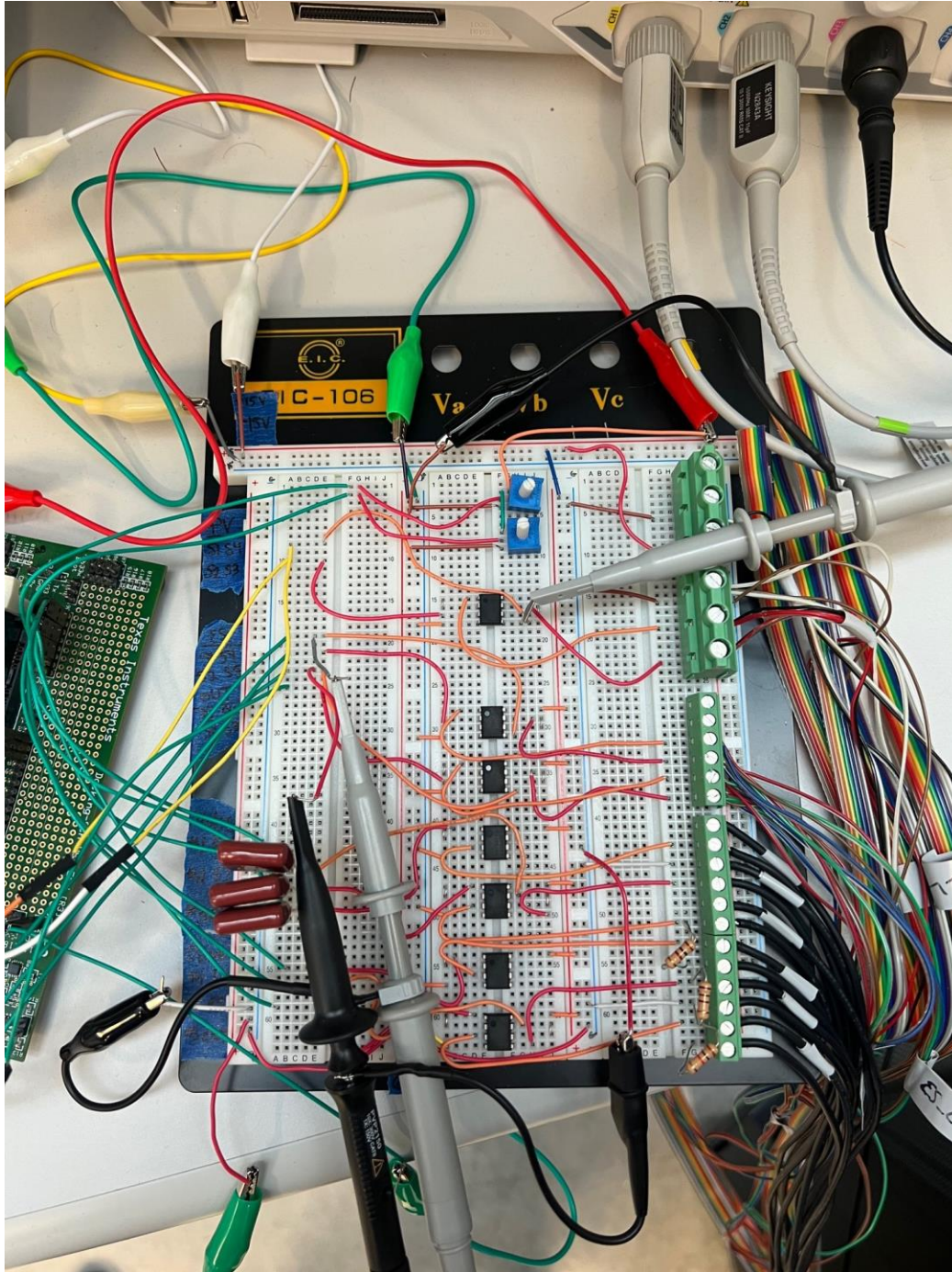


Figure 20: Buffer Board Circuit

Figure 20 shows the buffer board circuit. The buffer board was originally prototyped on a breadboard, despite the stray inductance associated with the numerous wires. Work is already underway to create a second generation buffer board that is manufactured on a printed circuit

board. In the circuit, the top left pair of wires are analog input voltages sent from the output of the potentiometer. The controller will read those analog inputs as reference signals (either bus voltage reference or bus output power reference). The user can dynamically tune the potentiometer to achieve a change in the reference signal. There are additional digital output signals from the control card sent to the gate driver board for the gate driver signals. Those signals are each passed through an op-amp to condition the signal to be used as a gate drive signal. The terminal blocks on the top right are gate driver power and switching signals to the gate driver boards. The terminal blocks on the bottom right are sensor outputs for voltage and current. Those signals are passed through the op-amps as well. The capacitors on the bottom left are to filter out high frequency noise from the voltage sensors before sending the analog signal to the control card as an analog input. The current sensors have much less noise and therefore do not require filtering capacitors.

2.6.2 Test Bed Parameters

A triple active bridge converter prototype was donated from EATON to the University of Pittsburgh's Energy Innovation Center. This converter was a product of the multi-group initiative for the DOE SuNLaMP project. The converter components are rated for 1kV and 50kW using 1200V CREE SiC MOSFET half bridges as the switching devices. However, due to infrastructure limitations of the power supply and loads of the test bed, a 150V, 1kW test was implemented for validation of the control. A picture of the converter setup is shown in Figure 21, and the operating specifications of the converter are given in Table 3. Further information about the tab converter test bed can be found in the following references [35], [36].

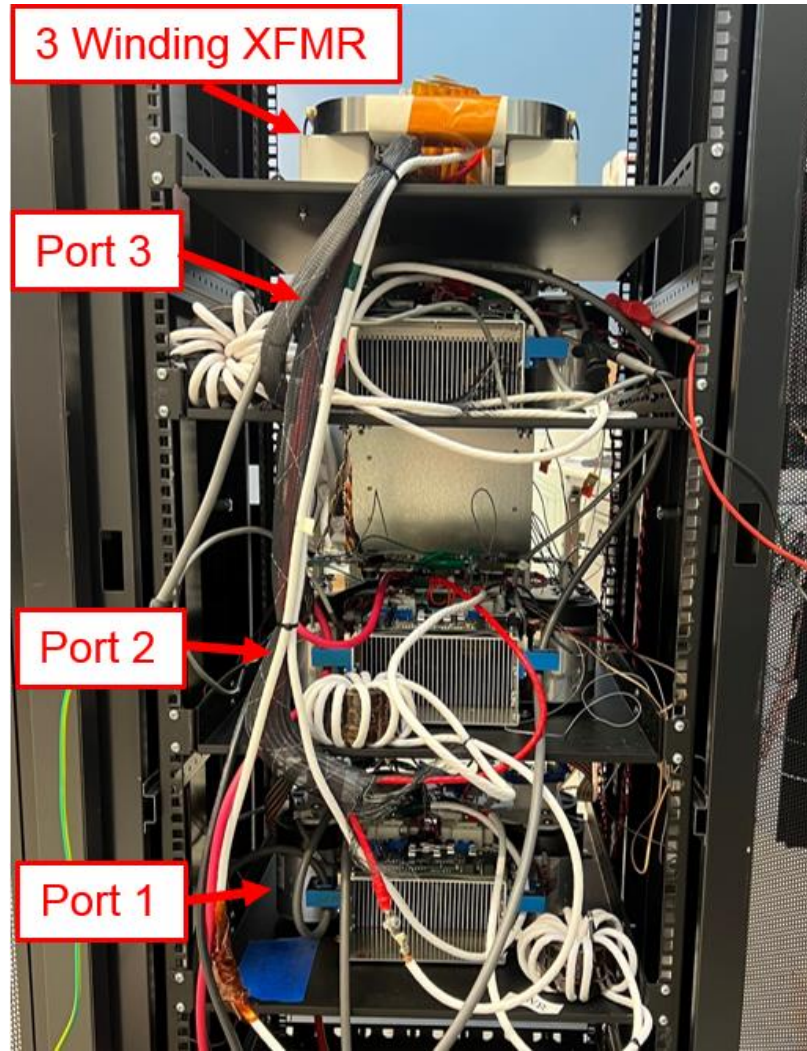


Figure 21: 50kW 3 Port Dual Active Bridge Converter

Table 3: Parameters for 3 Port Converter Prototype

Max. Output Power (KW)	50
Max. Output DC Voltage (V)	1000
PV Input range (V)	550 – 1000
Nominal PV MPPT Voltage (V)	800
ES Voltage Range (V)	500-600
Nominal ES Voltage (V)	600
Max. Output Current (A)	50A
Max. PV Input Current (A)	100A
Max. ES Input Current (A)	50A
Nominal Switching Frequency (Hz)	10,000

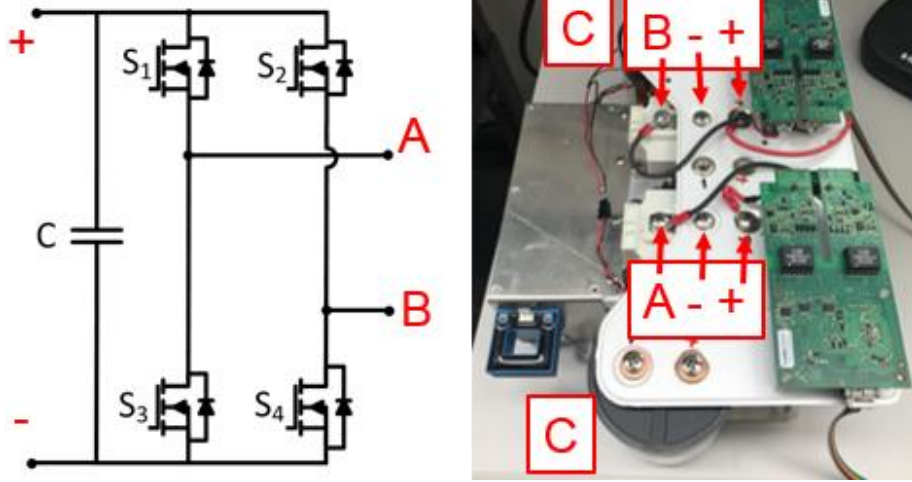


Figure 22: Single H-Bridge Schematic (Left) and Physical Layout with SiC Modules and Mounted Gate Driver Boards (Right)

Figure 22 shows the layout of a single H bridge within the test bed. The H bridge is comprised of heat sink with a current sensor mounted on the side. The bus capacitors and SiC MOSFETs are also mounted onto the heat sink. A bus bar plane is connected to the MOSFETs and capacitors. Finally, the gate driver boards are mounted with standoffs above the bus plane. The ac and dc terminals are labeled in Figure 22.

2.6.3 Experimental Setup

One key difference between the tab converter within the existing test bed and the current-fed tab converter discussed in earlier sections is the absence of the mutual inductor pairs at the current-fed ports. As a result, the proposed controller was re-derived using the techniques mentioned in Section 2.3—this time for a voltage-fed tab converter topology. The successful implementation of the proposed controller highlights the controller’s flexibility for use within voltage-fed 3-port converter topologies in addition to the original current-fed design. The goal of

this experiment is to demonstrate stable operation of the control on a physical system. The proposed operating parameters for the experiment are given in Table 4.

Table 4: Operating Parameters for 3 Port DAB Converter Experiment

Variable	Parameter	Value
V_{1DC}	Primary DC Voltage	150V
V_{2DC}	Secondary DC Voltage	75V
V_{3DC}	Tertiary DC Voltage	50V
n_1	Primary Turns Ratio	12
n_2	Secondary Turns Ratio	9
n_3	Tertiary Turns Ratio	15
L_1	Primary Winding Inductance	44 μ H
L_2	Secondary Winding Inductance	44 μ H
L_3	Tertiary Winding Inductance	72 μ H
f_s	Switching Frequency	10kHz
D_1, D_2, D_3	Switching Duty Cycles	0.5
R_{Load2}	Secondary Load	13.7 Ω
R_{Load3}	Tertiary Load	8.0 Ω

This experiment was performed at the test bed at the University of Pittsburgh's Energy Innovation Center. The test bed details are shown in Figure 23 and Figure 24. A 500V, 1kW Ametek power supply was used as the source. 2kW resistive loads were used as fixed loads. A few loads were placed in parallel and connected to the converter with a switch and are shown in Figure 23. Those switched loads allowed the converter to be tested under a load step condition. The power supply used in the experiment is shown in Figure 24.



Figure 23:Resistive Load Setup for TAB Test Bed



Figure 24: TAB Test Bed Power Supply

2.6.4 Experimental Results

The first step in the experimental operation of the TAB converter was to observe the ac switching waveforms, shown in Fig. 14. Port 1 was confirmed to be a $\pm 150\text{V}$ square wave, but was not included in the scope screenshot due to a lack of a 3rd high voltage probe. Likewise, the test bed had a single current probe, which is why port 2 current is the only current displayed in Fig. 14. Port 2 voltage, in purple, had ringing during transients up to about 85V peak before settling into a $\pm 75\text{V}$ square waveform; this was a predictable amount of ringing considering the converter is rated for much higher voltage and power operating conditions (up to 1kV and 50kW). Port 2 current, in blue, has a triangular shape and ranges between $\pm 20\text{A}$. The ac voltage at port 3 (orange) has significant non-ideal transient behavior. Despite being a $\pm 50\text{V}$ square waveform, the

overshoot reaches to approximately +125V. Likewise, the negative transient has a ‘bounce’ in voltage which brings the voltage back to 0V before settling to -50V. The results suggest a few improvements can be made to the test bed setup in future work, but ultimately did not prevent the experimental controller demonstration. For example, the ringing seen in the Figure 25 port 2 and port 3 ac voltages will occasionally create noise on the dc buses at ports 2 and 3. Future modifications to resolve the ringing issue could be obtaining a higher rated test bed power supply to reach the converter’s rated power, operating the load voltages closer to the transformer turns ratio of 12:9:15, and using loads rated for higher power dissipation.

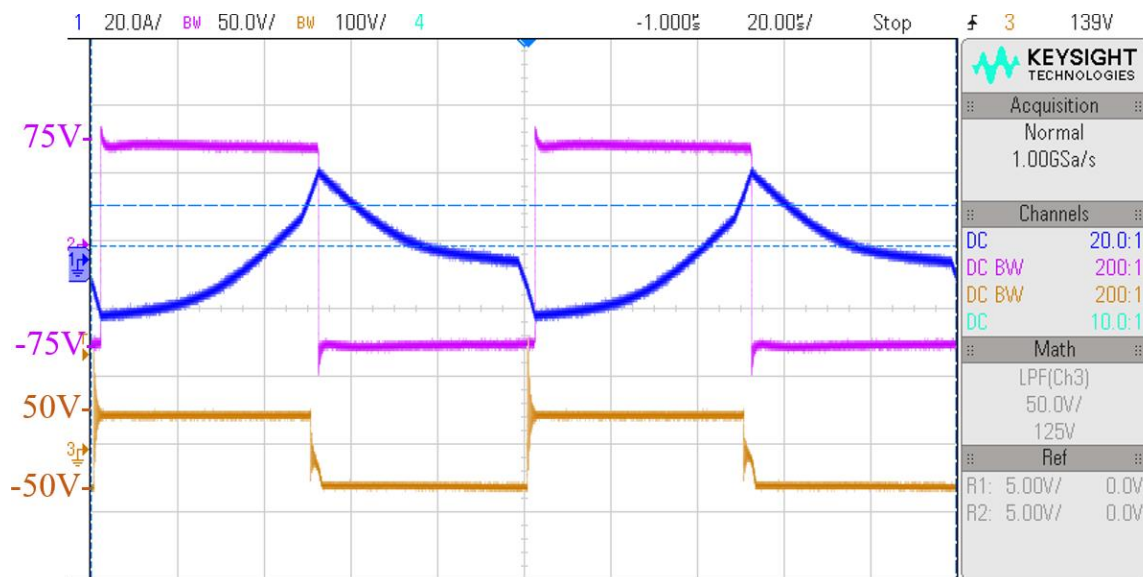


Figure 25: AC switching waveforms. Port 2 Voltage (Purple), Port 2 Current (Blue), and Port 3 Voltage (Orange). Port 1 Voltage, which is $\pm 150\text{V}$, is not shown.

After evaluating the ac waveforms of the converter, the steady-state stability of the dc bus voltages were confirmed. Also, the transient behavior of the dc bus voltages were studied. The converter was operated with a traditional PI controller as a reference, and then operated again with the proposed power flow controller. The waveforms for the experiment are given below in Figure 26.

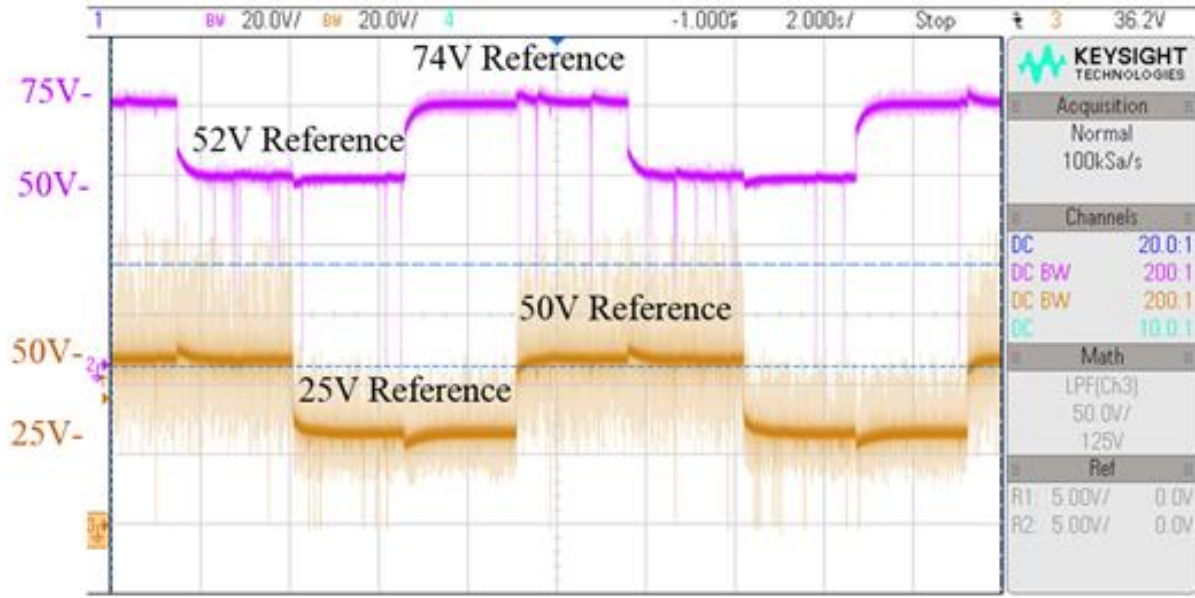
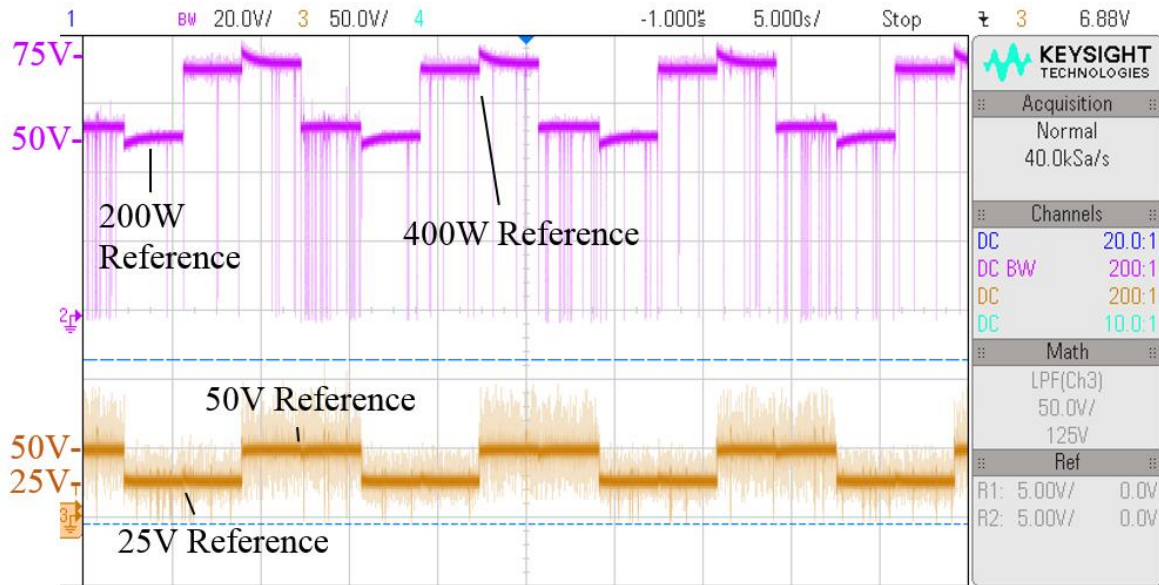


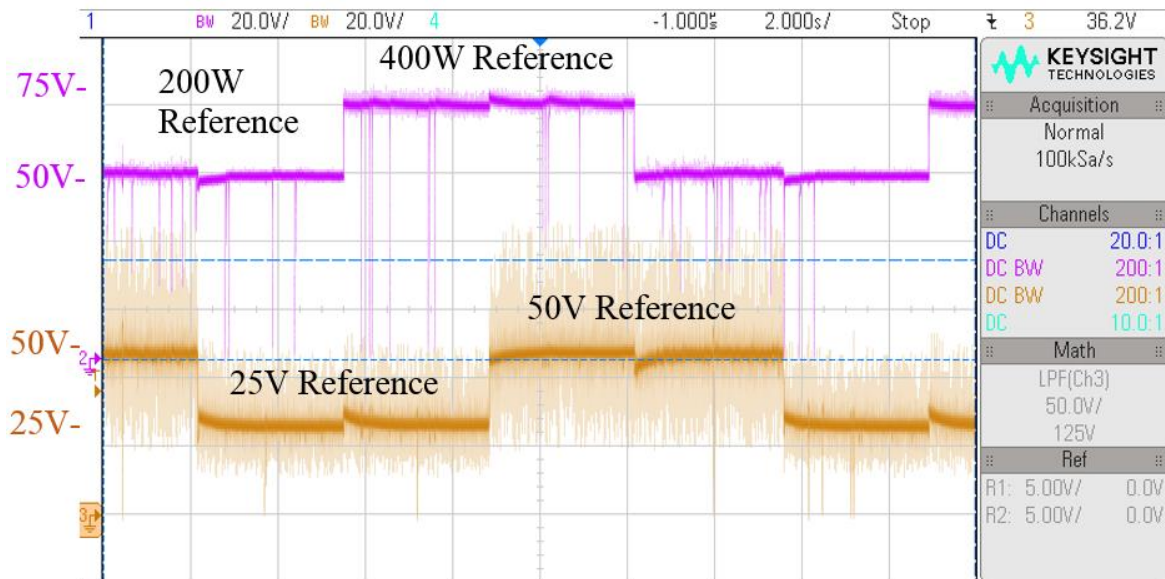
Figure 26: Voltage reference changes for port 2 dc bus voltage (purple) and port 3 dc bus voltage (orange) with PI controller on both ports 2 and 3 (reference case). Port 2 shows the transition between a 200W reference and 400W reference while port 3 shows the transition between a 25V reference and 50V reference.

Figure 26 shows the results of PI dc bus voltage regulation at ports 2 and 3. The PI control was tuned to have a critically damped response with no overshoot. The figure shows port 2 tracking a 52V reference (200W) with a reference transition to 74V (400W) and port 3 tracking a 25V reference with a reference transition to 50V. Figure 27 shows the results of the power flow controller at port 2 with a PI controller at port 3. The figure shows port 2 tracking a 200W reference with a reference transition to 400W and port 3 tracking a 25V reference with a reference transition to 50V. The voltage references were continually changed in this experiment since part of the motivation for developing the power flow control strategy was to operate during varying bus voltages. One final thing to note is the transient voltage drops in the dc bus voltage waveforms. This is a disturbance caused by the converter operation and not due to the control. In future work, ringing at the load ports for the test bed will need to be suppressed to prevent this transient discharging of the dc bus capacitors.

Figure 27 demonstrates stable operation of the power flow controller at port 2. Port 2 was selected instead of port 3 for the power flow controller because, due to its lower inductance, port 2 was more susceptible to experiencing coupled transients due to a load change at port 3. One key requirement for correctly tracking the power reference at port 2 is to have exact parameter information for the inductance values of the transformer. If not, the output power at port 2 will not accurately track the power reference. Figure 27(a) shows the performance of the controller using the inductance values from Table II, before tuning. Note how the steady-state bus voltage at port 2 changes with the bus voltage at port 3. Figure 27(b) shows the performance of the controller after manually tuning the inductance values within the control until the power reference was properly tracked at port 2, regardless of the bus voltage at port 3. Finally, after tuning the control, an outer PI control loop was added to increase/decrease the input into the controller if the measured power output deviated from the reference.



(a)



(b)

Figure 27: Port 2 power flow control before tuning (a) and after tuning (b). Port 2 DC Bus Voltage (Purple) and Port 3 DC Bus Voltage (Orange) with proposed power flow controller on port 2 and PI controller on port 3. Port 2 shows the transition between a 200W reference and 400W reference (with a resistive load) while Port 3 shows the transition between a 25V reference and 50V reference.

While the RTDS experiment was able to both demonstrate stable operation of the controller as well as compensation to eliminate voltage disturbances, a key gap in this test bed experiment is the inability to implement a large enough load change to create a voltage disturbance. This scenario requires a power supply and loads rated for the 50kW converter. However, despite not being able to generate a significant voltage sag during a load change, the stability of the power flow controller can still be confirmed when comparing Figure 26 and Figure 27. The proposed power flow controller in Figure 27 achieves similar steady-state performance to the PI controller in Figure 26.

2.7 Ring Bus implementation of Back-to-Back 3-Port Converters

The purpose of this section is to use the independent control described in previous sections to control the output power flow at each MVDC port. Ultimately, this converter topology will enable a redundant power flow path within a back-to-back network. The control will allow one port to rapidly change its power output without creating a disturbance at the other MVDC port. A PLECS simulation was created to verify stable operation of the converter using the coupled control strategy. After achieving stable steady-state performance in a single converter application in the previous sections, this section studies two converters were placed in a back-to-back configuration to create a small ring bus architecture. This section demonstrates the ability to create a redundant power flow path using two converters.

2.7.1 Validation of Network Control Using PLECS

A PLECS simulation was created to verify the accuracy of the average power equations and to confirm the control can achieve the desired power flow at the load ports. Since the converter controller operates to produce constant power output at port 3 based on the derived equations, the converter will not yield the expected power output if the equations are inaccurate. Thus, if the desired power output is achieved, then the average power equations are indeed accurate. The circuit schematic for the converter is shown in Figure 28.

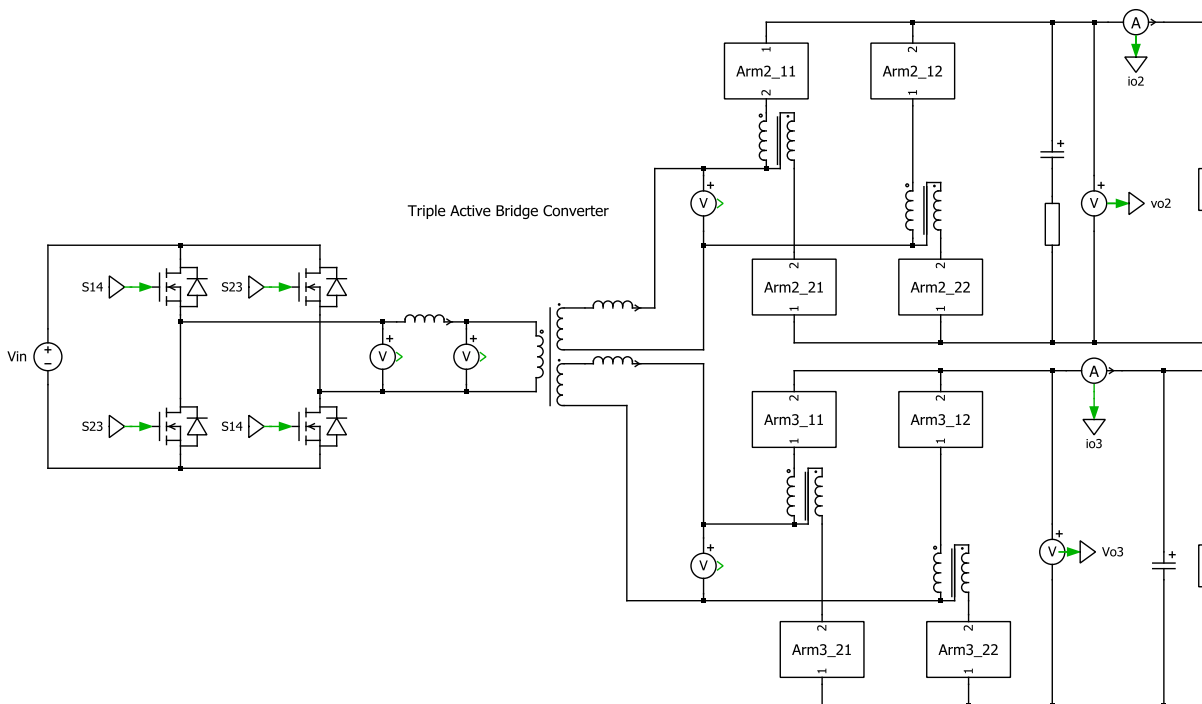


Figure 28: PLECS Simulation Model of CF3P-DAB Converter

The primary voltage source is a LVDC bus. The LVDC switches are in an H-Bridge configuration. The load ports of the converter are MVDC buses. The MVDC switching devices are switched cells in a stacked configuration, and the stacked submodules are called arms; for simplicity however, the model represents the arm voltage as an ideal voltage source that can be

switched in series or bypassed. The mutual inductor pairs are placed at each end of the transformer MV winding.

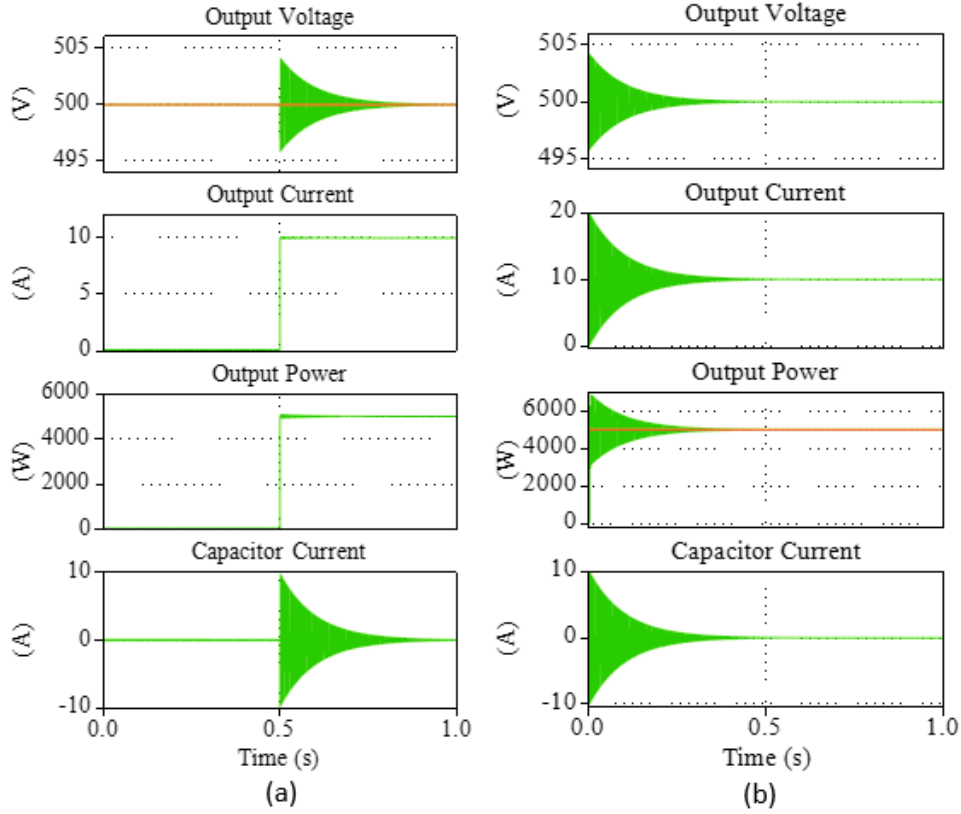


Figure 29: Output waveforms at (a) the secondary port during a load change from 0W to 5kW and (b) the tertiary port maintaining a constant 5kW load.

To confirm the accuracy of the derived average power waveforms, open loop control was used, and the average power output was checked against the predicted power output. For simplicity of closed loop control strategy, the simulation was run only on mode 1. However, since the average power equations were confirmed for all operating modes, the same approach will work for any mode and power flow direction. The key benefit to this coupled control strategy is that the load at one port can swing dramatically without affecting the power output at the second load port. To demonstrate this, Figure 29 shows that the introduction of a 5kW load to port 2 at 0.5s will have no effect on the power output at port 3.

2.7.2 PLECS Simulation of Back-to-Back Converters

One of the key benefits to a three-port converter is the ability to actively reconfigure a network using converter control. In Figure 30, the example ring network is created to feed power to a temporary, but critical load. For simplicity of keeping the lookup table-based control in only one mode, the bidirectionality of the converters was not demonstrated in this paper. Instead, the power is split equally between the two DC buses and is sent to the load. However, if the entire operating range is desired, the results shown in Figure 11 and analysis in previous sections can be used to create control for the entire operating range of the converter. In that case, a single DC bus could feed the load and the second bus would act as a standby bus.

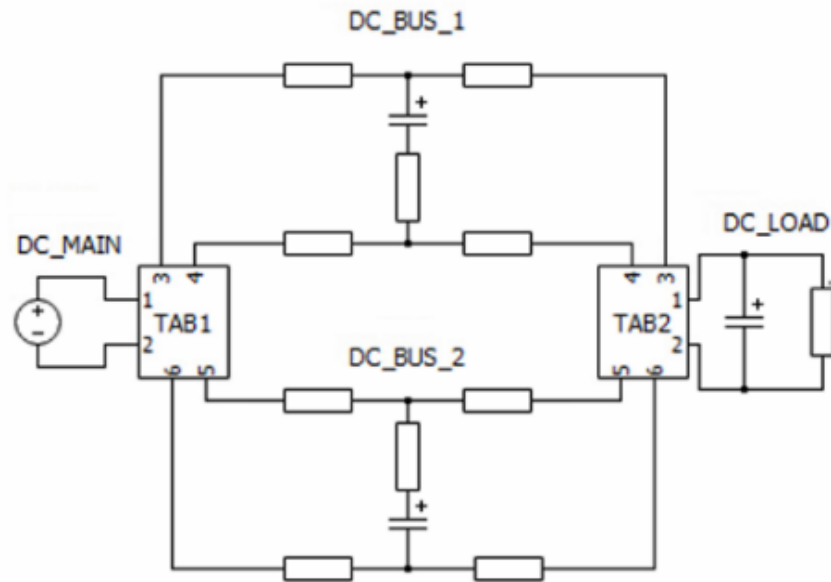


Figure 30: PLECS Simulation Model of Back-to-Back CFMP-DAB Converters.

Shown in Figure 31 are the results of the PLECS simulation for the ring network. The load is activated at $t = 0$, and the converters feed half of the power along each bus to deliver the required power to the load. Converter 1 delivers a constant 5kW through DC bus 2 while regulating the

capacitor voltage at DC bus 1. Conversely, converter 2 absorbs a constant 5kW from DC bus 1 while regulating the capacitor voltage at DC bus 2. After reaching steady state, the converters feed power to the load until the load is deactivated at $t = 0.25\text{s}$.

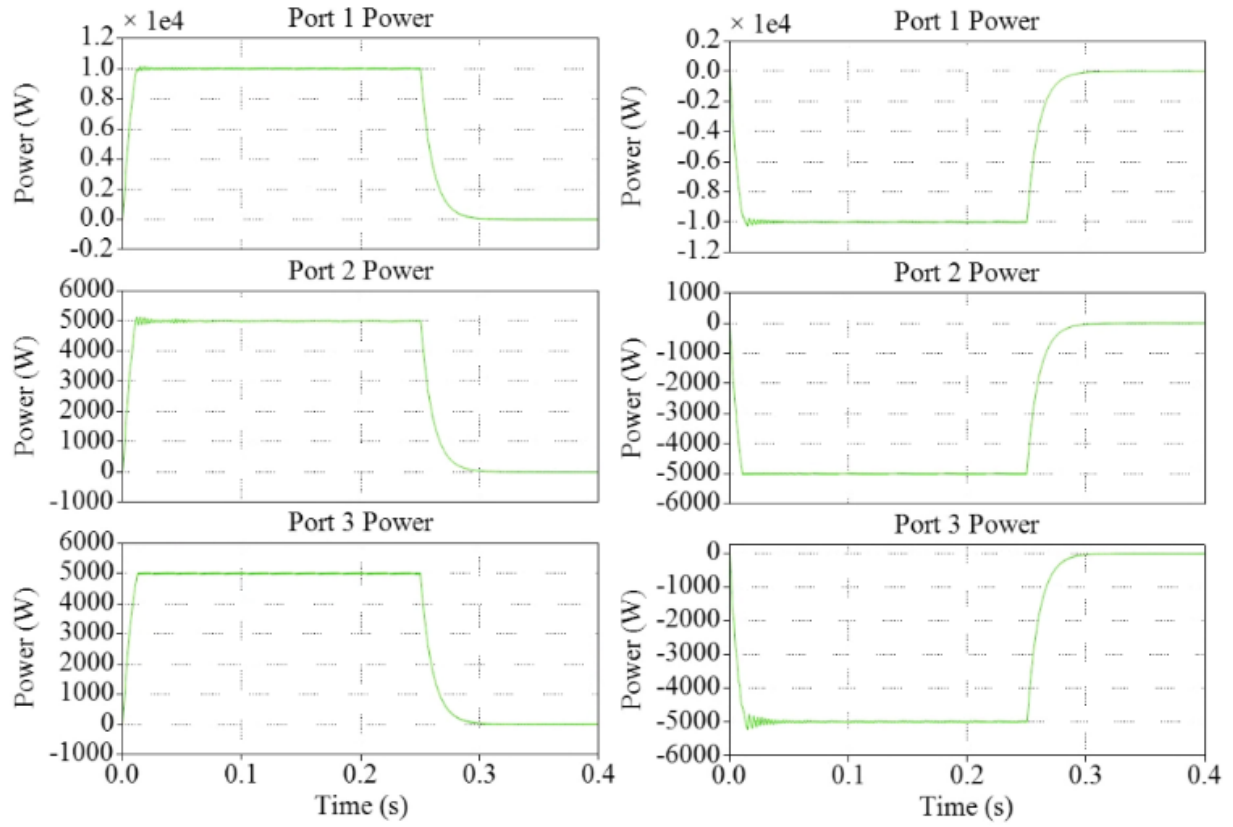


Figure 31: Output waveforms for (a) the first CFMP-DAB converter splitting 10kW delivery across two buses and (b) the second CFMP-DAB converter absorbing 5kW from each bus to feed a constant 10kW load. At time $t = 0.25\text{s}$, the load is deactivated and the converters are turned off.

2.8 Conclusions and Discussions

This experiment successfully employed a control strategy for a current-fed triple active bridge converter that prevents disturbances at a load port from disturbing the power flow at the second load port. By computing the relationships between the phase angles ϕ_2 and ϕ_3 and the port power outputs P_2 and P_3 , the power output at port 2 was able to be freely controlled by ϕ_2 while ϕ_3 was used to maintain a constant power output at port 3. The procedure was presented in such a way that the process for deriving the control relationships can be replicated for other multi-winding DAB-based converter topologies.

The configuration in Section 2.7 provided a method to obtain the average power output of a current-fed 3-port DAB converter for all operating modes. The resulting power output capacity for the entire control range was graphed. The average power flow equations were used to create a control strategy that permitted the average power at port 3 to remain constant while the average power at port 2 fluctuated under changing load conditions. This demonstrated the converter's ability to isolate a port from the transient events that occur at the other ports. Ultimately, two converters were used to create a ring bus network, which allowed power to be routed along two redundant paths to feed a critical load.

One thing to note about the proposed controller versus more traditional types of decoupled control is the fact that the proposed controller is valid for all operating conditions and bus voltages. Traditionally, a decoupling matrix is generated by linearizing around an operating point. However, if the operating point changes, the decoupling matrix requires re-derivation, which is computationally intensive. The proposed controller does not require re-derivation under changing operating conditions, but the proposed control does require extra math operations, such as a square root, which could limit the bandwidth of the controller. Another challenge with using the proposed

the controller is its dependence on knowing an accurate value of the transformer inductance for proper operation. The need to have an accurate parameter value for inductance within a DAB converter is a motivation for the projects listed in Section 3.

3.0 Research Plan: Objective #2 - Nonlinear Observer and Parameter Estimator for Dual Active Bridge Converter

3.1 Literature Review

This objective aims to utilize two separate nonlinear control techniques to enhance the control of a dual active bridge (DAB) converter. In particular, a current observer and an inductance parameter estimator will be developed. The current observer will be used to predict dc current bias on the transformer. The parameter estimator will be used to predict the value of the transformer series inductance, which will be demonstrated in an application with a dynamically changing inductance. Note that parts of this project work were collaborative. For completeness, the full project details will be reported in this section, and for transparency, contributions made from individuals other than the author of this dissertation will be identified.

3.1.1 Current Observer

DC magnetization within transformers is a well-known problem for high power converters [37]. Typical phase-shift operation of a DAB assumes that the primary and secondary bridges operate in a symmetrical manner, meaning that the duration of positive voltage is equal to the duration of negative voltage across the transformer windings. In practice, slight deviations in control lead to asymmetrical switching behavior. The result is that a volt-second imbalance is applied to the windings of the transformer; and as a result, the current waveform experiences a dc bias. S. Han et. al. defined well the phenomenon of DC flux on a transformer, and consequently,

the surge in magnetizing current resulting from a DC flux bias [38]. As the flux through a transformer experiences a DC flux, the peak flux becomes higher and eventually the transformer saturates. At this point, the magnetizing current experiences a large surge. Figure 32 depicts the magnetizing current surge scenario described in [38].

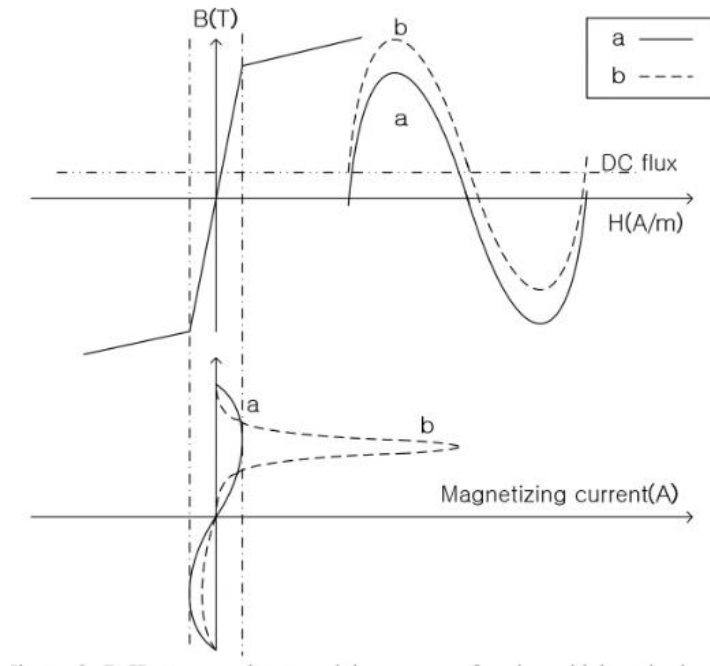


Figure 32: B-H curve and magnetizing current for sinusoidal excitation for (a) average flux = 0, and (b) average flux $\neq 0$ [38]

Due to the saturation problem, prevention of transformer DC magnetization and saturation is a necessary capability for a DAB controller. This control process can be typically broken down into two distinct steps: 1) measure and detect that DC magnetization is occurring and 2) take necessary switching actions to eliminate the DC magnetization. Many controllers use the ‘equal area’ method to detect DC bias in flux or current [38]–[40]. Typically, average current is either measured via integration, [38] which is typically slow to respond (many cycles), or via predictive peak current regulation [40], which is faster to respond (one or two cycles). Compensation is then performed by modifying phase shifts and duty cycles at both the primary and secondary bridges in

an asymmetrical manner to offset the dc bias. It should be noted that the predictive method relies heavily on accurate component values, such as transformer winding inductance. The predictive method will not properly remove DC flux offsets if the inductance value used is inaccurate. The unique controller proposed for this objective should be able to respond quickly to dc flux offsets while also being more resistant to inaccurate component measurements. The details of the proposed control will be explained in the upcoming sections.

Future work: A proposed use for the current observer that was identified in this literature review, but not explored in this dissertation is to use the predicted current waveform to ensure ZVS. A control strategy ensuring ZVS operation using the current observer is left for future work. At present, there are many analyses published which detail the exact criteria for optimal operation of a dual active bridge converter [41]–[43]. Often, multiple control schemes are required to achieve a wide operating range for a DAB converter [42]. A reference experiment used for this project can be found in [44]. This reference experiment employs a phase shift modulation scheme and details the operating conditions that ensure soft switching.

3.1.2 Parameter Estimator

The solid-state transformer (SST) has been a top emerging technology for future power distribution systems for over a decade [45]. The primary circuit topology within a SST is the dual active bridge (DAB) converter. A key feature of the SST for distribution systems is the use of a high frequency transformer (several to tens of kHz) instead of a line frequency transformer (typically 50 or 60Hz). The high frequency transformer has significantly reduced volume and weight, which is a desirable feature for applications with footprint restrictions. In addition, the power electronic switches are controllable, which empowers the SST to play an active role in

power flow control. The converter's ability to respond to load changes is a central focus of this paper.

A primary design consideration of the DAB converter within a SST is the transformer and its associated leakage inductance. Typically, the inductance value is chosen based on the power flow requirements of the converter. However, with the emergence of advanced magnetic materials for use in power converters, consideration should be taken for the unique behaviors enabled by the new materials. For example, saturated core current limiters could be incorporated into the magnetics design, thereby limiting fault current in medium voltage dc grid applications [46], [47]. Also, anisotropic and spatially tuned core materials can shape the flux path and thermal dissipation within the transformer [48], [49]. Lastly, emerging tunable magnetics could enable the ability to dynamically control the series inductance value of the DAB converter, which is a consideration in this paper [50], [51]. With the possibility of a varying series inductor, a method is explored in this paper to estimate the value of the inductance and adjust the control accordingly.

The motivation for implementation of a varying inductor within a DAB converter is to adjust the series inductance to attain a wider operating range. Typically, a larger series inductance is selected when a wider operating range is desired, at the cost of less efficient operation at full load [52]. With a tunable inductor, the inductance could be higher at light loads, and lower at heavy loads, theoretically allowing the DAB converter to operate with more efficiency as shown in Figure 33.

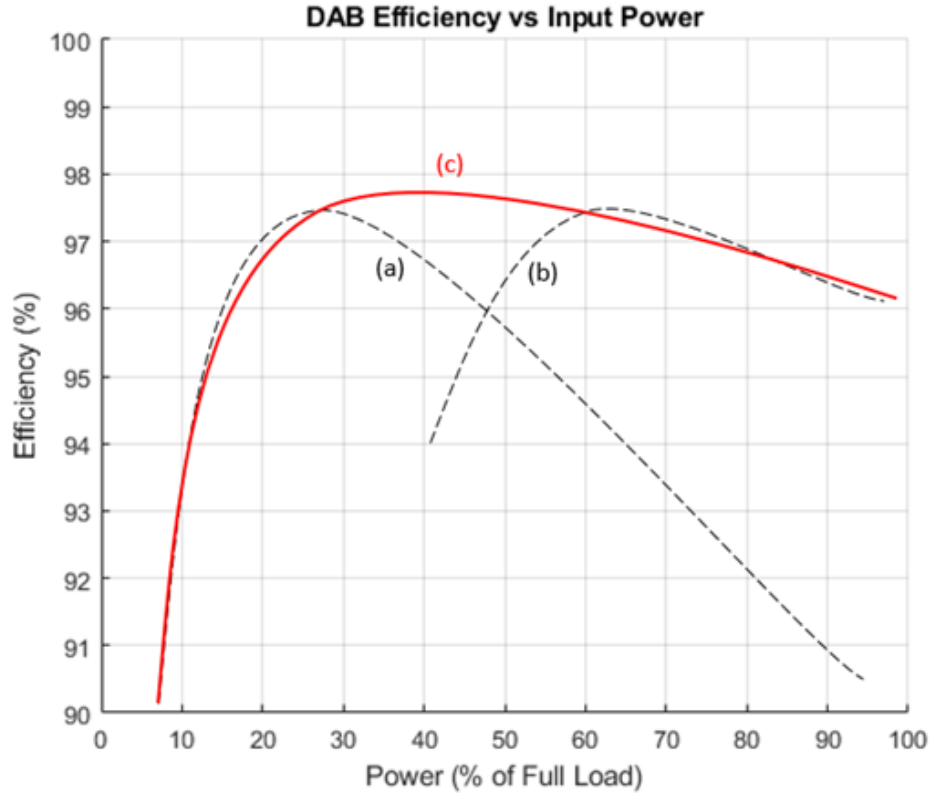


Figure 33: Conceptual DAB efficiency curves with (a) wide operating range and high leakage inductance $L = 2.5L_0$ {where L_0 is an arbitrary inductance value}, (b) high efficiency at max load and low leakage inductance $L = L_0/2.5$, and (c) both high efficiency and wide operating range using a tunable inductor $L_0/2.5 \leq L \leq 2.5L_0$

3.2 Development of Observer

This section details the procedure to develop the observer. First, the behavior of a dual active bridge converter will be modeled analytically using its dynamic equations. Then, an observer will be created to estimate the transformer current waveform, and in turn, the flux through the transformer. Ultimately, the accuracy of the estimator is confirmed with a PLECS simulation.

3.2.1 Mathematical Model of DAB Converter

The DAB converter has been extensively modeled mathematically and has been implemented within projects that prototyped various DAB topologies [42], [45], [53]–[56]. The model used for the current observer will be derived by taking the fundamental and first few harmonics of the primary and secondary switching voltages. The DAB circuit is shown in Figure 34. The example application is a DC source with an interfacing DAB converter to feed a DC load. The load bus also has a bus capacitor.

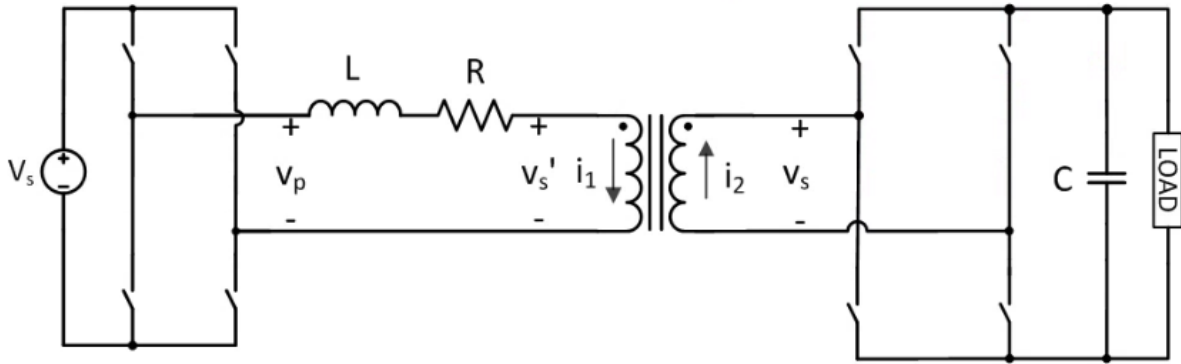


Figure 34: Dual Active Bridge Converter Circuit Model

The transformer model used in Figure 34 is a simplistic and does not include magnetizing inductance of the transformer. For steady state operation, this is acceptable; however, under changing operating conditions, the magnetizing inductance could have a significant current contribution and affect the converter's performance. One of the key benefits of a nonlinear observer is that the simple model in Figure 34 is sufficient for steady state operation, and under transient conditions, the nonlinear behavior will be able to detect the unmodeled behavior and provide corrective actions proportional to the magnitude of the transient disturbance. The project found in [57] demonstrates the observer's ability to provide an estimation of corrective action required, based on a crash detection scheme for a vapor compressor. The proposed current

observer will provide a corrective response as a DAB converter is experiencing a DC current bias, which could lead to transformer saturation.

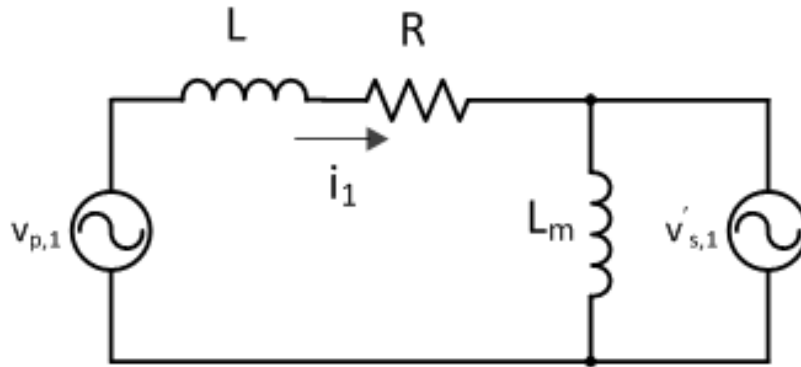


Figure 35: Fundamental Harmonic Model of DAB Converter

A Fourier series analysis will be performed on the square waveforms for the primary and secondary bridges. The resulting harmonic voltages will be treated as AC voltage sources. Shown in Figure 35 is the circuit model for the primary harmonic. This model will be the basis for the dynamic equations that will be used for the observer.

3.2.2 Development of Observer

The proposed observer for this project is a Robust Integral Square of Error (RISE) observer. This observer has been used in past projects for tracking piston collisions and detecting faults within PV systems and robots [57]–[59]. The observer is known for having a fast convergence time to the signal that it is observing. The derivation of this RISE observer from the fundamental circuit model in Figure 35 was completed by Dr. Michael McIntyre from the University of Louisville.

The observer requires a few assumptions to be applicable to a given control problem. 1) Certain operating waveforms will need to be known. Fortunately, using the DAB converter model

in Figure 35, the voltage applied to the transformer windings will be known during operation. The primary voltage source will have a constant voltage, and the bus capacitor for the load will be sufficiently large such that the voltage change during a switching cycle will be negligible. A voltage sensor on the dc buses and knowledge of the switching signals is sufficient. 2) The component parameters for winding inductance and resistance of the transformer must be known for the observer to function properly. 3) All operating variables must be piecewise continuous and bounded. At first glance, the square voltage waveforms for v_p and v_s' appear to violate the piecewise requirement, which is why a Fourier analysis will be used to approximate the behavior as sinusoidal.

Historically, the benefit to using the RISE observer is the speed at which the observer can respond to transient conditions. In this case, the observer will be developed to track the current flowing through the transformer. Typically, to detect a DC current bias, the current measurement must be averaged over many switching cycles. The observer, on the other hand will rapidly detect a dc current bias. By allowing the converter to act quickly, the converter will extend the lifetime of the high frequency transformer.

3.2.3 Observer validation using PLECS

A circuit simulation was developed within PLECS, based off of the demo file for a dual active bridge converter and is shown in Figure 36. The primary port has a voltage source which represents a dc bus. The secondary port has a dc bus capacitor and resistive loads. Each port has a full H bridge and the transformer has an associated winding resistance, leakage inductance, and magnetizing inductance.

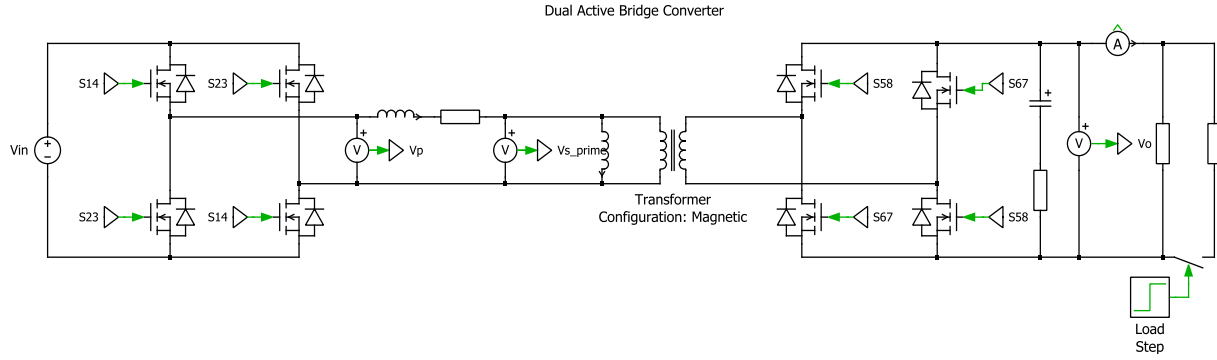


Figure 36: DAB Converter Model within PLECS for Current Observer

The observer model was implemented within PLECS using integrators, gain blocks, etc. to achieve the observer mathematics. Figure 37 shows the block diagram of the current observer model based on a RISE observer.

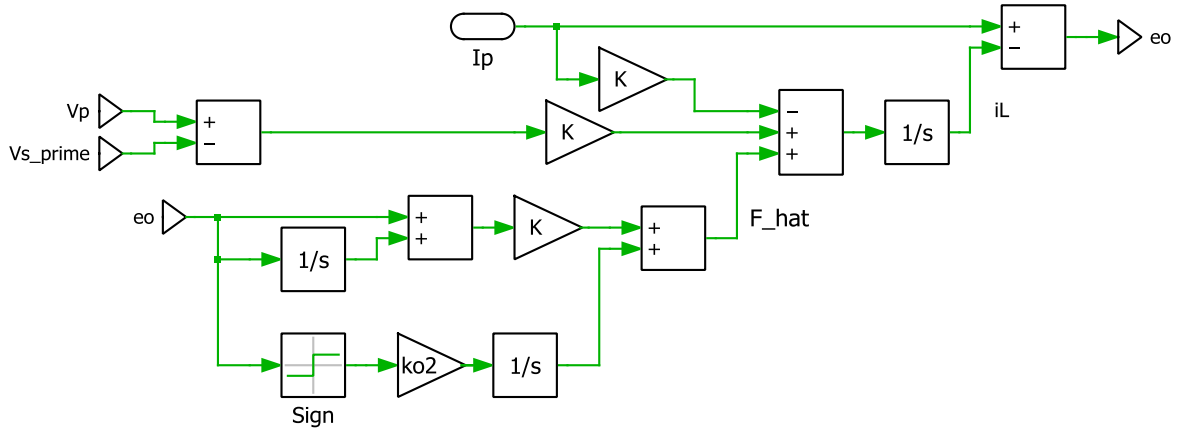


Figure 37: Inductor Current Estimator for i_L with the High Frequency Voltages as Inputs

The simulation was run and the measured current was compared to the estimated current. Initially, the current estimation error e_o was nonzero, but as $t \rightarrow \infty$, the error becomes zero. Figure 38 shows the current estimation error for the simulated current versus the estimated current.

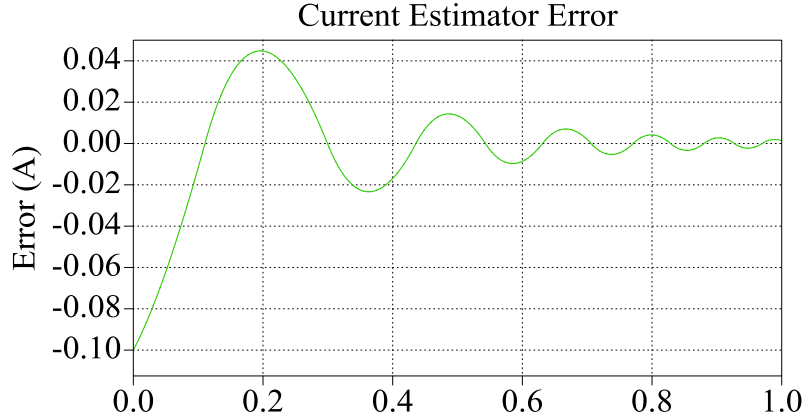


Figure 38: Current Estimator Error

3.3 Detection and Compensation of DC Flux Using Observer

This section discusses the proposed method to detect dc magnetization in the transformer. When the controller identifies a dc current bias in the transformer, the controller will implement a switching routine to compensate for the dc bias. This control logic and compensation is implemented within simulation to confirm proper performance of the controller.

3.3.1 Detection of DC Flux and Magnetizing Current

Due to the slow nature of integrators, detection of a dc offset within the average transformer current usually requires many switching cycles [40]. That also assumes that the current measurement is accurate enough to reliably detect dc current bias. A key benefit of the proposed detection scheme using a nonlinear observer is that the ability to accurately track current behavior means that the controller has the ability to reliably predict a dc current offset. The controller is able to detect a dc offset as fast as a single half cycle (when compared with the previous half-

cycle) and decide immediately if compensation is required. In practice, a few half cycles may be averaged to be more resistant to noise. This section will apply a dc offset to the current of the converter under normal operation. The average current deviates from zero, and as a result, the controller detects then compensates for this event.

The PLECS simulation in Figure 36 was run with a load step at 0.5s. This is based on the PLECS demo file for a DAB converter. The ac current under normal operating conditions is shown in Figure 39. In Figure 40, a modification is made to the pulse duration of the secondary switches to purposefully create an imbalance. This figure demonstrates how a slight offset of switching duration can cause the current through the transformer to have a dc bias. In this instance, the current will continuously increase until the transformer core saturates. In order to prevent such a scenario, a compensation scheme will be developed in the following section.

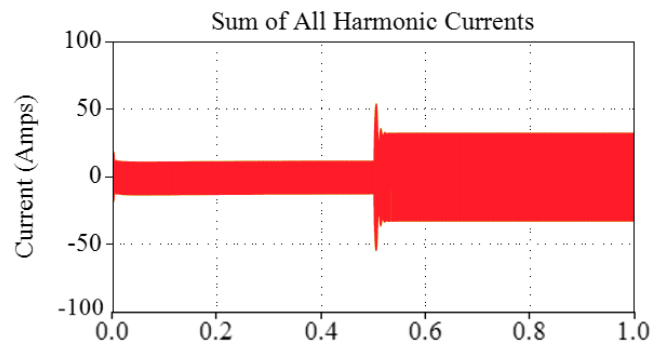


Figure 39: AC Current of DAB with Load Step at 0.5s

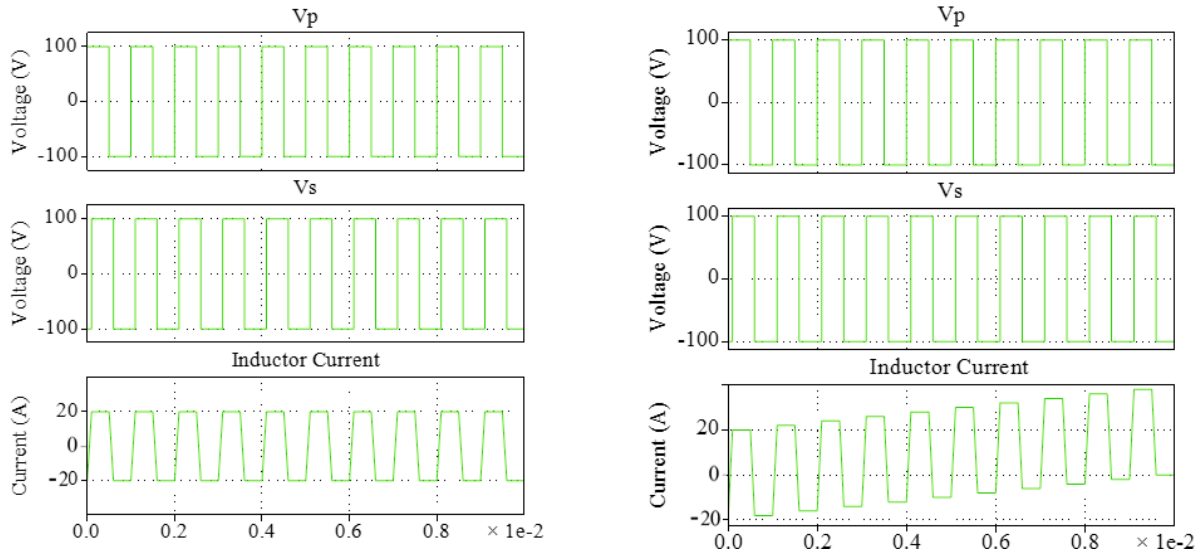


Figure 40: AC Voltages and Currents for Symmetrical Switching, $V_p = 0.5$; , $V_s = 0.5$ (Left) and Asymmetrical Switching, $V_p = 0.5$; , $V_s = 0.495$ (Right)

3.3.2 Compensation of DC Flux

Removal of a DC current bias within a transformer is straightforward (when using phase-shift control). Typically, for balanced operation of phase-shift control, the duty cycles of the primary and secondary bridges must be equal. When the duty cycles are unequal, this imposes a dc offset in the transformer. The result of this phenomenon is that the duty cycles are kept strictly equal under normal conditions. However, unequal duty cycles can be used to remove an existing dc offset in the transformer by applying a dc bias which counters the existing offset [38], [40].

Figure 41 shows the transformer current as a dc current bias is imposed. In this case, at $t = 0.05s$ the dc current bias begins to decrease from 0 until the transformer saturates. The transformer saturation limits were not selected for an application, but merely are arbitrary to demonstrate this operating example. At $t = 0.3s$, the bias is removed and the current returns to

an average current of 0A. The load step occurs at usual at $t = 0.5s$. At $t = 0.55s$, the dc current bias is once again applied to the current until it is removed at $t = 0.8s$.

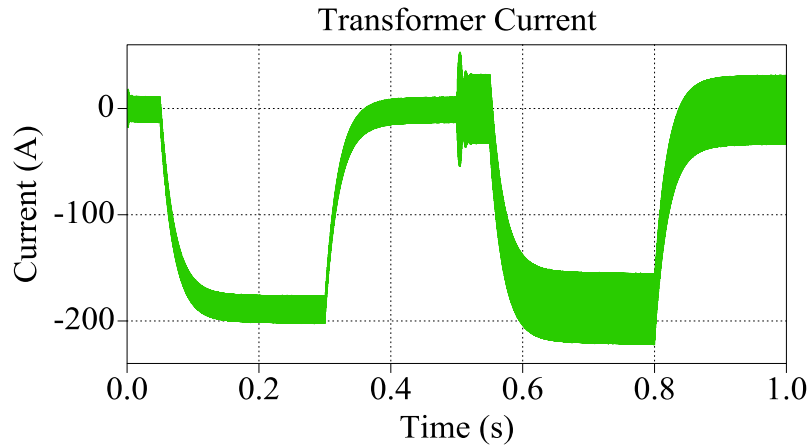


Figure 41: DC Current Bias is Applied to Transformer at $0.05s < t < 0.3s$ and again at $0.55s < t < 0.8s$

The compensation strategy was then implemented into the DAB controller. Since single phase shift control is used in the PLECS simulation, the duty cycle remains at $D = 0.5$ in typical operation. After implementation of the current observer, the average current across a half cycle was computed. If the controller detects a nonzero average current, the controller will adjust the duty cycle of the secondary H bridge to be either $D = 0.495$ or $D = 0.505$, depending on the polarity of the dc bias. Figure 42 shows the performance of the compensation strategy as the same transformer current bias is introduced to the converter.

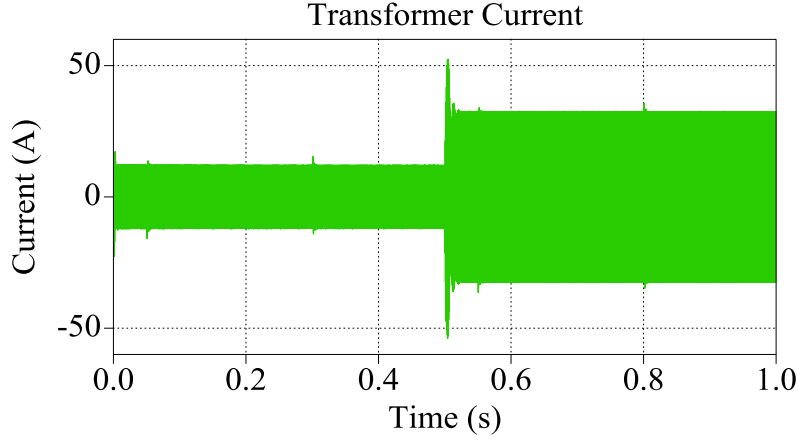


Figure 42: Transformer Current with Compensation Strategy Implemented. DC Current Bias is Applied to Transformer at $0.05s < t < 0.3s$ and again at $0.55s < t < 0.8s$

3.4 Parameter Estimator for Inductance within a Dual Active Bridge Converter

There have been many in-depth studies on modulation strategies to ensure efficient operation of the DAB converter [41], [43], [44], [60]. When discussing efficiency, two common loss mechanisms are discussed for the switching devices: switching loss and conduction loss. Likewise, the two leading loss mechanisms for the transformer are usually conduction losses and magnetization losses. Usually, the power electronic switches and transformer are both evaluated when considering efficiency of the DAB converter. Typically, after component parameters are chosen, the easiest method to improve converter efficiency is to operate the switches using ZVS. ZVS operation reduces switching losses by using commutation currents to charge or discharge nonlinear switch output capacitance. By allowing the capacitance to charge/discharge with commutation currents, the switches themselves can be ‘soft switched’, which minimizes switching losses. This section will explore another method to improve the efficiency of a DAB converter: by dynamically changing the transformer inductance under different operating modes.

3.4.1 Background

A primary design consideration of the DAB converter within a solid-state transformer (SST) is the transformer and its associated leakage inductance. Typically, the inductance value is chosen based on the power flow requirements of the converter. However, with the emergence of advanced magnetic materials for use in power converters, consideration should be taken for the unique behaviors enabled by the new materials. For example, saturated core current limiters could be incorporated into the magnetics design, thereby limiting fault current in medium voltage dc grid applications [46], [47]. Also, anisotropic and spatially tuned core materials can shape the flux path and thermal dissipation within the transformer [48], [49]. Lastly, emerging tunable magnetics could enable the ability to dynamically control the series inductance value of the DAB converter, which is a consideration in this project [50], [51]. With the possibility of a varying series inductor, a method is explored within this Section 3.4 to estimate the value of the inductance and adjust the control accordingly.

The motivation for implementation of a varying inductor within a DAB converter is to adjust the series inductance to attain a wider operating range. Typically, a larger series inductance is selected when a wider operating range is desired, at the cost of less efficient operation at full load [52]. With a tunable inductor, the inductance could be higher at light loads, and lower at heavy loads, theoretically allowing the DAB converter to operate with more efficiency as shown in Figure 43.

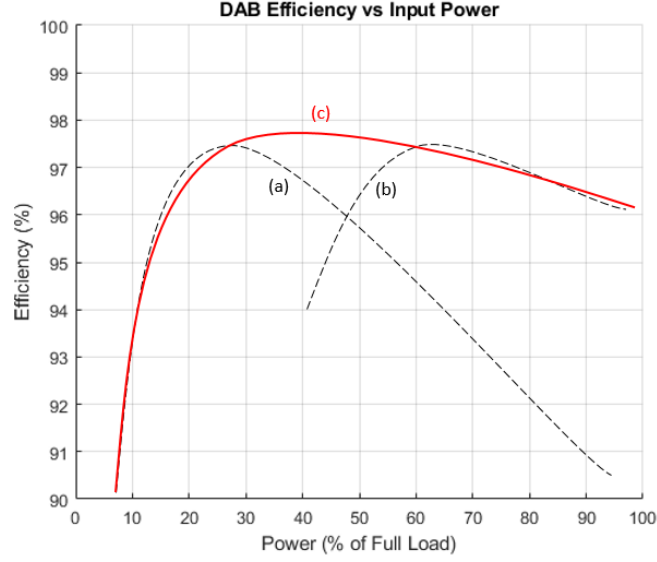


Figure 43: Conceptual DAB efficiency curves with (a) wide operating range and high leakage inductance $L = 2.5L_0$ {where L_0 is an arbitrary inductance value}, (b) high efficiency at max load and low leakage inductance $L = L_0/2.5$, and (c) both high efficiency and wide operating range using a tunable inductor $L_0/2.5 \leq L \leq 2.5L_0$

This project introduces a parameter estimator to detect a dynamically changing inductance within a DAB converter, and a subsequent controller that incorporates the estimated inductance value to tune the controller gains.

3.4.2 Dual Active Bridge Model

A standalone DAB converter is explored in this project along with the parameter estimation scheme. The DAB converter model is shown below in Figure 44. The primary side source is treated as an ideal dc voltage source and the secondary side is treated as a resistive load (R_{load}) with an associated dc bus capacitor (C). The physical transformer is represented as a series inductance (L), a winding resistance (R), and an ideal transformer.

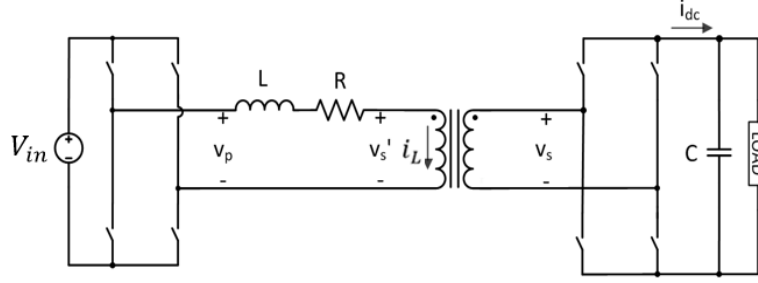


Figure 44: Dual Active Bridge Converter Model

The average output power and current functions of a DAB converter have been well defined in literature and are shown in (3-1) and (3-2) [23], [61]. The switching frequency is defined as f and the phase shift can either be defined in radians (ϕ) from $-\pi$ to π , or as a ratio (α) from -0.5 to +0.5. With an output capacitor and resistive load, the dynamic behavior of the DAB's output voltage is given in (3-3).

$$P = \frac{V_{in} V'_{out}}{2fL} \frac{\phi}{\pi} \left(1 - \frac{|\phi|}{\pi} \right) \quad (3-1)$$

$$I_{dc,avg} = \frac{V_{in}}{2fL} \frac{\phi}{\pi} \left(1 - \frac{|\phi|}{\pi} \right) \quad (3-2)$$

$$\frac{dV_{out}}{dt} = -\frac{1}{R_{load}C} V_{out} + \frac{1}{C} \left(\frac{V_1}{2fL} \frac{\phi}{\pi} \left(1 - \frac{|\phi|}{\pi} \right) \right) \quad (3-3)$$

3.4.3 Dual Active Bridge Controller Structure

The proposed controller structure is shown in Fig. 3 in blue, which incorporates the parameter estimator with the base controller architecture in black originally proposed by Cardozo

et al. [61]. The second-order nature of the controller closed-loop transfer function allows the gains K_1 and K_2 to be directly computed from the design specifications of the converter, and then updated in real time by the output of the parameter estimator. The gain equations are listed as (3-4) and (3-5). The controller is designed to have a critically damped large signal transient response.

$$K_1 = 4\xi\omega_n CLf - \frac{2Lf}{R_{load}} K_{est} \quad (3-4)$$

$$K_2 = -\frac{2CLf\omega_n^2}{K_{est}} \quad (3-5)$$

In Fig. 3, the proposed parameter estimator will estimate the inductance value and only update the value of \hat{L} if the inductance has changed beyond a certain threshold. The compensation operates by adjusting the ratio of estimated inductance \hat{L} , to the original inductance L , through $K_{est} = \frac{\hat{L}}{L}$ and then adjusts the natural frequency (ω_n) of the large signal response according to $\hat{\omega}_n = \omega_n / K_{est}$. While the compensation loop is active, the controller maintains the critically damped performance requirement but will change the speed of convergence of the large signal transient response according to the change in inductance. Upon a significant change of inductance, the controller will output the estimate \hat{L} and update the gain term, K_{est} . The controller gains are given in (3-4) and (3-5), respectively [61]. For a critically damped system, $\xi = 1$.

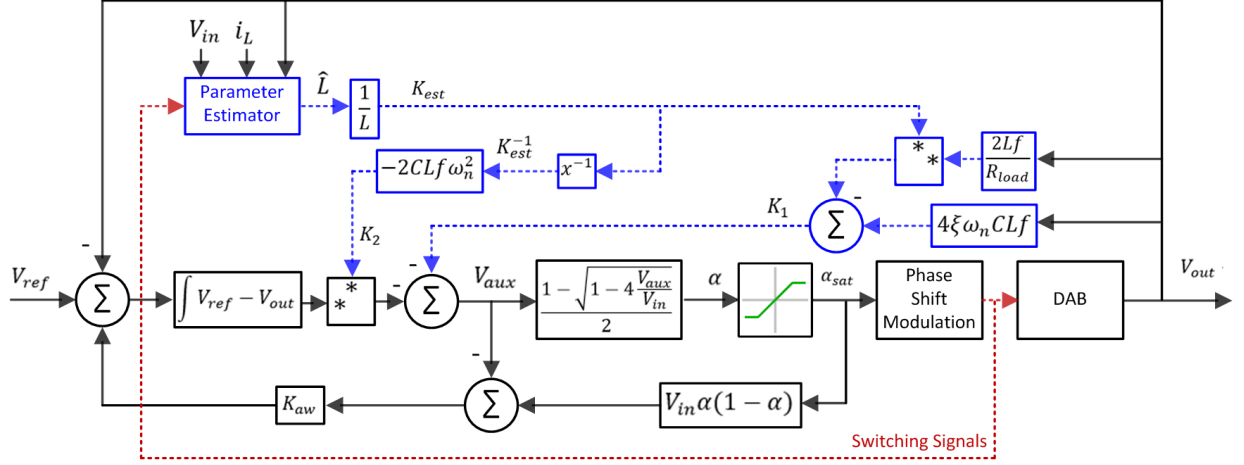


Figure 45: Augmented Control Block Diagram Architecture with Parameter Estimator

3.4.4 Parameter Estimator

The parameter estimator scheme is particularly promising, as having real-time parametric information will enhance the performance of future control strategies for DAB converters. As the primary winding inductance is central to our scheme, a cycle average model for the primary current dynamics is defined in (3-6), where $I(t)$ is the average primary winding current, L is the uncertain primary winding inductance, and the R is the uncertain primary winding resistance. The average control input is known and is a function of the delay angle and is defined in (3-7). The primary current $I(t)$, and the control input $u(\phi)$ are assumed measurable and persistently excited [62]. The fundamental harmonic model used for the analysis is shown in Figure 46.

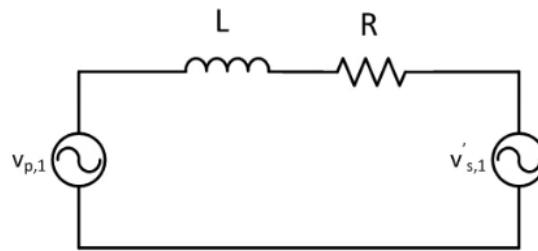


Figure 46: DAB Converter Fundamental Harmonic Model

$$L\dot{I} + RI = u(\phi) \quad (3-6)$$

$$v_p - v'_s(\phi) = u(\phi) \quad (3-7)$$

$$\dot{I} = \mathbf{W}\boldsymbol{\theta} \quad (3-8)$$

To develop the parameter estimation scheme, the current dynamics are written as (3-8), where $\mathbf{W} \triangleq [W_1 \quad W_2] \in \mathbb{R}^{1 \times 2}$ is the known regression vector. In (3-8) $W_1 = u(\phi)$ and $W_2 = -I(t)$. Also in (3-8), the unknown parameter vector is defined as follows: $\boldsymbol{\theta} \triangleq [\theta_1 \quad \theta_2]^T \in \mathbb{R}^{2 \times 1}$ where $\theta_1 = 1/L$ and $\theta_2 = R/L$. To facilitate the PE scheme design, an estimation error is defined as (3-9). In (3-9), $I_f(t)$ is a filtered version of primary current and is defined as (3-10), where $b \in \mathbb{R}^+$ is a PE scheme gain. $I_f(t)$ is not measurable in (3-10) because the derivative of the current is not measurable. Instead, an implementable form is defined in (3-11) and (3-12).

$$\varepsilon \triangleq \hat{I}_f - I_f \quad (3-9)$$

$$\dot{I}_f \triangleq -bI_f + b\dot{I} \quad (3-10)$$

$$I_f = P_1 + bI \quad (3-11)$$

$$\dot{P}_1 = -b(P_1 + bI) \quad (3-12)$$

$$\hat{I}_f = \mathbf{W}_f \hat{\boldsymbol{\theta}} \quad (3-13)$$

$$\dot{\mathbf{W}}_f \triangleq -b\mathbf{W}_f + b\mathbf{W} \quad (3-14)$$

In (3-12), $P_1(t)$ is an auxiliary filter signal generated from the system dynamics. To finalize the terms required for $\varepsilon(t)$ in (3-9), \hat{I}_f is defined in (3-13), where $\mathbf{W}_f \in \mathbb{R}^{1 \times 2}$ is the filtered

regression vector given by (3-14) where, $\mathbf{W}_f(t_0) = [0 \ 0]$. In (3-13), the parameter estimates, $\hat{\boldsymbol{\theta}}(t) = [\hat{\theta}_1 \ \hat{\theta}_2]^T \in \mathbb{R}^{2 \times 1}$, are defined. From (3-8), (3-10), and (3-14) it is possible to describe $\dot{I}_f(t)$ as (3-15). Taking the time derivative of (3-13) and utilizing (3-14), (3-16) can be written. Now by subtracting (3-16) from (3-15) the resulting expression can be written as (3-17), where $\tilde{\boldsymbol{\theta}}(t) \in \mathbb{R}^2$ is the estimated parameter error signal defined as (3-18). To complete the PE scheme design, a continuous-time least squares update law is utilized to generate the parameter estimates and is described in (3-19) and (3-20) [62].

$$\dot{I}_f + bI_f = \dot{\mathbf{W}}_f \boldsymbol{\theta} + b\mathbf{W}_f \boldsymbol{\theta} \quad (3-15)$$

$$\dot{\hat{I}}_f + b\hat{I}_f = \frac{d}{dt}(\mathbf{W}_f \hat{\boldsymbol{\theta}}) + b\mathbf{W}_f \hat{\boldsymbol{\theta}} \quad (3-16)$$

$$\dot{\varepsilon} + b\varepsilon = \frac{d}{dt}(\mathbf{W}_f \tilde{\boldsymbol{\theta}}) + b\mathbf{W}_f \tilde{\boldsymbol{\theta}} \quad (3-17)$$

$$\tilde{\boldsymbol{\theta}} \triangleq \boldsymbol{\theta} - \hat{\boldsymbol{\theta}} \quad (3-18)$$

$$\dot{\hat{\boldsymbol{\theta}}} \triangleq -\mathbf{K}_{ls} \frac{\mathbf{P}_{ls} \mathbf{W}_f^T \varepsilon}{1 + \gamma \mathbf{W}_f \mathbf{P}_{ls} \mathbf{W}_f^T} \quad (3-19)$$

$$\dot{\mathbf{P}}_{ls} \triangleq -\mathbf{K}_{ls} \frac{\mathbf{P}_{ls} \mathbf{W}_f^T \mathbf{W}_f \mathbf{P}_{ls}}{1 + \gamma \mathbf{W}_f \mathbf{P}_{ls} \mathbf{W}_f^T} \quad (3-20)$$

$$\hat{L} \triangleq 1/\hat{\theta}_1 \quad (3-21)$$

$$\hat{R} \triangleq \hat{\theta}_2/\hat{\theta}_1 \quad (3-22)$$

In (3-19), \mathbf{K}_{ls} is a constant diagonal gain matrix, γ is a positive constant, and \mathbf{P}_{ls} is a covariance matrix, which is defined in (3-20). In (3-20), $\mathbf{P}_{ls}(t_0) = k_0 \mathbf{I}_2$, where k_0 is a constant gain, and \mathbf{I}_2 is the standard 2x2 identity matrix. The primary winding inductance estimate is given in (3-21), likewise, the resistance estimate is given in (3-22). **Remark:** From (3-21) and (3-22), special care is needed to avoid $\hat{\theta}_1 = 0$. To achieve this condition, the projection algorithm as described in [62] must be utilized. Figure 47 shows the block diagram of the PE.

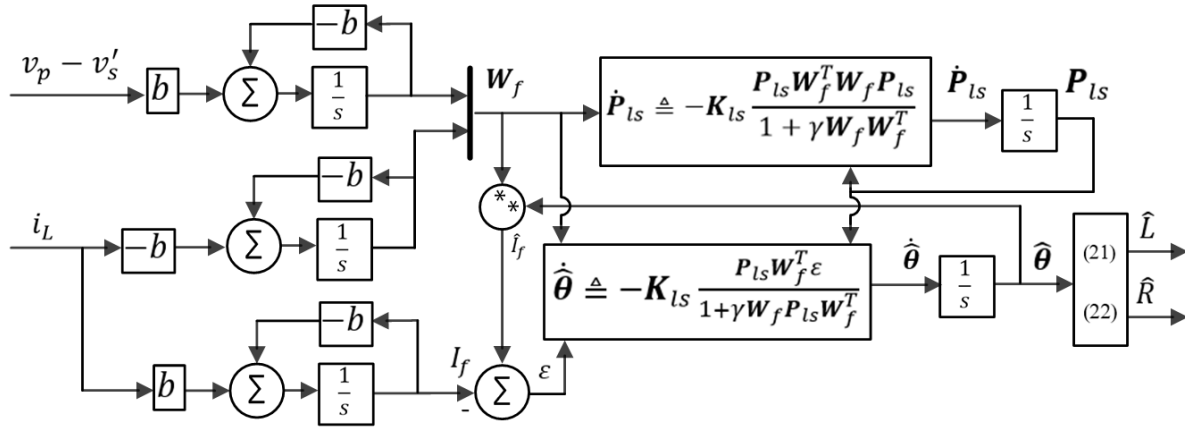


Figure 47: Parameter Estimator Block Diagram

Theorem 3.1: The least square update law as designed in (3-19) and (3-20) ensures $\tilde{\theta}(t) \rightarrow 0$ as $t \rightarrow \infty$, provided that four sufficient conditions are met. The first is that the plant of estimation is strictly proper. The second is that the system's input is piecewise continuous and bounded. Thirdly is that the system's output of the plant of estimation is bounded. The last is the following persistence of excitation conditions holds: $\alpha_1 \mathbf{I}_2 \leq \int_{t_0}^{t+\delta} \mathbf{W}^T(\sigma) \mathbf{W}(\sigma) d\sigma \leq \alpha_2 \mathbf{I}_2$ where $\alpha_1, \alpha_2, \delta$ are constants and \mathbf{W} as defined in (3-8).

Proof: In order to prove that $\tilde{\theta}(t) \rightarrow 0$ as $t \rightarrow \infty$, Theorem 2.5.3 from [62] is followed directly. In (3-10), the plant of estimation can be redefined as follows:

$$\frac{I_f}{r_f} = \frac{b}{s + b} \quad (3-23)$$

where the input $r_f(t) \in \mathbb{R}$, is defined as $r_f(t) = \dot{i}(t)$. It is clear from (3-23) that the plant is strictly proper. In order to prove the input meets the 2nd condition, the average model defined in (3-6) is utilized. In this model we assume that the current $I(t)$ and the control input $u(\phi)$ are bounded, therefore $r_f(t)$ is also piecewise continuous and bounded. The third condition is met by utilizing typical linear analysis tools to demonstrate that both $I_f(t), \dot{I}_f(t) \in \mathcal{L}_\infty$, hence proving the output of the plant of estimation is bounded. The reader is directed to the proof in [62] to satisfy the final condition

3.4.5 PLECS Simulation of Control Strategy

The DAB converter, controllers, and parameter estimator were initially modeled in PLECS. The circuit model used is shown in Figure 48. The component values were selected based on a reference experiment and can be found in Table I [61]. To confirm proper control, the large signal transient response for the controller is shown in . Note that the selection of percent overshoot was 2% to verify proper operation of the model when compared to the reference experiment. Moving forward with the control hardware-in-the-loop experimentation in this paper, the system control will be critically damped, with no overshoot and $\xi = 1$.

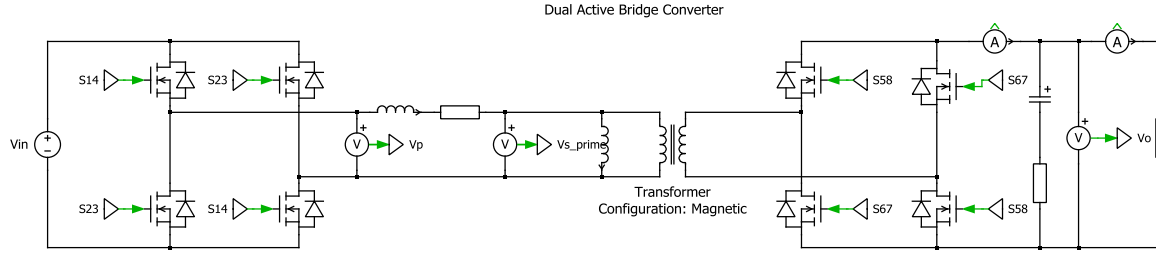


Figure 48: PLECS DAB Converter Model

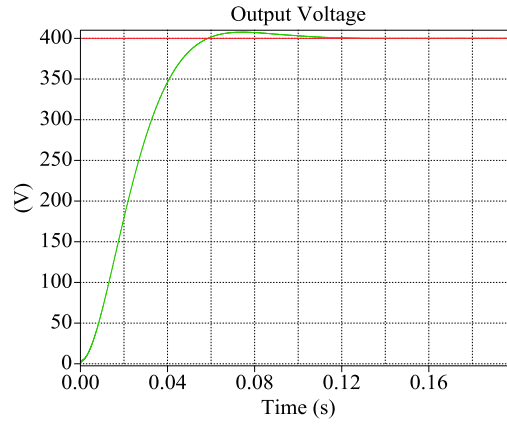


Figure 49: Load Bus Voltage Large Signal Transient

Table 5: System Parameters and Design Requirements

Parameter	Value	Parameter	Value
Input Voltage	400V	Switching Frequency	10kHz
Output Voltage	400V	XFMR Turns Ratio	1:1
Series Inductance	189 μ H	Load Resistance	40 Ω
Magnetizing Inductance	2.0mH	Percent Overshoot	2%
Output Capacitance	1.35mF	Settling Time	0.1s

3.4.6 Control Hardware-in-the-Loop Experiment

The DAB converter was simulated in real-time using a Typhoon HIL402 hardware-in-the-loop system. A Texas Instruments F28379 controller was used and programmed with the TI C2000 coder and target blockset within PLECS. The HIL402 provided the current and voltage

measurements from a simulated DAB converter as an output and the F28379 control card responded with PWM switching signals for the converter within the real-time digital simulation. The controller was designed to be large-signal critically damped based on the parameters of a reference experiment found in Table 5. The diagram of the Typhoon HIL experimental setup is shown in Figure 50.

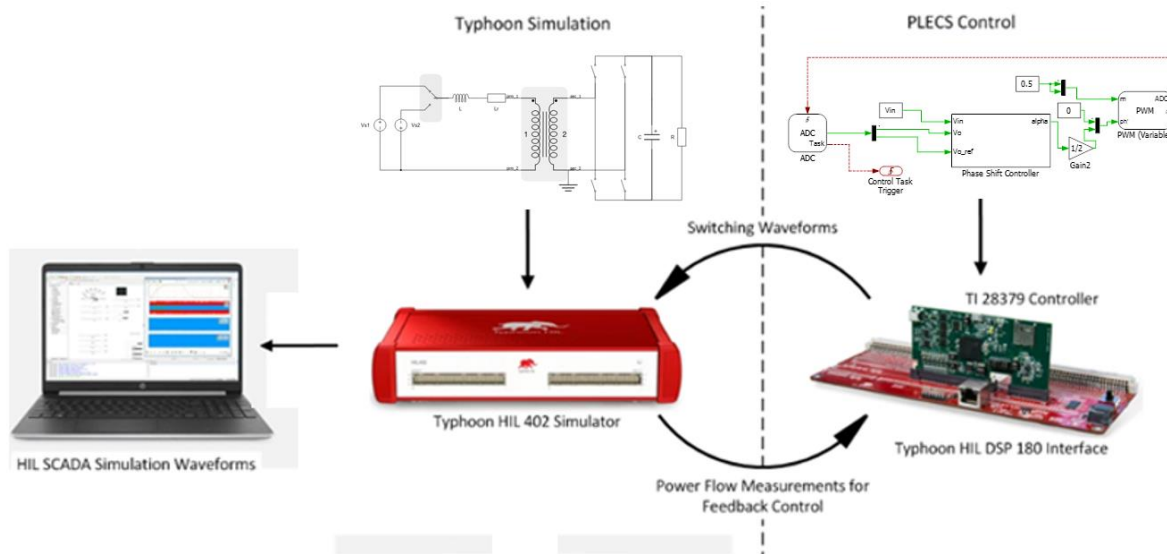


Figure 50: Typhoon HIL Experimental Setup

Two trials were performed. Trial #1 confirms that the PE scheme can detect the inductance value, and Figure 51 shows the PE will converge in under 1[ms]. The parameter estimator requires knowledge of the dc bus voltages and the high frequency transformer current measurement.

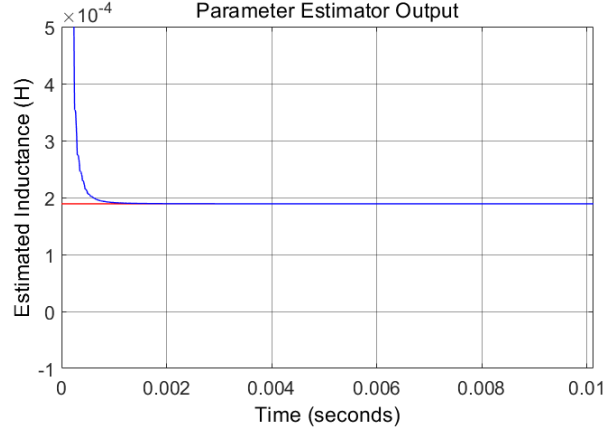


Figure 51: Estimated Inductance (blue) vs Modeled Inductance (red)

Trial #2 computes $K_{est} = \hat{L}/L$ from the PE inductance estimate \hat{L} and the original inductance value L , then will update the controller gains when the inductance changes beyond a set threshold. Figure 52 and Figure 53 show the large signal transient responses for an output voltage reference change. When $K_{est} = 1$, the inductor is at its nominal value (189 μ H). As the inductor deviates from nominal (due to purposeful tuning of the model parameters in this CHIL experiment), the value of K_{est} is updated by the PE. The controller updates gains K_1 and K_2 to ensure a critically damped response in all scenarios of K_{est} .

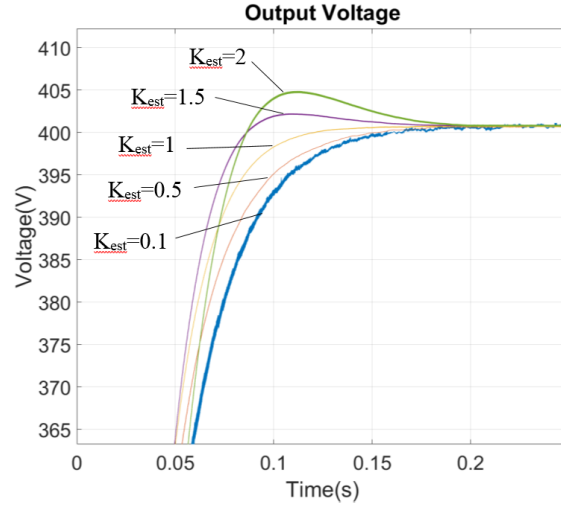


Figure 52: Large Signal Transient without Parameter Estimator

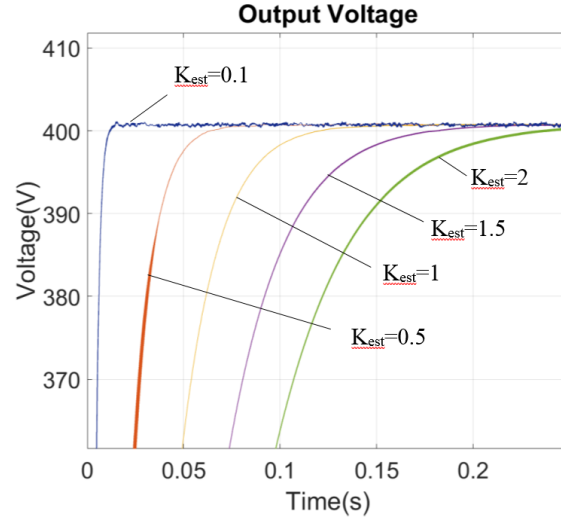


Figure 53: Large Signal Transient with Parameter Estimator and compensation for values of $K_{est} = \hat{L}/L$.

3.5 Conclusions and Discussions

Section 3.0 introduced observer and parameter estimator techniques that could be utilized to enhance the control performance for a DAB converter. A current observer was introduced,

which estimated the ac current across the transformer windings using knowledge of voltages, switching signals, and inductance values. With the current observer to estimate the value of the ac current, a control scheme was introduced to compensate in the event of a dc current bias. The control scheme was modeled and presented in PLECS.

This section also presented a parameter estimation scheme for inductance within a DAB converter using measured voltage and current values. The estimate of inductance was then used within an outer loop of the controller to facilitate a response to inductance changes in real time. This outer loop can be employed within a variety of controller architectures. The control strategy is useful in a variety of applications, from gain tuning for increasing controller performance to enabling switched inductor combinations at different discrete power outputs. When considering the use of state-of-the-art tunable inductors within DAB converters, a parameter estimation scheme such as the one presented will provide necessary feedback for the control system.

4.0 Research Plan: Objective #3 – Finite Element Analysis of 3-Winding Transformer within a Triple Active Bridge Converter

The purpose of Objective 3 is to model the behavior of a 3-winding transformer within a triple active bridge converter test bed. This project is an analysis of the 1kV-rated triple active bridge converter test bed at the Energy Innovation Center at the University of Pittsburgh. With the ongoing trend to increase voltage and power flow ratings of SST devices, the test bed is expected to be a critical experimental station for future projects. The finite element analysis will estimate the magnetic performance of the transformer to give confidence of operating behavior before a full power test. Two separate winding configurations will be evaluated for the transformer, and the model itself will be created within the FEMM finite element analysis software.

4.1 Literature Review

Converters containing multi-winding transformers are becoming highly studied in academic, government labs, and early corporate R&D environments. The galvanic isolation inherent to transformers make them desirable in scenarios where reliability and fault safety are a priority. Multi-winding transformers can also be used to increase the operational voltage, such as utilizing 4-port DAB converters to achieve medium voltage ranges [63].

Multiport converters are desirable for applications where multiple buses or sources are interconnected [30]. This has been especially beneficial for distributed generation paired with energy storage to interface with the grid [21], [64]. As DC networks reach medium voltage levels,

such as proposed in [11], it becomes important to have the capability to segment the network in such a way that parts of the network can be deactivated while the rest of the network remains online. Figure 54 provides an example MVDC network where pumped hydro, wind, battery, solar, and HVDC all connect into MVDC networks which interface with the traditional AC grid. A 3-port converter will lend itself well to this application, where power flow rates continuously change.

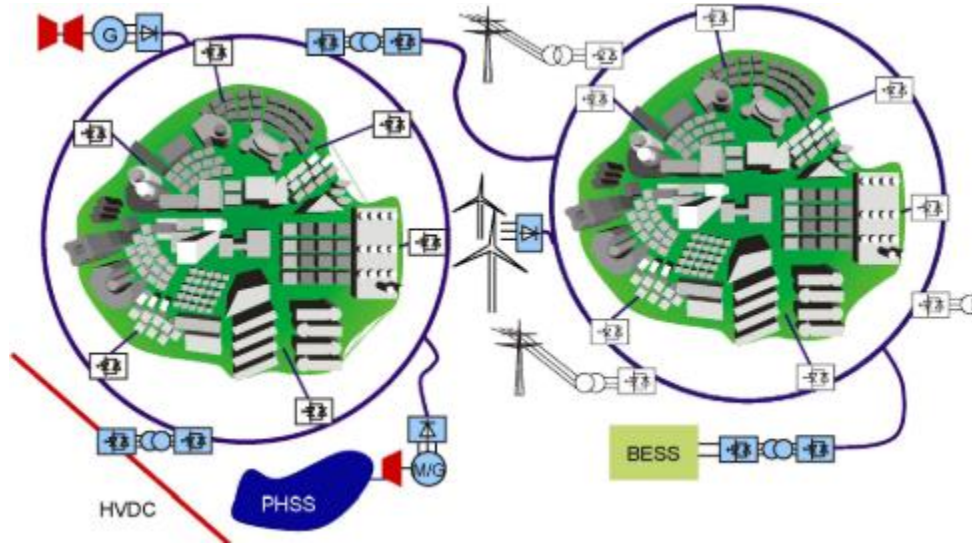


Figure 54: Proposed multi-terminal DC network [11]. Note that 3-port converters could be used to decouple parts of the DC network in case maintenance or an outage occurs.

With the key benefits of the 3-port DAB converter established, it becomes important to understand exactly how the converter performs as the power flow at each port varies. Circulating flux and currents could occur, which would increase losses and reduce overall efficiency and lifetime of the converter. In general, for a 2-port DAB circulating currents can be reduced or eliminated altogether by either modifying hardware (which will limit the converter operating range), or by use of control [65]. This same principle applies to the 3-port DAB, but with increased complexity due to magnetomotive force being shared among 3 windings instead of 2.

The triple active bridge converter test bed was a product of the National Energy Technology Laboratory's SuNLAMP project. At present, this project demonstrates one of the

highest voltage TAB converter prototypes in existence. The aim of Objective #3 is to evaluate the transformer hardware within the converter to provide an understanding of flux paths and behavior under various operating conditions.

4.2 TAB Circuit Topology

The circuit topology used in this study will be a 3-port dual active bridge, often called a triple active bridge. The operating parameters of the TAB converter will then be used as inputs in the finite element analysis model. The proposed circuit is shown in Figure 55 and has a DC voltage source V_{DC1} which feeds 2 bidirectional load buses. Each port has a full H bridge connected to its respective transformer winding. The voltages across the primary, secondary, and tertiary windings are v_1 , v_2 , and v_3 , respectively. S_{x-yy} denotes the switch, where x is the port number and yy designates which switch it is within the H bridge. Each load port has its own bus capacitor (v_{Co2} or v_{Co3}), load ($LOAD2$ or $LOAD3$), and distributed generation source (i_{DG2} or i_{DG3}). The distributed generation sources are included to demonstrate how a bidirectional power flow situation could result.

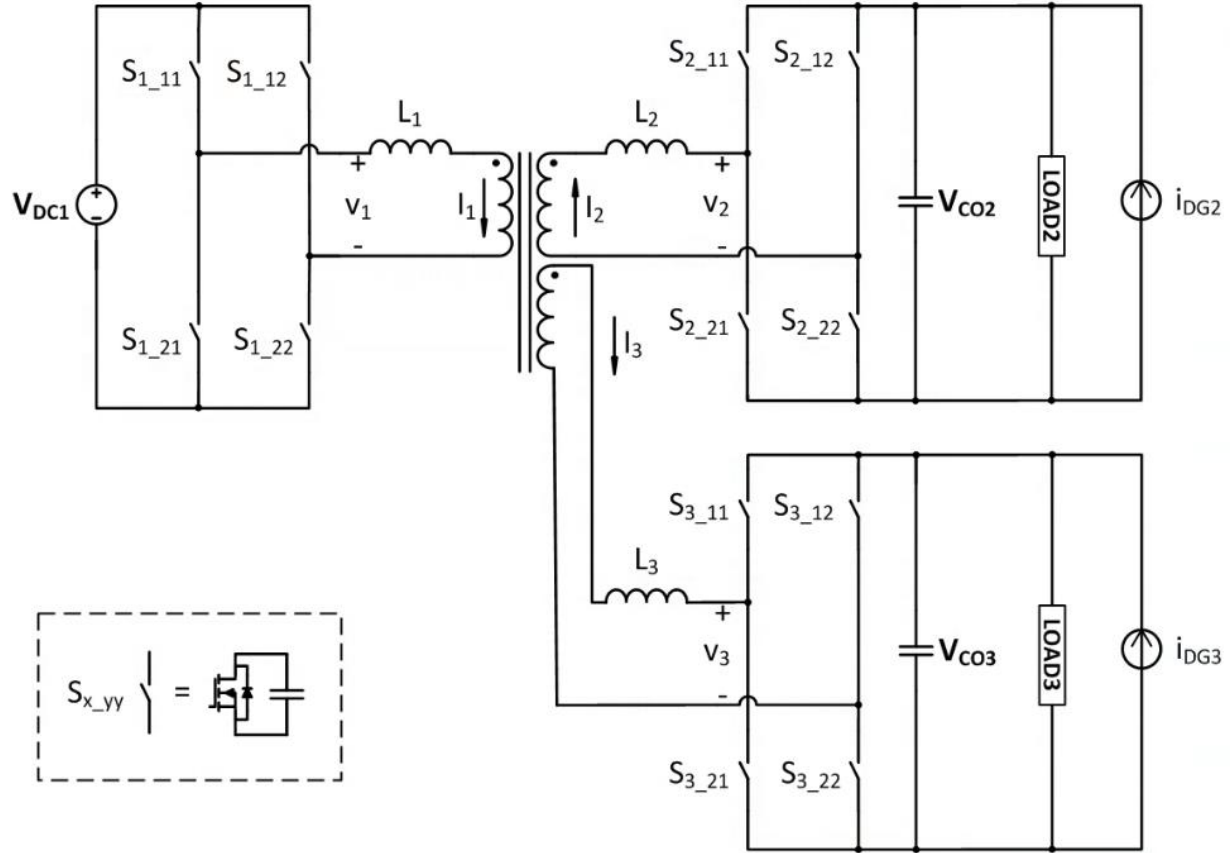


Figure 55: Triple active bridge converter topology

4.2.1 Circuit Control

The power flow equations for a triple active bridge converter are well known from [18].

The power flow equation for a DAB without duty cycle control is:

$$P = \frac{V_1 V_2}{n \omega L} \varphi \left(1 - \frac{|\varphi|}{\pi} \right) \quad (4-1)$$

Using techniques in [18], the converter model can be converted into the delta model as shown in Figure 56. Doing so allows (4-1) to be used in power flow computations between each port.

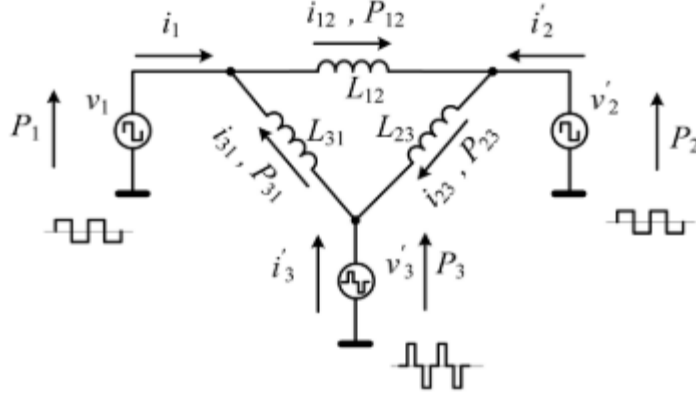


Figure 56: Delta model of triple active bridge converter [18]

The standard control described in [18] is proposed as the reference control for Objective #3. Since Objective #3 is focused on modeling the transformer performance, the controller itself will not be modeled. Instead, selecting a type of control is necessary to know the high frequency current experienced by the transformer. Some advanced control techniques for the TAB converter include peak current control, which will reduce the overall stress upon the transformer. Since the standard single phase shift control is typically a ‘worst case scenario’ condition for transformer current, this type of control was referenced when computing the current within the transformer.

4.3 Finite Element Model

The transformer model was built within the FEMM software. First, to get dimensions measurements were taken of the physical transformer. Figure 57 shows the test bed transformer. The transformer specifications were designed as part of NETL’s SuNLaMP project and are given in Table 4. Further details about the transformer design can be found in [35].

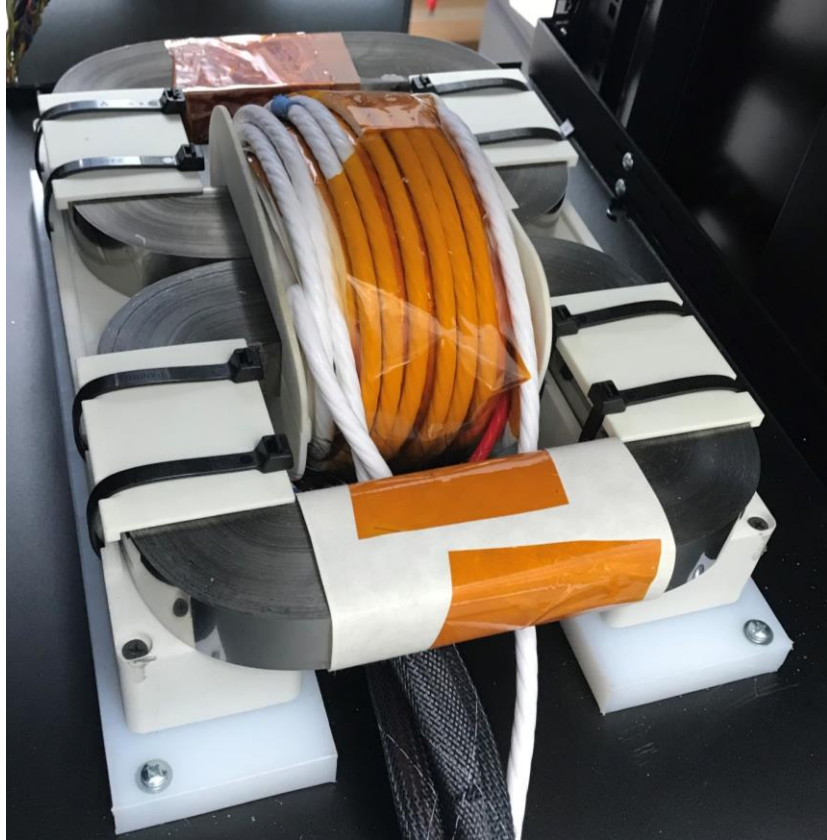


Figure 57: 3-Winding Transformer for Triple Active Bridge Converter

The transformer consists of two separate core loops. The core can be considered shell type with a concentric windings around the center of the core. The core material is ferrite ribbons. Manufacturing the core material into ribbons means that the flux is likely to travel along the path of the ribbon instead of traveling between ribbon layers. The benefit to this approach is that flux at the outer edges has a higher reluctance path to traverse towards the inner edges, which keeps a more uniform flux density and reduces the flux density at the inner edges of the core. This anisotropic behavior is important to capture within the materials definition of the FEMM model. The bobbin acts as a shield between the core and the windings. The windings themselves are 4 and 6 gauge litz wire. The FEMM model was developed and is shown in Figure 58.

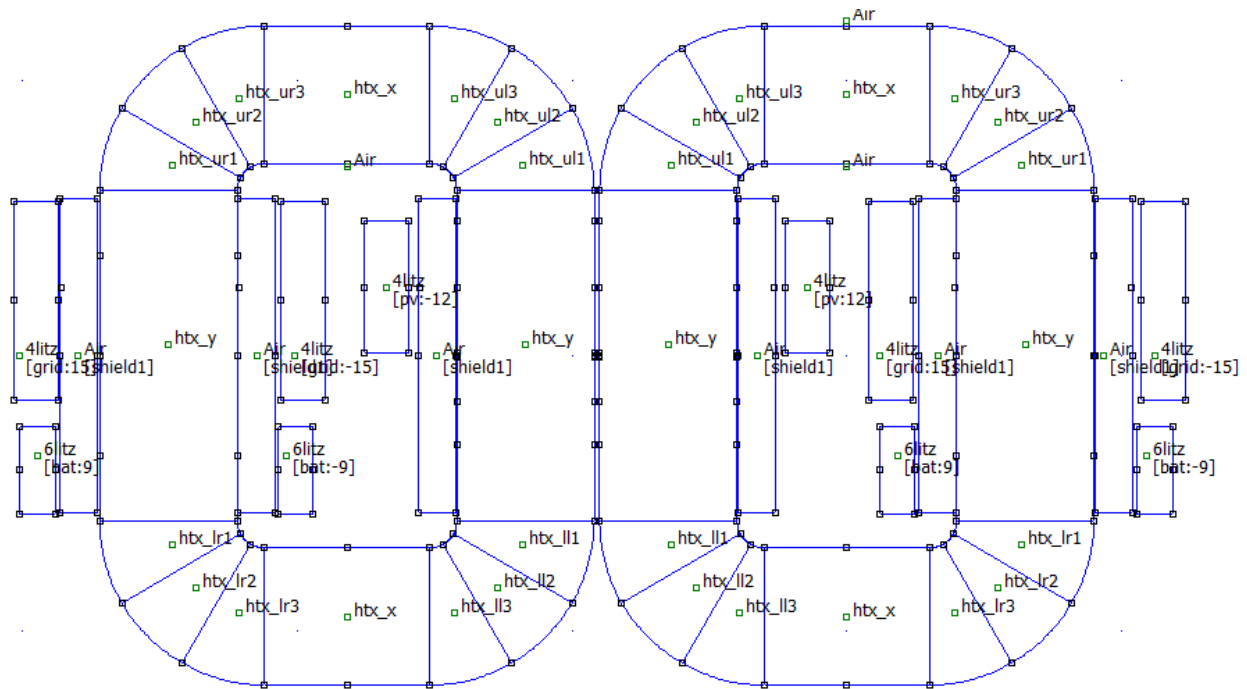


Figure 59: FEMM Model of Split-Winding Configuration for 3-Winding Transformer

4.4 Finite Element Analysis Results

The finite element analysis was ran for various scenarios of power flow at each port. To compute the current values for the simulation, the following formula was used:

$$I_{RMS} = \frac{P_{avg}}{V_{RMS}} \quad (4-2)$$

Since the applied voltage to the windings is an ideal square wave with amplitude equal to the bus voltage, then V_{RMS} is equal to the bus voltage. From Table 3, the RMS voltage at the PV bus is 800V, at the battery bus is 600V, and at the load bus is 1,000V. Three power flow scenarios were evaluated for both winding configurations. The parameters for the three scenarios are given in

Table 6. PV power is defined as positive when power is delivered by the PV port. BAT and OUT power is defined as positive when power is consumed by the BAT and OUT port.

Table 6: Finite Element Analysis Scenarios

Scenario	PV Power	BAT Power	OUT Power	PV Current	BAT Current	OUT Current
1	50kW	0kW	50kW	62.5A _{rms}	0A _{rms}	50A _{rms}
2	25kW	-25kW	50kW	31.25A _{rms}	-41.6A _{rms}	50A _{rms}
3	50kW	25kW	25kW	62.5A _{rms}	41.6A _{rms}	25A _{rms}

The scenarios are shown below in Figure 60 through Figure 65. Each scenario has two winding configurations, the concentric wound configuration and the split-winding configuration.

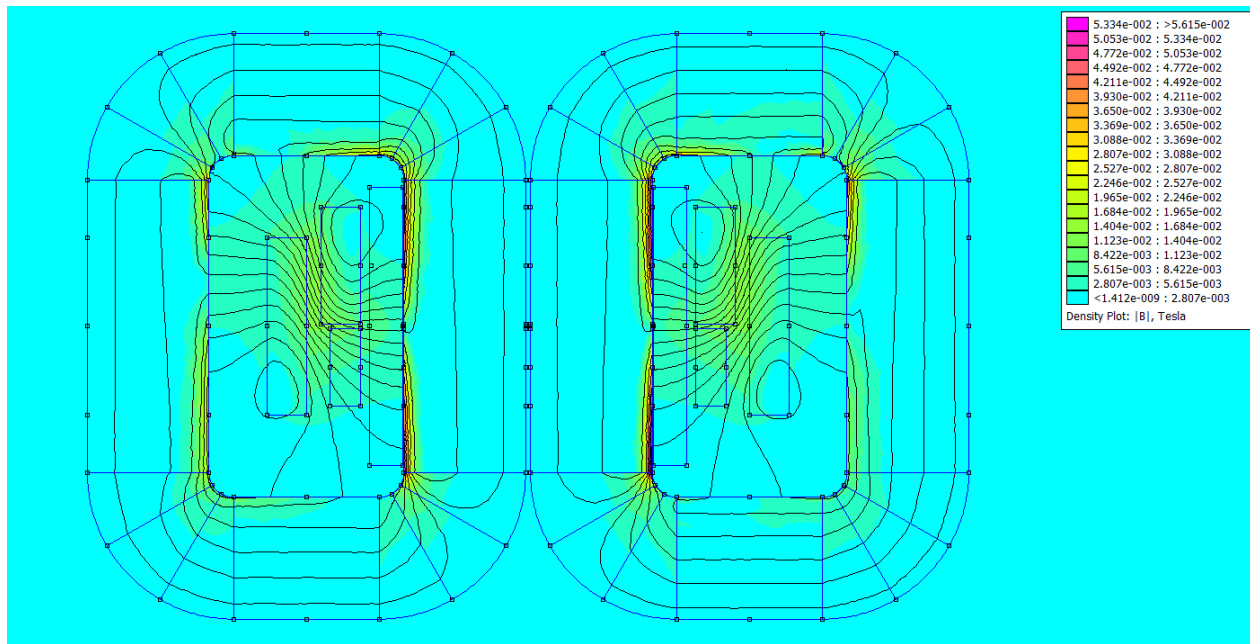


Figure 60: FEMM Simulation Results – Scenario #1, Concentric Wound Configuration

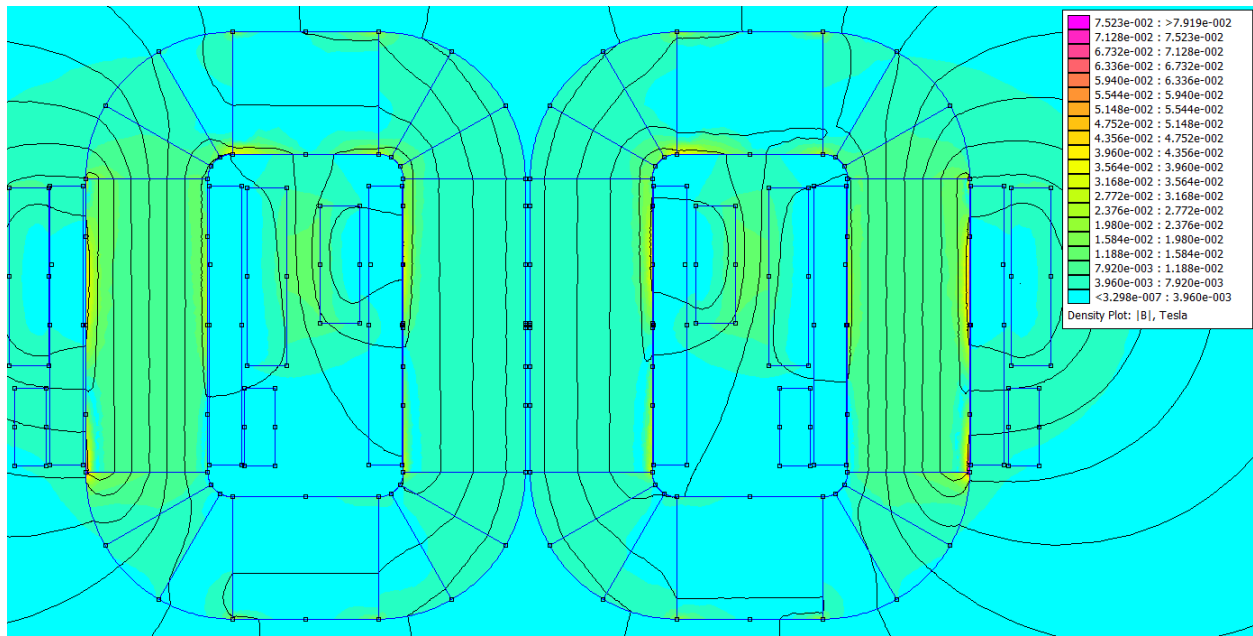


Figure 61: FEMM Simulation Results – Scenario #1, Split-Winding Configuration

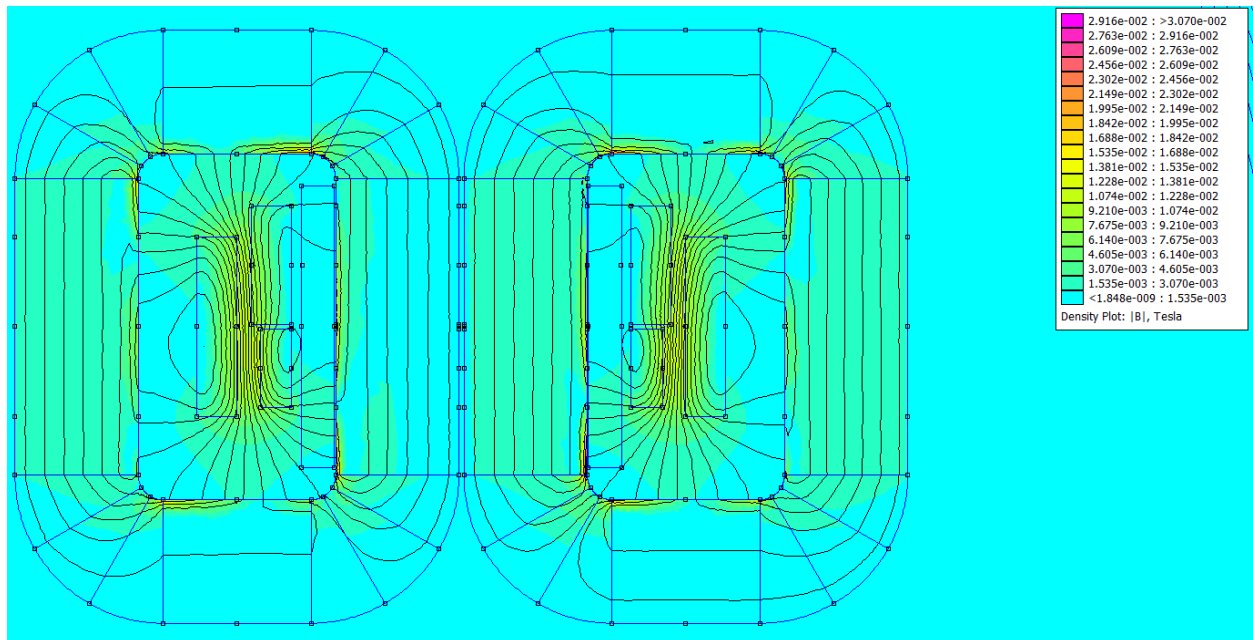


Figure 62: FEMM Simulation Results – Scenario #2, Concentric Wound Configuration

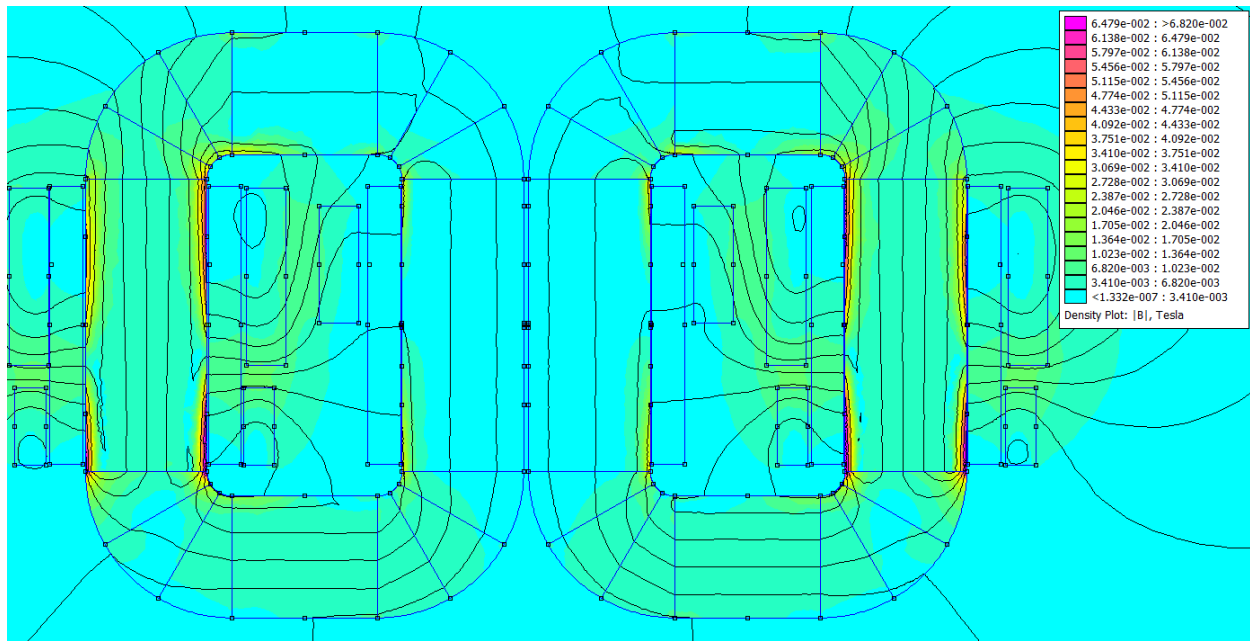


Figure 63: FEMM Simulation Results – Scenario #2, Split-Winding Configuration

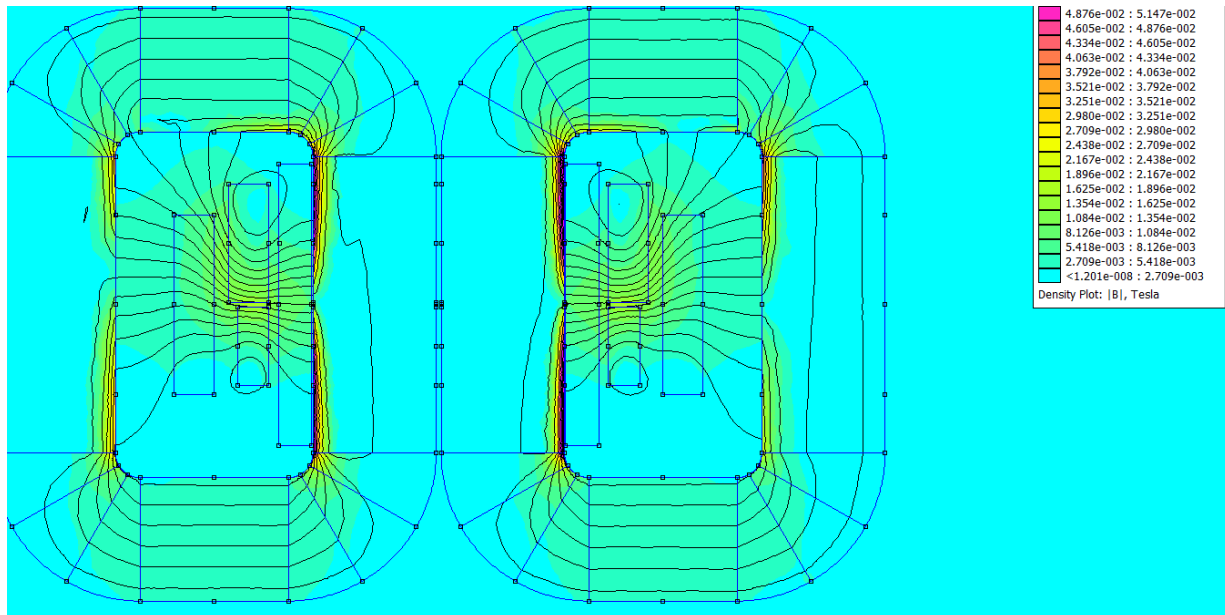


Figure 64: FEMM Simulation Results – Scenario #3, Concentric Wound Configuration

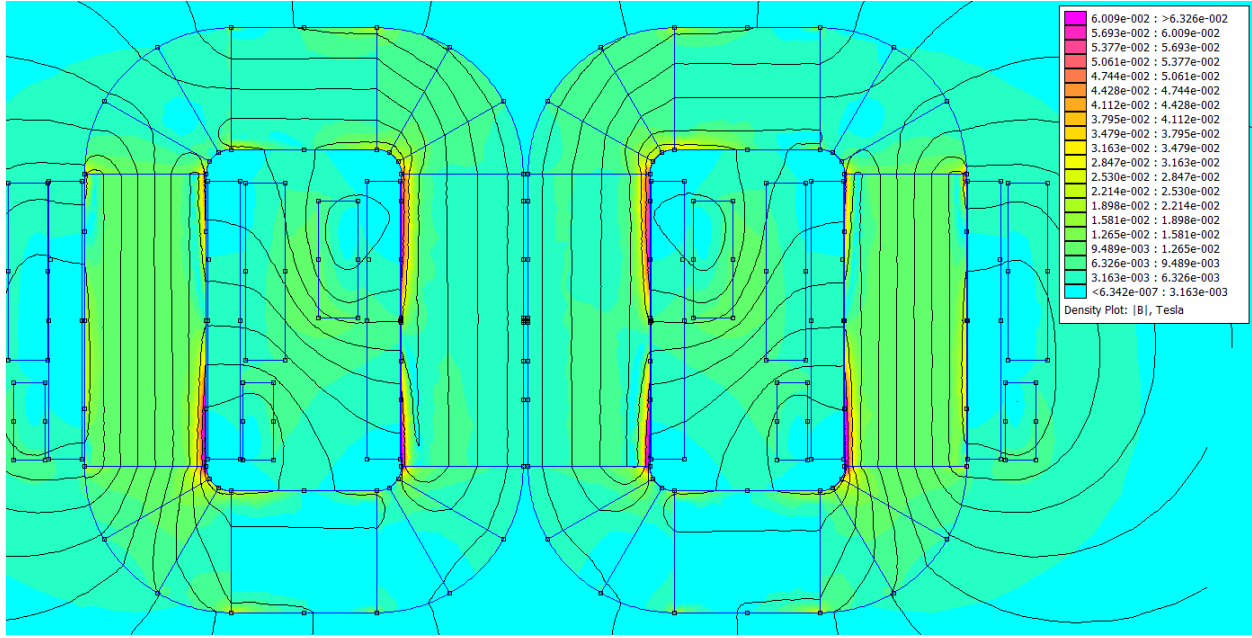


Figure 65: FEMM Simulation Results – Scenario #3, Split-Winding Configuration

A few key observations can be made from the results of the simulation. First, the split-winding configuration actually had a lower flux density peak for Scenario #1 than the flux density for the concentric winding configuration. For Scenarios #2 and #3 though, the flux density is higher in the split-winding configuration. From the magnitudes of the flux density, there isn't much difference between the two winding types. Another observation is that the concentric wound core seems to have a much more contained magnetic field. The split-winding configuration generates a magnetic field that extends beyond the physical transformer. With that in mind, the concentrically wound transformer would be a preferable winding configuration to reduce stray flux from generating electromagnetic interference.

The self-inductance of each winding was also evaluated. The results are given below in Table 7. From this information, more information can be gleaned about the parameters of the 3-winding transformer. The FEMM software also provides a method to extract the mutual coupling of inductance between each port. If the delta winding model is utilized, a the mutual inductance

can be used with the self-inductance results to determine the inductance values of the 3-winding transformer.

Table 7: Finite Element Analysis Scenarios and Self-Inductance

Scenario	Port 1 Self-Inductance	Port 2 Self-Inductance	Port 3 Self-Inductance
1	4.1 μ H	N/A	3.2 μ H
2	3.5 μ H	2.2 μ H	3.0 μ H
3	4.5 μ H	3.7 μ H	3.6 μ H

4.5 Conclusions

This finite element analysis provided a deeper understanding of the magnetic performance of the 3-winding transformer within the triple active bridge converter. A key factor that was noticed was how the concentrically wound configuration was able to capture stray flux much more effectively than the split-winding configuration. Since electromagnetic interference is a common concern with operating power electronics at the tens of kilohertz ranges, it is desirable to reduce stray flux as much as possible. One thing to notice as well is that this is a 2D finite element analysis tool, so stray flux traversing in the z-axis was not captured.

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