Dynamic Performance Improvement of Non-Isolated DC-DC converters and PV Energy Harvesting Systems using One Step Finite Control Set Model Predictive Control coupled with geometrical domain analysis

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The proposed research project uses the well-documented Model Predictive Control (MPC) framework to improve the dynamic performance of power converters and differential power processing (DPP) architecture with the help of geometrical domain analysis. The first research task is to implement a One Step Finite Control Set MPC (FCS-MPC) for a DC-DC boost converter. In the proposed control scheme, the cost function is built using time-optimal trajectories of the boost converter to solve the convergence issue brought by the non-minimum phase behavior of this system. The constraint of the proposed FCS-MPC limits important voltage deviations when using time-optimal trajectories. The second research task aims at proposing a generalized One Step FCS-MPC for the most common Non-Isolated DC-DC converters (buck boost and buck-boost). The proposed control scheme uses a unified switching model of non-isolated DC-DC converters and adapts the existing time-optimal boundary controllers to the FCS-MPC framework. The contributions are the avoidance of non-minimum phase issues, the limitation of voltage deviation and current spikes, and the possibility to target a specific steady state switching frequency. The third research task involves the implementation of FCS-MPC control schemes for the Differential Power Processing (DPP) PV-bus direct architecture. In this architecture a bidirectional Flyback is connected in parallel with each PV panel to operate a maximum power point tracking (MPPT). This system incorporates a string converter controlling the PV string current minimizing the power processed by bidirectional Flyback converters with a

Least Power Point Tracking (LPPT) algorithm. In this research task the classical direct duty cycle control MPPT is replaced by a FCS-MPC MPPT using geometrical domain analysis. The classical LPPT implemented with PI controllers is replaced by a FCS-MPC where the cost function is the power processed by the bidirectional flyback converters. The benefit is to avoid interactions between LPPT and MPPTs with an increase in the control dynamic performance. Overall, the proposed set of control schemes improves the minimization of power stress on bidirectional Flyback converters.

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Nomenclature

CCS-MPC	Continuous Control Step Model Predictive Control
DPP	Differential Power Processing
DPC	Direct Power Control
DTC	Direct Torque Control
EMPC	Explicit Model Predictive Control
FCS-MPC	Finite Control Set Model Predictive Control
FOC	Field Oriented Control
GPC	Generalized Predictive Control
HIL	Hardware-in-the-Loop
LPPT	Least Power Point Tracking
MILP	Mixed Integer Linear Programming
MIPS	Million of Instructions Per Second
MO-MPC	Multiobjective Model Predictive Control
MPPT	Maximum Power Point Tracking
MPC	Model Predictive Control
M^2PC	Modulated Model Predictive Control
MPP	Maximum Power Point
MP^3C	Model Pulse Pattern Predictive Control
NSS	Natural Switching Surface
OSS-MPC	Optimal Switching Sequence Model Predictive Control

OSV-MPC	Optimal Switching Vector Model Predictive Control
PWM	Pulse width Modulation
RHPZ	Right Half plane Zero
SVM	Space Vector Modulation
VOC	Voltage Oriented Control

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1.0 Introduction

1.1 Background

1.1.1 Emergence of Model Predictive Control in Power Electronics and Power Systems

The primary concepts of model predictive control (MPC) emerged in the 1960s as an application of optimal control theory [1] before finding industry applications in the 1970s [1]-[2]. In the late 1990, more than 4500 publications existed in the field of linear MPC in a diverse range of domains such as refining, petrochemicals, chemicals, food processing, aerospace and defense, mining and metallurgy as well as the automotive industry. [2]-[3]. In the meantime, power electronics and power systems field lately adopted MPC theory because of the limited processing power available. The reason is that MPC implementation requires to solve a control problem in real time which implies an important processing power when systems, such as power electronics systems, requires a small sampling period due to very short time constant. In fact, the first application of MPC theory in power electronics was related to high power systems with low switching frequency in the 1980s [4].

With the important increase in processing power illustrated in figure 1 and the advent of microprocessors, an increasing number of control schemes tied to MPC theory were created for power electronics systems as illustrated in figure 2 [5].

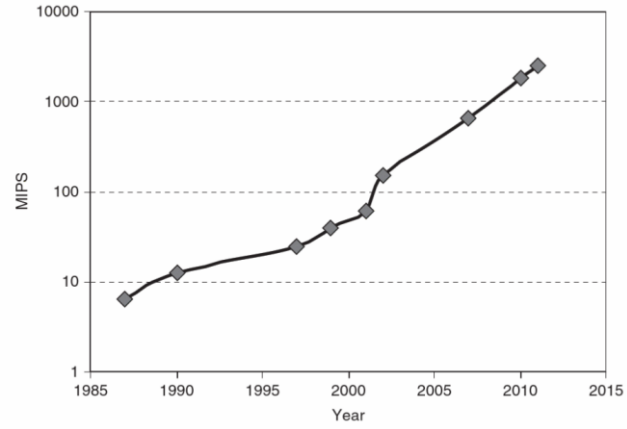


Figure 1: Evolution of Digital Hardware Processing Power in Million of Instruction Per Seconds (MIPS) [1]

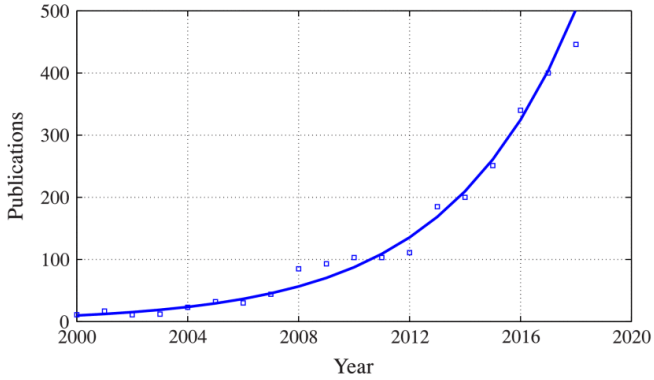


Figure 2: Evolution of annual MPC-related peer reviewed publications appearing in IEEE Xplore since 2000 (related to power electronic systems)

1.1.2 Existing Predictive Controllers applied to Power Converters and Drives

As illustrated by figure 3, MPC belongs to a larger family controller called predictive controllers. This type of controller uses a system model to predict the future behavior of the system to choose the best control decision.

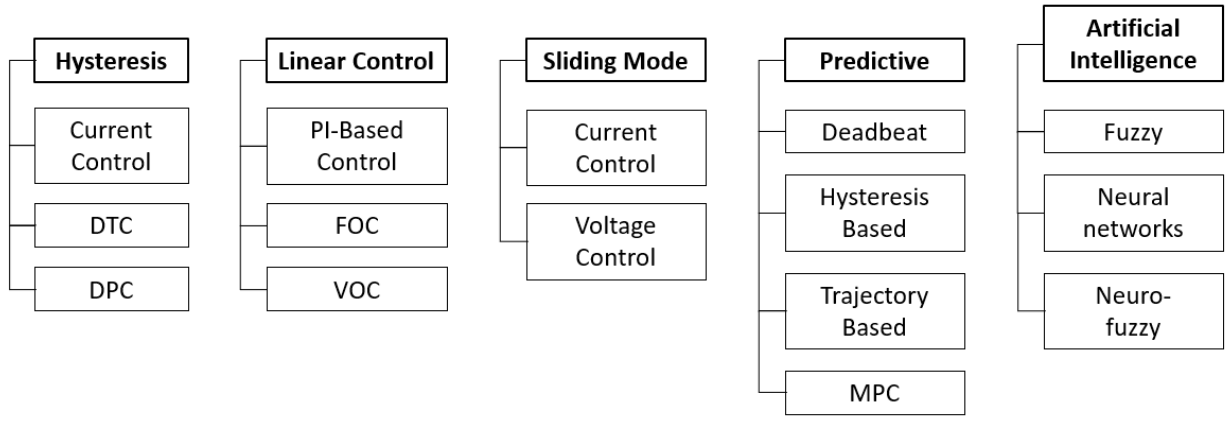


Figure 3: Classification of most common control schemes for power converters and drives [1], [6]

The difference between each type of predictive controller is the optimization criterion applied to generate the control signal. For deadbeat control schemes the optimization criterion is to reach the target output value or set the error to zero after a finite number of sampling instants [7]-[8]. While for hysteresis-based and trajectory-based predictive controller, the optimization intent is to maintain the system states inside a specific area and along a precalculated trajectory respectively [9]. For MPC, the optimization is tied to the minimization of a cost function symbolizing the control objectives set by the control designer.

1.2 Classification of Model Predictive Controls used in Power Electronics and Drives

As a starting point, let us consider a general power electronic system where $u \in R^{n_u}$ is the input vector (also called manipulated variables) and $y \in R^{n_y}$ the output vector (also called controlled variables) of the system. Both vectors **u** and **y** can contain real values as well as integer values.

In figure 4 presenting the different families of MPC, Continuous Control Set Model Predictive Control (CCS-MPC) refers to a type of MPC where the system is assumed be of continuous nature and the input vector u, resulting from the optimization, is composed of real valued components [11].

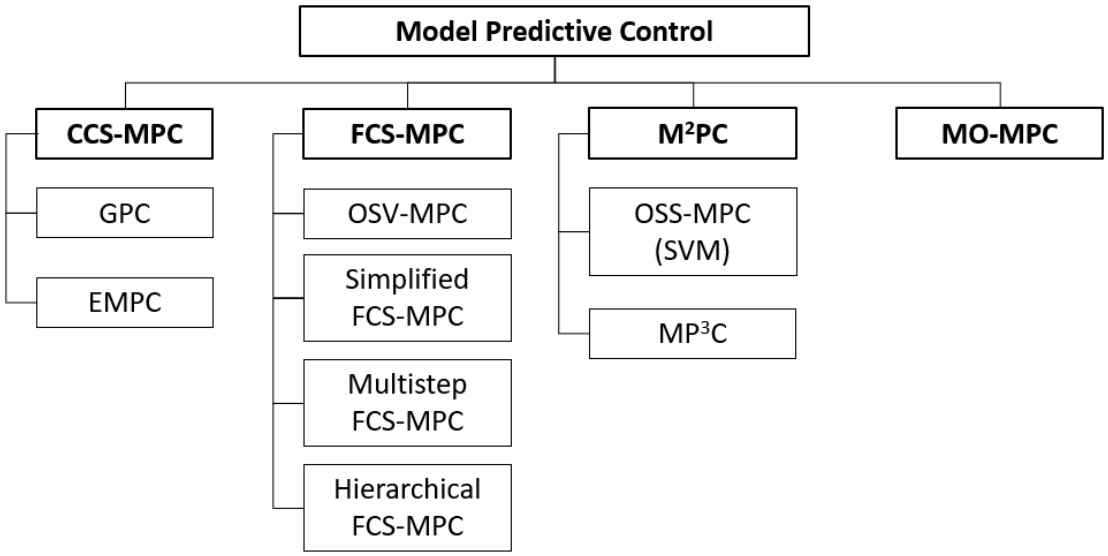


Figure 4: Classification of Model Predictive Controllers

In the context of power converters and drives, the presence of a continuous control signal is associated to the use of a modulator (e.g Space Vector Modulation (SVM) or Pulse Width Modulation (PWM)) that translates the control signal into gating signals driving semiconductor switches of the system. Because of the modulator, such control schemes in figure 5 are considered to be indirect control problem.

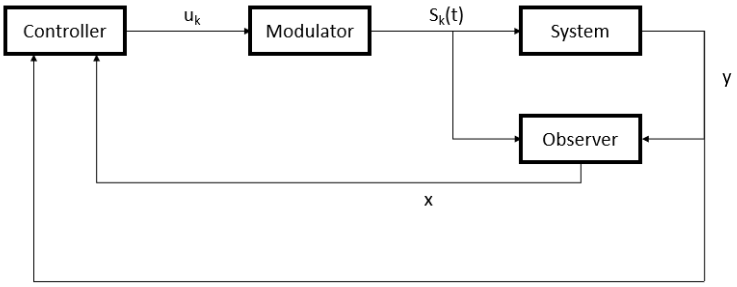


Figure 5: Indirect Control Scheme

The modulator also sets a fixed switching frequency for the system switches. To estimate the future behavior of the controlled system, the control stage requires the state vector $x \in R^{n_x}$ of the system. An observer is used to reconstruct the missing elements of the state vector using a model of the system fed with the control variable u. Observer estimation of state vector is specifically designed to converge to the real state vector by feeding back the difference between the response of this model and the actual output of the system to the controller.

The most common examples of CCS-MPC are the Generalized Predictive Control (GPC) and the Explicit MPC (EMPC). GPC is particularly suited for linear and unconstrained optimization problems [12]-[13]. EMPC solves the optimization problem offline to obtain an explicit control law stored in the form of a look up table. Therefore, the remaining online calculation effort is limited to a search algorithm applying the control law from the offline optimization [14]-[15].

The second family of Model Predictive Control presented in figure 4 is Finite Set Model Predictive Control (FCS-MPC) where the finite number of system states is considered in the MPC framework. This type of MPC is said to be a direct control problem since no modulator is required as in figure 6 and the output of the Model Predictive Controller is a specific switching state with a correponding input vector u.

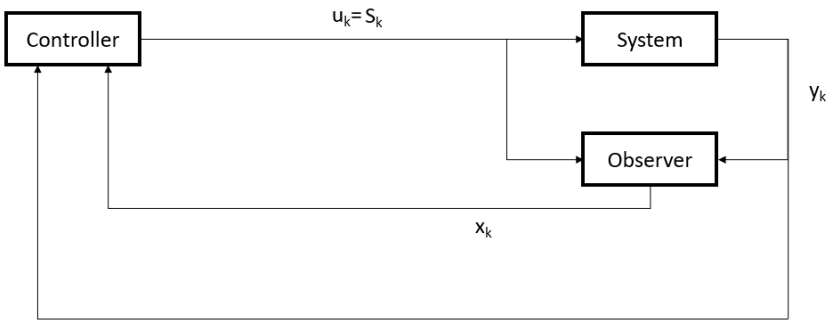


Figure 6: Direct Control Scheme

The first type of FCS-MPC is the optimal switching vector MPC (OSV-MPC) where each possible input vector u is evaluated thanks to a cost function symbolizing the control objectives [16]. The vector u associated with the minimum cost function is applied until the next sampling instant. This type of FCS-MPC is the most widely used in the FCS-MPC family because of its implementation and formulation simplicity. In the literature OSV-MPC is often referred as FCS-MPC since it was the first type of FCS-MPC to emerge in power systems application. The first drawback of OSV-MPC is the high computional cost required to solve optimization problem. The computation cost requirement can be mitigated with the use of simplified FCS-MPC [17]-[18], Multistep FCS-MPC [19]-[21] and Hierarchical FCS-MPC [22]-[25]. The second drawback is is the variable switching frequency since the same input vector can be used in two consecutives sampling instant for OSV-MPC.

This problem is solved by the Modulated MPC or MP^2C presented in figure 4 since this type of model predictive control includes a modulation scheme in the cost function. In the case of Optimal switching sequence MPC (OSS-MPC) only specific sequences of input vectors are considered in the optimization problem [26]-[27]. The SVM scheme determines which input

vectors and their application time to obtain a set of possible switching sequences. The switching sequence with the minimum cost function is applied until the next sampling instant. As the application times are associated with switching sequence, the switching frequency can be made constant. A different kind of modulation is explored combining the optimized pulse paterns concepts and Model Predictive Control framework to obtain the Model Predictive Pulse Pattern Control (MP^3C) [28].

The Multi-Objective MPC (MO-MPC) presented in figure 4 uses the multi-objective formulation to avoid the adjustment of the weighting factors composing the cost function [29]. The notion of weighting factor and its use in Model Predictive Control are explained in the next section.

The scope of this work is focused in the application of OSV-MPC, named FCS-MPC throughout this document, since this type of MPC is the most intuitive and easy to implement.

1.3 Basic Principles of FCS-MPC

This section presents the key design aspects of FCS-MPC to build a generalized MPC framework for the rest of this document. Five key attributes common to all MPC variations and formulations are defined in [2]:

- The internal dynamic model
- Cost Function (with weighting factors)
- Optimization Stage
- Receding horizon policy
- Constraints

The next subsections describe the key attributes defined above and the specificities brought by the FCS-MPC formulation. The first subsection describes the internal dynamic model while the second subsection describes the optimization stage along with the cost function and the receding horizon policy. Finally the last subsection describes the constraints of Model Predictive Control.

1.3.1 Internal dynamic model

The MPC formulation requires an internal dynamic model of the system to predict its future states and outputs and input the best control decision. This internal dynamic model is the state-space representation of the system in (1) for linear systems such as power electronic systems and drives where x, y and u are the same state, output and input vectors defined in section 1.2. $\boldsymbol{F}$, $\boldsymbol{G}$ and $\boldsymbol{C}$ are the system, input, and output matrix, respectively.

$$\begin{aligned} \dot{x} &= \boldsymbol{F}x + \boldsymbol{G}u \\ y &= \boldsymbol{C}x + \boldsymbol{D}u \end{aligned} \tag{1-1}$$

In the context of FCS-MPC, the system is controlled in the discrete domain with discrete variables $x(k)$, $y(k)$ and $u(k)$. The system of equations (1-1) can be discretized using the Forward Euler discretization of (1-2) to obtain (3) where T_s is the sampling period, $\boldsymbol{A} = \boldsymbol{I} + \boldsymbol{F}T_s$ and $\boldsymbol{B} = \boldsymbol{G}T_s$.

$$\dot{x} = \frac{x(k+1) - x(k)}{T_s} \tag{1-2}$$

$$\begin{aligned} x(k+1) &= \boldsymbol{A}x(k) + \boldsymbol{B}u(k) \\ y(k) &= \boldsymbol{C}x(k) + \boldsymbol{D}u(k) \end{aligned} \tag{1-3}$$

The purpose of system of equations in (1-3) is to predict the system states at next sampling instant $x(k+1)$ for each specific control decision $u(k)$, knowing the current system state $x(k)$.

1.3.2 Minimization of the Cost Function and Receding horizon policy

The control objectives set by the Model Predictive Control is expressed by the mean of the cost function, evaluating a specific control decision. A generalized formulation of the cost function is expressed in (1-4) mapping a set of input vectors $\boldsymbol{U}(k) = \begin{bmatrix} u^T(k) \\ u^T(k+1) \\ \vdots \\ u^T(k+N_p-1) \end{bmatrix}$ to a real scalar value over a finite *horizon* of N_P time steps.

$$J\big(x(k), \boldsymbol{U}(k)\big) = \sum_{l=k}^{k+N_p-1} \Lambda(x(l), u(l)) \tag{1-4}$$

(4) is the sum of stage costs $\Lambda(.,.)$ over N_P time steps ahead, each computed using the current state vector $x(k)$, as a starting point, cost and the elements of $\boldsymbol{U}(k)$ along with discrete-time dynamic model introduced in (1-3) to calculate each $x(l)$.[2] introduces the notion of *receding horizon policy* where only the first element of $\boldsymbol{U}(k)$ is applied and $\boldsymbol{U}(k)$ is recalculated at the next sampling instant. In the literature MPC are referred to be long horizon prediction as N_P gets higher providing better closed-loop performances than short horizon prediction where Np gets small or equals 1. However, increasing the length of horizon prediction worsen the computational cost required to implement the control scheme. A common usage is to express each stage cost as a linear expression of control objectives $J_i(x(l), u(l))$ in (1-5) for the time step l.

$$\Lambda\big(x(l), u(l)\big) = \sum_{i=1}^{n} \lambda_i J_i(x(l), u(l)) \tag{1-5}$$

Each λ_i is called a weighting factor and is a key design feature since it adjusts the trade-off between control objectives. A high weighting factor λ_i prioritizes the associated control objective J_i.

The minimization of the cost problem subject to the discrete time internal dynamic system and constraints on input, state and output vectors (detailed in the next section) can be formulated as mixed-integer linear programming (MILP) problem in (1-6).

$$\begin{aligned} U_{opt}(k) = \arg \underset{Uk}{minimize}\, & J\big(x(k), \boldsymbol{U}(k)\big) \\ & x(l+1) = \boldsymbol{A}x(l) + \boldsymbol{B}u(l) \\ subject\ to \quad & y(l) = \boldsymbol{C}x(l) + \boldsymbol{D}u(l) \\ & \forall l = k, \dots, k + N_p - 1 \end{aligned} \tag{1-6}$$

In the case of FCS-MPC (OSV-MPC), the input vector can only take a discrete number of values and the MILP problem is solved by calculating the cost function associated to each possible input vector and select the input vector with the minimum cost function.

1.3.3 FCS-MPC Constraints

In all MPC formulations and variations, state, output and input vectors can be restricted by the general constraints defined in (1-7) using bounded continuous set $\boldsymbol{X}$, $\boldsymbol{Y}$ and $\boldsymbol{U}$ where n_X, n_Y and n_U are the dimensions of the state, output and input vectors respectively.

$$\begin{aligned} x &\in \boldsymbol{X} \subseteq R^{n_X} \\ y &\in \boldsymbol{Y} \subseteq R^{n_Y} \\ u &\in \boldsymbol{U} \subseteq Z^{n_U} \end{aligned} \tag{1-7}$$

The constraints on state and output vectors are used to evaluate the state predictions from the internal dynamic model. In fact, if a predicted state or output is estimated to not respect the constraint, the associated cost function is set to infinity (hard constraint). Since the control

decision is taken based on the minimization of cost function, setting the cost function to infinity is equivalent to ignore the possibility to apply the associated control decision.

In the context of the FCS-MPC, only a discrete number of possible input vectors (corresponding to the number of switching states of a power electronic system) is considered. Therefore, in the case of FCS-MPC, the input vector constraint in (1-7) should be replaced by $\boldsymbol{U} \subseteq Z^{n_u}$.

1.4 Contribution

The first contribution of this work, mentioned as research task 1, is to apply geometrical domain analysis to design a Time Optimal One Step FCS-MPC for boost converter. The purpose in the use of geometrical domain analysis is to avoid the non-minimum phase behavior disturbing FCS-MPC schemes. The second purpose is to mitigate the large load transients when time optimal boundary control is used.

The second contribution, mentioned as research task 2, is to extend the previous FCS-MPC to non-isolated dc-dc converters using the unified switching model in geometrical domain.

The third contribution, referred as research task 3, aims at applying FCS-MPC to series PV-bus direct Bidirectional Flyback Differential Power Processing to improve the control dynamic performance and power stress minimization. The proposed control scheme is solving the interaction issue between Maximum Power Point (MPPT) Tracking and Least Power Point Tracking (LPPT) algorithm.

1.5 Thesis Organization

Section II develops the construction of cost function using natural trajectories, and constraint for the time optimal One Step FCS-MPC of DC-DC boost converter, also referred as research task 1. Section III generalizes the concepts of section II to common Non-Isolated DC-DC converters using a unified switching model. Section III is dedicated to research task 2 and formulates the cost function leading to a time optimal regulation and targeting a specific switching frequency. In this section, the proposed control scheme is validated using a Control Hardware-in-The Loop simulation. Section IV presents the proposed set of FCS-MPC of research task 3 for the series PV bus direct flyback bidirectional DPP. Section VI concludes this work with potential future research tasks.

2.0 Research Task #1-FCS-MPC for a DC-DC Boost Converter Ensuring Time Optimal regulation and Controlled Output Voltage Deviation

2.1 Literature Review and Motivation

Traditional linear controllers used for basic DC-DC topologies such as buck, boost and buck-boost converter use the small signal representation to obtain a linear representation of the system [1]. With this representation, useful analysis tools in the frequency domain were developed such as pole placement, root locus and bode plot [8]. However, for the boost converter, the input to output (output voltage) transfer function from small signal analysis contains a right half plane zero (RHPZ), limiting the dynamic performance of linear controllers. If a system's transfer function contains a RHPZ, the system is said to have a non-minimum phase behavior characterized by an initial undershoot in response to a step change [2] This behavior disturbs another type of control: the one step finite control set (FCS)-Model Predictive control (MPC) [2]-[5] In fact, a one-step FCS-MPC uses a mathematical model (predictive model) to estimate the converter states for the next sampling period for each control action. Because of the initial undershoot, the non-minimum phase behavior can mislead the one step FCS-MPC. To anticipate this behavior, the prediction horizon of the FCS-MPC can be extended [4], [6]. However, extending the prediction horizon increases the computational burden. Algorithms such as [7] aim at reducing this computational burden but increases the complexity of the FCS-MPC.

In response to the dynamic performance limitation of linear controllers mentioned earlier, geometrical domain analysis was developed as an alternative to the small signal analysis. Using the state plane where the x-axis represents the capacitor voltage and the y-axis the inductor

current, a geometrical point of view of the converter behavior is adopted. A typical geometrical based control uses a switching surface (SS) as a boundary to divide the state plane into areas that will condition the control action [8]. Such controllers are called boundary controllers because their development relies on a boundary in the state plane. A good example of boundary control is sliding mode control (SMC) using a first order SS to create a simple and robust control algorithm [9]-[12]. Because the transition along the first order SS is slow, other boundary controls using curved switching surfaces such as Second Order Switching Surfaces are used [13]. The dynamic response is improved when using this type of switching surface when compared to SMC but exhibits overshoots during start-up and large load transient. To solve the overshoot problem, boundary controllers using natural state plane trajectories of the boost converter as switching surfaces, also called Natural Switching Surfaces (NSS), are developed in [14] (boundary boost converter). The use of these switching surfaces ensures the converter to reach steady state in one switching action which represents a time optimal regulation [15], and a constant switching frequency. However, the proposed boundary control in [14] shows time optimal performances without considering an important dynamic performance factor-the output voltage deviation [16]. Those downsides are reduced in [17] merging geometrical domain analysis and averaging to create average natural trajectories. However, this strategy increases the control complexity compared to time optimal boundary control of [14].

As mentioned in section 1.1, MPC can include non-linear expressions and system constraints through the design of a cost function. The motivation behind this work is to use the geometrical analysis developed in [14] to formulate a cost function that will track specific time optimal trajectories within the proposed one step FCS-MPC. The proposed control scheme is designed to have the same dynamic performances as [14] while offering the possibility to limit

the voltage deviation setting a constraint on the FCS-MPC. Two main contributions can be listed since boundary controllers are improved by FCS-MPC as much as FCS-MPC benefits from the geometrical domain analysis. On one hand, geometrical analysis offers a solution to avoid the non-minimum phase behavior that perturbs the one step FCS-MPC. On the other hand, large voltage deviation from [16] can be limited with FCS-MPC constraints.

In Section 2.2, the normalization process of the boost converter to obtain a predictive model and Natural Trajectories of the converter is reviewed. Section 2.3 presents the dynamic performance indices from [16], specific to boost converter output voltage regulation. Section 2.4 recalls key aspects of time optimal boundary control using NSS from [14]. Section 2.5 of the paper describes the key aspects of the proposed One-Step FCS-MPC such as the predictive model, the cost function using Natural Trajectories tracking expressions, and input parameter constraint. Section 2.6 presents the results of the MATLAB simulation of the boost converter with the proposed control to validate the FCS-MPC design and compares its dynamic performance with the boundary controller in [14] using the dynamic performance indices of [16]. Section 2.7 presents the limitations of the proposed FCS-MPC from this section.

2.2 Boost Converter Normalization and Discrete Relationships

The behavior of the boost converter illustrated in figure 7 can be described with differential equations (2-1) and (2-2) where $u = 0$ when the MOSFET is OFF and $u = 1$ when the MOSFET is ON.

$$C\frac{dV_o}{dt} = (1-u)I_L - I_o \tag{2-1}$$

$$L\frac{dI_L}{dt} = V_{cc} - (1-u)V_o \tag{2-2}$$

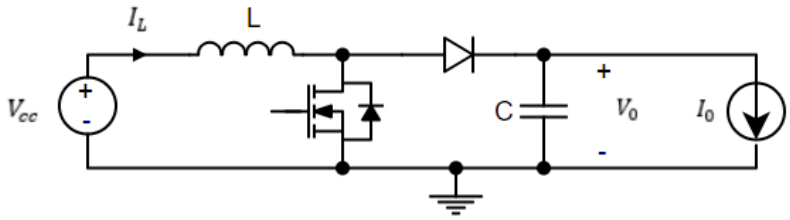


Figure 7: DC-DC boost converter

Continuous Conduction Mode is assumed in this work. The following base values were utilized to normalize the system of differential equations to obtain (2-3) and (2-4) where V_r is the desired output voltage setpoint.

$$V_{base} = V_r \qquad T_{base} = 2\pi\sqrt{LC}$$

$$Z_{base} = \sqrt{L/C} \qquad I_{base} = V_{base}/Z_{base}$$

$$\frac{1}{2\pi}\frac{dV_{on}}{dt_n} = (1-u)I_{Ln} - I_{on} \tag{2-3}$$

$$\frac{1}{2\pi}\frac{dI_{Ln}}{dt_n} = V_{ccn} - (1-u)V_{on} \tag{2-4}$$

From (2-3) and (2-4), the discretized relationships, listed as (2-5) and (2-6), are obtained to create a predictive model. T_{sn} represents the normalized sampling period of the inductor current and capacitor voltage.

$$V_{on}(k+1) = 2\pi T_{sn}\big((1-u)I_{Ln}(k) - I_{on}(k)\big) + V_{on}(k) \tag{2-5}$$

$$I_{Ln}(k+1) = 2\pi T_{sn}(V_{ccn} - (1-u)V_{on}(k)) + I_{Ln}(k) \tag{2-6}$$

Time Optimal Control framed by geometrical analysis relies on building time optimal trajectories in the state plane using natural trajectories of converter states in both switching modes (MOSFET ON or OFF). As shown in figure 8, a state plane analysis of the converter behavior gives a visual representation of the states trajectory when u is maintained at 0 (λ_{OFF}) or at 1 (λ_{ON}), corresponding to the OFF NSS and ON NSS of the converter, respectively.

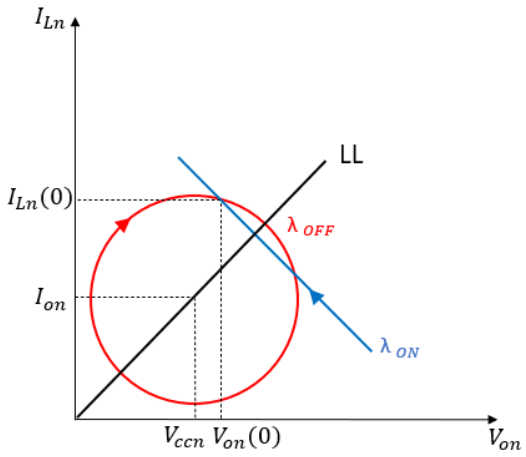


Figure 8:ON and OFF natural switching surfaces of the boost converter

Equations (2-7) and (2-8) are the analytical expression of the ON NSS and OFF NSS respectively, obtained by transformation of the time-domain solution of (2-3) and (2-4) as presented in [14].

$$\lambda_{ON}: I_{Ln} = -\frac{V_{ccn}}{I_{on}} V_{on} + I_{Ln}(0) + \frac{V_{ccn}}{I_{on}} V_{on}(0) \qquad (2\text{-}7)$$

$$\lambda_{OFF}: (I_{Ln} - I_{on})^2 + (V_{on} - V_{ccn})^2 = (I_{Ln}(0) - I_{on})^2 + (V_{on}(0) - V_{ccn})^2 \qquad (2\text{-}8)$$

With (2-5) and (2-6), it is possible to explain the orientation taken by the converter as each NSS represents 1 of 2 states in figure 2. The OFF NSS is a circle whose center is defined by the DC operating point (V_{ccn}, I_{on}) and whose radius is the distance between the DC operating point and

the point defined by the initial conditions (V_{on} (0), I_{Ln} (0)). The ON NSS is a line with a slope equal to $-\frac{V_{CCn}}{I_{on}}$ and intersects the initial condition coordinate.

The load line (LL) presented in figure 8 and in the equation below corresponds to the set of equilibrium points of the converter where the OFF NSS tangent and the ON NSS are identical.

$$LL: I_{Ln} = \frac{I_{on}}{V_{ccn}} V_{on}$$

2.3 Dynamic Performance indices for boost converter

Figure 9 illustrates the desired time optimal trajectory for different transient types to ensure MTC. All these trajectories are time optimal since each one of them is composed of only one ON NSS and one OFF NSS. This is equivalent to regulating within one switching action [15],[16].

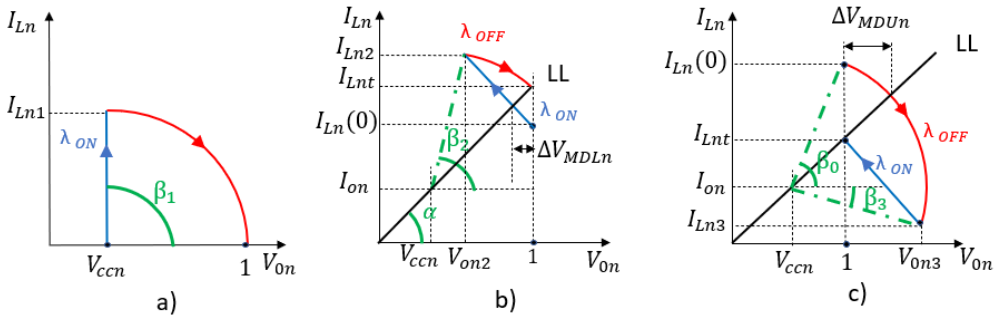


Figure 9: Time optimal trajectories for start-up (a), loading (b) and unloading (c) transient.

Three types of transients are considered in this figure: loading transient, unloading transient and start-up transient. The start-up refers to controlling the output voltage from a value equal to the

DC input voltage, V_{ccn}, to the desired output voltage equal to 1 when normalized. Loading and unloading transient scenarios refer to the converter response to an increase and a decrease in the load current I_0, respectively. In the two last transient cases, the voltage needs to be regulated to its reference value with a different target inductor current $I_{Lnt} = \frac{i_{on}}{V_{ccn}}$ resulting from the change in load current I_0.

In [16], theoretical performance limits of boost converters are developed to provide objective dynamic performance indices ranging from 0 to 1. Section 2.3.1 and 2.3.2 review the dynamic performance indices related to recovery time and voltage deviation for the three transient types mentioned above, respectively.

2.3.1 Voltage Deviation Performance Indices

Figure 9a shows that the minimum start-up voltage overshoot Δv_{OS} is zero. The difference between the desired output voltage and the initial output voltage, $V_r - V_{cc}$, is used as a reference in the voltage deviation index related to start-up transient *SOi* in (2-9).

$$SOi = \frac{V_r - V_{cc}}{V_r - V_{cc} + 2\Delta v_{OS}} \tag{2-9}$$

Figure 9b and 9c illustrate the minimum voltage deviation during a loading transient Δv_{MDLn} and an unloading transient Δv_{MDUn}, respectively. In both cases, the minimum deviation is achieved once the load line has been reached. Thanks to this observation, Δv_{MDLn} in (2-10) and Δv_{MDUn} in (2-11) are geometrically calculated.

$$\Delta v_{MDLn} = \frac{(i_{Lnt} - i_{Ln}(0))i_{Lnt}}{1 + {i_{Lnt}}^2} \tag{2-10}$$

$$\Delta v_{MDUn} = V_{ccn} - 1 + \sqrt{\frac{(i_{Ln}(0) - I_{on})^2 + (1 - V_{ccn})^2}{1 + {i_{Lnt}}^2}} \tag{2-11}$$

In (2-12), the minimum voltage deviation is used as a reference to objectively analyze the peak-to-peak voltage excursion $\Delta v_{pk-pk(L/U)}$ from the voltage regulation during a loading transient (subscript L) or an unloading transient (subscript U).

$$DR_{(L/U)} = \frac{\Delta v_{MD(L/U)}}{\Delta v_{pk-pk(L/U)}} \tag{2-12}$$

2.3.2 Recovery Time Performance Indices

The normalized minimum settling time during start-up transient (2-13) is calculated using the geometrical values from figure 9a (β_1 and I_{L1}) and (2-2), [16].

$$t_{MS_n} = \frac{i_{Ln1}}{2\pi V_{ccn}} + \frac{\beta_1}{2\pi} = \frac{1}{2\pi}\left(\frac{1}{V_{ccn}} - 1\right) + \frac{1}{4} \tag{2-13}$$

This minimum is used as a reference to objectively analyze the settling time,t_{start}, in (2-14).

$$ST_i = 1 - 0.5log\left(\frac{t_{start}}{t_{MS}}\right) \tag{2-14}$$

The minimum recovery time for a loading transient scenario requires determining the intersection point (i_{Ln2}, V_{on2}) (figure 9b) between the initial ON NSS and the target OFF NSS. With this point, β_2 and α can be calculated [16]. Using (2-2), the theoretical minimum normalized recovery time for a loading transient t_{MRL_n} is given in (2-15).

$$t_{MRL_n} = \frac{i_{Ln2} - i_{Ln}(0)}{2\pi V_{ccn}} + \frac{\beta_2 - \alpha}{2\pi} \tag{2-15}$$

A similar calculation is possible for the unloading transient to obtain the intersection point between the initial OFF NSS and the target ON NSS. (i_{Ln3}, V_{on3}) (figure 9c). After that, β_0 and

β_3 are computed to estimate the minimum recovery time for a given unloading transient in (2-16).

$$t_{MRU_n} = \frac{i_{Lnt} - i_{Ln3}}{2\pi V_{ccn}} + \frac{\beta_0 + \beta_3}{2\pi} \tag{2-16}$$

Equation (2-15) and (2-16) are used as a reference to inspect the loading (t_{recL}) and unloading transient (t_{recU}) recovery time, respectively, in (2-17).

$$RTi_{(L/U)} = 1 - 0.5\log\left(\frac{t_{rec(L/U)}}{t_{MR(L/U)}}\right) \tag{2-17}$$

2.4 Time Optimal Boundary Control using NSS

The boundary control presented in [14] aims at ensuring a MTC during start-up and when the output voltage undergoes large load changes. The control scheme from [14], presented below, distinguishes two cases based on the capacitor voltage v_{on}. Each case has its own control law.

Case I: $\boldsymbol{V_{on} < 1}$

If $\sigma_1 > 0$, then $u = 0$, else $u = 1$

Case II: $\boldsymbol{V_{on} > 1}$

If $\sigma_2 > 0$, then $u = 1$

Where,

$$\sigma_1 = (i_{Ln} - I_{on})^2 + (v_{on} - V_{ccn})^2 - (1 - V_{ccn})^2 - \left(\frac{I_{on}}{V_{ccn}} - I_{on}\right)^2 - \Delta r^2 \tag{2-18}$$

$$\sigma_2 = i_{Ln} + \left(\frac{V_{ccn}}{I_{on}}\right) v_{on} - \left(\frac{I_{on}}{V_{ccn}} + \frac{V_{ccn}}{I_{on}}\right) \tag{2-19}$$

Control laws σ_1 and σ_2 are created replacing $V_{on}(0)$ by 1 and $I_{Ln}(0)$ by $I_{Lnt} = \frac{i_{on}}{V_{ccn}}$ in (2-8) and (2-7), respectively. Equation (2-18) is the relationship of the OFF NSS circle including the target point (1,I_{Lnt}) with an increment Δr^2 in its radius. Equation (2-19) is the relationship of the ON NSS containing the target point. Figure 10 illustrates control laws σ_1 and σ_2 in the state plane domain.

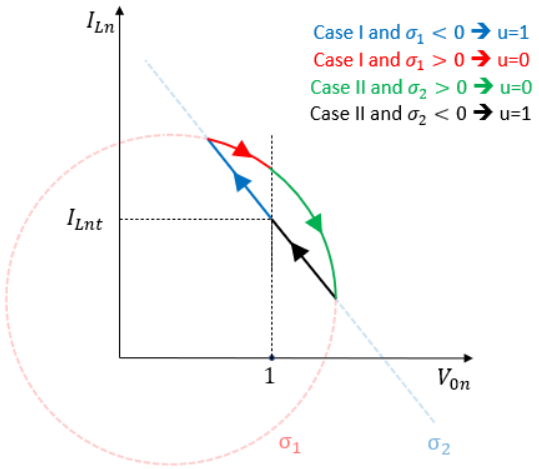


Figure 10: State plane representation of control laws from [14].

If the normalized capacitor voltage is inferior to 1 (case I), the MOSFET is kept ON if the converter states are inside the OFF NSS containing the point (1, $\frac{I_{on}}{V_{ccn}}$). Once the converter states reach the target OFF NSS, the MOSFET is turned OFF and the system evolves along the target OFF NSS. Then, once the normalized capacitor voltage is superior to 1 (case II), the MOSFET is turned ON when it reaches the ON NSS containing the point (1, $\frac{I_{on}}{V_{ccn}}$), putting the converter states back in case I.

The purpose of the increment Δr^2 is to have a control on the output voltage ripple in (2-20), inductor current ripple in (2-21) and switching frequency (2-22).

$$\Delta V_{on} = \frac{2\sqrt{\Delta r^2}}{\sqrt{1 + \left(\frac{V_{ccn}}{I_{on}}\right)^2}} \tag{2-20}$$

$$\Delta I_{Ln} = \frac{V_{ccn}}{I_{on}} \Delta V_{on} \tag{2-21}$$

$$f_{sw} = \frac{2\pi}{T_{base} \Delta V_{on}} I_{on}(1 - V_{ccn}) \tag{2-22}$$

The MOSFET is kept ON until reaching the target OFF NSS under start-up and loading transient as in figure. 9a and 9b. The MOSFET is kept OFF until reaching the target ON NSS under an unloading transient like in figure 9c. From these statements, the boundary control scheme ensures the MTC for start-up and large load changes.

2.5 Proposed Finite Control Set Model Predictive Control based on NSS tracking

The design of the FCS-MPC relies on three key features: the predictive model, a cost function representing the feature to be minimized and constraints on input variables used for the control. Equations (2-5) and (2-6) are used as the predictive model in the proposed FCS-MPC. Section 2.5.1 describes the cost function designed for time optimal control while section 2.5.2 presents the constraint on the output voltage deviation.

2.5.1 NSS Tracking Cost Function for Time Optimal Control

Figure 11 introduces vectors V_1 and V_2, useful for the cost function design, along with the expected time optimal trajectories.

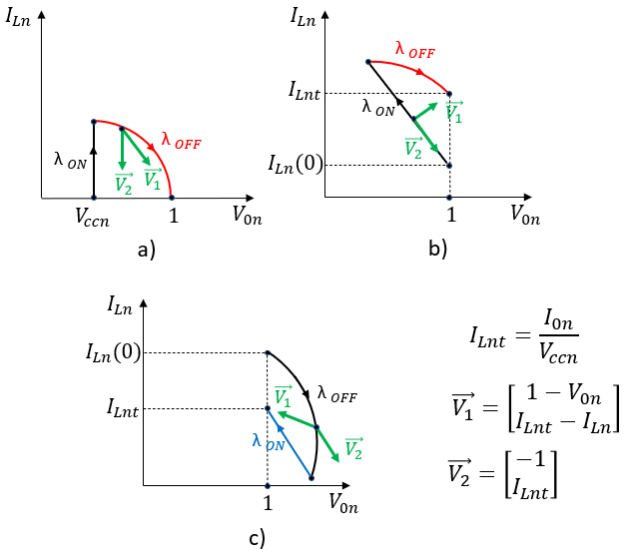


Figure 11: Ideal trajectories for MTC in state-plane domain for (a) start-up transient, (b) loading transient and (c) unloading transient

From this figure, two situations are considered. One scenario is illustrated in (a) and (b) where the state trajectory ends with an OFF NSS in red whereas the other scenario is illustrated by (c) where the state trajectory ends with an ON NSS in blue. Since the system offers only two possible switching positions, the first situation can be translated into tracking the OFF NSS containing the target point (1, I_{Lnt}) while the other situation is equivalent to tracking the ON NSS including the target point (1, I_{Lnt}).

The OFF NSS tracking is translated into a cost function term in (2-23), decreasing when the converter states evolve along the ideal trajectory of (a) under start-up conditions or (b) for a

loading transient, where $R^2 = (I_{Lnt}(k) - I_{on}(k))^2 + (1 - V_{ccn})^2$ and can be verified from the diagrams in figure. 11.

$$J_{ref_{OFF}}(I_{Ln}(k+1), V_{on}(k+1)) = \left|\left\|\overrightarrow{V_1}\right\|\left\|\overrightarrow{V_2}\right\| - \overrightarrow{V_1}.\overrightarrow{V_2}\right| + \left|\left(I_{Ln}(k+1) - I_{on}(k)\right)^2 + (V_{on}(k+1) - V_{ccn})^2 - R^2\right| \quad (2\text{-}23)$$

Similarly, the ON NSS tracking is expressed in (2-24) as a decreasing term when the converter states evolve along the trajectory in (c) for an unloading transient.

$$J_{ref_{ON}}(I_{Ln}(k+1), V_{on}(k+1)) = \left|\left\|\overrightarrow{V_1}\right\|\left\|\overrightarrow{V_2}\right\| + \overrightarrow{V_1}.\overrightarrow{V_2}\right| + \left|1 + I_{Lnt}(k)^2 - I_{Ln}(k+1)I_{Lnt}(k) - V_{on}(k+1)\right| \quad (2\text{-}24)$$

The first term of the addition in (2-23) and (2-24) uses a scalar product between a vector representing the orientation and direction taken by the tracked NSS at the target point (-$\overrightarrow{V_2}$ for ON NSS and $\overrightarrow{V_2}$ for OFF NSS) and a vector $\overrightarrow{V_1}$ going from the current position to the target point. In (2-23), this term will be minimized if $\overrightarrow{V_1}$shares the same direction and orientation as $\overrightarrow{V_2}$. Similarly, the first term of (2-24) is minimized if $\overrightarrow{V_1}$ shares the same direction and orientation as $-\overrightarrow{V_2}$.

The second term of the addition in (2-23) compares the square of the distance from the DC operating point and the current position with the distance from the DC operating point and the target point. Similarly, the second term in (2-24) refers to the distance between the x-intercept of the ON NSS tied to the current position and the x-intercept of the ON NSS tied to the target point.

To create the cost function (2-25), (2-23) and (2-24) are combined using a factor λ equal to 1 if the ON NSS tracking is enabled and 0 if OFF NSS tracking is enabled.

$$J = \lambda J_{ref_{ON}} + (1 - \lambda)\, J_{ref_{OFF}} \tag{2-25}$$

Figure 12 illustrates the mapping of the state plane domain with λ values. Lambda is equal to 1 if the converter states are located above the current target ON NSS on the state plane and 0 otherwise.

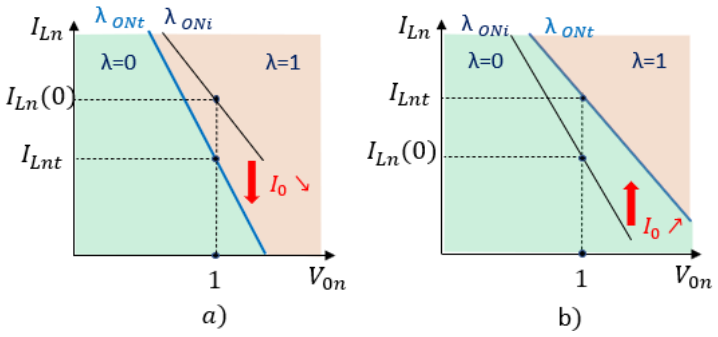


Figure 12: Lambda mapping when Io increases (a) or decreases (b) at t=0

In (a), the load current I_0 decreases at time t=0 when the normalized converter state is (1, $I_{Ln}(0)$) and assumed to be the objective point before I_0 changes. Before this change, the current target ON NSS tracked by the control scheme is λ_{ONi}.

The decrease in load current induces a decrease in the objective inductor current I_{Lnt} and the new ON NSS to be tracked becomes λ_{ONt} in light blue in figure 12a. The consequence is also a change in the mapping of λ values that corresponds at this instant to figure 12a. At t=0, the λ value is initially equal to 1, enabling the tracking of the target ON NSS to reach the reference voltage and current. Similarly, figure 12b presents the situation where the load current increases. In that case, I_{Lnt} increases and λ is initially equal to 0 at t=0.

2.5.2 Constraints of the proposed FCS-MPC

As the cost function reduction is made to ensure Time Optimal Control regardless of the voltage deviation, constraints on the maximum output voltage of the converter are set to limit this deviation. If the predicted output voltage for one switching structure leads to a voltage deviation greater than the maximum allowed by the constraint, then *J* is equal to infinity forcing the control to choose the other switching possibility. If both switching structures lead to an infinite cost function, the OFF-switching structure is chosen by default. However, the voltage needs to achieve a minimum deviation given by (2-10) and (2-11) to reach the target during a loading or an unloading transient, respectively. An important thing to consider for the constraint, in addition to the minimum deviation, is the voltage ripple. Equations (2-26) and (2-27) estimate this voltage ripple at the point of minimum voltage deviation for loading and unloading transient, respectively. From figure 9b and 9c, the voltages corresponding to the minimum deviation for loading transient $(1 - \Delta v_{MDLn})$ and unloading transient $(1 + \Delta v_{MDUn})$ are located on the load line (LL). Therefore, the inductor current can be deduced from these points. Using the inductor current, (2-5) can be used to estimate the maximum voltage ripple between ON and OFF switching decision for both loading transient in (2-26) and unloading transient in (2-27).

$$\delta_{Ln} = 2\pi T_{sn} \times \max\left(\left|I_{on} - \frac{I_{on}}{V_{ccn}}(1 - \Delta v_{MDLn})\right|, |I_{on}|\right) \tag{2-26}$$

$$\delta_{Un} = 2\pi T_{sn} \times \max\left(\left|I_{on} - \frac{I_{on}}{V_{ccn}}(1 + \Delta v_{MDUn})\right|, |I_{on}|\right) \tag{2-27}$$

The constraint applied is given in (2-28). It is expressed proportionally to the highest minimum voltage deviation, with the expected voltage ripple, between the loading and unloading transient case to ensure stable regulation in both transient scenarios. In (2-28), *p* is the variable

set by the designer to adjust the voltage deviation proportionally to the maximum of the minimum voltage deviation with its associated voltage ripple and must be greater or equal to 1.05.

$$|V_{0n} - 1| < p \times \max\left(\Delta v_{MDLn} + \delta_{Ln}, \Delta v_{MDUn} + \delta_{Un}\right) \quad (2\text{-}28)$$

The proposed FCS-MPC, including the predictive model, cost function and constraints defined above, is illustrated by the flowchart in figure 13 and is only applied to voltage regulation.

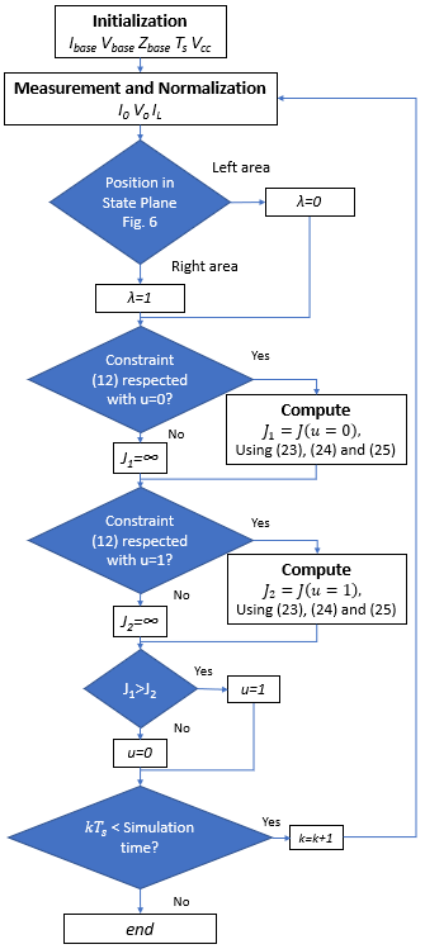


Figure 13: Proposed FCS-MPC Flowchart

The initialization step consists of offline calculations of base values essential for normalization. Then, I_o, V_o and I_L are measured at a sampling frequency of T_s and normalized. The first "if" condition attributes a value to λ based on the location of the converter states on the state plane. The second "if" condition uses the prediction from (2-5) and (2-6), when u=0, to determine if the constraint in (2-28) is respected for the OFF-switching decision. If this constraint is respected, the associated cost function J_1 is computed using (2-23), (2-24), (2-25) and set to infinity otherwise. The third "if" condition repeats this process for u=1 with its associated cost function J_2.In the fourth "if", the switching decision u is set to 1 if $J_2$is inferior to $J_1$and to 0 otherwise. Finally, the last "if" condition checks for the end of simulation and loops back to the measurement and normalization step. It is important to note that during start-up transients, the constraints are disabled and the second and third "if" conditions are forced to the "yes" path.

2.6 Simulation Results

This section compares dynamic performances of NSS control laws of [14] and the proposed FCS-MPC of figure 13. Both control schemes are implemented to regulate the output voltage of the DC-DC boost converter in figure 1 in Simulink with L=1.07mH, C = 267μF, V_{cc} = 10V, V_r = 22V and Ts = 25μs. Figure 14 illustrates the different time domain voltage transients from the NSS control laws of [14] and the proposed FCS-MPC without the voltage constraint.

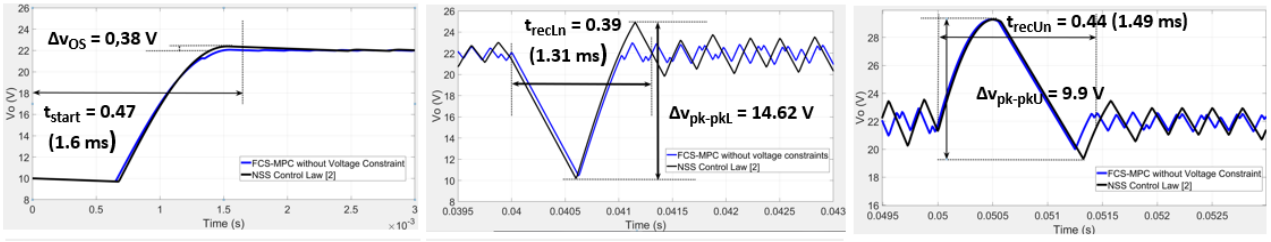


Figure 14: Simulation Results of the converter start-up transient (left) loading transient (center) and unloading transient (right) in the time domain using NSS control Laws of [6] (black) and proposed FCS-MPC without voltage constraint (blue))

The graph on the left of figure 14 is the start-up transient occurring at a constant I_0 = 0.12 A while the graph in the center shows the loading transient when I_0 is increased from 3.5 to 5A and the graph on the right shows the unloading transient when I_0 is decreased from 5 to 3.5A. This experiment aims at proving that the proposed cost function alone ensures a time optimal regulation.

Considering these load current changes, the dynamic performance of the proposed control without voltage limitation and the NSS control laws of [14] are compared in the web plot of figure 10a using benchmarking tools from section 2.3. From the experiment conditions of figure 14, the ideal settling time for start-up, loading and unloading transients are t_{MSn}=0.441, t_{MRLn}=0.305 and t_{MRUn}=0.320, respectively. The minimum voltage deviation for loading and unloading transient are Δv_{MDLn}= 0.15 and Δv_{MDUn}=0.17, respectively. Therefore, results from figure 16a show the proposed control without voltage constraints is a time optimal regulation like in [14] and exhibits the same underperforming dynamic regulation performance [16]. Figure 15 illustrates the different voltage transients in the time domain from the NSS control Laws of [14] and from the proposed control with a voltage constraint (p=1.1 in (2-28)) under the same conditions as figure 14.

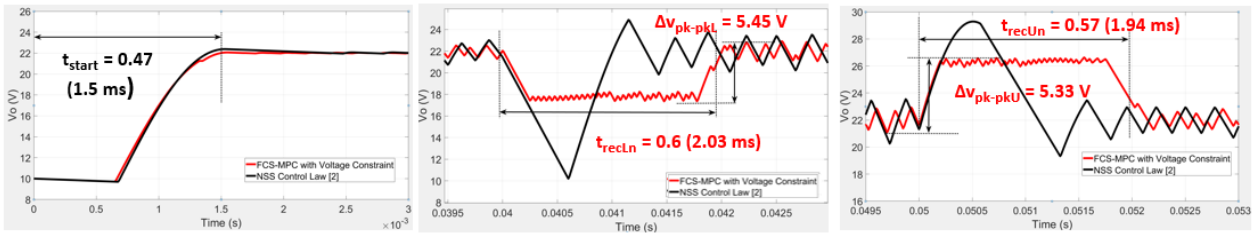


Figure 15: Simulation Results of the converter start-up transient (left) loading transient (center) and unloading transient (right) in the time domain using NSS control laws of [6] (black) and proposed FCS-MPC with voltage constraint (red)

The expected voltage ripple for the loading and unloading transient scenario with minimum voltage deviation are δ_{Ln}=0.021 and δ_{Un}=0.023. Therefore, the maximum voltage deviation constraint is set to 4.67 V from (2-28), meaning that the capacitor voltage is not allowed to elevate above 26.67 V or below 17.33 V. The web plot of figure 16b proves that the proposed FCS-MPC with voltage constraints ensures an improved dynamic regulation (DRi_U=0.6, DRi_L=0.73) and still excellent recovery time (RTi_L=0.85, RTi_U=0.86).

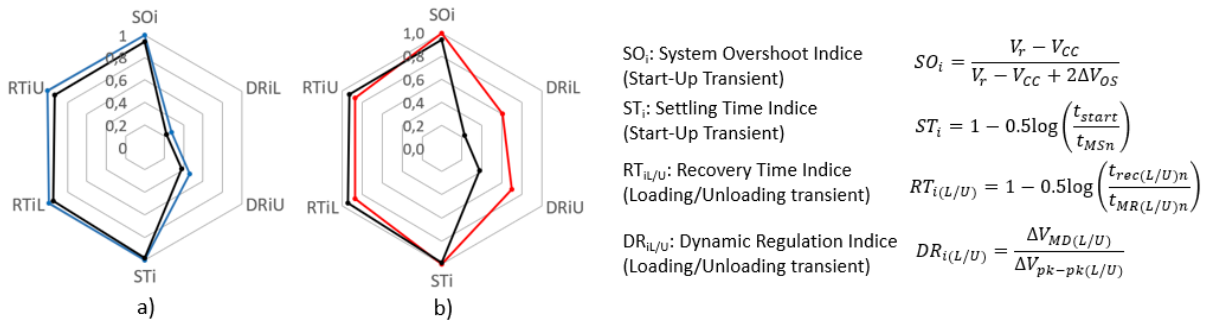


Figure 16: Benchmarking indices of (a) NSS control laws (black) compared with proposed FCS-MPC without voltage constraint (blue) and (b) NSS control laws (black) compared with proposed FCS-MPC with Voltage Constraint (red)

Figures 17 and 18 use the same color code as [16] to interpret the performance index value where green, yellow, orange, and red correspond to excellent, good, regular, and poor performance index, respectively. Figure 17 illustrates the evolution of performance indices related to the loading transient (RTi_L, DRi_L) and the unloading transient (RTi_U, DRi_U) as p is increased.

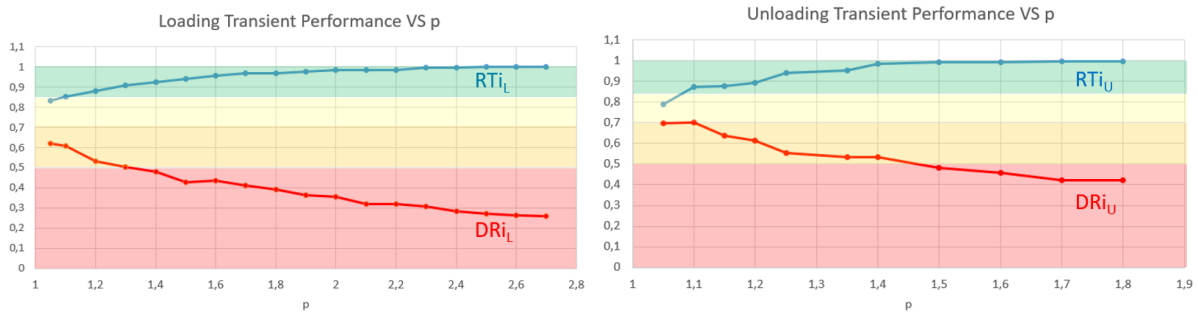


Figure 17: Evolution of loading (left) and unloading (right) transient performances with voltage deviation constraint.

As can be expected, the voltage regulation is faster (RTi_L and RTi_U closer to 1) as p is increased. Moreover, the strictest constraint applied (p=1.05) leads only to a regular performance for voltage deviation, with values below or equal to 0.7 for DRi_L and DRi_U, for two reasons. The first one comes from the minimum voltage constraint calculation based on the minimum voltage deviation for one type of transient in (2-28). If the difference between $\Delta v_{MDLn}$and Δv_{MDUn} is high, the maximum of the voltage deviation performance index for the other type of transient is highly impacted. In the context of the experiment, $\Delta v_{MDUn} + \delta_{Un} > \Delta v_{MDLn} + \delta_{Ln}$, the index performance DRi_L is decreased to make sure the minimum voltage deviation is respected during the unloading transient, explaining why DRi_L is systematically smaller than DRi_U. Finally, the switching period T_s has an impact on both margins δ_{Ln} and δ_{Un} which will impact the minimum

voltage deviation constraint. Additionally, as T_s increases, the steady-state voltage oscillation amplitude also increases which deteriorates the voltage deviation performance indices. Figure 18 represents the evolution of loading and unloading transient performances with switching period when the voltage deviation constraint is the strictest (p=1.05).

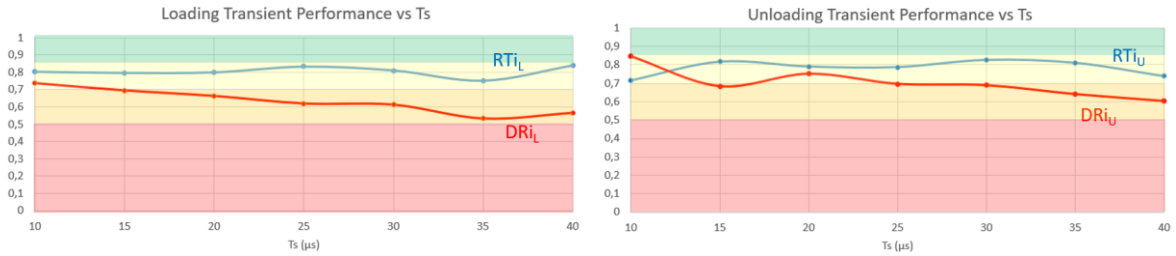


Figure 18: Evolution of loading (left) and unloading (right) transient performances with sampling period (p=1.05).

For both loading and unloading transient, the voltage deviation index is improved as the sampling period is decreased while the recovery time index remains good, oscillating around 0.8. In the context of the experiment, voltage deviation performance indices are equivalent to recovery time performance indices at a sampling frequency of 10µs.

2.7 Limitations

As the proposed FCS-MPC is applied for different operating points, one can notice that the performance related to settling time is degraded as the input voltage V_{ccn} is decreased as illustrated in figure 19. One of the time optimal FCS-MPC objectives presented in the next section is to solve this issue.

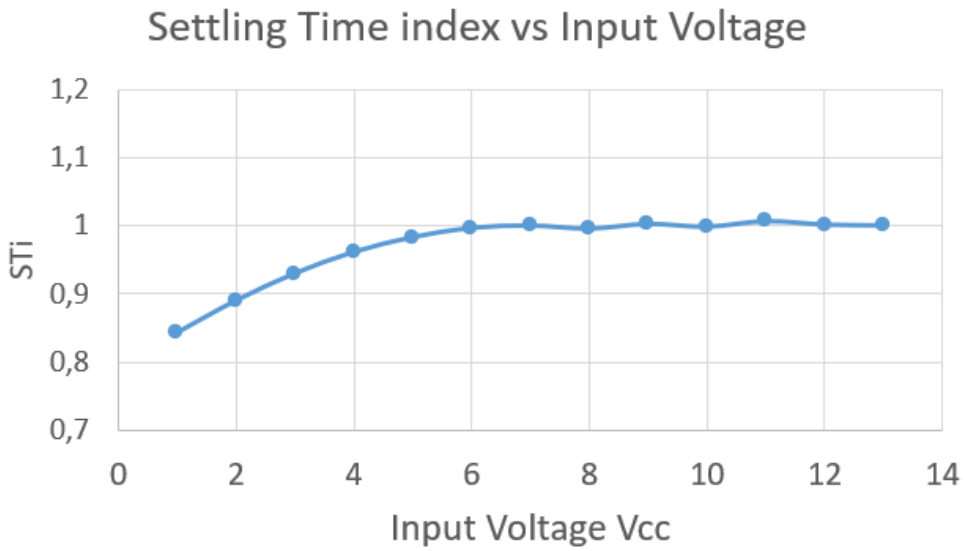


Figure 19: Impact of Vccn on the Settling Time Performance Index

3.0 Research Task #2-Unified FCS-MPC for non-isolated Synchronous DC-DC converter ensuring Time Optimal regulation, controlled output voltage deviation and inductor current overshoot

3.1 Literature Review and Motivation

In literature, a general approach of converter modeling is proposed in [17] where a unified expression of natural trajectory for all non-isolated converters is formulated. A similar time optimal boundary control is also proposed for buck [18]-[19] and buck-boost [20] converter as well as benchmarking indices like [16] for buck converters [21]. The first contribution of Objective 2 is to use the generalization brought by [17] and geometrical steady-state characteristic developed in [14] and [20] to formulate a cost function targeting a specific steady-state switching frequency. The second contribution is to reformulate the cost function to avoid the limitation in settling time dynamic performance.

3.2 Generalized Predictive Model and Natural Switching Surfaces

All three of the DC-DC converters from figure 20 can be modeled using generalized differential equations given in (3-1) and (3-2) where k_{ω}, m_1 and m_2 are different depending on the converter type (see Table I). In Table I, u is set to 0 or 1 if the MOSFET Q1 is OFF or ON respectively. The MOSFET Q2 is OFF when u=1 and ON when u=0.

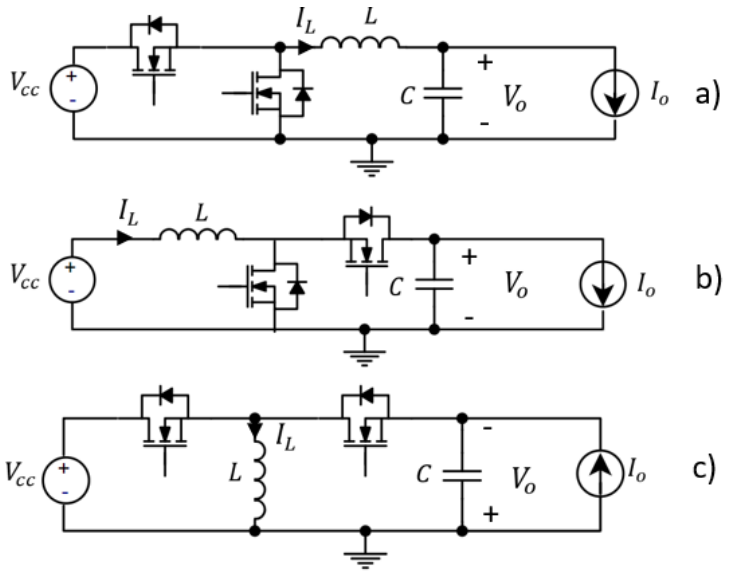


Figure 20: DC-DC buck (a), boost (b) and buck-boost (c) converter

$$L\frac{dI_L}{dt} = k_\omega(m_1 V_{cc} - V_o) \tag{3-1}$$

$$C\frac{dV_o}{dt} = k_\omega(I_L - m_2 I_o) \tag{3-2}$$

Table 1: Parameters of the unified predictive model

	Buck	Boost	Buck-Boost
k_ω	1	$1-u$	$1-u$
m_1	u	$\frac{1}{1-u}$	$\frac{u}{1-u}$
m_2	1	$\frac{1}{1-u}$	$\frac{1}{1-u}$
I_{Lnt}	I_{on}	$\frac{I_{on}}{V_{ccn}}$	$I_{on}\left(1+\frac{1}{V_{ccn}}\right)$
V_{rn}	1	1	1

For all three converters, the following base values are used to obtain normalized expressions (subscript n) in table I and the system of differential equations to obtain (3-3) and (3-4). V_r represents the desired output voltage setpoint.

$$V_{base} = V_r \qquad T_{base} = 2\pi\sqrt{LC}$$

$$Z_{base} = \sqrt{L/C} \qquad I_{base} = V_{base}/Z_{base}$$

$$\frac{1}{2\pi}\frac{dI_{Ln}}{dt_n} = k_\omega(m_1 V_{ccn} - V_{on}) \tag{3-3}$$

$$\frac{1}{2\pi}\frac{dV_{on}}{dt_n} = k_\omega(I_{Ln} - m_2 I_{on}) \tag{3-4}$$

A generalized predictive model can be expressed in (3-5) and (3-6) applying the Forward Euler discretization to (3-3) and (3-4). Note that T_{sn} represents the normalized sampling period of inductor current and capacitor voltage.

$$I_{Ln}(k+1) = I_{Ln}(k) + T_{sn} 2\pi k_\omega(m_1 V_{ccn} - V_{on}(k)) \tag{3-5}$$

$$V_{on}(k+1) = V_{on}(k) + T_{sn} 2\pi k_\omega(I_{Ln}(k) - m_2 I_{on}(k)) \tag{3-6}$$

Both the time optimal boundary control and the proposed control require the derivation of natural trajectories of converter states in the state plane analysis in both switching modes (MOSFET ON or OFF).

As illustrated in figure 21, a state plane analysis of each converter gives a visual representation of its behavior when u is maintained at 1(λ_{ON}) or maintained at 0 (λ_{OFF}) corresponding to the ON NSS or OFF NSS respectively of the converter.

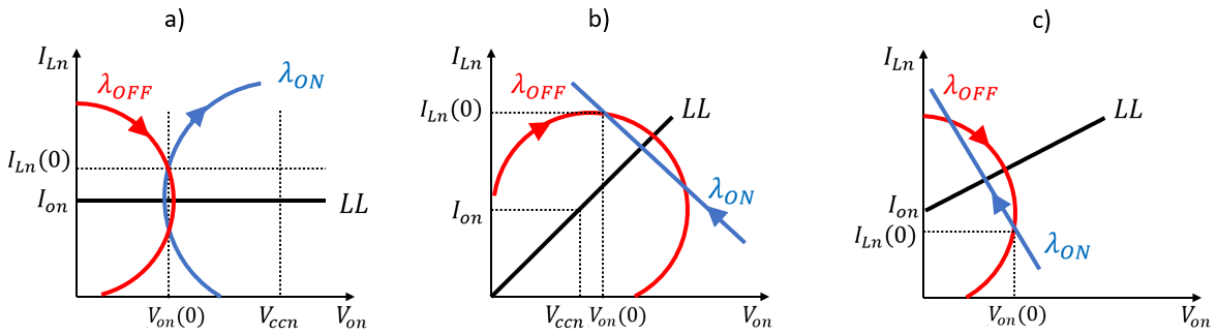


Figure 21: Load Line (Black), OFF (red) and ON (blue) Natural trajectory for buck (a), boost (b) and buck-boost (c)

(3-7) is the generalized analytic expression of ON(u=1) or OFF(u=0) NSS and uses variables from table I.

$$(V_{on} - m_1 V_{ccn})^2 + (I_{Ln} - m_2 I_{on})^2 = (V_{on}(0) - m_1 V_{ccn})^2 + (I_{Ln}(0) - m_2 I_{on})^2 \quad (3\text{-}7)$$

This equation can be illustrated in the state plane as a circle of center $(m_1 V_{ccn}, m_2 I_{on})$, the generalized DC operating point. The radius of this circle is the distance between the initial condition $(V_{on}(0), I_{Ln}(0))$ and the generalized DC operating point.

In the case m_1 and m_2 are infinite (boost and buck-boost converter when u=1), the state trajectory is expressed as the tangent of the unified NSS circle of (3-7) in (3-8).

$$\lambda_{ON} : I_{Ln} = -\frac{V_{ccn}}{I_{on}} V_{on} + I_{Ln}(0) + \frac{V_{ccn}}{I_{on}} V_{on}(0) \quad (3\text{-}8)$$

Load line presented in figure 21 represents the set of equilibrium points where both ON and OFF NSS share the same tangent. It can also be represented as a line passing through the center of any OFF NSS and the target point (V_{rn}, I_{Lnt})

$$LL: I_{Ln} = \frac{I_{on} m_{2_{u=0}} - I_{Lnt}}{V_{ccn} m_{1_{u=0}} - V_{rn}} (V_{on} - V_{rn}) + I_{Lnt}$$

3.3 Dynamic Performance indices for Voltage Regulation of Non-Isolated DC-DC Converters

The goal for this section is to provide the tools to analyze the performance of the generalized control scheme applied to each converter. This section reports the development of Dynamic performance indices for buck, boost and buck-boost using geometrical domain analysis in section 3.3.1, 3.3.2 respectively. The dynamic performance indices for boost converter are different from section 2.3 since the target voltage and initial capacitor voltage are not necessarily equal to 1

3.3.1 Buck Converter

As for boost converter in section 2.3, the benchmarking indices for buck converter are based on the converter performance limit for start-up, loading and unloading transient using the geometrical variables introduced in figure 22

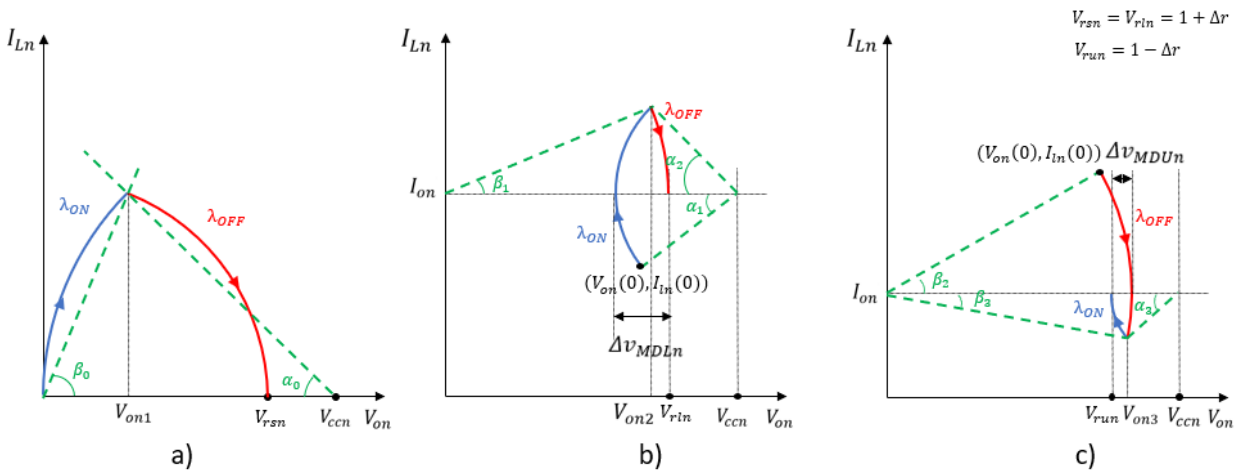


Figure 22:Buck Converter time optimal trajectories for start-up (a), loading (b) and unloading (c) transient.

3.3.1.1 Voltage Deviation Performance Indices

Figure 22a shows that the minimum overshoot expected for the buck converter is equal to zero. The target voltage V_r, being the difference between the initial voltage and the output voltage is chosen as reference for the voltage deviation index *SOi* in (3-9) related to start-up transient where Δv_{OS} is the measured voltage overshoot.

$$SOi = \frac{V_{rsn}V_r}{V_{rsn}V_r + 2\Delta v_{OS}} \tag{3-9}$$

Figure 22b and c illustrate that the minimum voltage deviation for loading and unloading transient, respectively, is reached at the load line. From this observation, the minimum voltage deviation for loading transient (3-10) and unloading transient (3-11) can be computed.

$$\Delta v_{MDLn} = V_{rln} - V_{ccn} + \sqrt{(V_{ccn} - V_{on}(0))^2 + (I_{on} - I_{Ln}(0))^2} \tag{3-10}$$

$$\Delta v_{MDUn} = -V_{run} + \sqrt{V_{on}(0)^2 + (I_{on} - I_{Ln}(0))^2} \tag{3-11}$$

In the same way as for boost converter in section 2.3, the minimum voltage deviation for loading (Δv_{MDLn}) and unloading transient (Δv_{MDUn}) is used as a reference for the expression of voltage deviation performance index (3-12), where $\Delta v_{pk-pk(L/U)}$ is the measured peak to peak excursion of voltage during loading and unloading transient respectively.

$$DR_{(L/U)} = \frac{\Delta v_{MD(L/U)}}{\Delta v_{pk-pk(L/U)}} \tag{3-12}$$

3.3.1.2 Recovery Time Performance Indices

To determine the minimum recovery time for start-up transient in (3-16) it is required to compute V_{on1} using (3-13) before calculating α_0 and β_0 represented in figure 22a using (3-14) and (3-15) respectively.

$$V_{on1} = \frac{{V_{rsn}}^2}{2V_{ccn}} \tag{3-13}$$

$$\alpha_0 = cos^{-1}(1 - \frac{{V_{rsn}}^2}{2{V_{ccn}}^2}) \tag{3-14}$$

$$\beta_0 = cos^{-1}\left(\frac{V_{rsn}}{2V_{ccn}}\right) \tag{3-15}$$

$$t_{MS_n} = \frac{\alpha_0 + \beta_0}{2\pi} \tag{3-16}$$

This minimum is used as a reference for the measured settling time t_{start} in the recovery time index of the start-up transient in (3-17).

$$ST_i = 1 - 0.5log\left(\frac{t_{start}}{t_{MS}}\right) \tag{3-17}$$

Likewise, the minimum recovery time for loading transient in (3-22) requires computing V_{on2} with (3-18) before computing α_1, α_2 and β_1 illustrated in figure 22b using (3-19), (3-20) and (3-21) respectively.

$$V_{on2} = \frac{-(V_{on}(0) - V_{ccn})^2 - (I_{Ln}(0) - I_{on})^2 + {V_{rln}}^2 + {V_{ccn}}^2}{2V_{ccn}} \tag{3-18}$$

$$\alpha_1 = cos^{-1}(\frac{V_{ccn} - V_{on}(0)}{\sqrt{(V_{on}(0) - V_{ccn})^2 + (I_{Ln}(0) - I_{on})^2}}) \tag{3-19}$$

$$\alpha_2 = cos^{-1}(\frac{V_{ccn} - V_{on2}}{\sqrt{(V_{on}(0) - V_{ccn})^2 + (I_{Ln}(0) - I_{on})^2}}) \tag{3-20}$$

$$\beta_1 = cos^{-1}(\frac{V_{on2}}{V_{rln}}) \tag{3-21}$$

$$t_{MRL_n} = \frac{\alpha_1 + \alpha_2 + \beta_1}{2\pi} \tag{3-22}$$

V_{on3}, given in (3-23), along with α_3, β_2 and β_3 represented in figure 22c and given in (3-24), (3-25) and (3-26) respectively are essential to determine the minimum time for unloading transient in (3-27).

$$V_{on3} = \frac{V_{on}(0)^2 + (I_{Ln}(0) - I_{on})^2 - (V_{run} - V_{ccn})^2 + {V_{ccn}}^2}{2V_{ccn}} \tag{3-23}$$

$$\alpha_3 = cos^{-1}(\frac{V_{ccn} - V_{on3}}{V_{ccn} - V_{run}}) \tag{3-24}$$

$$\beta_2 = cos^{-1}(\frac{V_{on}(0)}{\sqrt{V_{on}(0)^2 + (I_{Ln}(0) - I_{on})^2}}) \tag{3-25}$$

$$\beta_3 = cos^{-1}(\frac{V_{on3}}{\sqrt{V_{on}(0)^2 + (I_{Ln}(0) - I_{on})^2}}) \tag{3-26}$$

$$t_{MRU_n} = \frac{\alpha_3 + \beta_2 + \beta_3}{2\pi} \tag{3-27}$$

Using (3-22) and (3-27) as reference it is possible to objectively analyze the measured loading t_{recL} and unloading recovery time t_{recU} using (3-28).

$$RTi_{(L/U)} = 1 - 0.5\log\left(\frac{t_{rec(L/U)}}{t_{MR(L/U)}}\right) \tag{3-28}$$

3.3.2 Boost Converter

The benchmarking indices for boost converter are based on the converter performance limit for start-up, loading and unloading transient using the geometrical variables introduced in figure 23.

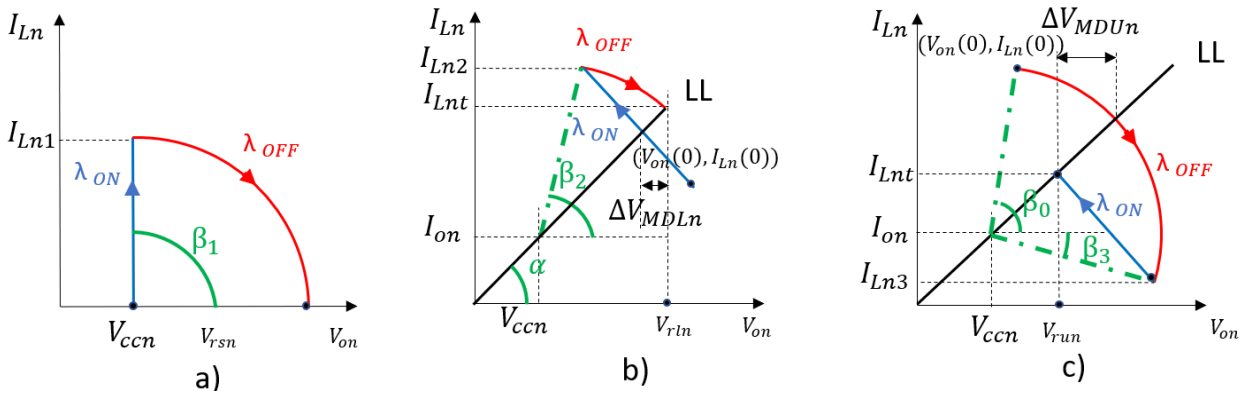


Figure 23: Boost Converter time optimal trajectories for start-up (a), loading (b) and unloading (c) transient.

3.3.2.1 Voltage Deviation Performance Indices

Figure 23a shows that the minimum overshoot expected for the buck-boost converter is equal to zero. The difference between the desired output voltage and the initial output voltage, $V_{rsn}V_r - V_{cc}$, is used as a reference in the voltage deviation index related to start-up transient *SOi* in (3-9), where Δv_{OS} is the measured voltage overshoot.

Figure 23b and c illustrate that the minimum voltage deviation for loading and unloading transient, respectively, is reached at the load line. From this observation, the minimum voltage deviation for loading transient (3-29) and unloading transient (3-30) can be computed.

$$\Delta v_{MDLn} = V_{rln} - \left(\frac{\frac{V_{ccn}}{I_{on}} V_{on}(0) + I_{Ln}(0) - I_{on}}{\frac{I_{on}}{V_{ccn}} + \frac{V_{ccn}}{I_{on}}} \right) \tag{3-29}$$

$$\Delta v_{MDUn} = V_{ccn} + \sqrt{\frac{(V_{on}(0) - V_{ccn})^2 + (I_{Ln}(0) - I_{on})^2}{1 + \left(\frac{I_{on}}{V_{ccn}}\right)^2}} - V_{run} \tag{3-30}$$

In the same way as for boost converter in section 2.3, the minimum voltage deviation for loading (Δv_{MDLn}) and unloading transient (Δv_{MDUn}) is used as a reference for the expression of voltage deviation performance index (3-12), where $\Delta v_{pk-pk(L/U)}$ is the measured peak to peak excursion of voltage during loading and unloading transient respectively.

3.3.2.2 Recovery Time Performance Indices

The minimum recovery time in (3-31) is used as a reference for the measured settling time t_{start} in the recovery time index of the start-up transient in (3-17).

$$t_{MS_n} = \frac{I_{Ln1}}{2\pi V_{ccn}} + \frac{\pi/2}{2\pi} = \frac{V_{rsn} - V_{ccn}}{2\pi V_{ccn}} + \frac{1}{4} \tag{3-31}$$

Likewise, the minimum recovery time for loading transient requires computing I_{Ln2}. This value is obtained by finding the intersection between the OFF and ON surface on figure 23b. The expression of I_{Ln2} in (3-35) is obtained by solving the quadratic function $l_1 {I_{Ln2}}^2 + l_2 I_{Ln2} + l_3 = 0$, where l_1, l_2 and l_3 are described in (3-32), (3-33) and (3-34) respectively.

$$l_1 = \left(1 + \left(\frac{I_{on}}{V_{ccn}}\right)^2\right) \tag{3-32}$$

$$l_2 = -2\left(I_{on} + I_{Ln}(0)\left(\frac{I_{on}}{V_{ccn}}\right)^2 + (V_{on}(0) - V_{ccn})\frac{I_{on}}{V_{ccn}}\right) \tag{3-33}$$

$$\begin{aligned} l_3 = {I_{on}}^2 + \left(\frac{I_{on}}{V_{ccn}}\right)^2 I_{Ln}(0)^2 + 2(V_{on}(0) - V_{ccn})\frac{I_{on}}{V_{ccn}} I_{Ln}(0) + (V_{on}(0) - V_{ccn})^2 \\ - (I_{Lnt} - I_{on})^2 - (V_{rln} - V_{ccn})^2 \end{aligned} \tag{3-34}$$

$$I_{Ln2} = \frac{-l_2 + \sqrt{{l_2}^2 - 4l_1 l_3}}{2l_1} \tag{3-35}$$

The minimum recovery time for loading transient in (3-38) requires computing α and β_2 in (3-36) and (3-37) respectively

$$\alpha = sin^{-1}\left(\frac{\frac{I_{on}}{V_{ccn}}V_{rln}}{\sqrt{\left(\frac{I_{on}}{V_{ccn}}V_{rln}\right)^2 + {V_{rln}}^2}}\right) \tag{3-36}$$

$$\beta_2 = sin^{-1}\left(\frac{I_{Ln2} - I_{on}}{\sqrt{\left(\frac{I_{on}}{V_{ccn}}V_{rln} - I_{on}\right)^2 + (V_{rln} - V_{ccn})^2}}\right) \tag{3-37}$$

$$t_{MRL_n} = \frac{\beta_2 - \alpha}{2\pi} + \frac{I_{Ln2} - I_{Ln}(0)}{2\pi V_{ccn}} \tag{3-38}$$

The minimum recovery time for unloading transient requires computing I_{Ln3}. This value is obtained by finding the intersection between the OFF and ON surface on figure 23c. The expression of I_{Ln3} in (3-42) is obtained by solving the quadratic function ${u_1 I_{Ln2}}^2 + u_2 I_{Ln2} + u_3 = 0$, where u_1, u_2 and u_3 are described in (3-39), (3-40) and (3-41) respectively.

$$u_1 = \left(1 + \left(\frac{I_{on}}{V_{ccn}}\right)^2\right) \tag{3-39}$$

$$u_2 = -2\left(I_{on} + I_{Lnt}\left(\frac{I_{on}}{V_{ccn}}\right)^2 + (V_{run} - V_{ccn})\frac{I_{on}}{V_{ccn}}\right) \tag{3-40}$$

$$u_3 = {I_{on}}^2 + \left(\frac{I_{on}}{V_{ccn}}\right)^2 {I_{Lnt}}^2 + 2(V_{run} - V_{ccn})\frac{I_{on}}{V_{ccn}} I_{Lnt} + (V_{run} - V_{ccn})^2 - (I_{Ln}(0) - I_{on})^2 - (V_{on}(0) - V_{ccn})^2 \quad (3\text{-}41)$$

$$I_{Ln3} = \frac{-u_2 - \sqrt{{u_2}^2 - 4u_1u_3}}{2u_1} \quad (3\text{-}42)$$

β_0 and β_3 illustrated in figure 23c and given in (3-43) and (3-44) respectively, are essential to determine the minimum time for unloading transient in (3-45).

$$\beta_0 = sin^{-1}\left(\frac{I_{Ln}(0) - I_{on}}{\sqrt{(I_{Ln}(0) - I_{on})^2 + (V_{on}(0) - V_{ccn})^2}}\right) \quad (3\text{-}43)$$

$$\beta_3 = sin^{-1}\left(\frac{I_{on} - I_{Ln3}}{\sqrt{(I_{Ln}(0) - I_{on})^2 + (V_{on}(0) - V_{ccn})^2}}\right) \quad (3\text{-}44)$$

$$t_{MRU_n} = \frac{\beta_0 + \beta_3}{2\pi} + \frac{I_{Lnt} - I_{Ln3}}{2\pi V_{ccn}} \quad (3\text{-}45)$$

Using (3-38) and (3-45) as reference it is possible to objectively analyze the measured loading t_{recL} and unloading recovery time t_{recU} using (3-28).

3.3.3 Buck-boost Converter

The benchmarking indices for buck-boost converter are based on the converter performance limit for start-up, loading and unloading transient using the geometrical variables introduced in figure 24. The calculations are like the boost converter case.

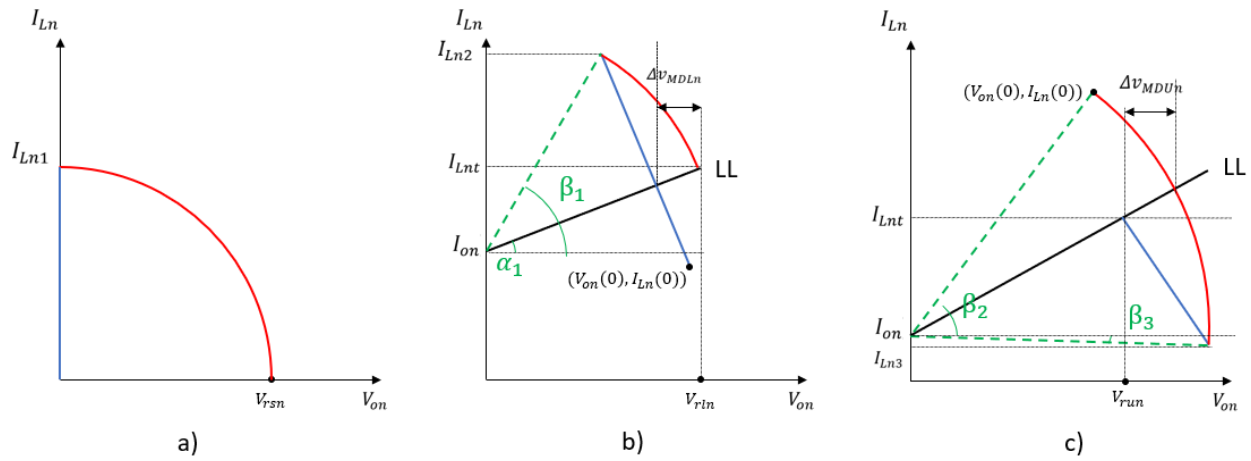


Figure 24: Buck-Boost Converter time optimal trajectories for start-up (a), loading (b) and unloading (c) transient.

3.3.3.1 Voltage Deviation Performance Indices

Figure 24a shows that the minimum overshoot expected for the buck-boost converter is equal to zero. The target voltage V_r, being the difference between the initial voltage and the output voltage is chosen as reference for the voltage deviation index *SOi* in (3-9) related to start-up transient where Δv_{OS} is the measured voltage overshoot.

Figure 24b and c illustrate that the minimum voltage deviation for loading and unloading transient, respectively, is reached at the load line. From this observation, the minimum voltage deviation for loading transient (3-46) and unloading transient (3-47) can be computed.

$$\Delta v_{MDLn} = V_{rln} - \left(\frac{\frac{V_{ccn}}{I_{on}} V_{on}(0) + I_{Ln}(0) - I_{on}}{\frac{I_{on}}{V_{ccn}} + \frac{V_{ccn}}{I_{on}}} \right) \tag{3-46}$$

$$\Delta v_{MDUn} = \sqrt{\frac{V_{on}(0)^2 + (I_{Ln}(0) - I_{on})^2}{1 + \left(\frac{I_{on}}{V_{ccn}}\right)^2}} - V_{run} \tag{3-47}$$

In the same way as for boost converter in section 2.3, the minimum voltage deviation for loading (Δv_{MDLn}) and unloading transient (Δv_{MDUn}) is used as a reference for the expression of voltage deviation performance index (3-12), where $\Delta v_{pk-pk(L/U)}$ is the measured peak to peak excursion of voltage during loading and unloading transient respectively.

3.3.3.2 Recovery Time Performance Indices

The minimum recovery time in (3-48) is used as a reference for the measured settling time t_{start} in the recovery time index of the start-up transient in (3-17).

$$t_{MS_n} = \frac{I_{Ln1}}{2\pi V_{ccn}} + \frac{\pi/2}{2\pi} = \frac{V_{rsn}}{2\pi V_{ccn}} + \frac{1}{4} \tag{3-48}$$

Likewise, the minimum recovery time for loading transient requires computing I_{Ln2}. This value is obtained by finding the intersection between the OFF and ON surface on figure 24b. The expression of I_{Ln2} in (3-52) is obtained by solving the quadratic function $l_1 {I_{Ln2}}^2 + l_2 I_{Ln2} + l_3 = 0$, where l_1, l_2 and l_3 are described in (3-49), (3-50) and (3-51) respectively.

$$l_1 = \left(1 + \left(\frac{I_{on}}{V_{ccn}}\right)^2\right) \tag{3-49}$$

$$l_2 = -2\left(I_{on} + I_{Ln}(0)\left(\frac{I_{on}}{V_{ccn}}\right)^2 + V_{on}(0)\frac{I_{on}}{V_{ccn}}\right) \tag{3-50}$$

$$l_3 = {I_{on}}^2 + \left(\frac{I_{on}}{V_{ccn}}\right)^2 I_{Ln}(0)^2 + 2V_{on}(0)\frac{I_{on}}{V_{ccn}} I_{Ln}(0) + V_{on}(0)^2 - (I_{Lnt} - I_{on})^2 - {V_{rln}}^2 \tag{3-51}$$

$$I_{Ln2} = \frac{-l_2 + \sqrt{{l_2}^2 - 4l_1 l_3}}{2l_1} \tag{3-52}$$

The minimum recovery time for loading transient in (3-55) requires computing α_1 and β_1 in (3-53) and (3-54) respectively

$$\alpha_1 = sin^{-1}\left(\frac{\frac{I_{on}}{V_{ccn}}V_{rln}}{\sqrt{\left(\frac{I_{on}}{V_{ccn}}V_{rln}\right)^2 + {V_{rln}}^2}}\right) \tag{3-53}$$

$$\beta_1 = sin^{-1}\left(\frac{I_{Ln2} - I_{on}}{\sqrt{\left(\frac{I_{on}}{V_{ccn}}V_{rln}\right)^2 + {V_{rln}}^2}}\right) \tag{3-54}$$

$$t_{MRL_n} = \frac{\beta_1 - \alpha_1}{2\pi} + \frac{I_{Ln2} - I_{Ln}(0)}{2\pi V_{ccn}}) \tag{3-55}$$

The minimum recovery time for unloading transient requires computing I_{Ln3}. This value is obtained by finding the intersection between the OFF and ON surface on figure 24c. The expression of I_{Ln3} in (3-59) is obtained by solving the quadratic function ${u_1 I_{Ln2}}^2 + u_2 I_{Ln2} + u_3 = 0$, where u_1, u_2 and u_3 are described in (3-56), (3-57) and (3-58) respectively.

$$u_1 = \left(1 + \left(\frac{I_{on}}{V_{ccn}}\right)^2\right) \tag{3-56}$$

$$u_2 = -2\left(I_{on} + I_{Lnt}\left(\frac{I_{on}}{V_{ccn}}\right)^2 + V_{run}\frac{I_{on}}{V_{ccn}}\right) \tag{3-57}$$

$$u_3 = {I_{on}}^2 + \left(\frac{I_{on}}{V_{ccn}}\right)^2 {I_{Lnt}}^2 + 2V_{run}\frac{I_{on}}{V_{ccn}}I_{Lnt} + {V_{run}}^2 - (I_{Ln}(0) - I_{on})^2 - V_{on}(0)^2 \tag{3-58}$$

$$I_{Ln3} = \frac{-u_2 - \sqrt{{u_2}^2 - 4u_1 u_3}}{2u_1} \tag{3-59}$$

β_2 and β_3 illustrated in figure 24c and given in (3-60) and (3-61) respectively, are essential to determine the minimum time for unloading transient in (3-62).

$$\beta_2 = sin^{-1}\left(\frac{I_{Ln}(0) - I_{on}}{\sqrt{(I_{Ln}(0) - I_{on})^2 + V_{on}(0)^2}}\right) \tag{3-60}$$

$$\beta_3 = sin^{-1}\left(\frac{I_{on} - I_{Ln3}}{\sqrt{(I_{Ln}(0) - I_{on})^2 + V_{on}(0)^2}}\right) \tag{3-61}$$

$$t_{MRU_n} = \frac{\beta_2+\beta_3}{2\pi} + \frac{I_{Lnt} - I_{Ln3}}{2\pi V_{ccn}} \tag{3-62}$$

Using (3-55) and (3-62) as reference it is possible to objectively analyze the measured loading t_{recL} and unloading recovery time t_{recU} using (3-28).

3.4 Generalized Formulation of Time Optimal Boundary Control using NSS

In this section, the time optimal boundary control laws and design procedure for DC-DC buck, boost and buck-boost converter of Ordonez et al. are reviewed using the generalized model developed previously. This control ensures a minimum time control (MTC) for three types of transients presented in objective 1: start-up transient, loading transient and unloading transient. The goal is to regulate the output voltage to its setpoint with output current disturbances.

3.4.1 Generalized Control Laws

For DC-DC buck, boost and buck-boost, time optimal boundary control is ensured using the unified control laws below, using variables from table I.

Case I: $\boldsymbol{I_{Ln} > I_{Lnt}}$

If $\sigma_{u=0} > 0$, then $u = 0$, else $u = 1$

Case II: $\boldsymbol{I_{Ln} < I_{Lnt}}$

If $\sigma_{u=1} > 0$, then $u = 1$

Where,

$$\sigma_{u=0} = (V_{on} - m_{1_{u=0}} V_{ccn})^2 + (I_{Ln} - m_{2_{u=0}} I_{on})^2 - \left(V_{rn} - m_{1_{u=0}} V_{ccn}\right)^2 - (I_{Lnt} - m_{2_{u=0}} I_{on})^2 \quad (3\text{-}63)$$

and if $m_{1_{u=1}}$ and/or $m_{2_{u=1}}$ is infinite

$$\sigma_{u=1} = I_{Ln} + \frac{V_{ccn}}{I_{on}} V_{on} - I_{Lnt} - \frac{V_{ccn}}{I_{on}} V_{rn} \quad (3\text{-}64)$$

Else,

$$\sigma_{u=1} = (V_{on} - m_{1_{u=1}} V_{ccn})^2 + (I_{Ln} - m_{2_{u=1}} I_{on})^2 - \left(V_{rn} - m_{1_{u=1}} V_{ccn}\right)^2 - (I_{Lnt} - m_{2_{u=1}} I_{on})^2 \quad (3\text{-}65)$$

The control law in case I identifies if the converter states are inside the OFF Natural Trajectory circle containing the target point. If yes, then the MOSFET is kept ON until reaching the target OFF Natural Trajectory. In case II, the MOSFET is OFF if inside the ON Trajectory containing the target point. The MOSFET is ON once the target ON NSS is reached. In the case, m_1 and m_2 are both infinite, the target ON Natural Trajectory is a line. The MOSFET is kept ON

if the states are below the target ON Natural Trajectory and kept OFF otherwise. When the control laws above are applied, the expected state plane trajectory during a loading transient is illustrated by figure 25.

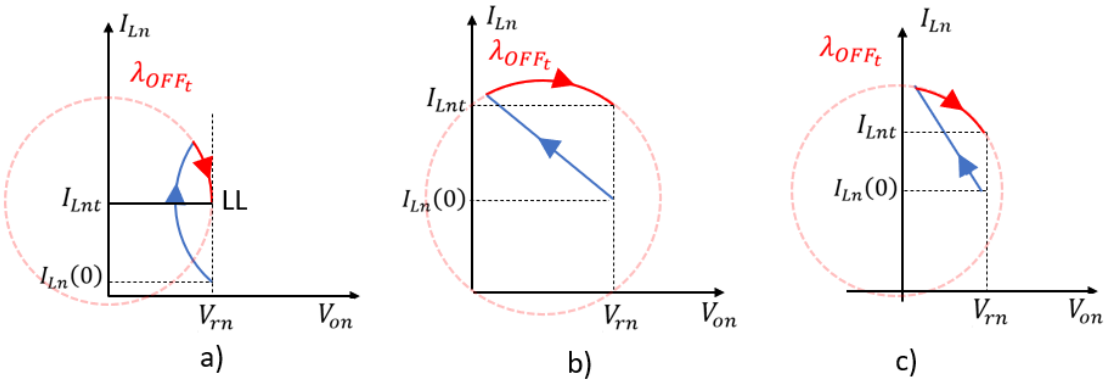


Figure 25: Time Optimal Trajectory during Load transient for buck, boost, and buck-boost converter

Ideally, in the situation of figure 25, the converter is switched ON until reaching the OFF Natural Trajectory containing the target point. Each trajectory is a time optimal regulation trajectory since it is composed of one OFF Natural Trajectory and one ON Natural Trajectory. In other words, the reference point in the state plane is reached in one switching action.

3.4.2 Steady-State Characteristics with linear ON Natural Trajectory

In literature, steady-state characteristics from the time optimal control are analyzed for the boost [14] and buck-boost [20] converter. The two converters have a linear ON NSS leading to a similar analysis. To have a better control over the current and voltage ripple as well as the switching frequency, the control law in case I is slightly incremented by a factor Δr^2.The adjusted control laws are defined below.

Case I: $\boldsymbol{I_{Ln} > I_{Lnt}}$

If $\sigma_{u=0} - \Delta r^2 > 0$, then $u = 0$, else $u = 1$

Case II: $\boldsymbol{I_{Ln} < I_{Lnt}}$

If $\sigma_{u=1} > 0$, then $u = 1$

The equation (3-66), derived in [14] and [20], represents the correlation between the increment Δr^2 and the steady-state output voltage ripple ΔV_{on} for boost and buck-boost converter.

$$\Delta r^2 = \frac{(\Delta V_{on})^2}{4}\left(1 + \left(\frac{V_{ccn}}{I_{on}}\right)^2\right) \tag{3-66}$$

From [14] and [20], a general formulation of the normalized ON time and OFF time is provided in (3-67), when *u=0* and *u=1* respectively, and in the case where one of the NSS is a line (boost or buck-boost).

$$(t_{OFF/ON})_n = \frac{\Delta V_{on}}{2\pi k_\omega (I_{Lnt} - m_2 I_{on})} \tag{3-67}$$

The switching frequency is computed in (3-68) using ON and OFF time provided by (3-67)

$$f_{sw} = \frac{1}{T_{base}(t_{ON_n} + t_{OFF_n})} \tag{3-68}$$

3.4.3 Steady-State Characteristics with circular ON Natural Trajectory

Literature does not provide steady state characteristics using the factor Δr^2 like in [14] and [20]. For the buck converter both NSS are circular making (3-66) and (3-67) not suitable to determine the switching frequency. However, a similar analysis is possible in the case of the buck converter using the adjusted control laws below.

Case I: $\boldsymbol{I_{Ln} > I_{Lnt}}$

If $\sigma'_{u=0} > 0$, then $u = 0$, else $u = 1$

Case II: $\boldsymbol{I_{Ln} < I_{Lnt}}$

If $\sigma'_{u=1} > 0$, then $u = 1$

Where,

$$\sigma'_{u=0} = (V_{on} - m_{1_{u=0}} V_{ccn})^2 + (I_{Ln} - m_{2_{u=0}} I_{on})^2 - \left(\sqrt{\left(V_{rn} - m_{1_{u=0}} V_{ccn}\right)^2 + \left(I_{Lnt} - m_{2_{u=0}} I_{on}\right)^2} + \Delta r\right)^2 \quad (3\text{-}69)$$

And

$$\sigma'_{u=1} = (V_{on} - m_{1_{u=1}} V_{ccn})^2 + (I_{Ln} - m_{2_{u=1}} I_{on})^2 - \left(\sqrt{\left(V_{rn} - m_{1_{u=1}} V_{ccn}\right)^2 + \left(I_{Lnt} - m_{2_{u=1}} I_{on}\right)^2} + \Delta r\right)^2 \quad (3\text{-}70)$$

(3-71) is obtained subtracting the inductor current solutions of the system of equation below after replacing m_1, m_2 and k_ω by the values related to the buck converter in table I.

$$\begin{cases} \sigma'_{u=0} = 0 \\ \sigma'_{u=1} = 0 \end{cases}$$

$$\Delta r = \frac{-V_{ccn} + V_{ccn}\sqrt{1 + \frac{\Delta {I_{Ln}}^2}{4(V_{ccn} - 1)}}}{2} \quad (3\text{-}71)$$

(3-72) should be used to estimate ON and OFF time instead of using (3-67) before calculating the switching frequency using (3-68).

$$(t_{OFF/ON})_n = \frac{\Delta I_{Ln}}{2\pi k_\omega (m_1 V_{ccn} - V_{rn})} \quad (3\text{-}72)$$

3.5 Proposed Generalized Finite Control Set Model Predictive Control

This section presents the proposed generalized FCS-MPC using unified predictive model and natural trajectories presented in section 3.2. Section 3.5.1 and 3.5.2 define the cost function for linear and circular ON Natural Trajectory, respectively, ensuring time optimal regulation for loading, unloading and start-up transient. Section 3.5.3 and 3.5.4 detail the inductor current and output voltage constraints of the proposed FCS-MPC, respectively. Section 3.5.5 summarizes the different steps of the proposed FCS-MPC.

3.5.1 Cost Function for time optimal regulation with linear ON Natural Trajectory

In section 3.4, two cases are distinguished, where each case has a specific control law, to obtain time optimal trajectories. Each case can be formulated as tracking a specific natural trajectory. For case I, this is the OFF Natural trajectory with a radius slightly higher (Δr^2) than the OFF natural trajectory including the target point. To be valid as a cost function, the OFF natural trajectory tracking term should decrease as it gets closer to the target OFF natural trajectory. (3-73) is the subtraction of the radius squared of the OFF trajectory including the predicted states ((3-5) and (3-6)) and the radius squared of the target OFF trajectory.

$$J_{OFF} = \Big|(V_{on}(k+1) - m_{1_{u=0}}V_{ccn})^2 + (I_{Ln}(k+1) - m_{2_{u=0}}I_{on})^2 - \left(V_{rn} - m_{1_{u=0}}V_{ccn}\right)^2 - \left(I_{Lnt} - m_{2_{u=0}}I_{on}\right)^2 - \Delta r^2\Big| \tag{3-73}$$

Therefore, it illustrates how close the predicted state of the converter is from the target OFF natural trajectory and should decrease as it gets closer to it.

For case II, this is the ON Natural trajectory containing the target point. (3-74) is the absolute value of the difference between the x-intercept of the ON trajectory including the predicted state and the x-intercept of the target ON natural trajectory.

$$J_{ON} = \left| \frac{I_{on}}{V_{ccn}} (I_{Ln}(k+1) - I_{Lnt}) + V_{on}(k+1) - V_{rn} \right| \tag{3-74}$$

The distinction between case I and II in the proposed FCS-MPC is based on the position with respect to load line.

The penalty factor λ is introduced to combine J_{OFF} and J_{ON} into one general cost function in (3-75). λ is set to 0 if under the load line (case I) and to 1 otherwise (case II).

$$J = \lambda J_{OFF} + (1-\lambda) J_{ON} \tag{3-75}$$

3.5.2 Cost Function for time optimal regulation with circular ON Natural Trajectory

In section 3.4.3, control law of case I and case II include an increment Δr in the radius of target ON and OFF Natural Trajectory. With the same philosophy as section 3.5.1, the target OFF and ON Natural Trajectory tracked by the cost function term of (3-76) and (3-77), respectively, include this increment Δr

$$J_{OFF} = \left| (V_{on}(k+1) - m_{1_{u=0}} V_{ccn})^2 + (I_{Ln}(k+1) - m_{2_{u=0}} I_{on})^2 - \left(\sqrt{\left(V_{rn} - m_{1_{u=0}} V_{ccn}\right)^2 + \left(I_{Lnt} - m_{2_{u=0}} I_{on}\right)^2} + \Delta r \right)^2 \right| \tag{3-76}$$

$$J_{ON} = \left| (V_{on}(k+1) - m_{1_{u=1}} V_{ccn})^2 + (I_{Ln}(k+1) - m_{2_{u=1}} I_{on})^2 - \left(\sqrt{\left(V_{rn} - m_{1_{u=1}} V_{ccn}\right)^2 + \left(I_{Lnt} - m_{2_{u=1}} I_{on}\right)^2} + \Delta r \right)^2 \right| \quad (3\text{-}77)$$

Therefore, (3-76) is used in place of (3-73) and (3-77) in place of (3-74) in the generalized cost function (3-75).

3.5.3 Current Constraint

If the role of the cost function of (3.75) is to ensure a time optimal regulation, it can be at the price of important current spikes during large load transients. The implementation of inductor current constraint in (3.78) allows to intuitively set a maximum for this converter state and avoid current spikes.

$$I_{Ln}(k+1) < I_{Lnmax} \quad (3\text{-}78)$$

If the condition in (3-78) is not true for the predicted state $I_{Ln}(k+1)$, the cost function associated to the switching decision of the predicted states is set to infinity.

3.5.4 Voltage Constraint

Time optimal regulation induced by the cost function in (3-75) implies also important voltage deviation, degrading the overall dynamic performance [22]. The capacitor voltage constraint in (3-79) is implemented to prevent important voltage deviations.

$$|1 - V_{on}(k+1)| < \Delta V \quad (3\text{-}79)$$

As in (3-78), if (3-79) is not true for the predicted state $V_{on}(k+1)$, the cost function associated to the switching decision of the predicted states is set to infinity. ΔV is the maximum deviation for the predicted states and needs to be adjusted to allow for a minimum deviation required for voltage regulation. During a loading or unloading transient, the minimum deviation is reached once the load line has been reached [16], [21]. Since for the buck converter the maximum voltage deviation is reached when crossing the load line, it is not necessary to apply a voltage deviation constraint for this converter.

3.5.5 Steps of the Proposed FCS-MPC

The generalized FCS MPC is illustrated in figure 26 where the constraint to be respected can be either the voltage deviation or the maximum inductor current. Offline actions are required in the initialization phase to obtain the base values as well as the parameters of table I corresponding to the controlled DC-DC converter (Section II). Each sampling of I_o, I_L and V_c is normalized using the base values computed in the initialization phase. The first step of the proposed control is to compute the two sets of predicted states ($V_{on}(k+1)|_{u=0}$, $I_{Ln}(k+1)|_{u=0}$) and ($V_{on}(k+1)|_{u=1}$, $I_{Ln}(k+1)|_{u=1}$) representing the expected converter states if the MOSFET is kept OFF and if the MOSFET is kept ON, respectively. In this first step, the calculation of the radius increment Δr^2 or Δr and the voltage deviation constraint ΔV, if the constraint is chosen to be on capacitor voltage, are included.

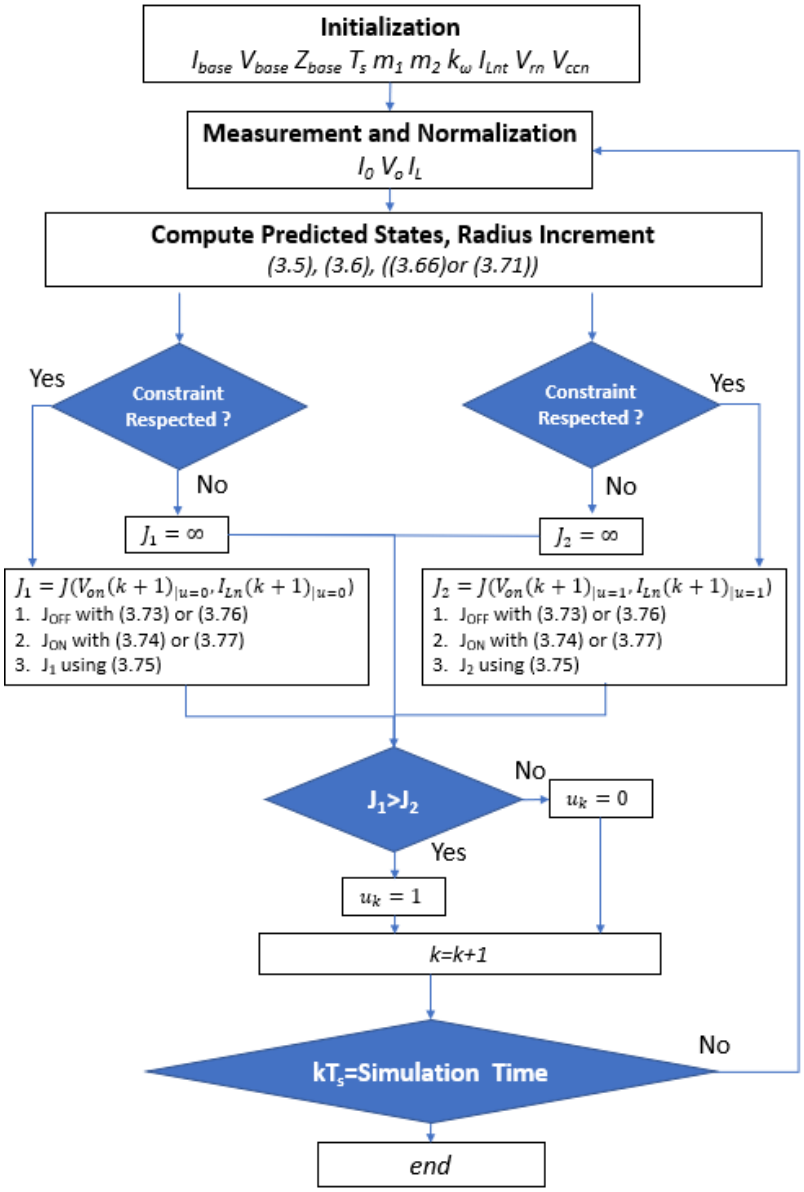


Figure 26: Flowchart of the proposed FCS-MPC

The second step consists in working in parallel with the two sets of predicted states presented earlier. For each switching decision, the algorithm verifies if the constraint on voltage or current is respected If the predicted states do not respect the constraint, the associated cost function is set to infinity. If the constraint is respected, the cost function is calculated according to section 3.5.1 or 3.5.2. Finally, the switching decision leading to the minimum cost function is

chosen for the upcoming sampling period T_s. Once this decision is taken the system repeats this sequence of action from the measurement and Normalization phase until end of simulation.

3.6 Simulation Results

3.6.1 DC-DC Buck Converter

This section compares dynamic performances of Time Optimal Boundary control laws of [18]-[19] and the proposed FCS-MPC of figure 26 with parameters adjusted for buck converter. Both control schemes are implemented to regulate the output voltage of the DC-DC buck converter in figure 20 in Simulink with L=1.07mH, C = 267µF, V_{cc} = 10V, V_r = 5V, Ts = 1.25µs and a desired switching frequency f_{sw}=1 kHz. Figure 27 illustrates the evolution of converter states in time domain during a start-up transient ($I_o = 0\ A$), loading transient (I_o increasing to 2 A) and unloading transient ($I_o$decreasing to 1 A) when the time optimal boundary control of [18]-[19] is applied. Figure 28 shows the evolution of the converter states under the same conditions when the proposed FCS-MPC is applied without current constraints.

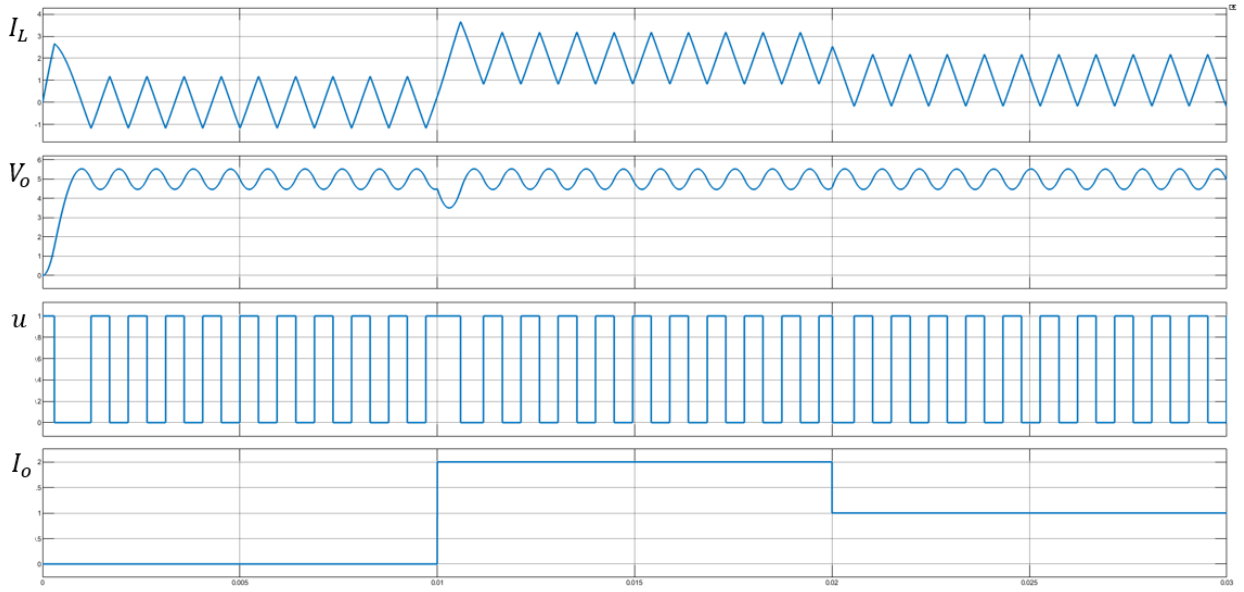


Figure 27: Evolution of Buck converter States and control actions when Time Optimal Boundary Control of [18]-[19] is applied

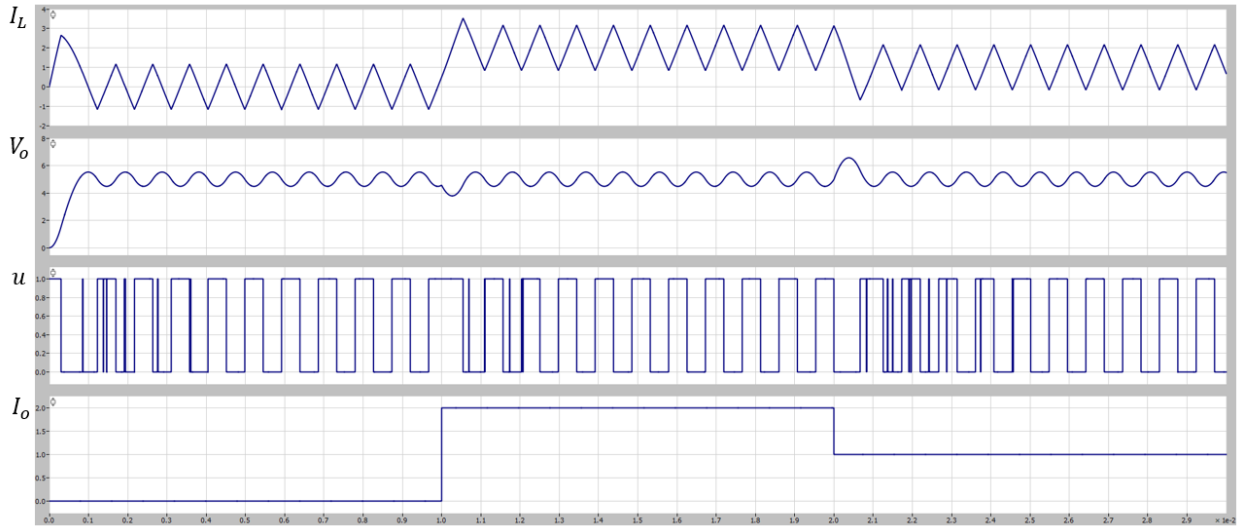


Figure 28: Evolution of Buck converter States and control actions when proposed FCS-MPC without Voltage Constraint is applied

As illustrated by figure 30a, the proposed FCS-MPC with no constraint on current and the time optimal boundary control shares the same dynamic performances.

The next set of experiment aims at analyzing the impact of the current constraint on the proposed FCS-MPC performance where the maximum current allowed is 3.2 A. Figure 29 shows that the inductor current is limited during the loading transient

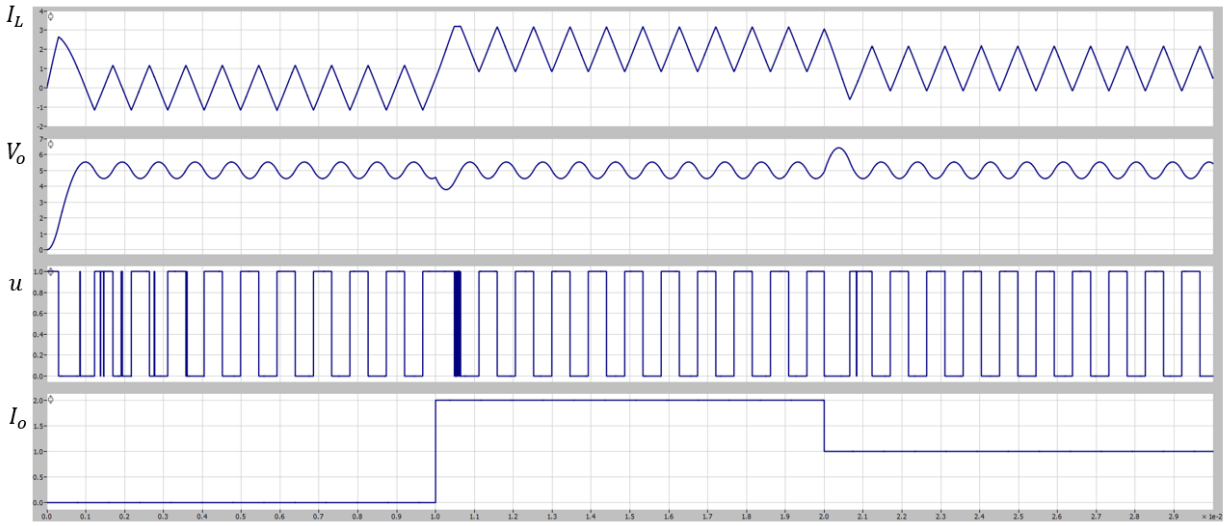


Figure 29: Evolution of Buck converter States and control actions when proposed FCS-MPC with current Constraint is applied

The dynamic performance indices from figure 30 shows that the current constraint has no significant impact on the voltage regulation in this case

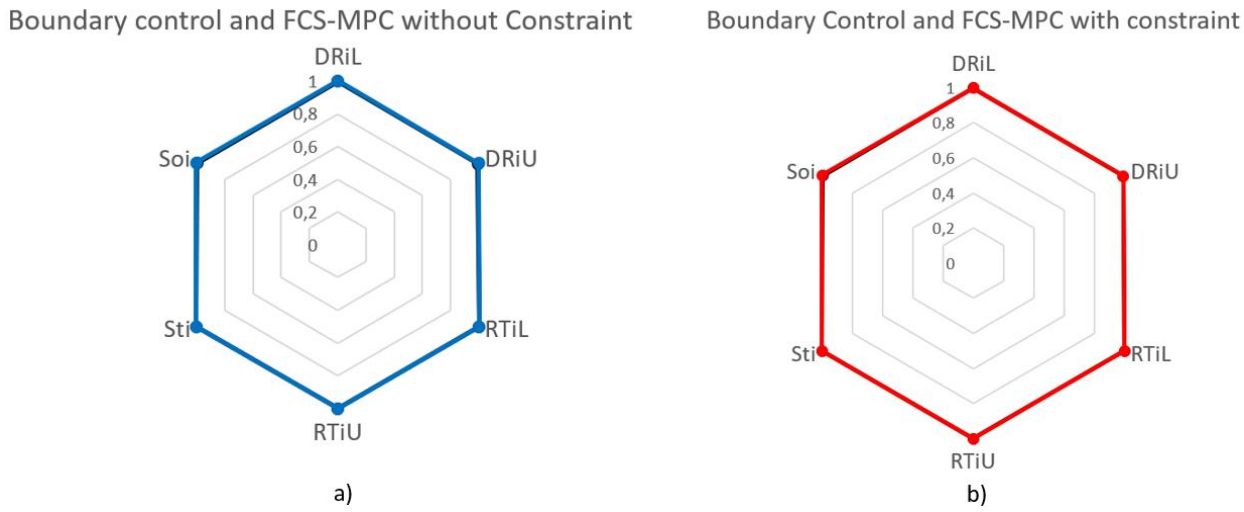


Figure 30: Benchmarking indices of (a) Time Optimal Boundary control laws (black) compared with proposed FCS-MPC without current constraint (blue) and (b) Time Optimal Boundary control laws (black) compared with proposed FCS-MPC with current Constraint (red)

Finally, figure 31 presents the frequency component of the gating signals, when the output current is maintained at 1 A under the same conditions as the simulation of figure 28. The objective is to validate the target switching frequency implemented by Δr is reached.

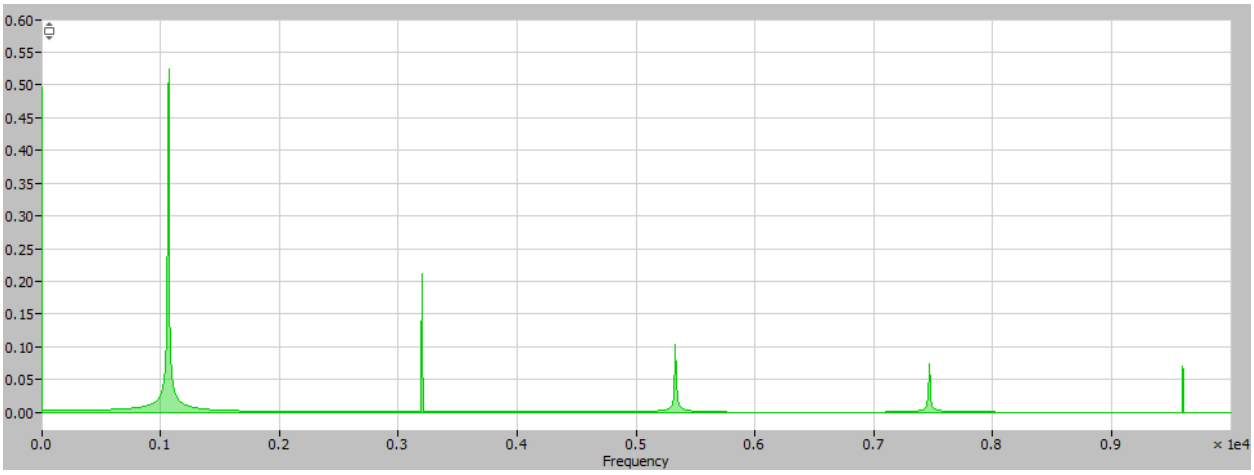


Figure 31: Fourier Analysis of the Gate signal for Buck Converter

In this figure, there is a DC component of value 0.5 V because the signal is a square wave with a highest value at 1 V and a lowest value at 0 V. The fundamental is located at 1070 Hz with harmonics at 3210 and 5350 Hz which is expected for a square wave of fundamental 1070 Hz. Therefore, the switching frequency is at 1070 Hz which is close to the objective of 1 kHz implemented.

3.6.2 DC-DC Boost Converter

This section compares dynamic performances of Time Optimal Boundary control laws of [14] and the proposed FCS-MPC of figure 26 with parameters adjusted for boost converter. Both control schemes are implemented to regulate the output voltage of the DC-DC boost converter in figure 20 in Simulink with L=1.07mH, C = 267µF, V_{cc} = 5 V, V_r = 10 V, Ts = 1.25µs and a desired switching frequency f_{sw}=1 kHz. Figure 32 illustrates the evolution of converter states in time domain during a start-up transient ($I_o = 0.12\ A$), loading transient (I_o increasing to 2 A) and unloading transient (I_o decreasing to 1 A) when the time optimal boundary control of [14] is applied. Figure 33 shows the evolution of the converter states under the same conditions when the proposed FCS-MPC is applied without voltage constraints.

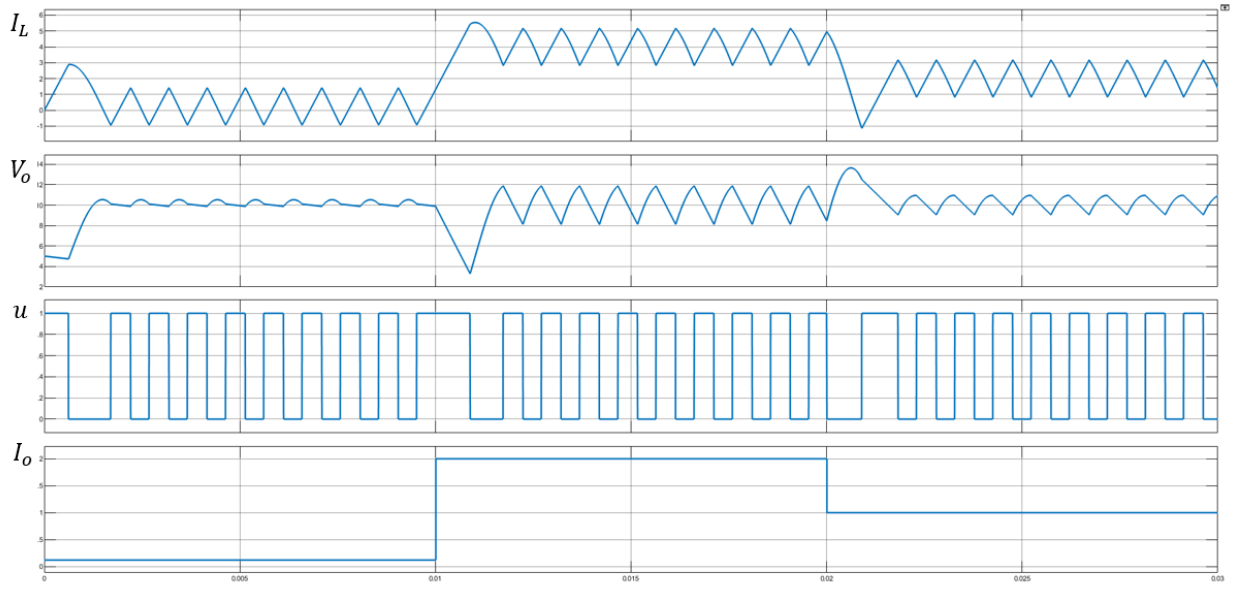


Figure 32: Evolution of Boost converter States and control actions when Time Optimal Boundary Control of [14] is applied

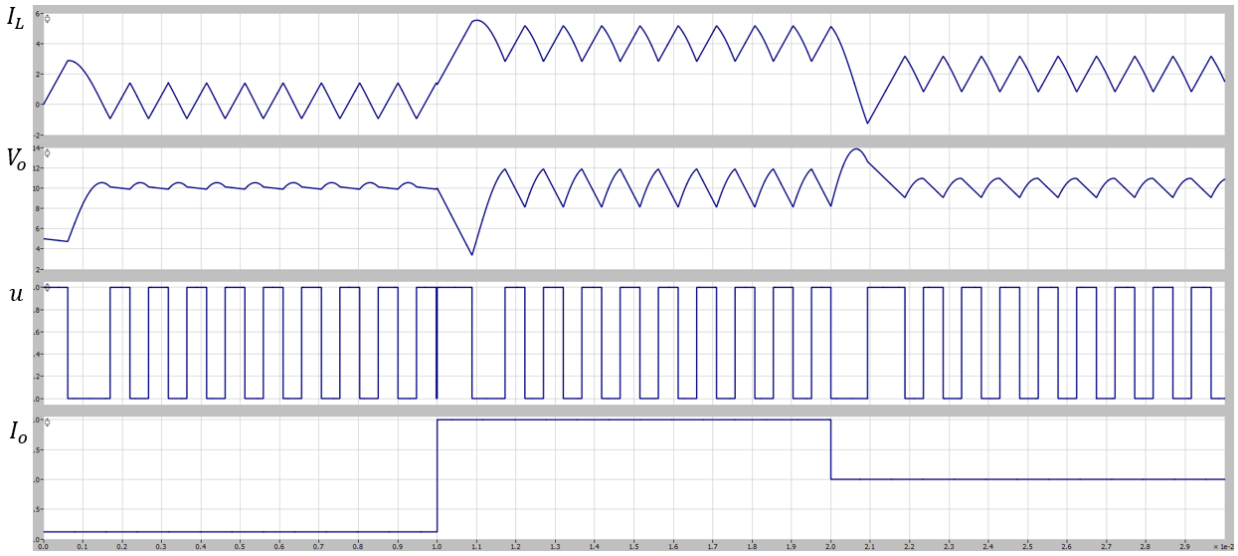


Figure 33: Evolution of Boost converter States and control actions when proposed FCS-MPC without voltage constraint is applied

As illustrated in figure 35a, the dynamic performance of time optimal boundary control and FCS-MPC wihtout constraint are identical

The next simulation consists in investigating the performance of the FCS-MPC under the same condition as figure 33 but applying a voltage deviation constraint $|V_{on} - 1| < 0.5$ meaning that the deviation should not exceed 5 V. The evolution of converter states with the FCS-MPC with this voltage constraint is shown in figure 34.

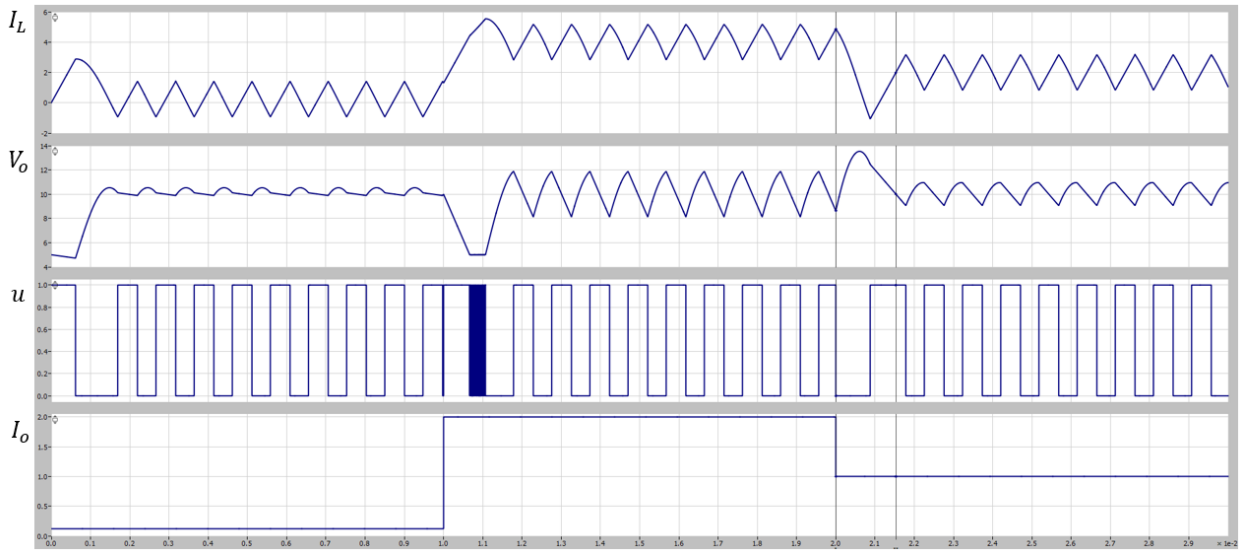


Figure 34: Evolution of Boost converter States and control actions when proposed FCS-MPC with voltage constraint is applied

Figure 35b shows that the voltage deviation constraint associated with the algorithm in figure 26 exhibits excellent voltage deviation performance with almost no impact on recovery time indices when compared to time optimal boundary controller.

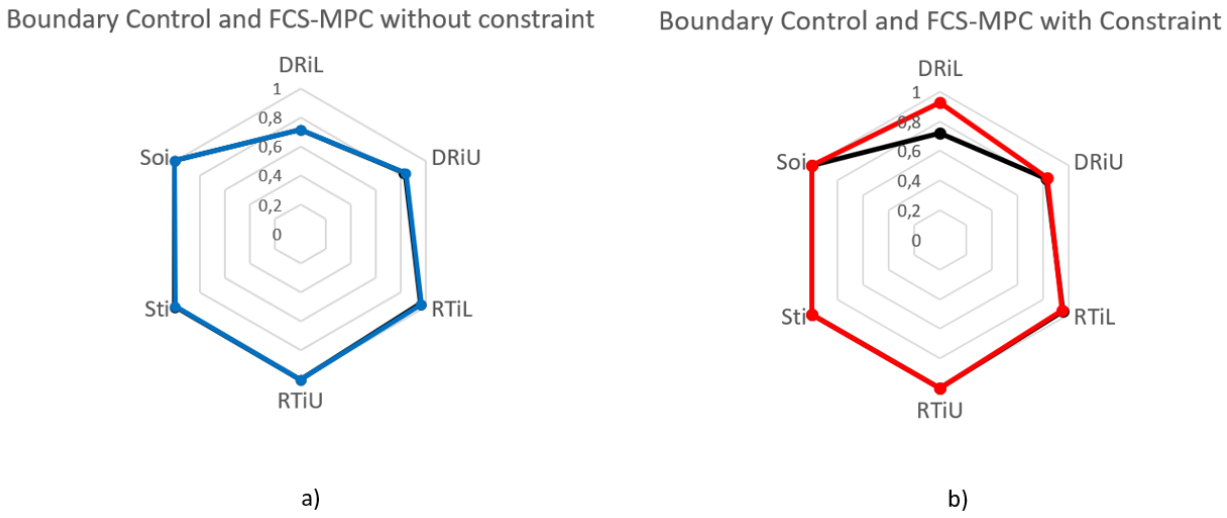


Figure 35:Benchmarking indices of (a) Time Optimal Boundary control laws (black) compared with proposed FCS-MPC without voltage constraint (blue) and (b) Time Optimal Boundary control laws (black) compared with proposed FCS-MPC with Voltage Constraint (red)

Finally, figure 36 presents the frequency component of the gating signals, when the output current is maintained at 1 A under the same conditions as the simulation of figure 28. The objective is to validate the target switching frequency implemented by Δr^2 is reached.

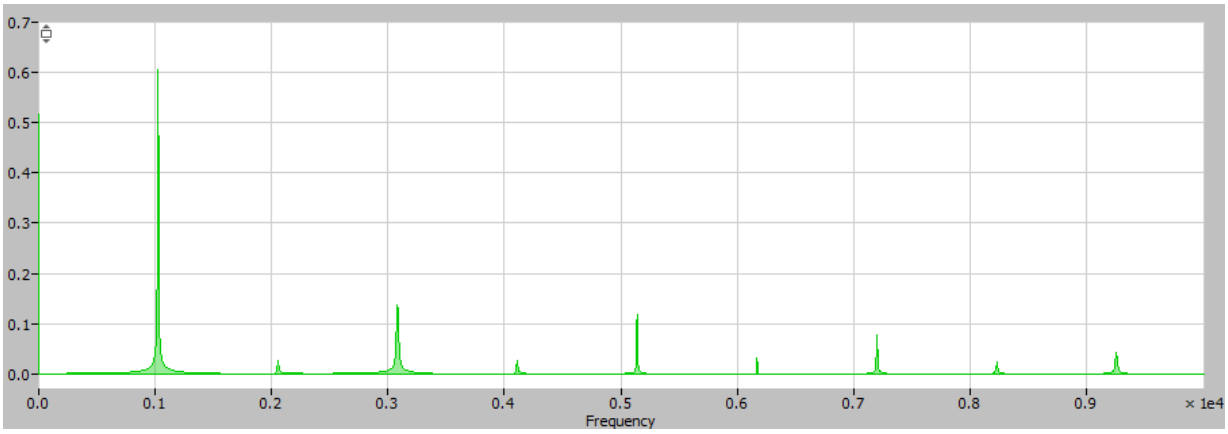


Figure 36: Fourier Analysis of the Gate signal for Boost Converter

In this figure, there is a DC component of value 0.5 V because the signal is a square wave with a highest value at 1 V and a lowest value at 0 V. The fundamental is located at 1030 Hz with harmonics at 3090 and 5150 Hz which is expected for a square wave of fundamental 1030 Hz. Therefore, the switching frequency is at 1030 Hz which is close to the objective of 1 kHz implemented.

3.6.3 DC-DC Buck-Boost Converter

This section compares dynamic performances of Time Optimal Boundary control laws of [21] and the proposed FCS-MPC of figure 26 with parameters adjusted for buck-boost converter. Both control schemes are implemented to regulate the output voltage of the DC-DC buck-boost converter in figure 20 in Simulink with L=1.07mH, C = 267µF, V_{cc} = 10V, V_r = 10V, Ts = 1.25µs and a desired switching frequency f_{sw}=1 kHz. Figure 37 illustrates the evolution of converter states in time domain during a start-up transient ($I_o = 0.12\ A$), loading transient (I_o increasing to 2 A) and unloading transient (I_o decreasing to 1 A) when the time optimal boundary control of [20] is applied. Figure 38 shows the evolution of the converter states under the same conditions when the proposed FCS-MPC is applied without voltage constraints.

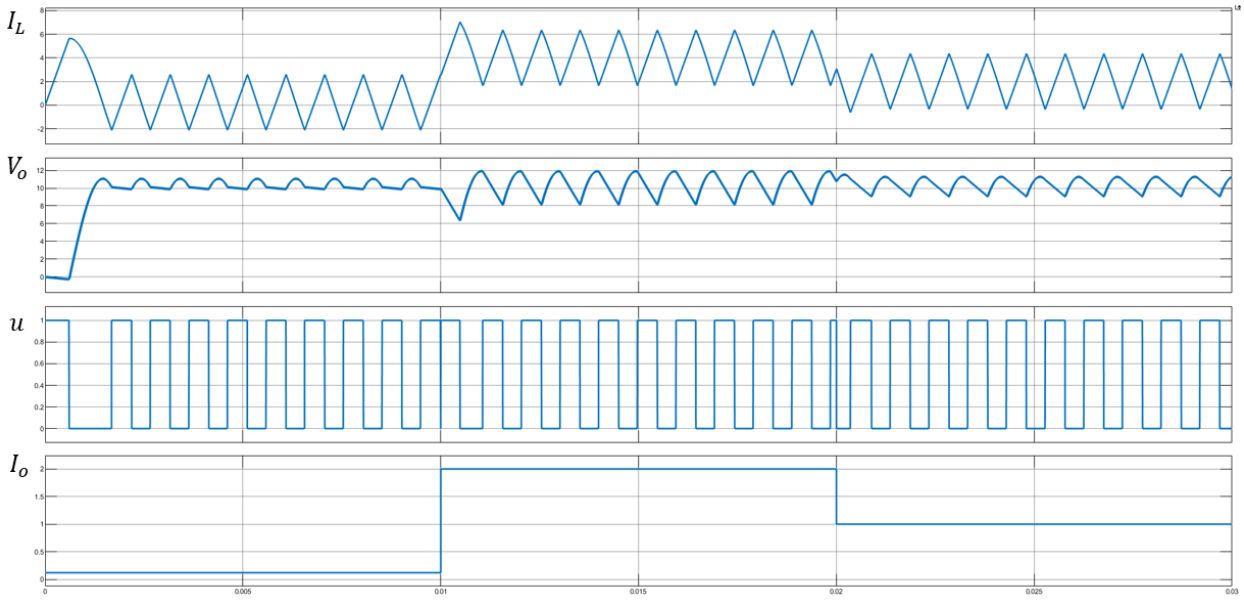


Figure 37:Evolution of Buck-Boost converter States and control actions when Time Optimal Boundary Control of [20] is applied

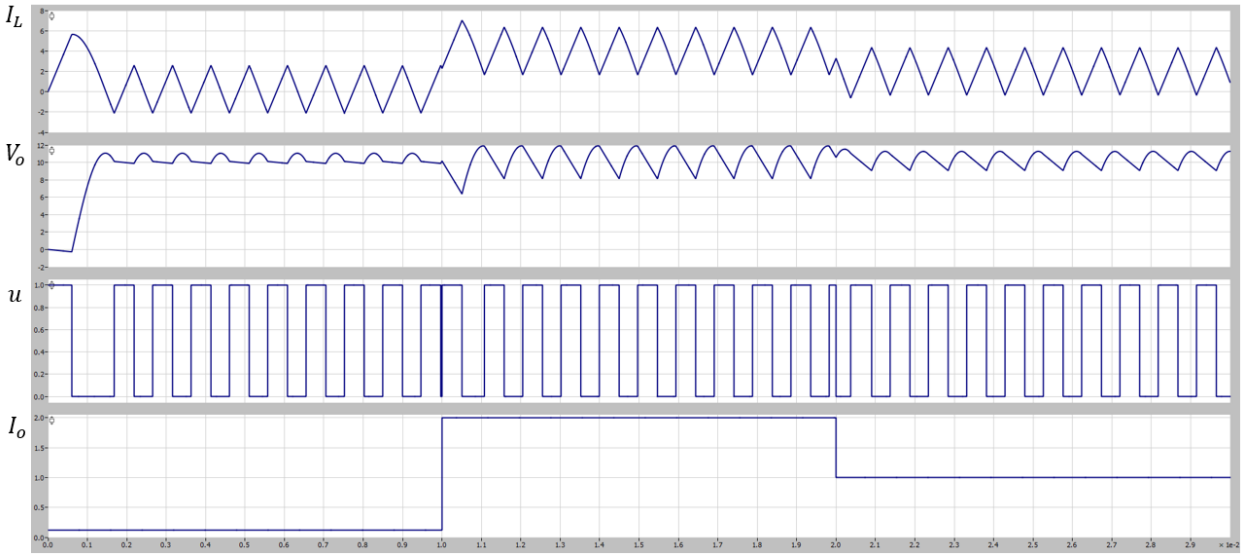


Figure 38: Evolution of Buck-Boost converter States and control actions when proposed FCS-MPC without voltage constraint is applied

For both, control schemes, the actual switching frequency is approaching the target frequency of 1 kHz. As illustrated in figure 40a, the dynamic performance of time optimal boundary control

and FCS-MPC wihtout constraint are identical with poor performance for voltage deviation index under loading transient.

The next simulation consists in investigating the performance of the FCS-MPC under the same condition as figure 38 but applying a voltage deviation constraint $|V_{on} - 1| < 0.2$ meaning that the deviation should not exceed 2V. The evolution of converter states with the FCS-MPC with this voltage constraint is shown in figure 39.

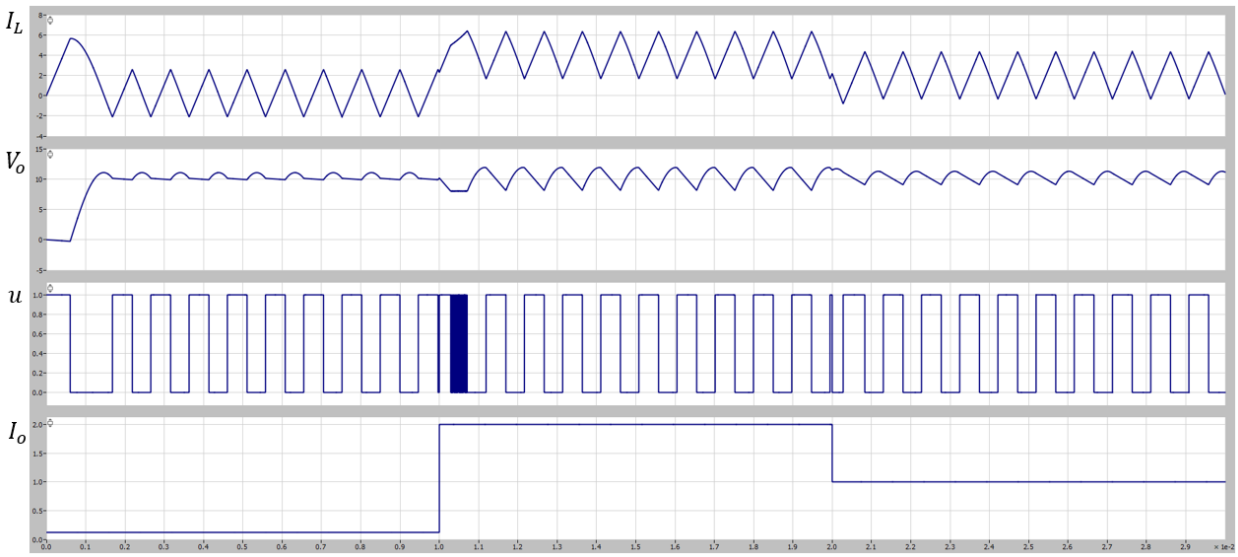


Figure 39: Evolution of Buck-Boost converter States and control actions when proposed FCS-MPC with voltage constraint is applied

Figure 40b shows that the voltage deviation constraint associated with the algorithm in figure 26 exhibits good voltage deviation performance for both loading and unloading transient with good recovery time performances.

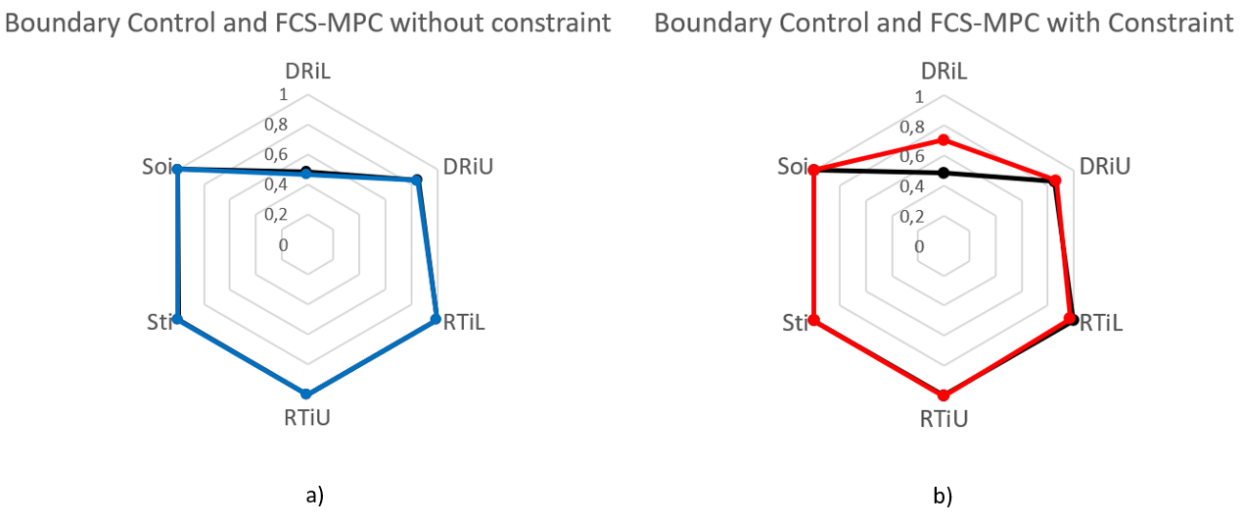


Figure 40: Benchmarking indices of (a) Time Optimal Boundary control laws (black) compared with proposed FCS-MPC without voltage constraint (blue) and (b) Time Optimal Boundary control laws (black) compared with proposed FCS-MPC with Voltage Constraint (red)

Finally, figure 40 presents the frequency component of the gating signals, when the output current is maintained at 1 A under the same conditions as the simulation of figure 38. The objective is to validate the target switching frequency implemented by Δr^2 is reached.

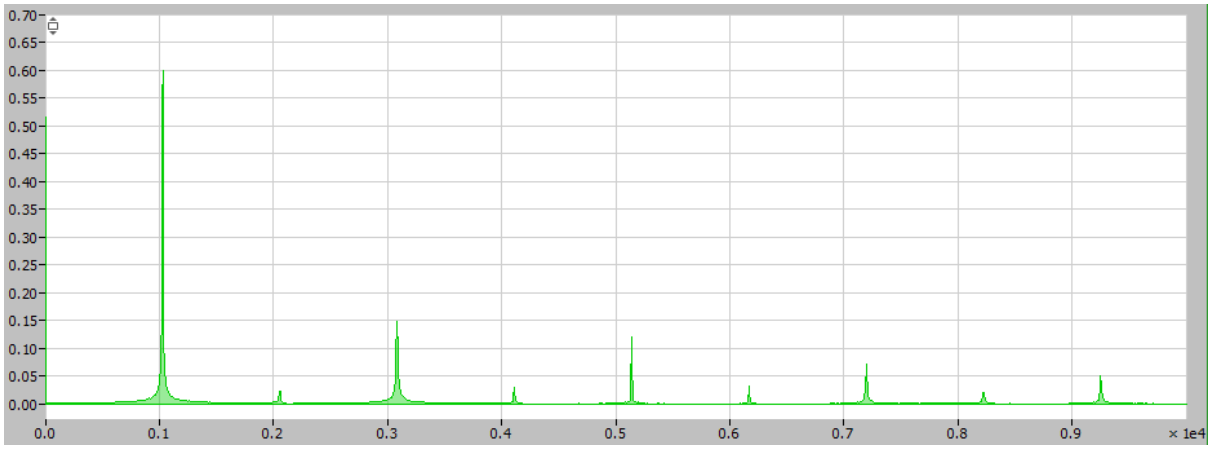


Figure 41: Fourier Analysis of the Gate signal for Buck-Boost Converter

In this figure, there is a DC component of value 0.5 V because the signal is a square wave with a highest value at 1 V and a lowest value at 0 V. The fundamental is located at 1030 Hz with harmonics at 3090 and 5150 Hz which is expected for a square wave of fundamental 1030 Hz. Therefore, the switching frequency is at 1030 Hz which is close to the objective of 1 kHz implemented.

3.7 Control Hardware in-the-Loop Experiment Results

This section presents the results of real time experiments of the proposed control schemes. As illustrated by figure 42, each converter of figure 20 is simulated by the Typhoon HIL box 402 while the proposed control schemes are integrated into a TI23879s using PLECS coder. During the Control Hardware-in-the-Loop (CHIL) simulation, the control card and the real time simulation of a non-isolated dc-dc converter interact thanks to the DSP 180 interface card.

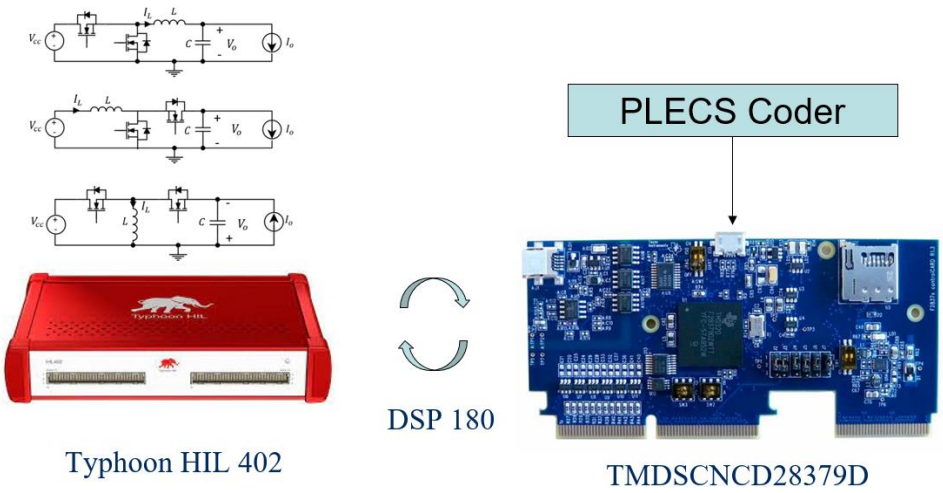


Figure 42: Hardware-in-the-Loop (HIL) simulation of a non-isolated dc-dc converter with the proposed FCS-MPC

Figure 43 shows the CHIL experimental set up where the C code of the proposed FCS-MPC of figure 26 is first implemented using PLECS coder as shown in figure 44.

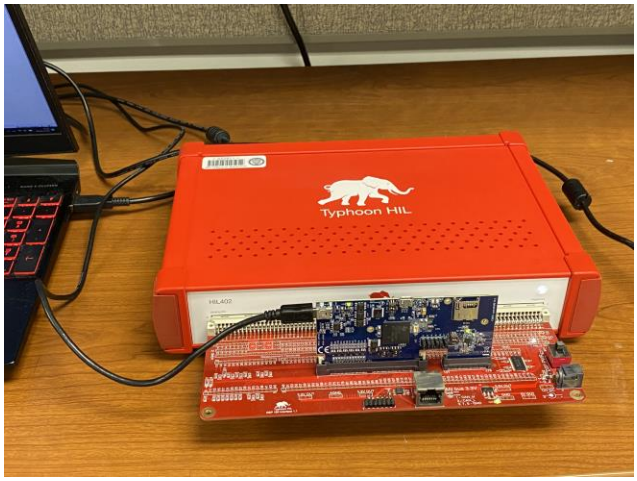


Figure 43: Experimental setup for the Control Hardware-in-the-Loop simulation

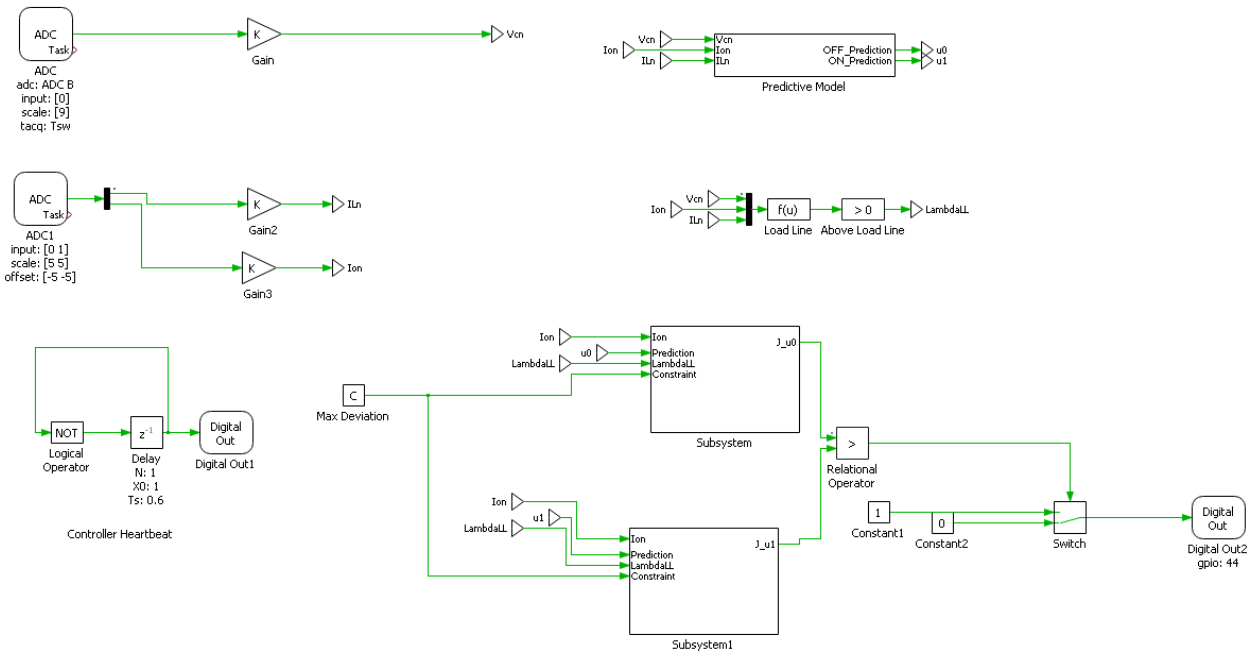


Figure 44: Proposed FCS-MPC for the boost converter on PLECS CODER

After that, the dc-dc converter real time simulation is launched where data can be collected on HIL scada after drawing the dc-dc converter using the Typhoon schematic editor.

3.7.1 Buck Converter

This section presents the experimental result of the proposed control scheme for the buck converter where L=1.07mH, C = 267µF, V_{cc} = 10V, V_r = 5V, Ts = 50 µs and a desired switching frequency f_{sw}=1 kHz. The constraint has been set to limit the inductor current to 3.8 A. Figure 45 presents the inductor current, output voltage and gate signals waveform for the start-up transient.

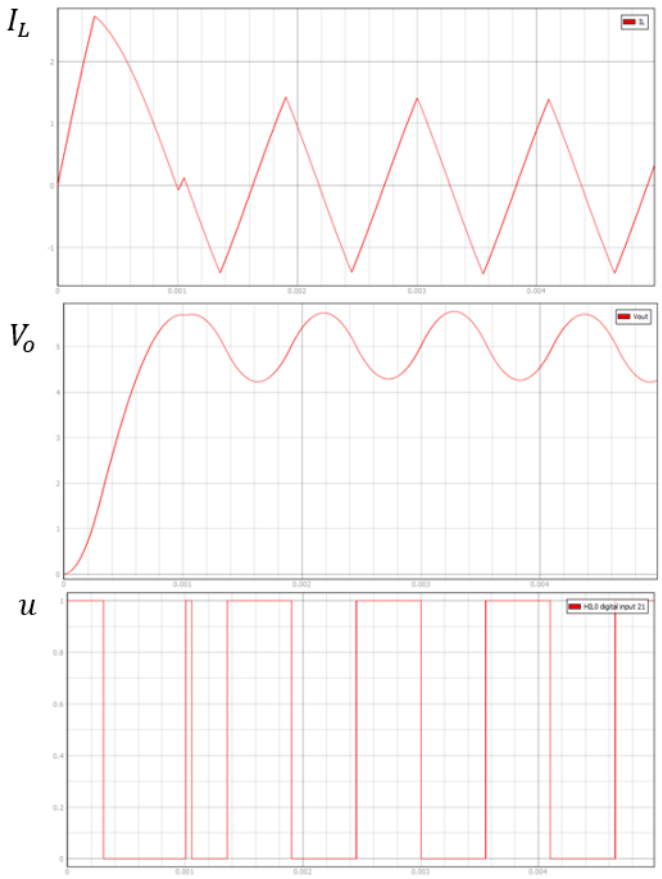


Figure 45: CHIL simulation result of I_L (top), V_o (middle) and u (left) of the buck converter under start-up transient

Figure 46 present the CHIL experiment results for the loading transient where the output current increased from 0.001 A to 2A. The inductor current is limited by the current constraint set in the proposed FCS-MPC but still exceeds the constraint. This is due to the important sampling period that has an impact on the precision of the internal dynamic model.

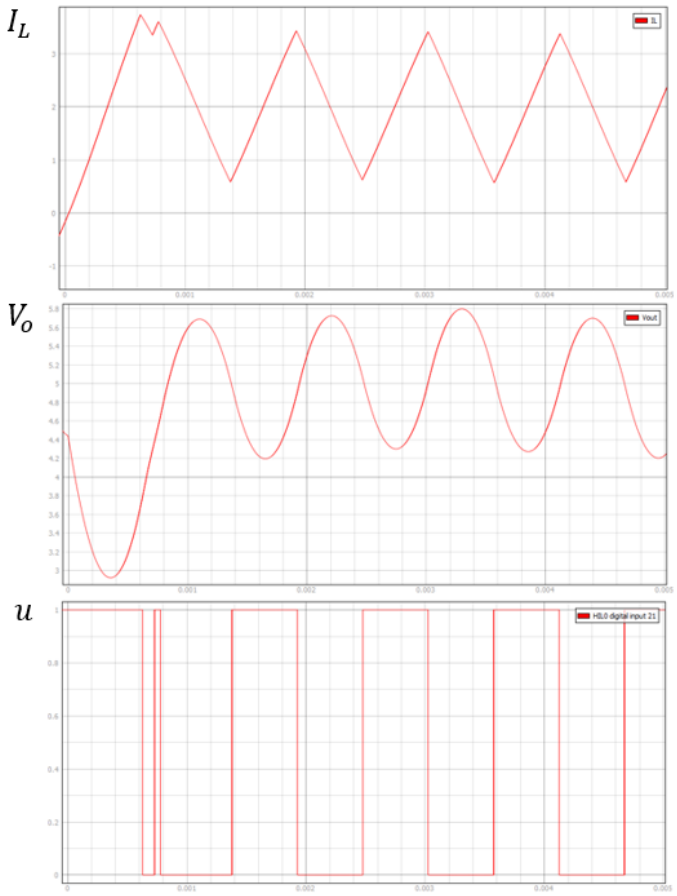


Figure 46: CHIL simulation result of I_L (top), V_o (middle) and u (left) of the buck converter under loading transient

Figure 47 present the CHIL experiment results for the unloading transient where the output current decreased from 2 A to 1 A.

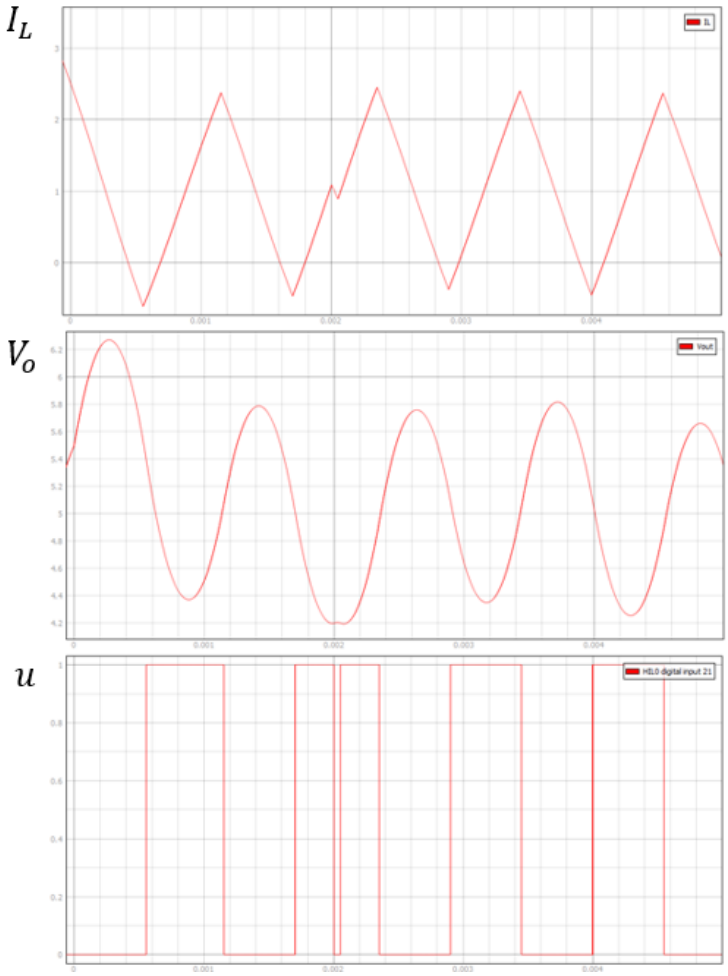


Figure 47: CHIL simulation result of I_L (top), V_o (middle) and u (left) of the buck converter under unloading transient

Figure 48 presents the benchmarking indices for the CHIL simulation of the proposed FCS-MPC applied for the buck converter. In this figure the voltage deviation indices are slightly worse than the indices presented in figure 30 due to the important sampling frequency.

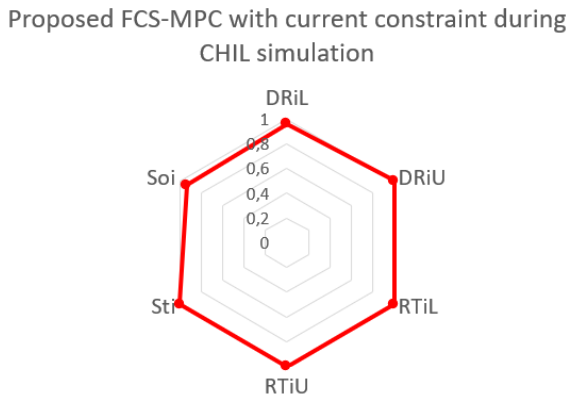


Figure 48: Benchmarking indices of proposed FCS-MPC with Current Constraint for Buck

Finally, figure 49 presents the frequency component of the gating signals, when the output current is maintained at 1 A like figure 31.

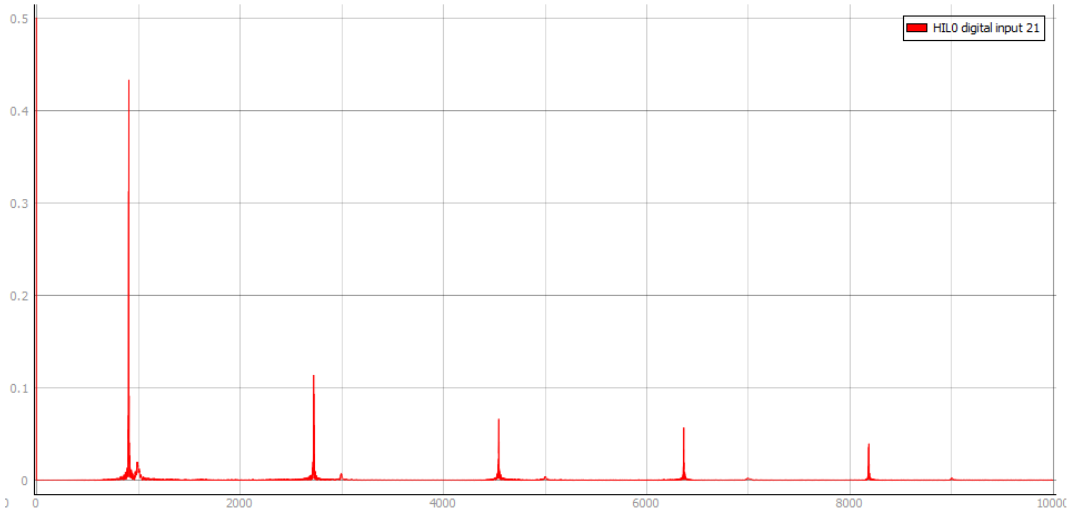


Figure 49: Fourier Analysis of the Gate signal for Buck Converter

In this figure, there is a DC component of value 0.5 V. The fundamental is located at 910 Hz with harmonics at 2730 and 4550 Hz which is expected for a square wave of fundamental 910 Hz. Therefore, the switching frequency is at 910 Hz which is close to the objective of 1 kHz implemented.

3.7.2 Boost Converter

This section presents the experimental result of the proposed control scheme for the boost converter where L=1.07mH, C = 267μF, V_{cc} = 5V, V_r = 10V, Ts = 50 μs and a desired switching frequency f_{sw}=1 kHz. The constraint has been set to limit the voltage deviation to 6 V. Figure 50 presents the inductor current, output voltage and gate signals waveform for the start-up transient.

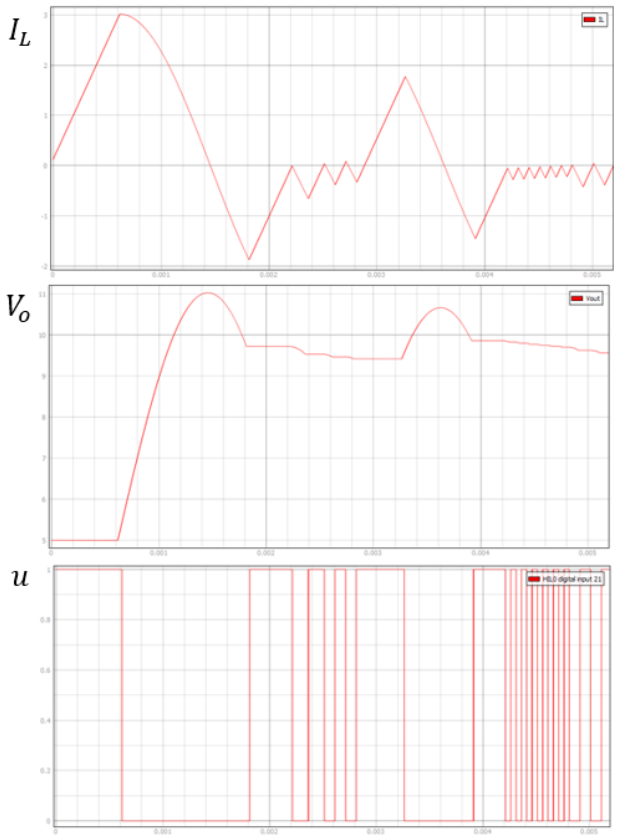


Figure 50: CHIL simulation result of I_L (top), V_o (middle) and u (left) of the boost converter under start-up transient

Figure 51 present the CHIL experiment results for the loading transient where the output current increased from 0.001 A to 2A. The voltage is limited by the voltage deviation constraint set in

the proposed FCS-MPC but still exceeds the constraint. This is due to the important sampling period that has an impact on the precision of the internal dynamic model.

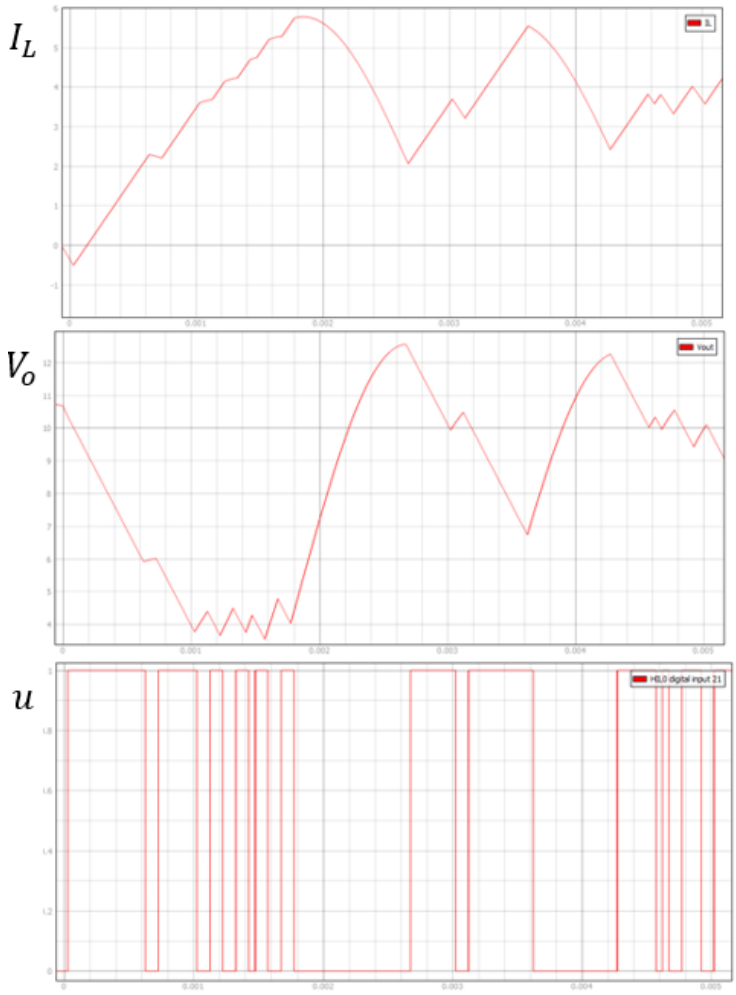


Figure 51: CHIL simulation result of I_L (top), V_o (middle) and u (left) of the boost converter under loading transient

Figure 52 present the CHIL experiment results for the unloading transient where the output current decreased from 2 A to 1 A.

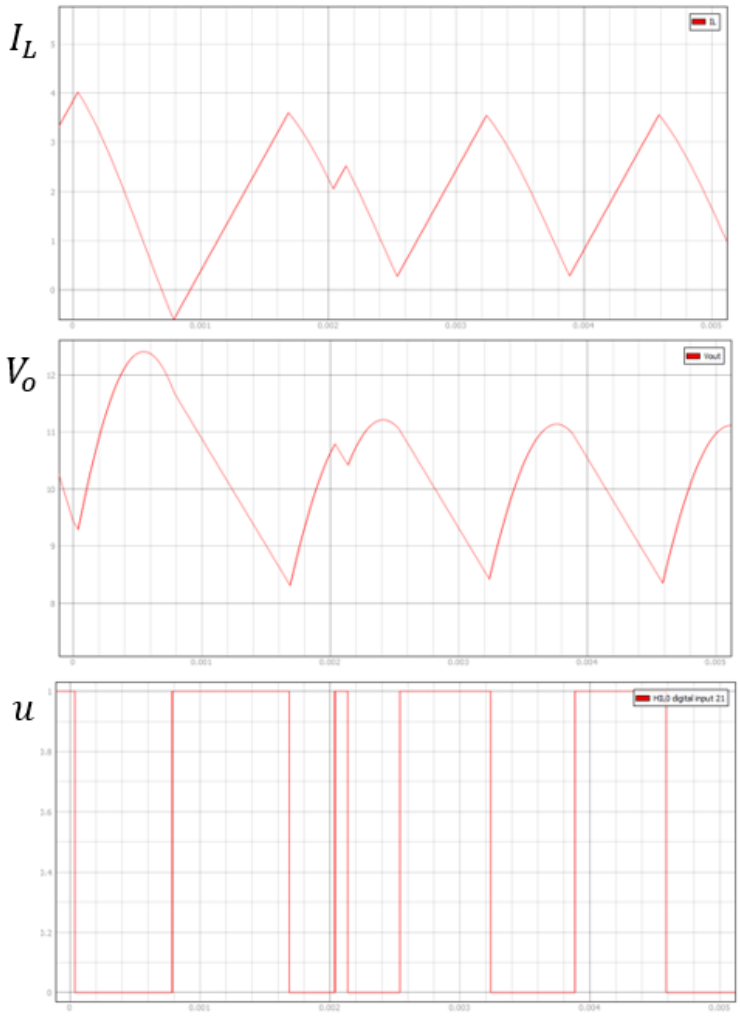


Figure 52: CHIL simulation result of I_L (top), V_o (middle) and u (left) of the boost converter under unloading transient

Figure 53 presents the benchmarking indices for the CHIL simulation of the proposed FCS-MPC applied for the boost converter. In this figure the unloading voltage deviation and start-up overshoot indices are slightly worse than the indices presented in figure 35 due to the important sampling frequency.

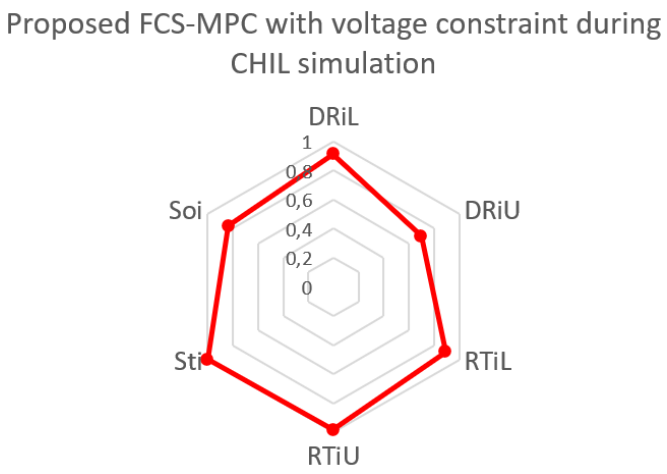


Figure 53: Benchmarking indices of proposed FCS-MPC with Voltage Constraint for Boost

Finally, figure 54 presents the frequency component of the gating signals, when the output current is maintained at 1 A like figure 36.

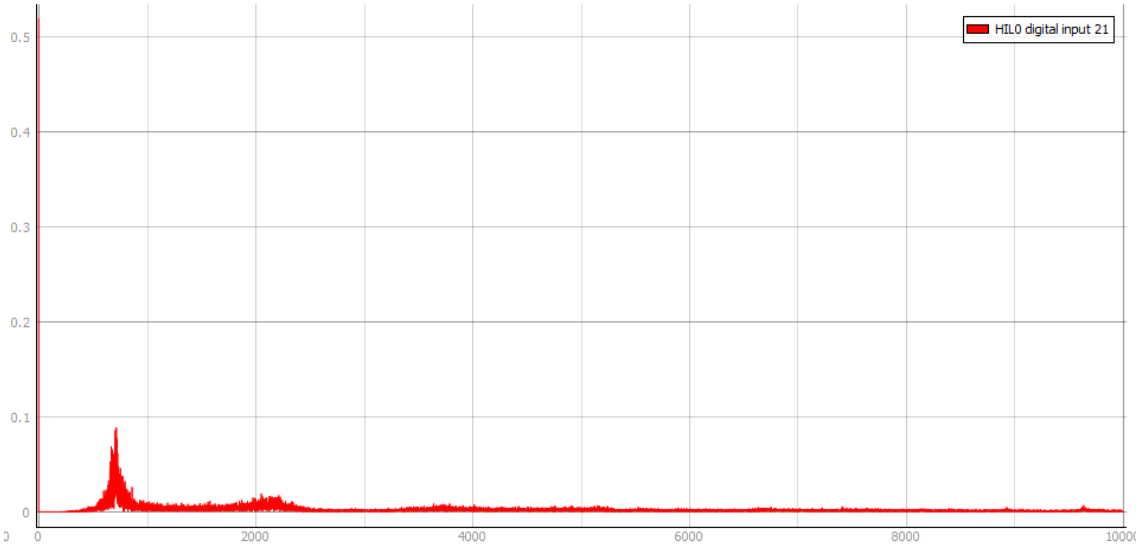


Figure 54: Fourier Analysis of the Gate signal for Boost Converter

In this figure, there is a DC component of value 0.5 V. The switching frequency is at 710 Hz which does not correspond to the objective of 1 kHz implemented.

3.7.3 Buck-Boost Converter

This section presents the experimental result of the proposed control scheme for the boost converter where L=1.07mH, C = 267µF, V_{cc} = 10V, V_r = 10V, Ts = 50 µs and a desired switching frequency f_{sw}=1 kHz. The constraint has been set to limit the voltage deviation to 6 V. Figure 55 presents the inductor current, output voltage and gate signals waveform for the start-up transient.

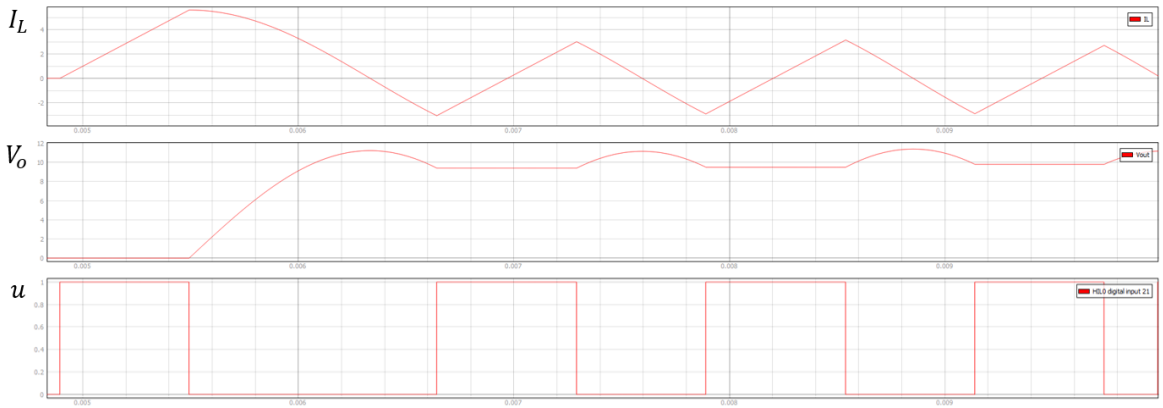


Figure 55: CHIL simulation result of I_L (top), V_o (middle) and u (left) of the buck converter under start-up transient

Figure 56 present the CHIL experiment results for the loading transient where the output current increased from 0.001 A to 2A. The voltage is limited by the voltage deviation constraint set in the proposed FCS-MPC but still exceeds the constraint. This is due to the important sampling period that has an impact on the precision of the internal dynamic model.

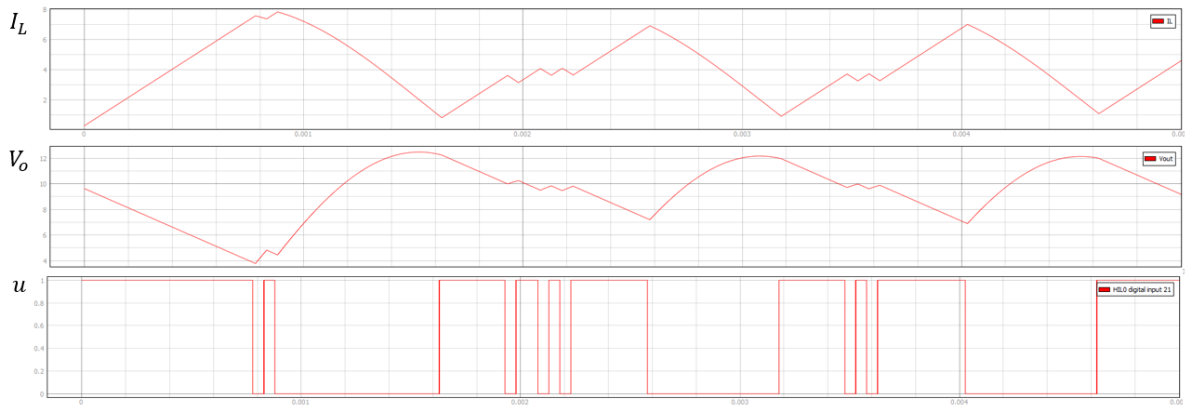


Figure 56: CHIL simulation result of I_L (top), V_o (middle) and u (left) of the buck-boost converter under loading transient

Figure 57 present the CHIL experiment results for the unloading transient where the output current decreased from 2 A to 1 A.

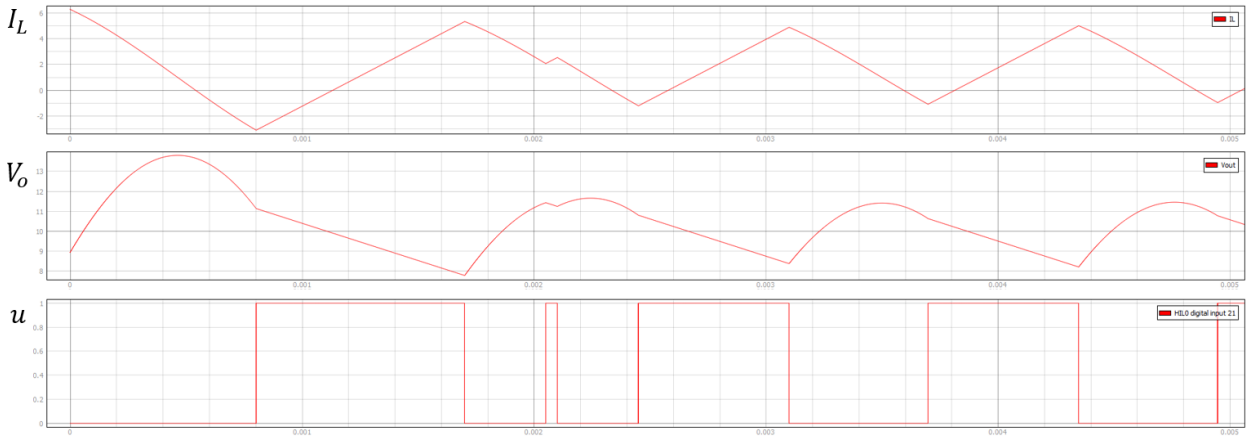


Figure 57: CHIL simulation result of I_L (top), V_o (middle) and u (left) of the buck-boost converter under unloading transient

Figure 58 presents the benchmarking indices for the CHIL simulation of the proposed FCS-MPC applied for the boost converter. In this figure the loading voltage deviation is slightly

worse than the indices presented in figure 40 because the voltage deviation constraint is larger in the case of the CHIL simulation.

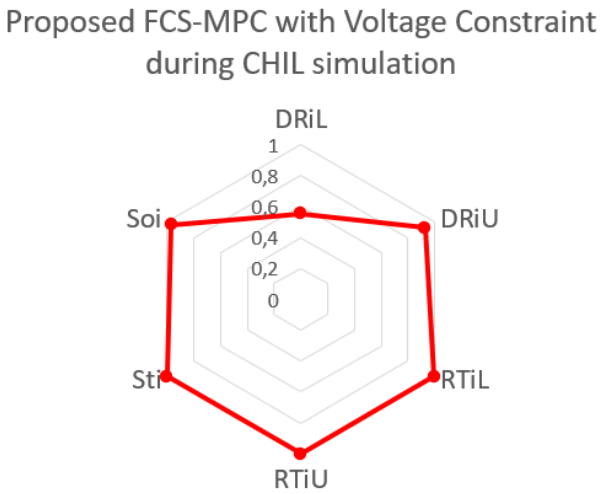


Figure 58: Benchmarking indices of proposed FCS-MPC with Voltage Constraint for Buck-Boost

Finally, figure 59 presents the frequency component of the gating signals, when the output current is maintained at 1 A like figure 41.

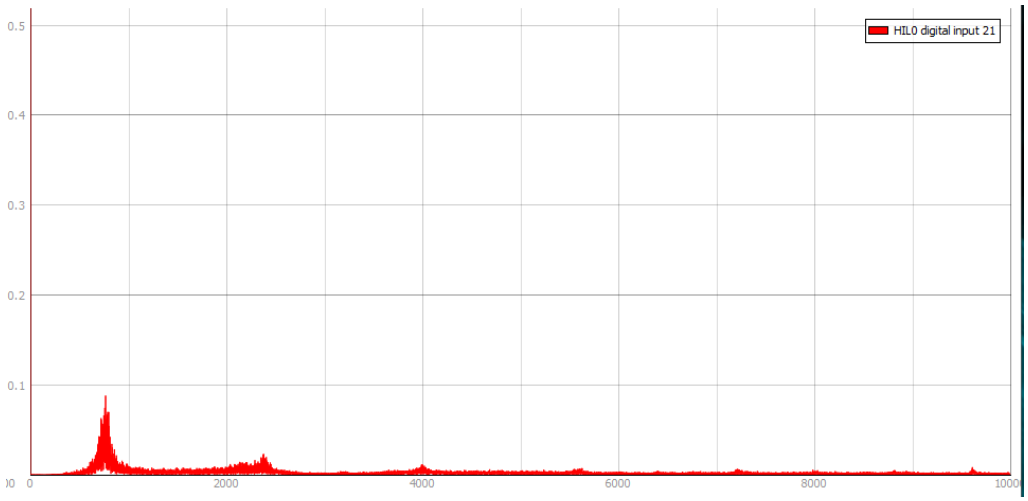


Figure 59: Fourier Analysis of the Gate signal for Buck-Boost Converter

In this figure, there is a DC component of value 0.5 V. The switching frequency is at 770 Hz which does not correspond to the objective of 1 kHz implemented.

3.8 Sensitivity of Converter and Proposed FCS-MPC parameters

The first objective of this section aims at studying the impact of DC-DC converter parameters on the generalized proposed FCS-MPC performance using the benchmarking indices. Section 3.8.1 and 3.8.2 present the impact of output capacitance *C* and inductance *L* respectively. Section 3.8.3 details the proposed control performance for different values of input voltage for each DC-DC converter. The second objective is to discuss the influence of the proposed FCS-MPC design parameters on the control performance. Section 3.8.4 presents the proposed control performances with different values for the sampling period while section 3.8.5 deals with the target switching frequency parameter. Section 3.8.6 studies the influence of a delay on the application of the control decision on the performance of the proposed FCS-MPC.

3.8.1 Sensitivity of the inductance L on control performance

Figure 60 presents the dynamic performance of each DC-DC converter when the value of the inductance L is different from the nominal value used by the proposed FCS-MPC. For each DC-DC converter, the base inductance value L is set to $1.07\,mH$, C is equal to $267\,\mu F$ with a sampling period $T_{sw} = 1.25\,\mu s$. For the buck converter, $V_{cc} = 10\,V$, $V_r = 5\,V$ and the inductor current is limited to $3.2\,A$ with a target switching frequency of $1\,kHz$. For the boost converter , $V_{cc} = 5\,V$, $V_r = 10$V with a voltage deviation constraint of $5\,V$ and a target switching frequency

of $1\,kHz$. For the buck-boost converter, $V_{cc} = 10\,V$, $V_r = 10\text{V}$ with a voltage deviation constraint of $5\,V$ and a target switching frequency of $1\,kHz$. These conditions allow for each converter to have comparable operating points.

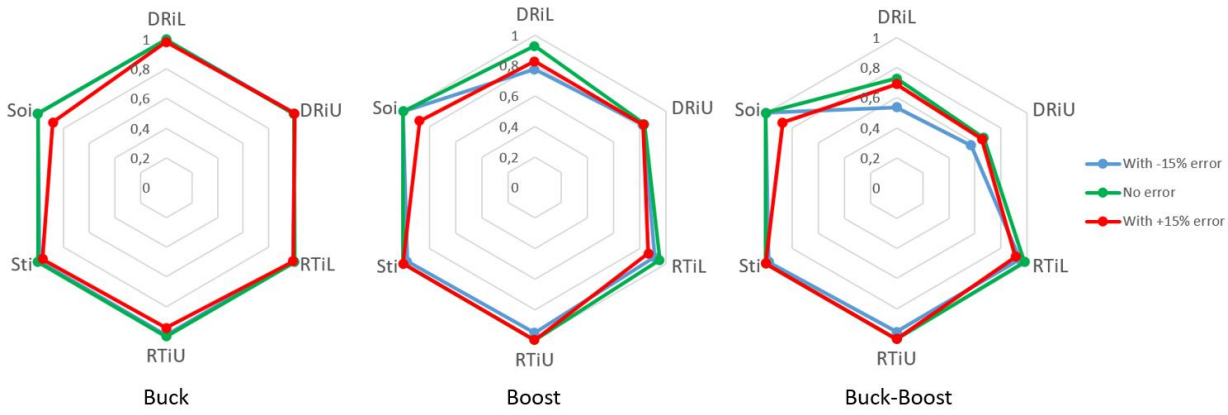


Figure 60: Dynamic Performance indices of DC-DC converters with variations in L

In the case of the buck converter, only the deviation performance for start-up transient (*SOi*) seems to be significantly impacted by an alteration of 15% in the inductance value. Recall, for the boost and buck-boost converters the constraint is set to improve the voltage deviation performance DRi_L. Figure 60 shows this performance index can be significantly impacted while recovery time performances are less impacted. The alteration of inductance value L causes an error in the states' predictions from the internal dynamic model that uses the nominal inductance value. This error can cause a delay in the switching action timing that increases recovery time and voltage deviation. However, if this increase in recovery time is relatively small compared to the minimum recovery time (3-28), the resulting increase in voltage deviation can be significant when compared to the minimum voltage deviation. This can be demonstrated by the following example.

In this example, a 15% change in the inductance value causes a delay in the ON switching of 150 sampling periods with respect to time optimal control during the loading transient. With an initial condition of $I_L(0) = 1.1\,A$ and $V_o = 10.22V$, the minimum recovery time is $0.0013\,s$ with an expected deviation of around $7V$ ($DRi_L = 0.779$) from calculations provided in section 3.3.2. With this recovery time delay of 150 sampling periods of $1.25\,\mu s$, the recovery time index RTi_L is equal to 0.971 and with an expected voltage deviation of 8.4 V (increase of 1.4 V from the switch ON delay and (3-2)) equivalent to a voltage deviation index DRi_L equal to 0.64. This example illustrates that a potential delay from the prediction error causes a much larger difference in the voltage deviation index than in the recovery time index.

3.8.2 Sensitivity of the Capacitance C on control performance

Figure 61 presents the dynamic performance of each DC-DC converter when the value of the capacitance C is different from the value used by the proposed FCS-MPC. For the buck converter, $V_{cc} = 10\,V$, $V_r = 5\,V$ and the inductor current is limited to $3.2\,A$ with a target switching frequency of $1\,kHz$. For the boost converter , $V_{cc} = 5\,V$, $V_r = 10$V with a voltage deviation constraint of $7\,V$ and a target switching frequency of $1\,kHz$. For the buck-boost converter, $V_{cc} = 10\,V$, $V_r = 10$V with a voltage deviation constraint of $5\,V$ and a target switching frequency of $1\,kHz$.

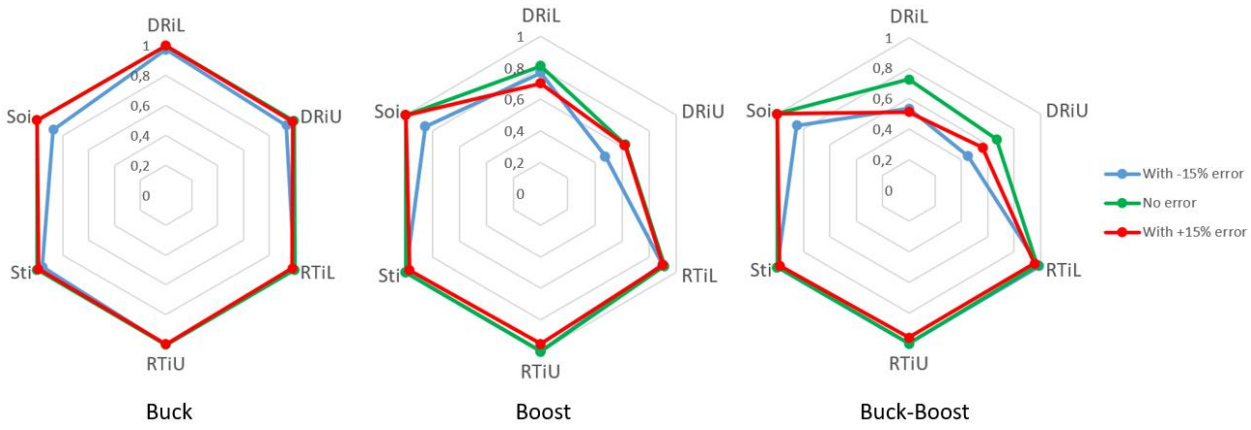


Figure 61: Dynamic Performance indices of DC-DC converters with variations in C

For the three DC-DC converters, a deviation from nominal in the capacitance has a moderate influence on the voltage deviation performance for start-up transient. In the case of the boost and buck-boost, voltage deviation performance indices are more impacted than recovery time performance indices like in section 3.8.1. An alteration of the C value also causes errors in the prediction of converter states with potential switching delays. As seen in section 3.8.1, these delays impact more voltage deviation indices than recovery time indices.

3.8.3 Impact of input voltage V_{cc}

Figure 62 presents the dynamic performance of each DC-DC converter for different values of input voltage V_{cc}. For each DC-DC converter, L is set to $1.07\,mH$, C is equal to $267\,\mu F$ with a sampling period $T_{sw} = 1.25\,\mu s$. For the buck converter $V_r = 5\,V$ and the inductor current is limited to $3.2\,A$ with a target switching frequency of $1\,kHz$. For the boost converter $V_r = 10\text{V}$ with a voltage deviation constraint of $10\,V$ and a target switching frequency of $1\,kHz$. For the buck-boost converter, $V_r = 10\text{V}$ with a voltage deviation constraint of $10\,V$ and a target switching frequency of $1\,kHz$.

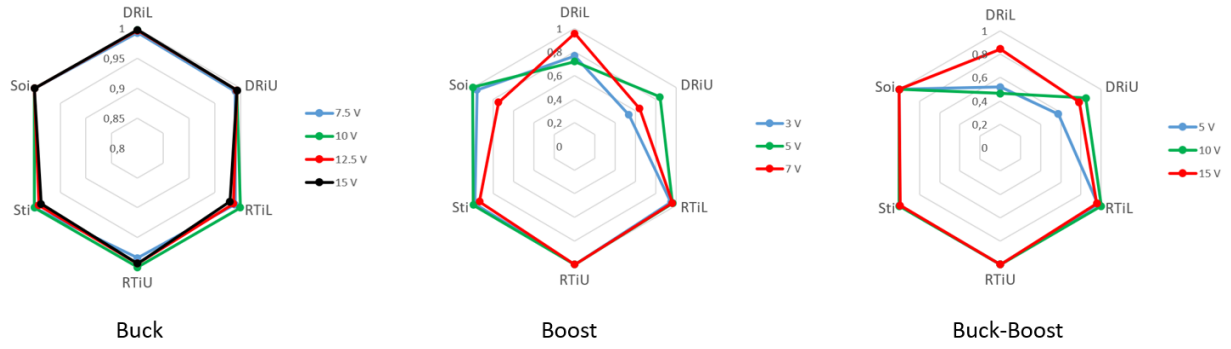


Figure 62: Dynamic Performance indices of DC-DC converters with different values of Input Voltage

The results from figure 62 confirm that the proposed FCS-MPC ensures a time optimal control for various operating points of each converter. Voltage deviation indices fluctuate with the operating point. These variations come from the calculation of minimum voltage deviation in (3-29), (3-30), (3-46) and (3-47) that depends on the input voltage. Therefore, for a constant voltage deviation, the index varies because the expected minimum voltage deviation in (3-12) varies.

3.8.4 Impact of sampling Period T_s

Figure 63 presents the dynamic performance of each DC-DC converter for different values of sampling period including $1.25, 15, 30, 45$ and $60\ \mu s$. Parameters for each DC-DC converter and the associated proposed FCS-MPC are identical to section 3.8.1.

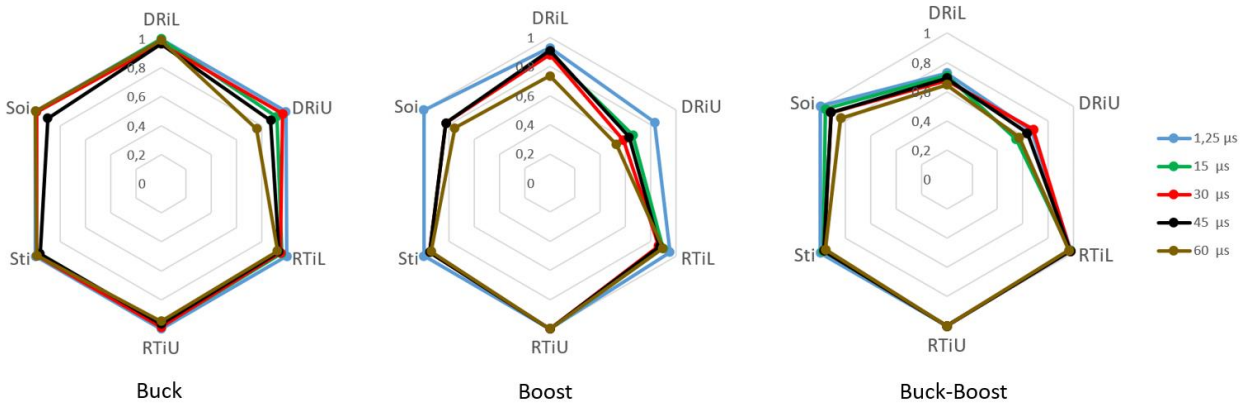


Figure 63: Dynamic Performance indices of DC-DC converters with different values of sampling period

For each converter, each performance index is degraded as the sampling period is increased. However, performance indices related to voltage deviations are more impacted by the increase of sampling period than recovery time performance indices. The increase in sampling period delays the switching action with respect to the time optimal control. As stated in section 3.8.1, this delay has more impact on the voltage deviation indices than on recovery time indices. A significant degradation is observed at a sampling period of $60\mu s$.

3.8.5 Maximum Target Switching Frequency

A target switching frequency can be implemented in the cost function expression thanks to Δr for buck and Δr^2 for boost and buck-boost converter. The calculation of Δr^2 and Δr associated with a target switching frequency is given in (3-66) and (3-71) respectively. A smaller value of Δr^2 or Δr leads to higher switching frequency. Since the switching frequency cannot exceed the sampling frequency of the controller, the target switching frequency used in the calculation of Δr^2 or Δr should never be greater than the sampling frequency.

3.8.6 Impact of delay on control decision application

Figure 64 presents the dynamic performance of each DC-DC converter for different time delays on the control decision application. Parameters for each DC-DC converter and the associated proposed FCS-MPC are identical to section 3.8.1.

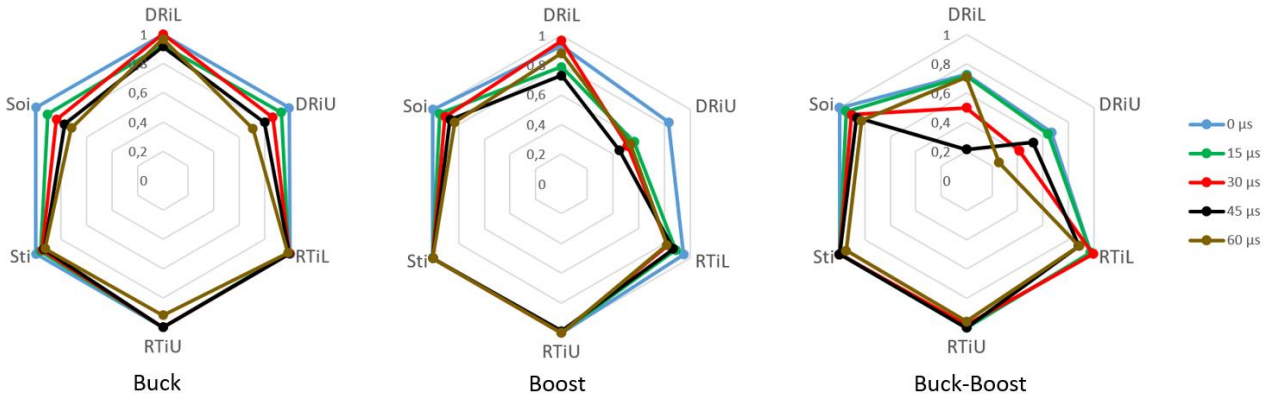


Figure 64: Dynamic Performance indices of DC-DC converters with different values of sampling period

For each converter, each performance index is degrading as the time delay is increased. As explained in section 3.8.1, a delay in the switching action with respect to the time optimal control has more impact on voltage deviation indices than recovery time indices. From figure 64, the delay should not exceed $30\,\mu s$ for the proposed FCS-MPC to exhibit correct dynamic performances.

3.9 Experiment on Synchronous Buck Converter

3.9.1 PCB Layout of the buck converter

The integrated circuit (IC) CSD97396Q4M has been chosen for this experiment because it integrates both the synchronous buck converter and the gate driver. The supply voltage to gate driver and circuitry V_{DD} has been set to 5V while the input voltage pin V_{in} has been set to 15V. It is required for the buck converter to operate in Continuous Conduction Mode (CCM) at any time, therefore the pin $SKIP\#$ is set to 5V. Figure 65 illustrates the schematic of the experimental DC-DC buck converter developed in KiCad. The operating condition of the synchronous buck converter are similar to the CHIL experiment conditions with an output current ranging from 0 to 2A. The input voltage V_{cc} is set to 15V (input voltage pin V_{in}) while the inductance $L = 1\,mH$ and the capacitance $C = 235\,\mu F$. A bootstrap capacitor of $0.1\,\mu F$ is connected between pin BOOT_R and BOOT. This capacitance aims at providing the charges to turn on the Control FET.

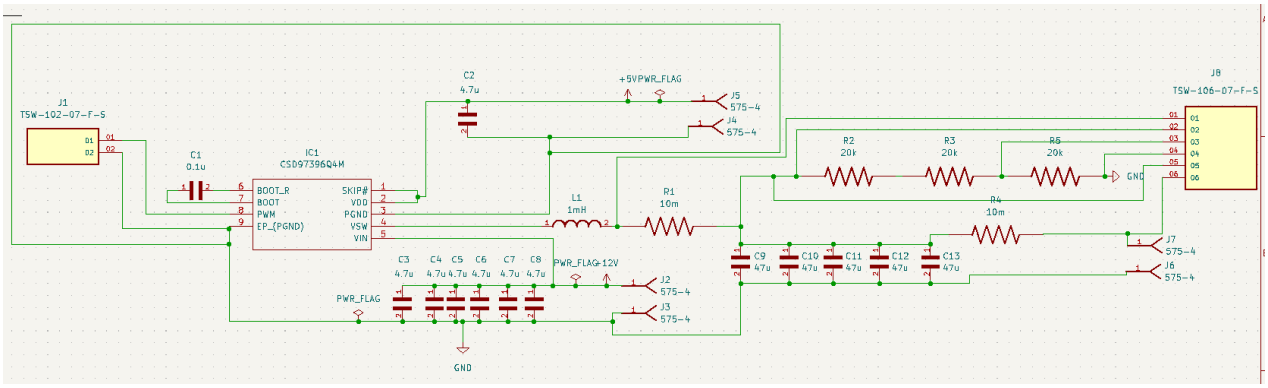


Figure 65: Schematic of the experimental buck converter developed in KiCad

In figure 65, the output capacitance is the summation of five 47 μF capacitance in parallel. The purpose of this design choice is to split the total current among the five capacitances to avoid temperature rises. The inductance L has been chosen to handle up to 3.6 A, a value expected from the CHIL experiment results of the buck converter. A 5 V power supply ($J5$ and $J4$), a 15 V power supply ($J2$ and $J3$) and an external current source ($J7$ and $J6$) are connected with banana plug connectors to the Buck converter PCB. $R1$ and $R4$ are 10 $m\Omega$ shunt resistors used for measurement of inductor current I_L and output current I_o respectively. $R2$, $R3$ and $R5$ are used as a voltage bridge divider to divide the output voltage measurement by 3. Figure 66 represents the bill of materials (BOM) used for the assembly of the board.

Id	Designator	Package	Quantity	Designation
1	L1	INDRD2921W163D3810H2616P	1	1mH
2	C10,C9,C12,C11,C13	CAPC2012X145N	5	47u
3	J8	SAMTEC_TSW-106-07-F-S	1	TSW-106-07-F-S
4	C4,C7,C6,C3,C8,C2,C5	CAPC1608X90N	7	4.7u
5	R2,R3,R5	RESC1608X55N	3	20k
6	J3,J5,J7,J4,J2,J6	KEYSTONE_575-4	6	575-4
7	R4,R1	RESC1608X55N	2	10m
8	IC1	CSD97396Q4M	1	CSD97396Q4M
9	J1	SAMTEC_TSW-102-07-F-S	1	TSW-102-07-F-S
10	C1	CAPC1005X55N	1	0.1u

Figure 66: BOM used for the assembly of buck converter

Figure 67 illustrates the buck converter layout in KiCad while figure 68 shows the buck converter assembled.

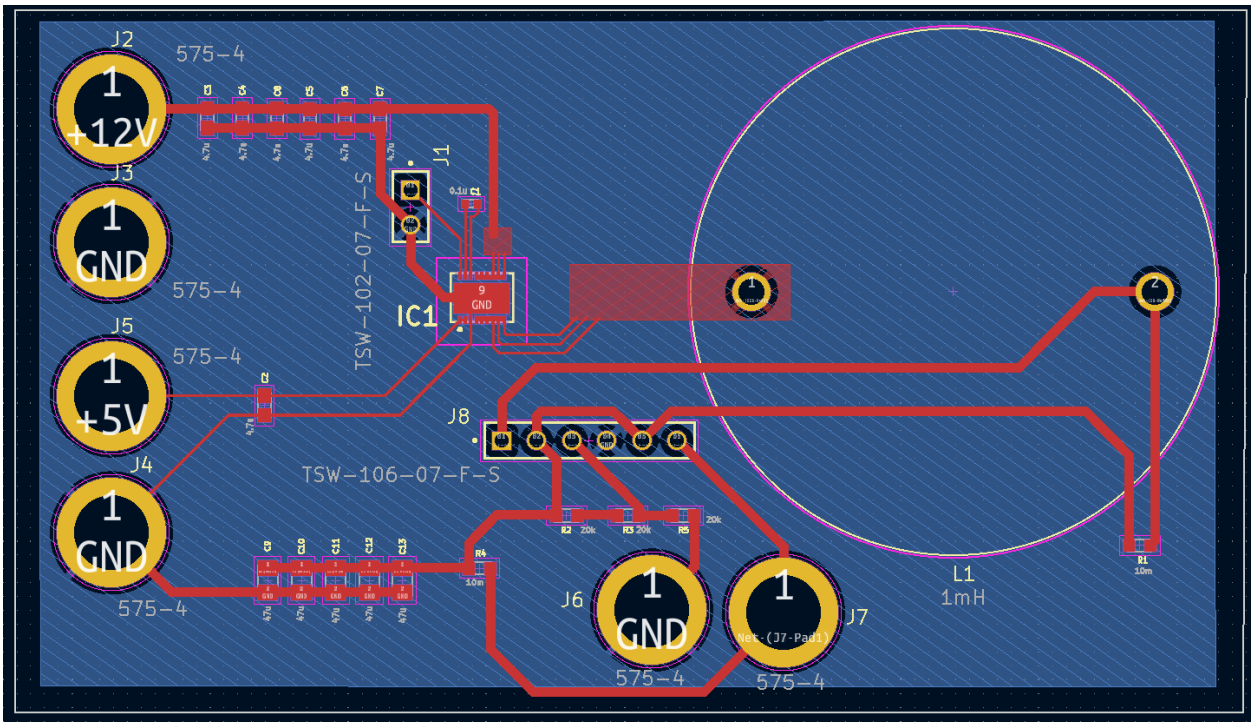


Figure 67: Buck converter Layout in KiCad

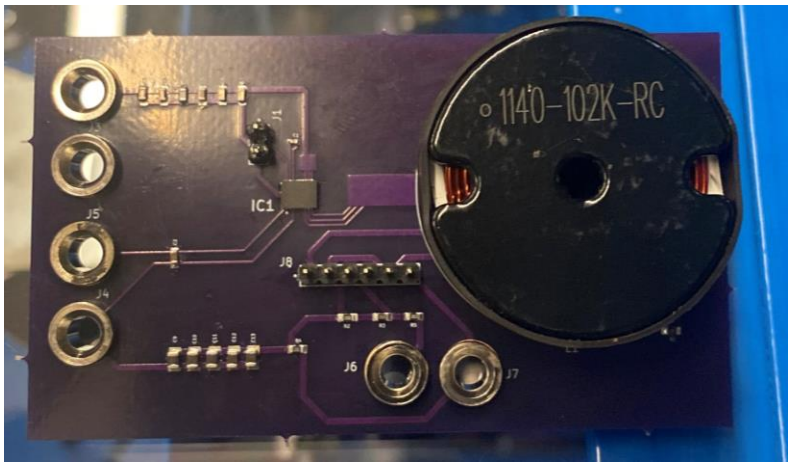


Figure 68: Buck Converter design

3.9.2 I/O Interface of the control card

From the CHIL experiment, a reasonable range for the output voltage is between 0 and $15V$ while an acceptable range for inductor current is between -2.5 and $4\ A$. From the voltage bridge divider in figure 65, the measurement of V_o from the buck converter design should vary from 0 to $5\ V$. The voltage bridge divider in figure 69 multiplies this measurement by 0.6 to obtain a value between 0 and 3V for the control card. The shunt resistor should give a measurement signal varying from $-25\ mV$ to $40\ mV$ and from 0 to $20\ mV$ for the measurement of I_L and I_o respectively. Since the control card only accepts measurement signals between 0 and 3.3V, I_o measurement is amplified by a factor 141. I_L measurement needs to be amplified by a factor 47 and offset by around $1.5\ V$. Figure 69 represents the operational amplifier circuits (LM741CN) that scale and offset the measurement signals.

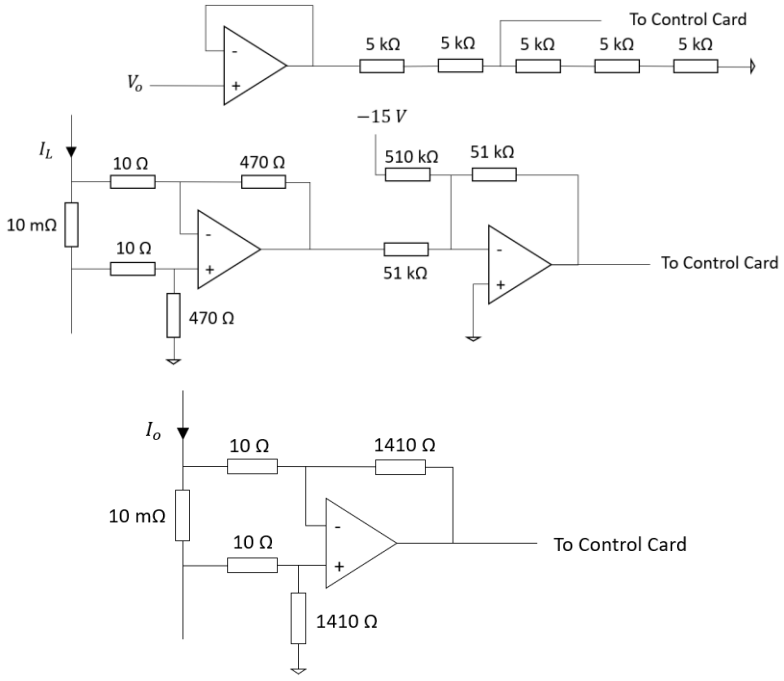


Figure 69: Schematic of the scaling and offset of buck converter measurements

Figure 70 represents the implementation of the measurement amplification and scaling of figure 69.

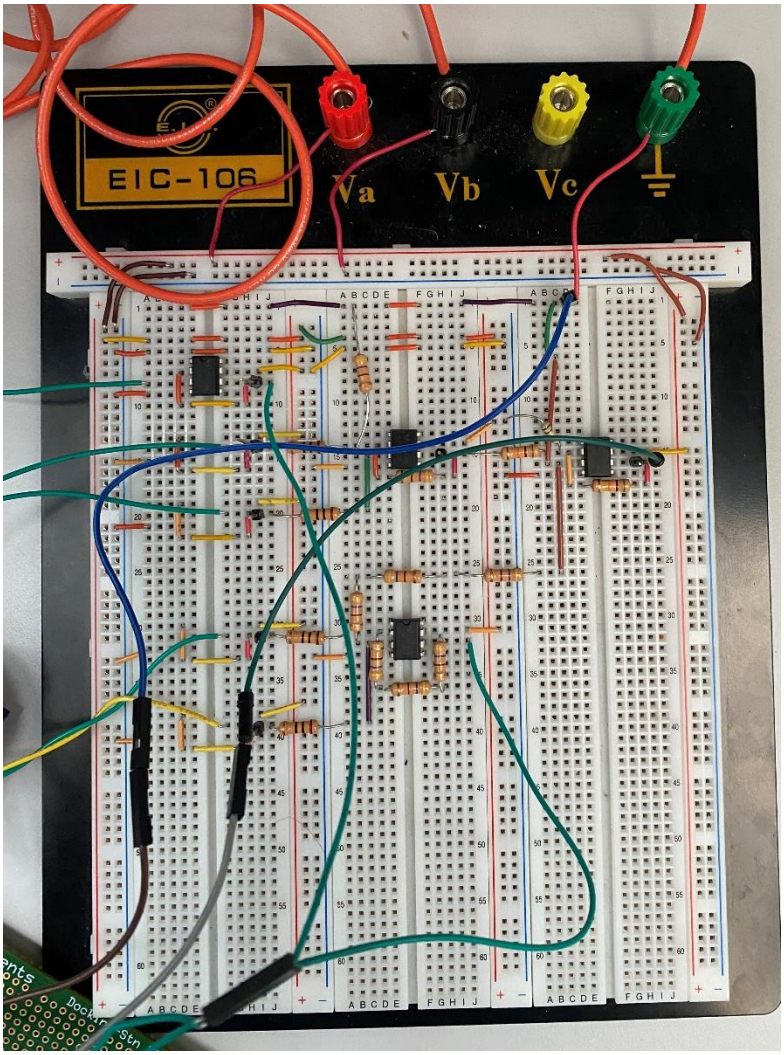


Figure 70:Implementation of measurement scaling and offset

The inputs and outputs of the control card TMDSCNCD28335 are probed using the Docking Station USB-EMU R3 illustrated in figure 71.

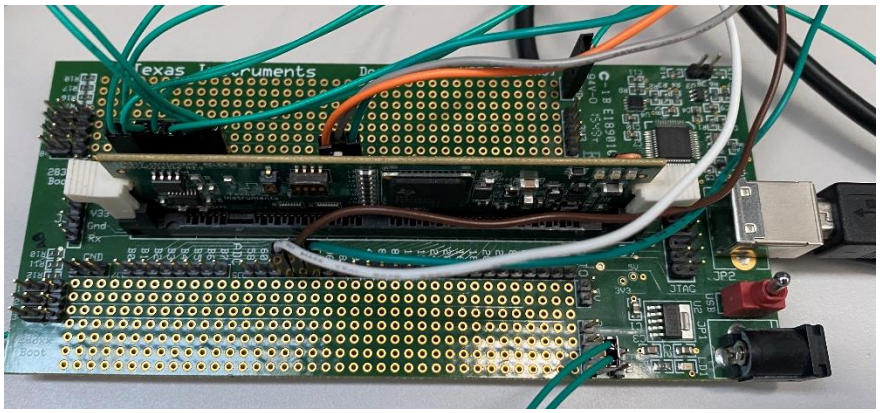


Figure 71: Docking Station USB-EMU R3

3.9.3 Experiment Results

The proposed FCS-MPC implemented for the buck converter design of section 3.9.1 is set with reference voltage $V_r = 7V$, with a target switching frequency of 1 kHz and a sampling period of 100 μs. This implementation is shown in figure 72.

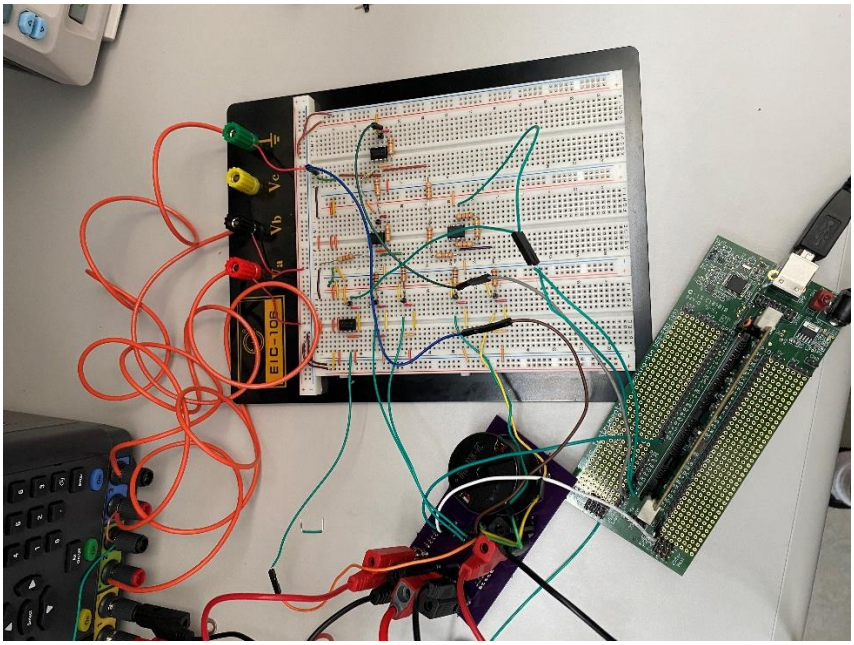
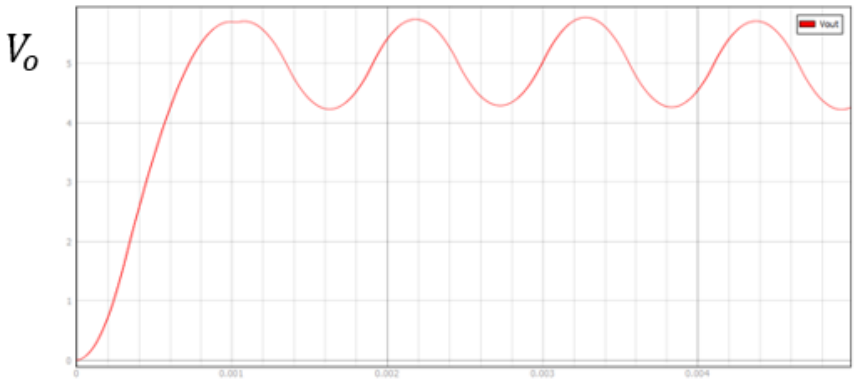


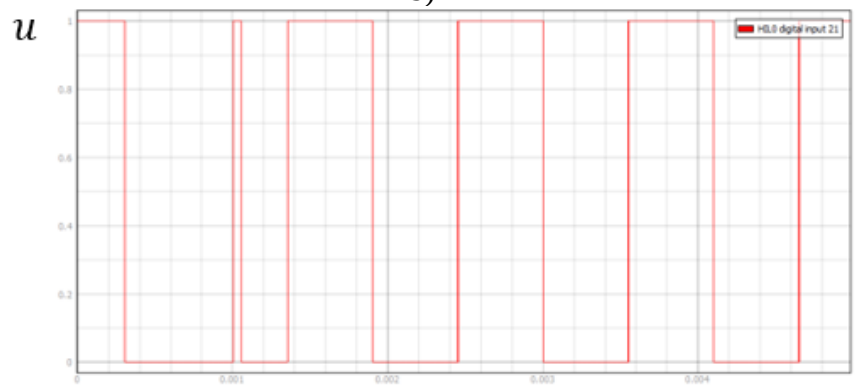
Figure 72: Proposed FCS-MPC of the buck converter

Figure 73a illustrates the output voltage and gating signals from the experimental set up. This result can be compared with results from CHIL experiment of section 3.7.1 that has similar operating conditions and is also found in figure 73b and c

a)



b)



c)

Figure 73: Output voltage and gate signal comparison between hardware (a) and CHIL platform (b and c)

This figure shows that for a start-up transient ($I_o = 0$). When the converter turns on as shown in the green rectangle, the output voltage undergoes an estimated $600\ \mu s$ surge that is too fast for the control card to sample having a sampling rate of $100\ \mu s$. This leaves the control card only 6 samples to capture the surge which is insufficient for the card to operate time optimally.

Between the green and orange rectangle, the converter is set in the OFF state while the initial condition on the inductor current is non-zero. Therefore, the inductor current feeds the capacitor resulting in a rise of capacitor voltage. After risen, the system begins to oscillate once again due to LC interaction but below the reference setpoint.

The proposed control exhibits time optimal behavior at the start of the orange rectangle since the voltage reference is reached in one switching action. We know it is time optimal at this point because it is the earliest point in the ON/OFF sequences for which the output voltage oscillates at a constant switching frequency. This is a similar behavior as the results from figure 45 where the reference voltage is reached in one switching action.

The output voltage manages to reach steady-state oscillating around 8 V. This difference between the reference value and actual steady-state value comes from a larger sampling period with the prototype ($50\ \mu s$ for CHIL and $100\ \mu s$ for the hardware), as explained in section 3.8.4, and the current drawn from the voltage measurement set-up used to condition signals for the controller.

Figure 74 shows the steady-state behavior of the output voltage and gating signals. In this figure, the steady state switching frequency obtained is equal to $1.5\ kHz$ which is significantly different from the target switching frequency of $1\ kHz$. This difference can be explained by the large sampling period that impacts the precision of the proposed FCS-MPC to operate at the

desired switching frequency. As per section 3.7.2 and 3.7.3, a larger sampling period causes a difference between expected and measured switching frequency.

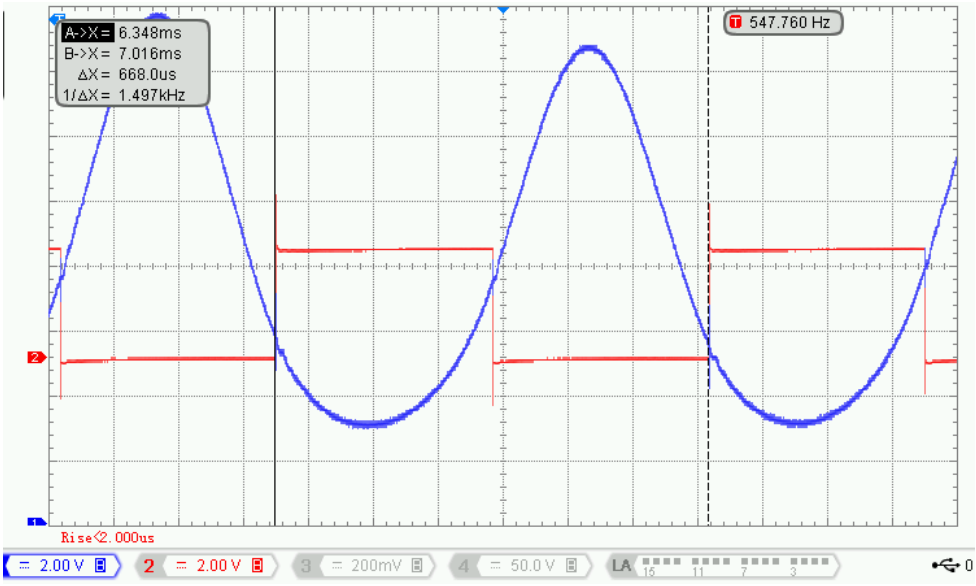


Figure 74: Steady-state behavior of gating signals (red) and Output Voltage (blue)

4.0 Research Task #3-Improvement of Maximum Power Point Tracking(MPPT) and Least Power Point Tracking (LPPT) dynamic performances in DPP architecture using FCS-MPC

4.1 Literature Review and Motivation

4.1.1 Benefits of PV Differential Power Processing

A common usage to exploit the power from PV is to adopt the bulk conversion topology of figure 75, often utilized to reach a higher voltage than the typical value provided by a single PV.

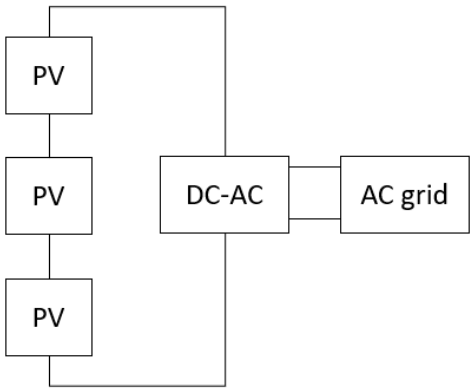


Figure 75: series PV connected with a central inverter

In this configuration panels are connected in series with a central inverter that focuses on finding the operating point for maximum power production from the string of PVs also called Maximum Power point (MPP) [1]. However, due to partial shading [2] or aging [3], each PV module has a different MPP current. Therefore, since the series connection imposes the same

current going through each PV the overall power production of the bulk conversion topology is degraded. To avoid this decrease of performance, each PV panel is connected to an individual converter. In fact, each converter ensures an exact maximum power point tracking (MPPT) of its associated PV module. In literature DC optimizer [4]-[6] in figure 76a or microinverters [7]-[9] in figure 76b are referred as possible solutions to fulfill this role.

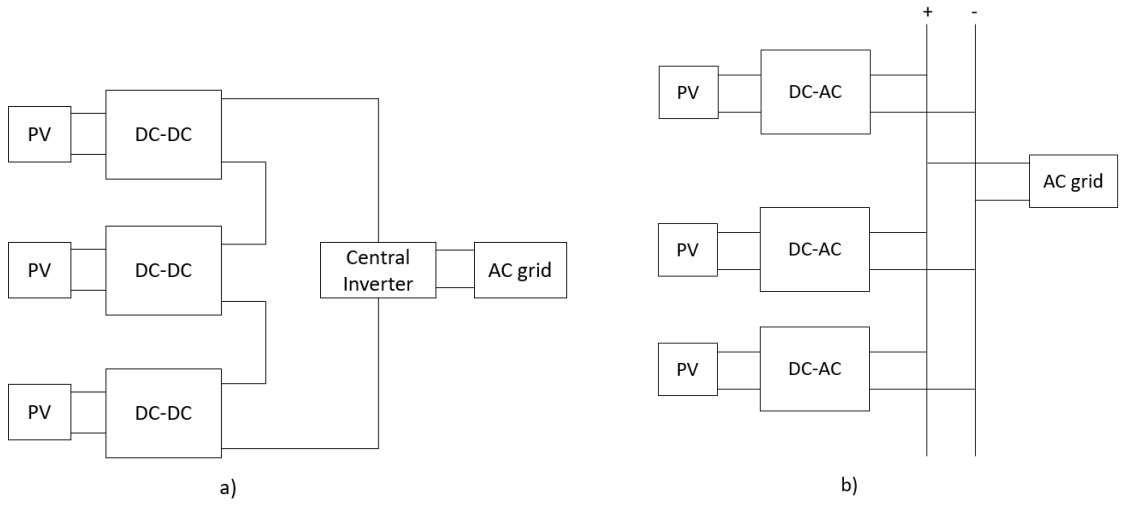


Figure 76:FPP DC optimizers (a) and module integrated inverters (or microinverter)

Because each converter processes the full power rating of an individual PV, these individual converters are often referred as full power processing (FPP) converters. The latter statement coupled with the increased number of conversion stage leads to a decrease in the power conversion efficiency.

Differential power processing (DPP) converters emerged as an improvement of FPP converter keeping each PV at its MPP but processing only the mismatch in power between two adjacent PV. Hence, the power rating of DPP converters is decreased when compared to FPP converters improving reliability and efficiency, reducing cost and size of components [10]-[11].

In literature, a DPP structure is said to be parallel if the DPP converter compensates the mismatch in PV MPP voltage and series if the DPP converter compensates the mismatch in PV MPP current [12].

The general idea of parallel DPP converter represented in figure 77 is to supply the mismatch between a common bus voltage and the MPP voltage for each PV panel. All PV modules are connected in parallel with a central converter interfacing the grid voltage. Direct Connection parallel DPP [13] and parallel DPP with a front-end converter [13]-[14] are the two existing families of parallel DPP.

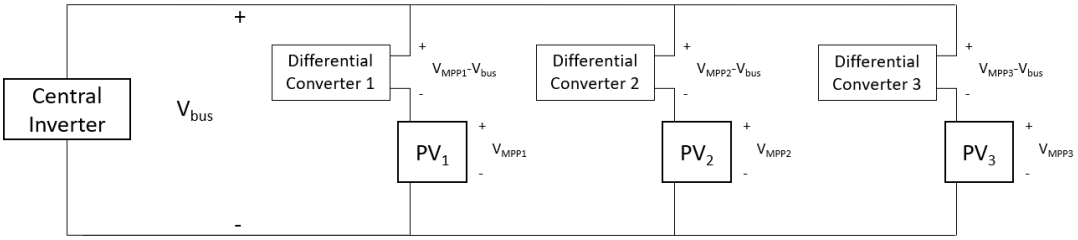


Figure 77: Conceptual idea of Parallel DPP architecture

The conceptual idea of series DPP architecture in figure 78 is to implement differential converters supplying the difference in MPP current between two adjacent PV modules.

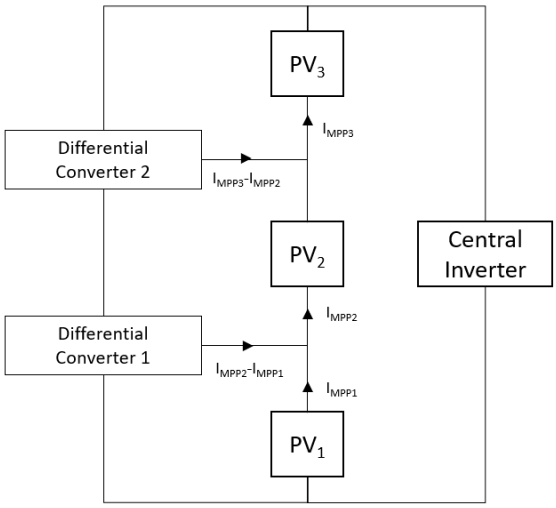


Figure 78: Conceptual idea of series DPP architectures

This structure is the direct improvement of the FPP mentioned earlier because it deals with PV modules connected in series. Since series architecture is more referenced than the parallel architecture, there is more room for comparison between classical control and Model Predictive Control of series DPP architecture than parallel architectures.

4.1.2 Comparison of series DPP architectures

4.1.2.1 Series PV-PV DPP

Series PV-PV DPP architecture illustrated in figure 79 regroups structures where the input and output connection of differential converters are PV modules.

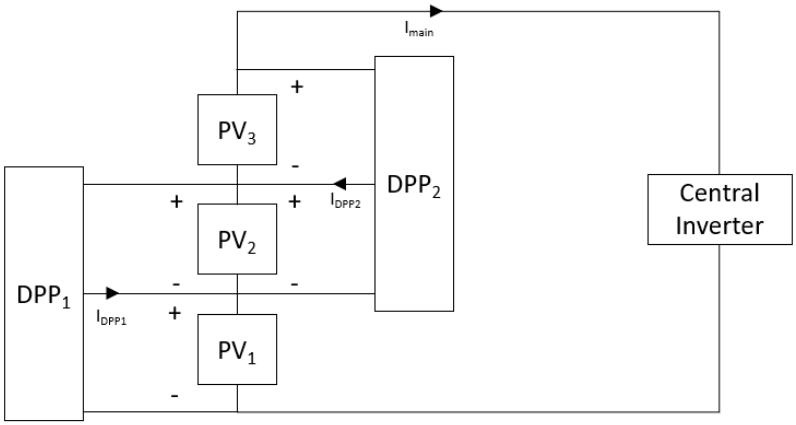


Figure 79: Series PV-PV DPP architecture

For this structure, a string of n PV panels requires n-1 differential converters where one converter maintains one PV element at its MPP, and the central converter control realizes the MPPT of the entire PV string. Therefore, since the target operating point of the entire system is unique, the remaining PV panel MPP is also maintained when the MPP of the n-1 PV panels and the MPP of the entire PV string is reached [1], [12]. There is only one value of string current I_{main} for the maximum power production of the entire PV string. One of the most used topologies for PV-PV architecture is the switched inductor topology used in [1], [11], [15]-[17] where the voltage applied to the inductor is one of the adjacent PV voltage. Another topology used for PV-PV architecture is resonant switched capacitor topology in [18], [19] where zero voltage switching can be implemented.

One main advantage of PV-to-PV architecture is the low voltage rating of the differential converters since they are rated for PV voltage values. On the other hand, PV-PV architecture is a highly coupled system since the expression of differential current between two adjacent PVs might involve the control action of two differential converters [1], [12].

4.1.2.2 Series PV-bus and PV-bus direct architecture

Figure 80 shows the typical structure of Series PV-bus DPP architecture where one connection of the differential converter is a PV panel and the other is the common voltage bus that inputs the central inverter.

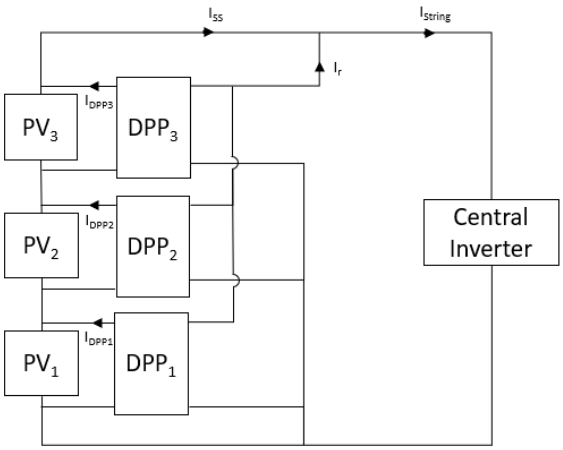


Figure 80: Series PV-bus DPP architecture

In this system, a string composed of n PV elements require n differential converters. For appropriate operation, the differential converter should be an isolated topology like the flyback converter [20]. In fact, boost topology is mentioned as a potential solution for PV-bus architecture in [1] but is not considered as a true DPP converter in [12] since the low side switch of boost converter is connected to the ground. Hence, when the low side switch is ON, the voltage applied to the inductor is the sum of all PV voltages below the converter. Other specific solutions exist in literature such as the stacked LLC resonant converter in [21] and a multi-stacked SEPIC converter in [22]. However, [21] and [22] are implementing a voltage balancing of PV elements to extract the maximum power from the PV elements which is not considered as an exact MPPT. Contrary to the series PV-PV DPP architecture, each PV panel has its MPPT

made by a differential converter, meaning that I_{string} is an extra degree of freedom available for another purpose. In [1] and [22], it has been demonstrated that there exists one unique value of I_{string} that minimizes the power losses through the differential converters and that MPPT is reached for each individual PV element for any string current. Nevertheless, DPP converters needs to allow bidirectional power flow to reach minimum power losses which is not the case of the topologies mentioned earlier [20]-[22]. One challenge in controlling the string current for power losses minimization lies in its dependency on the return current I_r from the DPP converters. To decouple the substring current I_{ss}, directly tied to the power losses through differential converters, from the string current controller by the inverter, an alternate version of PV-bus architecture called direct PV-bus architecture is illustrated in figure 81.

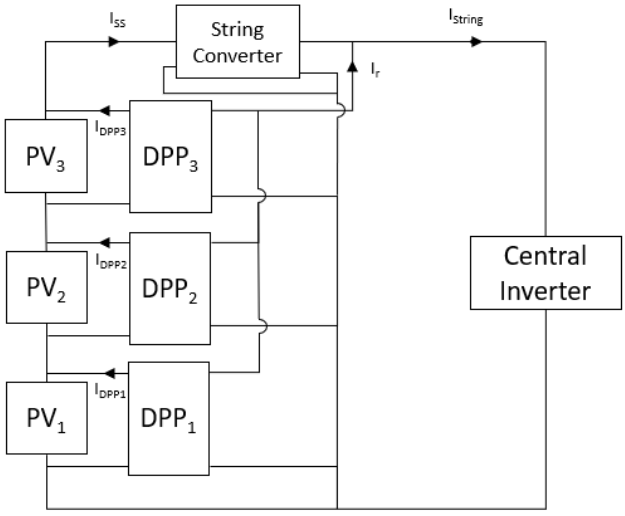


Figure 81: Series PV-bus direct DPP architecture

In this structure, the string converter control scheme aims at controlling the substring current to minimize the power losses through each DPP converter. In the literature, this architecture is implemented with a boost topology as a string converter implementing a least power point

tracking (LPPT) [23] and a unit LPPT [24]. While the first control scheme focuses on minimizing the total power processed by DPP converters, the second mitigates the worst case power processed by any DPP converter.

4.1.2.3 Serie PV-Isolated Port architecture

Figure 82 presents the serie PV-Isolated Port (IP) DPP or PV to Virtual Bus where each differential converter is connected to a PV element and an independent isolated bus.

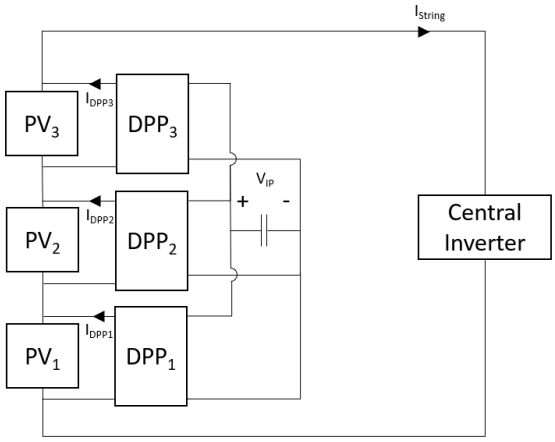


Figure 82: Series PV-IP DPP architecture

This structure is similar to the previous series PV-bus DPP architecture involving n differential converters for a string of n PV panels. However, each differential converter is connected to a separate voltage bus. Since the PV elements are exchanging power with a separate voltage bus, this voltage can be potentially smaller than for PV-bus structure allowing for a smaller voltage rating of components and cost reduction. On the other hand, this isolated port requires a net exchange of power with PV elements equal to zero to have a stable voltage. This constraint implies that exact MPPT for each PV panel might not be achievable for any string current which

is a downside for this architecture. In literature, only isolated topologies such as bidirectional flyback converter is used for this architecture

4.1.2.4 Discussion on the choice of serie DPP architecture

DPP structure in general is a good candidate to apply MPC framework since the overall system is multivariable. Moreover, DPP converters are switched non-linear systems which can be easily apprehend by MPC. Finally, numerous algorithms applying MPC for MPPT can be found in literature.

Among all the series DPP structure, the PV-bus direct architecture is the most promising to apply the Model Predictive Control. In fact, contrary to the PV-PV architecture, MPPT of each individual PV element can be reach for a wide range of string current values. The control of this system has a multiobjective nature since the MPP of each PV panel can be reached with a specific string current value that minimizes power losses on DPP converters. For PV-IP architecture, the constraint on the net power exchange between the isolated port and the PV elements adds an extra level of complexity when compared to PV-bus direct architecture. The PV-IP architecture would surely benefit from a control scheme developed around the MPC framework and should be considered in a future work.

4.1.3 Contributions

Figure 83 illustrates the PV differential power processing system under study, composed of two DPP converters using the bidirectional flyback topology and a boost converter controlling the current through the PV string.

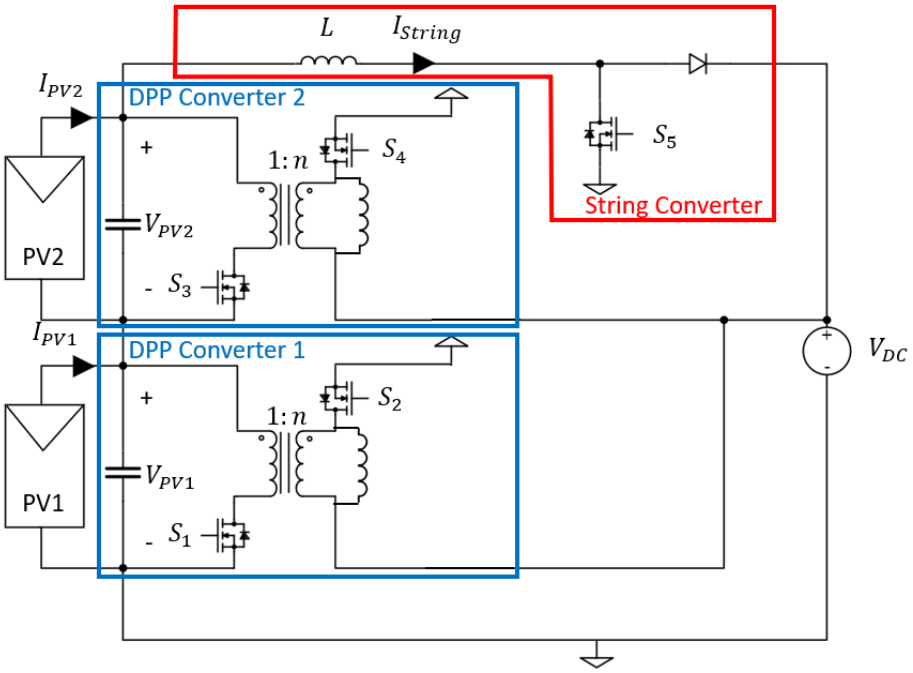


Figure 83: Detailed Schematic of the DPP PV-bus direct architecture under study

Each DPP converter connects a PV element and the input of the central inverter (modeled as a DC voltage in the far right) with a converter controlling the current through the PV string. A control approach is proposed in [23] where each DPP converter is controlled to achieve MPPT for each PV element while the boost converter is controlled to achieve LPPT minimizing the total power stress on DPP converters. However, for both MPPT and LPPT to work simultaneously, it is required to implement different time scales otherwise the MPPT algorithm perturbs the LPPT algorithm and vice versa. In this work, the classical LPPT is replaced by a one-step FCS-MPC with a similar control objective to solve this issue. The MPPT algorithm of [23] is also replaced by a one-step FCS-MPC. The key contribution of this work is the absence of time-scale constraints of each algorithm since few interactions are expected between the two FCS-MPC. Additional improvement related to FCS-MPC schemes are significant dynamic performance improvement [25] and the absence of PI controller tuning requirements [26]-[27].

The first part of this paper reviews the classical control schemes for the DPP architecture and explains how the MPPT can disturb the LPPT convergence. The second part of this paper explains the design of the FCS-MPC MPPT for bidirectional flyback converters while the third part explains the design of a one-step FCS-MPC for the boost converter aiming to minimize the power stress on the DPP converters. In the third part, the results of a PLECS simulation model are presented to validate both control schemes and that they can work simultaneously with identical time scales.

4.2 Classical Control of the DPP system

4.2.1 DPP achieving MPPT

Each DPP converter is controlled applying the Perturb and Observe (P&O) Algorithm of figure 84 to find the maximum power point (MPP) of its associated PV panel [11]. Each DPP converter illustrated in figure. 83 is a bidirectional flyback converter and has its output voltage directly controlled using pulse width modulation. In the case of the bidirectional flyback converter working in CCM, the output voltage V_{PV} in (4-1) increases as the duty cycle d increases.

$$V_{PV} = \frac{nV_{DC}d}{(1-d)} \tag{4-1}$$

At each sampling of PV voltage $V_{PV}(k)$ and current $I_{PV}(k)$, the P&O algorithm directly updates the duty cycle to reach the MPP. Therefore, the classical control implemented for the DPP converters is called direct duty cycle control MPPT. If the perturbation of voltage ΔV_{PV}

resulting from the last change of duty cycle $d(k-1)$ induces an increase of power ($\Delta P_{PV}(k) > 0$) then the duty cycle should be modified in the same direction as ΔV_{PV}. If the power is decreased, then the duty cycle should be modified in the opposite direction of ΔV_{PV}. The duty cycle variation Δd is a key design parameter of this algorithm both influencing the MPPT convergence speed and oscillation amplitude around MPP voltage. A large Δd offers a faster convergence but large oscillations around the MPP voltage while a small Δd means smaller oscillations but with a slower convergence. The relation between voltage oscillation and duty cycle variation is given in (4-2).

$$\Delta V_{PV} = \frac{nV_{DC}}{(1-d)^2}\Delta d \tag{4-2}$$

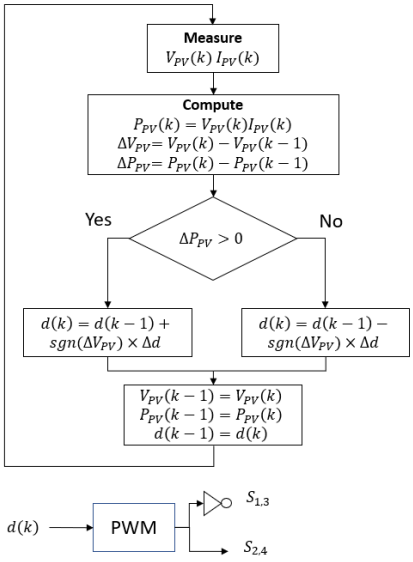


Figure 84:Direct Duty Cycle Control Maximum Power Point Tracking (MPPT) using Perturb and Observe (P&O)

4.2.2 String Converter achieving LPPT

Since each DPP converter is associated to one PV panel for MPPT, the MPP of the whole PV string can be tracked for multiple values of string current. In other words, the string current is an extra degree of freedom that can be controlled by the string converter to reduce the power stress on the DPP converters. Equation (4-3) corresponds to the absolute value of total power processed by DPP converters in the system of figure 83.

$$\Sigma|P_{\Delta}| = V_{PV1}\left|I_{PV1} - I_{String}\right| + V_{PV2}\left|I_{PV2} - I_{String}\right| \quad (4\text{-}3)$$

Assuming $I_{PV2} > I_{PV1}$ and $V_{PV2} > V_{PV1}$, three expressions of $\Sigma|P_{\Delta}|$ can be distinguished based on the sign of $I_{PV1} - I_{String}$ and $I_{PV2} - I_{String}$. If $I_{PV1} > I_{String}$,then both terms are positive, and the power processed is given by equation (4-4). If $I_{PV2} > I_{String} > I_{PV1}$, then only $I_{PV2} - I_{String}$ is positive and the power processed is given by equation (4-5). If $I_{String} > I_{PV2}$, then both terms are negative, and the total power processed is given by equation (4-6). Note that both (4-4) and (4-5) are decreasing functions while (4-6) is an increasing function.

$$\Sigma|P_{\Delta}| = V_{PV1}I_{PV1} + V_{PV2}I_{PV2} - (V_{PV1} + V_{PV2})\, I_{String} \quad (4\text{-}4)$$

$$\Sigma|P_{\Delta}| = -V_{PV1}I_{PV1} + V_{PV2}I_{PV2} + (V_{PV1} - V_{PV2})\, I_{String} \quad (4\text{-}5)$$

$$\Sigma|P_{\Delta}| = -V_{PV1}I_{PV1} - V_{PV2}I_{PV2} + (V_{PV1} + V_{PV2})\, I_{String} \quad (4\text{-}6)$$

The black curve of figure 85 illustrates the evolution of power processed with the string current using (4-4), (4-5) and (4-6). It is important to note that this waveform contains a single minimum at $I_{String} = I_{PV2}$ that is tracked using a P&O algorithm which defines the process of Least Power Point Tracking (LPPT) of figure 86. The string current $I_{String}(k)$ is controlled by modifying the reference current $I_{ref}(k)$ used by the PI controller.

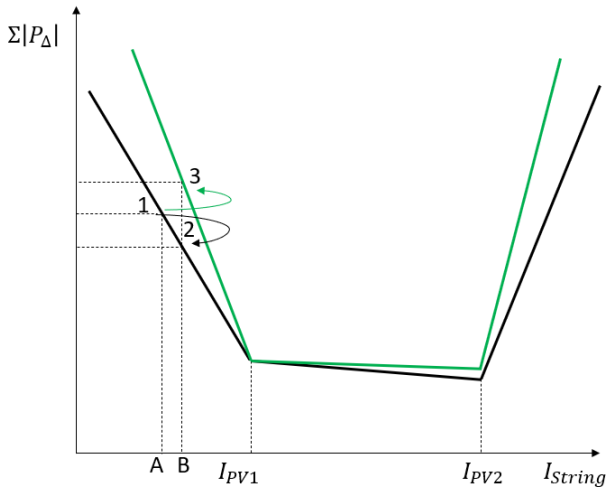


Figure 85: Evolution of Power Processed by DPP converters Waveform when VPV1 is increased

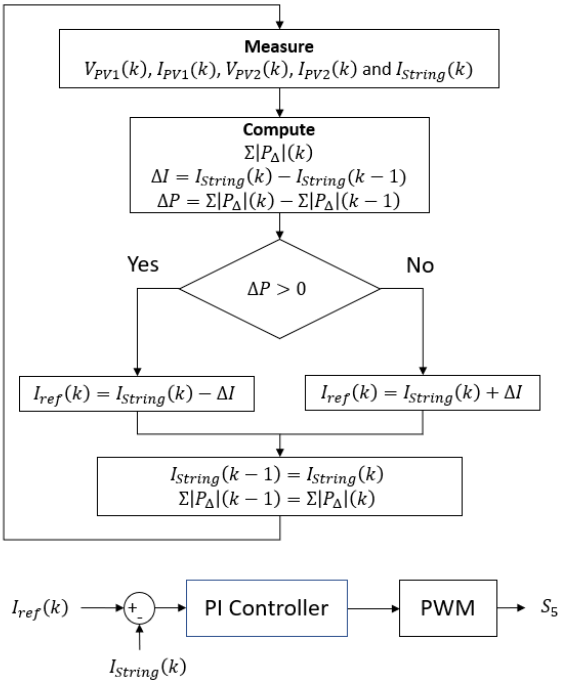


Figure 86: Perturb and Observe (P&O) Least Power Point Tracking (LPPT)

If the perturbation of current ΔI from the last change of reference current $I_{ref}(k-1)$creates an increase in power processed ($\Delta P(k) > 0$) then the string current should be controlled toward the opposite direction of ΔI. The string current should be controlled toward the same direction as ΔI if the power processed is decreased.

4.2.3 Interactions between MPPT and LPPT

As detailed in section 4.2.1, MPPT P&O requires a perturbation ΔV_{PV} to decide on the update of d which modifies the power processed by DPP converters. In figure 85, if only V_{PV1} is increased while I_{PV1}, I_{PV2} and V_{PV1} are constant, the power processed waveform will change from the black curve to the green curve. Let's consider that the algorithm of figure 86 is applied at point B and V_{PV1} is constant between sampling of point A and sampling of point B. The power measured at B is located on the black curve at 2 leading to a negative difference of power (difference between 1 and 2). This forces the algorithm to increase further the string current reference to approach the minimum power processed. However, if V_{PV1} has been increased, the power measured at B is located on the green curve at 3 leading to a positive difference of power (between 1 and 3). This misleads the LPPT of figure 86 into decreasing the current reference while the minimum power at $I_{String} = I_{PV2}$ should be approached by increasing this reference as shown in the green curve of figure 85.

4.3 One Step FCS-MPC MPPT of bidirectional Flyback Converter

The output voltage control of a bidirectional flyback converter exhibits non-minimum phase behavior, disturbing any classical one step FCS-MPC. In the literature, a large signal approach called geometrical domain analysis is adopted to create a boundary controller that avoids the non-minimum phase behavior in the case of the buck-boost converter [10]. Since the bidirectional flyback converter exhibits a similar behavior, the proposed FCS-MPC MPPT also uses the geometrical domain analysis for the design of its cost function. Section 4.3.1. presents the derivation of the internal dynamic model along with the geometrical domain analysis of the flyback converter. Section 4.3.2 presents the cost function design using the geometrical domain analysis from Section 4.3.1. Section 4.3.3 adds the MPPT objective to the framework of Section 4.3.1 and Section 4.3.2 to establish the proposed FCS-MPC MPPT.

4.3.1 Flyback Converter Normalization

The behavior of the bidirectional flyback converter illustrated in figure 87 is described by (4-7) and (4-8) where u=1 when the primary side MOSFET is ON and the secondary side MOSFET is OFF and u=0 when the primary side MOSFET is OFF and the secondary side MOSFET is ON.

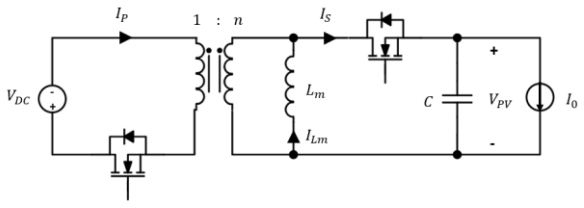


Figure 87: Bidirectional Flyback Converter

$$C\frac{dV_{PV}}{dt} = (1-u)I_{Lm} - I_o \tag{4-7}$$

$$L\frac{dI_{Lm}}{dt} = u(nV_{DC}) - (1-u)V_{PV} \tag{4-8}$$

Equations (4-7) and (4-8) are normalized to obtain (4-9) and (4-10) using the following base values. Note that V_{ref} is the desired output voltage.

$$V_{base} = V_{ref} \qquad T_{base} = 2\pi\sqrt{L_m C}$$

$$Z_{base} = \sqrt{L_m/C} \qquad I_{base} = V_{base}/Z_{base}$$

$$\frac{1}{2\pi}\frac{dV_{PVn}}{dt_n} = (1-u)I_{Lmn} - I_{on} \tag{4-9}$$

$$\frac{1}{2\pi}\frac{dI_{Lmn}}{dt_n} = u(nV_{DCn}) - (1-u)V_{PVn} \tag{4-10}$$

The normalized internal dynamic model, (4-11) and (4-12), is obtained by discretization of (4-9) and (4-10) using the forward Euler discretization and considering a normalized sampling period of T_{sn}.

$$V_{PVn}(k+1) = V_{PVn}(k) + T_{sn}2\pi((1-u)I_{Lmn}(k) - I_{on}(k)) \tag{4-11}$$

$$I_{Lmn}(k+1) = I_{Lmn}(k) + T_{sn}2\pi(u(nV_{DCn}) - (1-u)V_{PVn}(k)) \tag{4-12}$$

The magnetizing current I_{Lm}(k) is computed at each sampling period using the current measured at the primary and secondary with $I_{Lm}(k) = I_S(k) + \frac{I_P(k)}{n}$.The output current of the current source in figure 87 is $I_o(k) = I_{string}(k) - I_{PV}(k)$ for each DPP converter. The geometrical domain analysis consists in studying the converter dynamic in the state plane where

the normalized output voltage $V_{PVn}$is along the x-axis, and the normalized magnetizing current I_{Lmn} is along the y-axis as seen in figure 88.

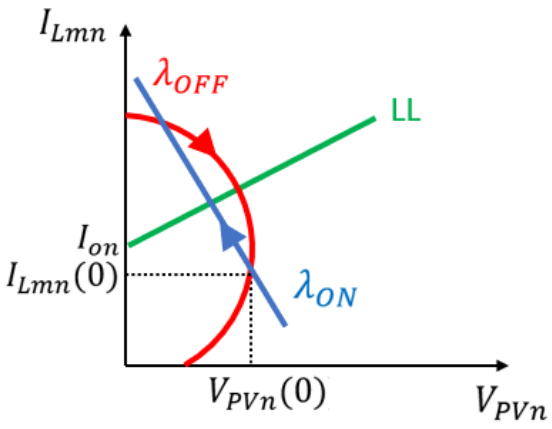


Figure 88: ON and OFF natural switching surfaces of the bidirectional Flyback converter

In this figure, if $I_{Lmn}(0)$ and $V_{PVn}(0)$ are the initial conditions, the converter states evolve along the OFF natural trajectory (red) when *u* is maintained at 0 and along the ON natural trajectory (blue) when *u* is maintained at 1. The OFF natural trajectory and ON natural trajectory equations, listed as (4-13) and (4-14) respectively, are obtained by solving (4-9) and (4-10) to get an expression of $V_{PVn}(t)$ and $I_{Lmn}(t)$ before eliminating the time dependency from this solution [5].

$$\lambda_{OFF}: {V_{PVn}}^2 + (I_{Lmn} - I_{on})^2 = 1 + (I_{Lmn}(0) - I_{on})^2 \tag{4-13}$$

$$\lambda_{ON}: I_{Lmn} = -\frac{nV_{DCn}}{I_{on}}(V_{PVn} - V_{PVn}(0)) + I_{Lmn}(0) \tag{4-14}$$

The OFF natural trajectory expression is the equation of a circle where the center is the DC operating point (V_{ccn}, I_{on}). The radius of this circle is the distance between this circle and the initial condition point. The ON natural trajectory is a line with a slope of $-\frac{nV_{DCn}}{I_{on}}$ passing

through the initial condition point. The load line (LL) in (4-15) defines all the possible equilibrium points of the converter where the tangent of any OFF natural trajectory is equal to the ON natural trajectory.

$$I_{Lmn} = I_{on} + \frac{I_{on}}{nV_{DCn}} V_{PVn} \tag{4-15}$$

4.3.2 Proposed Cost Function for Natural Trajectory Tracking

This work proposes the tracking of specific natural trajectories instead of voltage references, to avoid issues related to non-minimum phase behavior. More specifically the proposed FCS-MPC is designed to track either the ON natural trajectory or the OFF natural trajectory including the target point $(1, I_{Lmnt})$, both illustrated in figure 89, following the position of the converter states in the state plane.

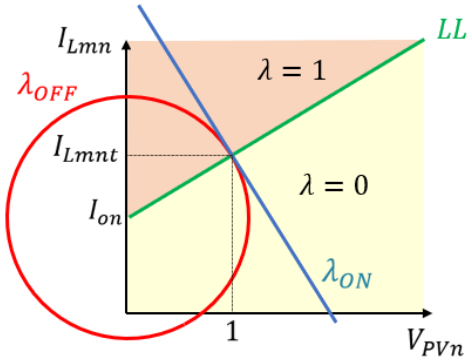


Figure 89:Target ON (blue) and OFF (red) Natural trajectories and lambda mapping in the state-plane for a given V_{ref}

The target point abscissa is equal to 1 since it is normalized by the current reference voltage V_{ref} given by the P&O algorithm. The target point ordinate is located on Load Line given by (4-15)

meaning that $I_{Lmnt} = I_{on}\left(1 + \frac{1}{nV_{DCn}}\right)$. Therefore, the cost function of this FCS-MPC is built with an OFF natural trajectory tracking term in (4-16) and an ON natural trajectory tracking term in (4-17) using the OFF natural trajectory expression of (4-13) and the ON natural trajectory of (4-14), respectively.

$$J_{OFF} = |V_{PVn}(k+1)^2 + (I_{Lmn}(k+1) - I_{on})^2 - (1 + (I_{Lmnt} - I_{on})^2)| \quad (4\text{-}16)$$

$$J_{ON} = \left|\frac{I_{on}}{nV_{DCn}}(I_{Lmn}(k+1) - I_{Lmnt}) + V_{PVn}(k+1) - 1\right| \quad (4\text{-}17)$$

Equation (4-16) compares the radius squared between a set of predicted states and the DC operating point with the radius of the target OFF trajectory. In (4-16), the term $(1 + (I_{Lmnt} - I_{on})^2)$ is the radius squared of the OFF trajectory that includes the target point $(1, I_{Lmnt})$. Equation (4-17) compares the x-intercept of the ON trajectory including the predicted states and the x-intercept of the ON trajectory including the target point. Equations (4-16) and (4-17) are combined using the penalty factor, λ, to express the cost function of the proposed FCS-MPC in (4-18).

$$J = (1 - \lambda)J_{ON} + \lambda J_{OFF} \quad (4\text{-}18)$$

In (4-18) and from figure 89, the OFF trajectory tracking term is active above the load line ($\lambda = 1$) and the ON trajectory tracking term is active on and below the load line ($\lambda = 0$).

4.3.3 Proposed FCS-MPC Maximum Power Point Tracking

Figure 90 illustrates all the steps involved in the proposed FCS-MPC MPPT applied for DPP converters.

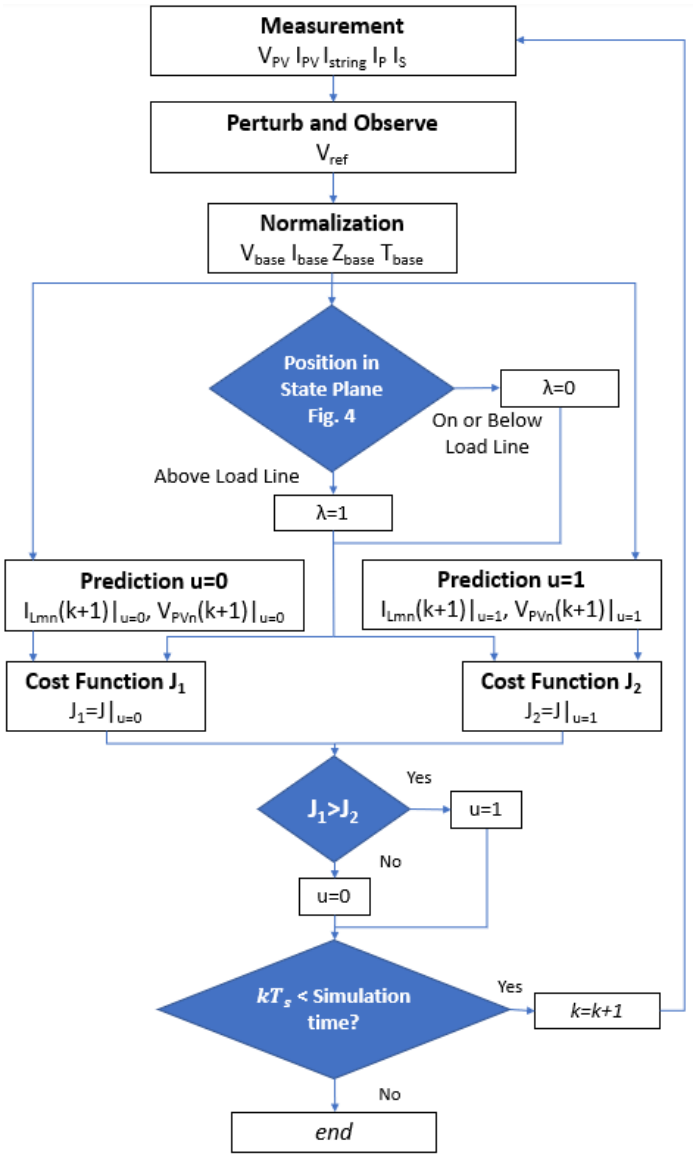


Figure 90: Proposed FCS-MPC MPPT Flowchart

The first step consists in updating the reference voltage with a P&O algorithm. This algorithm is like figure. 84 but the result of the "yes" and "no" path should be replaced by $V_{ref}(k) = V_{PV}(k) + \Delta V$ and by $V_{ref}(k) = V_{PV}(k) - \Delta V$, respectively. With this new reference voltage, the base values are updated for the normalization of the input values. The second step consists of three tasks that can be realized in parallel. The first one consists of locating the

current states with respect to the load line to determine the value of λ. The two other tasks consist of computing the set of predictions for $u = 0$ and $u = 1$ using (4-11) and (4-12). Next, the cost function associated with $u = 0$, J_1 is calculated using the predictions for this switching decision and λ. A similar calculation is realized to obtain the cost function associated with $u = 1$, J_2 using the predictions for this switching decision and λ. Finally, the switching decision leading to the smallest cost function is chosen for the upcoming sampling period.

4.4 One Step FCS-MPC of Boost Converter

The objective of this one step FCS-MPC is to minimize the power stress on each DPP converter by acting on the string current, I_{String}. Thus, the internal dynamic model (4-19) predicts the string current for each switching decision where $u = 0$ when the MOSFET is OFF and $u = 1$ when the MOSFET is ON in figure 83.

$$I_{String}(k+1) = I_{String}(k) + \frac{T_s}{L}\left(V_{PV1}(k) + V_{PV2}(k) - u(nV_{DC})\right) \quad (4\text{-}19)$$

The total power processed by the DPP converters is formulated as the cost function in (4-20) since the objective is to determine which switching decision leads to the minimum power stress on the DPP converters.

$$J_{boost} = V_{PV1}(k)\left|I_{String}(k+1) - I_{PV1}(k)\right| + V_{PV2}(k)\left|I_{String}(k+1) - I_{PV2}(k)\right| \quad (4\text{-}20)$$

Figure 91 illustrates, similarly to figure 90, the steps for the one step FCS-MPC controlling the asynchronous boost converter. In section 4.2.2, it has been established that the classical LPPT is based on P&O algorithm and uses the perturbation ΔI for the control of string current. The proposed FCS-MPC chooses the switching decision with the least power stress on

the differential converters to track this minimum without any measurement of ΔP. Therefore, it can be expected that the algorithm of figure 90 and figure 91 can work simultaneously with the same time scale since ΔP could be disturbed by changes of V_{PV1} and V_{PV2}.

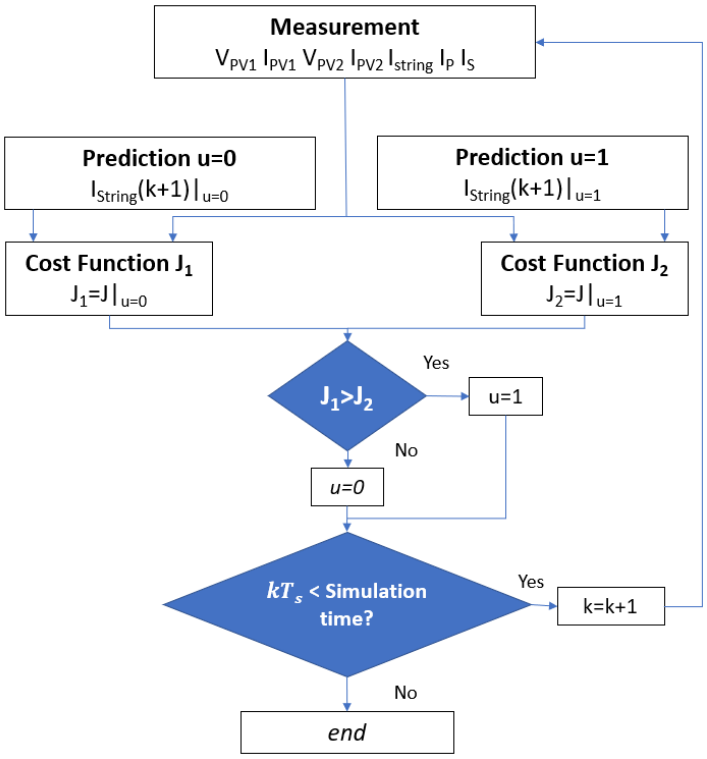


Figure 91: Proposed Boost FCS-MPC Flowchart

4.5 Simulation Results

A simulation model of figure 83, with the parameters used in Table II from [23], has been implemented in PLECS to validate the proposed control schemes and compare them to traditional control of Section 4.2. PV 1 has a theoretical MPP voltage of 26.2 V with a MPP

current of 2.23 A (58.5W), exposed to an irradiance of $1000\ W/m^2$. PV 2 has a theoretical MPP voltage of 27.9 V with a MPP current of 2.96 A (82.5W), exposed to an irradiance of $950\ W/m^2$.

Table 2: Simulation Parameters of DPP Architecture under Study

Parameter	Value
DC link Voltage (V_{DC})	110 V
Magnetizing Inductance (L_m)	100 µH
PV Capacitance (C)	2200 µF
Turns Ratio (n)	0.25
Boost Converter Inductance (L)	550 µH

The classical control schemes of Section 4.2 have been implemented with the following parameters. The sampling rate for MPPT (figure 84) is set to 1.35s while the sampling rate for LPPT (figure 85) is 15 times faster with a period of 0.09s. The proportional gain k_p and integral gain k_i for the boost current control are set to 0.01 and 5, respectively. The voltage perturbation ΔV_{PV} of MPPT is set to 0.5 V, corresponding to a Δd of approximately 0.005 for both PV panels.

The top curve of figure 92 shows the direct duty cycle control MPPT implemented for both PV elements. This figure proves the MPPT is operating properly since PV 1 and PV 2 voltage oscillate around their respective MPP voltage. The bottom curve of figure 92 illustrates the classic PI control LPPT where the string current I_{String}(red) is regulated close to PV 2 current I_{PV2} (blue). The variations of I_{PV2} come from the P&O of the MPPT that changes the operating point of PV 2. This figure proves that the classical control minimizes the power processed by DPP converters since, from Section II, $I_{String} = I_{PV2}$ is the theoretical condition

where the total power processed is minimized when $I_{PV2} > I_{PV1}$ and $V_{PV2} > V_{PV1}$. Note for the top curve of figure 92, $V_{PV2} > V_{PV1}$ is always verified.

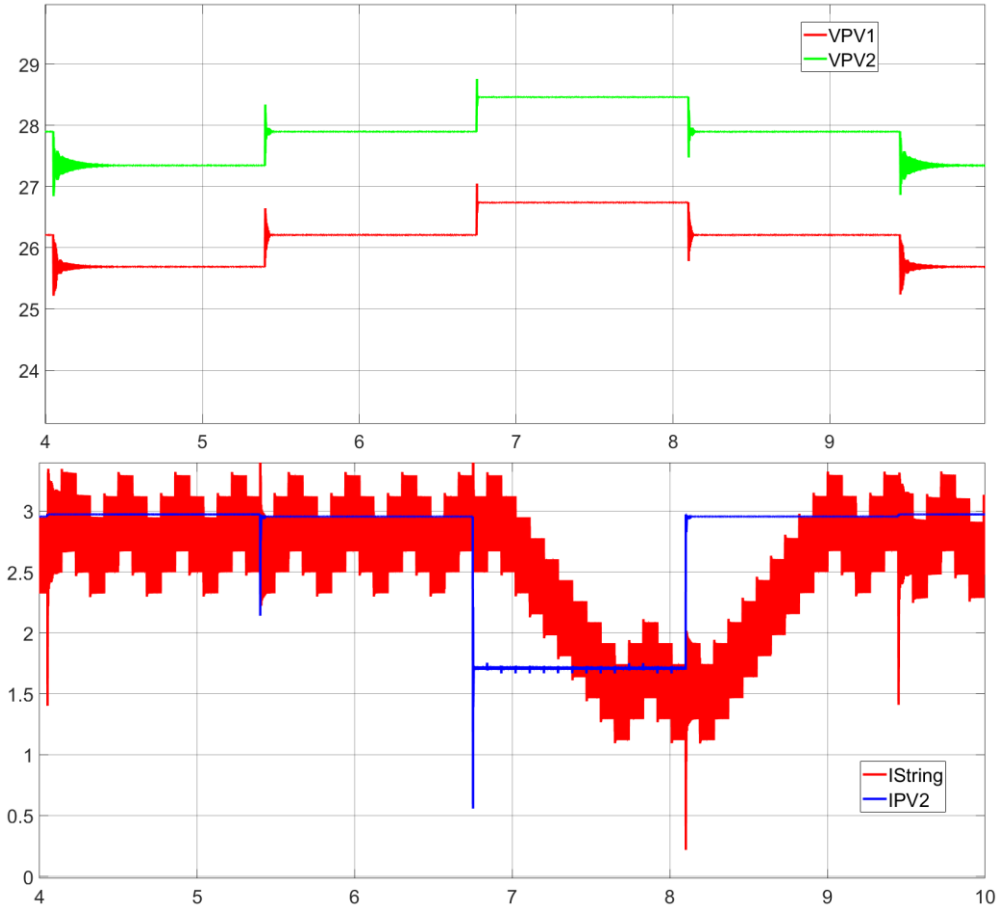


Figure 92: Steady State Operation of Classical MPPT (top) and LPPT (bottom)

The proposed control FCS-MPC MPPT from Section 4.3 and boost converter FCS-MPC from Section 4.4 are both implemented with the same sampling period of $2.5\mu s$. In other words, the MPPT and power stress minimization algorithm are operating at the same sampling rate contrary to the classical control schemes of Section 4.2. The variation of voltage ΔV of the FCS-MPC MPPT P&O is set to 0.5V for each DPP converter.

The top curve of figure 93 shows that the proposed FCS-MPC MPPT is operating like the classical MPPT control scheme of figure 84 since PV 1 and PV 2 voltage are oscillating around their MPP voltages.

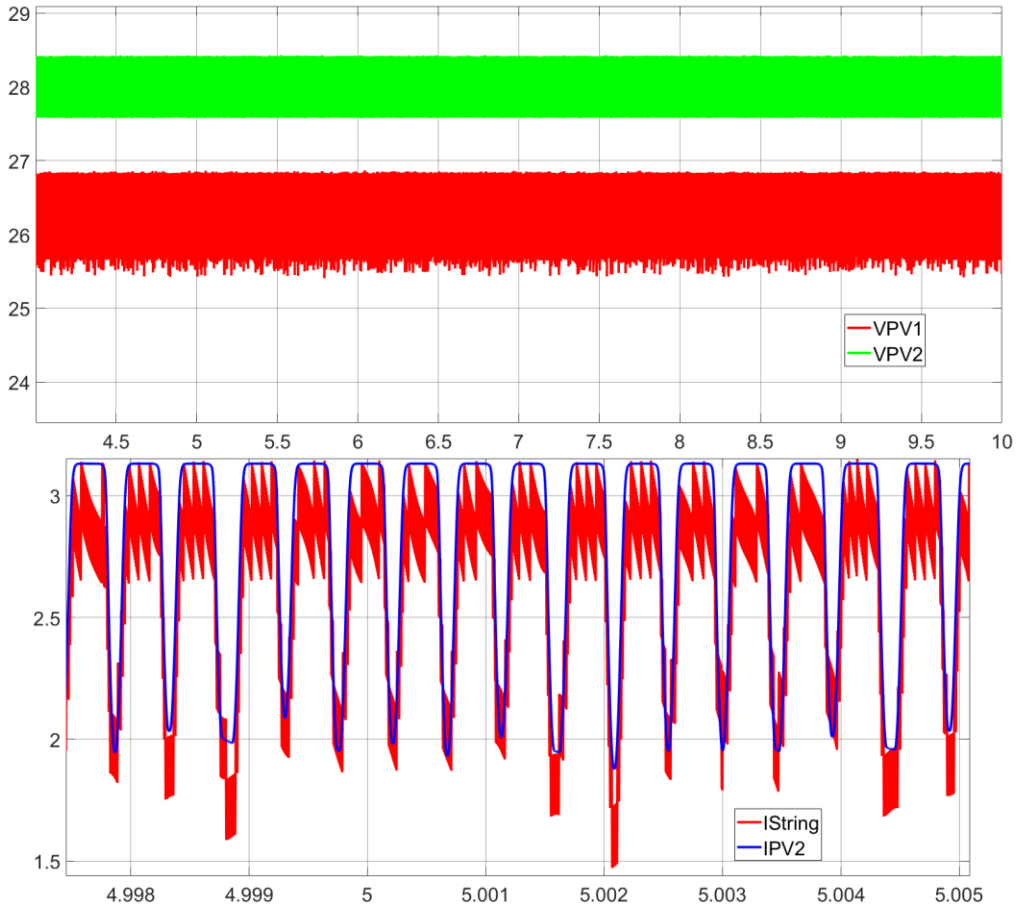


Figure 93: Steady State Operation of proposed FCS-MPC MPPT (top) and boost converter FCS-MPC (bottom).

However, both PV voltages oscillate at a much higher frequency since the proposed FCS-MPC MPPT uses a shorter sampling period meaning a faster update of V_{ref} (P&O from FCS-MPC MPPT) than the update of the duty cycle d (P&O from direct duty cycle control MPPT).

The bottom curve of figure 93 illustrates the proposed FCS-MPC (figure 91) regulating I_{String}. Like in the bottom curve of figure 92, this figure proves that the proposed FCS-MPC minimizes the power processed by DPP converters since I_{String}(red) is also regulated close to I_{PV2}(blue). However, with the proposed FCS-MPC, I_{String} follows more closely variations of I_{PV2} than the classical control scheme meaning an improved dynamic performance in string current regulation.

At this point, one can conclude that the proposed FCS-MPC MPPT (top curve of figure 93) and boost converter FCS-MPC (bottom curve of figure 93) can operate with the same time scale.

The goal of figure 94 is to observe the benefit of an improved string current regulation on the power processed minimization.

The top curve of figure 94 illustrates the measured (blue) and theoretical minimum (red) total power processed when the classical set of control schemes is implemented. At time t=6.75s and 8.1s, it can be observed that the measured power processed is the furthest away from the theoretical minimum. Those times coincides with duty cycle updates from P&O and transient periods where I_{String} has not yet converged to I_{PV2} (bottom curve of figure 92). The middle curve of figure 94 illustrates the measured (blue) and theoretical minimum (red) power processed by DPP converters when the proposed set of control schemes is applied. In that case, it can be observed that the measured power follows closely the minimum value even if the PV 2 operating point is being changed by the P&O of the FCS-MPC MPPT. The bottom curve of figure 94 is a zoomed-in region of the middle curve of figure 94 to show how closely the measured power follows the minimum power.

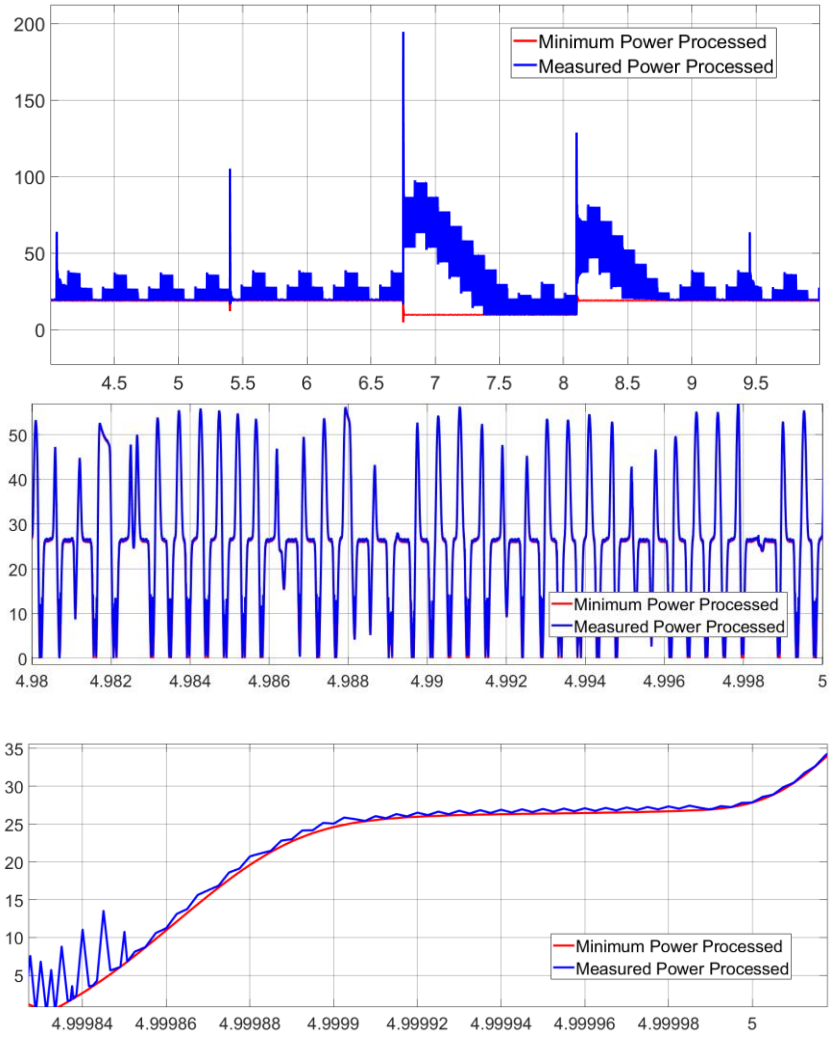


Figure 94: Comparison of Measured and Minimum Processed Power by DPP converters using classical control schemes (top) and control schemes (middle) (zoomed-in (bottom))

Comparing the result of the classical PI control LPPT (top curve) and the proposed FCS-MPC (middle and bottom curve), it can be concluded that the decrease in I_{PV2} transient period leads to a better minimization of the total power processed. Therefore, it can be concluded that the proposed set of control schemes offers a better minimization of power stress than the classical control schemes.

5.0 Conclusion and Future Work

First, a One-step FCS-MPC for DC-DC boost converter tracking specific NSS including the target point while ensuring a stable MTC has been proposed. The addition of the voltage deviation constraint increases the recovery time but offers the possibility to adjust a trade-off between time optimality and voltage deviation in a straightforward manner. Then, thanks to a unified model of non-isolated DC-DC converters, geometrical domain analysis concepts can be applied for buck, boost and buck-boost converters. The proposed One step FCS-MPC ensures a time optimal regulation, with the possibility to limit voltage and current deviation while targeting a specific steady-state switching frequency. The proposed control scheme is validated through simulation and Control Hardware In The Loop experiment using the Typhoon HIL box. Finally, the proposed control scheme is used to control series PV-bus direct DPP architecture. This control scheme is associated with a classical FCS-MPC that minimizes the power processed by DPP converters. This set of FCS-MPC offers a better minimization of power stress than classical control set found in literature. A potential extension of this work would be to apply the proposed FCS-MPC to series DPP PV-IP architecture where the goal is to regulate the Isolated Port Capacitor voltage at a constant value.

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