Design and TID Testing of COTS-Based, Two-Phase, Point-of-Load Converters Using GaN HEMTs for Aerospace Applications

by

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B.S. Electrical Engineering, University of Pittsburgh, 2020

Submitted to the Graduate Faculty of

the Swanson School of Engineering in partial fulfillment

of the requirements for the degree of

Master of Science

University of Pittsburgh

2023

UNIVERSITY OF PITTSBURGH

SWANSON SCHOOL OF ENGINEERING

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Design and TID Testing of COTS-Based, Two-Phase, Point-of-Load Converters Using GaN HEMTs for Aerospace Applications

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The use of commercial off-the-shelf (COTS) parts in space applications has elicited increased interest, especially in the pursuit of higher-performance satellite hardware for missions that can accept higher risk. This hardware includes DC-DC point-of-load (PoL) converters; this category of power electronics performs the critical function of adjusting the voltage and current levels provided by a mission's power distribution infrastructure in order to appropriately feed its loads, which are often computational in nature. The COTS-equivalent parts available for PoL converters enable significantly higher efficiencies, increased current output, reduced volume and mass, improved EMI characteristics, and lower costs. Additionally, the growing availability of COTS switching devices based in gallium nitride (GaN), which is a wide bandgap semiconductor, offers fast switching with reliable radiation performance in a small physical footprint, among other advantages. To effectively integrate potential COTS components into aerospace designs that feature high-power processors, FPGAs, and memories as loads, it is necessary to ascertain the total ionizing dose (TID) tolerance of the COTS control circuitry and power switches. As a result, multiple high-power-density, two-phase synchronous buck converters were developed utilizing various COTS control chips and GaN high electron mobility transistors (HEMTs). GaN devices were used due to their resistance to TID, with several devices having been tested up to 1Mrad. Additionally, multiphase buck converters are a favorite for generating high current power rails that are needed for computational loads like FPGAs. A variety of silicon-based COTS controllers and GaN HEMTs were selected as candidates for future mission applications based on current and voltage ratings.

A comparison between the designed PoL modules is presented with both simulation and hardware results. To see how the controllers perform in a radiation environment, the various modules were stressed up to 10krad through enhanced low dose rate sensitivity (ELDRS)

testing and up to 100krad at a high dose rate. Converters were tested and measured against their baseline performance after each application of radiation. The converter modules' electrical design and characteristics before, throughout, and after radiation testing, as well as comparisons between simulation and hardware performance and measured efficiency data, are presented.

Keywords: point-of-load converters, multiphase converters, aerospace power electronics, TID, COTS, GaN.

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Preface

I would like to start by thanking my advisor, Dr. Brandon Grainger, for his support and guidance throughout the ups and downs of my studies and my research as I pursued the Master's degree. I would also like to thank Thomas Cook, Jeffrey Boye, and Joseph Kozak for sharing their knowledge about the topics in this work and providing resources and assistance (and snacks) when needed. Thank you as well to Chi Pham, Sarah Katz, and Natnael Ahmed for their technical support of the radiation side of this research effort.

I would like to acknowledge my professors and mentors from my undergraduate years, my graduate studies, and internships and co-ops. I appreciate your help and insight as I learn, grow, and develop as a person and as an engineer.

Thank you to my family and friends, including my peers in the Electric Power Technologies Lab - thank you for your love and encouragement, for reminding me that I am capable, and for grand adventures, big and small. My parents especially have been hugely important in my journey through life and school; where I am now is in large part because of your love and support.

This research was ignited and funded by the Johns Hopkins Applied Physics Laboratory (JHUAPL) Independent Research and Development (IRAD) grant, with support from the industry and government members of the NSF Center for Space, High-Performance, and Resilient Computing (SHREC) and the NSF IUCRC Program under Grant No. CNS-1738783.

1.0 Introduction

A continuing trend in electronics is developing physically smaller and more power-dense circuits, while maintaining or improving efficiency and reliability. This trend is relevant across the realm of electronics applications, but it is especially pertinent in power electronics for space missions, where power conversion can occupy a significant Size, Weight, and Power (SWaP) footprint. Space electronics generally encounter harsh temperature and radiation environments, which consequently means that, for performance and protection, radiation-hardened components tend to be bulky, costly, and of sub-optimal performance. Yet, space missions are striving for greater functionality in the same or smaller packaging, heralding a push for higher power density. At the same time, wide bandgap semiconductor devices, such as gallium nitride (GaN) transistors, are receiving more attention for their power-dense footprints packed with performance advantages over silicon metal oxide semiconductor field effect transistors (MOSFETs), such as immensely better radiation tolerance [18, 33].

1.1 The Space Environment and Radiation

There are three main types of radiation effects that semiconductor devices experience in space: single event effects (SEEs) which are primarily due to cosmic rays or protons, displacement damage (also known as total non-ionizing dose (TNID)) which is primarily due to neutrons and/or protons, and total ionizing dose (TID) which is primarily due to energetic electrons and protons (with the exact contributions dependent on the specific orbit) [21, 33]. TID is the ionizing radiation dose absorbed by a sample, defined as energy absorbed per unit mass, so the same radiation exposure can result in different doses for different materials. Anywhere this paper refers to a TID in rad, the units are actually rad(Si), or the dose in rad absorbed by silicon. This absorbed dose results in the production of electron-hole pairs within the material, and while some recombine, diffuse, or drift out of the device, some holes become trapped and ultimately result in device failure, usually through cumulative

parametric shifts that eventually lead to tolerance violations and functional deterioration [21]. Unbiased complementary metal oxide semiconductor (CMOS) devices in a radiation environment are generally capable of enduring greater TID levels compared with devices that are biased during irradiation, but the opposite is true for bipolar devices [21].

To combat the myriad of problems introduced by radiation, electronics for space are designed or manufactured to be radiation-hardened, or radiation-tolerant, meaning that they are qualified to remain within specifications up to certain stated radiation levels. Unfortunately, a radiation-hardened component can cost hundreds to thousands of dollars and, with the added design and packaging to withstand space flight and radiation, can occupy large areas of PCB real estate. For example, the dimensions of a radiation-hardened synchronous buck converter, the TPS50601A-SP from Texas Instruments, are 12.7mm x 7.37mm (500mil x 290.2mil) with a maximum output current of 6A [11]. Though this package is almost entirely self-contained as a buck converter, mission loads operating at higher currents would require several of these parts together (hence an even larger solution size) to meet load demand without pushing the maximum current on any singular part.

1.2 High Power Density and Miniaturization

The sizable packages and footprints of radiation-hardened components pose an obstacle to high-power-density design, especially for power conversion stages. Current radiation-hardened point-of-load (PoL) power converters are big, as mentioned with the TPS50601A-SP. On the other hand, the LTM4657 from Analog Devices is a comparable commercial off-the-shelf (COTS) buck converter that is also self-contained, can output a maximum current of 8A, and fits in a smaller package measuring 6.25mm x 6.25mm (246.06mil x 246.06mil) [14]. However, building a DC-DC buck converter for space flight with discrete parts instead of a self-contained chip necessitates a controller, switching devices, gate drivers (if not already integrated with the controller), inductors, input and output capacitors, diodes, and other passives, all of which must be able to tolerate the space environment. Attempts to miniaturize electronics, including PoL converters and space electronics, have included the

exploration of smaller and less expensive COTS parts (such as the LTM4657) as alternatives to radiation-hardened components, new and modified control methodologies [17, 25], the choice or optimization of topology [24, 34], specific features such as coupled inductors for multiphase topologies [39], careful consideration of PCB layout [34], magnetics including planar magnetics [41], re-evaluating device packaging and making it smaller [27, 34], and better thermal management for individual parts and overall design [27, 38].

1.3 Wide Bandgap Semiconductors and GaN HEMTs

A product of the emergence and continuing development of wide bandgap semiconductor devices, GaN high electron mobility transistors (HEMTs) demonstrate intriguing advantages over traditional silicon MOSFETs that touch high-power-density design and the search for viable COTS parts for space flight. The bandgap of GaN is 3.4 eV, compared with 1.1 eV for silicon; wide bandgaps enable characteristics such as higher critical electric fields, higher breakdown voltage levels, and higher-temperature operation [22, 43]. Another feature of GaN that sets it apart from silicon is its lower on-resistance, which curtails a margin of conduction loss.

GaN HEMTs, shown in Figure 1, are laterally structured devices with no gate oxide, but they have a two-dimensional electron gas (2DEG) formed by the physical strain between the HEMT's AlGaN and GaN layers, which consequently attracts electrons due to GaN's piezoelectric qualities [38]; the 2DEG has a higher electron mobility than semiconductor crystals [22]. With low input and output capacitance, these GaN-based transistors are capable of high switching frequencies, on the order of MHz, that, in turn, increase power density due to a lower overall solution size [18, 19, 40]. Regarding other switching-associated losses, silicon MOSFETs have an intrinsic antiparallel body diode due to their PN junctions; during switching operations without zero voltage switching (ZVS) mechanisms, the antiparallel body diode must flush remaining charges before it can move into a reverse-biased blocking state - this is the basis of reverse recovery loss. On the contrary, GaN HEMTs do not have

PN junctions, body diodes, or minority carriers but can conduct in the reverse direction, so they do not undergo the reverse recovery process and do not necessarily need an antiparallel diode; the absence of reverse recovery in GaN HEMTs further diminishes switching losses [9, 22, 28, 35].

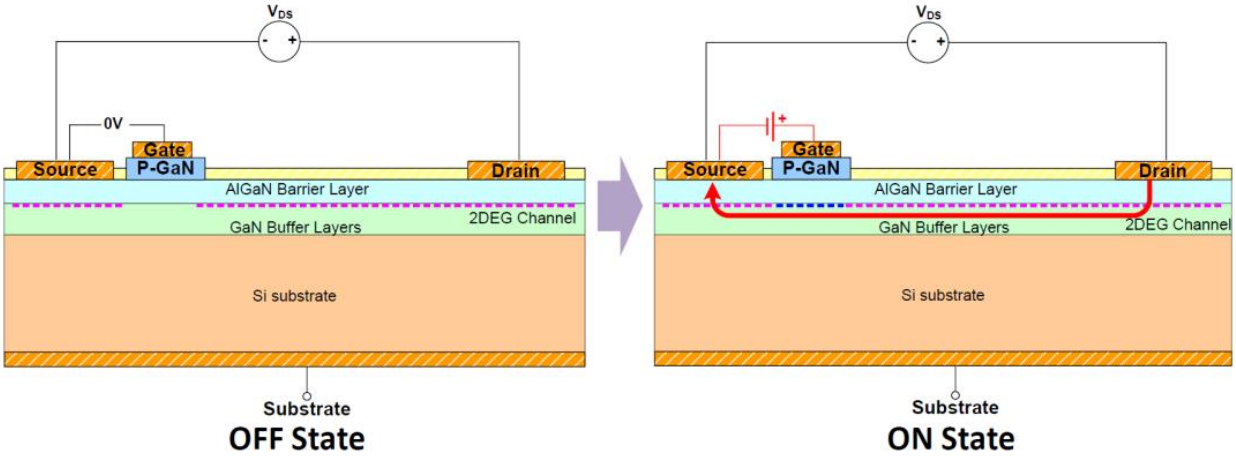


Figure 1: Structure of a GaN HEMT [15]

With respect to the space environment, since many commercial GaN HEMTs have a Schottky metal gate that can dissipate charge, and no gate oxide to trap charge, these transistors become much less susceptible to TID effects [22, 23, 30, 40]. They also operate with smaller depletion regions, rendering them less sensitive to radiation dose rate [23]. TID testing on a number of GaN HEMTs, both COTS and radiation-hardened components, has determined that the GaN devices perform exceedingly well, at least as well as radiation-hardened silicon MOSFETs. Moreover, the results of testing show that many GaN-based transistors can survive up to and over 1Mrad of TID [18, 33]. The significant advantages of GaN HEMTs over silicon MOSFETs make them a very appealing choice for high-density, space-rated power converters.

1.4 Contribution of this Work and Organization of Thesis

The work highlighted in this thesis has two aims. One is to explore miniaturization of DC-DC point-of-load converters for space applications using a GaN-based, multiphase buck topology in conjunction with a selection of less costly and smaller COTS parts. The second aim is to evaluate the TID performance and survival of the chosen COTS parts, especially the controllers.

This paper begins in Section 2.0 with details about the design of the PoL converters from concept and specifications to hardware design, followed by information about testing the boards at baseline and under radiation in Section 3.0. Results of converter testing are presented and discussed in Section 4.0, and Section 5.0 notes points for future work building on the efforts described in this thesis. Finally, Section 6.0 summarizes and draws conclusions about the presented inquiry into miniaturized DC-DC PoL converters for space applications.

2.0 Design

This section describes the process and decisions involved in the design of these DC-DC PoL converters.

2.1 Converter Specifications

The DC-DC buck converters designed in this research are PoL devices intended for computational loads, for which 1.0V, 1.8V, and 3.3V are typical voltages for core power rails [23]. The specifications enumerated in Table 1 were desired goals for performance. Overall solution size, maximum output current, and TID tolerance were flexible metrics, influenced by the available and selected components, their layout on a board, and their ability to continue operating while (and after) being irradiated.

Table 1: Target Specifications for Converter Designs

Parameter	**Goal**
Overall Solution Size	12.70mm x 17.78mm (500mil x 700mil)
Input Voltage Range	3.3V - 6V
Output Voltage Range	850mV - 2.5V
Maximum Output Current	15A
Minimum Efficiency	80%
DC Accuracy of Output Voltage	+/- 1.5%
TID Tolerance	100krad

2.2 Topology

The choice of converter topology can impact miniaturization through sizing and choice of components, mitigation of losses, and functionality that enhances operation and efficiency. Since the PoL converters in this work strive to support up to 15A of current at full load, a multiphase buck topology was chosen in order to split current between two phases.

Single-phase buck topologies, pictured in Figure 2, guide all of the converter current through one path. At lower output currents, the single-phase buck converter performs very well, and the associated conduction losses are not overly concerning. However, high output currents, often demanded by computational loads, burden components in that single path with large conduction losses and thus necessitate selecting components rated for high enough power. Additionally, computing loads typically need power supplies with low voltage ripple and the ability to respond quickly to transients; minimizing output voltage ripple corresponds to minimizing output current ripple (and minimizing parasitic resistances of the output stage), which benefits from large inductances, but fast transient responses instead demand small inductances to enable quicker changes in current [26, 39]. Selection of an output inductor can become a challenge as well due to limits on saturation current for a single packaged inductor [42].

Multiphase topologies connect multiple power converters of the same type in parallel (i.e., two or more buck converters, with switching and output stages, in parallel), such that the time shift between the phases allows their output current ripple to overlap; this overlap destructively interferes to reduce the ripple of the total converter output current. With lower ripple on the overall output current, each branch can take advantage of smaller inductors, which respond faster to transients and occupy a reduced footprint. The multiphase buck topology with individual inductors per phase has limitations to be aware of as well. Smaller inductances per phase increase each phase's current ripple and consequently its peak current - greater peak current and large ripple correspond to higher conduction losses per phase and may contribute to switching losses [24, 26, 39]. Also, [24] states that the multiphase topology with each branch having its own inductor serves only to distribute losses rather than attenuate them.

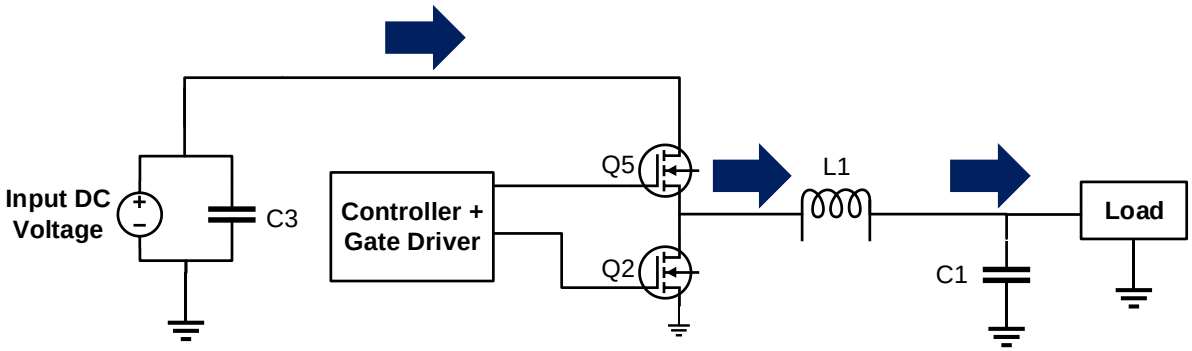


Figure 2: Single-Phase Buck Topology

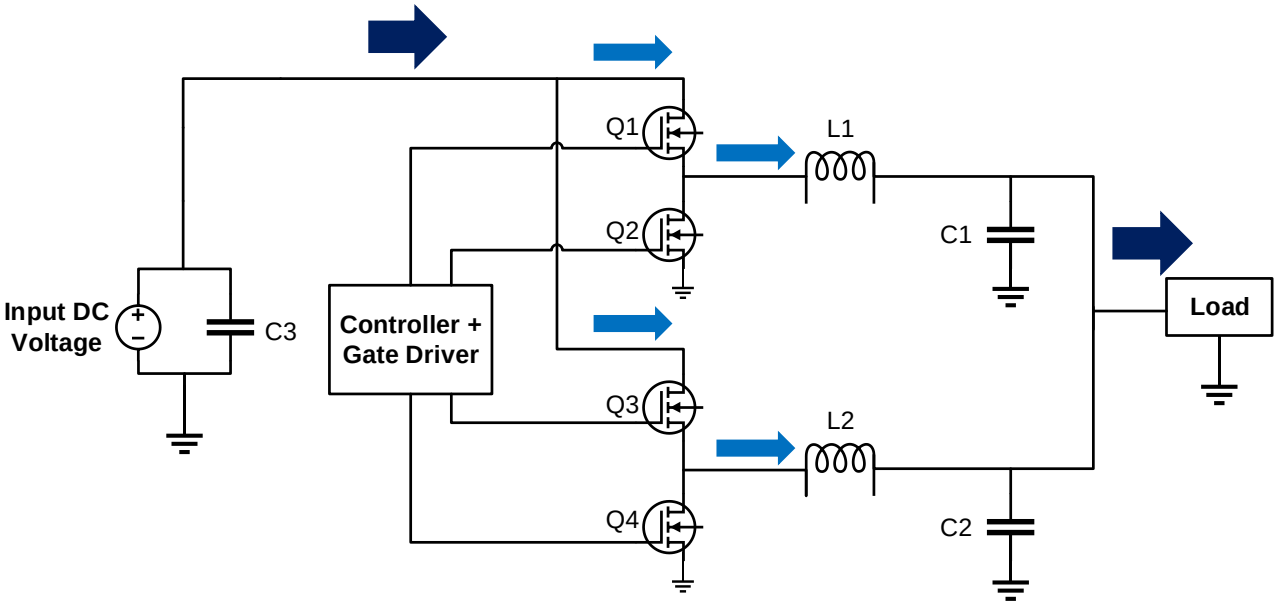


Figure 3: Two-Phase Buck Topology

For a single-phase buck converter, as illustrated in Figure 2, the input/output voltage relationship and output current ripple equation are [26]:

$$V_{out} = D * V_{in}$$

$$\Delta I_{out} = \frac{(V_{in} - V_{out}) * D}{L * f_{sw}} = \frac{V_{in} * (1 - D) * D}{L * f_{sw}}$$

For a multiphase buck converter with two phases, as depicted in Figure 3, assuming that the inductors in each phase are equal ($L_1 = L_2 = L$) and that the phases switch at a 180° shift from each other, the input/output voltage relationship, overall output current ripple, and phase current ripple are [26]:

$$V_{out} = D * V_{in}$$

$$\Delta I_{out} = \frac{(V_{in} - 2V_{out}) * D}{L * f_{sw}} = \frac{V_{in} * (1 - 2D) * D}{L * f_{sw}}$$

$$\Delta I_{phase} = \frac{(V_{in} - V_{out}) * D}{L * f_{sw}} = \frac{V_{in} * (1 - D) * D}{L * f_{sw}}$$

In this research, the dual-phase buck topology illustrated in Figure 3 was adopted for a variety of reasons. Given that the load is computational in nature and the desired full-load current is high for a low-power converter, splitting the current into 7.5A maximum per phase would translate into smaller components and, in turn, a smaller converter form factor, while maintaining a low output voltage ripple. The smaller components would partially be attributed to lower ohmic losses - thus lower power dissipation leading to reduced power ratings required for components - resulting from the lower current level per phase. On top of lessened conduction losses per component, the multiphase topology affords the use of smaller inductors, a component that tends to be challenging for high-power-density applications.

The high switching frequency of 1MHz and the integration of GaN transistors compound the benefits of the multiphase topology in this work. High switching frequencies prompt the use of physically smaller passive components, which further contributes to shrinking the size of the inductor [18, 22, 34]. GaN transistors have lower on-resistance compared with silicon MOSFETs, and by circumventing the higher forward voltage drop seen when GaN conducts in the reverse direction (discussed later), the conduction losses due to higher phase current ripple can be alleviated [28, 35]. Because GaN can turn on and turn off rapidly with lower gate capacitance versus silicon MOSFETs, switching losses also become less of a concern. Regarding the notion that this topology distributes rather than attenuates losses, the efficiency gains from using GaN HEMTs instead of silicon MOSFETs help to compensate, and the distribution of loss as opposed to the concentration of loss may aid in the thermal management of the boards designed in this work, since the PCB itself has a significant role in conducting heat [27].

2.3 Controller, GaN HEMT, and Gate Driver Selection

The primary critical components to choose for these multiphase buck converters were the COTS silicon-based controllers and GaN HEMTs. In searching for controllers and transistors, the space parts derating guides in [36], specifically "Derating Requirements for PEMs" and "Transistor Derating Requirements", were applied to the datasheet specifications.

The controller selection was filtered based on multiphase capability, input voltage thresholds, output voltage ranges, switching frequency, recommended topology/applications per the datasheet, gate driver needs, package dimensions, availability of stock, junction temperature, and radiation hardness or tolerance. The controllers purchased for the converters included Linear Technology's LTC7802, ADP1850, LTC3861, and LTC3861-1 and Texas Instruments' LM3000 and radiation-hardened TPS7H5001-SP. The controllers ultimately used in designs

were narrowed to the LTC7802, ADP1850, and LTC3861 due to time constraints, lack of models for simulation, or significant similarity between one part and another (i.e., LTC3861 versus LTC3861-1). Table 2 lists the key parameters of the three selected COTS controllers, derated per [36].

Table 2: Key Parameters of the Chosen COTS Multiphase Controllers

	LTC7802	**ADP1850**	**LTC3861**
Input Voltage Range (Derated)	3.6V - 32V	0.8V - 16V	2.4V - 19.2V
Output Voltage Range (Rated)	0.8V - 0.99*Vin V	0.6V - 18V	-
Switching Frequency (Derated)	70kHz - 2.1MHz	140kHz - 1.05MHz	0 - 1.575MHz
Maximum Junction Temperature (Derated)	85°C	85°C	85°C
Dimensions	4mm x 5mm (157.48mil x 196.85mil)	5mm x 5mm (196.85mil x 196.85mil)	5mm x 6mm (196.85mil x 236.22mil)
Datasheet Reference	[16]	[1]	[5]

The GaN HEMTs were considered based on drain current and drain-source voltage limits, on-resistance, switching frequency, package dimensions, integration of a gate driver, the number of transistors in a single package, recommended topology/applications per the datasheet, availability of stock, junction temperature, and radiation hardness or tolerance. The HEMTs purchased were Texas Instruments' half-bridge LMG5200; EPC's 2001C, 2015C, and 2302 with EPC23101; and GaN Systems' GS61008P. The HEMTs employed in designs were reduced to the EPC2001C, EPC2015C, and GS61008P as a result of discovered interface incompatibility or the manufacturer working on the product in its engineering phase. Table 3 lists the key parameters of the three selected GaN HEMTs, derated per available silicon power MOSFET guidelines in [36].

Some controllers, notably the LTC3861, required a gate driver. The gate drivers selected for use in the converter designs were Texas Instruments' automotive grade LM5113-Q1 and Linear Technology's LTC4449; the LTC4449 was kept as the sole gate driver for the de-

Table 3: Key Parameters of the Chosen COTS GaN HEMTs

	EPC2001C	**EPC2015C**	**GS61008P**
Maximum Drain Current (Derated)	27A	39.75A	67.5A
Maximum Drain-to-Source Voltage (Derated)	75V	30V	75V
On-Resistance (Rated)	7mΩ	4mΩ	7mΩ
Switching Frequency (Rated)	-	-	10+MHz
Maximum Junction Temperature (Derated)	110°C	110°C	110°C
Dimensions	4.1mm x 1.6mm (161.42mil x 62.99mil)	4.1mm x 1.6mm (161.42mil x 62.99mil)	7.6mm x 4.6mm (299.21mil x 181.10mil)
Datasheet Reference	[12]	[13]	[4]

signs because of interface incompatibility between the LM5113-Q1 gate driver and LTC3861 controller. The LTC4449 gate driver can accommodate a maximum 30.4V input and a maximum junction temperature of 85°C, derated per [36], in a package measuring 2mm x 3mm (78.74mil x 118.11mil) [6].

2.4 Power Circuitry

Beyond the necessary power components for the converter (i.e., input and output capacitors, inductors, and transistors), additional gate circuitry, low-side reverse-conduction diodes, and bootstrap components were added to these circuits to further adjust transistor characteristics and manage stresses on the HEMTs.

GaN HEMTs have a restricted safe operating region at the gate, with a slim overhead margin between typical gate drive voltages and their maximum gate voltage to accommodate overshoot, so gate drive management is critical [20, 29, 35]. Another phenomenon to account for is the Miller turn-on effect, where the gate voltage bounces when the opposite half-bridge transistor turns on, which is due to the high dv/dt (high rate of change of voltage) of turn-

on compounded by L-C ringing [9]. The Miller turn-on effect becomes problematic in GaN HEMTs because their gate threshold voltage, about 1.5V, is typically lower than that of the silicon MOSFET, meaning that GaN HEMTs have a greater risk of spurious turn-on and subsequent shoot-through (only one transistor in a half bridge should be on at any given time, never both) [15]. Severe negative voltage spikes also present a concern - as a device turns off, reverse currents can induce negative voltage surges at the gate, which can be made worse by ringing caused by L-C resonance [9].

There are multiple ways to address damaging gate voltage excursions. One way is to add external gate resistors, ideally one for turn-on and a separate one for turn-off (to which a reverse-oriented Schottky diode is added) to route Miller current [9, 23]. The resistor serves to dampen voltage overshoot, but it slows transistor turn-on and turn-off, which tends to increase the overlap between voltage and current transitions and, in turn, switching loss [9, 20, 29]. So, balance between resistance level and damping is required. In addition to the external gate resistor, a Zener diode can be added in the bootstrap circuit across the bootstrap capacitor to clamp high-side gate voltages [23, 35]. The bootstrap circuit is a charging circuit consisting of a Schottky diode feeding a capacitor through a series resistor; the purpose of the bootstrap circuit is to cyclically garner sufficiently high voltages to drive the switching operation of the high-side transistor.

While GaN HEMTs do not experience reverse recovery losses, there are dead-time periods when the transistor conducts in the reverse direction; GaN transistors exhibit a higher reverse-conduction voltage drop than silicon MOSFET body diodes do [28, 35]. To circumvent the losses associated with this characteristic, a reverse-oriented Schottky can be connected in parallel with the low-side transistor (between ground and the switch node) to reduce the voltage drop seen during dead-time conduction [35].

2.5 Control Circuitry

In addition to the controller, GaN HEMTs, gate drivers, and power components, a set of appropriate capacitors and resistors, as specified by the datasheets, was critical to properly configure the controllers for the intended converter functionality.

All three of the selected controllers needed a resistor, whose magnitude was tailored based on the datasheet, to set the switching frequency. For each controller, voltage feedback was achieved through a resistive voltage divider whose source was tapped from the output voltage rail. Another resistor was employed to establish the soft-start ramp-up time of the output voltage since the controllers do not turn on and output instantaneously (near-instantaneous ramp-up of the output voltage carries a high dv/dt, which poses problems for signal quality and imposes more stresses on the components). For the LTC3861, the soft-start ramp-up time was instead set using a capacitor per [5].

Current sensing was established for two of the controllers through DCR sensing. DCR sensing capitalizes on the existence of the inductor's parasitic DC resistance (an ideal inductor behaves like a short circuit) by attaching an R-C network across the inductor; this network siphons a tiny amount of current to charge a capacitor whose resultant voltage, if the resistor and capacitor are aptly tuned, is proportional to the inductor current [37]. Using a separate resistor with low parasitic inductance for current sensing would be more accurate, but it adds cost, dissipates more power, and takes up space - on the other hand, the DCR method utilizes an existing component with an established inductance, which saves on cost and space without adding parasitic inductance, but the inductor's DC resistance usually varies with temperature [37]. One controller (ADP1850) performs current sensing with the $R_{DS,on}$ method, which calculates current by evaluating the voltage drop across the low-side transistor's on-resistance when it conducts; for this controller, there was a current sense amplifier whose gain was set by a shunt resistor connected at the low-side transistor gate [1, 37].

The controllers also had compensation networks to set the switching regulator control loop characteristics, including the current trip threshold for protection [1, 5, 16]. The compensation was constructed with a resistor and capacitor in series and with another capacitor in parallel across the series R-C string. Modifying the resistance and capacitance tuned the gain and bandwidth of the control loop, respectively, and influenced the closed-loop stability of the system [16].

Each controller possessed one or more PGOOD pins - the binary value read from these pins reflected the controller's verification as to whether its behavior and output were viable. The value could be binary 0, such that PGOOD read approximately 0V, or binary 1, such that PGOOD yielded approximately the internal supply voltage, which in this case was about 5V.

Some controllers had customizable options as well to select features, if available, such as light-load operation, spread spectrum mode, and phase shifting relationships. These are discussed further in the hardware design and bring-up procedure sections.

2.6 Converter Design Tools

To design these converters, LTPowerCAD and LTSpice were heavily leveraged to explore topology performance, select appropriate values of passive components, and understand the functional wiring required for each controller network. LTPowerCAD is a tool developed by Linear Technology to expedite the design of power supplies (i.e., power converters). It contains a database of Linear Technology/Analog Devices components, notably controllers, and upon setting the desired specifications (within the capability of the component), the tool generates the circuit and magnitude of passives necessary for proper function and operation at those specifications. LTSpice is a circuit simulation program with libraries of components and devices and the capability of accepting Spice-compatible manufacturer models. This software can trace anticipated voltages and currents for power signals and control signals, as well as calculate signal parameters (maximum, minimum, average), power dissipation, and efficiency.

2.7 Simulation

Converter designs developed with LTPowerCAD were simulated in LTSpice to characterize and tune their start-up, steady-state, and load-step behavior. Manufacturer models were used to best represent the GaN HEMTs, controllers, and gate drivers in simulation. The primary objectives of the simulations were to configure designs that achieved 1.8V at the converter output with a 1MHz switching frequency, small and controlled output voltage ripple, fast start-up with critical damping or low overshoot, and the ability to handle no load through full loading (15A).

The LTPowerCAD design file for the two-phase converter using the LTC7802 controller is depicted in Figure 4.

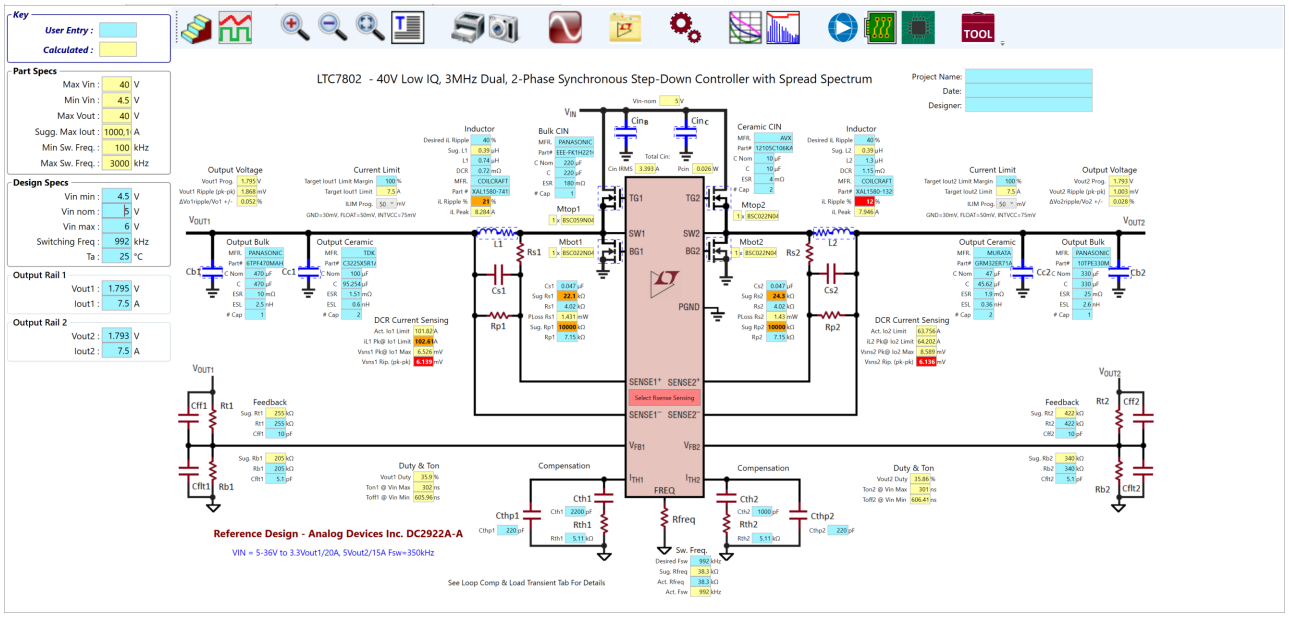


Figure 4: Converter Design with LTC7802 Controller in LTPowerCAD

The circuit schematic of the LTC7802 x EPC2015C converter for simulation is shown in Figure 5. The manufacturer model for the LTC7802 controller already existed in LTSpice, and the model for the EPC2015C GaN HEMT was imported from a set of files created by the manufacturer, EPC. Many of the components were generated by LTPowerCAD based on user-specified inputs (i.e., input voltage, output voltage, maximum output current ripple, switching frequency).

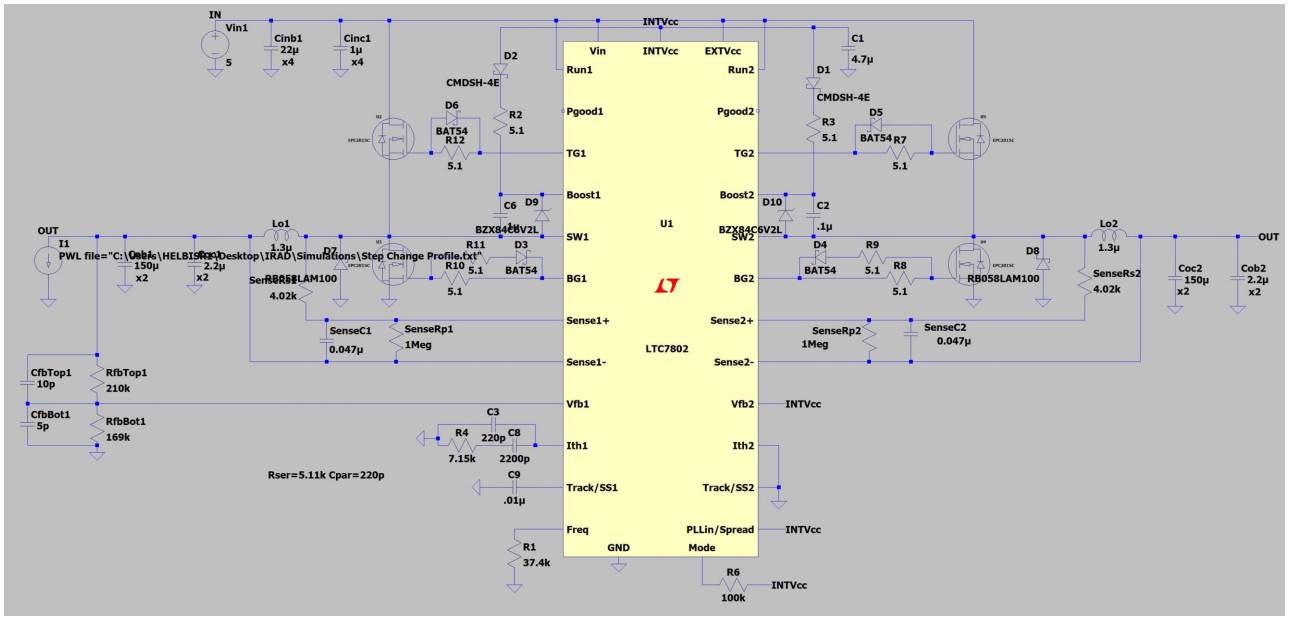


Figure 5: Circuit Schematic of LTC7802 x EPC2015C Converter in LTSpice

2.8 Passives and Diode Selection

Based on the design and editing in LTPowerCAD and LTSpice of the circuit network around the controller and GaN HEMTs, passive components and diode part numbers were selected with sufficiently high current and voltage ratings, and with automotive qualifications when possible, to handle the power anticipated by the simulations. Aside from current and voltage ratings and automotive grade, package size, distributor stock, and applicable NASA standards, specifically S-311-P-829 for ceramic capacitors [31], were prioritized.

LTPowerCAD selected the values of resistors and capacitors. In LTSpice, the average and maximum power dissipation were calculated for each resistor in the circuit, and the average and maximum voltage across each capacitor were determined to facilitate selection of resistors and capacitors with appropriate ratings. On the web pages of electrical component distributors, the ceramic capacitors were further filtered to focus on temperature coefficients of X7R, X5R, and C0G/NP0. The temperature coefficients indicate how the ceramic capacitors' capacitance varies over a range of temperatures, and the mentioned coefficients maintain relatively stable capacitances [32].

In general, for larger capacitances such as the input/output capacitors, tantalum-polymer capacitors were chosen instead of ceramic, due to the guidelines in [31]. Tantalum capacitors exhibit an explosive failure mode, where impurities and cracks in the tantalum dielectric incite mitigation behaviors by the capacitor cathode; however, current flowing too quickly through the dielectric deformities causes the mitigation dynamic between the dielectric and cathode to become combustible. By replacing the cathode with a polymer, the polymer's mitigation behaviors quench the explosive failure mode [32].

Additionally, LTPowerCAD discerned the necessary inductance value using the user-specified maximum output current ripple, switching frequency, and voltage parameters. Beyond the inductance value, given that the full-load output current was targeted at 15A, each phase's inductor required a saturation current sufficiently higher than 7.5A to leave a margin for current ripple and some off-nominal operation. Other considerations made on the distributor web pages included low DCR resistance, a current rating of at least 7.5A, and a high self-resonant frequency (greater than 1MHz to avoid large variations and volatility in voltages and currents). Shielded inductors were preferred over unshielded because the shielding helps to reduce electromagnetic interference (EMI), which injects disruptive noise into converter signals [3, 8].

The gate drive diodes, antiparallel low-side diodes, and bootstrap diodes were all Schottky diodes to allow a conditional, directed path of conduction with a lower forward voltage drop than a standard PN-junction diode. The bootstrap circuit also contained a Zener diode, as mentioned, to clamp the voltage on the HEMT gate. For the Schottky diodes, the important characteristics to consider were low forward voltage in the current range of

interest, fast recovery to support fast converter switching, low reverse leakage current, and low capacitance in the voltage range of interest if possible to aid in fast switching and reduce the potential for parasitic L-C interactions. Regarding Zener diodes, the bootstrap Zener diode needed to clamp the voltage to approximately 5V to protect the transistor gate, so one of the critical fields to filter was the reverse voltage rating. Other attributes to specify were an appropriate maximum power rating to handle the power dissipation calculated by LTSpice and low reverse leakage current.

Once the characteristic filters were applied to the component search, the selection was refined by choosing the smallest surface-mount package and footprint, tightening the tolerance range, and opting for automotive grade. Size-wise, the packages and footprints were to be as small as possible, but not smaller than 0402 or a similar size (for parts with packages and footprints defined on a different scale). The goal was to design PoL converters with small dimensions, but the restriction on the minimum size was primarily driven by a need to be able to manually manipulate components if needed. As for the tolerances, tighter tolerances were necessary for control-related components; the power components could afford slightly more lenient tolerances, but more stringent tolerances were chosen if available and if they did not add much cost. The component grading was not required but added a measure of performance certainty when the option could be selected - automotive grade components are qualified to operate in the high-temperature, high-vibration environment of vehicles. Harsh temperature and mechanical vibration are notable elements of space flight, which indicate that automotive grade COTS parts should be more dependable for space applications than standard COTS parts.

2.9 Hardware Design Tools

Once acceptable converter operation was determined in simulation, the designs in LTSpice were translated into schematics in Altium, complete with part numbers for every component. Most selected components had an associated PCB footprint supplied by the manufacturer, but for components without a manufacturer-defined PCB footprint, a footprint was created in Altium based on measurements in the component datasheet. The Altium schematic for the LTC7802 x EPC2015C board is delineated in Figure 6.

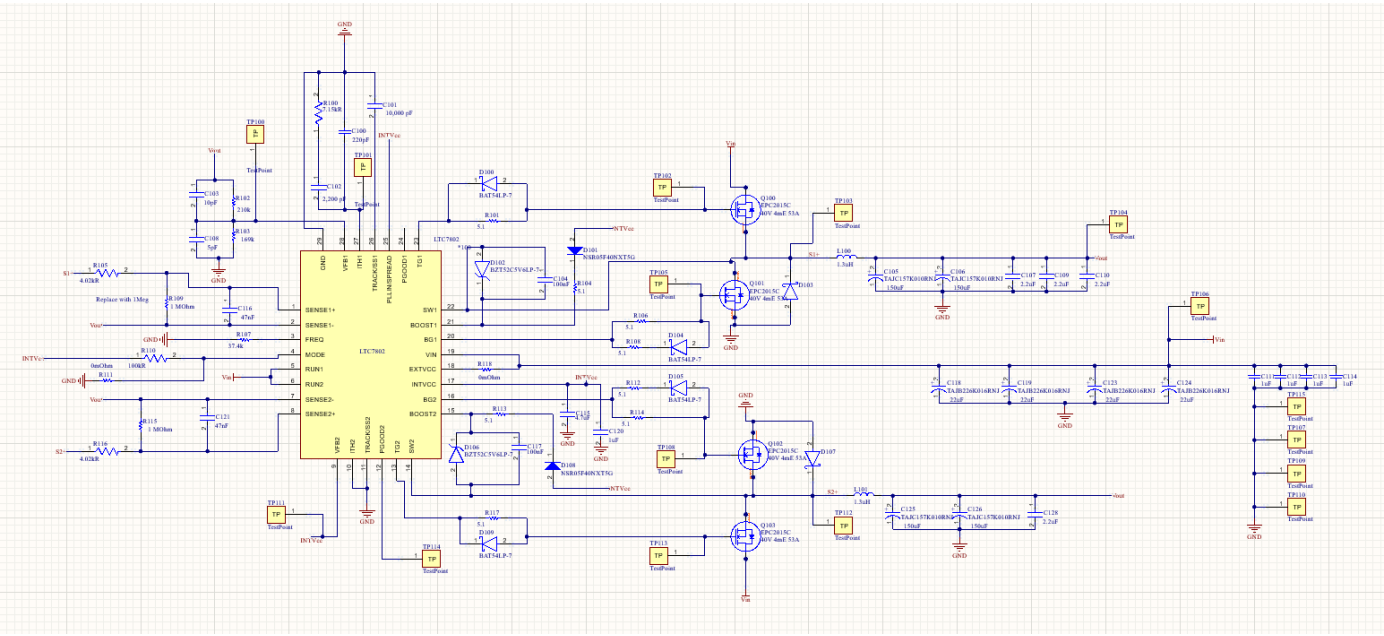


Figure 6: Schematic of LTC7802 x EPC2015C Converter in Altium

Altium's PCB editor was utilized for board layout, with guidance from the Saturn PCB Toolkit and manufacturer requirements for PCB fabrication [7]. The information provided by the Saturn PCB Toolkit assisted in determining the size and number of vias and the copper trace width in order to accommodate the anticipated maximum current in that pathway. The Saturn PCB via sizing tool is highlighted in Figure 7. Among other details, the PCB manufacturer guidelines stated the requirements for minimum via dimensions and minimum trace/space width. The smallest via could have a hole size of 0.2032mm (8mil), and all vias needed to have at least a 0.1270mm (5mil) diameter annular ring around the hole, meaning

that the annular ring, or the pad around the via hole, had to add at least 0.2540mm (10mil) to the size of the via hole. For example, a via with a 0.2032mm (8mil) hole needed to have a total diameter of 0.4572mm (18mil) at the very least. Trace/space refers to how wide a copper trace on a PCB is and how much physical space separates one PCB element from another element connected to a different power/control signal net - whether copper to copper, via to copper, solder mask to solder mask, via to pad, etc. - respectively. Per the manufacturer [7], traces were required to be at least 0.1016mm (4mil) wide, and spaces also needed to be 0.1016mm (4mil) at a minimum.

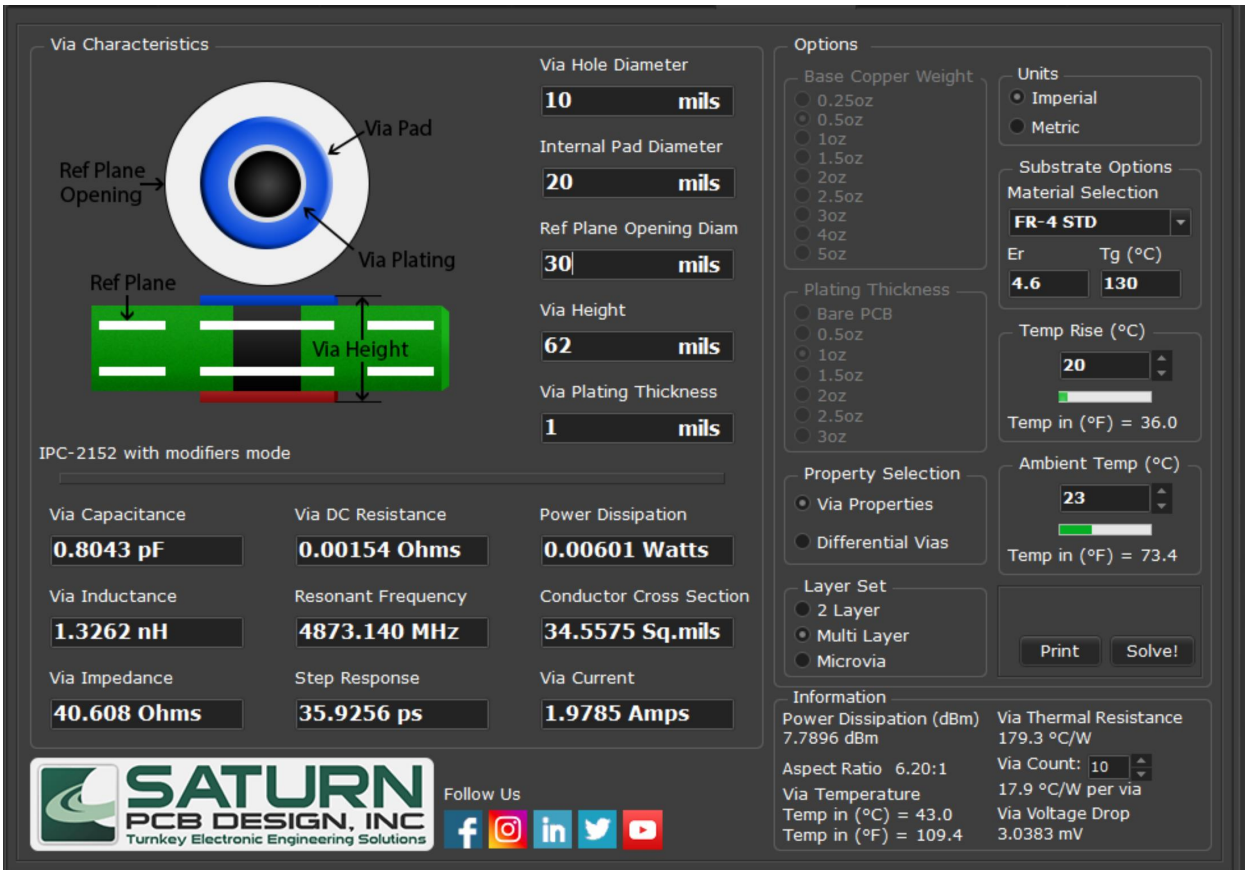


Figure 7: Saturn PCB Toolkit Via Sizing Tool

After the PCBs were laid out in Altium, Gerber files, NC Drill files, and ODB++ files were outputted so as to review the PCB layouts, submit the files to inform board fabrication (the manufacture of the boards), and provide the necessary information to correctly assemble (place components on) the boards.

2.10 Hardware Design

The goal of PCB design for these converters was to reduce the board dimensions as much as possible while maintaining sufficient space for routing and for separating sensitive networks, such as feedback voltage lines, from noisy networks, such as the switch nodes.

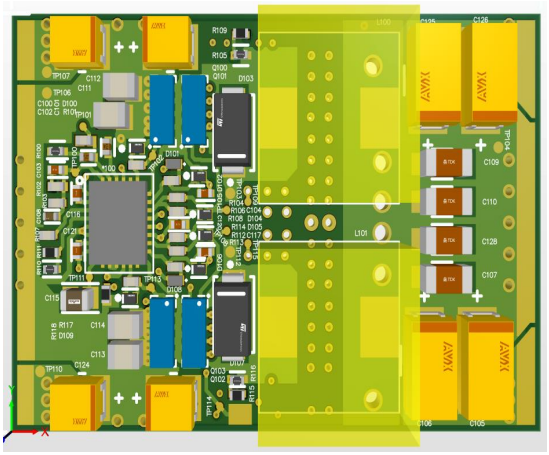
Each converter board was a standard four-layer PCB. Signals, especially power signals and test points, were routed primarily on the top layer, but the third layer was also available for traces that did not fit well on the top layer, particularly cross-board traces. For the purposes of testing and enabling the possibility for flush mounting on a carrier PCB, the converters occupied one-sided PCBs. The use of through-hole vias-in-pad aided the miniaturization effort and, along with dedicated thermal vias, provided some thermal wicking.

The schematics and PCBs were generated such that pins with multiple features, set up through different connections and/or components, would have all of those features available for use on the board. The manipulation of parts to set these features is described later in the bring-up procedure.

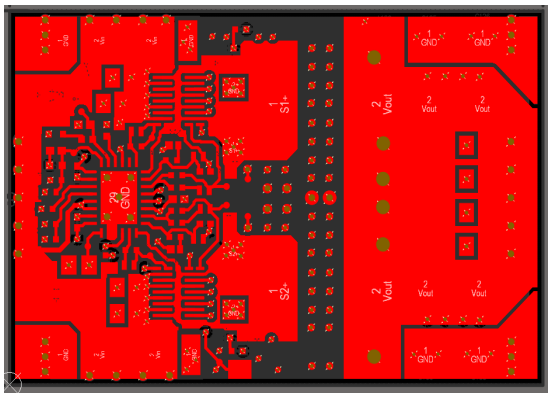
Specific size constraints were posed by the Enhanced Low-Dose Rate Sensitivity (ELDRS) chamber and the High Dose Rate (HDR) chamber. For the HDR chamber at the JHUAPL radiation laboratory, the units under test must be 254mm x 254mm (10in x 10in) or smaller, and for the laboratory's ELDRS chamber, the units must be 152.4mm long x 76.2mm wide (6in x 3in) or smaller, where 12.7mm (0.5in) on either side of the board's length must be clear and used only for slotting into the chamber (thus leaving 127mm (5in) of usable space over the length).

The Altium PCB layouts for the LTC7802 x EPC2015C converter are shown in 3D view and by layer in 2D view in Figure 8.

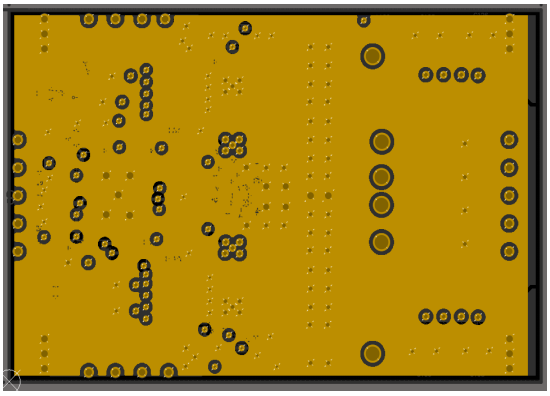
Figure 9 compares the PCBs generated for the designs in terms of physical dimensions, intended switch node phase shift, and any additional customized features (discussed later in the bring-up plan). The LTC7802 x EPC2015C boards were the smallest of the three



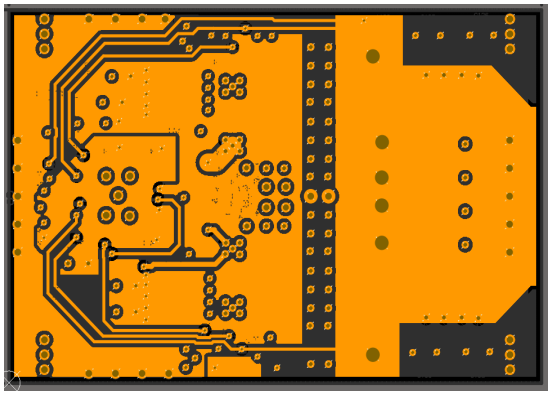
3D View



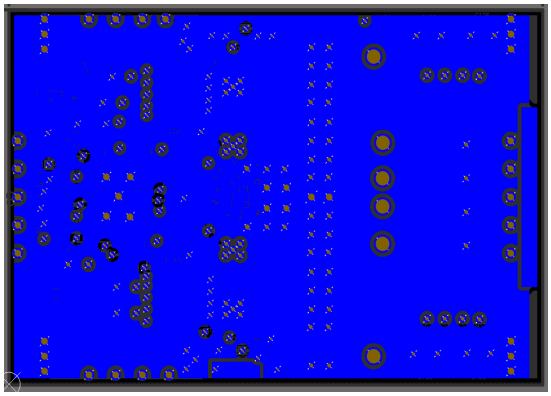
Top Layer – Power/Signal



Layer 2 – GND



Layer 3 – Power/Signal



Bottom Layer – GND

Figure 8: 3D View of PCB and 2D View of Layers for LTC7802 x EPC2015C Board in Altium

designs, while the ADP1850 x GS61008P boards were the largest. It is worth noting that the GaN Systems HEMTs (GS61008P) covered a greater area than the EPC transistors, and the LTC3861 controller required a discrete gate driver, which necessitated an additional component that the LTC7802 x EPC2015C and ADP1850 x GS61008P boards did not have.

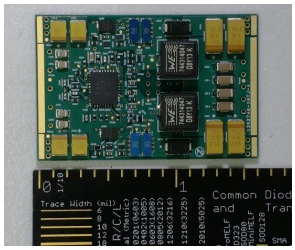
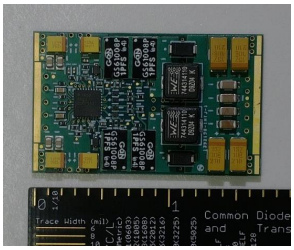
			
	LTC7802 x EPC2015C	**LTC3861 x EPC2001C**	**ADP1850 x GS61008P**
Dimensions	38.10 x 25.40 mm (1500 x 1000 mil)	41.48 x 26.90 mm (1633 x 1059 mil)	43.38 x 26.57 mm (1708 x 1046 mil)
Dual-Phase Phase Shift	180° phase shift	180° phase shift	180° phase shift
Customizations	• Inductors replaced due to out-of-stock/discontinued part • Pulse-skipping mode selected for light load • Spread spectrum mode enabled		

Figure 9: Comparison of Designed Converter PCBs. The pictured ruler measures inches.

To simplify converter design with respect to form factor, provide flexibility during testing, and facilitate compliance with the radiation chamber, a motherboard was created to serve as a standard test fixture for the converter boards. Each motherboard had one or two modules to mount one converter per module; a module had banana jacks for input voltage/ground and output voltage/ground, as well as test loops to probe these nets and provide an easy point of connection to ground for the oscilloscope probes. A module could most easily accommodate a converter if its dimensions were smaller than 48.26mm long x 37.084mm wide (1900mil x 1460mil). On the back side of each module, up to four 0.5Ω resistors configured in parallel

could be soldered to load a converter. At 1.8V nominal output from the converter, by Ohm's Law, each resistor would increase the load current demand by 3.6A. The physical dimensions of each motherboard module were 50.165mm x 60.579mm (1975mil x 2385mil). The front and back of a two-module motherboard are displayed on the left side of Figure 10.

The converters' top-layer input voltage, output voltage, and ground planes had sections of solder mask pulled back from the left and right edges, aligned with the exposed planes on the motherboard modules, so the boards were mounted on motherboard modules using formed segments of soldered bus wire. The right side of Figure 10 depicts converter boards mounted on the motherboard modules.

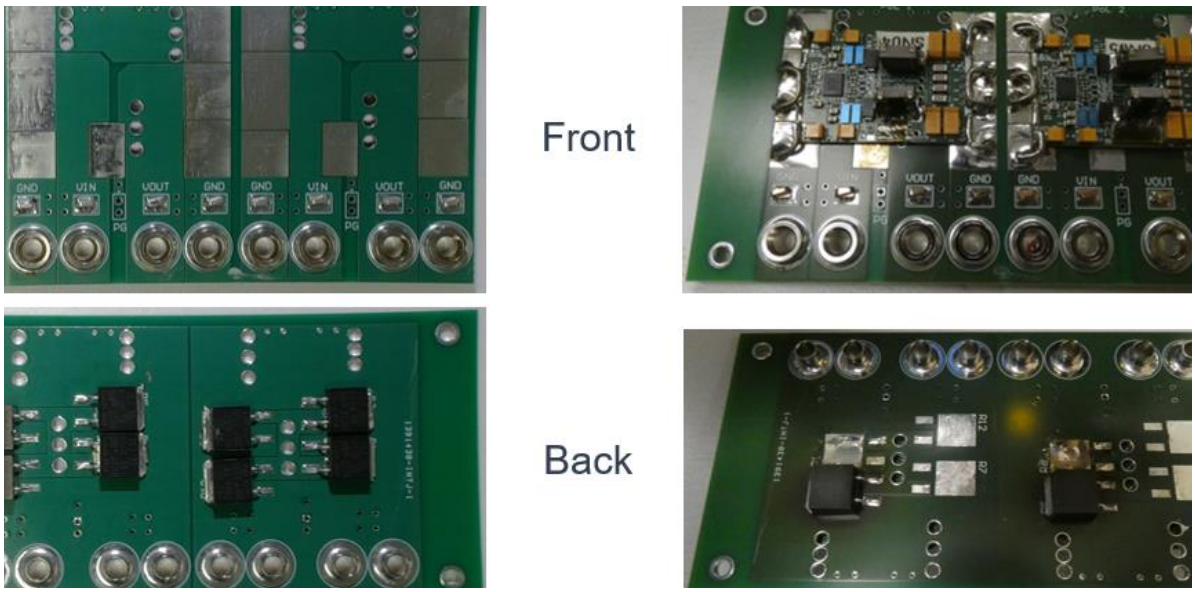


Figure 10: On the left, the front and back of a two-module motherboard PCB. On the right, two converters mounted on the front of the motherboard modules with one load resistor on the back of each module.

In this work, no-touch PCBs were ordered. The manufacturer's no-touch PCB process relies more heavily on automation to assess a layout's Design for Manufacturability (DFM) and to fabricate the boards to ensure that the PCB turns out just as the design files directed [2].

3.0 Testing

The following section details which board design permutations underwent testing as well as the testing that was conducted.

3.1 Tested Converters

Of the six designed, fabricated, and assembled converter permutations, three permutations with three boards per permutation were tested, for a total of nine boards under test. The permutations comprised the LTC7802 with EPC2015C, LTC3861 with EPC2001C, and ADP1850 with GS61008P.

These permutations were selected due to time constraints that capped the number of designs that could be completed, manufactured, assembled, and tested, and due to a desire to experiment with as many different controllers, GaN HEMTs, and gate drivers from the chosen parts as possible, within the time and resource limitations.

3.2 Bring-Up and Baseline Testing

Once the boards were fabricated and assembled, the converters underwent a bring-up procedure before first turn-on. Initial preparations of the boards covered serial number assignment and pictures to document the new board. The bring-up procedure encompassed continuity checks for unanticipated short circuits and open circuits, measured evaluations of component and node impedances, and visual inspections for correct placement and polarity of capacitors and diodes. The final piece of the bring-up process involved removing or adding components as desired or necessary for the purposes of setting a certain controller feature, correcting a design issue, or accommodating a different variation of a part.

The customizations mentioned in the final piece of the bring-up procedure were exercised on the LTC7802 and LTC3861 converter boards. Figure 9 alludes to the features that were picked. For the LTC7802 x EPC2015C converter, pulse-skipping mode for light-load operation was chosen. Pulse-skipping mode functions by forcing the high-side transistor to stay off at very light loads - essentially, to skip pulses, or not switch. It strikes a balance between the controller's other options, burst mode and forced continuous mode; pulse-skipping mode boasts low output ripple, low audio noise, and lower radio frequency (RF) interference compared with burst mode, while supporting higher light-load converter efficiencies versus forced continuous mode [16]. Additionally, spread spectrum mode was enabled for the LTC7802 x EPC2015C converter. Spread spectrum mode works to reduce EMI by varying the designated switching frequency as necessary within certain tolerance bounds [16]. For the LTC3861 x EPC2001C converter, the designer can choose between a few options to set the phase shift between phase 1 and phase 2 of a dual-phase converter, as well as the shift between phase 1 and the output clock signal, which would be used to link more LTC3861 controllers to aggregate more phases [5]. In this work, since only one LTC3861 controller was needed, the phase shift between phase 1 and the clock signal was ignored, and the controller was configured to switch phases 1 and 2 180° apart.

Baseline testing served to characterize the converter parameters and performance prior to exposing the boards to radiation. The boards were tested at unloaded conditions and at loaded conditions, with a 0.5Ω resistor as the load. Parameters of interest during baseline testing included: input voltage and current, output voltage and ripple, output current, the good designation as set by the controller (i.e., PGOOD), switch nodes and phase timing relationship, gate signals for all four transistors, feedback voltage, compensation network voltage, efficiency, switching frequency, start-up time and transient, and temperature.

As a note, in this work, PGOOD was not examined closely as there was a design error for the LTC7802 and LTC3861, which required an external pull-up resistor on the PGOOD pin, unlike the ADP1850 which contained an internal pull-up resistor.

Via the motherboard banana jacks, the converters were fed a 5V input from a DC power supply with active over-current protection. The various parameters of interest were then captured on an oscilloscope set to a 20MHz bandwidth and, for DC quantities, with a digital multimeter; the temperature was measured using a tabletop thermal camera.

3.3 Radiation Testing

Radiation testing for this research focused only on total ionizing dose (TID), both at a low dose rate to test ELDRS and at high dose rates (HDR). The ELDRS and HDR chambers utilized Cobalt-60 sources to irradiate samples with gamma rays. The sole focus on TID was a result of the time, cost, and available resources necessary to conduct the tests - the Johns Hopkins University Applied Physics Laboratory is home to an ELDRS chamber and an HDR chamber with knowledgeable radiation engineers onsite. As is mentioned later in "Future Work", holistic characterization of radiation effects and behavior would include not only TID testing, but also heavy ion testing and neutron beam testing, which provide more information about SEEs and TNID.

The breakdown of radiation dosing is displayed in Table 4. During irradiation, the key parameters to monitor were input voltage and input current, as they were accessible by way of the power supply displays. Between doses, the metrics of interest covered input voltage and current, output voltage and ripple, output current, the good designation as set by the controller (i.e., PGOOD), switch nodes and phase timing relationship, feedback voltage, efficiency, switching frequency, and start-up time and transient. Since these PoL converters were intended to establish appropriate power rails for computational loads during space flight, the converters were powered on during radiation testing.

Table 4: Radiation Dosing and Test Specifications

Radiation Testing	**1. ELDRS**		**2. HDR**	
Dose Rate	22mrad/s, 21.7mrad/s		1.5krad/min	
	Dose Step	*Dose Duration* *Cumulative TID*	*Dose Step*	*Dose Duration* *Cumulative TID*
Dose 1	4.887krad	61.7004 hours 4.887krad TID	10krad	6.58 minutes 20krad TID
Dose 2	5.023krad	64.3047 hours 9.91krad TID	10krad	6.58 minutes 30krad TID
Dose 3	-	-	30krad	19.75 minutes 60krad TID
Dose 4	-	-	40krad	26.34 minutes 100krad TID

The U.S. Department of Defense Test Method Standard MIL-STD-883-1 [10] mandates that electronics with bipolar or BICMOS components be irradiated at a rate of less than or equal to 10mrad/s to evaluate ELDRS behavior. Given time constraints and the experimental and low technology readiness level (TRL) nature of this research, the ELDRS dose rates in this work were increased, but the dose rates and dose delineations still provided good information about ELDRS and HDR converter performance.

The nine boards were irradiated simultaneously; to accommodate this set-up, each converter was provided with 5V from one channel of a DC rack power supply through a 12-foot twisted power cable and the motherboard banana jacks. Each channel of the power supplies was isolated (uncoupled) from other channels on the same rack supply, and each had active over-current and over-voltage protection.

3.4 Annealing

After radiation testing, all nine irradiated boards were annealed at 90°C in a thermal chamber for nine days. The purpose of post-radiation annealing is to assess whether the converters could self-heal incurred damage from irradiation and, if so, to what extent. In some cases, the radiation-induced failure is recoverable, meaning that the units power on and function at or close to pre-radiation metrics, but in other instances, this failure is catastrophic and has destroyed the converters.

[10] suggests that, for accelerated annealing as was conducted here, the electronics be baked at 100°C for 168 hours, or 7 days. To compensate for the lower temperature setting of the thermal chamber, the converters in this work were annealed for a longer period of time.

4.0 Results

This section presents the results of testing where the simulated behavior and the irradiated performance were evaluated against the non-irradiated baseline functionality.

4.1 Baseline vs. Simulated

The simulation work in LTSpice was used as a benchmark for comparing the hardware performance. For the LTC7802 x EPC2015C, the output voltage at steady state was 1.7942V with a critically damped transient, and the switch nodes were out of phase with no overlap. For the ADP1850 x GS61008P, the output voltage at steady state was 1.7997V with a transient overshoot of approximately 0.2V, and the switch nodes were out of phase with no overlap. Finally, for the LTC3861 x EPC2001C, the output voltage at steady state was 1.8019V with an overshoot of about 0.75V, and the switch nodes were out of phase with no overlap.

The hardware performance, captured in Figures 12 and 13, and simulation results, seen in Figure 11, are compared in Table 5.

Table 5: Comparison Between Simulation and Baseline for Converter Parameters

	Output Voltage (V)		**Reference Voltage (V)**		**Output Voltage Ripple (mVpp)**		**Switch Node Phase Shift (ns)**		**Start-Up Time (us)**		**Frequency (MHz)**	
	Simulation	*Baseline (Averaged)*	*Simulation*	*Baseline (Averaged)*	*Simulation*	*Baseline (Averaged)*	*Simulation*	*Baseline (Averaged)*	*Simulation*	*Baseline (Averaged)*	*Simulation*	*Baseline (Averaged)*
LTC7802 x EPC2015C	1.7942	1.779	0.79995	0.7944	1	22.9	440	504	636.6	666.7	1.1455	1.111
ADP1850 x GS61008P	1.7997	1.815	0.59989	0.6029	0.06	93.3	510	680	54.66	64.53	1.042	0.9921
LTC3861 x EPC2001C	1.8019	1.793	0.60017	0.5979	2.4	92.1	510	459	424.15	2190.5	0.990	1.077

The baseline hardware tests and simulations generally corroborated each other, though there were small discrepancies in the values, likely due to parasitics and component imperfections.

However, there were significant variations in the start-up time for the LTC3861 x EPC2001C between the simulated characteristic and the baseline test. This was the only controller that required an external gate driver; it is possible that the simulation models for either the controller or gate driver were not entirely accurate with respect to converter start-up. A more likely explanation is that [5], the datasheet for the LTC3861, states that the capacitor used to set the start-up time should be greater than 10nF, unlike the 1nF capacitor installed on these boards. Although the 1nF capacitor posed no issues in simulation, the hardware may have discounted it or been adversely affected by it during start-up.

Also, the switch node phase shift of the ADP1850 x GS61008 hardware diverged from the simulation - this unexpected behavior is discussed further in the next subsection.

4.2 Baseline vs. Irradiated

The data collected throughout baseline and radiation testing were compiled and analyzed. A summary of the TID results is as follows: the ADP1850 x GS61008P boards survived through 30krad TID, while the LTC7802 x EPC2015C and LTC3861 x EPC2001C boards survived through 20krad TID. It is worth mentioning that two of the three ADP1850 x GS61008P boards survived through 60krad, but the third board suffered a hard failure; it is unclear whether the failure of the third board was a result of radiation, so it is possible that the ADP1850 x GS61008P boards can indeed withstand irradiation through 60krad TID. The ideal goal of 100krad proved to be too aggressive for the components selected for test.

The oscilloscope pictures in Figure 12 display the pre-irradiated baseline start-up, transient, and settling characteristics of the converters (left column) versus at the last successful TID milestone before failure (right column). The images in Figure 13 show the pre-irradiated

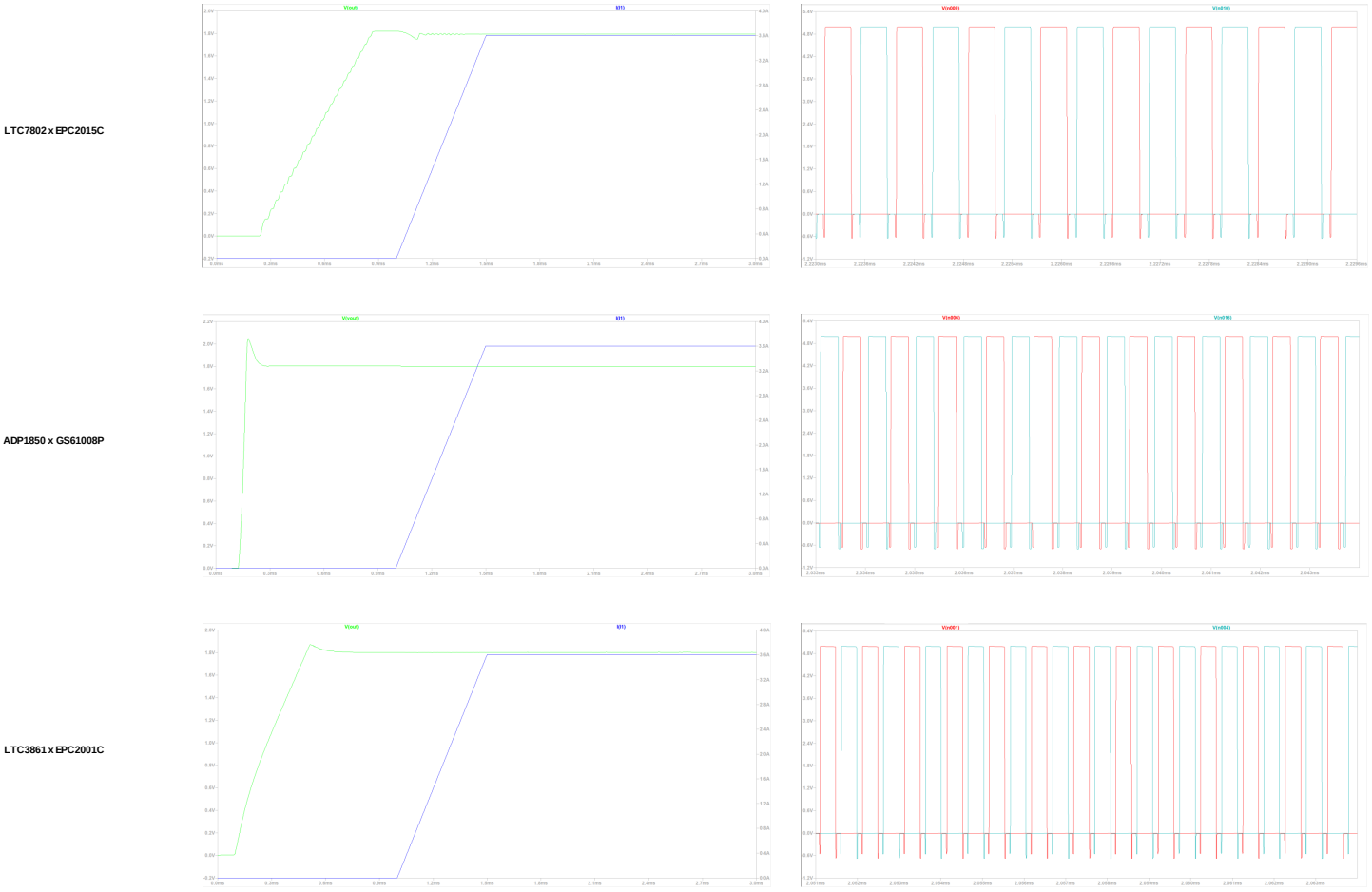


Figure 11: Characteristics of Simulated Converter Designs. The left image in each pair shows the start-up and settling of the output voltage with the ramped current sink load, and the right image depicts the Phase 1 and Phase 2 switch nodes.

versus last successful TID milestone behavior for the switch nodes of each phase. For each parameter, the TID testing did not appear to elicit any noticeably concerning performance from the converters; the graphs in Figures 14 to 18 provide numerical detail about the converter performance.

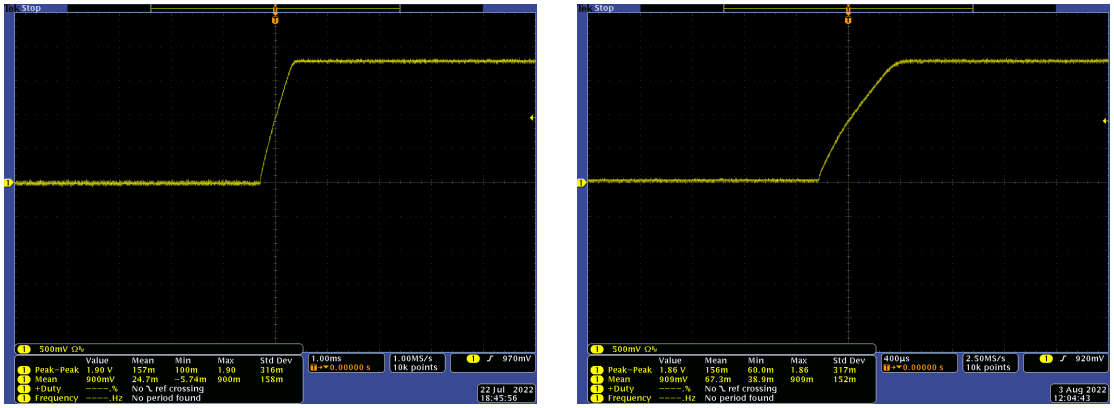
The graphs in this section are laid out such that there are nine lines on each plot, one for each of the nine boards. The three design permutations are represented by a different color (blue = LTC7802 x EPC2015C, yellow = ADP1850 x GS61008P, green = LTC3861 x EPC2001C), and the individual serial numbers within a design permutation are demarcated by a circle (first SN), square (second SN), or triangle marker (third SN).

The assessment of converter performance considered the proximity of an experimental parameter to its desired value, the parametric shift over the course of TID irradiation, and the behavior of one design versus the others. The original target specifications for the converters are contained in Table 1, although, as mentioned earlier, the 100krad TID target was found to be too aggressive for the chosen components.

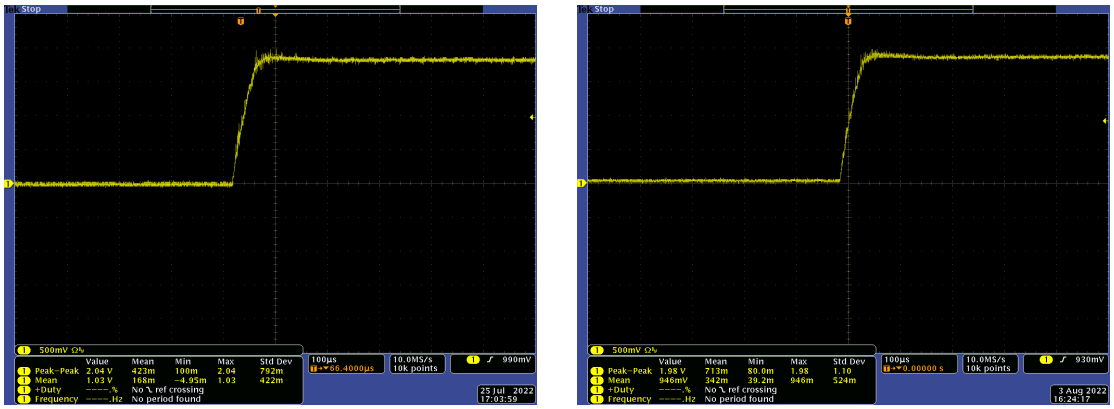
In terms of efficiency, plotted in Figure 14, all three designs met the minimum efficiency target of 80% at a nominal output voltage of 1.8V and nominal output current of 3.6A. Two of the LTC7802 x EPC2015C boards slightly outperformed the ADP1850 x GS61008P boards until the former design failed in radiation testing, but all six of these boards maintained greater than 91% efficiency over the course of testing. The LTC3861 x EPC2001C boards were noticeably less efficient than the other two designs but still posted efficiencies greater than 85% at all radiation benchmarks until failure. It is likely that the LTC3861 x EPC2001C design was less efficient due to the need for a discrete gate driver, whereas the other two designs had gate drivers integrated into the controllers.

The output voltage and ripple are crucial parameters of interest in addition to efficiency. Despite a designed nominal voltage of 1.8V, with some difference that may be attributed to variation in real component characteristics (as opposed to simulated components) and parasitic effects, there was clear parametric drift in the LTC7802 x EPC2015C and the LTC3861 x EPC2001C, as depicted in Figure 15, while the ADP1850 x GS61008P remained steady. The reference voltage that informs the controller response reflected these trends; Figure 16 captures the flat feedback level of the ADP1850 x GS61008P, whereas it shows the

LTC7802 x EPC2015C



ADP1850 x GS61008P



LTC3861 x EPC2001C

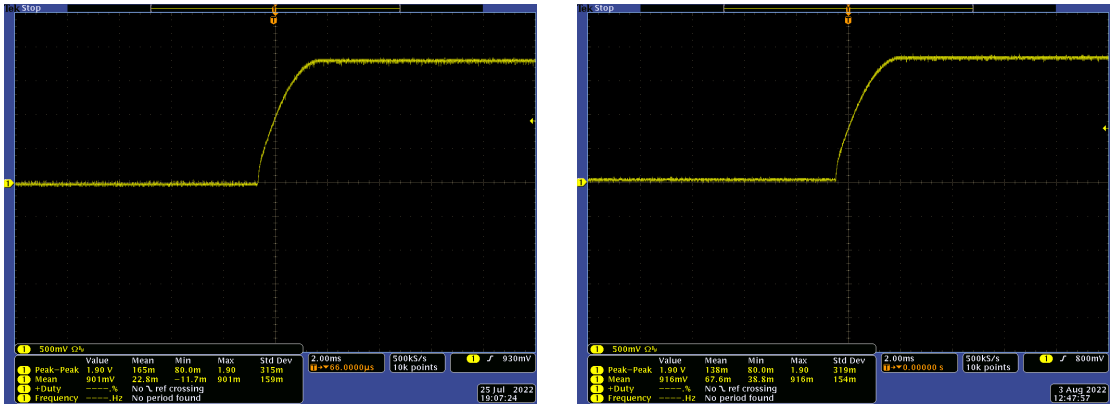
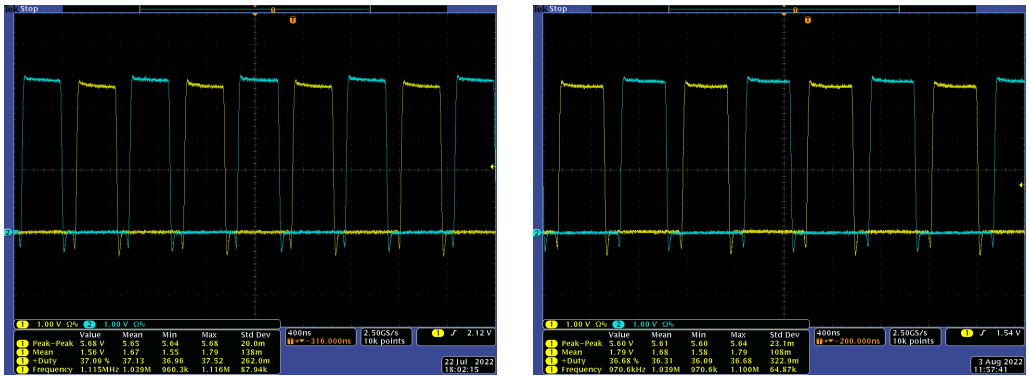
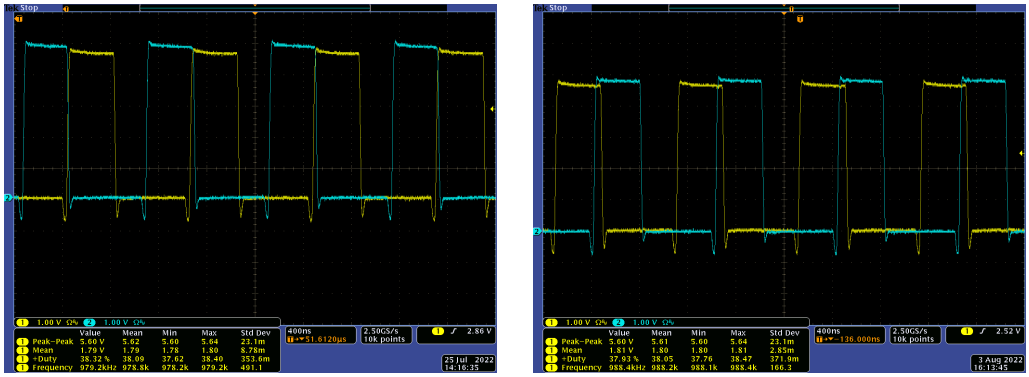


Figure 12: Start-up and Settling of Designed Converter PCBs. The left column is at baseline and the right column is at the last successful irradiated test before the failing dose.

LTC7802 x EPC2015C



ADP1850 x GS61008P



LTC3861 x EPC2001C

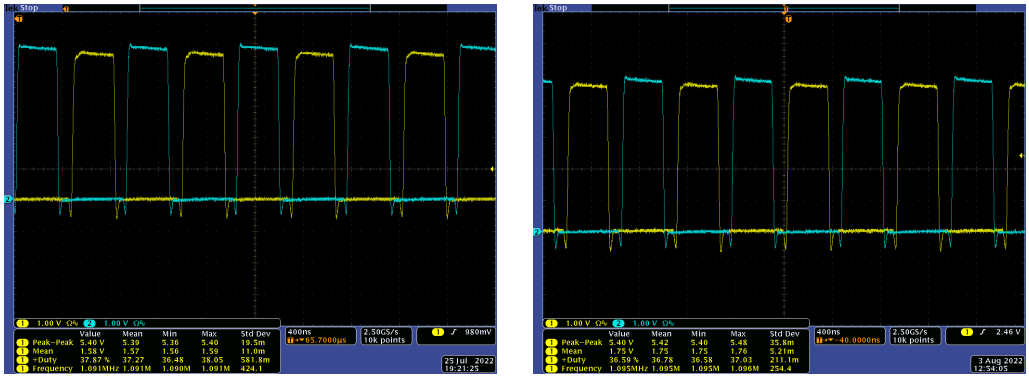


Figure 13: Switch Nodes of Designed Converter PCBs (Channel 1 = Phase 1, Channel 2 = Phase 2). The left column is at baseline and the right column is at the last successful irradiated test before the failing dose.

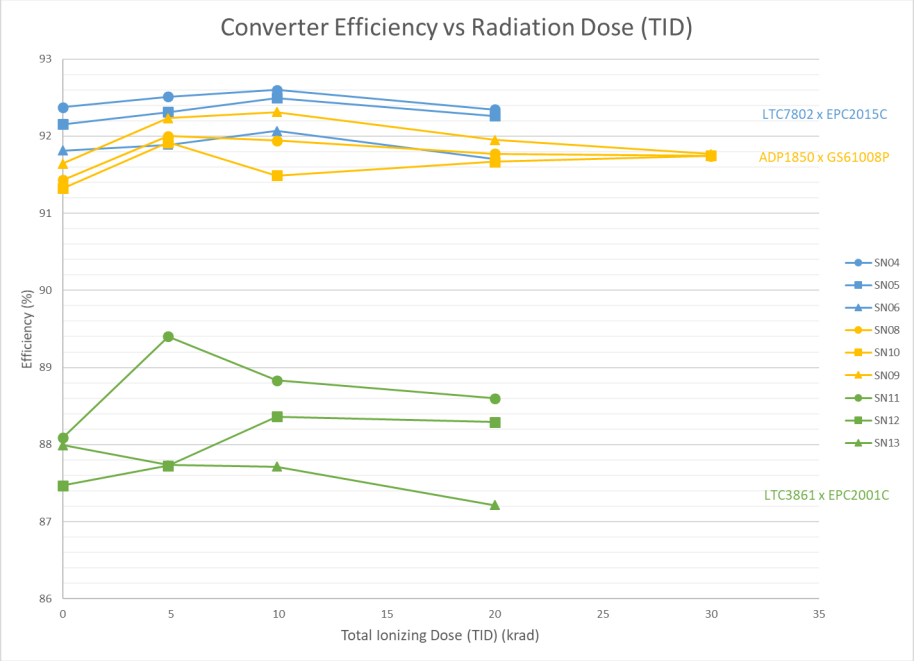


Figure 14: Plot of Converter Efficiency (%) versus Radiation (krad)

downward shift of the other two reference voltages, which consequently drove the controller to push its output voltage lower. This radiation-induced phenomenon is likely due to a shift in the internal bandgap voltage reference used for the output voltage setpoint. The output voltage ripple, plotted in Figure 17, exhibited volatility in value. It is possible that the measured ripple captured the actual ripple competing with noise from the nearby inductor, coupled through the oscilloscope probe's ground lead. The output voltage as a whole quantity adhered to the accuracy boundaries in the original specifications of +/-1.5% (1.773V - 1.827V), but the LTC7802 x EPC2015C boards drifted out of tolerance between 5 and 10krad of dosing.

It is interesting to note that all three designs were meant to have a 180° phase shift between the two phases. However, only two designs - the LTC7802 x EPC2015C and the LTC3861 x EPC2001C - had phases switching at approximately that shift. For a 1MHz nominal switching frequency, the period is 1us, so 180° situates the time shift at 500ns. The ADP1850 x GS61008P phase shift, as charted in Figure 18, fluctuated heavily from baseline

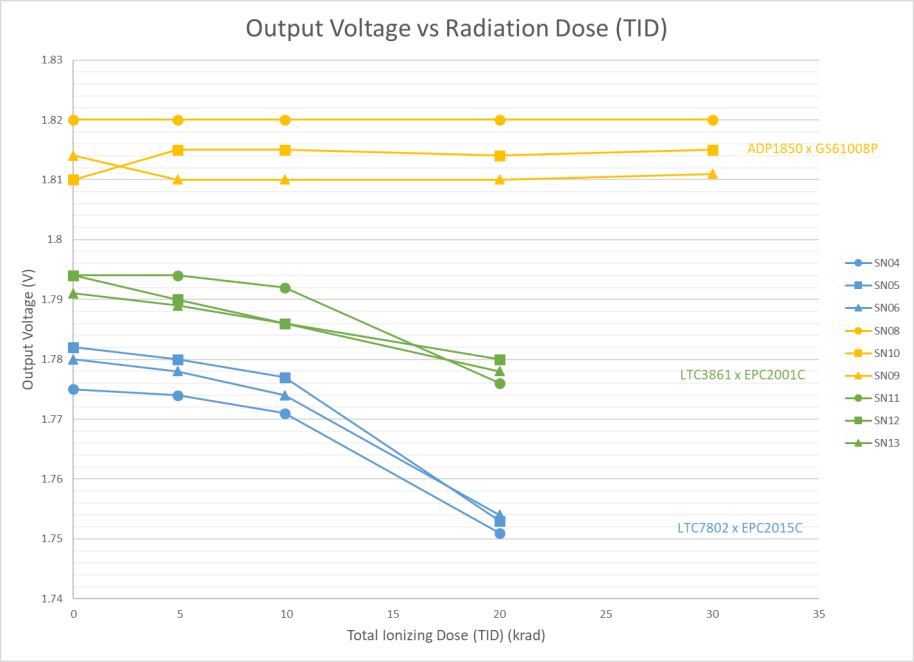


Figure 15: Plot of Output Voltage (V) versus Radiation (krad)

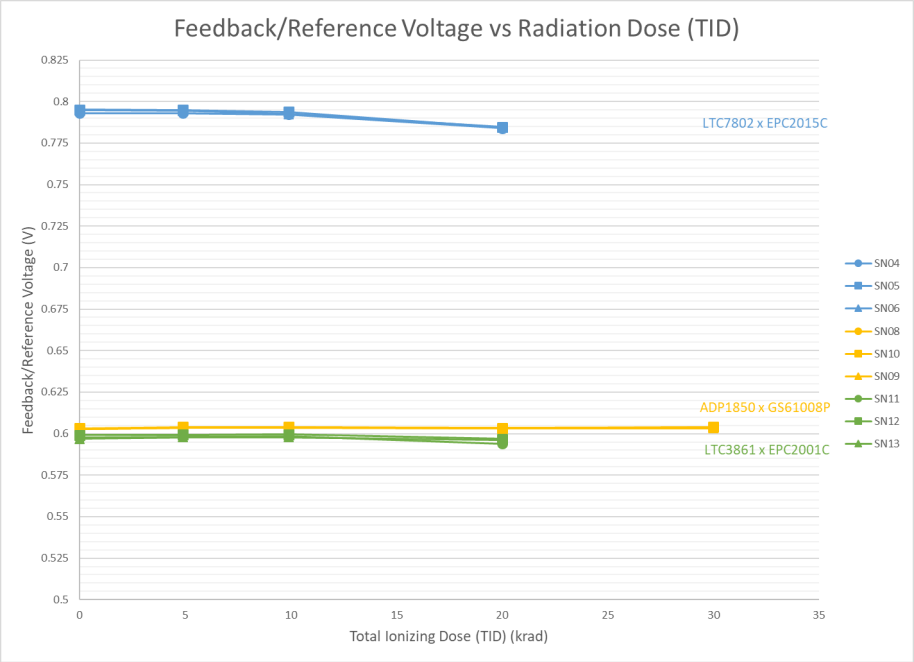


Figure 16: Plot of Reference/Feedback Voltage (V) versus Radiation (krad)

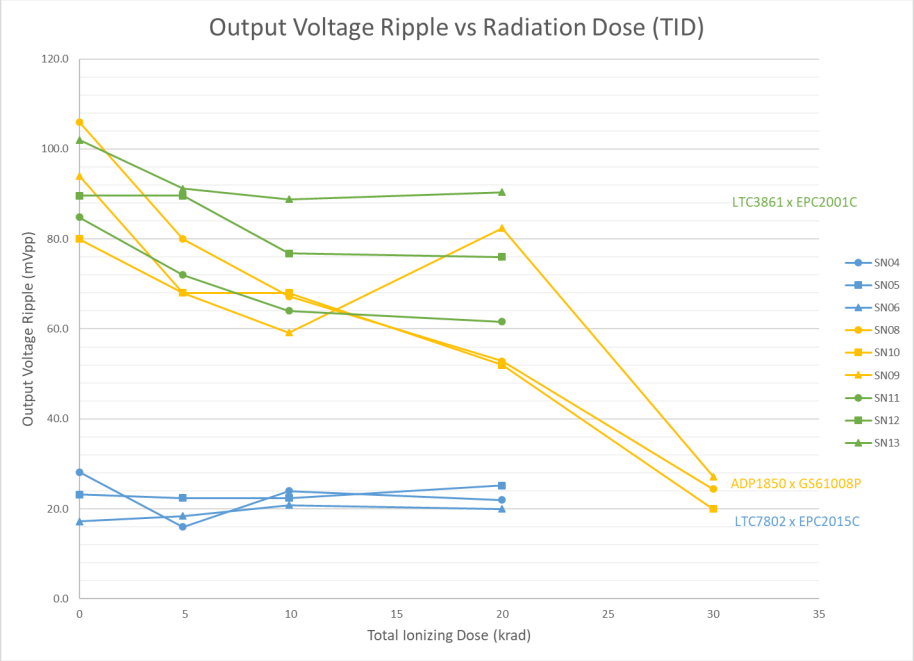


Figure 17: Plot of Output Voltage Peak-to-Peak Ripple (mVpp) versus Radiation (krad)

onwards and did not line up with the expected shift at any point. The discrepancy in phase shift between design and experiment may be another factor that affected the measured output voltage ripple, given that the even distribution of phase activity in a multiphase topology is supposed to destructively interfere to reduce ripple. Additionally, the high-side kelvin connection source sense pins on the GS61008P transistors were disconnected due to a routing error; the lack of finer tuning and correction provided by these pins may also be a culprit.

Regarding converter behavior at the time of failure, some boards, particularly the LTC7802 x EPC2015C boards, did not start up at all, but others, particularly the LTC3861 x EPC2001C boards, managed to start up before their functionality unraveled after a brief period of time. With GaN HEMTs being less susceptible to TID effects, the most likely weak link was the controllers. Points of failure with these devices may have included spurious operation due to an excess of undispersed charges, parameters drifting far enough out of tolerance to incite abnormal behavior, and radiation effects forcing controller shutdown.

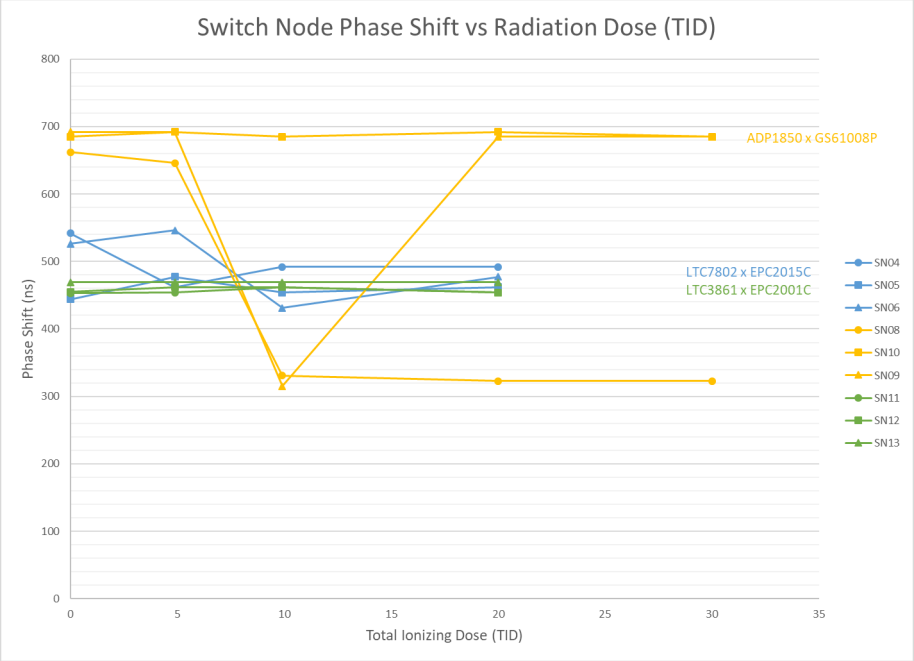


Figure 18: Plot of Switch Node Phase Shift in Time (ns) versus Radiation (krad)

Observations of temperature made using a tabletop FLIR camera indicated that the single hottest component in the system was the load resistor on the motherboard, which could reach temperatures up to and over 150°C during one round of biased data collection.

4.3 Annealed Boards

After annealing for nine days at 90°C, the converters were tested again to evaluate whether they recovered from TID effects. The collected post-anneal parametric data is contained in Table 6. The table highlights key converter parameters and juxtaposes post-anneal data with pre-radiation baseline data. Eight out of the nine boards operated successfully. The ninth board, an ADP1850 x GS61008P board, failed entirely; as mentioned previously, it is suspected that the converter may have experienced non-radiation-related physical damage, such as a failed component or unintentional electrical over-stress during

testing. The remaining ADP1850 x GS61008P boards and the LTC3861 x EPC2001C converters rebounded in behavior, very close to or matching their initial baseline functionality. The LTC7802 x EPC2015C boards rebounded as well, but with a larger margin between baseline and post-anneal values such that the post-anneal output voltages fall outside of the DC accuracy range.

Table 6: Comparison of Baseline and Post-Anneal Data for Key Converter Parameters

		Efficiency (%)		**Output Voltage (V)**		**Reference Voltage (V)**		**Output Voltage Ripple (mVpp)**		**Switch Node Phase Shift (ns)**	
		Baseline	*Post-Anneal*	*Baseline*	*Post-Anneal*	*Baseline*	*Post-Anneal*	*Baseline*	*Post-Anneal*	*Baseline*	*Post-Anneal*
LTC7802 x EPC2015C	*SN04*	92.38	90.97	1.775	1.7300	0.7931	0.7823	28.2	7.2	542	432
	SN05	92.16	91.26	1.782	1.7328	0.7952	0.7805	23.2	5.4	444	421
	SN06	91.82	90.93	1.780	1.7303	0.7949	0.7760	17.2	5.0	526	432
ADP1850 x GS61008P	*SN08*	91.43	90.37	1.820	1.8180	0.6026	0.6043	106.0	19.8	662	653
	SN10	91.32	90.58	1.810	1.8133	0.6032	0.6041	80.0	12.2	685	679
	SN09	91.64	Failed	1.814	Failed	0.6028	Failed	94.0	Failed	692	Failed
LTC3861 x EPC2001C	*SN11*	88.09	87.97	1.794	1.7919	0.5976	0.5997	84.8	19.6	453	453
	SN12	87.47	87.68	1.794	1.7885	0.5991	0.5990	89.6	20.2	455	463
	SN13	87.99	86.81	1.791	1.7880	0.5969	0.5992	102.0	22.8	469	474

Evaluating the collected data, despite the volatile output voltage ripple and uneven phase shift, the ADP1850 x GS61008P showed promise as a great PoL converter candidate - it survived the most total ionizing dose with the most consistent output voltage and with efficiencies rivaling those of the most efficient board design in this work.

5.0 Future Work

This research could be augmented and advanced through a variety of possibilities for future work. Regarding revisions to the existing board designs, a few connections ought to be altered to enhance converter performance; the primary example of this is ensuring that supplemental pins, notably the Source Sense pin on the GS61008P GaN HEMTs, are properly utilized to maximize their benefit. Additionally, swapping bent segments of soldered bus wire connections for through-hole or castellated vias could assist in mitigating parasitics and thermal barriers at the mounting interface.

In terms of testing, the experimentation conducted in this research could be supplemented through studies examining load-step responses and resulting efficiency changes. To do so, the power dissipation of the load resistors and thermal management for the motherboard should be considered in more depth.

For further attempts at miniaturization and performance gains, exploring a coupled inductor for multiphase topologies and, application permitting, a double-sided board design could be fruitful. Coupled inductors capitalize on the advantages of multiphase topologies and provide additional value - where separate smaller inductors per phase improve the overall output ripple and enable faster transient responses but worsen phase current rippling, coupled inductors preserve low output ripple and fast transient response while alleviating phase current rippling [26]. In this work, the inductors and tantalum-polymer input/output capacitors were the largest passive components physically; current and future research into high-frequency magnetics in particular could produce functionally better inductors and ones with tinier footprints, which would be especially useful for high-power-density efforts and PoL power converters.

With respect to the radiation environment of space, the converters designed in this research appreciably survived accumulated charge due to TID - while biased, which makes them more susceptible to irradiation failure [21] - and presented themselves as potential candidates for future space missions with anticipated TID exposure up to 20-30krad. To more stringently qualify these converters and their COTS parts for space applications, testing these

boards in heavy-ion conditions, with a proton source, and in a neutron beam would complete the radiation characterization of the devices. Incorporating a greater variety of COTS parts to design with and test in radiation would amass more radiation performance data and open new alternatives for substituting large, expensive radiation-hardened components for smaller, less costly commercial parts.

One final, yet significant, note to mention is the lack of guidelines for designing with GaN for space flight - specifically, the absence of derating information for GaN devices. As silicon, notably in MOSFET devices, has been the predominant semiconductor material in switching devices for a long time, derating standards have been codified in documents such as NASA's EEE-INST-002 [36]. In this research, derating of components and parameters followed the rules made for silicon, laid out in [36]. However, these rules and standards should be re-evaluated for GaN given that GaN devices exhibit different features and behaviors versus silicon devices, and current derating guidelines based on silicon may insufficiently capture the baseline capabilities and functionality of GaN HEMTs and their superior radiation performance.

6.0 Conclusion

In this research, several designs of DC-DC point-of-load buck converters were created in an effort to miniaturize the boards, utilize high electron mobility transistors (HEMTs) based in the wide bandgap semiconductor gallium nitride (GaN), and characterize a set of commercial off-the-shelf (COTS) components in total ionizing dose (TID) testing. These PoL converters implemented a dual-phase topology on a one-sided PCB at a higher switching frequency of 1MHz, with the objective of providing 1.8V with low ripple and 15A at full loading to computational loads. The COTS parts chosen for design and experimentation comprised the LTC7802, LTC3861, and ADP1850 controllers; the EPC2015C, EPC2001C, and GS61008P GaN HEMTs; and the LTC4449 gate driver. In total, nine boards were manufactured, assembled, and tested: three LTC7802 x EPC2015C, three LTC3861 x EPC2001C, and three ADP1850 x GS61008P. The boards were tested at baseline (no radiation), after 5 and 10krad cumulative TID in the enhanced low dose rate sensitivity (ELDRS) chamber, and after additional doses in the high dose rate chamber of 10, 30, and 40krad. The LTC7802 x EPC2015C and LTC3861 x EPC2001C boards lasted through 20krad of TID, and the ADP1850 x GS61008P boards survived through 30krad with steady output voltages and efficiencies above 90%. The converter designs and results presented in this paper add to the collection of inquiries into GaN devices, point-of-load converters, lower power miniaturization, and COTS experimentation for space missions, while offering ideas for further development and pursuits in these areas.

Bibliography

[1] Adp1850 - wide range input, dual/two-phase, dc-to-dc synchronous buck controller.

[2] Faq // basic circuit boards with no-touch.

[3] Filter design for smps: Shielded vs. unshielded inductors for smps.

[4] Gs61008p - bottom-side cooled 100 v e-mode gan transistor datasheet.

[5] Ltc3861 – dual, multiphase step-down voltage mode dc/dc controller with accurate current sharing.

[6] Ltc4449 - high speed synchronous n-channel mosfet driver.

[7] No touch pcb faq — sierra circuits.

[8] Shielded inductors.

[9] Gn001 application guide: Design with gan enhancement mode hemt, 2 2018.

[10] Mil-std-883-1: Department of defense test method standard: Environmental test methods for microcircuits, part 1: Test methods 1000-1999, 9 2019.

[11] Tps50601a-sp radiation hardened 3-v to 7-v input, 6-a synchronous buck converter, 10 2019.

[12] Epc2001c - enhancement mode power transistor, 2021.

[13] Epc2015c - enhancement mode power transistor, 2021.

[14] Ltm4657 - 20vin, 8a step-down dc/dc umodule regulator, 3 2021.

[15] Gn001 application note: An introduction to gan enhancement-mode hemts, 3 2022.

[16] Ltc7802 - 40v low iq, 3mhz dual, 2-phase synchronous step-down controller with spread spectrum, 5 2022.

[17] Philippe C Adell, Ming Sun, Kishan Joshi, Gregory Allen, Zhe Yang, and Bertan Bakkaloglu. Radiation-tolerant digital multiphase current-mode hysteretic point-of-load regulator. *IEEE Transactions on Nuclear Science*, 65:896–902, 2018.

[18] Ansel Barchowsky, Ahmadreza Amirahmadi, Chris Stell, Elvis Merida, Gary Bolotin, and Greg Carr. A class of gan-based, radiation-hardened power electronics for jovian environments. pages 3339–3345, 2019.

[19] Ansel Barchowsky, Joseph P. Kozak, Brandon M. Grainger, William E. Stanchina, and Gregory F. Reed. A gan-based modular multilevel dc-dc converter for high-density anode discharge power modules. In *2017 IEEE Aerospace Conference*, pages 1–10, 2017.

[20] Ansel Barchowsky, Joseph P Kozak, Michael R Hontz, William E Stanchina, Gregory F Reed, Zhi-Hong Mao, and Raghav Khanna. Analytical and experimental optimization of external gate resistance for safe rapid turn on of normally off gan hfets. pages 1958–1963, 2017.

[21] Robert Baumann and Kirby Kruckmeyer. Radiation handbook for electronics, 2019.

[22] Kristen Boomer, Leif Scheick, and Ahmad Hammoud. Body of knowledge for gallium nitride power electronics, 10 2020.

[23] Thomas Cook, Aidan Phillips, Christopher Siak, Alan D George, and Brandon M Grainger. Evaluation of point of load converters for space computational loads. pages 1–12, 2020.

[24] Michael de Rooij and Quentin Laidebeur. Meeting the power and magnetic design challenges of ultra-thin, high-power density 48 v dc-dc converters for ultra-thin computing applications. *IEEE Power Electronics Magazine*, 8:30–36, 2021.

[25] Yudai Furukawa, Ippei Sugimoto, Fujio Kurokawa, Haruhi Eto, Tsuyoshi Higuchi, and Ilhami Colak. Miniaturization of buck-boost dc-dc converter with fast p control. pages 1100–1103, 2015.

[26] John Gallagher. Coupled inductors improve multiphase buck efficiency, 2012.

[27] John S Glaser, Assaad Helou, Muskan Sharma, Robert Strittmatter, and Michael de Rooij. Simple high-performance thermal management of chip-scale gan fets. pages 44–49, 2021.

[28] John S Glaser and David Reusch. Comparison of deadtime effects on the performance of dc-dc converters with gan fets and silicon mosfets. pages 1–8, 2016.

[29] Joseph P. Kozak, Ansel Barchowsky, Michael R. Hontz, Naga Babu Koganti, William E. Stanchina, Gregory F. Reed, Zhi-Hong Mao, and Raghav Khanna. An analytical model for predicting turn-on overshoot in normally-off gan hemts. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(1):99–110, 2020.

[30] Joseph P. Kozak, Ruizhe Zhang, Qihao Song, Jingcun Liu, Wataru Saito, and Yuhao Zhang. True breakdown voltage and overvoltage margin of gan power hemts in hard switching. *IEEE Electron Device Letters*, 42(4):505–508, 2021.

[31] Dennis Krus. S-311-p-829: Capacitor, ceramic, multilayer chip, space applications, 7 2013.

[32] James Lewis. They're just capacitors? - bald engineer, 6 2016.

[33] Alex Lidow, Tony Marini, Stefano Michelis, David Reusch, Robert Strittmatter, and Max Zafrani. *GaN Power Devices and Applications*. Power Conversion Publications, 1 edition, 2022.

[34] Robert C N Pilawa–Podgurski. Emerging circuit techniques to utilize wide-bandgap semiconductors in compact, lightweight, and efficient power converters. pages 5.6.1–5.6.4, 2021.

[35] David Reusch and Michael de Rooij. Evaluation of gate drive overvoltage management methods for enhancement mode gallium nitride transistors. pages 2459–2466, 2017.

[36] Kusum Sahu. Eee-inst-002: Instructions for eee parts selection, screening, qualification, and derating, 4 2008.

[37] Kevin Scott and Henry Zhang. Switch mode power supply current sensing - part 3: Current sensing methods.

[38] Johan Strydom, David Reusch, Steve Colino, and Alana Nakata. Using enhancement mode gan-on-silicon power fets (egan fets), 2017.

[39] Charles R Sullivan and Minjie Chen. Coupled inductors for fast-response high-density power delivery: Discrete and integrated. pages 1–8, 2021.

[40] J Y Tsao, S Chowdhury, M A Hollis, D Jena, N M Johnson, K A Jones, R J Kaplar, S Rajan, C G de Walle, E Bellotti, C L Chua, R Collazo, M E Coltrin, J A Cooper, K R Evans, S Graham, T A Grotjohn, E R Heller, M Higashiwaki, M S Islam, P W Juodawlkis, M A Khan, A D Koehler, J H Leach, U K Mishra, R J Nemanich, R C N Pilawa-Podgurski, J B Shealy, Z Sitar, M J Tadjer, A F Witulski, M Wraback, and J A Simmons. Ultrawide-bandgap semiconductors: Research opportunities and challenges. *Advanced Electronic Materials*, 4:1600501, 2018.

[41] Saragadam Vibhusha and Bhanudas S Bhosale. Realization of high-efficiency miniaturized 24w dc-dc converter using planar magnetics for space applications. pages 1–6, 2017.

[42] Kae Wong and David Evans. Merits of multiphase buck dc/dc converters in small form factor applications, 3 2015.

[43] Ruizhe Zhang, Joseph P. Kozak, Ming Xiao, Jingcun Liu, and Yuhao Zhang. Surge-energy and overvoltage ruggedness of p-gate gan hemts. *IEEE Transactions on Power Electronics*, 35(12):13409–13419, 2020.