# Investigation into the Design and Operation of Foundry Compatible Electrically Driven Waveguide-Integrated Microheaters for Phase Change Photonics

by

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"'I did some *researchin'*. Real, serious stuff.' [Wayne] paused. 'Why do they call it *re*search if I've only done it this one time?'

'Because I'll bet you had to look things up twice,' Waxillium said."

-Brandon Sanderson, *The Alloy of Law*

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Phase change chalcogenides such as $Ge_2Sb_2Te_5$ (GST) enable advanced optical devices for applications such as in-memory computing, reflective displays, tunable metasurfaces, and reconfigurable photonics. Designing reliable and efficient electrical heaters to control phase change materials can be challenging due to the strict thermal requirements required to achieve reversible switching devices, namely high temperatures and extremely fast quenching rates for amorphization. This dissertation presents a multiphysics simulation framework for modeling semiconductor waveguide-integrated microheaters designed to switch optical phase change materials, as well as experimental characterizations of fabricated devices. The developed model is used to explore the effects of geometry, doping, and electrical pulse parameters, enabling optimization of switching speed and energy consumption in these electro-optical devices. Experimental Raman thermometry data is presented that verifies the theoretical framework, and new heater structures with the potential for improved performance are proposed for theoretical and experimental investigation. These novel heater structures' optical performances and electrothermal efficiencies are compared, creating design guidelines for application-specific implementation.

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## Preface

There are too many people and too short a space to fully thank them all here, but I'll give it a go. They say it takes a village to raise a child, but they didn't mention it takes a major metropolitan area to complete a work of this magnitude. I would like to specially thank Dr. Feng Xiong for all of his help and support, both personally and professionally throughout the years, as well as Dr. Nathan Youngblood for helping me finish out strongly. I would also like to thank Dr. William Stanchina, for helping get me my start in the graduate program here, and helping to show me what it takes to continue to be successful as a researcher. I would also like to thank my committee for their time and efforts. To all my lab mates, current and past, I would say thank you for all your efforts either directly or indirectly. More specifically, I would like to thank Mohammed Sharbati, Qingzhou Wan, Yanhao Du, and Joe Kozak for helping me through the majority of my graduate school career and showing me the way to the end.

Personally, I want to say a special thank you to all 4 of my parents, as well as my siblings and niblings, without you guys I for sure would not have made it this far. I would also like to thank all of my friends for putting up with all of the late night rants and stress fests I've included them in. I would like to shoutout Chris Dumm for all of the editing help as well as all of the tech talk sessions we've had over the years. And finally, my wife and life partner Erica Erickson. I could write another full 100 pages about how much you mean to me, but I'll have to restrict myself in the interest of time. We both know that none of this would have been possible if it weren't for all of the love and support you've given me throughout the years. You are the best and I love you.

From the bottom of my heart, thank you all.

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# 1.0 Introduction

Since the discovery of the PN junction in the mid-20$^{th}$ century, silicon has quickly become one of the most studied materials on the planet, kickstarting the modern multi-billion-dollar electronics industry. Decades of focused research have led to mature, efficient processes for silicon-based semiconductor fabrication and plummeting electronics costs. However, the limits predicted by Moore's law are finally beginning to hold firm. For example, modern microprocessors are unable to exceed clock rates of about four GHz before thermal management issues arise. In addition, there are diminishing returns on power savings: after a certain point, smaller transistors do not consume less power [1]. An alternative technical approach to these limitations is derived from the field of photonic computing: silicon-based photonic devices.

The body of incumbent photonic literature describes several different waveguide structures which can be categorized by operating principle, material type and other factors, some of which are shown in Figure 1.1. Two major waveguide families exist: *planar*, and *non-planar*. Planar waveguides are relatively simple devices, confining light in only one transverse direction. Such devices tend to have limited applications due to their larger sizes; thus, more focus has been directed toward development of non-planar waveguides (perhaps most notably the conventional optical fiber). Non-planar waveguides confine light in two dimensions allowing for more complex and practical devices [2]–[4].

Despite all of these possible variations in waveguide types, Si waveguides dominate the field of microphotonics, largely due to a combination of favorable properties and the maturity of Si semiconductor fabrication techniques. Si is optically transparent at the wavelengths used for

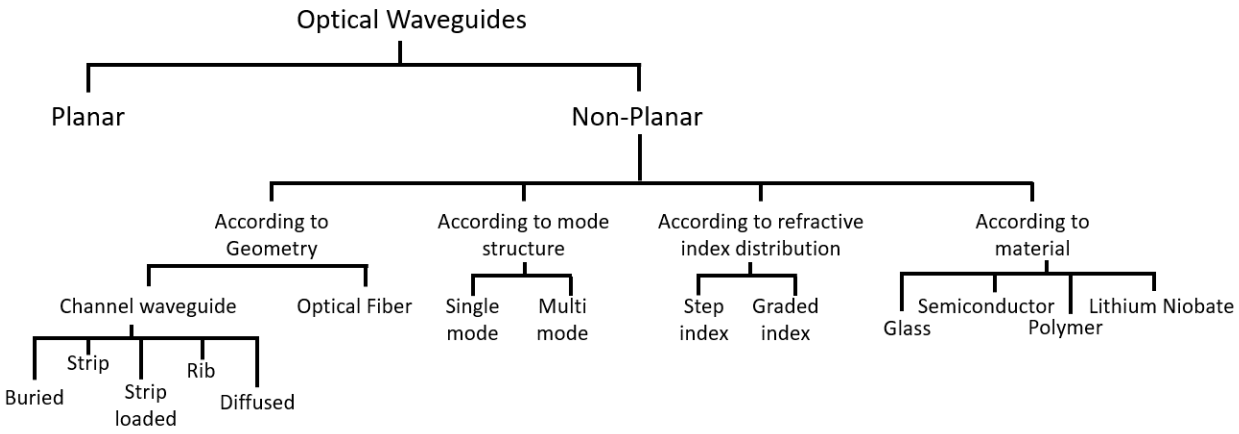


**Figure 1.1 - Types and categorization of optical waveguides. Reproduced from [5].**

standard telecommunications (1.3–1.6 μm) and has a large contrast in refractive index when compared both with its native oxide and air. These differences in refractive index allow for strong light confinement, making compact optical devices easier to realize. This work will focus on Si based rib waveguides (planar film of material with a raised slab), as they are among the most common for integrated photonic devices.

## 1.1 Silicon Photonics

The field of silicon photonics started garnering interest in 1987 when Soref and Bennet first predicted the free carrier dispersion effect in silicon [6]. This effect is also known as the plasma dispersion effect, and will be hereafter referred to as such to prevent confusion with the free carrier absorption effect [7]. Soref and Bennet used a numerical Kramers-Kronig analysis to predict refractive-index perturbations (for both the real and imaginary portions, $n$ and $k$, respectively) in crystalline-silicon due to applied electric fields or injected free carriers [6] . This discovery of a controllable refractive index was implemented by integrating a PN junction into a

Si waveguide structure, making a phase modulator, the first component towards a photonic integrated circuit (PIC) [8]–[10].

While the discovery of the plasma dispersion effect was a key factor in enabling optical control, the search for high quality waveguides was also paramount. In fact, the first PICs would not be developed until after these standard chips were available [8]–[10]. With Bruel's development of silicon-on-insulator (SOI) wafers in 1991, light could now be confined to a portion of a chip, and established lithography techniques could be used to fabricate Si waveguides with custom geometries on chip [11].

Although the SOI waveguides were initially fairly large, on the order of micrometers [12], a de-facto industry standard of a 220 nm Si layer was quickly adopted, with several device milestones being realized: low losses [13], tight bending radii [14], and multiple other key components [15]–[19]. Standardization allowed for rapid maturation of fabrication processes, expanding Si's dominance from the established electronics market into microphotonics. While thicker Si layers offer advantages for certain applications [20], many of the critical devices required to implement fully optical integrated circuits have been developed using the 220 nm Si standard, some general categories of which are shown in Figure 1.2. These devices have contributed heavily to the field of interest of this work: photonic based computation and memory devices.

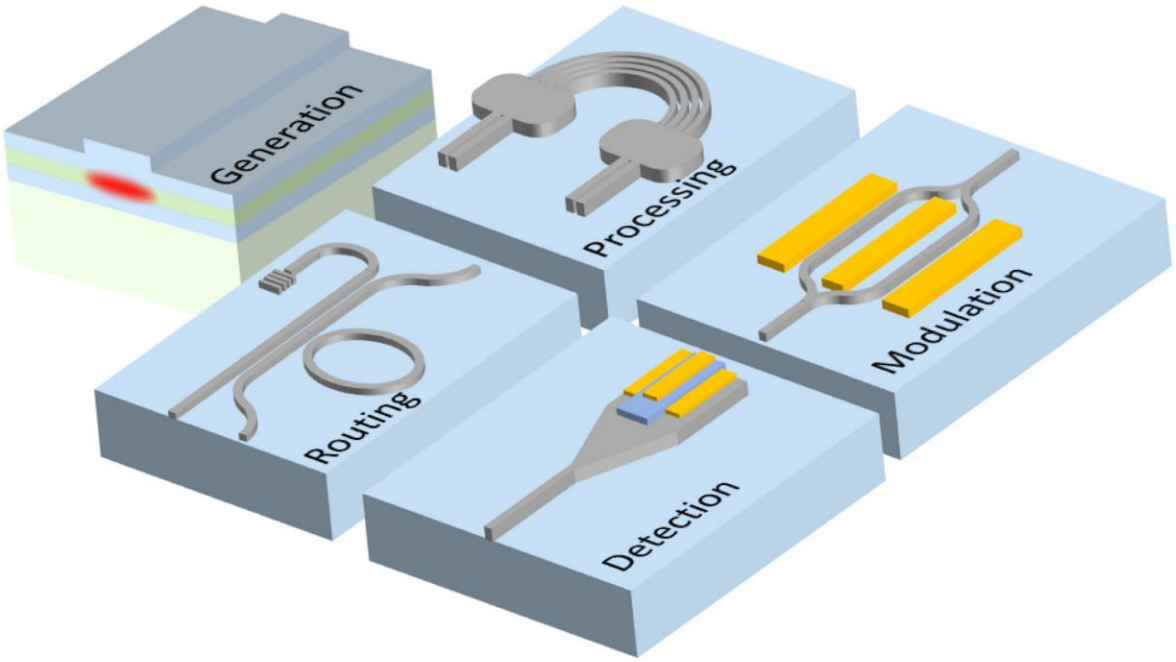


**Figure 1.2 – Examples of essential photonic circuit components. Reprinted from [21].**

## 1.2 Photonic Integrated Circuit Applications – Photonic Computing

Advances in the field of Si photonics described in the previous sections have enabled development of photonic-based computing and memory devices, the subject of this investigation. While there is presently only limited research activity in development of von-Neumann based optical computing [22], optical technologies may have particular value in implementation of artificial neural networks (ANNs).

Artificial neural networks (ANNs) have been successfully implemented for various complex tasks including: image and pattern recognition, speech recognition, machine translation, and surpassing humans at strategy games [23]–[28]. Despite these strides in neuromorphic

computing, the hardware implementation of traditional ANNs have been limited by the fact that digital transistors (the basic computing unit of modern computers) simply do not behave in the same manner as the analog synapses found in the human brain. The human brain is the current target in low power, fault tolerant computation systems, as shown in Figure 1.3 [1], [29]. With this goal in mind, two main types of ANNs have emerged: deep neural networks (DNNs) and spiking neural networks (SNNs).

DNNs are more traditional neural networks and contain a large amount of complexity along with many layers. These networks are capable of supervised, semisupervised and unsupervised learning, and excel in tasks where large amounts of training data are available [30]. Contemporary commercial availability of powerful parallel computation devices like graphic processor units (GPUs) and field programmable gate arrays (FPGAs) has accelerated development and testing of the field of new learning algorithms and network structures.[31] At present, however, DNNs are fundamentally limited due to a lack of scalability. As problem complexity increases, DNNs require more and more computational resources to conduct training [32].

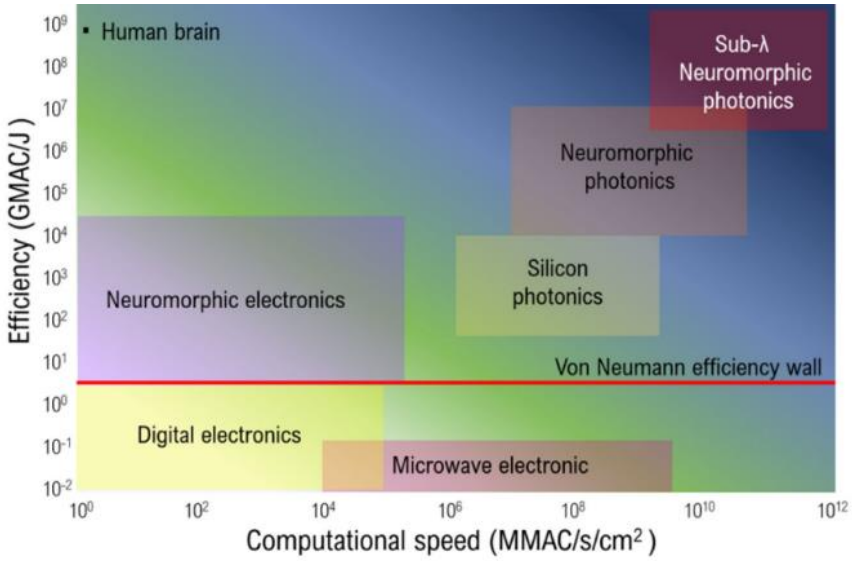


**Figure 1.3 - Comparison of computational efficency vs. speed for different computing systems. Reprinted from [1].**

In contrast, SNNs have attracted attention due to their close similarity to biological systems (namely the human brain). In SNNs the input signals are spikes, rather than the constant feed found in traditional DNN neurons. This spike-based signal system is widely believed to be one of the main reasons that the brain is so adept at sequence recognition and memory, although a full discussion of this is beyond the scope of this work [33]. Sequence recognition is an active development area in neuromorphic computing; therefore, devices capable of implementing spike-based computing are of great interest [34]. These devices enable systems to work with stimuli that are strongly timing dependent, such as speech recognition and image detection [35].

Although silicon photonic devices have been investigated due to their potential to exceed the limitations on traditional electronic devices, they are especially promising for neuromorphic and ANN applications because many of the effects used in photonic devices can be described in the framework of nonlinear dynamics. Initially established in 1985, it took some years for both photonics and neuroscience to advance beyond laboratory demonstrations to become broadly

applicable [36], [37]. Once established though, ANNs very quickly began producing results in hardware and algorithm developments [38]–[42]. Most excitingly, photonics based SNNs are also showing exceedingly promising results in terms of speed and information density [43]–[48].

Previously, photonic neuromorphic hardware applications were limited due to (1) difficulties in implementing optical memory and logic, and (2) the absence of photonic manufacturing industries [1]. However, implementation of phase change materials (PCMs) into different aspects of optical devices is frequently credited as a catalyst for recent advancements in photonics technology, enabling applications of photonic neuromorphic devices [49]. To understand the benefits offered with pairing PIC components with PCM, Chapter 2.0 will briefly review the history of PCMs, their operating principles and how PCMs have been integrated into PICs.

## 2.0 Phase Change Materials

PCM technology has been extensively developed within the optical data storage industry. While there were two main classes of disks at the advent of optical disk storage (magneto-optical and phase-change media), phase-change disks using PCMs became ubiquitous, finally being implemented in DVD and Blu-ray disks [50]. This level of maturity in understanding PCM optical properties and fabrication processes allowed researchers to readily begin integrating them into photonic devices [51], [52]. A PCM considered for nonvolatile photonic applications must have several key features, namely: high contrast in optical properties; high-speed phase transition; low phase-transition temperatures (without thermal disturbance around room temperatures); long term stability; and a large number of rewritable cycles [52]. $VO_2$ is a well-established phase change material with extensively documented properties, but its phase change is inherently volatile. Therefore this work mainly considers chalcogenide alloys, since both the crystalline and amorphous phases are stable at room temperature [52]. The Ge-Te-Sb ternary phase diagram is given in Figure 2.1, along with indications of milestone discoveries for PCM devices and compositions. In addition, some basic properties of popular PCMs are given in Table 1.

Chalcogenide alloy based PCMs (e.g., the well-known $Ge_2Sb_2Te_5$ (GST)), are characterized by their ability to rapidly and reversibly switch between amorphous and crystalline states. This process is illustrated in Figure 2.2. Crystalline PCMs can be amorphized (blue curve) by being heated above their melting temperature, and then being rapidly quenched, preventing any long-term order from forming. Long-term order can be reestablished through crystallization (red

**Table 1 – Common PCMs along with their optical properties and transformation temperatures. Reproduced from [53].**

| PCM | Complex R.I. (Am) | Complex R.I (Cr) | Transition Temp. | Volatile |
|---|---|---|---|---|
| **GST-225** | 4.6 + 0.18*i* | 7.2 + 1.9*i* | 600 ℃ | No |
| **$Sb_2S_3$** | 2.712 +0*i* | 3.308 + 0*i* | 270 ℃ | No |
| **$Sb_2Se_3$** | 3.285 + 0*i* | 4.050 + 0*i* | 200 ℃ | No |
| **GSST** | 3.325 + 0.00018*i* | 5.083 + 0.35*i* | 250 ℃ | No |
| **$VO_2$** | 2.75 0.4*i* | 2.1 + 1.3*i* | 68 ℃ | Yes |

curve) by heating the material up above its crystallization temperature and giving the atoms enough time to diffuse to the energetically favorable lattice sites, resulting in the crystalline phase.

Between the crystalline and amorphous states in PCMs, there is a large difference in optical properties resulting from the amount of vacancies in each phase. The vacancies inside the structure of Ge/Sb materials form *p-p* orbitals, which are very susceptible to local distortions. During amorphization, heat-induced lattice vibrations will cause misalignment of the *p-p* orbitals, reducing the number of resonant bonds in the material, which will significantly reduce the dielectric constant of the amorphous phase.

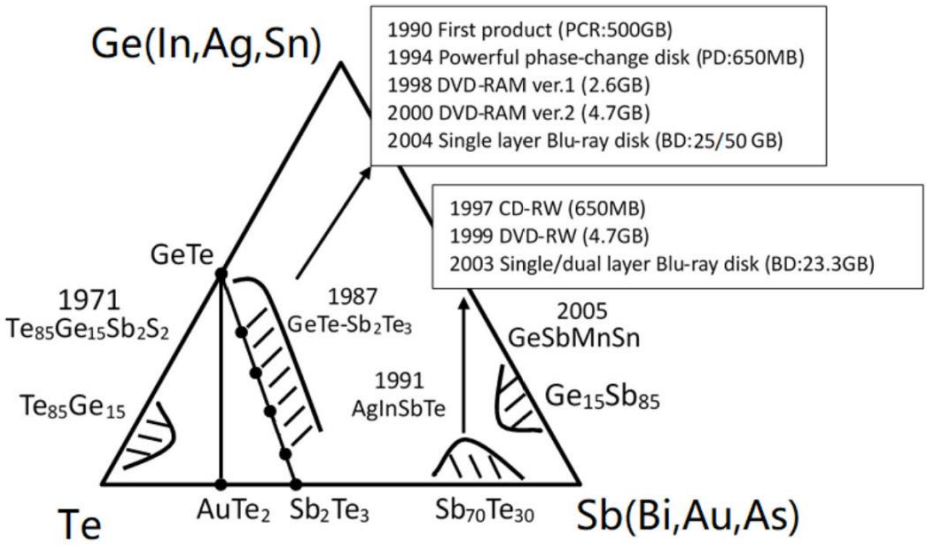


**Figure 2.1 - Ge-Te-Sb phase diagram. Insets show key dates of technological and compositional discoveries. Reprinted from [50].**

The controllable crystalline structure of PCMs provides a platform for development of PICs. PCMs can have several metastable crystalline phases, each with its own optical properties, possibly due to free carrier absorption caused by electron localization effects [52], [54], [55]. By controlling the amount and type of phases present in a PCM during operation, the optical properties can be precisely modulated, potentially enabling applications such as multi-level photonic memory devices and neuromorphic photonic computers [56]. By leveraging this, PCMs offer a promising solution for controlling both the amplitude and phase of light on-chip in a compact form factor [53], [57]. Integrating PCMs into primary optical devices has led to large improvements in performance and will be briefly discussed.

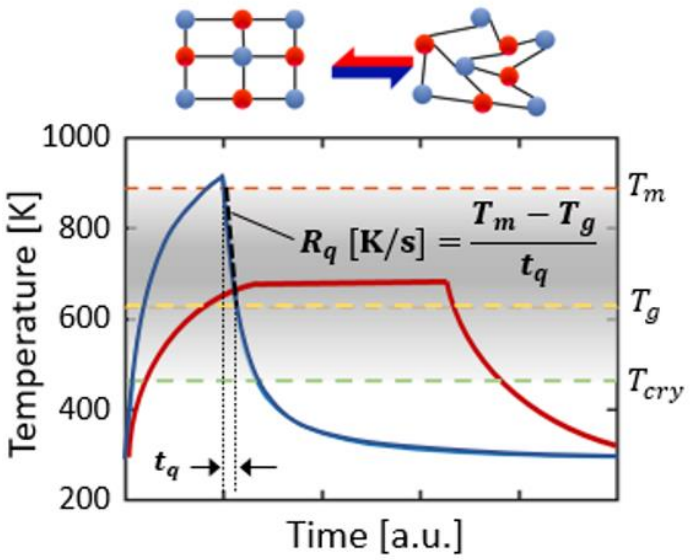


**Figure 2.2 - Example of PCM behaviors. Required thermal profiles for crystallization (red) and amorphization (blue).**

### 2.1.1 Directional Coupler

Directional couplers can reasonably be considered the most important building block for constructing photonic integrated circuits. When light is confined in a waveguide, it can be evanescently coupled to a nearby waveguide, splitting the power and signal into two coherent, but separate places [5], [58], [59]. This is typically done by bringing the two waveguides close enough together for a length that satisfies:

$$L > L_c = \frac{\pi}{\beta_s - \beta_a} \qquad \textbf{Equation 2-1}$$

where $L_c$ is the critical coupling length, and $\beta_s$ and $\beta_a$ are the symmetric and antisymmetric propagation constant values obtained from transfer matrix methods [58], [59]. Furthermore, the amount of signal transfer between the waveguides is dependent on the waveguide geometry,

separation distances, and signal wavelength and polarization [5]. Figure 2.3 gives the critical coupling length, $L_c$ calculated through effective index-based matrix methods (EIMM) and two-dimensional finite-difference time-domain (2D-FDTD) methods for both transverse electric (TE) and transverse magnetic (TM) polarizations, as a function of separation of two straight waveguides made of SU-8 [5].

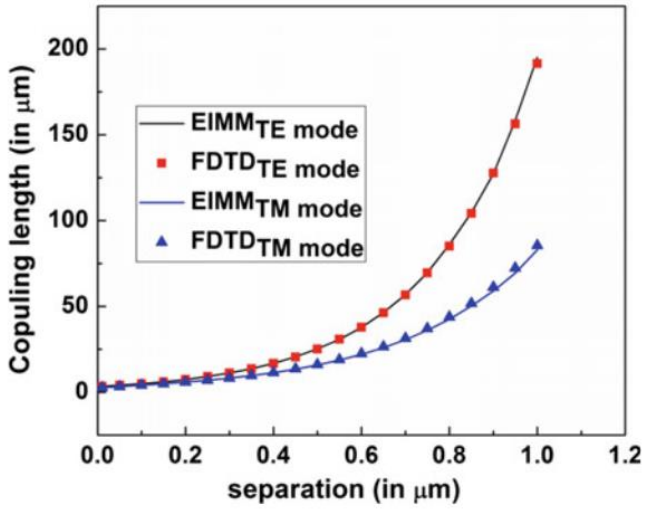


**Figure 2.3 – Critical coupling length vs. separation between waveguides. Calculations were performed through effective index-based matrix methods (EIMM) and two-dimensional finite-difference time-domain (2D-FDTD) methods for both transverse electric (TE) and transverse magnetic (TM) polarizations. Reprinted from [5].**

This coupling effect was first demonstrated on SOI wafers using ribbed Si waveguides in 1995 by Trinh, Yegnanarayanan and Jalali [60]. Their coupled waveguides, as shown in Figure 2.4, were able to operate with excess insertion losses as low as 1.9 dB. Historically, this development in the SOI platform enabled other developed photonics technologies to suddenly move from traditional laboratory-style implementations into PICs. SOI-platform active and passive optical components quickly became the backbone for subsequent development of PICs.

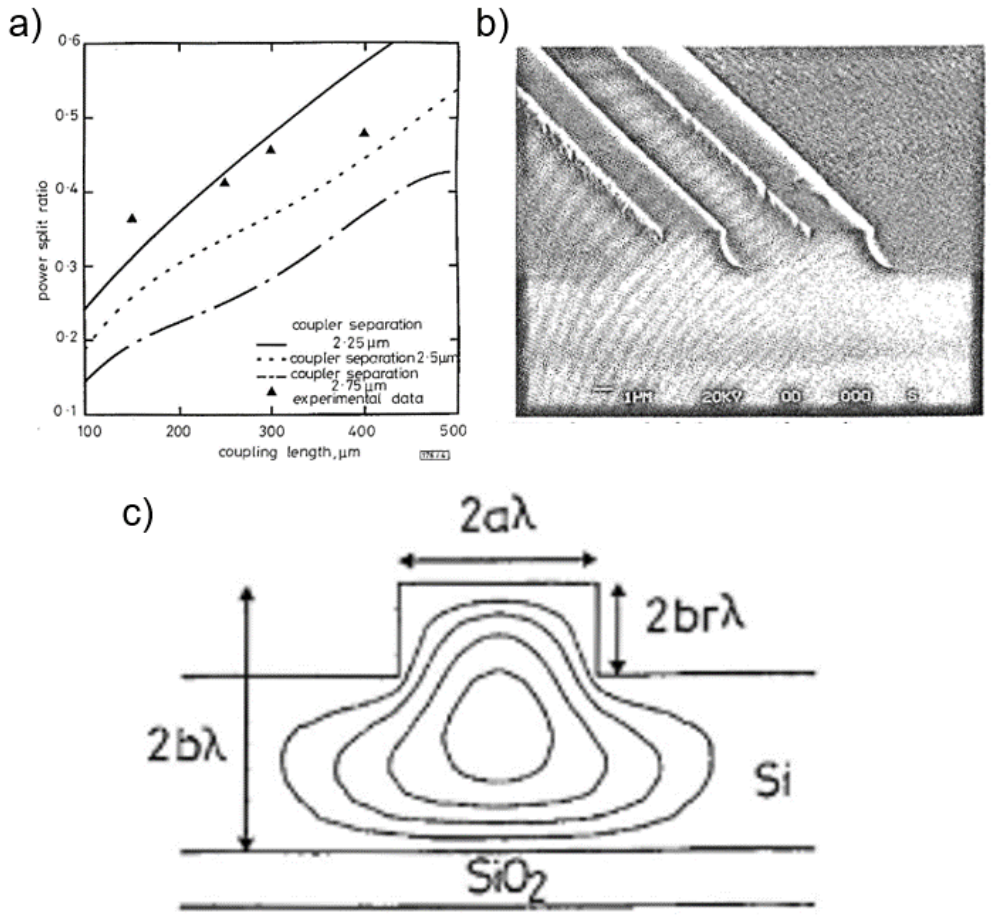


**Figure 2.4 – Initial demonstration of directional coupling in SOI platforms. (a) The power split ratio as a function of coupling length. (b) An SEM image of the coupled Si rib waveguides. (c) Schematic of the desired rib topology, complete with eigenmodes of the optical signal outlined. Reprinted from [60].**

While directional couplers are now an established technology and form the backbone of photonic circuitry, the ability to route light signals from one path to another for different operations is vital for building complex components. While such optical switches have been demonstrated in the past [61]–[63], they typically need large footprints, high power consumption, or both. While resonator-based switches have been proven to reduce footprint and power consumption [64]–[66], they are inherently highly sensitive to manufacturing defects and thermal fluctuations, rendering them difficult to control on the large scale. PCMs have been demonstrated to provide strong,

nonvolatile modulation to existing waveguides. When integrated on top of a potential switching location, the phase of the PCM determines which branch the output signal propagates down.

### 2.1.2 Mach-Zehnder Interferometer

Actively controlling the phase of an optical signal is fundamental for enabling complex calculations using optical devices. One of the basic ways of achieving this is through a Mach-Zehnder Interferometer (MZI). MZIs were first described in 1891 by Ludwig Zehnder, and then refined in 1892 by Ludwig Mach [68]. The MZI was initially formulated as a way to perform optical measurements, and has since proven very useful for measuring and identifying several facets of quantum mechanics [68]. In a basic MZI, a light beam is first split into two paths, and then recombined before arriving at a detector. Based on the relative phase acquired by the beams on their separate paths, the recombination will then transmit the beam at levels somewhere between 0 and 100% of its initially incoming power [68].

For basic waveguide-integrated MZIs, the path is typically split between two branches, with one containing an integrated PN diode. When the PN diode is forward biased, a large number of carriers will be injected into the optically active zone, and the refractive index of the branch will change as described by the plasma dispersion effect [68]. This change in refractive index causes the two branches to interfere when recombined, varying the output intensity of the device as a function of the signal applied to the PN diode branch. However, traditional MZIs are inherently volatile devices, requiring a constant power supply to operate [69]. While nonvolatile phase shifters have been achieved [70]–[72], they can suffer from high losses, poor scalability and a natural incompatibility with standard Si fabrication processes.

Controlling the phase of optical signals is required for a complete integrated optical device. While several different on-chip control mechanisms have been demonstrated, they typically suffer from large device footprints, large optical losses, or incompatibility with traditional semiconductor fabrication techniques [69]. While PCMs have potential for implementing phase modulation in photonic chips, traditional PCMs like GST can have large optical losses, making them difficult to incorporate efficiently. However, in recent years, low-loss PCMs have been developed [69], [74]–[78]. For example, $Sb_2Se_3$ integrated waveguides were measured to have 0.03 dB/μm at telecommunication wavelengths [69]. These types of integrated PCM devices offer nonvolatile solutions for phase modulation.

### 2.1.3 Tunable Ring Resonator

Although optical modulators were long established by the mid-2000s, existing prototypes were large structures, unsuited for PICs [64]. With this in mind, researchers began investigating light-confining resonating structures that would enhance the effect of a changing refractive index. Although at first these devices were demonstrated using an optical control signal, as will be discussed later, this construction is impractical for large scale device arrays [65]. These devices' transmission was highly sensitive to the signal wavelength, with drastically diminished transmission at wavelengths corresponding to integer multiples of the ring circumference. By tuning the effective refractive index of the resonance ring, the resonance wavelength could be changed, inducing strong modulation of the transmitted signal, as shown in Figure 2.5c.

In 2005, Xu et al. demonstrated an electrically driven ring resonator structure to modulate optical signals, as shown in Figure 2.5. Their device used an integrated PIN diode to inject carriers

into the ring, tuning the refractive index of the structure. Although PIN diodes are typically considered slow devices overall (with injection of carriers in a forward biased PIN diode occurring on the order of 10 ns), the resonating nature of their device removed the speed limitation [66]. When operated at high voltages, the optical transmission reaches saturation long before the electrical rise time, as the carrier concentrations meet the minimum carrier injection required to achieve modulation before the device is saturated with carriers.

This concept is distinct from traditional thinking where injected carriers are tuned to target the minimum carrier injection. Performance of these devices is also unlike the MZIs discussed previously, as operating waveguide integrated MZIs at higher voltages starts to strongly affect the optical transmission [66]. However, long forward biasing periods can lead to free carriers diffusing into the section of the ring that is not part of the PIN junction, leading to longer fall times (~1.5 ns) than typical fall times of reverse biased PN diodes (on the order of 10 ps) [66].

Although many types of optical switches and phase modulators have been developed as discussed previously, ring resonator structures offer some of the most promising results, due to their small device footprint and enhanced efficiency from optical resonances [79]. However, traditional PIN or PN based ring resonators require a constant power supply to maintain the switched state. By integrating PCMs into the device, a nonvolatile modulation mechanism is introduced [49]. This has been leveraged to utilize ring resonators into many complex optical devices, most notably optical switches. In addition, modern low-loss PCMs have successfully been implemented into such structures to further improve performances [80].

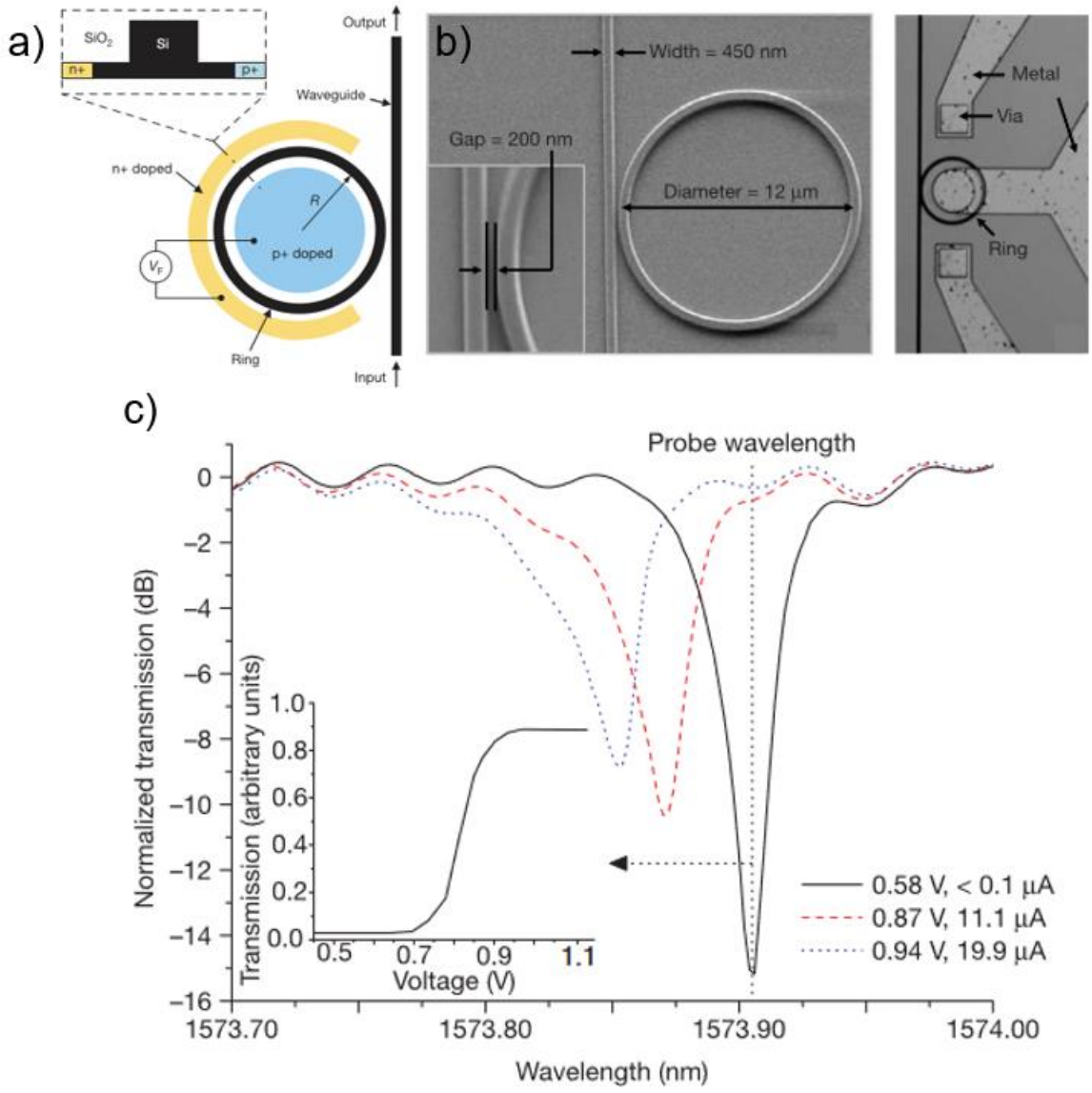


**Figure 2.5 - Electrically driven resonator ring. (a) Device schematic with inset showing the profile of the rib waveguide that makes up the ring. (b) SEM images of fabricated rings. (c) Wavelength specific resonsance of the ring structure. Reprinted from [64].**

### 2.1.4 Multiplexer/Demultiplexer

Multiplexers/Demultiplexers are key components in signal systems and have been used for centuries, first dating back to the days of telegraphs [81]. Their ability to either select one of many incoming signals and propagate it forward (multiplexing) or conversely, taking one input signal and sending it down one of multiple possible outputs (demultiplexing), allow multiple inputs to be combined into a single data stream. Typically, multiplexers are paired with demultiplexers in one device. This pairing is the backbone of modern signal transmission.

Although wavelength multiplexers were initially developed in the early 1990s, integrated waveguide multiplexers on SOI substrates were lagging in development, with the first 4-channel wavelength multiplexer being demonstrated by Trinh et al. in 1997 [82]. Their device, schematically shown in Figure 2.6, used two slab waveguide star couplers (a common optical device that distributes input signals uniformly along several output ports) which were connected by an array of waveguides with incrementally different pathlengths. Although integrated multiplexers like this have since been adapted and refined, crosstalk remains an issue, requiring new innovations as the amount of bandwidth needed for modern devices continues to increase.

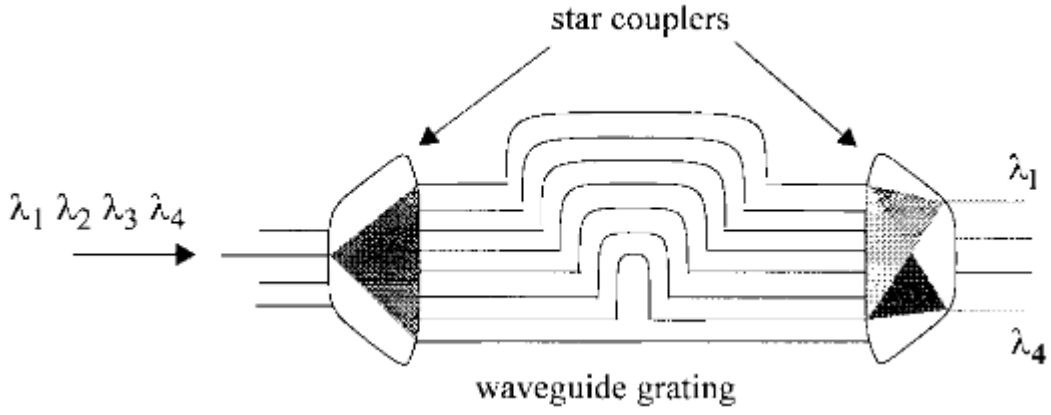


**Figure 2.6 - Schematic of the first 4-channel wavelength multiplexer. Reprinted from [82].**

PCMs have been integrated into optical devices to create both wavelength division multiplexing (WDM) and mode division multiplexing (MDW). Structures capable of addressing individual devices among large arrays of devices have been demonstrated [2], [83], [84]. In WDM, the phase of the PCM was used to selectively address a single unit in a 16 x 16 memory array [2]. Although still in their infancy, the high speed and ease of (de)multiplexing of optical memory devices offer massive gains in speed and efficiency over their electrical counterparts. While these advantages for WDM, as well as time division multiplexing (TDM), are exciting, they are rapidly approaching their theoretical Shannon limit [84]. With this in mind researchers have redirected their efforts towards MWD [84]. Since MWD utilizes differing orthogonal modes, each mode is independent, and more signals are able to utilize the same paths without interference [84]. A recent device was presented with 100 nm bandwidth that can accommodate 4 modes, the fundamental TE and TM modes, as well as the first TE and TM modes. This device utilizes GSST, and can switch between the four modes in just 10 μm [84]. These advances in (de)multiplexing pave the way towards more compact and higher informational density devices.

### 2.1.5 Light Sources and Detector

Light sources and detectors able to be integrated on-chip are also required to construct PICs. Pure crystalline Si does not have a direct bandgap, making the possibility of a traditional monolithic Si laser impossible. While novel Si based lasers are an active development area [66], [85], [86], commercially successful methods typically package external light generation solutions with PICs. SiN on SOI platforms provide another possible external light solution [87]. Although SiN has no useful active optical effects, it does have extremely low propagation losses. As a result, various

investigators have utilized SiN waveguide layers to route large scale light sources, coupling them and rerouting them into the specific SOI active devices as necessary, as depicted in Figure 2.7 [88].

Detectors are frequently constructed based on Si/Ge strained layer superlattices, which can be integrated into existing Si fabrication processes. The introduction of Ge atoms into a Si lattice through molecular beam epitaxy (MBE) converts the indirect bandgap of Si to a direct bandgap via Brillouin zone folding [89]. As early as 1974, it was predicted that the super-period imposed on the lattice of the host crystal could change the indirect character of the Si band structure [90]. This super-period will give rise to minizones that are not observed in the native host crystal. While the Brillouin zone dimensions shrink normal to the layers (in the direction of super lattice growth), its original size is maintained within the layers themselves. A specific period length of the super lattice can then be calculated and chosen such that the minimum of the conduction band is then folded back into the center of the Brillouin zone forming a direct band gap [89]. This process is illustrated in Figure 2.8.

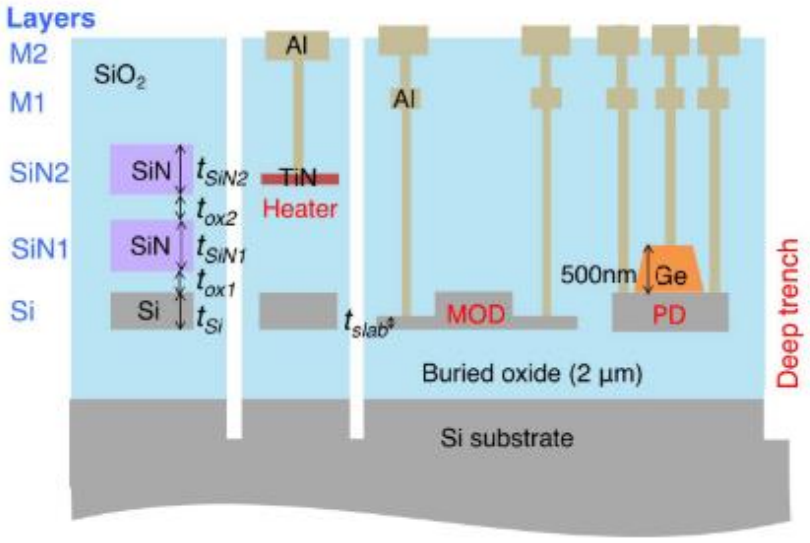


**Figure 2.7 - Cross section of a SiN on SOI platform. This multilayer platform contains SiN transport layers, integrated with active Si devices. Reprinted from [87].**

This effect was then leveraged to grow integrated photodetectors into Si waveguides [93]. In this initial structure, a thin layer (20 periods of 30 nm Si + 5 nm $Si_{0.55}Ge_{0.45}$) would be grown on top of a *p*-doped Si waveguide. This stack is then covered with a 100 nm undoped Si-buffer layer and finally a 50 nm thick n-doped Si contact layer. This reported structure was optimized via mode matching to maximize coupling between the waveguide and the photodetector while minimizing optical losses due to the contact layers. This structure was able to achieve bandwidths of up to 2 GHz while minimizing optical losses to below 1 dB/cm [93].

While strained Si-Ge semiconductor systems seem to be the most efficient way to offer on-chip photodetection, there have been investigations into PCMs' applicability for photoconductive applications such as photodetectors, displays and smart windows [57], [94]–[96]. Chalcogenide PCMs are low-bandgap semiconductors. Longstanding thinking suggests that photothermal effects, such as those that aid in crystallization in all-optical systems, dominate photoconductivity effects. This line of thinking is in stark contrast to other chalcogenide materials where photoconductivity effects dominate, which has made them the traditional bases for solar cells and image sensors [96], [97]. However, it has recently been observed that the relative contributions of the photoconductive and photothermal effects can be tuned in PCMs, opening the door to PCM-based photonic devices [96].

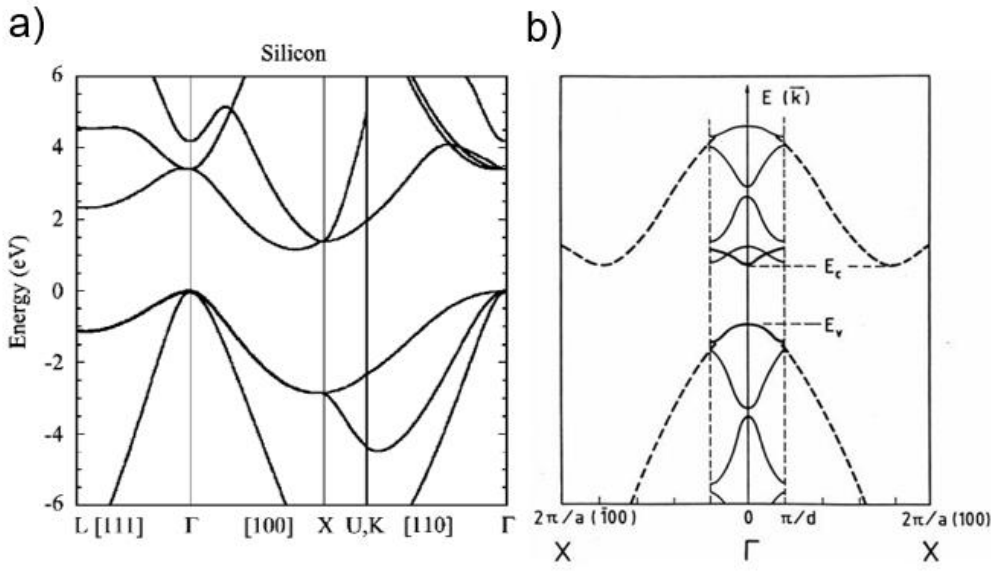


**Figure 2.8 – Example of Brillouin zone (BZ) folding. (a) An unstrained Si band structure compared with (b) BZ folding effect, which forms a direct bandgap. (a) Reprinted from [91], (b) reprinted from [92].**

PCMs are traditionally limited in two key aspects: (1) slow crystallization times and (2) high temperatures required for amorphization [98]. Limitation (1) is being addressed by the material design community through a search for suitable PCM alloys with high crystallization speeds [99]–[101]. The focus of the present work will be investigating and characterizing various PCM heater structures to increase efficiencies and elucidate how structure design influences overall device performance, mitigating issues stemming from limitation (2). Advanced control of the switching of PCMs can be achieved through both novel materials engineering methods, and highly controlled heating techniques [102]. While both techniques are currently prominent in research, this work will be focused on understanding and improving the heating methods of PCM based photonic devices. Integrated PCM photonic devices have thus far been categorized by two heating mechanisms: optical and electrical sources.

## 2.2 Optically Switching PCMs

Optical switching of PCMs offers unique benefits in speed and scalability. While lab-based devices can be initially characterized through external laser excitations [103], on-chip applications use write pulses that are confined to the waveguide itself, or in the nearfield limit [3], [4]. This type of writing removes the diffraction limit traditionally associated with optical heating and allows for aggressive scaling of these devices. These types of all-optical devices have been used to demonstrate arrays of memory devices [3], [103], and even an all-optical calculation apparatus [4].

While all-optical systems offer exciting possibilities for potential future devices, they also present their own unique challenges. As the number of photonic components increases, both generating and routing the optical control signals to individual devices becomes increasingly difficult. This is especially evident when addressing individual memory cells in large-scale arrays which requires either precise timing of overlapping pulses [4] or resonant components which limit device density, as they are extremely sensitive to outside perturbations [2], [3], [47]. Researchers have turned from optical to electrical switching of PCMs, since addressing individual devices in electrical systems is common practice and enables retention of the speed benefits offered by optical read signals.

## 2.3 Electrically Switching PCMs

Electrical control signals can be generated and routed to individual devices in a compact circuit using straightforward fabrication techniques, including multilevel interconnects. Developing a reliable, efficient, and high-speed electrical interface to control optical phase change devices is therefore highly desirable.

Electrically switching PCMs have generally been implemented through one of two distinct methods (illustrated by the generalized thermal circuit models shown in Figure 2.9a: (1) direct heating of the PCM, or (2) indirect heating using a nearby microheater. The direct method passes electrical current through the PCM itself, resulting in Joule heating which initiates the phase transition [104]–[107]. This approach can be fast and highly efficient (e.g., sub-nanosecond and <100 pJ switching has been demonstrated in electrical phase change memory cells [108]–[110]), but it is limited to switching volumes much smaller than the optical wavelength. This volumetric limitation is a result of localized conductive paths forming through the material during the crystallization process, creating a short circuit. When the two electrical contacts become shorted, current becomes localized to that region of the device making heating and further crystallization of other regions significantly less efficient. While this phenomenon can be addressed by reducing the optical mode volume through hybrid photonic-plasmonic device structures [111]–[114], reducing insertion loss remains an outstanding challenge for these devices.

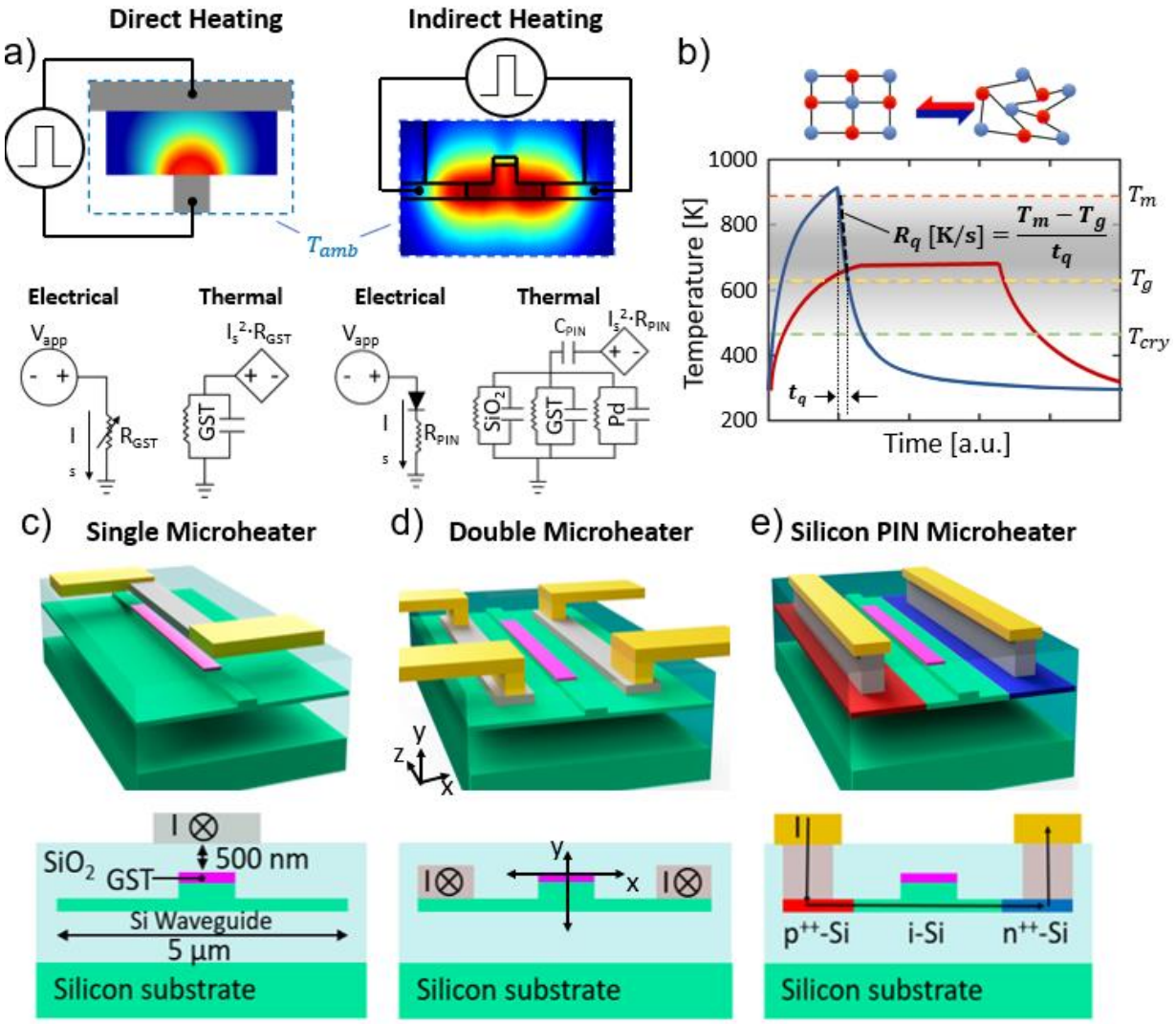


**Figure 2.9 - Comparison of direct vs. indirect switching of phase change devices, as well as heater structures studied in this work. (a) Example devices illustrating direct and indirect switching of phase change materials, along with electrical and thermal circuit models of each. (b) Illustration of annealing curves to achieve crystallization (red) and amorphization (blue) in GeTe-based phase change materials, along with an equation defining the quench rate, $R_q$, of the amorphization process. (c)-(e) 3D schematics and cross sections of the three devices simulated in this study.**

To reversibly switch larger volumes of material, it is necessary to use indirect heating which decouples the heating mechanism from the electrical conductance of the PCM. Indirect

heating also enables electrical switching of emerging optical PCMs (e.g., $Ge_2Sb_2Se_1Te_4$ [80], $Sb_2S_3$ [76], [115], and $Sb_2Se_3$ [116]), which have low electrical conductivity in both amorphous and crystalline states. Indirect electro-thermal switching using microheaters integrated close to the PCM layer has recently been investigated in the context of reconfigurable RF [117]–[120] and photonic switches [111], [121]–[126], but a comprehensive study of various design trade-offs has not been performed for the latter. For electrically switched phase change photonic devices, key performance metrics include optical insertion loss, switching speed, energy efficiency, and cycling endurance, which are often interdependent and require careful optimization. For example, reducing the programming pulse duration not only serves to improve the switching speed of phase change memory, but also reduces the programming energy [125]. However, shorter programming pulses require higher peak powers to reach the same transmission level and thus have the potential to cause greater thermal fatigue to the memory cell. Therefore, it is important to model the interaction of these various dynamics during the design of phase change photonic devices.

## 2.4 Research Goals and Approach

The goal of this work is to characterize different types of integrated heaters for Si rib waveguides: PIN diodes; PN diodes; and single-doping structures. Simulation studies have been conducted on PIN and PN diodes, as well as two types of external metallic heater designs. Work on single-doped structures has begun but expanding the existing models to correctly model high-field behaviors is currently outstanding, as will be discussed. These designs were modeled and are presented comparatively. The influence of various design aspects of each device on performance

were assessed through computational modeling and compared based on their heating efficiency. Efficiency comparison was accomplished through a well-established figure of merit [98], [127] as well as the optical signal loss for that type of structure. In addition, experimental studies have been conducted on PIN diodes and single-doping structures and will be presented in Section 4.0.

## 3.0 Initial FEA Model of Heater Structures

While there are many novel indirect heating structures being developed [125], [127], [128], not all of them are directly compatible with existing foundry processes for silicon integrated photonics. This work focuses on heaters that can be fabricated by existing foundry processes, enabling more straightforward integration into larger scale photonic circuits. The transient thermal response of the chosen device geometries is investigated to better understand design trade-offs of programming energy, switching time, and optical insertion loss. Three different microheater designs for electrically controlled phase change photonics were initially explored, specifically for amorphization, which is more technically challenging to achieve than crystallization [69], [79], [122], [123], [126], [129]–[131]. Amorphization requires the device to reach higher temperatures (e.g., the melting temperature, $T_m$, is ~900 K for GST [132]) and then cool (e.g., the glass-transition temperature, $T_G$, is ~625 K for GST [99]) with extremely fast quenching rates ($R_q = \frac{T_m - T_G}{t_q} \sim 10^9 - 10^{10}\ K/s$ for GST [133]) in order to "freeze" the atoms in the amorphous state, rather than the energetically-favorable crystalline state(s). Examples of both crystallization and amorphization thermal cycles are shown in Figure 2.9b, with the quenching rate of the material highlighted in the amorphization curve.

All heater designs explored in this work utilize a common silicon-on-insulator rib waveguide structure, encapsulated by 500 nm of $SiO_2$ (Figure 2.9c-e), which is one of the most common structures for photonic devices. Waveguide dimensions, phase change material thickness, and presences of an encapsulation layer are held constant throughout the first set of simulations to

**Table 2 - Novel heating structure performances for amorphization.**

| Microheater Design | Pulse Time | Switching Energy | Heater Size | Cell Size | Material |
|---|---|---|---|---|---|
| **Single-Doped Si [69]** | 400 [ns] | 7.39 [nJ/μm$^2$] | ~15.5 x 8.5 [μm$^2$] | 4 x 6 [μm$^2$] | $Sb_2Se_3$ |
| **ITO [128]** | 50 [ns] | ~1.67 [nJ/μm$^2$] | 2 x 3 [μm$^2$] | 2 x 3 [μm$^2$] | GST |
| **Graphene (Sim.) [127]** | 0.22 [ns] | 2.4 [pJ/μm$^2$] | ~1.4 x 5 [μm$^2$] | 0.5 x 5 [μm$^2$] | GST |
| **Graphene (Exp.) [125]** | 5 [μs] | 3.59 [nJ/μm$^2$] | 10 x 5 [μm$^2$] | 3 x 4 [μm$^2$] | GSST |

enable a direct comparison of the thermal response between different designs (i.e., consistent thermal mass). The specific dimensions of these devices are shown in Figure 3.1. To account for thermal dissipation along the length of the silicon waveguide, each device's waveguide structure beyond the heater area is extended in the direction of propagation, for a total device length of 50 μm. The active area of each microheater is located in the center of the device. The microheater is 5 μm long with a corresponding 5-μm-long layer of PCM on top of the rib. Thin-film Si properties [134], [135] are applied to the waveguide structure while the underlying Si substrate (10 μm thick) is modeled as a bulk material, with its bottom face held at constant room temperature ($T$ = 293.15 K). The PCM used in this work was chosen to be GST, as its well-characterized material properties make it a common choice for these types of devices [126], [136].

Since all three devices use an electro-thermal design, these results can be generalized to any optical PCM provided a candidate PCM's amorphization temperature and melt-quench rate for reversible switching are considered during design of a particular heater [133]. The GST used in this work was modeled using material properties as reported in [126]. Palladium (Pd) contacts were chosen due to their high melting temperature and the availability of experimental data for Pd/Si thermal systems [137]. Further details on the material properties used can be found in Figure 3.1 and Table 3. It is worth reiterating that this area of investigation focused only on optimization

of the amorphization (reset) process in the PCM, and that this particular modeling process provides no insight into crystallization processes.

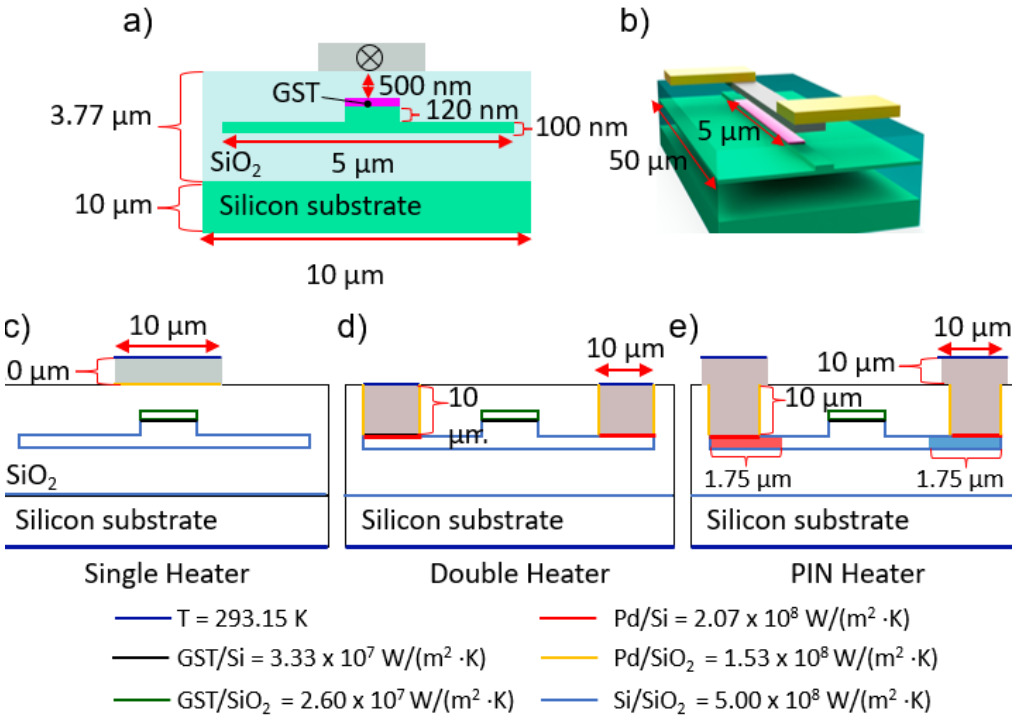


**Figure 3.1 – Details on simulated structures used in these studies. (a)-(b) Dimensions of aspects used in all 3 devices, (c)-(e) specific dimensions of each device studied in this work. In addition, thermal boundary conductance of each material pair present in this model is highlighted.**

Thermal performance of the three designs was assessed in COMSOL Multiphysics® [138] using the Heat Transfer Module. Conduction was the dominant heat transfer mode, as both convection and radiation proved to have minimal contribution for these structures at the time scales considered. The AC Circuits Module was used for both metallic heater devices and the Semiconductor Module was used for the PIN diode heater. The two metallic heater designs utilize an electro-thermal model coupled through Joule heating and temperature-dependent material properties. Joule heating occurs from charge carriers dissipating energy within the atomic structure of the material, and is calculated through the well-established equation:

$$P_{Joule} = \vec{J} \cdot \vec{E}$$ **Equation 3-1**

This is most focused in areas of devices with the lowest cross-sectional areas normal to current flow. Our metallic heaters are designed such that these occur as close to the PCM as possible.

The PIN microheater uses a 2D semiconductor-thermal model which is coupled through temperature-dependent material properties, semiconductor effects and Joule heating to calculate the dynamic heating profile of the device. While heating will occur mostly in areas of smallest cross-sectional areas as described above, other heating effects arise due to changing cross sectional area through the device, and recombination of carriers at the edges of the intrinsic region.

All 3D models simulated (both metallic heaters and the imported 3D PIN diode heater) utilized free tetrahedral meshes, calibrated for heat transfer using COMSOL proprietary settings. These meshes were then further refined using COMSOL's adaptive mesh refinement method. The 2D semiconductor-thermal model utilized free quadratic meshing elements calibrated for semiconductor physics using COMSOL proprietary settings. Mesh size for the waveguide and $SiO_2$ encapsulation layers were then manually refined through an iterative solving process, until solution stability was achieved, even with increasing mesh refinement. The quadratic meshing elements for the Si substrate was exponentially distributed from the $SiO_2$/Si interface. All models were solved using multifrontal massively parallel sparse (MUMPS) direct solver techniques.

**Table 3 – Material thermal properties used in the model.**

| **Material** | $\boldsymbol{k}$ **[W/(m*K)]** | $\boldsymbol{Cp}$ **[J/(kg*K)]** | $\boldsymbol{\rho}$ **[kg/m^3]** |
|---|---|---|---|
| **Si (thin film)** | $k(T)$ from [134] | $Cp(T)$ from [135] | 2329 |
| **$SiO_2$** | $k(T)$ from COMSOL | $Cp(T)$ from COMSOL | 2200 |
| **Pd** | 11.3 | 244 | 12023 |
| **GST [126]** | 0.19 | 199 | 6270 |

## 3.1 Metallic Heaters

The first design investigated is the most straightforward electro-thermal solution: a Pd metallic resistive microheater deposited on top of the $SiO_2$ encapsulation layer. As shown in Figure 3.1c, voltage is applied across the single metal heater and the resulting current heats the device through Joule heating. The heat generated at the microheater is then conducted through the $SiO_2$ encapsulation layer and into the PCM beneath. The 500 nm of encapsulating $SiO_2$ was chosen to minimize the optical insertion loss due to the metal while keeping the vertical distance between the heater and PCM as small as possible (i.e., promoting temperature rise in the PCM). While this design is simple to fabricate, the low thermal conductivity of $SiO_2$ and the distance between the heat source and PCM results in a device with a problematically large thermal capacitance and a slow thermal response (see Figure 3.2a).

To improve thermal capacitance and response time, a second device was explored which uses two Pd metallic microheaters embedded in the $SiO_2$ and in thermal contact with the Si waveguide as shown in Figure 2.9d. The heat generated by these two heaters is able to flow through the additional pathway of the partially etched silicon layer, which has a much higher thermal conductance than $SiO_2$ (~60 vs. 1 W/(m·K) at room temperature [99], [138]), resulting in faster heating as seen in Figure 3.2b.

Using the above-described methods, all devices were simulated to predict the switching dynamics which are shown in Figure 3.2a-c. In these simulations, the volume average of a 500 nm × 500 nm region of the PCM at the device center is measured (dashed outline in Figure 3.2g-i) to determine the switching threshold for amorphization. The input electrical characteristics required to reach the melting temperature of PCM were determined for each device through an iterative

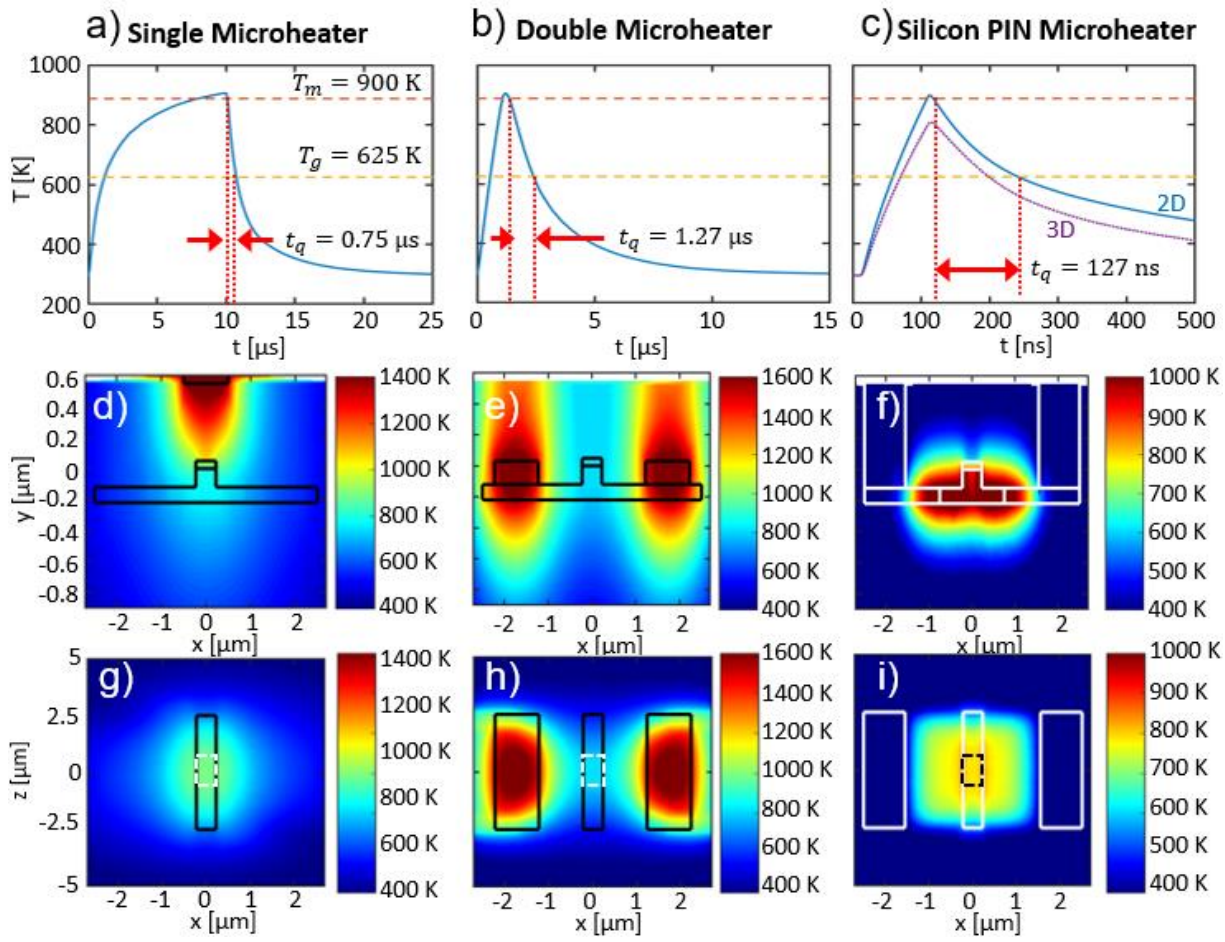


**Figure 3.2 – Initial results of the COMSOL simulations. (a)-(c) Heating curves of the three simulated structures. Both the melting (orange) and glass (yellow) transition temperatures ($T_m$ and $T_g$, respectively) of the PCM are marked, as well as the quench time, $t_q$. Plot in c) also highlights the difference between 2D (blue) and 3D (purple) models where the reduced temperature is due to heat dissipation along the waveguide in the direction of propagation. (d)-(f) Cross section snapshots of the simulated structures at peak GST temperature. (g)-(i) Temperature profile of the 3D models at the midway point of the GST to highlight the uniformity of the heating for the 5-µm-long PCM. Note: the slight asymmetry in g) is caused by additional heatsinking from the opposing metal contacts in Figure 2.9c.**

simulation process. The single microheater required a 302 mV pulse (19 mW peak power) for 10 µs and the double microheater required a 460 mV pulse (85 mW peak power) for 1 µs. All pulses were applied at $t$ = 10 ns. The electrical pulse amplitudes and durations were chosen to ensure that

**Table 4 - Common PCM thermal properties.**

| Material | $T_g$ [K] | $T_m$ [K] | Quench Rate [K/s] |
|---|---|---|---|
| **GeTe** | 418 [139] | 998 [140] | ~$10^9$ [140] |
| **$Sb_2Te_3$** | 350 [139] | 890 [141] | ~$10^{10}$ [142] |
| **$Sb_2S_3$** | 573 [76] | 819 [76] | ~$10^9$ [143] |
| **$Sb_2Se_3$** | 442 [144] | 893 [69] | ~$10^9$ [69] |
| **$Ge_2Sb_2Te_5$** | 625 [99] | 900 [132] | ~$10^9$ [133] |
| **$Ge_2Sb_2Se_1Te_4$** | 523 [145] | 900 [145] | ~$10^8$ [125] |

the center of the PCM exceeded $T_m$ while the Pd and Si did not exceed their melting temperatures (1825 K and 1685 K, respectively [146], [147]).

Snapshots of the cross-sectional thermal profile of the devices at the end of each programming pulse are shown in Figure 3.2d-f. After heating, the time required for the PCM to cool from the melting temperature to the glass transition temperature was also calculated for each design (for the GST used in this work the glass transition temperature, $T_g$, is set at 625 K due to fast heating rate effects [99]). This quench time, $t_q$, allows us to estimate the melt-quench rate in our devices: $R_q = \frac{T_m - T_g}{t_q}$. The resulting melt-quench rate must be greater than the critical cooling rate for amorphization of the PCM in question [133], [148] (~$10^9$ K/s for our GST [136], [149]) as mentioned previously. Thus, the maximum melt-quench rate of the electro-thermal microheater will determine which PCMs can be reversibly switched. Various PCMs and their relevant thermal properties are listed in Table 4 to provide a guide for future microheater designs. Differing values of $T_g$ and $T_m$ reported in the literature arise due to variations in materials thickness, dimensions,

and nanostructures. All of these factors would impact quench rates for the specific material configurations reported. To enable a reasonable comparison between the various literature descriptions of PCMs, $t_q$ is estimated from the minimum duration of the programming pulse during the rapid quenching process [69], [125], [133], [140], [142], [143].

## 3.2 PIN Diode

The third and final device investigated uses a waveguide-integrated PIN diode, as shown in Figure 2.9e. This Si PIN diode serves as the microheater when forward biased [126]. Voltage is applied to the source-drain contacts of the PIN junction and current flows perpendicular to the optical path through the diode. By using the waveguide itself as the heater, the thermal capacitance of the device is much lower than the first two designs, which is expected to result in much faster GST heating and cooling rates. The 1.5-µm-long internal intrinsic region used here ensures minimal optical loss through the switching region. Both the *p*- and *n*-type regions of the Si rib are doped at $\mathbf{10^{20}\ cm^{-3}}$, to ensure ohmic contacts with the metal and to increase the forward-biased current. The influence of intrinsic width and *p*- and *n*-doping levels in this PIN heater are explored in later sections.

Due to high doping levels in the PIN diode, full Fermi-Dirac carrier statistics are used to model the carrier concentrations of this degenerately doped semiconductor system. In addition, to investigate the change in carrier mobilities in the different regions of the diode under operation, the Arora, Fletcher, and Caughey-Thomas mobility models were used to account for

carrier-carrier, high field velocity, and phonon and impurity scattering effects, respectively [150]–[152]. These mobility models are explored briefly in the following sections:

### 3.2.1 Arora Mobility Model

The Arora mobility model is an empirically derived formula that takes into account phonon-carrier scatterings due to temperature effects, as well as lattice-carrier scatterings due to impurities [152]. Classical theory was able to accurately calculate the mobility of devices for doping concentrations of up to $10^{19}$ $cm^{-3}$ and temperatures of up to 500 K, but does not hold for higher dopings and higher temperatures. Arora et al. took classically calculated values as well as experimentally measured values at higher doping/temperatures and fit them to a well-established equation [153]:

$$\mu_{Ar} = \mu_{min} + \frac{\mu_o}{1 + \left(\frac{N}{N_o}\right)^{\alpha}} \qquad \textbf{Equation 3-2}$$

where the constants $\mu_{min}, \mu_o, \alpha$ and $N_{ref}$ are material-specific. To account for temperature effects, these constants scale accordingly with:

$$X = X^{ref}\left(\frac{T}{T_{ref}}\right)^{\beta_X} \qquad \textbf{Equation 3-3}$$

where $X = \mu_{min}, \mu_o, N_o, \alpha$

These values for Si are given in the original work [152] and are used commonly in the field [126], [127].

### 3.2.2 Fletcher Mobility Model

The Fletcher mobility model considers carrier-carrier scattering effects. It is based on classically derived expressions for mutual diffusion of two groups of charged particles, assuming an isotropic effective mass for both holes and electrons [150]. This carrier-carrier mobility effect is calculated:

$$\mu_{Fl} = \frac{\left(\frac{T}{T_{ref}}\right)^{\frac{3}{2}} F_1}{(np)^{\frac{1}{2}} \cdot \ln\left(1 + \left(\frac{T}{T_{ref}}\right)^{2} (np)^{-\frac{1}{3}} \cdot F_2\right)} \qquad \textbf{Equation 3-4}$$

where $n$ and $p$ are the electron and hole concentrations, respectively, and $F_1, F_2$, and $T_{ref}$ are material specific parameters, and for Si they are taken from [154]. This addition to the carrier mobilities is then taken into account through Matthiessen's rule:

$$\frac{1}{\mu_i} = \frac{1}{\mu_{o,i}} + \frac{1}{\mu_{cc}}, i = n, p \qquad \textbf{Equation 3-5}$$

where $\mu_o$ is the initial mobility (input mobility). While both the calculation of $\mu_{cc}$ and Matthiessen's rule are just first order approximations, more rigorous quantum mechanical derivations and comparison to experimental results have proven the validity of this model [155], [156].

### 3.2.3 Caughey-Thomas Mobility Model

Caughey-Thomas mobility models are used to consider high electric field scattering effects. Although this model was originally empirically derived in 1967 by Caughey and Thomas [153], it was further extended and verified by Canali et al. in 1974 for higher fields and constant

temperatures, and that extended form is used in this work [151]. The effect of high-field scatterings is applied to the mobility through:

$$\mu_{i,ct} = \frac{\mu_{i,o}}{\left(1 + \left(\frac{\mu_{i,o} F_i}{v_{i,sat}}\right)^{\alpha_i}\right)^{\frac{1}{\alpha_i}}}, i = n, p \qquad \textbf{Equation 3-6}$$

where $\mu_{i,o}$ is the initial mobility (input mobility) and $F_i$ is the component of the electric field parallel to the carrier current. $v_{i,sat}$ and $\alpha_i$ scale with temperature similar to the Fletcher model described above (or rather, the Fletcher model scales similarly to these as it is partially based off the Caughey-Thomas method) such:

$$X_i = X_{i,o}\left(\frac{T}{T_{ref}}\right)^{\beta_{X,i}}, X = \alpha, v_{sat} \qquad \textbf{Equation 3-7}$$

and $\alpha_{i,o}, v_{i,o}$ and $\beta_{X,i}$ are all measured material parameters, given in [151].

### 3.2.4 Total Mobility Used

The total effects from these scatterings were then incorporated by calculating $\mu_{ct}(\mu_{FI}(\mu_{Ar}))$ and using the resulting mobility as the carrier mobilities. For initial model simplicity, these calculations were performed and then used as constant mobility values of their respective region and can be found in Table 5.

**Table 5 - Material mobility properties used in the model.**

| **Doping = $10^{17}$** | $\mu_n$ [cm$^2$/(V·s)] | $\mu_p$ [cm$^2$/(V·s)] |
|---|---|---|
| **P** | 235 | 165 |
| **I** | 215 | 162 |
| **N** | 250 | 175 |

| **Doping = $10^{18}$** | $\mu_n$ [cm$^2$/(V·s)] | $\mu_p$ [cm$^2$/(V·s)] |
|---|---|---|
| **P** | 75 | 60 |
| **I** | 45 | 42 |
| **N** | 62 | 52 |

| **Doping = $10^{19}$** | $\mu_n$ [cm$^2$/(V·s)] | $\mu_p$ [cm$^2$/(V·s)] |
|---|---|---|
| **P** | 25 | 20 |
| **I** | 27 | 25 |
| **N** | 22 | 18 |

| **Doping = $10^{20}$** | $\mu_n$ [cm$^2$/(V·s)] | $\mu_p$ [cm$^2$/(V·s)] |
|---|---|---|
| **P** | 14 | 12 |
| **I** | 20 | 18 |
| **N** | 16 | 14 |

### 3.2.5 Out-of-Plane Heat Flux

Finally, to investigate how the heat flow along the waveguide affects these devices, the full thermal profile of the 3D devices is estimated. Heat generation at each linear position in the 2D PIN device ($\boldsymbol{Q_{tot}}\ (\boldsymbol{x}, \boldsymbol{t})$) is applied to a 3D device model, enabling the full thermal profile to be solved using the heat transport module. This approximation assumes that *y*- and *z*-components of the current through this device are minimal, and accordingly the 2D results for heat generation can be extended uniformly along the 5-µm-long active region. The PIN heater utilized a 6.2 V pulse driving pulse for 100 ns (160 mW peak power, also applied at $t$ = 10 ns) without exceeding the melting temperatures of the Si waveguide or Pd contacts.

All three designs were able to heat the PCM above $T_m$ = 900 K, although the PIN microheater showed much faster operating speeds. After analyzing the results from the 3D model, it is evident that heat spread along the waveguide plays a significant role in the thermal response. The peak temperature of the PCM dropped to 800 K, as shown by the dashed line in Figure 3.2c. This implies that a slightly higher power programming signal than predicted by the simpler 2D

model is needed for a real device, a conclusion which agrees with values reported in the literature (i.e., 6.6 V pulse for 100 ns reported in [126]).

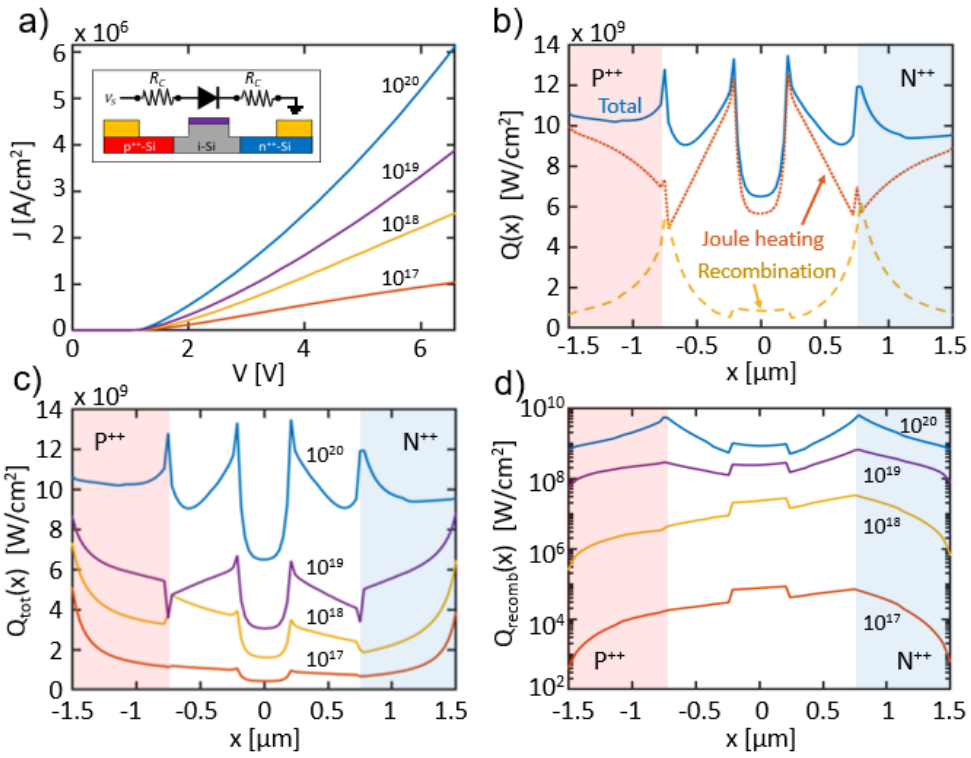


**Figure 3.3 – Comparison of different doping levels in PIN structures. (a) Current-voltage curves for the PIN diode with different p- and n-type doping levels. Higher doping reduces series resistance and increases carrier injection into the intrinsic region. (b) Heat per unit area, *Q(x)*, generated by the PIN microheater (p- and n-doping levels are $10^{20}$ cm$^{-3}$). Contributions from Joule heating (orange line) and carrier recombination (yellow line) are also shown. (c) Influence of doping on the total heat generated through the diode, $Q_{tot}$. (d) Heat generated due to carrier recombination, $Q_{recomb}$, for the curves in (c).**

The drastic reduction in switching energy for the PIN diode is due to the much smaller volume of material being heated as shown in Figure 3.2. Under forward bias, majority carriers from both of the degenerately doped regions ($N_A = N_D = 10^{20}\ cm^{-3}$) are injected into the intrinsic region, resulting in a high level of current being driven through the device, as depicted in Figure 3.3a [157]. This usually results in heat profiles centered around the intrinsic region only,

however for this device scale, the intrinsic region length is comparable to that of the doping region, and due to this the heat generated by each of the three regions needs to be considered. The effect of intrinsic region length is discussed in the following section.

When the PIN microheater is forward biased, the resistance of the doped regions is comparable to the resistance in the center intrinsic region due to charge injection. This is demonstrated by the following relation for a semiconductor's conductance:

$$\sigma = q(\mu_n\, n + \mu_p\, p) \qquad \textbf{Equation 3-8}$$

where $q$ is the elementary charge constant, μ is the mobility in that region and $n$ and $p$ are the carrier concentrations. More specifically in PIN diodes, the current is due to majority carriers as mentioned previously so Equation 3-8 can be written for the different regions:

$$\sigma_p = q(\mu_{p,p}\, p_p) \qquad \textbf{Equation 3-9}$$

$$\sigma_i = q(\mu_{n,i} + \mu_{p,i})n \qquad \textbf{Equation 3-10}$$

$$\sigma_n = q(\mu_{n,n}\, n_n) \qquad \textbf{Equation 3-11}$$

where the mobilities of the carriers in the different regions are designated by their subscripts (e.g., the mobility of holes in the *p*-region is denoted: $\mu_{p,p}$). In the intrinsic region, $p = n$ in order to satisfy charge neutrality. It is worth noting that each of these parameters are dependent on the voltage applied to the device, which requires a self-consistent solution. The carrier profiles through the device while forward biased are shown in Figure 3.4 and the mobilities used are found in Table 5 for an applied voltage of 6.2 V. Note that the levels of injected carriers into the intrinsic region are much larger than the intrinsic concentration, meaning this device is operating under high injection conditions [158]. This also causes carrier-carrier scattering to have a significant impact

on carrier mobilities in the intrinsic region. Since all three regions have comparable carrier concentrations and mobilities, heat should be generated relatively uniformly throughout the device. This can be confirmed through inspection of the band energy diagrams in Figure 3.4. A consistent voltage drop is observed across the region between the contacts, not only in the intrinsic region. This is an important observation as the heat generated by the doped regions of the device must be considered when calculating the cooling rate. In fact, this heating can be higher than that in the intrinsic region as shown in Figure 3.3b. This additional heat generation could contribute to slower quenching rates of PCMs, as well as lower energy efficiency due to the delocalization of the heating region. This consideration opens the door for further optimization in the design of next generation of electro-thermal heaters.

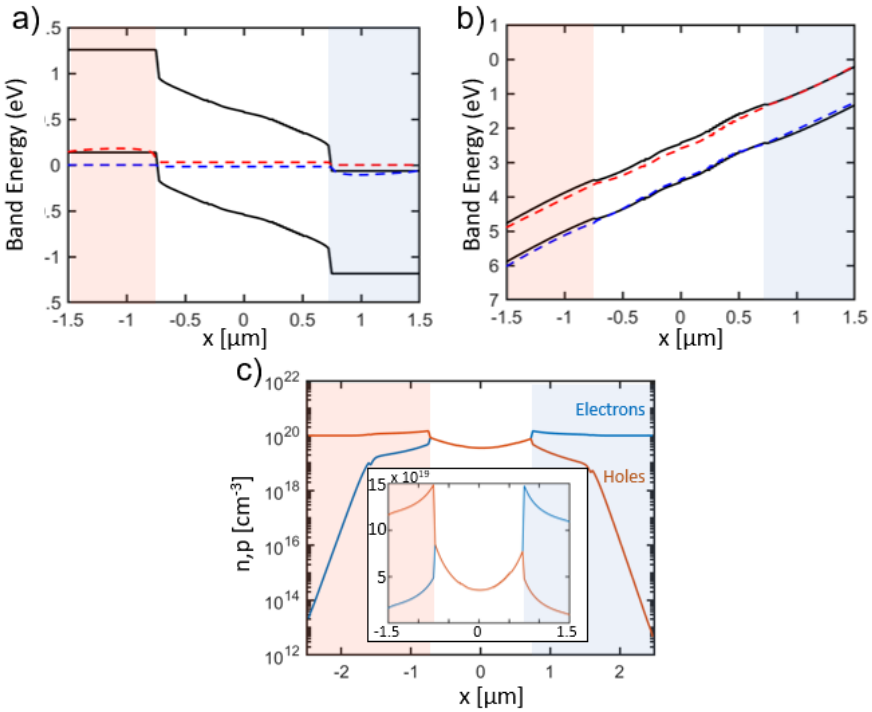


**Figure 3.4 - Operating dynamics of PIN diode with degenerate doping. (a)-(b) show the OFF/ON band diagrams for our device at $V_{app}$ = 6.2 V, (c) gives the electron/hole concentration through the diode while ON. Inset highlights the areas between the contacts, specifically the current crowding at the P/I and I/N interfaces.**

The heat generated per unit area by the PIN microheater normalized by thickness of the silicon waveguide is shown in Figure 3.3b. To elucidate the source of heating, we plot both the contributions due to Joule heating and carrier recombination in Figure 3.3b. There are noticeable peaks in heat generation at the interfaces from carrier-carrier recombination (yellow dashed line). There is also a significant amount of Joule heating generated by current crowding at either edge of the rib shown by peaks seen at ±0.225 μm, further adding to the amount of heat generated. When fabricating real devices, the location of maximum heating may change due to current crowding or large contact resistance between the silicon and Pd contacts [159]. These geometrical and material effects (intrinsic region width, doping levels) comprise a family of design parameters that can be investigated and optimized to further improve the efficiency and operating speed of these PIN heaters.

## 3.3 Doping Levels

To investigate the influence of doping on the device performance, the PIN microheater was simulated at different doping levels (with adjusted mobility values). However, as can be seen in Figure 3.3a, lowering the doping level decreases the amount of current generated, transitively decreasing the amount of heat generated. Much higher and/or longer-duration input pulses are therefore required to heat the PCM to the desired temperature, unacceptably lowering the energy efficiency of the device. Additionally, lowering the doping drastically reduces the amount of recombination in the device, which is proportional to the product of carriers in the intrinsic region, np. Thus, reducing the doping in the *n*- and *p*-regions leads to significantly lower recombination

heating rates (Figure 3.3d), as well as lower total heating (Figure 3.3c). For these simulations, ohmic contacts to the *n*- and *p*-regions were assumed regardless of doping level.

## 3.4 Intrinsic Region Length

It is well established that the length of the middle intrinsic region inside a PIN diode has an influence on the forward-biased current-voltage (J-V) curves for high injection conditions, so varying the length of the device used here results in different thermal behaviors [150], [158], [160]–[166]. As opposed to simple PN diodes, the middle intrinsic region of a PIN diode strongly controls the device's on-resistance. When the device is forward biased, majority carriers from both the *p*- and *n*-doped regions are injected into the intrinsic region, strongly modulating the conductivity of the device. The amount of carriers injected into the inner region is therefore a key parameter in designing these devices and, as will be demonstrated, is strongly influenced by the width of the region. The inner intrinsic region length is not only important to the transmission of the optical signal, but will also dictate the device's electrical and heating performance.

### 3.4.1 Carrier Distribution Through a PIN Diode

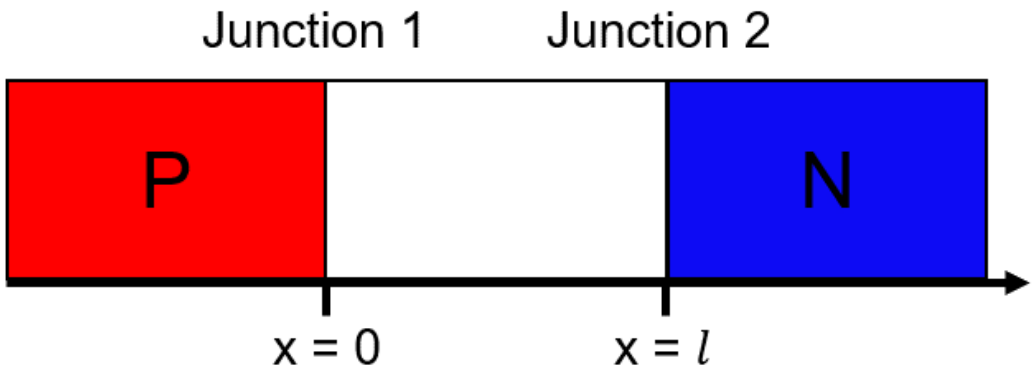


**Figure 3.5 - Theoretical PIN diode schematic for derivation of the carrier distribution.**

To determine the effect of the inner intrinsic region length, consider a two-dimensional PIN diode with an inner intrinsic length $l$, as described in Figure 3.5. Assumptions typically used in the literature will be followed, specifically from Berz [161]:

1. High injection in the intrinsic region.
2. Constant carrier lifetimes in the intrinsic region.
3. The values of the diffusion and mobility of the carriers is constant throughout the intrinsic region.
4. There are constant quasi-Fermi levels across the P/I and I/N junctions.
5. The recombination currents in the doped *p*- and *n*-regions is proportional to the square of the carrier density at the P/I (junction 1) and I/N (junction 2) interfaces.

Assumption 1 is proven true through examination of the injected carrier levels ($10^{20}$ $cm^{-3}$) when compared to the intrinsic carrier levels in the lightly doped intrinsic region ($10^{13}$ $cm^{-3}$). Assumption 2 is valid under high injection conditions when recombination centers are uniformly distributed through the intrinsic region, which is true for our computational model. Assumption 3

has been proven to be a valid first order approximation, and as such is still used in the initial model [158], [161]. Assumption 4 is held true for this derivation but is calculated more explicitly using Fermi-Dirac statistics in our computer model**.** Assumption 5 is fully justified for abrupt-junction devices with low injection levels at the opposite end of the intrinsic regions (junction 1 for electrons, junction 2 for holes).

In high-injection conditions, the current density for both electrons and holes can be derived through continuity expressions [167] :

$$J_n(x) = \frac{b}{1+b} I + eD\left(\frac{dn}{dx}\right) \qquad \textbf{Equation 3-12}$$

$$J_p(x) = \frac{1}{1+b} I - eD\left(\frac{dn}{dx}\right) \qquad \textbf{Equation 3-13}$$

where $I$ is the total current, $b = \mu_n/\mu_p$, $D$ is the ambipolar diffusion constant:

$$D = \frac{2D_n D_p}{D_n + D_p} \qquad \textbf{Equation 3-14}$$

and further noting that due to conservation of electrical neutrality $n(x) = p(x)$ in the intrinsic region. By then considering current continuity through the equation

$$\frac{dJ_{n(p)}}{dx} = \frac{en(p)}{\tau_{n(p)}} \qquad \textbf{Equation 3-15}$$

where $\tau_{n(p)}$ is the lifetime of the electrons (holes), Equation 3-13 yields with a constant $b$ value:

$$\frac{d^2n}{dx^2} = \frac{n}{L^2} \qquad \textbf{Equation 3-16}$$

where $L$ is the typical diffusion length, defined here as $L = \sqrt{D\tau}$. The solution of this differential equation is well-known, given boundary carrier concentrations $n_1$ and $n_2$ at junctions 1 and 2, respectively:

$$n(x) = \frac{n_1 \sinh\left(\frac{l-x}{L}\right) + n_2 \sinh\left(\frac{x}{L}\right)}{\sinh\left(\frac{l}{L}\right)} = p(x) \qquad \textbf{Equation 3-17}$$

At this point one can determine that the boundary carrier concentrations $n_1$ and $n_2$ have major contributions to the level of injected carriers into the intrinsic region. To calculate the value of these boundary conditions as a function of intrinsic region length, one should examine the minority carrier densities at the junctions ($J_n$ at junction 1, $J_p$ at junction 2). Equation 3-12 and Equation 3-13 yield:

$$J_n|_1 = \frac{b}{1+b} I + \left(\frac{eD}{L}\right)\left(-n_1 \coth\left(\frac{l}{L}\right) + \frac{n_2}{\sinh\left(\frac{l}{L}\right)}\right. \qquad \textbf{Equation 3-18}$$

$$J_p|_2 = \frac{1}{1+b} I + \left(\frac{eD}{L}\right)\left(\frac{n_1}{\sinh\left(\frac{l}{L}\right)} - n_2 \coth\left(\frac{l}{L}\right)\right) \qquad \textbf{Equation 3-19}$$

Taking advantage of assumption 5, the recombination current at the doped region interface is [168]:

$$J_n|_1 = q h_1 n_i^2 \qquad \textbf{Equation 3-20}$$

$$J_p|_2 = q h_2 n_i^2 \qquad \textbf{Equation 3-21}$$

where $h_i = \frac{i_{is}}{q n_i^2}$ is the emitter parameter for junction 1 and 2, and $i_{is}$ is the saturation current for $i = n, p$ at junction 1 and 2, respectively. Setting Equation 3-18 (Equation 3-19) and Equation 3-20 (Equation 3-21) as equivalent yields:

$$h_1 n_1^2 + \left(\frac{D}{L}\coth\left(\frac{w}{L}\right)\right) n_1 - \left(\frac{D}{L}\left(\frac{n_2}{\sinh\left(\frac{w}{L}\right)}\right) + \frac{1}{q}\left(\frac{b}{1+b}\right) I\right) = 0 \qquad \textbf{Equation 3-22}$$

$$h_2 n_2^2 + (\frac{D}{L}\coth\left(\frac{w}{L}\right) n_2 - \left(\frac{D}{L}\left(\frac{n_1}{\sinh\left(\frac{w}{L}\right)}\right) + \frac{1}{q}\left(\frac{1}{1+b}\right) I\right) = 0 \qquad \textbf{Equation 3-23}$$

By considering these two equations as quadratic in terms of $n_1$ and $n_2$, respectively the effect of the intrinsic region on the boundary conditions can be developed:

$$n_1 = \frac{1}{2h_1}\left(\frac{D}{L}\right)\left(-\coth\left(\frac{l}{L}\right) + \sqrt{\coth^2\left(\frac{l}{L}\right) + \frac{I}{I_1} + 4h_1\left(\frac{L}{D}\right)\left(\frac{n_2}{\sinh\left(\frac{l}{L}\right)}\right)}\right) \qquad \textbf{Equation 3-24}$$

$$n_2 = \frac{1}{2h_2}\left(\frac{D}{L}\right)\left(-\coth\left(\frac{l}{L}\right) + \sqrt{\coth^2\left(\frac{l}{L}\right) + \frac{I}{I_2} + 4h_2\left(\frac{L}{D}\right)\left(\frac{n_1}{\sinh\left(\frac{l}{L}\right)}\right)}\right) \qquad \textbf{Equation 3-25}$$

where

$$I_1 \equiv \frac{1+b}{4b}\left(\frac{qD}{h_1\tau}\right) \qquad \textbf{Equation 3-26}$$

$$I_2 \equiv \frac{1+b}{4b}\left(\frac{qD}{h_2\tau}\right) \qquad \textbf{Equation 3-27}$$

While these equations can be solved independently for large enough devices [161], for devices of the size scales in this work, the concentrations of carriers at the junctions are tightly coupled, and so they must be solved simultaneously. Regardless, by observation it is clear that the length of the intrinsic region controls the concentration of carriers at the boundaries, which controls the carrier concentration through the region, $n(x)$, whose gradient controls the current through the device, $J_n$ and $J_p$. Therefore, the length of the intrinsic region plays a major role in the electric performance of the device, and from that the heating performance of the device.

### 3.5 Simulation Study of Differing Intrinsic Regions

While the above derivation clearly shows that the length of the intrinsic region controls the concentration of carriers at the junctions and therefore the current through the device, the optical component of these structures also needs to be considered. As the inner intrinsic region decreases, the heavily doped silicon regions become closer to the waveguide and optical absorption will increase due to free-carrier absorption. The trade-off between switching efficiency and optical insertion loss must be considered. To investigate the effect on these devices, 2D simulations with intrinsic region lengths ranging from 450 nm to 1.5 μm were performed, all heated by 100 ns voltage pulses. While these results are from a 2D model, the thermal dynamics of the 3D model are expected to only differ by a scaling factor as seen in Figure 3.2c.

The peak temperatures of the PCM and the Si waveguide are extracted from the different device geometries with 100 ns voltage pulses of different applied amplitudes and are plotted in Figure 3.6. A forward biased PIN diode approximately behaves as a linear conductor above the forward voltage drop of the diode (~1.4 V for our model as shown in Figure 3.3a) due to the in-series resistance of the heavily doped regions. For a simple linear conductor, power dissipated due to Joule heating is equal to $P = \sigma V^2$. Using a linear thermal treatment $\Delta T = \frac{1}{m \cdot c_p} P$ yields the relationship: $\Delta T \propto P \propto V^2$. With this approximation in mind, the peak PCM temperatures (shown in Figure 3.6) are well-fit by a quadratic equation:

$$\boldsymbol{T_{peak} = \alpha(V - V_{bi})^2 + \beta(V - V_{bi}) + 273.15} \qquad \textbf{Equation 3-28}$$

where $V_{bi}$ is the built-in voltage of the device, $\alpha$ and $\beta$ are fitting variables, and the values found for the fittings in this work are listed in Table 6.

**Table 6 – Fitting parameters for $T_{GST}$ using Equation 3-28.**

| $l_{int}$ | $\alpha$ | $\beta$ |
|---|---|---|
| **0.45** | 51.95 | 90.29 |
| **0.9** | 35.32 | 39.55 |
| **1.1** | 31.73 | 25.00 |
| **1.2** | 28.78 | 25.39 |
| **1.5** | 24.57 | 12.52 |

The peak Si temperature investigated here is not a volumetric average (unlike the reported GST temperature, which is averaged volumetrically). Instead, the peak "local hotspot" Si temperature is reported. This is a more relevant metric as locations of high energy concentrations are where device failure is most likely to occur. These peak temperatures are attributed to current crowding at the edges of the rib waveguide and the significant amount of carrier recombination at the interfaces. Due to these complex effects, the peak silicon temperature does not follow Equation 3-28. For calculations of $V_{\max}$ a best fit line was used to interpolate the data.

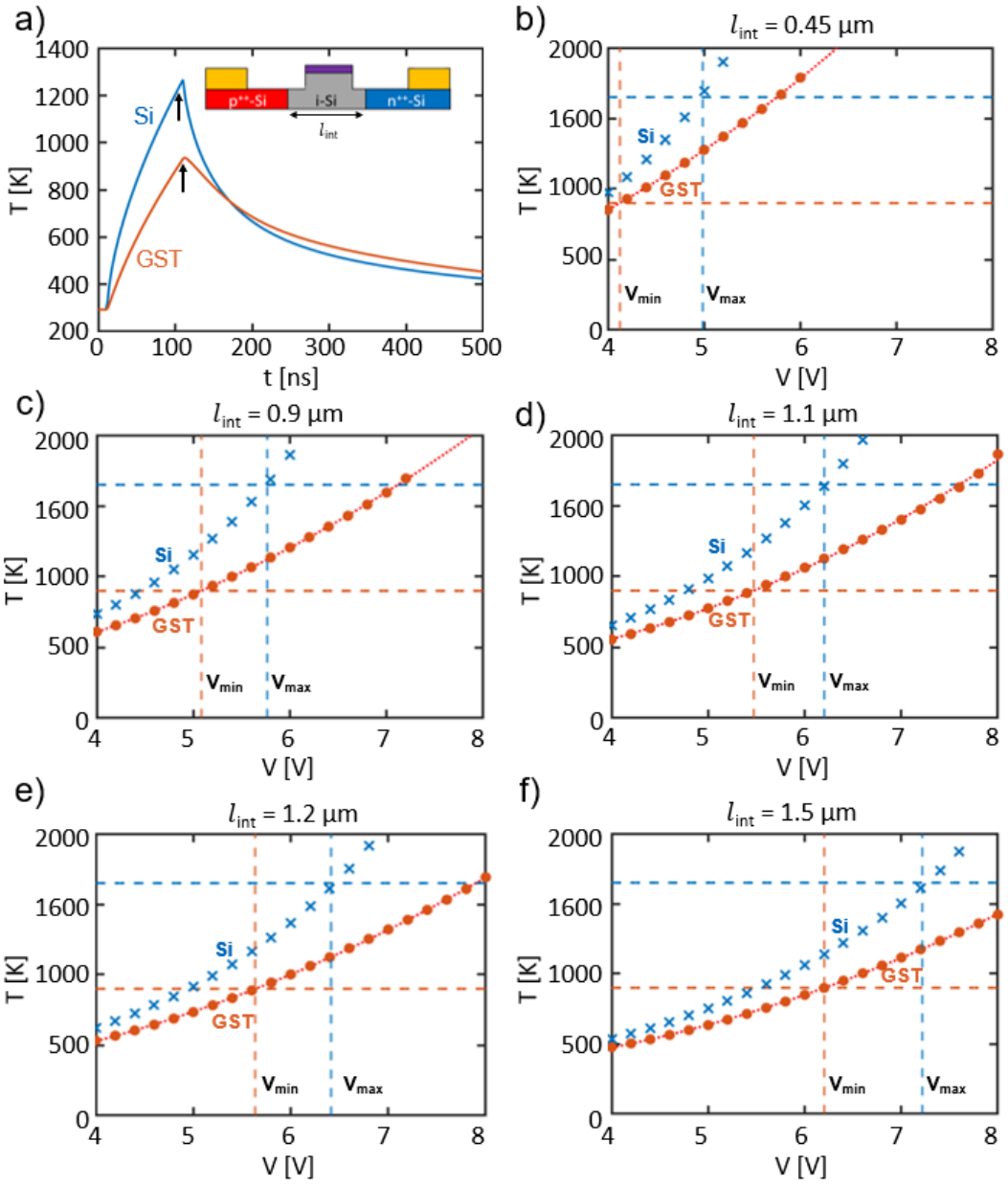


**Figure 3.6 - Different thermal performance of PIN diodes with different intrinsic region lengths. (a) Typical device thermal response as well as indication of where peak temperatures are being evaluated. (b)-(f) Peak temperature vs. applied 100 ns voltage pulse for both the GST (orange circles) and Si (blue crosses), for varying intrinsic region lengths. The voltage which heats the GST above the melting temperature ($V_{min}$) is shown by the orange vertical line. The maximum voltage that keeps the temperature of the Si device in a safe operating region ($V_{max}$) is shown by the blue vertical line. The temperature vs. voltage curve calculated by Equation 3-28 is shown by the red dashed line.**

Each set of data in Figure 3.6 is then evaluated to find the operating regions in which the PCM temperature is above $T_m$ and the Si temperature is well below the Si melting temperature ($T_{max,Si}$ = 1650 K, well below the typical melting point of Si [147]). These operating ranges are shown in Figure 3.7b, with $V_{max}$ corresponding to the voltage that exceeds $T_{max,Si}$ for a given intrinsic region length ($l_{int}$) while $V_{min}$ is the minimum voltage required for the PCM reach $T_m$. In practice, the maximum voltage may be limited by the ablation temperature of the PCM in question rather than the melting temperature of silicon (for GST this would be ~1200 K, corresponding to the reported boiling point of Te [169], [170]).

This information is summarized in Table 7 together with the minimum energy required to achieve amorphization and corresponding figure of merit (FOM). The FOM used here calculates the ratio of energy supplied to the device against the amount that is absorbed by the PCM. This FOM is calculated through [98], [127]:

$$FOM = \frac{m\, c_p\, \Delta T_{PCM}}{\int V \cdot I\, dt} = \frac{m\, c_p\, \Delta T_{PCM}}{E_{switch}} \qquad \textbf{Equation 3-29}$$

where *m* is the mass of the PCM, $c_p$ is the specific heat of the PCM at constant pressure, $\Delta T_{PCM}$ is the maximum temperature rise of the PCM. The denominator is the usual equation for calculating total energy of an electrical pulse.

For these devices, the minimum switching energy as a function of intrinsic width is given in Figure 3.7c which reveals that reducing $l_{int}$ below 1 μm will result in the most significant energy savings. While this behavior holds true for small scale devices, it is worth noting that at larger scales devices will deviate from this trend at significantly long intrinsic regions, as the initial assumptions used to build this model no longer hold true for such device geometries (e.g., high-injection operation and high-field regime for calculating carrier mobility) [161].

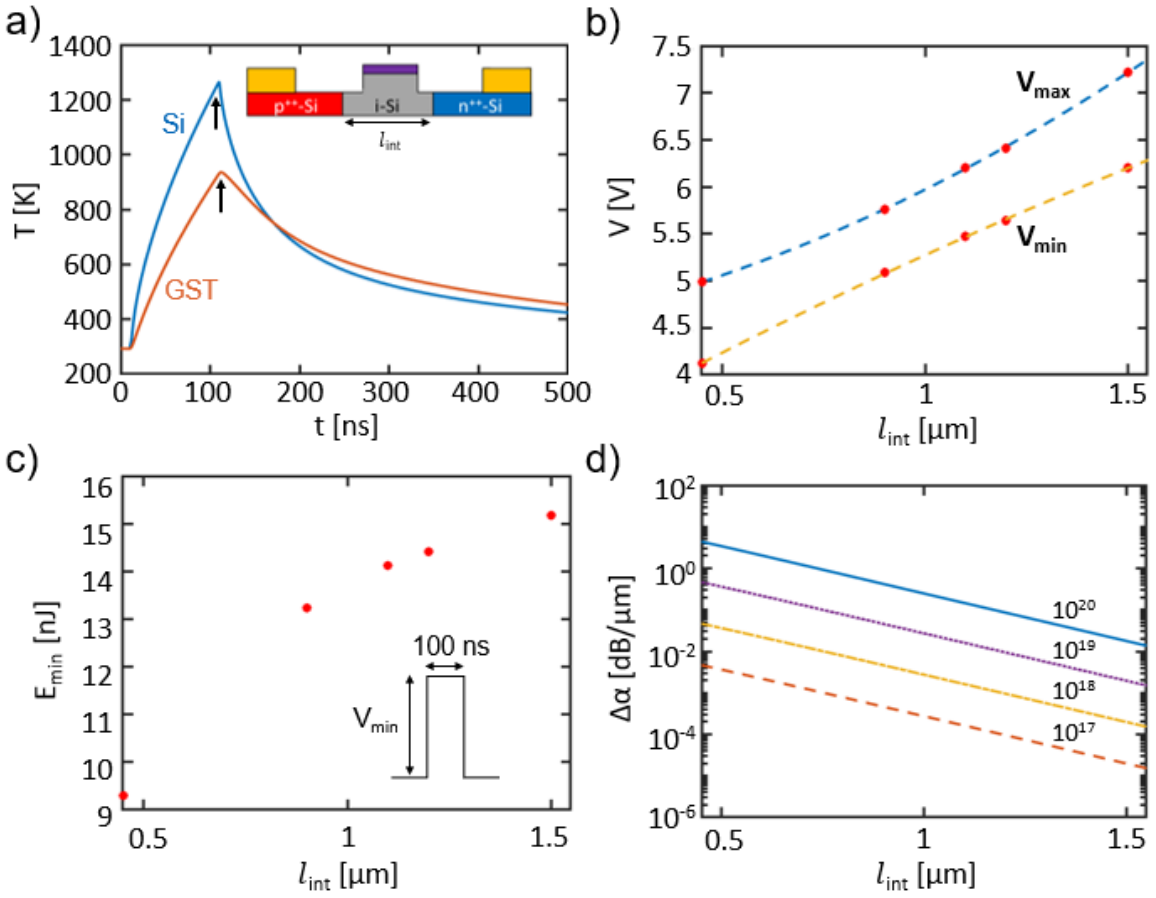


**Figure 3.7 - Effects of device geometry design for PIN heaters. (a) Example heating curve for the PIN diode used to extract peak temperatures of both the Si (blue) and GST (orange). (b) Operating range for different device geometries. $V_{min}$ is the minimum voltage required to heat the PCM above its melting point, while $V_{max}$ is the maximum voltage allowed before the Si starts to melt. (c) Minimum switching energy, $E_{min}$, calculated using $V_{min}$ as a function of intrinsic length. (d) Optical loss, $\Delta\alpha$, of the waveguide for different intrinsic region widths and doping levels.**

While the switching efficiency improves with decreasing intrinsic length, the heavily doped regions of silicon will introduce optical loss due to free carrier absorption. Thus, the trade-off between electro-thermal switching efficiency and optical insertion loss must be considered when designing with a specific application in mind. To calculate the optical loss of PIN diode as a function of intrinsic region width and doping concentration, the waveguide's complex effective

refractive index was simulated using Lumerical MODE, a 2D eigenmode solver. The model was swept over two parameters: intrinsic region width and refractive index of the silicon contacts. The refractive index of silicon is the function of numbers of holes ($N_h$) and electrons ($N_e$) in *p*-type and *n*-type, respectively:

$$\Delta n = -8.8 \times 10^{-22} \cdot \Delta N_e - 8.5 \times 10^{-18} \cdot (\Delta N_h)^{0.8} \quad \textbf{Equation 3-30}$$

$$\Delta \alpha = -8.5 \times 10^{-18} \cdot \Delta N_e + 6.0 \times 10^{-18} \cdot \Delta N_h \quad \textbf{Equation 3-31}$$

Equation 3-30 and Equation 3-31 provide the relationship between the change in the real part of the refractive index ($\Delta n$) and optical absorption ($\Delta \alpha$) from intrinsic silicon as a function of doping concentration for $\lambda$ = 1550 nm. From the results in Figure 3.7d, one can see that the optical loss increases both with decreasing intrinsic length and increasing doping concentration. As the optical loss of amorphous GST on a silicon rib waveguide is approximately 0.06 dB/μm, any absorption due to the doped contacts that is less than this will increase the overall absorption of the device by a negligible amount [171].

**Table 7 - Summary of geometric results (2D simulations).**

| $l_{int}$ [μm] | Range [V] | $V_{min}$ [V] | $I_{avg}$ [mA] | $E_{switch,min}$ [nJ] | FOM [%] |
|---|---|---|---|---|---|
| **0.45** | 0.863 | 4.123 | 22.60 | 9.318 | 0.91 |
| **0.90** | 0.679 | 5.085 | 26.10 | 13.272 | 0.64 |
| **1.10** | 0.732 | 5.474 | 25.90 | 14.178 | 0.60 |
| **1.20** | 0.775 | 5.639 | 25.60 | 14.436 | 0.59 |
| **1.50** | 1.014 | 6.205 | 24.50 | 15.202 | 0.56 |

### 3.6 Pulse Effect

The effects of pulse amplitude and duration on peak PCM temperature, quenching time, and quench rate was investigated. For these simulations, the intrinsic width was fixed to be $l_{int}$= 0.9 µm, providing a good trade-off between minimal optical loss and efficient switching energy. As in previous simulations, both the peak Si and GST temperatures are monitored to ensure the device does not exceed $T_{m,Si}$ which would lead to catastrophic failure, while still reaching amorphization temperatures in the PCM thin film. These temperatures are presented in Figure 3.8.

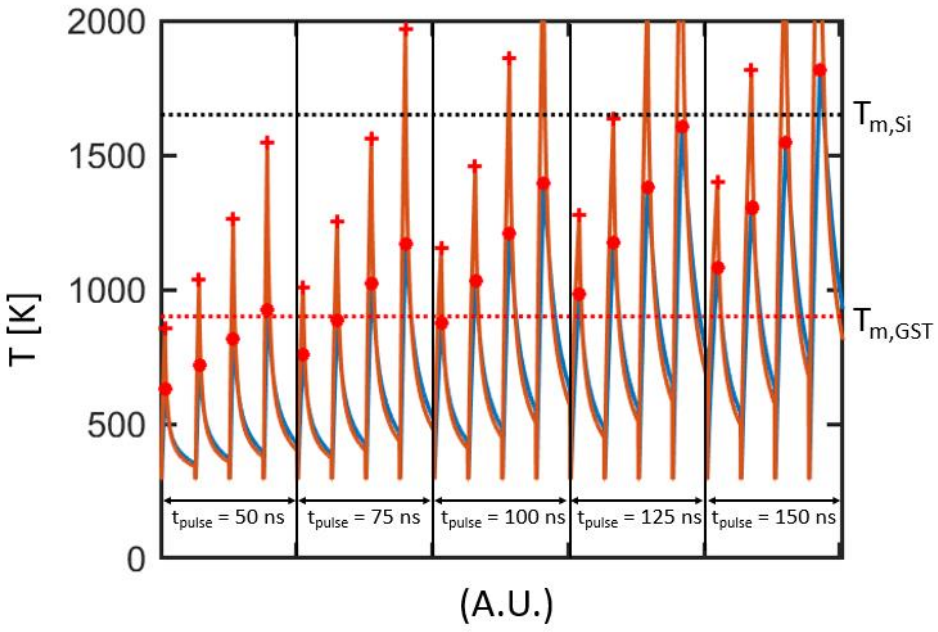


**Figure 3.8 - Thermal performance of devices with different programming pulses. Five different pulse widths (50, 75, 100, 125 and 150 ns) were paired with four different voltages (5, 5.5, 6 and 6.5 V). Plotted here are increasing voltages for each pulse width, with the peak temperatures highlighted for both the GST (circles) and the Si (crosses). Feasible pulse shapes are determined from those peak temperatures which are above the melting temperature of our GST (900 K) and below our maximum desired temperature of the underlying Si (1650 K).**

From these, Figure 3.9b plots the peak temperature of the center PCM volume (see black outline in Figure 3.2i) for pulse durations ranging from 50 ns to 150 ns and voltages ranging from 5 V to 6.5 V. The dashed blue and red lines in Figure 3.9b-d indicate the melting temperature threshold for Si and GST respectively with the unacceptable operating regions greyed out. For shorter pulses, higher voltages are required to amorphize the PCM, while lower voltages are required for longer pulse durations as shown in Figure 3.9b. However, the acceptable window of operation significantly reduces with decreasing pulse width. This has important implications for the long-term endurance of the PIN microheater and indicates an increased requirement for control when using short programming pulses, such as multilevel programming of GST [125].

Figure 3.9c-d plots the quenching times and quenching rates for the pulse parameters simulated in Figure 3.9b. Reducing the pulse duration seemingly reduces the quench time (increasing the quenching rate). This behavior is physically reasonable since longer pulse widths will allow more time for heat dissipation throughout the device during the pulse, increasing the temperature of the surrounding material and reducing the cooling speed of the microheater. For a given microheater geometry, there is a clear upper limit on the maximum quench rate achievable. This has important implications for the types of PCMs which can be electro-thermally switched in a reversible manner as indicated by Table 4. One approach to further improving the quenching rate of the PIN microheater (and also the minimum switching energy) is to concentrate heat generation in the intrinsic region while minimizing Joule heating in the heavily doped *p*- and *n*-regions. Introducing mid-level traps or recombination centers could be one method to improve heat generation via carrier recombination in the intrinsic region at the expense of increased optical loss. Another approach could be using a single dopant type throughout the microheater while varying the dopant concentration (i.e., $n^{++}/n/n^{++}$ or $p^{++}/p/p^{++}$), and will be investigated in more depth in

Section 4.0. This would enhance the voltage drop in the lightly doped *n*- or *p*-region and thus increase Joule heating in that portion of the device. This approach has been demonstrated for reversibly switching $Sb_2Se_3$ [69], but more work is needed to directly compare the energy efficiency, optical loss, and maximum quench rate with that of PIN microheaters.

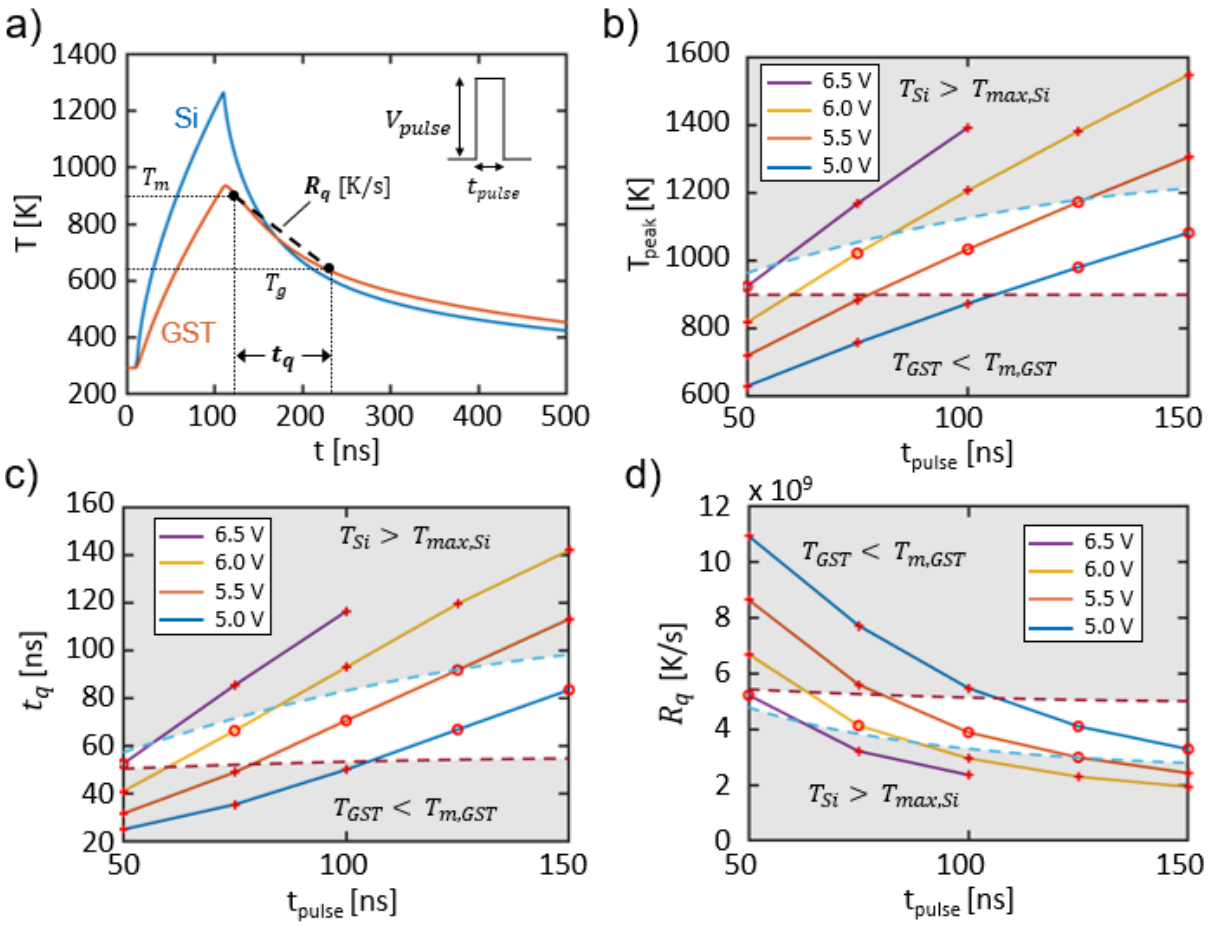


**Figure 3.9 – Pulse-shape effects on device thermal performance. (a) Example of a thermal curve for the device with the quench time, quench rate, and pulse characteristics defined. (b) Peak temperatures, $T_{peak}$ of the GST for different pulse amplitudes and widths. Pulse shapes that keep the Si temperature in a usable range while melting the GST are found within the unshaded area. (c) The quench times, $t_q$, and (d) the quenching rate, $R_q$, as a function of pulse shape. Shorter pulses increase the quenching rate but reduce the operating window since they require higher pulse amplitudes.**

## 3.7 Summary of Simulation Results

Relevant design parameters from these simulations are summarized in Table 8, useful as first order estimations during device design. These results show the PIN diode heater device is fast to operate, and uses its energy towards heating the PCM more efficiently, minimizing wasted heat in the device despite a higher pulse power. This conclusion is supported through visual inspection of the cross sections of the devices under operation as shown in Figure 3.2d-i. Similar reductions in heating volume will play a key role in minimizing cross talk in future large arrays of devices.

**Table 8 - Compiled results of initial design investigations.**

| Design | Pulse Time | Switching Energy | FOM [%] | $t_q$ | Quench Rate |
|---|---|---|---|---|---|
| **Single heater** | 10 [µs] | 192 [nJ] | 0.045 | 0.75 [µs] | 3.7 x $10^8$ [K/s] |
| **Double heater** | 1 [µs] | 85 [nJ] | 0.101 | 1.27 [µs] | 2.2 x $10^8$ [K/s] |
| **PIN (2D)** | 100 [ns] | 16 [nJ] | 0.532 | 127 [ns] | 2.2 x $10^9$ [K/s] |
| **PIN (3D)** | 100 [ns] | 16 [nJ] | 0.444 | 84.8 [ns]* | 2.1 x $10^9$ [K/s]* |

*3D curve used the max temperature of the GST, 799.4 K, rather than the melting temperature to evaluate since the model never actually achieved the melting temperature, $T_m$

# 4.0 Raman Thermometry

## 4.1 Raman Thermometry Background

Raman thermometry has been used since the 1990s to noninvasively measure temperature distributions in micro-scale objects [172]. In normal Raman spectroscopy, incident laser light is scattered inelastically by elementary excitations within the material. In a Stokes Raman process a small amount of incident photons are scattered inelastically, creating (Stokes) or absorbing (anti-Stokes) optical phonons near the $\Gamma$ point of the first Brillouin zone, as shown in Figure 2.8a. As Stokes scattering is much more statistically likely (at room temperature [173]), this process is then measured by the material specific shift in frequency of the backreflected signal, specifically ~520.7 $cm^{-1}$ for Si. Any changes in lattice temperature results in an energy shift of the optical phonon: $\Delta\nu/\Delta T \approx -0.021\ \mathrm{cm}^{-1}/\mathrm{K}$ for Si [172]. Due to the nondestructive and minimally invasive nature of this high spatial resolution process, it has been used to measure temperature distribution in small devices [172], [174], 2D materials thermal properties [175], [176], as well as many fluid flow applications [177], [178]. Here, this process is utilized to determine the operating temperature of integrated waveguide microheaters at different voltages [98].

## 4.2 Devices Investigated

### 4.2.1 Device Details

The ability to reversibly control the phase and amplitude of light in both a nonvolatile and highly compact form-factor has been a key motivation behind current research into optical phase-change materials (PCMs) [57]. However, achieving this reversible control using a scalable integrated approach (i.e., electronic integration) has been more challenging for the optical community than it has for the electronics community. This can be attributed to the significant difference in area and volume between electronic PCM memristors (typically sub-50 nm in *x*-, *y*-, and *z*-dimensions) and photonic PCM devices (typically >1 μm in-plane, while ≤50 nm out-of-plane) which rules out directly applying current to the PCM itself. To reversibly switch these materials, high melting temperatures (~900 K) and fast quenching rates (~0.1 to 1 K/ns in the case of $Ge_2Sb_2Te_5$) are required which demands careful thermal engineering [133]. Additionally, the heat source used to switch the PCM should be optically transparent to prevent high insertion loss.

To address this challenge, several approaches have been demonstrated to enable scalable electrical control over optical PCMs for photonic circuits using waveguide-integrated resistive microheaters. This includes the use of transparent conductors [128], [129], [179], metallic heaters [130], [180], [181], graphene [125], [182], doped-silicon waveguides [123], [183], and silicon PIN junctions [126]. For monolithic integration with silicon photonic platforms, microheaters based on single-doped silicon [123], [183], [184] and silicon PIN junctions [98], [126] are the most attractive choices as they can be fabricated using the same foundry-compatible processes commonly used to fabricate active silicon photonics devices (e.g., PN modulators [185] and doped-

silicon thermo-optic phase shifters [186]). While both designs can be easily incorporated into the standard silicon photonics process flow, these two approaches have their relative strengths and weaknesses. Using microheaters comprised of forward-biased silicon PIN junctions (here after referred to as "PIN microheaters") has the potential to have very low insertion loss as the waveguide can be patterned in the intrinsic region of the junction. However, the thermal response of these devices can be quite sensitive to device dimensions, the active area is restricted by the dimensions of the intrinsic region, and doping levels as we have observed in simulations [98] and shown experimentally in this work. On the other hand, single-doped silicon microheaters (here after referred to as "doped microheaters") have simpler design considerations, which can be arbitrarily large, at the expense of higher voltages. A direct comparison between these two designs is challenging, since the reported devices from previous works have been processed separately under different process flows and doping conditions.

In the present experiment, both doped and PIN microheater designs for switching PCMs which have been fabricated on the same chip together under the same conditions are compared. This work investigates the steady-state heating response of PIN and doped microheaters using Raman thermometry and compares different PIN device geometries to further understand critical design parameters for these embedded heaters. Damage at the metal contacts was observed in the PIN devices after steady-state measurements (but not the doped devices), prompting exploration of the conditions under which this damage occurs. Endurance tests performed on doped and PIN microheaters revealed that for the same electrical power dissipation, doped microheaters exhibited less thermally induced aging than PIN microheaters. These results highlight the need for further research to improve the efficiency and lifetime of these microheaters for phase-change photonics applications.

PIN microheaters of differing intrinsic region lengths and widths were fabricated in a 90 nm CMOS line at the MIT Lincoln Laboratory [183], along with an array of n-doped microheaters with a constant geometry and varying levels of internal doping. All devices were fabricated on silicon-on-insulator wafers with a device layer of ~140 nm Si on 1 µm of $SiO_2$. While waveguides were not patterned on these devices, the thin silicon device layer has similar dimensions to partially etched silicon contacts in a typical rib waveguide process. To make electrical contact to the silicon, 200 nm Al metal contacts were deposited on top of a thin Ti/TiN adhesion/barrier layer. Finally, a thin 10 nm passivating layer of $SiO_2$ was uniformly deposited on the chip which is needed to provide electrical isolation for a PCM layer deposited on top of the microheater.

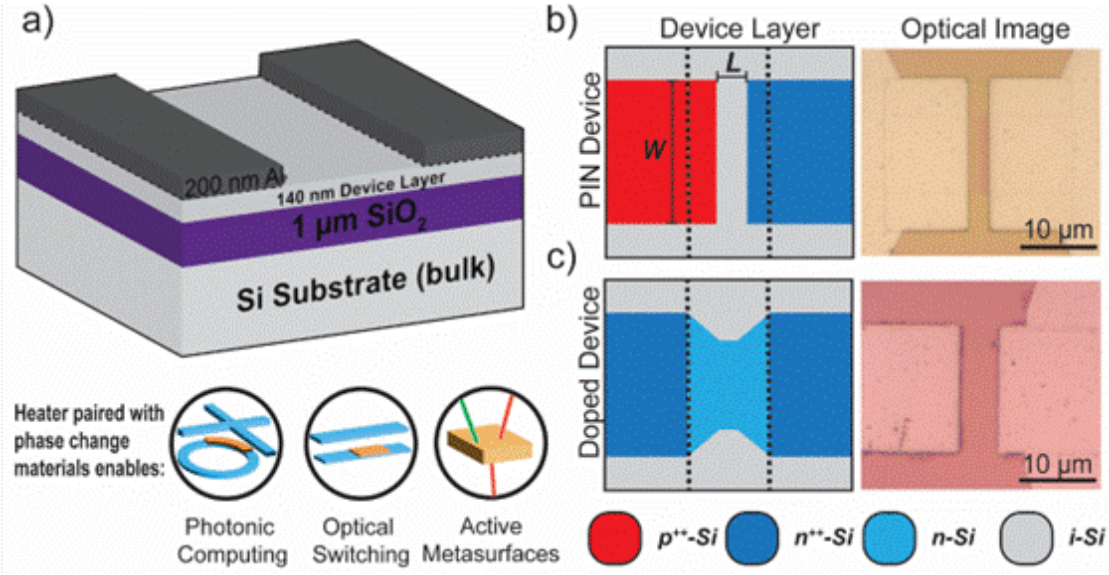


**Figure 4.1 - Schematic views of the microheaters studied. All devices share the same layer structure shown in (a), where the 10 nm passivating $SiO_2$ layer is omitted for clarity. Schematics of both the (b) PIN and (c) doped device layers are shown, with specific doping areas color coded as denoted. For the PIN device, specific *W* and *L* dimensions are denoted. Contact edges from the contact layer are represented on the device layer by dotted lines. The top-down views of both devices are paired with optical images of pristine devices. The doped regions for the PIN device can be seen faintly in the optical image, highlighting the much smaller size of these devices when compared to the doped microheaters.**

Twelve unique PIN microheater geometries were fabricated based on the design demonstrated by Zheng et al. [126] with four different device widths ($W$= 5, 10, 15, and 20 μm), and three different lengths ($L$ = 0.9, 1.2, and 1.5 μm) as indicated in Figure 4.1. To keep the contact resistance of the PIN devices consistent between different geometries, the distance between the edge of the metal contacts and the edge of the doped regions was kept constant at 0.8 μm, so that the total distance between contacts was always equal to $L$ + 1.6 μm. Additionally, the distance between each metal contact edge and the doped region edge was kept constant at 5 μm so that edge-to-edge, the contact was always $W$ + 10 μm. The doped microheaters based on the design by Ríos et al. [183] had a fixed geometry with 5 μm between contacts and a tapered, lightly *n*-doped channel, as shown in Figure 4.1. This channel tapers to a 10×0.5 $\mu m^2$ area which localizes the Joule heating to the PCM region in the waveguide center. The metal contacts for the *n*-doped devices are separated by 16 μm from edge-to-edge.

For the PIN microheaters, both the $p^{++}$ and $n^{++}$ regions of the device were heavily doped (~$10^{20}$ $cm^{-3}$) to minimize contact resistance as well as maximize current through the device [98]. The intrinsic region was unaltered, and as such is henceforth referred to as *undoped*. For the doped microheaters, the two $n^{++}$ regions used for ohmic contact were similarly heavily doped (~$10^{20}$ $cm^{-3}$), while the interior n-regions were lightly doped at two different levels. Devices 1 and 2 were doped with $n$ = 3 x $10^{18}$ $cm^{-3}$, while devices 3 and 4 were doped with $n$ = 8 x $10^{17}$ $cm^{-3}$.

### 4.2.2 Raman Experiments Details

Raman thermometry has emerged as a way to measure material specific temperatures inside of samples by tracking the shift of Raman peaks as a function of temperature [172], [175], [184], [187]–[191]. To acquire Raman spectra of our microheaters, a Horiba XploRA PLUS Raman microscope with 473 nm excitation laser and long working distance 50×, 0.55 NA objective was used, resulting in a diffraction limited spot size of 1.18 μm. The Raman measurements utilized a 25 mW, 473 nm laser for the measurement, but it was operated at 1% power (~0.25 mW) to ensure minimal excess heat was imparted into the devices through photon absorption. In order to convert the measured Raman spectra to the device temperature, the Si peak position vs. sample temperature was measured using a custom sample holder with built-in hotplate. Bare fabricated chips (prior to wire bonding) were placed on the hotplate with temperatures increasing from 25 °C to 300 °C in steps of 25 °C. The sample was held at each temperature for 10 minutes to ensure thermal equilibrium followed by the acquisition of three Raman spectra from undoped Si regions of the sample. All Si peaks from each calibration spectrum were fit to a Gaussian/Lorentzian hybrid curve, and the peak center locations for the three spectra per temperature were averaged. The resulting calibration curve is shown in Figure 4.2b and matches up well with other results in the literature [172], [175], [189]

After the calibration curve was obtained, the fabricated chip was attached and wire-bonded to a custom printed circuit board (PCB) to simplify electrical connectivity as shown in the inset in Figure 4.2a. This PCB and wire bonding setup not only allowed for consistent contact resistance to the device, but it also allowed the microscope stage to be mobile without disrupting the contact.

Devices were powered during the measurements using a Keithley 2450 Source Measure Unit (SMU) with up to 4 V for the PIN devices and up to 10 V for the doped devices.

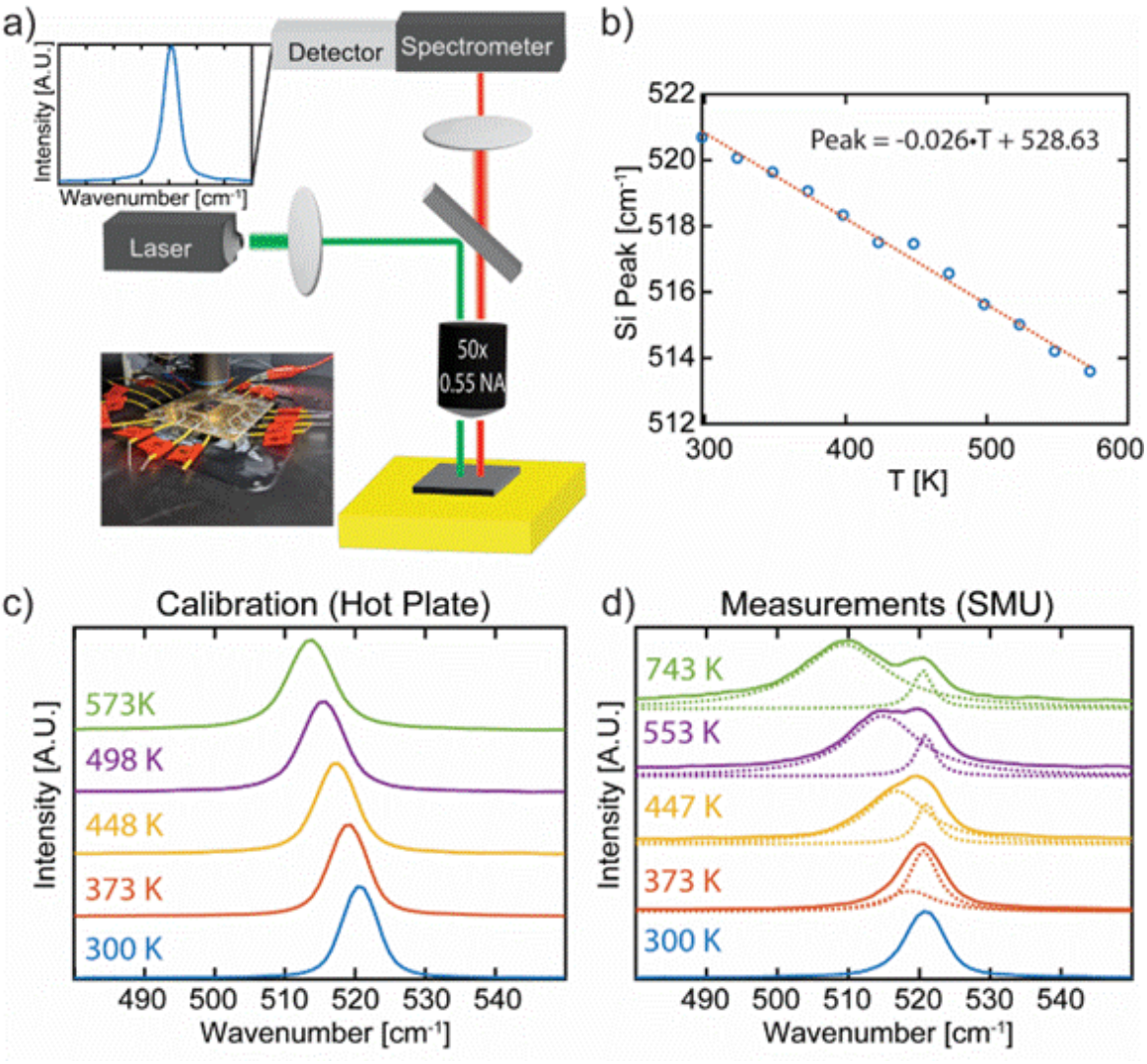


**Figure 4.2 – Explanation of Raman thermometry process. (a) Schematic of a Raman Microscopy process, inset shows an image of the wire bonded test sample. (b) Calculated calibration curve of Si peak location against a known temperature using a hotplate. (c) Example of the Si Raman peak shifting at known temperatures, generated by the in-situ hot plate. (d) Demonstrating the peak splitting observed at higher temperatures for the devices while powered. This peak splitting does not occur during generation of the calibration curve, due to the consistent heat provided by the hot plate used.**

To obtain temperature measurements, each applied DC voltage was maintained for 5 min to ensure both electrical and mechanical stability. Next, to ensure the beam was centered on the channel after any mechanical drift of the sample, the device was first mapped across the device length with the metal contacts providing reference points for the device edge. Then the z-direction was scanned to verify that the thin silicon device layer was in optimal focus. Three Raman spectra were then obtained and fit using a similar peak-fitting and averaging method used for the calibration data. However, at higher temperatures splitting of the Si peak occurred, as can be seen in Figure 4.2d. This splitting is attributed to the higher temperature of the thin Si device layer (i.e., the Si layer in which the microheater is fabricated) relative to the bulk Si substrate beneath the $SiO_2$, causing the Si peaks from the different temperatures of these two layers to split [184]. These peaks were fitted using a double Lorentz curve, and device temperature was then calculated using the redshift of the proper Si peak using the calibration curve (Figure 4.2b). This effect was not present in the generation of the calibration curve (Figure 4.2c), as the hot plate used ensured that both the thin film Si and the underlying Si substrate were at the same temperature, resulting in one single Lorentz peak for the Si temperature.

### 4.2.3 Expected Effects of Center Ribbed Waveguide vs. Planar Diode

These test structures are all planar diodes, with no waveguide ribs. Simulation-based thermal characterization predicts that adding the rib into the design introduces a changing cross-sectional area through the device, giving rise to local heating spots at either side of the rib [159], [192], [193]. However, this structure decreases the average volumetric heat generation in the center region, an effect of increased cross-sectional area with corresponding decreasing current density

in that region. For comparison, the heat generated for a silicon PIN diode under the same conditions as Figure 3.3b ($W_{int}$ = 1.5 µm, $V$ = 6.2 V) but without the additional 120-nm-thick waveguide in Figure 4.3a was calculated. For a given voltage it is estimated that presence of the waveguide rib results in an approximate 10% increase in temperature, specifically centered at the middle of the device, as shown in Figure 4.3a.

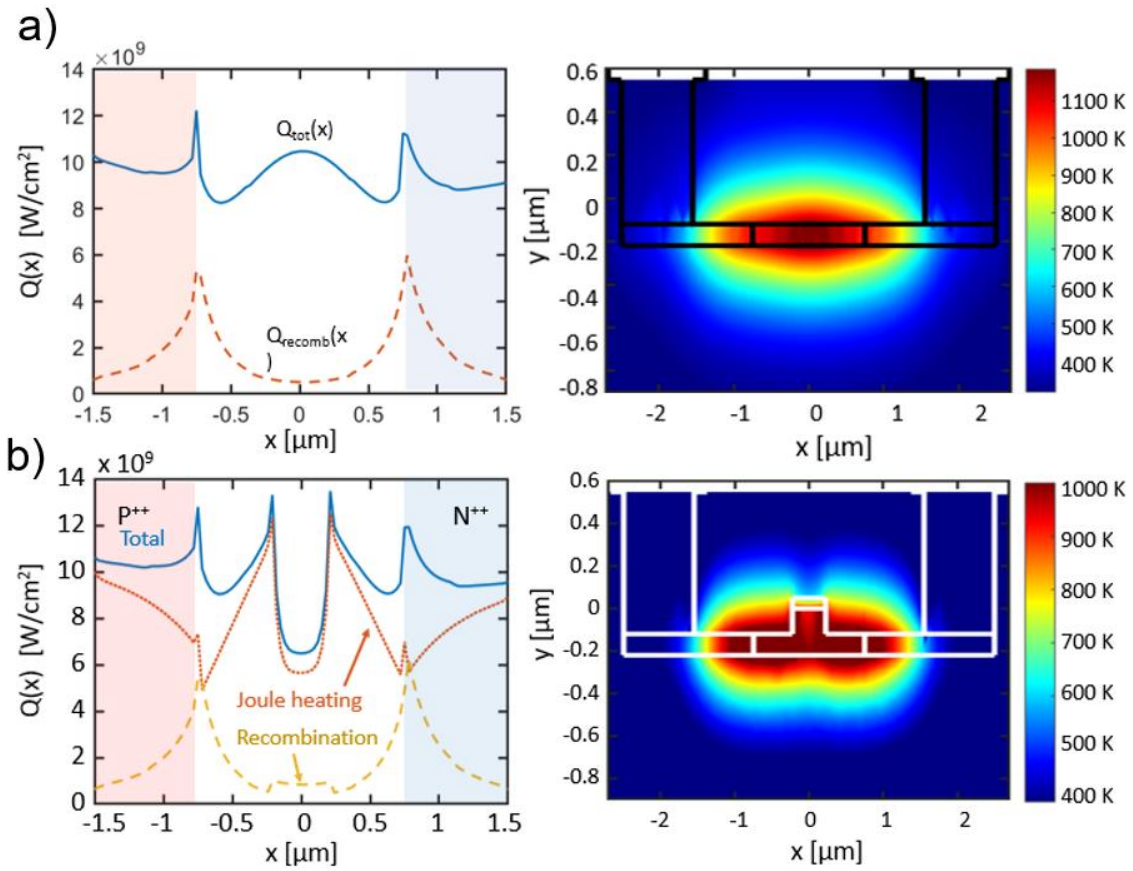


**Figure 4.3 – Comparison of the thermal performance of a planar vs. ribbed PIN diode. Normalized heat generated at pulse end, including the contribution from carrier recombination, as well as heat map at peak temperatue for (a) idealized planar diode and (b) ribbed diode.**

## 4.3 Single-Doped Results

### 4.3.1 Device Operations

The IV curves during Raman measurements for all 4 single-doped devices are shown in Figure 4.4. The measured current for each device is normalized by device width (*W*) to better facilitate comparison between the different device geometries as discussed later. The doped microheaters reveal nonlinear behaviors at higher applied voltages as can be seen in Figure 4.4. At lower applied voltages, like those available on-chip (<5 V), the IV behavior is linear as expected, resulting in the higher-doped device reaching higher currents (and therefore, higher applied power) at a given voltage [183], [184]. However, at higher applied voltages (~ >7 V), the device currents begin to exhibit nonlinear behavior, trending towards saturation. This is attributed to velocity saturation effects in silicon where the linear relationship between carrier velocities and electric field breaks down at high electric fields [194], [195].

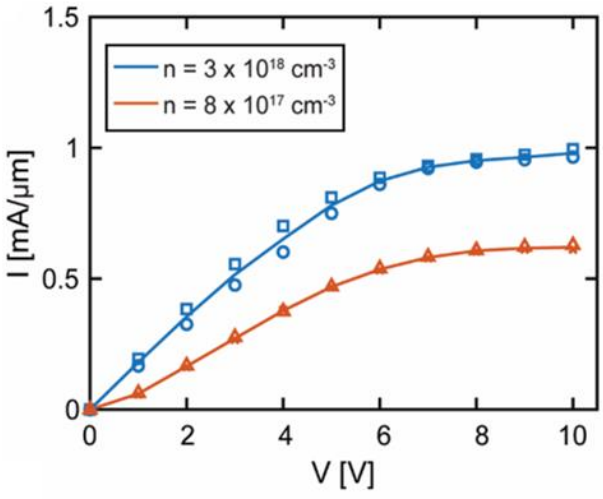


**Figure 4.4 – IV performance of the single-doped devices. Different point shapes come from different devices, two for each doping level.**

### 4.3.2 Velocity Saturation and Optical Phonon Scattering

As electronic devices continue to get aggressively scaled down in size, the electric field inside the device continues to get larger at standard operating voltages. As a result, understanding the impacts of high-field transport in silicon on the electrical and thermal performance of devices is increasingly important. In this work, the operating thermal principles of the single-doped devices can only be understood after considering the high-field transport effects on thermal generation.

High-field effects in semiconductors were first experimentally demonstrated in the early 1950s, with the advent of controllable short pulses, on the order of microseconds [195]. These short pulses are required to ensure minimal heating in the semiconductor, which decouples the measurements from high-temperature effects. These experimental studies mostly focused on Ge [194]–[197], the semiconductor of choice at the time, although studies on Si were also available [194], [197]. The historical experimental set up that was used is depicted in Figure 4.5a. To ensure that minimal heating occurred in the material, short pulses were used to drive the current. In addition, semiconductors with low numbers of carriers were used, to ensure that any energy transferred from the carriers to the lattice would be minimal. Under these conditions Ryder calculated that the lattice temperature would be raised by ~ 1 K per pulse [194]. Using this experimental design, Ryder was able to measure carrier velocity saturation in both Ge and Si at various temperatures; the results for n-type Si at room temperature are reproduced in Figure 4.5b.

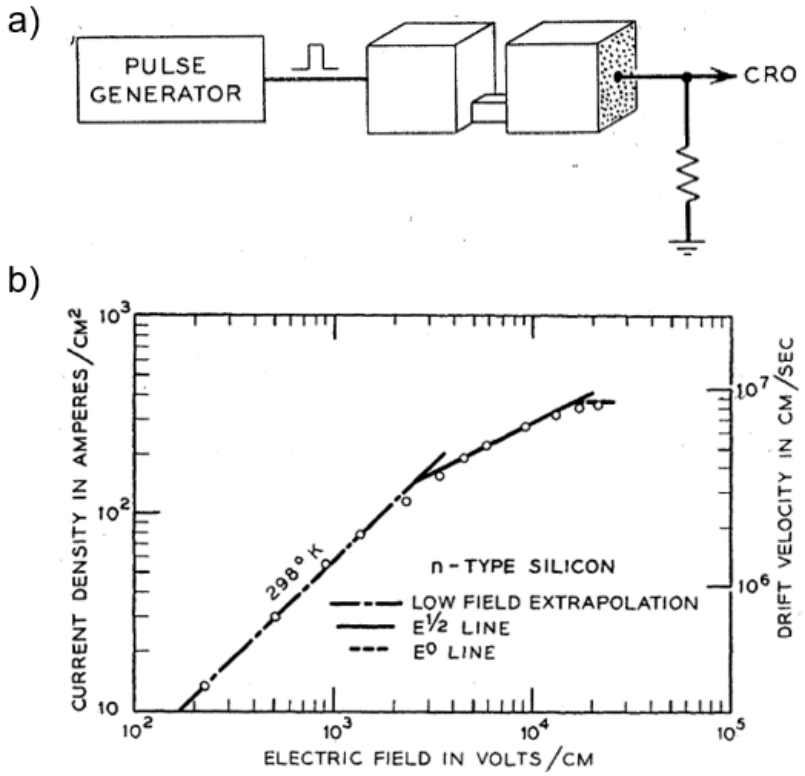


**Figure 4.5 – Initial work done on velocity saturation in semiconductors. (a) Schematic of the test structure used by Ryder and Schockley to test high-field transport in semiconductors, showing the electronic signal path through the etched channel, and out to a cathode-ray oscilloscope (CRO). (b) Experimental results showing saturation in n-type Si at room temperature. Reproduced from [194].**

These experimental results provided a basis for further work focused on determining the physical mechanism imparting this speed limit on semiconductor carriers. Ryder and Shockley initially concluded from their data that the energy losses due to velocity saturation was due to a combination of both acoustic and optical phonon scattering [196]. This theory was later expanded by Stratton, who showed that for Ge, the ratio of energy lost to acoustic vs. optical phonon modes is much smaller than 1 for energies up to ~1 eV [198]. Up to this point all theoretical analysis was done using the Boltzmann transport equation, and assuming the (standard) phenomenological relaxation time approximation [199]. However, with the introduction of Monte Carlo techniques

and a further maturity in the calculation of the full band structure of Si in the 1960's and 1970's, several new studies emerged taking more complex effects into account, including intervalley scattering, zone edge phonon modes, Umklapp processes and angular dependence of electron-phonon interactions [199]–[203]. Most of these studies support the standard assumption of velocity scattering being driven mostly by optical phonon interactions, although some have emerged that question how much of a role acoustic modes play in this effect [201]. While this is an interesting fundamental mechanistic question, a full discussion of specific phonon scattering interactions in high-field transport is beyond the scope of this work, so optical phonon scattering will be assumed to be the dominant velocity limiting process from hereon.

When a carrier in a semiconductor is accelerated such that its energy is higher than the optical phonon energy (~ 63 meV for Si [199]), the carrier will emit an optical phonon into the lattice and drop its momentum to almost zero, putting an upper limit on the drift velocity that carriers can achieve. This drift velocity "cap" is the observed upper limit on achievable current. Optical phonons in Si contribute very little to heat transport due to their flat dispersion mode, giving them low velocities. Instead, they decay into the faster acoustic modes, which then transport the heat away from the hot regions. However, the electron-phonon scattering time is fast (~0.1 ps) when compared to optical-acoustic decay times (~1 ps), so if there is significant rate of generation of optical phonons in a material, this can lead to a large buildup of optical phonons inside the material, corresponding to a high device temperature [202]. This cycle is illustrated in Figure 4.6.

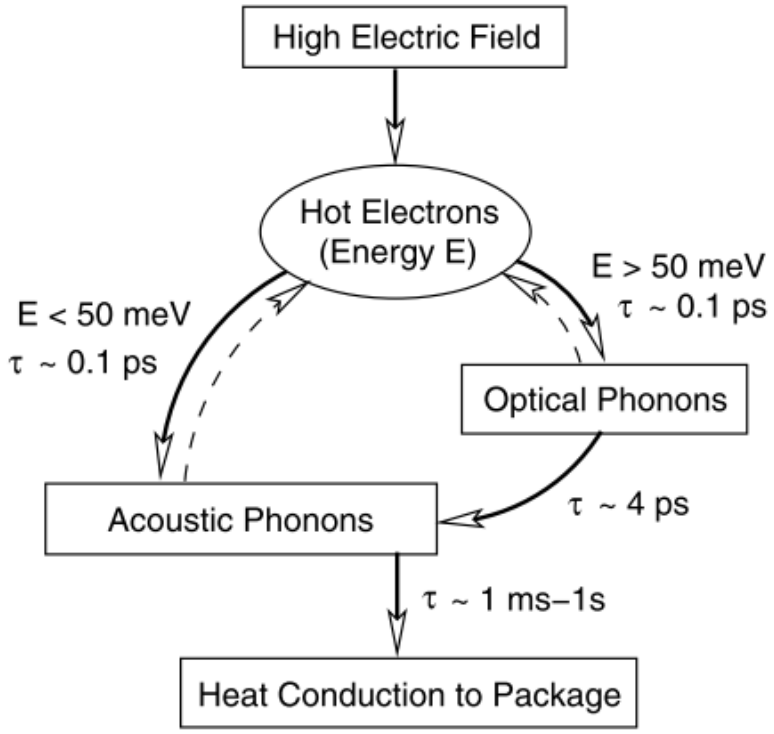


**Figure 4.6 - Diagram of electron-phonon scattering in semicondcutors. Diagram shows the process for both optical and acoustic phonons, as wel as optical-acoustic decay. All processes have their characteristic time scales listed as well. Reproduced from [202].**

### 4.3.3 Temperature Results

Figure 4.7a shows the corresponding device temperature as a function of applied voltage, and Figure 4.7b shows the calculated temperature as a function of applied power obtained using Raman thermometry. The doped microheaters were grouped by the concentration of the lightly n-doped region between the contacts. Heating in these devices should be approximately linear to applied power (quadratically to applied voltage in Figure 4.7a) due to Joule heating. For each

group of devices in Figure 4.7 (2 groups of 2 doped devices), a linear trend (quadratic for Figure 4.7a) was fit to compare the relative heating efficiency of the devices.

Interestingly, the devices with a lower doping level ($8\times10^{17}$ $cm^{-3}$) reach higher temperatures than the devices with higher doping ($3\times10^{18}$ $cm^{-3}$) for the same applied power above a certain threshold (see black dashed line in Figure 4.7b). This indicates that the devices with lower doping become more efficient heaters above this threshold, which happens to occur at the onset of velocity saturation (around ~7 V). One possible explanation for this effect is a higher phonon emission rate per carrier for the devices with lower doping levels.

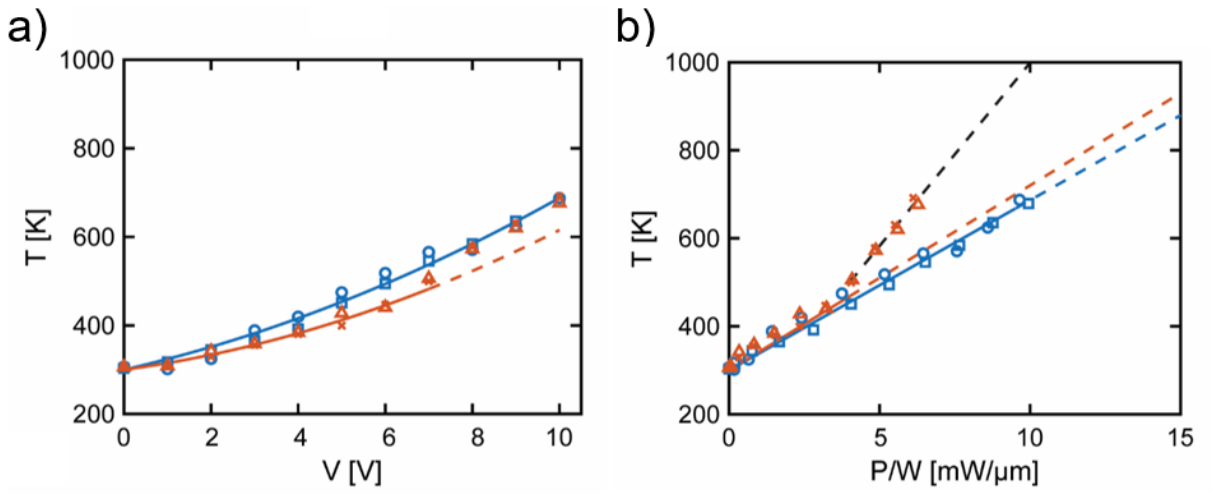


**Figure 4.7 – Raman thermometry results for single-doped devices. (a) Calculated device temperature vs. applied voltage. The n-doped devices are grouped by interior channel doping, and those are delineated by color. The specific device that the data points were taken from and designated by point shape, which are also grouped by color for ease of reference. For the $n = 8 \times 10^{17}$ $cm^{-3}$ devices in (a), continuation of the expected quadratic fit is given by the dashed orange line, showing the deviation from this behavior above 7 V. (b) Raman thermometry results shown vs. normalized applied power for doped devices. For the $n = 8 \times 10^{17}$ $cm^{-3}$ devices the deviation from expected Joule heating above 7 V is indicated by the dashed black line (a visual guide only), with the expected linear trend continuing using the dashed orange line.**

As discussed previously, velocity saturation has been widely accepted as optical phonon emission [199], [200], [202], [203], where once an electron's kinetic energy exceeds the optical phonon energy, it preferentially emits an optical phonon, causing its velocity to drop. This puts an effective cap on the carrier velocities seen in semiconductors, leading to the observed current saturation observed at high fields. To confirm this in the measured devices the IV curves for different channel lengths and doping levels was measured, as shown in Figure 4.8.

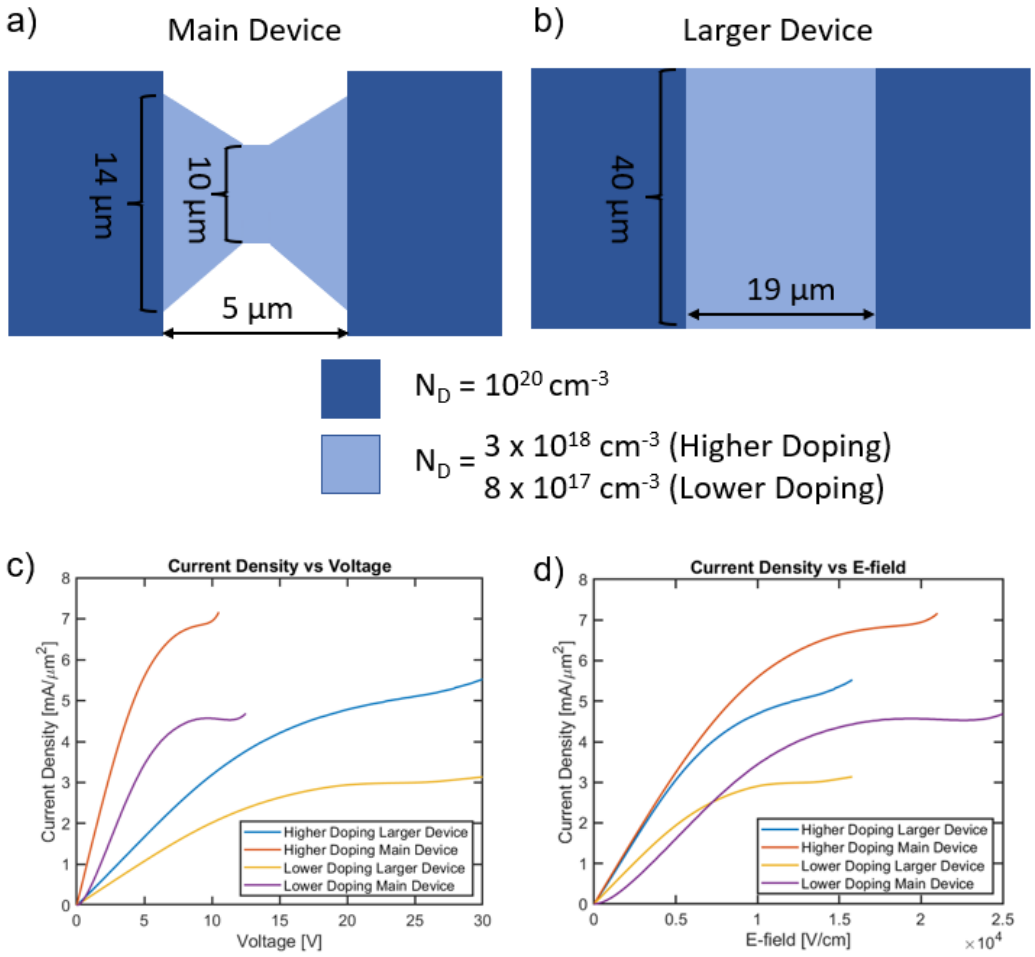


**Figure 4.8 - Schematics of the two types of devices tested. (a) Main devices from the text, (b) Larger devices. Each type of device was tested for both levels of interior doping, giving a total of 4 measurements. (c) The larger devices took larger amounts of current to reach saturation values, but when considered against (d) approximate electric field through the channel, all devices saturated around the same electric field magnitude (1 x $10^4$ V/cm).**

In Figure 4.8 devices that are the main subject of investigation in this work are denoted as "main device" and the other devices tested are denoted as "larger device." The larger devices have a channel length of 19 μm (~4x the main devices) and a channel width of 40 μm (3-4x the main devices). In addition, the larger devices have a constant channel width, not the tapered bow-tie shape of the main devices, as depicted in Figure 4.8a,b. Both types of devices were tested at both interior doping levels investigated in the main text. As shown in Figure 4.8c, the larger devices take larger applied voltages to reach velocity saturation. However, all devices reach saturation at the same channel electric field magnitude (~1 x $10^4$ V/cm), which is consistent with literature [194], [199]. In these devices, this result implies that there is a nonlinear increase in phonon production above a certain applied voltage (i.e., E-field), resulting in increased heating rates.

Considering a system below the saturation region, additionally knowing that mobility decreases with increasing doping ($\mu_n$ is ~2× lower at room temperature for the higher-doped devices [153]). Since the lower-doped devices have higher mobilities and below velocity saturation $v_{drift} = -\mu_n E$ is a valid assumption, we can thus conclude that the average carrier kinetic energy in the lower-doped device is higher ($E = \frac{m^* v_{drift}^2}{2}$). As the E-field continues to increase with increasing voltage, the kinetic energy of the carriers in both devices also increase, but the lower-doped devices are able to reach the optical phonon scattering regime at lower fields. As can be seen in Figure 4.7b, there is significant overlap in the device heating performance as a function of the applied power. However, once the lower-doped device reaches velocity saturation conditions (4 mW/μm at 7 V), the amount of heat generated greatly increases. As the E-field continues to increase beyond this point, the electrons in the channel emit optical phonons at a higher rate, increasing the amount of heat generated, due to the time required for optical-acoustic phonon

decay. The trend from pre-saturation conditions is continued using the dotted orange line to highlight this abrupt increase in heat generation in Figure 4.7.

Unexpected behaviors of the doped heaters has been shown in the current saturation range of operation exhibited at higher voltages (Figure 4.7a). We hypothesize the increased emission rate of optical phonons in devices operating at current saturation lead to a second, more efficient heating regime in these devices. Lower-doped devices are able to reach this regime at lower powers, as the average energy of a carrier is higher at a given input power, therefore outperforming higher-doped devices when strictly speaking about input power vs. temperature raise (Figure 4.7b). However, for applications that are limited to on-chip voltages (<5 V) traditional thinking still holds true and higher-doped devices do reach higher temperatures at lower voltages (Figure 4.7a).

## 4.4 PIN Results

### 4.4.1 Device Operations

The IV curves during Raman measurements for all devices are shown in Figure 4.9. As before, the measured current for each device is normalized by device width ($W$) to facilitate comparison between the different device geometries. As can be seen through the spread of points in Figure 4.9, there is a large spread among the different PIN devices (likely due to the high requirements for consistent fabrication of these devices). To further investigate the spread in performance, other PIN devices located on the same chip were characterized to determine if the spread originated in geometric effects or was based elsewhere.

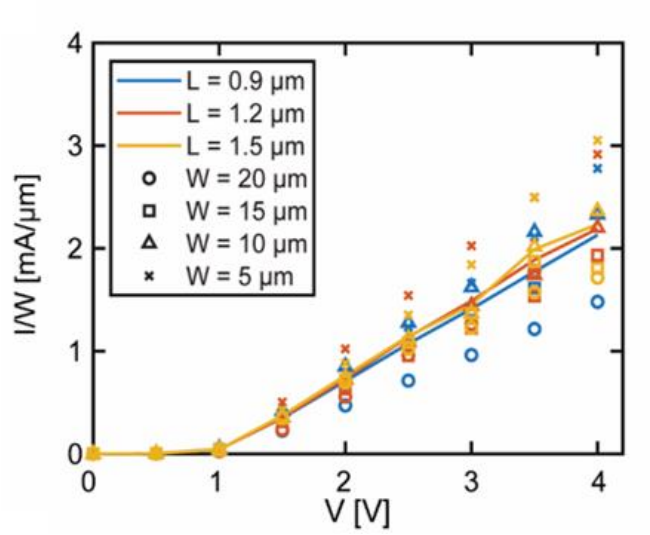


**Figure 4.9 – IV performance of the PIN devices. The solid lines are average IV performance, one for each length of the PIN devices, and one for each doping of the doped devices. Device *L* are indicated by point color, and device *W* are indicated by point shape (e.g., the device with *L* = 1.2 µm and *W* = 10 µm has data points that are orange triangles).**

### 4.4.2 PIN Device Reliability

To investigate the origin of the wide variation observed in the IV performance of the devices, the actual geometries of the devices were inspected via scanning electron microscopy (SEM), an example of which is shown in Figure 4.10. While this imaging modality is unable to verify if any dopants diffused into the intrinsic region, it does verify that the implanted regions were properly placed. In addition, any movement of dopants in these devices should be minimal or at least similar in each device as they are all subject to the same processing history. The results of these inspections are summarized in Table 9, and line up extremely well with their expected values. As such, the source of the spread in device performance must be rooted elsewhere.

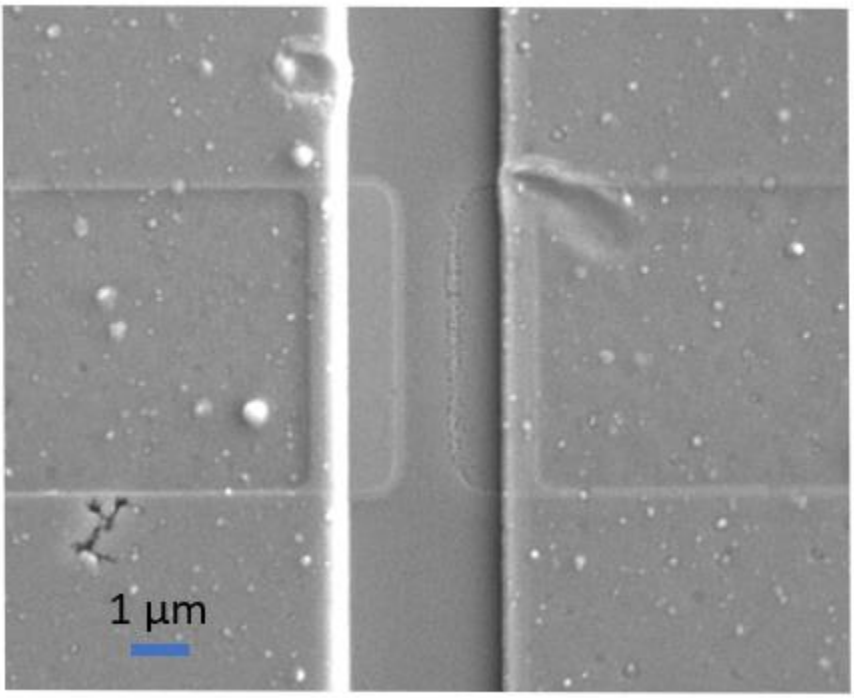


**Figure 4.10 – SEM image of an inspected device to verify correct geometery.**

**Table 9 – Comparison of desired device geometries compared to the measured features.**

| Device | Target *L* | Actual *L* | Target *W* | Actual *W* |
|---|---|---|---|---|
| **1** | 0.9 | 0.814 | 20 | 20.2 |
| **2** | 0.9 | 0.811 | 15 | 15.4 |
| **3** | 0.9 | 0.782 | 10 | 10.2 |
| **4** | 0.9 | 0.834 | 05 | 05.1 |
| **5** | 1.2 | 1.107 | 20 | 20.4 |
| **6** | 1.2 | 1.017 | 15 | 15.1 |
| **7** | 1.2 | 1.014 | 10 | 10.2 |
| **8** | 1.2 | 1.076 | 05 | 0.51 |
| **9** | 1.5 | 1.360 | 20 | 20.3 |
| **10** | 1.5 | 1.358 | 15 | 15.3 |
| **11** | 1.5 | 1.406 | 10 | 10.3 |
| **12** | 1.5 | 1.409 | 05 | 05.2 |

Other PIN devices on the same chip were electrically characterized to further investigate the performance variations. These devices were designated by 6 groups. Each device in these groups have the same level of $n^{++}$ and $p^{++}$ doping as the PIN devices of focus ($10^{20}$ $cm^{-3}$), and in each group each device nominally has the same geometry. For each device measured, 5 IV sweeps were performed to measure the consistency of the device performance. Group 1 (Figure 4.11a) is a large array of PIN devices, of a similar structure to the single-doped heaters investigated, but with larger doped areas and a smaller intrinsic region. Group 2 (Figure 4.11b) are large arcs, with a small intrinsic region. Group 3 (Figure 4.11c) are extremely large, straight PIN diodes, with a small intrinsic region. In group 3, devices 1-4 are all 800 μm wide, with an intrinsic region length of 1.6 μm. Devices 5-8 are 960 μm wide, with a smaller intrinsic region length of 1 μm. Groups 4 (Figure 4.11d), 5 (Figure 4.11e) and 6 (Figure 4.11f) are all of a similar structure to Group 1, but were fabricated in two orientations to test if the directionality of the devices had an effect on the fabrication process. Group 4 is parallel to group 1, while groups 5 and 6 are perpendicular. Of the two vertical device groups, group 6 has a larger intrinsic region.

Compared to the steady state IV curves shown in Figure 4.9, these devices were swept rather quickly, with a dwell time of 55 ms at each voltage. This should help ensure minimal movement of dopants through the device. As can be seen by the IV figures in Figure 4.11, not only is there a large variation in device-to-device measurements, each device also has a significant cycle-to-cycle variation. From these results it can be concluded that PIN diodes are extremely sensitive to small variations and imperfections in the fabrication process. As such, in order to promote reliable PIN diode performance, efforts must be invested into optimizing device design and fabrication processes must be invested into the fabrication processes.

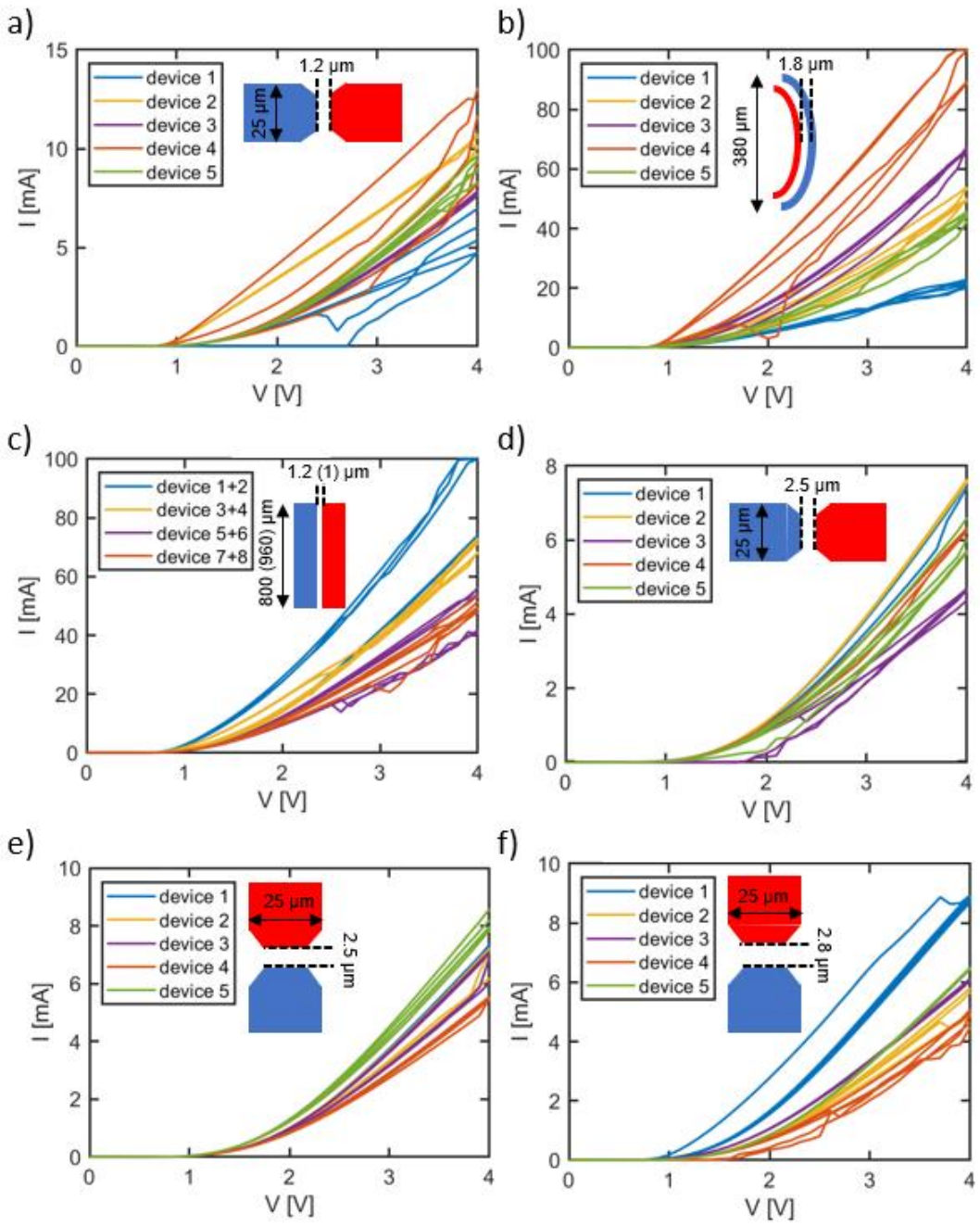


**Figure 4.11 – IV sweeps of various devices to investigate device consistency. All devices were on the same chip and subject to the same fabrication processes and history.**

### 4.4.3 Temperature Results

Even with the variation in the device performance, operating temperature for each device was measurable at a given voltage and power load. Figure 4.12a shows the corresponding device temperature as a function of applied voltage, and Figure 4.12b shows the calculated temperature as a function of applied power obtained using Raman thermometry. The temperatures for the PIN microheaters were grouped by device channel length (*L*). Heating in these devices should be approximately linear to applied power (quadratically to applied voltage in Figure 4.12a) due to Joule heating, although the PIN devices were expected to be slightly non-linear due to additional heating from carrier recombination at the P/I and I/N interfaces [98].

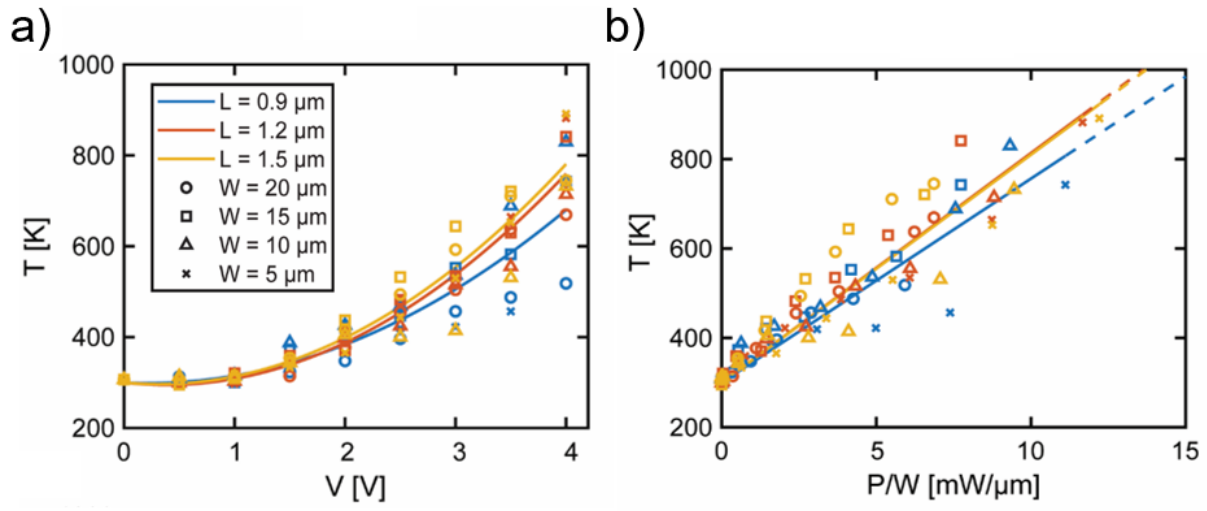


**Figure 4.12 - Results of the Raman thermometry measurements for PIN devices. (a) Calculated device temperature vs. applied voltage. Device *L* are indicated by point color, and device *W* are indicated by point shape (e.g., the device with *L* = 1.2 μm and *W* = 10 μm has data points that are orange triangles). (b) Results of the Raman thermometry measurements shown vs. normalized applied power. PIN devices are grouped by device *L*, and linear trend lines are fit for the data for each (both the 1.2- and 1.5-μm-long devices had similar trendlines, resulting in overlapping lines).**

As with previous presentations in this work, each group of devices in Figure 4.12a (3 groups of 4 PIN devices), was fit with a linear trend (quadratic for Figure 4.12b) to compare the relative heating efficiency of the devices. While it was expected that channel length would be the dominant parameter to influence current and heating in the PIN devices, significant variability in both the IV and thermal heating efficiency (see Figure 4.9, Figure 4.12) was observed. This concurs with the previous observation and characterization of PIN devices' greater sensitivity to fabrication processes in addition to specific device geometry effects.

While the initial goal of this work was to compare different intrinsic region lengths of PIN diodes, it became abundantly clear that a more important parameter was device width, *W*. With this in mind, temperature vs. power results were then normalized by device width, as the smaller (low *W*) devices all consistently outperform the larger (high *W*) devices due to the smaller volume being heated. In addition, it would appear that the smaller *L* devices heat much less efficiently than the wider devices, as evidenced by the lower slope of the trend line in Figure 4.12. This under-performance is due to the lower volume of material being heated, as well as the closer proximity of the contacts which act as heat sinks. In this steady state measurement, both of those factors result in lower total temperatures, although their performance in pulsed applications are projected to be better in terms of heating speed than wider devices [98].

As can be seen through the spread of points in Figure 4.9 and Figure 4.12, there is still a large spread among the different PIN devices. In comparison, the single-doped microheater devices heat more consistently, as well as more efficiently than the PIN devices (admittedly in part due to their tapered channel), depending on the interior region doping level, as demonstrated previously. Although this would seem to indicate doped microheater devices might be more useful in the field, it is worth emphasizing that PIN heaters still offer a high potential for heating

efficiency, as evidenced by their temperature vs. total applied power performance, as well as their performance for voltages traditionally available on chip (<5 V).

### 4.4.4 Device Damage During Operation

After performing Raman thermometry, it was observed that holding the device at high temperatures and current densities for several minutes cause significant damage to the $p^{++}$ terminal of the forward-biased PIN devices. This was consistently observed across the majority of the PIN devices tested. Figure 4.13 depicts an example. However, this damage was not observed in the doped devices. One possible explanation could be due to a larger separation of the metal contacts from the center region of highest temperature in the case of the doped devices. For the PIN devices, we attributed the cause of this damage to the relatively low melting temperature of the metal contacts (Al) which are exposed to high temperatures over several minutes. The damaged devices were imaged using scanning electron (SEM) and atomic force microscopy (AFM). AFM topographic scans revealed that damaged regions of the electrode indeed matched the ~200 nm thickness of the deposited Al layer (Figure 4.13c,d). SEM images of the device (shown in Figure 4.13b) also appear to show removal of the Al layer while the Ti/TiN adhesion and barrier layers remain undamaged after steady-state testing.

While steady-state operation can provide insights into device aging, these microheaters are intended to operate under pulsed conditions to reversibly switch optical PCMs. To investigate the potential effects that pulsed operation may cause on device performance and to observe which pulse conditions may cause similar electrode damage, endurance testing was carried out on new devices from both types of microheater as discussed in Section 4.5.

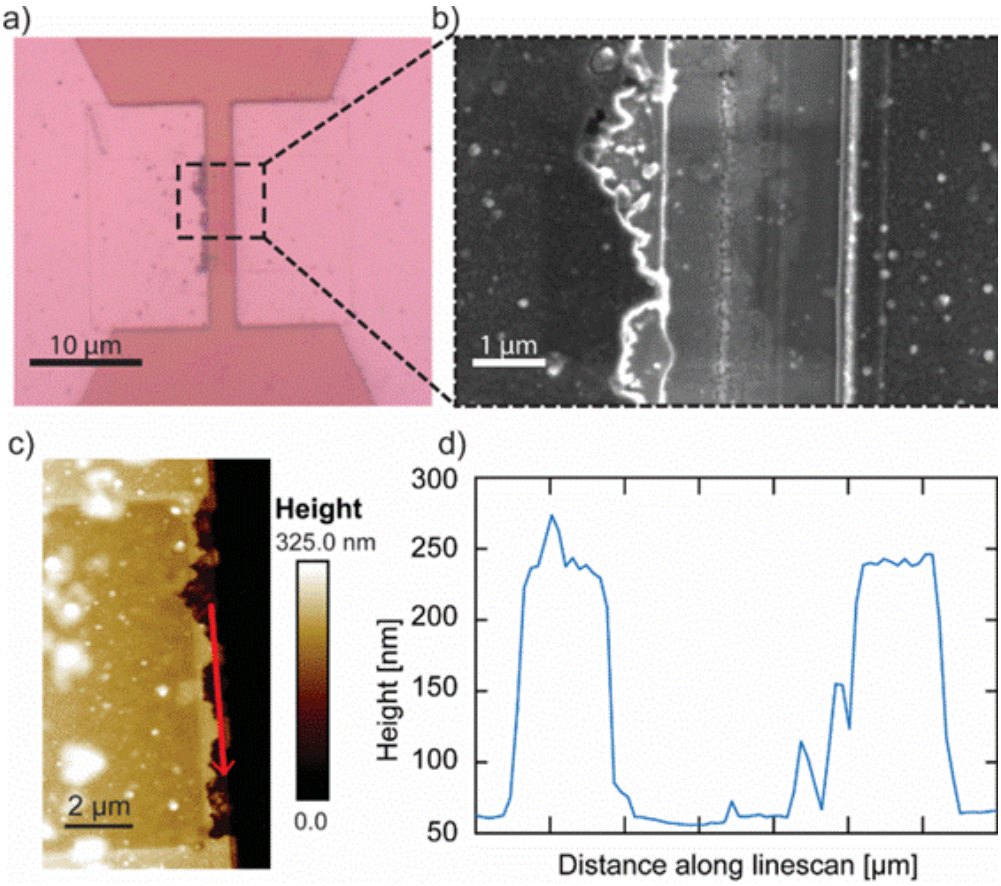


**Figure 4.13 – Example of damage observed during Raman thermometry process. (a) Device after being powered. (b) Scanning electron microscope image showing the contact disappearance. In addition, brighter spots in the midst of the channel indicate that the 10 nm $SiO_2$ passivation layer has burned off, allowing the underlying thin-film Si layer to shine brighter. The slightly darker area denotes carbon burn off from a previous, higher magnification scan. (c) Atomic force microscope image of the device (red line depicts the path of a line scan). (d) AFM line scan results showing the resulting step size is ~200 nm, implying the contact edge has completely delaminated and disappeared.**

## 4.5 PIN and Single-Doped Comparison

### 4.5.1 Device Reliability

To investigate the potential effects that pulsed operation may cause on device performance and to observe which pulse conditions may cause similar electrode damage, endurance testing was carried out on new devices from both types of microheater, as shown in Figure 4.14. For both the PIN and doped microheaters, a width of $W$ = 10 µm was chosen ($L$ = 0.9 µm for the PIN device, $n$ = 3 x $10^{18}$ $cm^{-3}$ for the doped device). During testing, up to 10 million pulses were applied to a test device, with varying pulse widths of 1 µs, 10 µs and 1 ms. To achieve a consistent power dissipation of 7.4 mW/µm in both devices, a pulse amplitude of 4 V and 8 V was used for the PIN and doped microheaters, respectively. The applied pulses had a 50% duty cycle for each test. At each decade, a short 400 ns long read pulse was applied to characterize the electrical performance of the stressed device. In addition, at the end of the 10 million pulses for each pulse width an IV sweep was performed, and the device was inspected using optical microscopy. Visible damage was not observed on the PIN device until after endurance testing using the 1 ms pulse width. No damage was observed in the doped device after endurance testing which agreed with observations from the Raman thermometry experiments. Although the damage did in fact occur in the PIN device as shown in Figure 4.14e, the electrical performance of the device as measured by IV was not significantly affected after cycling beyond a moderate increase in forward bias current.

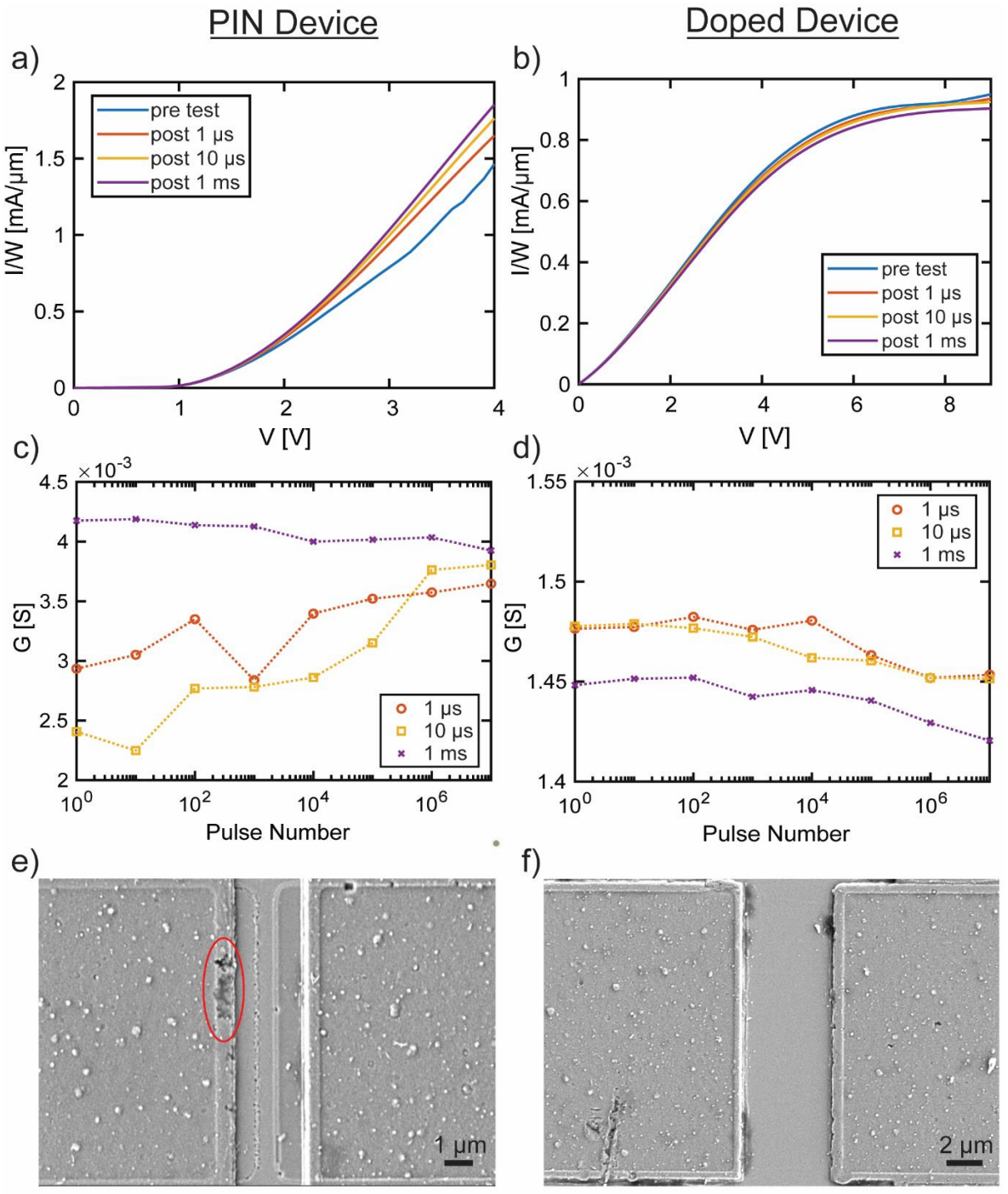


**Figure 4.14 – Results of endurance testing of the devices. IV sweeps of the (a) PIN and (b) n-doped device taken after each set of pulse widths. (c),(d) Device conductivity was measured after every decade of cycling. SEM images of the (e) PIN and (f) doped devices post testing showing the onset of damage in the PIN microheater (highlighted area), and lack of dmaage in the doped device.**

### 4.5.2 Overall Comparison

When comparing PIN microheaters with doped resistive microheaters, it is important to note some relative advantages and disadvantages of both designs. First, while not explored here, it is expected that the maximum intrinsic channel length must be limited to sub-10 μm to operate at reasonable applied voltages. This makes doped microheaters more appropriate for scaling to larger area devices (such as reconfigurable metalens pixel arrays). Secondly, to prevent electromigration, RF pulses can be used to heat doped microheaters which is an impossibility for microheaters based on PIN diodes. Finally, it seems that fabricating consistent embedded PIN devices is more challenging than doped devices, both in regard to mitigating the large degree of randomness observed in the IV performance of the devices and further optimizing device endurance. However, the potential for operating at low applied voltages (<5 V) with low optical insertion loss warrants further investigation, improvement and optimization. PIN and doped microheaters can offer comparable optical attenuation properties, (~0.4-0.02 dB/μm for devices of intrinsic region lengths 0.9-1.5 μm, shown in Figure 3.7d, [98] compared to 0.03 dB/μm for doping levels like those found in [183]). Regardless, the PIN devices tested here compared favorably with single-doped devices for the dimensions tested. With more improvements in both device structure, and fabrication methods, PIN heaters should have a bright future.

## 4.6 Conclusion

This work has studied the heating response of two different types of embedded doped Si heaters, PIN and single-doped devices. Specifically, the geometric effect of the intrinsic region length, and device width for PIN diodes was investigated. The PIN diodes were found to have a larger spread in device operation then expected, and as such are less consistent then the single-doped microheaters, as fabricated. Both these devices were held at high DC power, and their steady state temperatures measured through Raman thermometry methods, and it was found that both types of devices can reach significantly high temperatures under similar power density loads. Unexpected heating performances at higher power loads was also demonstrated, showing lower doping can result in more efficient heating in single-doped devices. During measurements damage was observed on the positive contacts of each PIN device, but notably not at all on the single-doped devices. The impact of this damage on electrical performance was investigated through endurance testing. The endurance testing revealed that while damage does begin to occur at high enough ON time (10 million 1-ms-long pulses) the damage did not affect device operation. From this investigation, it was concluded that both devices have high potentials for large scale embedded heaters for photonic devices, but PIN devices of this nature might require a higher investment in device design and fabrication processes, while single-doped microheater devices are, at present, simpler and more reliable in fabrication.

# 5.0 PN Heaters

Although PIN and single-doped devices have been investigated previously for their heating potential, PN diode performance in the same application is intriguing. Although PN junctions can suffer from larger optical attenuation than the other structures, this device style is feasible with careful control of the depletion region and has been implemented in several different devices [49], [185], [204]–[212]. Thermally, PIN diodes have local hotspots at the P/I and I/N junctions as discussed previously. However, these hotspots are typically far away from the phase change material (PCM) and a significant portion of generated heat is immediately conducted away by the metallic contacts. Single-doped devices are more uniform in heating, but the lightly doped region length is longer than the PCM patch, causing loss of heat and increased challenges in controlling temperature. Comparatively, PN diodes, will likely heat significantly via Joule heating throughout their body, but will also have significant local heating due to recombination at the P/N junction. This junction can be centered close to the PCM, which may enable improved thermal control of the PCM.

## 5.1.1 PN Junctions in Optical Devices

As discussed in Section 1.1, optical modulators based on silicon structures mostly function through the plasma dispersion effect, although thermo-optic effects have also been used [213]. Although the plasma dispersion effect was first implemented through PN structures, most subsequent work utilized PIN structures since they are a majority carrier driven device (compared

to the minority carrier driven PN devices), and accordingly have higher levels of moving charges. By forward biasing the PIN diode, free electrons from the *n*-region and free holes from the *p*-region are injected into the center intrinsic region, strongly modulating the optical properties [204]. While this is extremely efficient and able to strongly modulate the refractive index at low voltages (~1 V), it is limited in speed due to the recombination times of carriers (~ ns) [204], [207], [211]. For faster operating speeds, PN diodes can be reverse biased to modulate the size of their depletion region, thus changing the amount of free carriers in the optical path [185], [204]–[211]. This process is significantly faster as it is limited only by the capacitance of the junction, and carrier velocity saturation through the device [204]. In addition, while the modulation effect is volatile in nature, it is relatively power efficient when not switching. Power is only consumed by small leakage currents. However, significantly less carriers are transported in a PN diode than a PIN counterpart, and so the optical modulation effect can be much weaker.

### 5.1.2 Design of PN Photonic Structures

Multiple different PN junctions have been designed and implemented for photonic devices, as shown in Figure 5.1. It is convenient to classify them based on the orientation of the junction, vertical (Figure 5.1a) or horizontal (Figure 5.1b). While vertical junction devices are more complex in terms of fabrication, promising devices have been demonstrated, with operation speeds of up to 40 Gbit/s [185], [206], [211]. One such device had doping concentrations similar to those showed in Figure 5.1a, but additionally had a complex graded doping profile in the *n*-region, with $1.5 \times 10^{17}$ $cm^{-3}$ at the junction to match the *p*-region, and increasing to $3 \times 10^{17}$ $cm^{-3}$ at the very top of the waveguide [185]. Extremely good modulation performance was demonstrated in these

devices, with optical losses of 0.0018 dB/μm but with a low extinction ratio of only 1 dB [185]. Due to the complexity required in fabrication of these devices, horizontal junction devices will be the focus of this work.

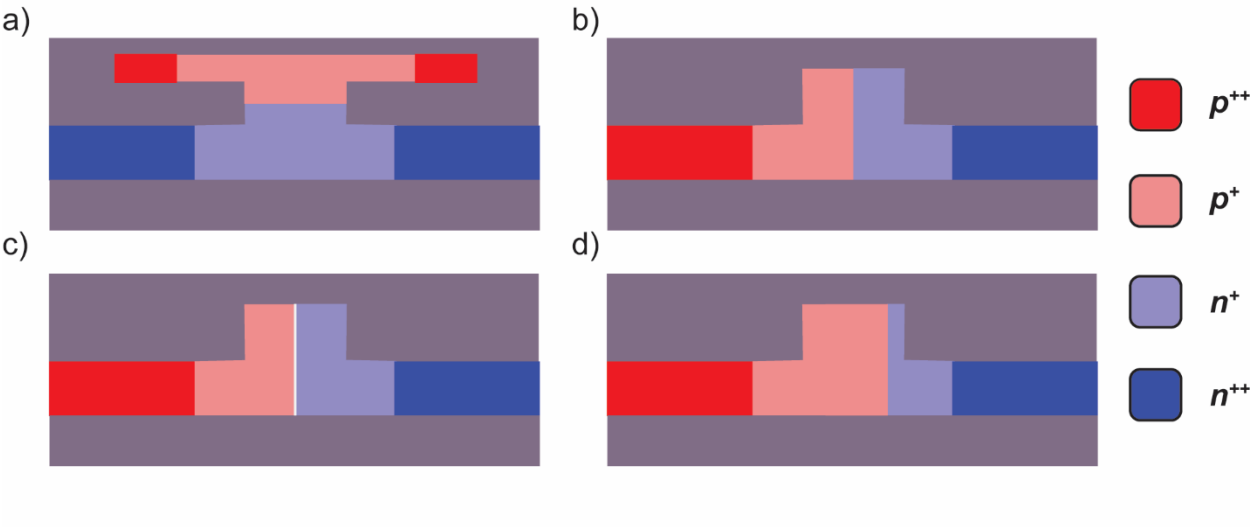


**Figure 5.1 – Examples of different PN junction devices for photonic devices. (a) Basic example of a vertical junction device. (b) Basic example of a symmetric horizontal device. (c) A basic horizontal device with a thin intrinsic region inserted to reduce junction capacitance. (d) A basic horizontal device with an offset junction, to make the waveguide area majority p-type.**

Within the design space of horizontal PN diode rib guides, there are numerous geometric design aspects that can be taken into account for optimizing device performance, including rib height and width, sidewall angles of the rib, how the distance from the optical path to the heavily doped areas, and so on. Additional complexities such as thin intrinsic regions in between the *p*- and *n*-regions (Figure 5.1c) to reduce junction capacitance can be considered as well. From there, the doping concentrations of both the heavily doped and lightly doped junction regions should be examined. The heavily doped regions need to be both sufficiently doped to ensure good ohmic contacts to the leads, but they also need to ensure low resistance access to the junction to ensure efficient biasing of the junction. The doping level of the lower-doped interior region then needs to

be optimized, as it strongly affects the optical performance of the device. The impact on heating performance of these different regions will be discussed in Section 5.1.5.

When designing horizontal PN junctions for photonic applications, it is important to understand the different interactions between *p*- and *n*-type Si, as originally outlined by Soref and Bennet [6], [185]. It is clear from their calculations that *p*-type Si is able to achieve a larger refractive index change with lower optical absorption levels. Due to this, asymmetrical junctions that have the majority of the waveguide be *p*-type have been demonstrated to provide larger optical modulation ranges, as shown in Figure 5.1d. On the other hand, some work has been done using majority *n*-type waveguides. This concept leverages the faster electrical depletion of *n*-type Si; these devices should theoretically lead to faster electrical performance [208]. While the positioning of the junction is an important facet in designing PN devices for optical performance, it's impact on heating is expected to be minimal, and will be explicitly investigated in Section 5.1.6.

### 5.1.3 Integration of PCM into PN Structures

As mentioned, the modulation range of PN devices can be fairly limited due to the amount of carriers being moved. Integrating PCM patches onto PN devices may enable the modulation range to be extended. Careful control of the phase of the PCM can help set the optical operating point, and small variations in the reverse biasing level can then tune the modulation as desired. If larger variations are then needed, the phase of the PCM can be switched again by quickly forward biasing the PN device, and then immediately returning to reverse bias to enable further modulation.

### 5.1.4 Simulation of PN Heaters

To successfully integrate PCMs into PN structures, the heating performance and efficiency of PN diodes needs to be investigated. Using COMSOL Multiphysics, a temperature dependent semiconductor model similar to that stated in Section 3.2 was established. The starting model was based on devices that were fabricated. A cross section is depicted in Figure 5.2a. The device features three regions of doping for each polarity. The *p*- and *n*-regions that form the diode junction are doped ~$10^{17}$ $cm^{-3}$ each, the $p^+$- and $n^+$-regions are doped ~$10^{18}$ $cm^{-3}$ each, and the heavily doped $p^{++}$- and $n^{++}$ -regions are doped ~$10^{20}$ $cm^{-3}$ each to ensure good ohmic contacts to the devices. The inclusion of the mid-level $p^+/n^+$ doping lowers the inline resistance of the device while maintaining low levels of optical attenuation. The junction for these devices was positioned in the middle of the rib. The benefits of offsetting the junction was assumed to be minimal (an assumption to be confirmed by subsequent simulation). For the PCM, an optical stack consisting of a thin layer of 31 nm of $SiO_2$, 17 nm of GST-225, and finally 10 nm of $SiO_2$ was considered, similar to the structure found in [214]. The bottom layer of $SiO_2$ electrically isolates the PCM, and the top layer provided passivation. To simulate real fabrication conditions, additional side wall optical stacks are added on either side of the waveguide rib, as pictured in Figure 5.2a.

The established temperature dependent semiconductor model was swept from 0–4 V applied to the positive terminal, reflecting the forward-bias conditions of operation most important to this work. The real device being investigated is a ring resonator, with contact lengths about 3x larger than the device length. In addition, the heavily doped $p^{++}$ and $n^{++}$ regions are not uniformly doped, with most of the dopants being concentrated near the surface to ensure ohmic contacts. To encapsulate the changing geometries and non-uniform doping effects, an empirical fitting value

was fit to the mobility models established in Section 3.2. As can be seen in Figure 5.2b, the performance of the model matches the experimentally measured values well for an empirical fitting value of 3.

With this established model, two design parameters were investigated to determine their impact on the heating performance of this structure. Since the doping level of the interior *p* and *n* regions strongly affects the optical performance of the device, they are left unchanged and the inclusion of the $p^+$ and $n^+$ regions is initially investigated. Additionally, the impact of offsets in the junction were investigated to assess if they offer additional heating benefits. The impact of the positioning of the heavily doped regions is easily calculated through Equation 3-31, and is subsequently discussed relative to other devices.

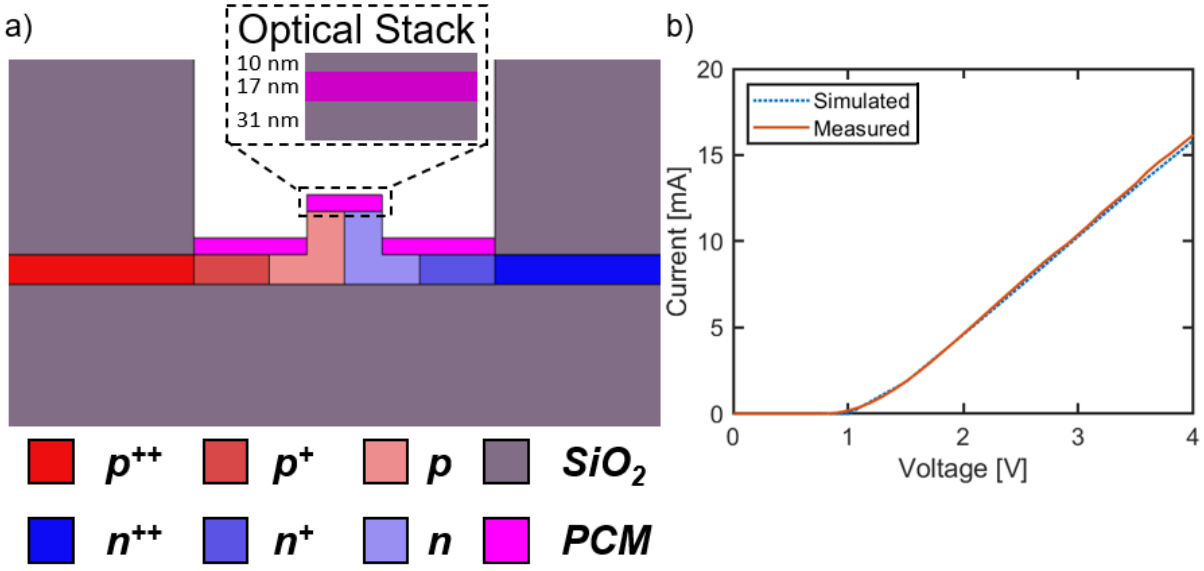


**Figure 5.2 – Simulated device structure as well as initial comparison to experimental data. (a) Schematic of fabricated PN modulator device for PCM switching. The three PCM patches in the diagram are optical stacks with actual geometries as shown in the inset. (b) IV performance of the fabricated device (solid line) and simulated model (dashed).**

### 5.1.5 Inclusion of the $p^+$ and $n^+$ Regions

As discussed, the inclusion of the interim $p^+$ and $n^+$ regions was an attempt to lower the inline resistance of the device while maintaining acceptable levels of optical attenuation. To investigate their impact on heating performance, simulations using the established model were performed using 100 ns driving pulses, and the $p^+$ and $n^+$ regions had their doping levels swept from ~$10^{17}$ to $10^{20}$ $cm^{-3}$, and the results of which are shown in Figure 5.3. As can be seen, there is significant improvement in temperature of the GST (Figure 5.3c,e) with increasing doping, specifically as the device moves from $10^{19}$ to $10^{20}$ $cm^{-3}$. This is because there is significant recombination heating occurring at the $p^{++}/p^+$ and $n^{++}/n^+$ interfaces. With equivalent, all of the recombination occurs closer to the waveguide, and accordingly the heating performance increases. Of note, in these simulations the max temperature of the Si was kept well within a feasible range, as shown in Figure 5.3d. Notably, the max temperature of the Si all converged at higher applied powers (Figure 5.3f), which is expected as the device moves closer to the intrinsic region of thermal operation.

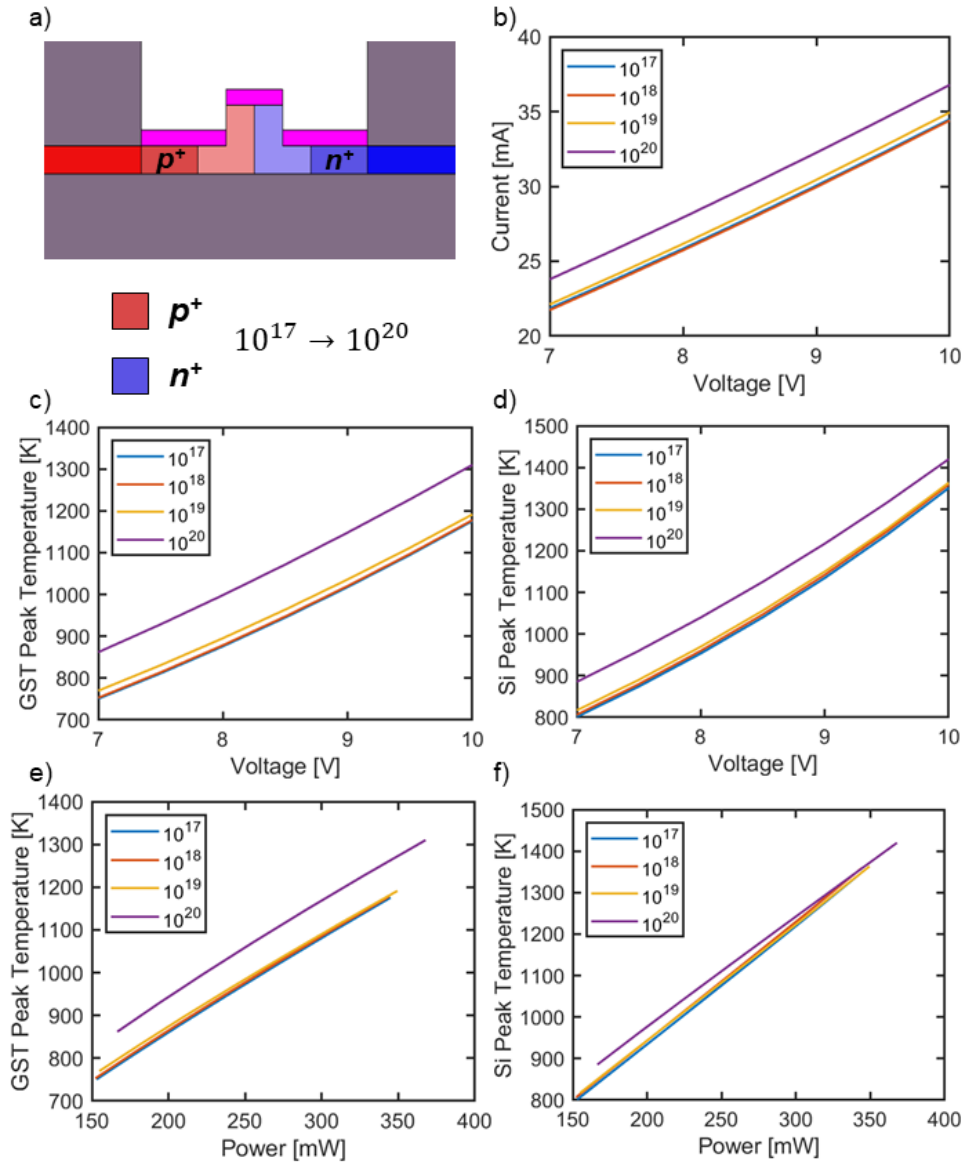


**Figure 5.3 – Initial simulation results of sweeping the interim $p^+$ and $n^+$ regions. (a) Schematic of the device simulated, showing the doping range used in simulation. (b) The device IV performance over the voltage range 7–10 V required in order to properly heat the GST. Doping is revealed to have a minor impact under levels of $10^{20}$ cm$^{-3}$. The peak temperatures of the (c) GST and (d) Si, showing that the GST was able to reach its melting temprature while keeping the Si well within an acceptable heating threshold. Peak temperatures are provided for the (e) GST and (f) Si vs. applied power, showing the clear improvement associated with doping levels of $10^{20}$ cm$^{-3}$. Notably, in (f), the temperatures overlap at higher power levels, likely reflecting the intrinsic regime of operation for temperature effects.**

To further expand upon the improvement offered by the heavier doping, the heat generated through the body of the device was measured. Due to the changing cross section of the device, the heat generated was normalized based on the height of the sample, as described in Section 3.2.5. For each doping level, the minimum voltage required to heat the GST above its melting temperature was selected. At that voltage the relative contributions from Joule and recombination heating, shown in Figure 5.4a-d. To better understand what is happening at each doping level, just the contributions from Joule heating (Figure 5.4e) and recombination heating (Figure 5.4f) are plotted. As described, at lower doping levels there is significant recombination heating at the $p^{++}/p^{+}$ and $n^{++}/n^{+}$ interfaces, but at $10^{20}$ $cm^{-3}$ doping levels, the recombination moves significantly closer to the GST. Finally, for each of the doping levels investigated, the quench time and quench rate for each was calculated at the minimum voltage required to achieve GST melting. As shown in Figure 5.5 there is a significant decrease (increase) of quench time (rate) for higher doping levels.

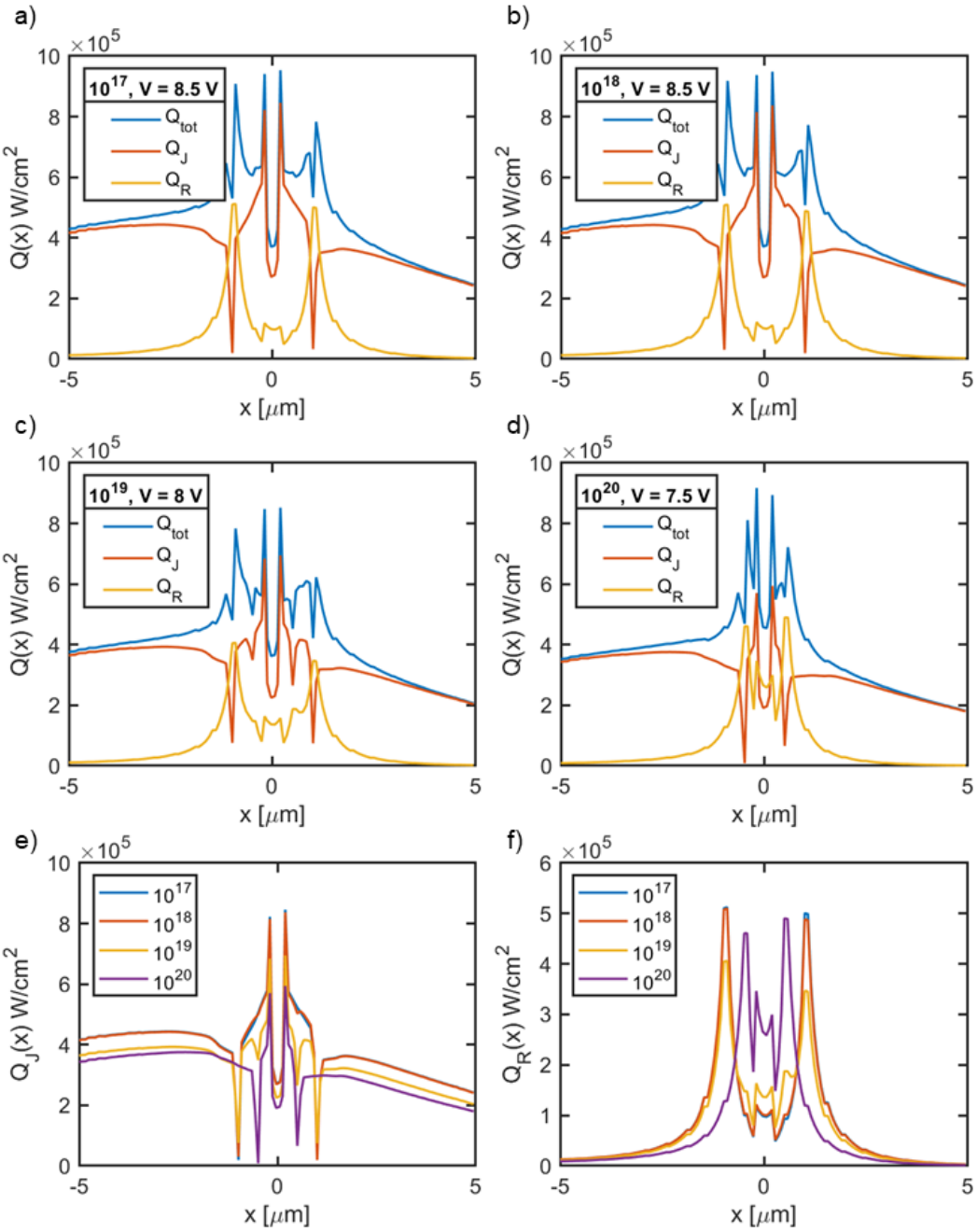


**Figure 5.4 – Normalized heat generated through a PN device with changing $p^+$ and $n^+$ doping. (a)-(d) Heat profiles of the simulated devices for $p^+/n^+$ doping levels $10^{17}$-$10^{20}$ $cm^{-3}$ showing the total normalized heat generated ($Q_{tot}$), as well as the contirbutions from Joule heating ($Q_J$) and recombination heating ($Q_R$). Comparison of the different heating levels of the devices for (e) $Q_J$ and (f) $Q_R$ showing the evolution of heating performance of the devices with changing doping levels.**

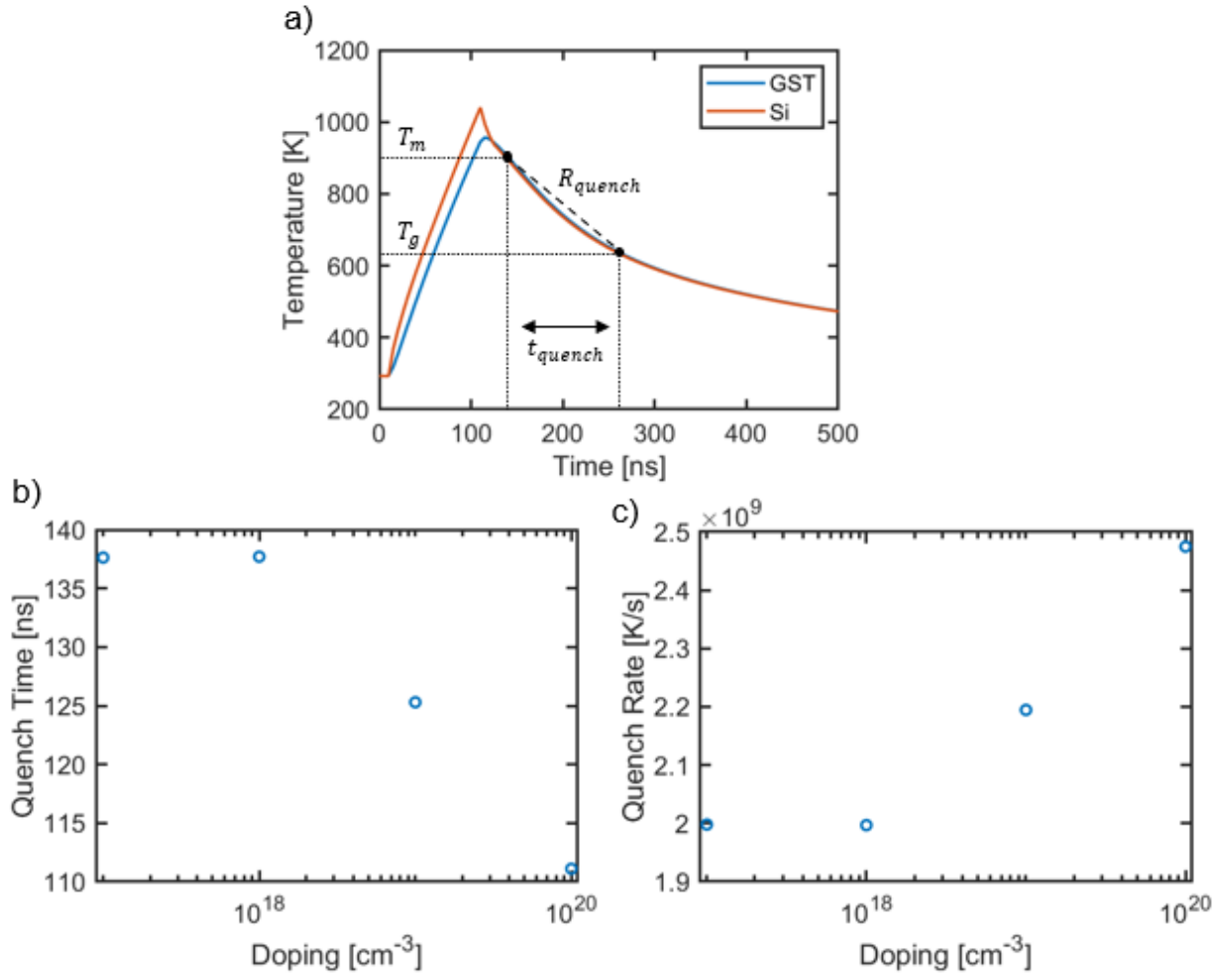


**Figure 5.5 – Quench time and rate as a function of $p^+$ and $n^+$ doping levels. (a) Schematic of calculation of the quench time ($t_q$), as well as the quench rate ($R_{quench}$). Calculated (b) $t_q$ and (c) $R_{quench}$ for different doping levels, showing a clear improvement in performance for higher doping levels.**

### 5.1.6 Junction Position Through the Waveguide

As discussed previously, the position of the junction through the rib waveguide can be placed to optimize optical performance. It is either offset towards the *n*-region (making the rib mostly *p*-Si) to increase modulation responses, or offset towards the *p*-region (making the rib

mostly *n*-Si) to increase operating speeds [185], [208]. This effect was expected to have minimal effect on the heating performance.

The established model (with doping levels as described in Section 5.1.4) was simulated using 100 ns pulses of 8 V. The junction position was swept from -0.125 µm to 0.125 µm (rib edges are located at ±0.25 µm) and the three extrema (-0.125 µm, 0 µm and 0.125 µm) are shown in Figure 5.6. As expected, the temperature of the GST had minimal changes (Figure 5.6b), due to slight changes in the overall heat generation of the device (Figure 5.6c). Those variations in overall heat generation arose from slight changes in the Joule heating (Figure 5.6d) as the local hotspots generated from recombination was still dominated by the effects at the $p^{++}/p^{+}$ and $n^{++}/n^{+}$ interfaces (Figure 5.6e). This indicates that positioning of the junction in the rib waveguide can be freely placed to optimize optical performance and will have minimal impact on the PCM switching capabilities of the device.

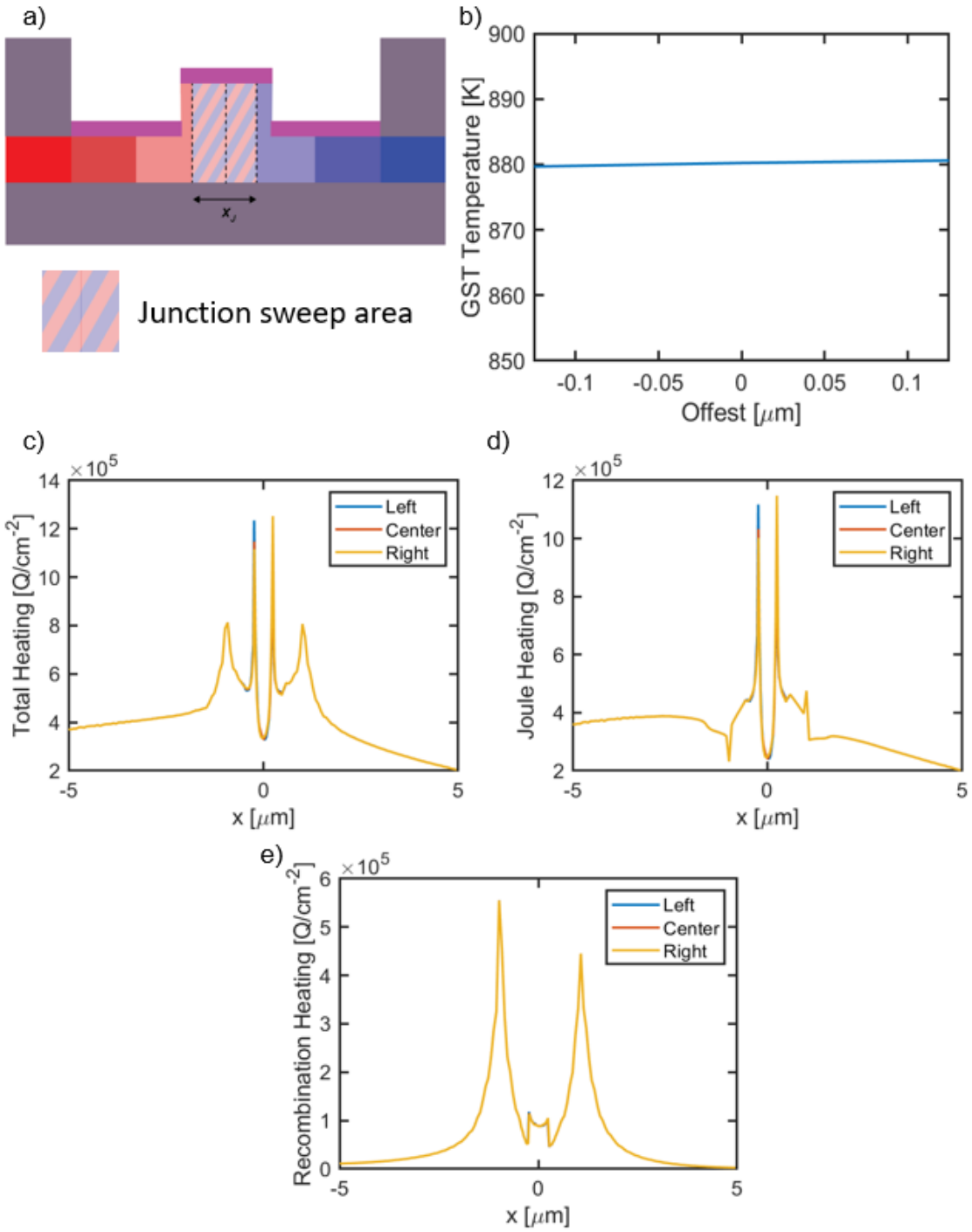


**Figure 5.6 – Effect of positioning of P/N junction on heating performance. (a) Schematic of the device simulated; the striped area shows the possible positions of the P/N junction. (b) Peak temperature of the GST as a function of the junction position, showing minimal changes. The heat profiles of the devices at the 3 extrema, left right and center showing (c) the total heating ($Q_{tot}$), (d) Joule heating ($Q_J$) and (e) recombination heating ($Q_R$).**

### 5.1.7 Overall Comparison of Devices Studied

To facilitate a final comparison of all the devices studied, three simulations were performed. Each device structure used the same geometry: 90 nm thick slabs, 130-nm-tall ribs, and 500-nm-wide ribs. The contacts were placed 4.75 µm away from the rib edges to ensure minimal impact on optical performance. Each device was simulated using 100-ns pulses of 5 V to simulate on-chip voltages, and to ensure the single-doped device was in the first regime of heating described in Section 4.3.3. Each simulation used a 2D temperature dependent semiconductor model similar to that outlined in Section 3.0, while the PN diode device specifically used the mobility scaling discussed in Section 5.1.4. To further simplify the PN model, the $p^+$ and $n^+$ regions were considered to be doped at $10^{20}$ $cm^{-3}$, which also maximized heating performance.

The changing parameters of each device is depicted in their schematic in Figure 5.7b-d. The PN diode investigated the heavily doped regions' distances from the center region (1, 1.5, and 2 µm), as well as doping levels ($10^{18}$, $10^{19}$, and $10^{20}$ $cm^{-3}$). The PIN diode investigated the length of the intrinsic region (0.9, 1.1, 1.2, and 1.5 µm), as well as the doping levels of the heavily doped regions ($10^{17}$, $10^{18}$, $10^{19}$, and $10^{20}$ $cm^{-3}$). The single-doped device investigated the length of the lightly doped channel (1, 2, 3, 4, and 5 µm) and the doping of the channel ($10^{15}$, $10^{16}$, $10^{17}$, and $10^{18}$ $cm^{-3}$). For each device simulation, the heating efficiency FOM (Equation 3-29) and optical losses (Equation 3-31) were calculated for comparison. An optimal device will have high heating efficiencies and low optical losses.

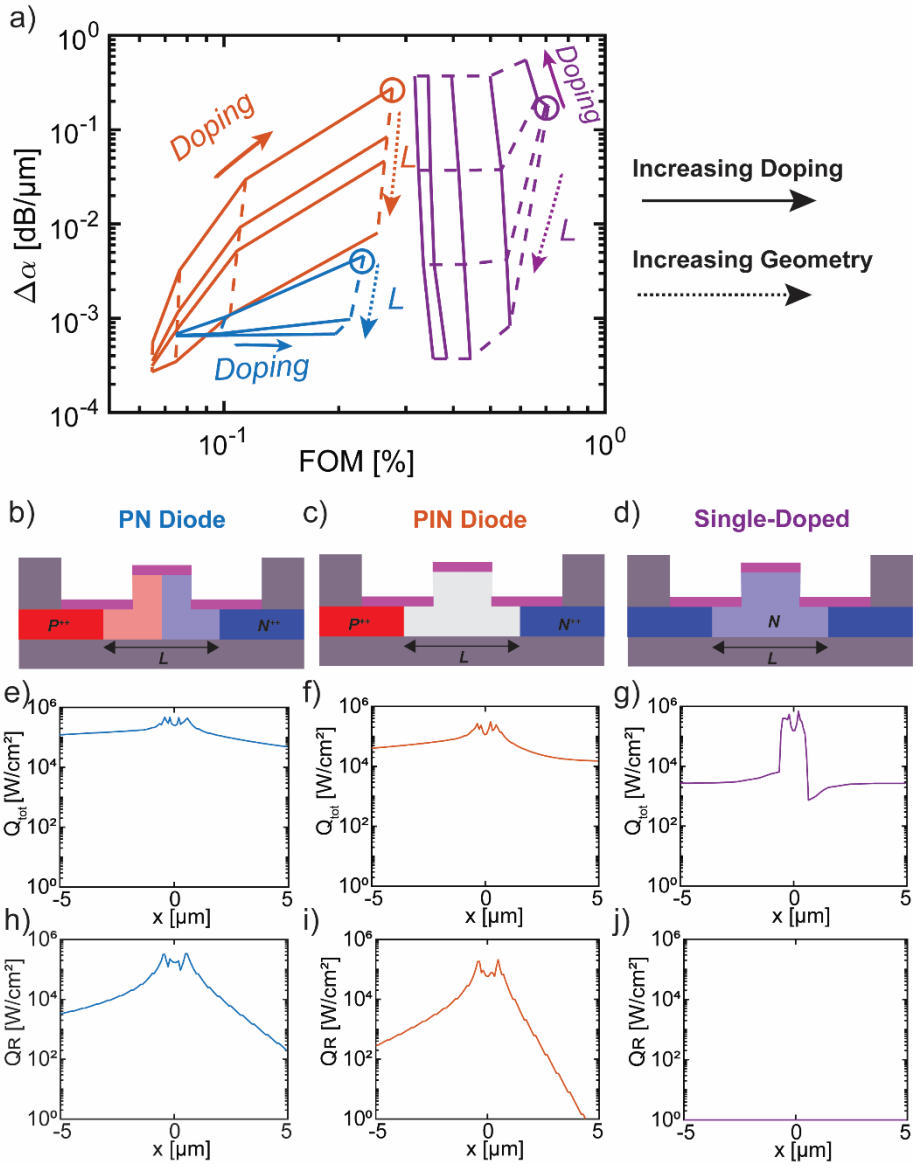


**Figure 5.7 – Final comparison of the design space of all three devices for on-chip voltages. (a) Initial comparison of the PN diode (blue) PIN diode (orange) and single-doped (purple) devices based on their heating efficencies and optical losses. Optimal device configurations will have low optical losses and high heating effecncies, corresponding to the lower right region of the graph. Solid lines represent same doping levels with changing geometry, while dashed lines show same geometries with changing doping. Schematics showing the device configurations, and highlighting the changing variables for the (b) PN, (c) PIN, and (d) single-doped devices. (e)-(g) Heat-generation profiles of the most efficent heating configurations of the three devices, as well as (h)-(j) their contributions from recombination heating.**

From initial inspection of Figure 5.7, it would appear that single-doped devices are the most efficient heater structures of the three. They offer the highest FOM with lowest optical losses. To further investigate the responsible mechanism, heat generated in each device's most efficient heating structure is calculated (Figure 5.7e-g). In addition, each device's contribution from recombination heating is calculated as well (Figure 5.7h-j). Even though there is extremely little contribution from recombination, the majority of the heat generated in the single-doped device is concentrated nearest the PCM. This is extremely interesting; as mentioned before, these simulations were performed with voltages available on chip (5 V) and as proposed in Section 4.3.3, these devices produce greater heat when operating at higher fields.

However, this result clarifies that all three devices are capable in-line heaters, offering similar optical losses in their most optimized forms. Future improvements to the structures of these devices could be investigated and implemented to further increase their heating FOMs. While PIN and PN devices seem to be limited in terms of heating efficiency, their ability to be biased to further modulate their optical properties give them a unique advantage relative to single-doped devices.

# 6.0 Future Work

This work explored different devices for indirect electric switching of phase change materials for photonic integrated circuits. Two metallic heater structures were initially proposed to give a basis of comparison for the integrated waveguide heaters. As expected, these structures exhibited favorable optical properties, but were limited in heating efficiency. Three waveguide integrated heater structures were subsequently proposed: PIN diodes; single-doped structures; and PN diodes. Each of these integrated devices had various tradeoffs depending on their fabrication specifics, and these were investigated and summarized in Figure 5.7 for on-chip applications (V = 5 V). Each of these devices are viable heaters for phase change photonic devices, and their use depends purely on the designer's budget for fabrication complexity, acceptable optical loss, and available driving voltage. Each of these devices is amenable to application-specific optimization as platform technologies. In this chapter, follow up work on each of these three devices is proposed to pave the way for future work quantifying the feasible design space of these integrated waveguide devices.

## 6.1 PIN Diodes

### 6.1.1 Optimization of PIN Fabrication Techniques

As discussed in Section 4.4.2, the reliability of the fabricated PIN devices was underwhelming. Devices with supposedly identical geometries exhibited large cycle-to-cycle and

device-to-device variabilities, as shown in Figure 4.11. While the underlying reason for this variability is still unknown, it is clearly specific to the PIN devices: the single-doped devices fabricated on the same chip did not exhibit the same levels of variability. For the geometric effects of PIN device design to be further investigated, the fabrication process used to make these devices needs to be examined to ensure more consistent device performance. In addition, future optimizations such as the implementation of a tapered channel (similar to those used in the single-doped devices) should be considered.

### 6.1.2 3D Simulations of PIN Diodes

In addition to the improvement on the fabrication techniques used, expanding the existing device model to a fully 3D model is the logical next step. Expanding out in the third dimension would make other optimizations such as changing intrinsic region shape and effects of bending radii easier to model and take advantage of, albeit at the expense of additional computational complexity. In addition, this model would be able to fully quantify the effects of out-of-plane heat flux, similar to the 3D approximation presented in Section 3.0. This established 3D model could then be used to further optimize the pulsed performance of these devices prior to fabrication, allowing for immediate improvements in device performance when fabrication process consistency has been addressed.

## 6.2 Single-Doped Structures

### 6.2.1 High-Field Modeling of Single-Doped Structures

Initial modelling of the single-doped structures under high-field conditions showed a distinct deviation in both saturation effects, as well as the measured temperature under these conditions. A 3D temperature dependent semiconductor model was developed using COMSOL Multiphysics, similar to that described in Section 3.2. The channel for this device was rectangular, as opposed to the tapered channel used in the real measured devices (Figure 4.1c). As shown in Figure 6.1a, the simulated current for the higher-doped device was consistently overestimated, while the current for the lower-doped device was initially overestimated but was over saturated at higher currents. As expected from this, the temperature calculated for the higher-doped device was significantly overestimated, while the temperature for the lower-doped device was significantly underestimated.

This discrepancy in experimental measurements and simulated values should be resolved in future efforts. While the underlying mechanism responsible for heating in these devices under high-field conditions is still debatable (Section 4.3.3), the measurements themselves are due to material specific shifting in the Raman spectra, and as such are reflective of true temperature in the devices. To further investigate this question, fast IV characteristics of these devices (on the order of ~10 ns driving pulses) should be conducted, which would eliminate temperature effects in the devices. These temperature-independent IV curves should yield more insight into the onset of velocity saturation under these high-field conditions, enabling design of device operation

regimes. Further, this new information on additional heat generation due to velocity-saturation should be incorporated into computational models, resulting in more realistic predictive analysis.

Secondary experimental validation of device temperature combined with further theoretical investigation into this operation regime should be conducted. Once confirmed, the new operating regime should be implemented into the existing simulation frameworks, enabling further investigation into real device operation. Ideally, heaters for switching small patches of PCMs should leverage this secondary heating regime. Understanding how to design devices to utilize this regime with voltages available on chip (< 5 V) could yield a new generation of more efficient heaters.

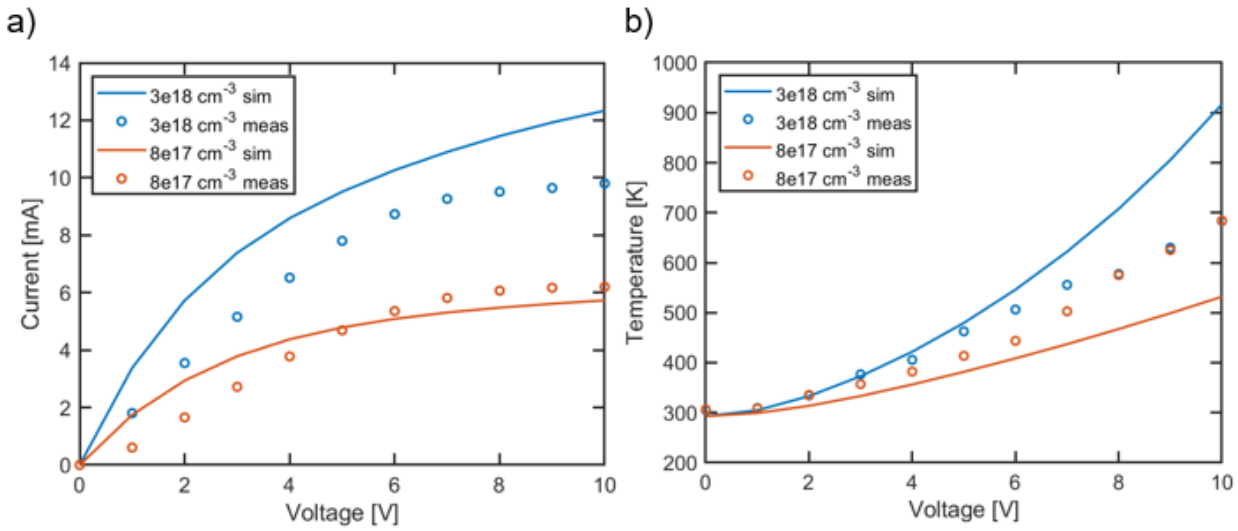


**Figure 6.1 – Initial modeling of single-doped structures compared with experimental characterization. Initial calculations show (a) overestimation of current and (b) underestimation of temperature of the established semicondcutor device model.**

## 6.3 PN Diodes

This study applied established models to a new photonics application. The simulated and experimental outcomes of this work revealed that the established model is limited and can be improved to better reflect real device operation. The scaling factor discussed in Section 5.1.4, while matching the measured data extremely well, is less than satisfactory overall. Further explorations in terms of symmetrical 2D models, full 3D models or a more complex mobility model should be added to further understand the devices.

In addition, while the overall comparison chart in Figure 5.7 does show a unique comparison of all devices, it can be made more in depth. A further mature single-doped model would help, but in addition all the simulations done for that figure were done at 5 V, which was not enough to melt the PCM. At higher applied voltages, the heating mechanisms may change and lead to different efficiencies, and it would be those that would be of further interest.

## 6.4 IR Scope for Fast Pulse Behavior of Integrated Waveguide Heaters

While Raman thermometry is an effective noninvasive measurement technique, it is inherently a long-timescale process. To measure device performance under actual ns-timescale operation speeds, a fundamentally different technique is required. As discussed previously, PCMs are effective in photonic switching applications due to the large change in their optical properties depending on the phase of the material. However, even prior to phase transformation, there are temperature-dependent factors influencing the reflective index of the PCM [215]. By initially

characterizing the temperature-dependent reflectivity of these devices, that relationship can be used to calculate the operating temperature profile over time of a PCM patch on top of an optical waveguide.

This process has been established and verified using COMSOL Multiphysics for measurements on a single-doped device similar to the “large device” pictured in Figure 4.8 using a 4.8 μs, 265 mW driving pulse [214]. As the operating range of the single-doped device was well below high-field conditions, a simple resistive heating model was adapted, using an electrical conductivity derived from the measured IV characteristics. The temperature calculated from the change in reflectivity of the PCM was in good agreement with the simulations, as shown in Figure 6.2b,d, showing that this technique can be valuable in nondestructively probing the fast heating performance of microheaters. Use of this technique will be invaluable to more detailed assessment of pulsed heating performances in the devices investigated here. While the Raman thermometry work presented in Section 4.0 is useful in proving that these devices can provide significant quantities of heat, their expected high-speed performances need to be verified.

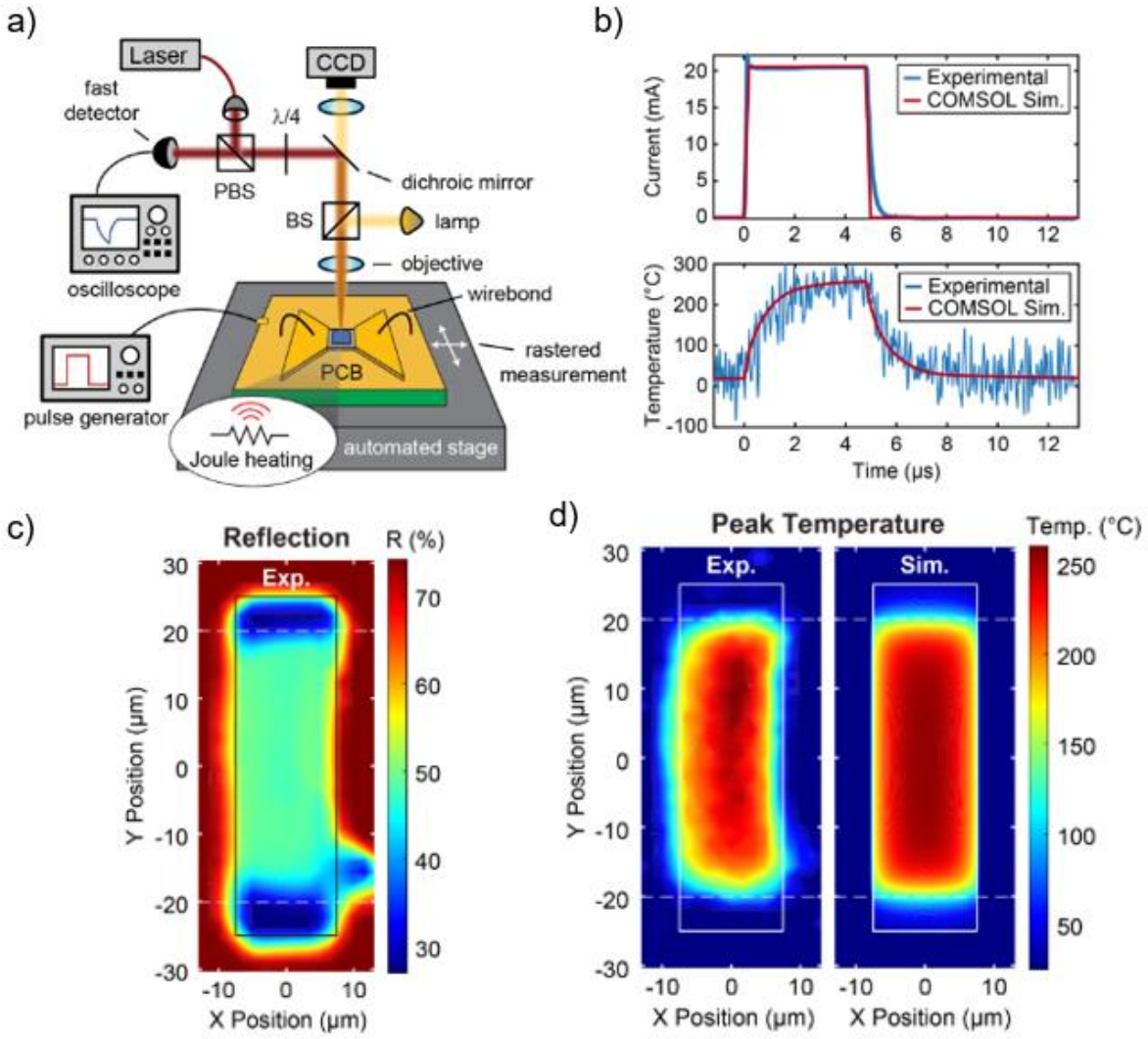


**Figure 6.2 - Experimental set up and initial characterization of optical probing of PCM operation temperatures. (a) Experimental schematic. (b) Experimentally measured and simulated results of driving current and peak temperature of the GST using a 4.8 μs 265 mW driving pulse. (c) Measured change in reflection at peak operating temperature. (d) Comparison of experimental vs. simulated peak tempearture. Reprinted from [214].**

# 7.0 Conclusion

Silicon photonic devices offer great potential for energy-efficient, high-speed, high-optical bandwidth switching. Photonic devices based on phase change materials offer a novel means to implement nonvolatility and an expanded range of effective operating points. While outstanding engineering issues must be addressed in design of the phase change materials themselves, this work offers a starting point in the characterization and optimization of the heater structures, and provides a framework for quickly designing heater-based photonic devices for novel candidate phase change materials. The three most basic types of integrated heaters that are readily available to be implemented using standard Si fabrication techniques were investigated. The effects of device geometry and doping level on both thermal and optical performance were further investigated for each device type. This work provides a first resource for future device design, including a set of forward calculations and experimental characterization that are useful in validation of new techniques and devices.

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