Josephson current in Hybrid Semiconductor-Superconductor One-Dimensional devices

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Bomin Zhang

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This dissertation was presented

by

Bomin Zhang

It was defended on

June 22, 2023

and approved by

Sergey Frolov, Associate Professor, Department of Physics and Astronomy

Michael Hatridge, Associate Professor, Department of Physics and Astronomy

Roger Mong, Associate Professor, Department of Physics and Astronomy

Hanna Salman, Associate Professor, Department of Physics and Astronomy

Benjamin Hunt, Professor, Department of Physics, Carnegie Mellon University

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Bomin Zhang, PhD

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Superconducting and semiconducting materials have been extensively studied as separate topics within the field of condensed matter, significantly contributing to the scientific and technological advancements of the 21st century. The hybrid systems combining these advancements have emerged as the primary focus in mesoscopic physics and quantum technology. While superconducting qubits based on these systems have demonstrated their superiority, topologically protected Majorana qubits hold considerable potential for future fault-tolerant quantum computing.

However, the realization of Majorana zero modes (MZM) requires the elegant balancing of various effects, including spin-orbit interaction, proximity-induced superconductivity, gate tuning, and Zeeman splitting, and it is crucial to have a profound understanding of these physics within microscopic devices. In this thesis, the primary focus is on the Josephson effect in hybrid nanowires junctions, using DC Josephson current as a tool to study spin-orbital interaction and orbital effect.

We first present our recent progress in Sn shell formation on InSb nanowires. Material analysis reveals a uniformly smooth shell half-covering the InSb nanowires and well-separated superconductor islands. Transport results indicate strong proximity-induced superconductivity. The enhanced proximity effect expands the parameter space into new regimes, suppressing disorder in the system and forming the basis of our studies in nanowire Josephson junctions.

Our studies of the Josephson effect proceed in two directions. On the one hand, we focus on fine-tuning transverse modes to achieve supercurrent transport through a single conduction channel. The orbital effect in the presence of an external field is analyzed by comparing the decay rate of supercurrent in few and multi-mode scenarios. On the other hand, we explore the skewed diffraction pattern of supercurrent induced by spin-orbit interaction,

demonstrating that it is a ϕ_0-junction with higher-order harmonics.

These three studies collectively illustrate our progress in reducing disorder in the system and exploring orbital and spin-orbit effects in nanowire junctions—crucial steps toward realizing MZM in hybrid systems.

In the final chapter, we study InSb nanowires coated with CdTe shells. Morphological studies reveal epitaxial growth of CdTe with a uniform thickness and a defect-free interface. This structure may inspire the design of future hybrid devices for realizing MZMs.

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Preface

Completing this thesis has been one of the most challenging endeavors of my life, yet it has also been a period of intense growth and rewarding discovery. As I reflect on the journey, it becomes clear to me that this achievement would not have been possible without the constant encouragement, expert guidance, and unwavering support of numerous individuals.

My deepest appreciation goes to my academic advisor, Prof. Sergey Frolov. Your invaluable counsel, patience, and enthusiasm are beyond compare. You enlightened my path into natural sciences, instilling in me the understanding that beneath every phenomenon lies a scientific law worth unravelling, never to be disregarded as merely a "violation of theory."

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To my parents: thank you for your unconditional love, faith, and sacrifice. Your constant

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Last but not least, I would like to extend my sincere thanks to my friends, whose supportive words and faith in my abilities helped me during the most challenging times. And my lovely cat Meow, you have given me the warmest company in the past two years

In retrospect, this thesis has been more than just a culmination of my academic work. It has been a journey that has taught me resilience, persistence, and the value of hard work.

The process has certainly not been smooth, and the product is not perfect. However, this thesis stands as a representation of my growth and learning, the relationships I have formed, and the challenges I have overcome. I hope that it will serve as a valuable contribution to the field and act as a stepping stone for future research.

Once again, thank you all for being a part of my academic journey.

1.0 Introduction

The Josephson effect is a remarkable phenomenon in the field of superconductivity [1, 2], which has garnered significant attention in recent years due to its potential applications in quantum information science and technology [3]. Notable applications include Superconducting Quantum Interference Devices (SQUIDs) [4, 5], superconducting qubits [6, 7], and voltage standards [8]. The current-phase relation (CPR) of Josephson junctions (JJs) serves as the fundamental basis for these applications [9].

On the other hand, semiconductors have long been the cornerstone of modern technology and are among the most versatile platforms for exploring and manipulating quantum states at the nanoscale [10, 11]. Key aspects rendering semiconductors suitable for quantum state manipulation include the ability to control their electrical conductivity by adjusting the concentration of charge carriers through doping or gating, thus enabling fine-tuning of electronic properties. This feature facilitates the creation of quantum wells, wires, and dots, which confine electrons in one or more dimensions. In semiconductors, the Zeeman effect, involving the splitting of energy levels in the presence of an external magnetic field, can be exploited to manipulate the spin states of charge carriers. Additionally, in semiconductors lacking inversion symmetry, the spin-orbit interaction couples the motion of charge carriers to their spin, leading to phenomena such as the Rashba [12] and Dresselhaus effects [13], which offer further avenues to manipulate charge carrier spin states [14].

Semiconductor nanowires not only inherit the advantages of semiconductors but also confine charge carrier transport to one dimension due to their widths being smaller than the Fermi wavelength. This confinement results in quantized energy levels and discrete quantum states, enhancing control over electronic properties owing to the high surface-to-volume ratio. Introducing superconducting electrodes to nanowires to create JJs can induce superconductivity in the nanowires via the proximity effect. This combination is predicted to fulfill the criteria for novel topological superconductivity and the Majorana bound states (MBS) can emerge at the ends of the semiconductor nanowire [15, 16]. MBS are characterized by their non-Abelian exchange statistics and robustness against local perturbations, making

them attractive candidates for fault-tolerant quantum computing [17, 18, 19].

Since the idea of building a Kitaev chain in solid state system was reported [20], numerous platforms have been proposed for realizing Majoranas [21, 22, 23], with claims of potential signatures of MBS [24, 25]. However, recent debates have arisen regarding whether the definitive 'smoking gun' of Majoranas has been found [26], as the coherence of MBS has not yet been established [27]. Disorder is the primary challenge in related research, as it can create additional sub-gap states [28], known as 'zero bias peaks', which were widely believed to be evidence of MBS [29, 30]. Disorder also results in decoherence of proximity-induced superconductivity and leads to the loss of protection and stability of MBS.

Minimizing disorder in superconductor-semiconductor heterostructures is crucial for identifying and studying MBS and benefits all related research mentioned previously. Efforts to mitigate the effects of disorder have included optimizing fabrication procedures [31], in-situ preparation and formation of interfaces, epitaxial growth, and more. The epitaxial growth of an aluminum (Al) shell on indium arsenide (InAs) nanowires marked a milestone in materials science [32], as it significantly reduced defects at the interface with the aid of state-of-the-art techniques. However, the notion that only epitaxial interfaces could host Majoranas has also limited subsequent studies due to strict material requirements; in other words, only Al-InAs/InSb systems meet these criteria. As the definitive evidence of MBS remains elusive, there is a growing demand for new platforms in the search for Majoranas.

This thesis comprises four main sections. Chapter 4 introduces our achievements in exploring new combinations of superconductor-semiconductor heterostructures. We investigated InSb nanowires half-covered by thin tin (Sn) shells and observed strong proximity-induced superconductivity [33]. The induced superconducting gap in the semiconductor nanowires can persist under significant external magnetic fields. The field-driven parity transition of charging energy in the island device indicates strong coherence of induced superconductivity. Intriguingly, material analysis revealed that the β-Sn grains in the shell, which are the origin of superconductivity, are not epitaxially grown on the InSb. This work demonstrate that epitaxial growth of superconducting leads is not a necessary precondition to study MBS in nanowire hybrid systems, significantly expanding the selection of superconductors for heterostructure devices and laying the foundation for the subsequent two

studies.

In Chapter 5, we present our efforts in studying the Josephson effect in the first electron mode achieved in Sn-InSb nanowire Josephson junction Quantum Point Contacts (QPCs). Previously, Josephson junctions made with InSb and ex-situ deposited NbTiN demonstrated that transport in multi-electron mode may suffer from disorder induced by the interference between orbital intermixing in the presence of an external field [34]. However, the behavior of Josephson current that transports through a single conduction channel remains unrevealed. Sn-InSb nanowires offer a promising platform with reduced defects. By fine-tuning the nanowire junction region, we demonstrated quantized conductance plateaus as evidence of quantum point contact and successfully located the gate voltage range where the first electron transverse mode is present. We studied the Zeeman and orbital effect in the first mode Josephson current.

In Chapter 6, we present evidence of the ϕ_0 junction [35]. The current-phase relation (CPR) is essential for all applications based on JJs; however, driving of the ground state phase in JJs remains elusive. By combining induced superconductivity, spin-orbit interaction, and Zeeman spin splitting in nanowires JJ, we characterized ϕ_0 junction by anomalous Josephson effect [36]. We show the non-zero phase offset in current-phase relation with high-order harmonics leads to a bias direction-dependent critical current. While previous studies have attempted to detect the phase shift associated with the ϕ_0 junction using SQUIDs [37]. This method relied on large magnetic fields and gate-tuning of nanowires, but leads to ambiougous interpratation as the path of supercurrent also changes with gate and the flux quantum is varying. In this work, we propose an alternative approach, utilizing supercurrent diffraction patterns to investigate the ϕ_0 junction state.

In Chapter 7, we explore the potential of combining II-VI and III-V materials to grow nanowires that exhibit effective surface passivation. Cadmium telluride (CdTe) is in-situ grown on indium antimonide (InSb) nanowires. A uniform thickness shell and lattice-matched interface are observed without an oxidation layer or defects disrupting the epitaxial relationship between the two materials. The electronic structure of the InSb-CdTe interface is studied using density functional theory. The transport data exhibit comparable mobility to bare InSb nanowires, indicating that no disorder is introduced into the nanowires. Such

physical layer confinement could lead to higher quality devices, and functioning as protection layer to prevent InSb from oxidation. The CdTe shell has the potential to function as an intuitive tunnel barrier between superconductor and semiconductor, allowing for the adjustment of coupling strength in the hybrid system by modifying the shell thickness.

2.0 Theory

In this chapter we briefly introduce the background and theory of superconductor-semiconductor hybrid nanowires Josephson junction.

2.1 Introduction

The concept of the Josephson junction (JJ) was proposed by Brian D. Josephson in 1962 [1, 2]. Josephson suggested that a thin insulator layer sandwiched between two superconductor leads could allow a zero voltage supercurrent to flow through it due to the coherent tunneling of superconducting electrons across the layer. This theory was further developed and is now well-known as the Josephson effect.

Josephson's prediction was based on the concept of a macroscopic wave function that describes the collective behavior of superconducting electrons in the electrodes. A more general understanding is that any two superconductors connected by a "weak link" exhibit the Josephson effect. The weak link can be an insulator, normal metal, constriction, semiconductor, or ferromagnetic material. In our case, all Josephson junctions studied consist of two superconductor leads and semiconductor nanowires.

In the following sections, we will begin with an introduction to the BCS theory of superconductivity and the proximity effect, as these are fundamental to understanding the Josephson effect. We will then discuss the basic properties of the Josephson junction and examine the behavior of the current-phase relation (CPR) in the JJ. We will demonstrate how the CPR is derived from the Hamiltonian of the Andreev bound state. Finally, since the weak link in our studies is made of semiconductor nanowires, we will discuss additional physics effects such as spin-orbit interaction (SOI) and Zeeman splitting, which must be included in the Hamiltonian. By considering all of these effects, we will provide a comprehensive picture of the physics involved in our studies.

2.2 Superconductivity and Proximity effect

2.2.1 BCS theory of Superconductivity

The BCS theory, developed by Bardeen, Cooper, and Schrieffer in 1957 [38], is a widely accepted microscopic theory that explains the phenomenon of superconductivity in metals and alloys. The theory is based on the concept of electron pairing, which occurs due to the attractive interaction between electrons and the lattice vibrations (phonons) in the crystal lattice of the material. These pairs are known as Cooper pairs, and they are held together by the exchange of virtual phonons.

When two electrons form a Cooper pair, they pair up in a way that minimizes the total energy of the system. This leads to the electrons forming a spin-singlet state $< \Psi_\uparrow(\mathbf{k})\Psi_\downarrow(\mathbf{k}) >$, in which their spins are paired up in opposite directions, resulting in a total spin of zero. This pairing of electrons leads to a reduction in the energy required for an electron to move through the lattice, and this reduction in energy leads to the phenomenon of superconductivity. Superconducting materials exhibit zero electrical resistance and can conduct electricity without any energy loss due to heating or dissipation. The BCS Hamiltonian, which describes the interaction between electrons and phonons in a superconductor, is given by:

$$H_{BCS} = \sum_{\mathbf{k},\sigma} \epsilon_{\mathbf{k}} c^\dagger_{\mathbf{k},\sigma} c_{\mathbf{k},\sigma} + \sum_{\mathbf{k}} \Delta(\mathbf{k}) c^\dagger_{\mathbf{k},\uparrow} c^\dagger_{-\mathbf{k},\downarrow} + h.c. \tag{2.1}$$

where $\epsilon_{\mathbf{k}} = \frac{(\hbar k)^2}{2m^*} - E_F$ is the kinetic energy of an electron with momentum $\mathbf{k}$, σ is the electron spin, $c^\dagger_{\mathbf{k},\sigma}$ creates an electron with momentum $\mathbf{k}$ and spin σ, $\Delta(\mathbf{k})$ is the energy gap, which represents the energy required to break apart a Cooper pair (Also known as superconducting pairing potential). The second term in the Hamiltonian describes the formation of Cooper pairs, where electrons with opposite spin and momentum form a bound state due to their attractive interaction mediated by lattice vibrations (phonons). The third term represents the energy required to break apart a Cooper pair.

The BCS Hamiltonian is a mean-field approximation, which neglects the effects of fluctuations in the electron pairing. More sophisticated Hamiltonians, such as the Eliashberg [39, 40]

and Hubbard models [41], include these fluctuations and can provide a more accurate description of superconductivity in certain materials and the temperature dependence of superconductivity.

If we diagonalize the BCS Hamiltonian and write it in Bogoliubov-de Gennes (BdG) form, it looks like:

$$H_{BCS} = \sum C_{\mathbf{k}}^{\dagger} \mathcal{H}_{BdG} C_{\mathbf{k}} \tag{2.2}$$

Where $C_{\mathbf{k}}^{\dagger} = (c_{\mathbf{k},\uparrow}^{\dagger}, c_{-\mathbf{k},\downarrow})$ and:

$$\mathcal{H}_{BdG} = \begin{pmatrix} \epsilon_{\mathbf{k}} & \Delta(\mathbf{k}) \\ \Delta^*(\mathbf{k}) & -\epsilon_{\mathbf{k}} \end{pmatrix} \tag{2.3}$$

The Bogoliubov-de Gennes (BdG) Hamiltonian is a generalized version of the Schrödinger equation, which takes into account the fact that electrons in a superconductor are paired and behave as a coherent entity, so the excitation can be counted as linear combinations of electrons and holes:

$$\mathcal{H}_{BdG} \begin{pmatrix} \psi_e(\mathbf{r}) \\ \psi_h(\mathbf{r}) \end{pmatrix} = E \begin{pmatrix} \psi_e(\mathbf{r}) \\ \psi_h(\mathbf{r}) \end{pmatrix} \tag{2.4}$$

Where $\psi_e(\mathbf{r})$ and $\psi_h(\mathbf{r})$ is the wave function of spin and holes at $\mathbf{r}$. The probability density of finding the a quasi-particle in an electron-like or hole-like state at position $\mathbf{r}$ is proportional to the square of the wave function.

It is easy to combine Eqn. 2.3 and Eqn. 2.4 and get eigenenergies:

$$E = \pm\sqrt{\epsilon_{\mathbf{k}}^2 + |\Delta(\mathbf{k})|^2} \tag{2.5}$$

and the density of states derived by taking $\rho(E) \equiv \frac{d\epsilon}{dE}$. The density of state $\rho(E) = 0$ if $E < \Delta$ and $\rho(E) = \frac{E}{\sqrt{E^2-\Delta^2}}$ if $E > \Delta$. This is demonstrated in Fig. 2.1(a). In most of the cases, the momentum of Cooper pairs is effectively zero. This is because Cooper pairs in a superconductor form a condensate, which is described by a macroscopic wave function that is uniform in space and has a well-defined phase. This wave function is called the order parameter and is proportional to the average value of the Cooper pair wave function:

$$\Psi(\mathbf{r}) = |\Psi_0(\mathbf{r})|e^{i\varphi(\mathbf{r})} \tag{2.6}$$

where r is the position in the material, $|\Psi_0(\mathbf{r})|$ is the magnitude of the order parameter and $\varphi(\mathbf{r})$ is its phase. For conventional BCS superconductor, the simple relationship: $|\Psi_0(\mathbf{r})| = \Delta$ is valid at temperature T close to 0.

However, it is important to note that this zero-momentum behavior is an idealized description of a superconductor, and in reality there are always perturbations and imperfections that can affect the behavior of Cooper pairs. In the presence of impurities, defects, external magnetic field [42, 2], or extra spin torque like spin-orbital interaction, the momentum distribution of Cooper pairs can become more complex, with non-zero momentum components that depend on the specifics of the system.

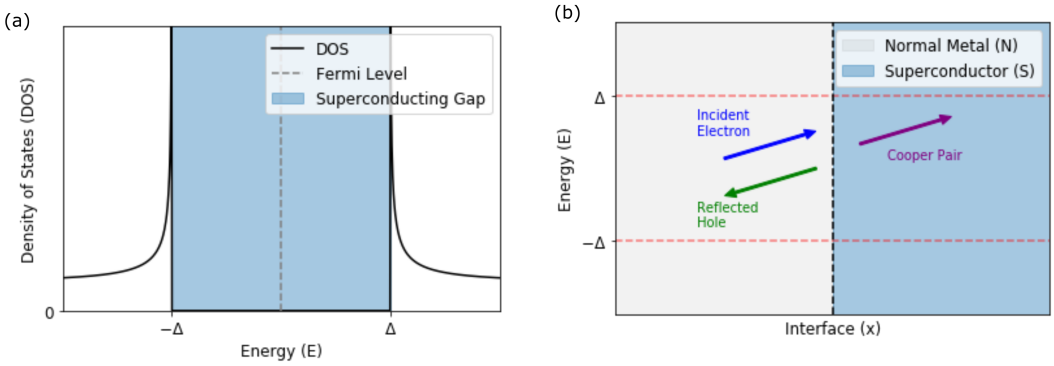

Figure 2.1: (a) Superconducting density of state with the energy gap Δ. Transport results in experimental of proximity induce gap in semiconductor can be found in Fig. 4.1. (b) Schematic of Andreev reflection for an incident electron with energy $E < \Delta$ at the interface of a normal metal(grey) and a superconductor(blue).

2.2.2 Proximity effect and Andreev reflection

In bulk superconductor, the $|\Psi_0(\mathbf{r})|$ in Eqn.2.6 is a constant value. When a superconductor is brought into close proximity with a normal material or another superconductor, the superconductivity of the first material can "induce" or "infect" the wave function of

the second material. As a result, the normal material can exhibit superconducting behavior as well. This is called proximity effect and is the fundamental of Josephson effect in his paper [1, 2].

The proximity effect is a fundamental phenomenon observed at the interface between a superconducting (S) material and a normal (N) metallic material. It arises due to the wave-like nature of electrons in a solid and the interplay of electronic states between the superconductor and the normal metal in the vicinity of their interface. When a superconductor and a normal material are in close proximity, the electrons in the normal material become entangled with the Cooper pairs in the superconductor. This entanglement can result in the formation of new quasiparticles with a modified energy spectrum, which includes energy states that are superconducting. As a result, the normal material can become superconducting as well.

Andreev bound states [43, 44], on the other hand, are localized energy states at the interface between a normal metal and a superconductor. They arise due to Andreev reflection and depicted in Fig. 2.1 (b). When an normal state electron with energy $E < \Delta$ incident on the normal metal side of the interface is reflected back as a hole with opposite momentum and charge, due to no quasiparticle states available in the superconducting state. This process results formation of a Cooper pair in the superconductor. When the upcoming electron has energy $E > \Delta$, it tunnel through the interface and remain as a normal state electron.

One can say Andreev bound states arise as a result of the same electron-hole pairing mechanism responsible for the proximity effect, and their presence affects the local density of states in both the normal metal and the superconductor.

In our case, Josephson junction is made with a weak link between two superconductor leads, so the phenomenon that occurs is the Multiple Andreev reflection (MAR) (depicted in Fig. 2.2). When an external voltage is applied across the junction, Cooper pairs from the superconductors tunnel through the barrier. In the presence of a voltage larger than the superconducting energy gap, electrons can undergo multiple Andreev reflections, leading to a series of correlated electron-hole pairs traveling back and forth between the superconductors.

During each MAR event, the electron (or hole) gains (or loses) energy equal to eV_{SD}, where V_{SD} is the voltage across the junction. When the energy gained by the electron

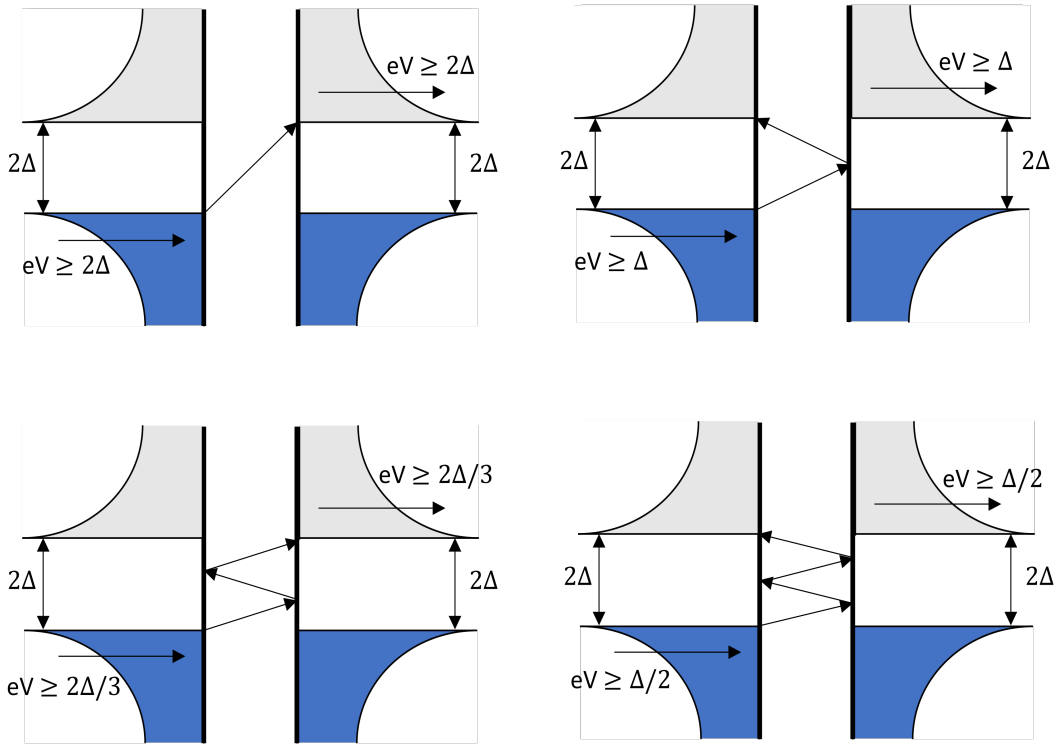

Figure 2.2: Schematic of Multiple Andreev Reflection in an S-N-S junction. Energy need to overcome the energy gap is $E \geq 2\Delta/n$ where n is the number of reflection.

(or hole) is sufficient to overcome the superconducting energy gap, it can enter the other superconductor as a quasiparticle. This process can contribute to an increase in the sub-gap current across the junction, as well as a modification of the density of states near the interface. MAR plays an important role in determining the transport properties of NS structures and known as evidence of transparent interface. Experiment results of MAR can be found at Fig. 4.2 (a).

2.3 Josephson effet

2.3.1 Basic properties of Josephson junction

Josephson started from the novel BCS theory, and gave the current phase relation of a Josephson junction should be:

$$I_{sw} = I_c sin(\phi). \tag{2.7}$$

Here ϕ is the difference in the phase of the Ginzburg-Landau wave funciton [45] between the two superconductors. Critical current I_c is the maximum supercurrent that the junction can support and it is determined by the energy. Switching current I_{sw} is the current where the transition between zero resistance and finite resistance happens. This is also called the direct-current (DC) Josephson effect.

If a voltage difference V is applied across the junction, the time evolution of phase difference ϕ is expressed as:

$$d(\phi)/dt = 2eV/\hbar. \tag{2.8}$$

This is called the alternating-current Josephson effect. Transport of each Cooper pair across the junction will result a energy change that equals to $2eV$.

The energy associated with the supercurrent flowing through the junction is Josephson energy, It can be derived from the 2.7 and 2.8 by having:

$$\begin{aligned} E &= \int I_s V dt = \int (\hbar/2e) d(\phi) \\ &= const. - E_j cos(\phi) \end{aligned} \tag{2.9}$$

Where $E_j \equiv \hbar I_c/2e$. The energy E reaches its minimum when the ϕ=0, which means there is no phase difference between two superconductors and it is equivalent to have a single piece of bulk superconductor.

2.3.2 Current-Phase Relation in Josephson junction

In a Josephson junction, the current-phase relation (CPR) describes the relationship between the supercurrent flowing through the junction and the phase difference between the superconducting wavefunctions on either side of the junction. The properties of the current-phase relation in a Josephson junction depend on several factors, including the junction geometry, the material properties of the superconductors and semiconductors, and the external environment. Here are some of the key properties [9]:

(1) A change of phase in either of the superconductor electrodes does not result in a change in the physical state and not affect the Josephson current flowing through the junction. So the CPR is a periodic function about 2π:

$$I_{sw}(\phi) = I_{sw}(\phi + 2\pi) \tag{2.10}$$

(2) If time-reversal symmetry is preserved, reversing the direction of the Josephson current will change the sign of the phase difference. This means that the current-phase relation (CPR) is an odd function:

$$-I_{sw}(\phi) = I_{sw}(-\phi) \tag{2.11}$$

(3) When the junction is in the ground state, the phase difference across the junction ϕ_0 is 0 or the integer multiple of 2π. There is no Josephson current flowing thorough the junction when it is in the ground state:

$$I_{sw}(\phi_0) = 0 \tag{2.12}$$

where $\phi_0 = 2\pi n$ and $n = 0, \pm1, \pm2, ...$

(4) When combining properties (1) and (2), there is also no Josephson current when phase difference is integer mutiple of pi ($\phi = \pi n$):

$$I_{sw}(\pi n) = 0, n = 0, \pm1, \pm2, ... \tag{2.13}$$

The form that Josephson first proposed(Eqn. 2.7) follows all the rules below, while a more general expression based on Foruier series is proposed later in [46]:

$$I_{sw}(\phi) = \sum_{i=1}^{\infty} (I_n sin(\phi n) + J_n cos(\phi n)). \tag{2.14}$$

Here I_n and J_n are coefficients of harmonic functions. In S-I-S junctions, I_n and J_n equals to 0 for n$\geq$2. Theoretically, ideal transparent junction should have all higher order harmonics survived, and there are several evidence of second harmonic CPR in varity of Josephson junction [47, 48, 49, 50].

When time reversal symmetry is preserved, J_n always equal to 0. There are several ways to break time-reversal symmetry in a Josephson junction, and they lead to a variety of interesting phenomena. We will later discuss the experimental evidence of ϕ_0-junction in Chp. 6.

2.3.3 Theory approach: From Andreev bound states to Josephson effect

To derive the expression for the Josephson current from the Andreev bound states, one can solve the BdG equation (Eqn.2.3). This approach was first employed by Kulik in 1969[51]. In his work, Kulik focused on the behavior of superconductor-normal metal-superconductor (SNS) junctions, where the normal metal (N) region is much shorter than the superconducting coherence length, but wider than the Fermi wavelength λ_F. He exmained the energy spectrum of the junction and how proximity effect influences the energy levels of the system. Beennakker and van Houten later discussed this in a Quantum Point Contact (QPC), where junction width $w_d << \lambda_F$ by adding an $\delta - function$ interface barrier [52], to include the quantized conductance in the normal state [53, 54]. To follow their interpretation, we start by assuming two superconductors are identical and the normal metal has no T_c and a length of L ($L << \xi$), so the magnitude of the order parameter (cooper pair potential) is given by:

$$\Delta_{\mathbf{r}} = \begin{cases} \Delta_0 e^{i\phi 1} & \text{if x < -L/2} \\ 0 & \text{if -L/2 < x < L/2} \\ \Delta_0 e^{i\phi 2} & \text{if x > L/2} \end{cases} \tag{2.15}$$

When energy of transport electron $E > \Delta$, the solution is a continuous spectrum because it is in normal state. When $E < \Delta$, there are discrete energy levels with eigenenergies:

$$E_n^{\pm} = \frac{v}{L}(2\pi n + \varphi \mp \phi) \tag{2.16}$$

Here positive symbol (+) describes an electron-like quasiparticle, negative (-) describes hole like. $\varphi(E) = arccos(E/\Delta_0)$, ϕ is the phase difference, v is the velocity of the excitation inside the normal metal and has a characteristic values $\Delta_0/v_0 \sim \xi_0^{-1}$. So we can transform it to:

$$\frac{E_n^{\pm} L}{\Delta \xi} = 2\pi n + arccos(E/\Delta) \mp \phi \tag{2.17}$$

and get the two lowest eigenvalues of energy $E^{\pm} = \pm\Delta cos(\frac{\phi}{2})$. When considering transmission eigenvalues T, we have the eigenvalue of ABS energy:

$$E^{ABS} = \pm\Delta\sqrt{1 - Tsin^2(\phi/2)}. \tag{2.18}$$

Taking Eqn. 2.18 into the Eqn. 2.9 gives the Josephson current transport through Andreev bound states in the junction:

$$I(\phi) = \frac{2e}{\hbar}\frac{dE}{d\phi} = \frac{e\Delta}{2\hbar}\frac{Tsin(\phi)}{\sqrt{1 - Tsin^2(\phi/2)}} \tag{2.19}$$

Note this expression only valid at zero temperature and can be used for approximation when finite temperature much smaller than the critical temperature. The transmission rate T is also used in the general Landauer formula, where conductance is:

$$G = \frac{2e^2}{h}\sum_{n=1} T. \tag{2.20}$$

When the junction length L is larger than l_{mfp} (l_{mfp} is the mean free path in the weak-link), transmission rate $T << 1$ and it is mainly diffusive transport in the junction. Eqn. 2.19 reduces to the expression of Josephson junction in Eqn. 2.7. Behave like a sinusoidal shape function (see Fig. 2.3 (b)).

In the opposite criteria, if the weak link demonstrate a ballistic transport with quantized conductance, ($L << l_{mfp}$), one has the clean limit with $T = 1$. Higher order harmonics is contributed and it turns to be the Eqn. 2.14. Behave like a non-sinusoidal shape function (see Fig. 2.3 (b)).

This is related to the experiment discussed in Chapter. 5, where we constructed QPC in nanowires Josephson junctions.

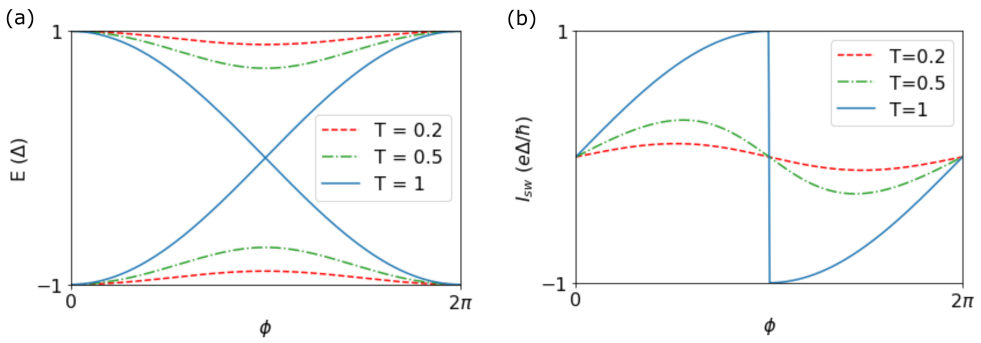

Figure 2.3: (a)ABS energy spectrum calculated with different Transmission rate T. (b) Corresponding Josephson current by taking $I_{sw} = \frac{2e}{h}\frac{dE_{abs}}{d\phi}$.

2.3.4 Topological non-trivial case in Josephson junction

If we consider a simple Josephson junction involving topological superconductors with a pair Majorana bound states (MBS) at each interface. When an electron tunnels across the junction, it can do so by splitting into two Majorana fermions, with one Majorana fermion remaining localized at each end of the junction.The non-trivial value of the topological invariant results in a fermion parity switch as a result of the change in the sign of the hopping t across the junction: $t \to -t$.

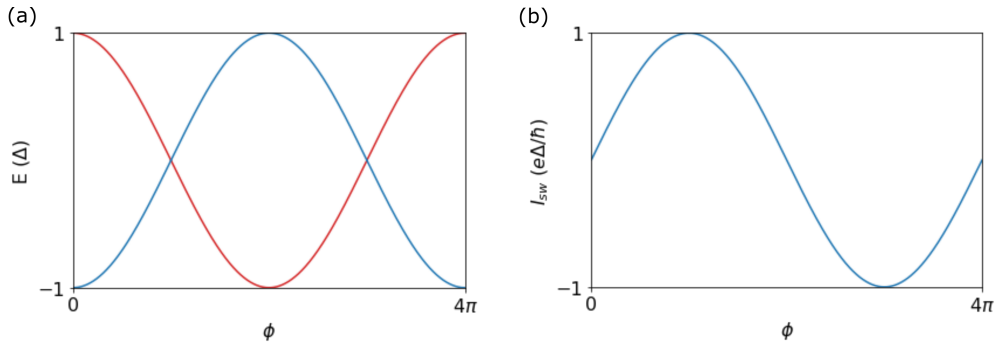

Figure 2.4: (a)ABS energy spectrum calculated with different Transmission rate T. (b) Corresponding Josephson current by taking derivative about the phase difference ϕ.

In this case, we can replot Fig. 2.3 in the phase range from 0 to 4π. Note that Majorana leads to perfect Andreev reflection at the interfaces so the transmission rate $T \equiv 1$. The energy spectrum change its sign at π and 3π. As a result, the energy spectrum and the corresponding Josephson current become function with a period of 4π.

Experimental attempts to detect the fermion parity switch in Josephson junctions are based on the AC Josephson effect. Driving the junction with a high-frequency microwave gives rise to steps like region in the I-V curve of the device. This is called Shapiro step. The steps occurs at voltage bias

$$V_{bias} = nf\Phi_0 \tag{2.21}$$

where n is integer number, f is the frequency of the microwave, $\Phi_0 = 2e/h$ is the superconducting flux quantum. The switch in fermion parity causes the period of the phase difference across the junction to become twice the flux quantum, leading to the absence of Shapiro steps corresponding to odd integer values of n.

2.4 Semiconductor Nanowires

2.4.1 Hamiltonian of a semiconductor band-structure

In this section I will briefly follow the related content in the Ref. [10]. To obtain the band structure Hamiltonian of a semiconductor, we want to solve the Schrödinger equation for non-interacting electrons in a periodic lattice potential. Consider the time-independent Schrödinger equation for an electron in a periodic lattice potential:

$$\hat{H}\psi(\mathbf{r}) = [-\frac{\hbar^2}{2m}\nabla^2 + V(\mathbf{r})]\psi(\mathbf{r}) = E\psi(\mathbf{r}) \tag{2.22}$$

where $\hat{H}$ is the Hamiltonian operator, and E is the energy eigenvalue. $\psi(\mathbf{r})$ is the electron wavefunction, $\hbar$ is the reduced Planck constant, m is the electron mass, ∇^2 is the Laplacian operator, and $V(\mathbf{r})$ is the periodic lattice potential, which satisfies:

$$V(\mathbf{r} + \mathbf{R}) = V(\mathbf{r}) \tag{2.23}$$

where $\mathbf{R}$ is a lattice vector. According to Bloch's theorem, the eigenfunctions of the Schrödinger equation in a periodic potential can be written as:

$$\psi_{n\mathbf{k}}(\mathbf{r}) = e^{i\mathbf{k}\cdot\mathbf{r}} u_{n\mathbf{k}}(\mathbf{r}) \tag{2.24}$$

where n is the band index, $\mathbf{k}$ is the wavevector, and $u_{n\mathbf{k}}(\mathbf{r})$ is a periodic function with the same periodicity as the lattice. Substituting this into the Schrödinger equation one gets:

$$\big\{\big[\frac{\mathbf{p}^2}{2m_e} + V(\mathbf{r})\big] + \big[\frac{\hbar}{m_e}\mathbf{k}\cdot\mathbf{p} + \frac{\hbar^2 k^2}{2m_e}\big]\big\} u_{n\mathbf{k}}(\mathbf{r}) = E_{n\mathbf{k}}(\mathbf{r}) \tag{2.25}$$

Here, $\mathbf{p} = -i\hbar\Delta$ is the momentum operator, m_e is the mass of free electron.

To solve this equation, we introduce a method that is called $\mathbf{k}\cdot\mathbf{p}$ perturbation theory. The main idea behind $\mathbf{k}\cdot\mathbf{p}$ theory is to treat the actual crystal potential as a perturbation of a simpler potential. The energy gap is between the lowest minimum of the conduction band and the maxima of the valence band, both are the symmetry points in the Brillouin zone and where the energy extrema occur. Hence, one can assume that the equation is solved for the special case $\mathbf{k} = 0$ and find the corresponding eigen-functions $u_{n0}(\mathbf{r}) \equiv |n\rangle$ and eigenenergies E_n.

The next step is to express the actual crystal potential as a perturbation of the simplified case E_n. This perturbation is then expanded in terms of the wavevector $\mathbf{k}$ and its corresponding energy bands:

$$\begin{aligned} E_n(\mathbf{k}) &= E_n + \frac{\hbar^2 k^2}{2m_e} + \frac{\hbar^2}{m_e^2} \sum_{m,m\neg n} \frac{|\mathbf{k}\cdot\mathbf{p}_{mn}|^2}{E_m - E_n} \\ &= E_n + \frac{\hbar^2 k^2}{2}\big(\frac{1}{m_e} + \frac{2}{m_e^2} \sum_{m\neg n} \frac{|\langle u_{m0}|\hat{\mathbf{k}}\cdot\mathbf{p}|u_{n0}\rangle|^2}{E_m - E_n}\big) \end{aligned} \tag{2.26}$$

Start from special case $\mathbf{k} = 0$, the energy dispersion remains parabolic like the dispersion of free energy. To describe the curvature of the parabola, one needs to use a parameter that is related to the material, conduction band effective mass m_{eff} where:

$$\frac{1}{m_{eff}} = \frac{1}{m_e} + \frac{2}{m_e^2} \frac{|\langle u_{c0}|\hat{\mathbf{k}}\cdot\mathbf{p}|u_{v0}\rangle|^2}{E_c - E_v} \tag{2.27}$$

Here $E_c - E_v = E_g$ is the energy of band gap. In Eqn. 2.26, the largest contributions to the last term arise from the valence band, because it is the closet energy band that is full-filled

with electron. So we simplify the last term by and the eigenenergies of conduction band can be approximated with:

$$E_c(\mathbf{k}) \approx E_c + \frac{\hbar^2 k^2}{2m_{eff}} \tag{2.28}$$

With the potential, the Hamiltonian writes:

$$H(\mathbf{k}) = \frac{\hbar^2 k^2}{2m_{eff}} + V(\mathbf{k}) \tag{2.29}$$

Note that the effective mass in the semiconductor is correlated with the energy of band gap. The main material I used is Indium Antimonide (InSb), it has a small effective mass and narrow bandgap. Our nanowires has width smaller than the Fermi wavelength ($d < \lambda_F$), confining the wacefunction into one dimensional system.

For a more accurate description of the band structure, one can use more advanced methods like the tight-binding approximation 6.12 and the first-principles calculations based on density functional theory (DFT) [55]. These methods provide a better representation of the periodic potential and the interactions between electrons and the lattice, leading to more accurate band structures and energy eigenvalues.

2.4.2 Zeeman energy

The Zeeman effect refers to the splitting of energy levels in an atom or solid due to the interaction between the magnetic field and the magnetic dipole moment μ of the electrons. In a semiconductor, this effect can influence the band structure and the properties of charge carriers.

The magnetic moment μ is described by the electron spin, the spin operator is defined as:

$$\boldsymbol{S} = \frac{1}{2}\boldsymbol{\sigma} \tag{2.30}$$

where the $\boldsymbol{\sigma} = (\sigma_x, \sigma_y, \sigma_z)$ have:

$$\sigma_x = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \qquad \sigma_x = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix} \qquad \sigma_x = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix} \tag{2.31}$$

The magnetic moment of the electron then writes as:

$$\boldsymbol{\mu} = -\frac{1}{2} g \mu_B \boldsymbol{\sigma} \tag{2.32}$$

Here, $\mu_B = |e|\hbar/2m_e$ =57.88 $\mu eV/T$ is the Bohr's magneton. g describes how rapidly the external field affect the motion of electron and is related to structure of material, it equals to 2 for free electron. In a homogeneous magnetic field, the Zeeman hamiltonian is:

$$H_{Zeeman} = -\boldsymbol{\mu} \cdot \boldsymbol{B} = \frac{1}{2} g \mu_B \boldsymbol{\sigma} \boldsymbol{B} \tag{2.33}$$

2.4.3 Spin-orbit interaction

The spin-orbit interaction (SOI) is a relativistic quantum mechanical effect that arises from the interaction between the electron's spin angular momentum and its orbital motion. When the electron move in an electric field with velocity $\mathbf{v}$, it suffers a effective magnetic field in its rest frame:

$$\boldsymbol{B'} = -\frac{1}{c^2} \boldsymbol{v} \times \boldsymbol{E} \tag{2.34}$$

This effective field interact with the magnetic momentum of electron via the Zeeman interaction, results a spin-orbit energy writes as:

$$\begin{aligned} H_{SO} &= -\frac{g\mu_B}{2} \frac{1}{c^2} (\boldsymbol{v} \times \boldsymbol{E}) \boldsymbol{S} \\ &= \frac{g\hbar}{4c^2 m_e^2} (\nabla V(\boldsymbol{r}) \times \boldsymbol{p}) \boldsymbol{S} \end{aligned} \tag{2.35}$$

Here we assume the electric field $\boldsymbol{E}$ is the result of the gradients of electrostatic potential V.

The intrinsic SOI in atoms and molecule is induced by the effective nuclear charge experienced by the electrons and its strength is related to the mass (atomic number) of the element. Rashba [56] and Dresselhaus SOI [13], on the other hand, are in low-dimensional semiconductor system and arise from inversion asymmetry. They are not directly related to the mass of the elements, but more relevant to the following discussion in this thesis.

The Dresselhaus effect originates from bulk inversion asymmetry in the crystal lattice, which is inherent to certain materials like zinc-blende semiconductors (ie., GaAs, InAs,

and InSb) or wurtzite semiconductor (ie., ZnO, ZnS, and CdS). In the context of zinc-blende semiconductors and with the confinement in the $\hat{z}$ direction, the Dresselhaus spin-orbit interaction of two-dimensional electron gas (2DEG) can be described by the following Hamiltonian:

$$H_D = \beta(\sigma_y p_y - \sigma_x p_x) \tag{2.36}$$

where β is the Dresselhaus spin-orbit coupling constant, which depends on the specific material and its band structure. k_x and k_y are the components of the electron's wavevector in the crystal direction of [100] and [010].

On the other hand, the Rashba effects originates from lack of structure inversion symmetry. This lack of inversion symmetry can result from an external electric field with gate voltage, or the presence of interfaces between different materials in a heterostructure. The electric field can be controlled by the gate voltage and perturbs spin of transport electron, makes it important in spintronics and quantum computing applications, as it can be used to manipulate electron spins.

The Rashba spin-orbit interaction can be described by the following Hamiltonian:

$$H_R = \alpha_R(p_x\sigma_y - p_y\sigma_x) \tag{2.37}$$

here α_R is the Rashba spin-orbit coupling constant, which depends on the specific material and the strength of the electric field or structural inversion asymmetry.

2.4.4 Hamiltonian of semiconductor nanowires Josephson junction

Both Hamiltonian describe the coupling between the electron's spin and its momentum in the crystal lattice. When writing Hamiltonian for our nanowires Josephson junction, the Dresselhaus spin-orbit interaction is neglected because it is not driven by the external magnetic or electric field. As a conclusion for this section, the Hamiltonian that is used in this thesis for nanowires Josephson junction is:

$$H = \left(\frac{\mathbf{p}^2}{2m_{eff}} - \mu\right) + \alpha_R(p_x\sigma_y - p_y\sigma_x) + \frac{1}{2}g\mu_B\boldsymbol{\sigma}\boldsymbol{B} + \Delta \tag{2.38}$$

Here μ is the chemical potential, which is controlled by the local electrostatic gate. Δ is the superconducting pairing potential. This equation is modified to 6.2 for the simulation based on the tight-binding model.

3.0 Experimental methods

In this chapter, we introduce the devices fabrication and measurements methods that have been used in our experiments, as well as the nanowires growth methods. In the nanowires growth section I will only focus on InSb nanowires growth. Sn-InSb nanowires growth will be discussed in the Chapter 4. CdTe-InSb nanowires growth will be discussed in the Chapter 7. In the fabrication section I will discuss nano-fabrication techniques involved in making the super-semiconductor hybrid devices based on InSb, Sn-InSb, CdTe-InSb and 2D quantum well. The measurement section includes measurement setup, quantum measurements based on DC and AC.

3.1 Nanowire growth

As a Ph.D student, I worked with four types of nanowires: InAs, bare InSb, InSb with Sn shell, and InSb with CdTe shell. I also assisted in the etching process for a 2D quantum well project. The InAs nanowires were grown at the Néel/CNRS Institute in Grenoble, France. The InSb nanowires were grown at the Eindhoven University of Technology. The wires were then transported to the University of California, Santa Barbara for Al or Sn superconducting shell deposition. The CdTe-InSb nanowires were grown at the Eindhoven University of Technology.

3.1.1 InSb nanowires

Indium antimonide (InSb) nanowires are widely studied as a promising candidate for achieving topological superconductivity. InSb has a small effective mass (of $0.015m_e$), allowing electrons to move significantly faster within the material. Bulk InSb has a small bandgap of $0.17meV$ at room temperature, making it easy to pinch the channel off by lowering the Fermi level to the valence band or fully saturate the wires with a small range of

gate voltage [57, 58]. Mobility measured from InSb nanowires with a diameter of approximately $100nm$ can be as high as $40000cm^2/Vs$ [59, 60], resulting in an average mean free path of approximately $200 - 300\ nm$, which is well-suited for quantum transport devices. The g-factor is large ($\approx$ 30 - 50).

All these properties make it an ideal platform for studying mesoscopic physics in quantum transport. When made into devices to study Josephson effect and topological superconductivity, InSb nanowires have exhibited strong Rashba spin-orbit interaction (spin-orbit length is 200nm, corresponding to SOI strength $\alpha = 200\text{nm}\cdot\text{meV}$) [61], which is fundamental for spin manipulation and trajectory control, and is necessary for studying the topology of materials. Another advantage of InSb is that it quickly forms a uniform and inactive oxide outer layer once exposed to air, preventing further degradation of the nanowire. Because InSb nanowires have been extensively studied, methods of removing the oxide layer and making transparent contacts with various metals and superconductors have been well-developed [24, 62, 63, 27].

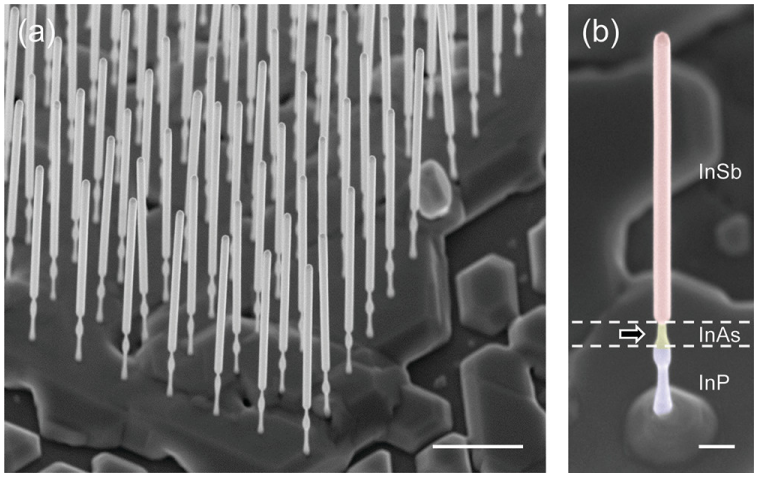

Figure 3.1: (a) low magnification image of nanowire array on the substrate. Scale bar corresponding to 1μm. (b) high magnification image of single nanowires with false color to indicates the different stacks of nanowires. Scale bar correspond to 200 nm. Figure is adapted from [64].

The growth of InSb nanowires utilizes a technique known as metal-organic vapor phase epitaxy (MOVPE), which is a chemical vapor deposition method based on the vapor-liquid-solid (VLS) mechanism [57, 64]. In contrast to the molecular-beam epitaxy (MBE) method

used for thin film growth by physical deposition [33], MOVPE relies on chemical reactions. A gold (Au) droplet with a radius of 20-50 nm is necessary as a catalyst for nucleation to initiate the growth. We used two methods to grow InSb nanowires: with or without an Indium Phosphate (InP) stem.

Figure 3.1(b) shows a representative scanning electron microscope (SEM) image of InSb nanowires grown with InP stem. Prior to growth, the sample is annealed to form a gold indium (Au-In) alloy between the gold catalyst and InP substrate, followed by the growth of InP for nucleation. An InAs stack is used as a buffer layer between the InP stem and InSb nanowires to reduce the lattice mismatch. However, the InAs region is easily broken, limiting the length of InSb nanowires in growth and resulting in a high yield of nanowires falling onto the substrate before wire transfer. Short wires are difficult to pick up, and falling wires stick to the substrate due to Van der Waals force, making them non-transferable. Remaining As atoms in the growth chamber can mix into the InSb structure, resulting in defects in the nanowires and disorder in transport measurement. To avoid introducing disorder from the mixing of source materials, a method for growing stemless InSb nanowires without an InP stem has been developed.

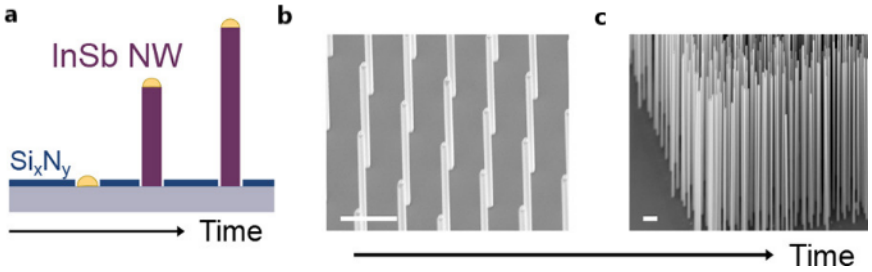

Figure 3.2: (a) Cartoon of stemless nanowires growth with Si_xN_y mask. (b)SEM image of nanowires array on the sample chip after 1hour growth. (c) SEM image of nanowires array on the sample chip after 5 hours growth. Nanowires with length over 5 μm is achieved. Scale bar is 1μm for both (b) and (c) panels are adapted from [60].

In Fig.3.2, we present a method for growing stemless nanowires. A selective-area mask is used to prevent direct layer growth on the InSb (111)B substrate. The entire process of growing stemless InSb nanowires is depicted in Fig.3.2 (a). Firstly, the substrate is cleaned

and covered with a uniform Si_xN_y layer with a thickness of 20 nm. Nano-openings are then defined using electron beam lithography (EBL) and formed by wet-etching Si_xN_y to expose the substrate. As the electron beam resist is not damaged by the wet-etching, it is used for positioning gold dots. A thin gold film of 15 nm is deposited in the sputtering chamber. After lift-off, only gold dots deposited in the nano-openings are left on the sample chips and will function as catalysts for growth. The stemless growth of InSb nanowires has high chemical purity and less disorder from material intermixing. This method achieves longer nanowires (Fig. 3.2 (c)), making it preferred for designing and fabricating Majorana devices.

3.2 Device fabrication

The projects in our lab involve the fabrication of various types of mesoscopic devices. I always recall my supervisor Sergey Frolov telling me during my first year in the lab, upon learning about my hobby of cooking, that fabrication is similar to cooking. Although the fabrication methods may vary depending on the device, there is a basic procedure to be followed: (1) design the pattern using PC software. (2) Draw the pattern using the lithography technique. (3) Fill the pattern with the superconductor deposition metal. (4) Remove all unwanted parts.

For our nanowire projects, there is an additional step, namely, transferring the nanowires under the microscope with the micro-manipulator. In this section, I will outline the complete fabrication steps involved in a typical Superconductor-Semiconductor-Superconductor Josephson Junction device. I will begin with an introduction to the lithography technique we employ in the project in Section 3.2.1. Next, I will discuss the preparation of the substrate chip we use for sample fabrication in Sections 3.2.2 and 3.2.3. Following this, I will elaborate on the main procedure and discuss all the details involved in our fabrication, from wire transfer in Section 3.2.4 to cleaning and deposition in Section 3.2.7.

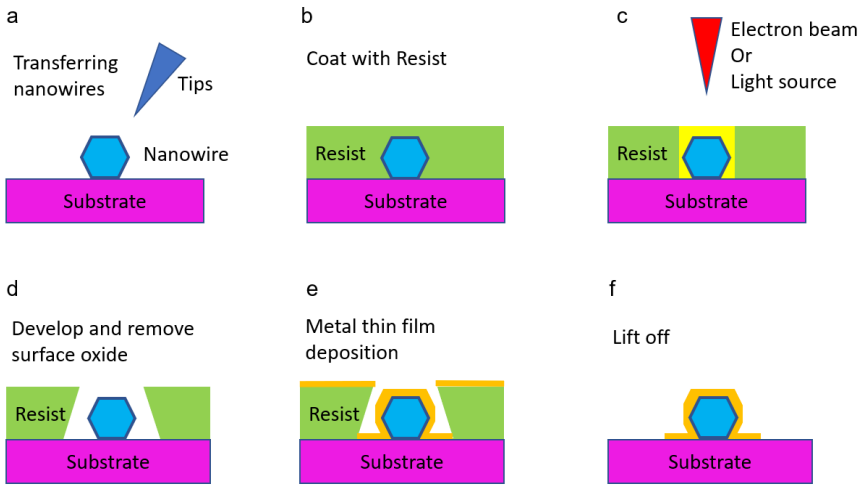

Figure 3.3: (a) Transfer nanowires onto the substrate with tungsten tips. (b) Coat the whole substrate with lithography resist. (c) Use E-Beam or light source to exposure sample based on design. (d) Develop the sample to removed exposed region. Followed by cleaning the surface of nanowires with physical or chemical etching. (e) Metal or superconductor deposition to have a uniform film over the chip. (f) Lift off unexposed resist. Film on the unexposed region will be removed at the same time.

3.2.1 Optical and Electron Beam Lithography

In industry, nanofabrication only uses optical lithography with masks for stability and cost control, resulting in fixed patterns. In research, however, flexibility is a priority requirement, and accuracy and speed can be sacrificed. Both optical and electron beam lithography equipment available in our cleanroom are patterned based on layout designs, allowing us to customize specific geometries for each device.

The basic steps of lithography can be found in Fig. 3.3(b) to (d) and always begin with coating the sample with optical or e-beam resist. Positive resists like PMMA or S1805 are most commonly used, and the chemical bonds connecting large compounds will break in the region exposed by e-beam or light source. The relatively smaller molecules released from the bonding can be dissolved in the development solution, resulting in the removal of the resist

at the exposed region. In the deposition chamber, a uniform film will cover everywhere, but the unexposed region will be protected by the resist, allowing the metal film in that region to be taken away in the lift-off step. Only in the region where the resist is exposed to the e-beam or light source, the sample is exposed to the deposition flow, and the metal film will stick to the sample and stay after lift-off.

In our nanofabrication process, we utilize mask-less aligner (MLA) for optical lithography. However, its accuracy is limited to the micrometer level due to alignment being done with a microscope. Despite this limitation, MLA is advantageous for quickly exposing large patterns such as wire-bonding pads, large markers, and waveguides. For instance, to pattern a matrix of global back-gate chips on a 4-inch wafer would take about an hour with MLA, whereas it would take 40 hours with electron beam lithography (EBL).

On the other hand, EBL has superior accuracy in writing and alignment and is widely used in nanofabrication research. The EBL equipment in our cleanroom is an upgraded scanning electron-beam microscopy (SEM) system produced by Raith. It accelerates the electron beam with a variable high voltage source ranging from 5kV to 30kV and directs it towards the sample at the focused area. The sample is mounted on a stage that can move in the XYZ directions. The pre-designed pattern is divided into small patterns by the writing field, and the stage is moved from one writing field to another. In the same writing field, the trajectory of the e-beam is bent by magnetic fields for patterning. Higher voltage provides better accuracy but also poses a risk of damaging the nanowires and dielectric. For our projects, 10kV is suitable for all our needs.

3.2.2 Global backgate chips

InSb semiconductor nanowires are highly tunable due to their small energy gap between valence and conduction bands. However, the regions of the nanowires that are covered by metal or superconductor films are dominated by these materials, making them difficult to control with gates. Therefore, our experiments focus on controlling the chemical potential in the uncovered parts of the nanowires. However, transferring nanowires onto a pre-defined gate pattern under a microscope is challenging and time-consuming. Additionally, controlling

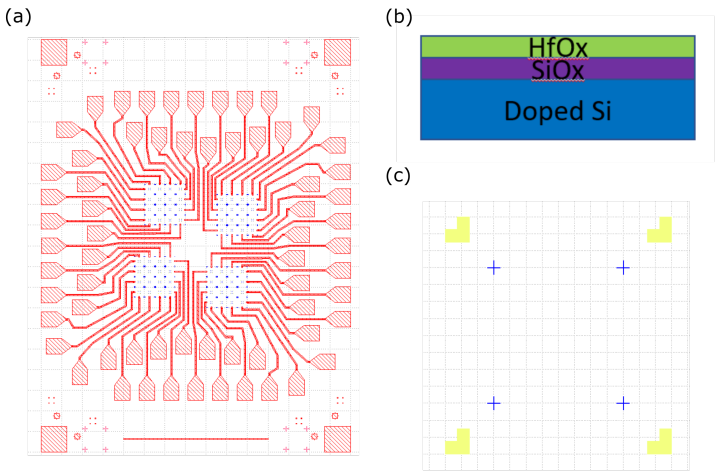

Figure 3.4: (a) Layout design of a global backgate chip. (b) Illustration of the backgate chip crosscut. (c) Zoom in of nanowires positioning area to show local bit markers and crossing markers.

local gates requires designing a connection between the gates and bonding pads during fabrication and using a pin on the measurement setup for voltage input.

When measuring simple two-terminal devices for characterizing nanowires or testing fabrication methods, a straightforward approach is to use global backgate chips. A full layout design of backgate chips can be found in [reference]. These chips are made with highly doped silicon, which has a resistance of 0.001-0.005 Ω per cm^2, and therefore remains conducting at base temperatures close to 0 K. On one side, the silicon is oxidized to form a SiOx layer with a thickness of 285 nm as a dielectric. When the silicon side is connected to a high voltage source, the entire substrate becomes a global gate, creating a uniform electric field along the out-of-plane direction. The chemical potential in all nanowires is tuned, but only the one connected to the measurement setup is studied. The SiOx dielectric layer protects nanowire devices from shorting to the gate and can withstand up to a 30 V voltage difference.

To improve the dielectric layer's performance, we added an extra layer of HfOx onto the SiOx using atomic layer deposition (ALD) as shown in Figure 3.4(b). However, since

the surface of SiOx becomes rough when exposed to air and may be contaminated with impurities, it is essential to clean the wafer with a chemical etching method known as Piranha etching [65]. The wafer is immersed in Piranha solution for 9 minutes, washed with pure water, and then blow-dried with a compressed nitrogen gun before being directly transferred into the ALD chamber for HfOx deposition. The recipe for HfOx deposition is a plasma at 150 °C.

The backgate chip pattern consists of two parts: markers and bonding pads as shown in Figure 3.4(a). The bonding pads and large square markers located at each corner of the chip are made using a maskless lithography system. The four small square markers at each corner with a side length of 1 μm are used for electron beam pattern generator (EBPG) auto-alignment. The design is duplicated into a matrix with horizontal and vertical spacing both equal to 6 mm to cover the entire 4-inch wafer. Before optical writing, the wafer is coated with LOR 5B and then S1805. The resist is spread over the wafer in the spinner with 4000 (LOR) and 5000 (S1805) rpm, and baked for 9 minutes at 195 °C for LOR and 5 minutes at 115 °C for S1805. Since the laser light source decays over time, the exposure dose should be selected with an annual dose test. This exposure does not require any alignment. After writing, the chips are developed by sinking them in the developer 351 (1:4 diluted with distilled water) for 75s, distilled water for 30s, AZ 400K (1:4 diluted with distilled water) for 30s, and distilled water for another 30s. Then, they are blow-dried with compressed nitrogen gas. There may be residues due to developer and resist, which are cleaned using a plasma asher that gently mills everything. Finally, the wafer is transferred to the Plassys evaporator chamber for deposition of 5 nm Ti and 50 nm Au. The lift-off process is performed by immersing the wafer in Remover PG overnight and then ultrasonicating it for 20 minutes.

After the fabrication of the large square markers, the whole wafer is diced into small pieces to pattern smaller markers using electron beam lithography (EBL). Each piece contains 9 chips arranged in a 3 by 3 configuration. To prevent the chips from being damaged during dicing and cutting, a thick resist layer is applied to cover the sample. PMMA 950 A4 resist is used, and the sample is spun at 1000 rpm for 1 minute, resulting in a resist layer that is about 500 nm to 1 μm thick. This resist layer can be easily removed by soaking the sample in Acetone after cutting. The same protective layer can also prevent contamination and keep

the chips clean during long-term storage, and therefore should be considered before placing them in a desiccator.

The small local markers and bit markers shown in Fig.3.4(c) are created using EBL. The wafer is coated with PMMA 950 A4 by spinning it at 5000 rpm for 1 minute, then baked at 175°C for 15 minutes. The EBL setup includes a 10 kV accelerating voltage, a 10 μm aperture, and a 10 mm working distance. Alignment is achieved by using the e-beam to align the large square markers on the design and on the chips. After EBL writing, the pattern is developed using MIBK/IPA in a 1:3 ratio for 60 seconds, then IPA for 60 seconds, and finally, blow dried with N2 gas. The chip is then cleaned with plasma asher and 5 nm Ti and 15 nm Au are deposited using the plassys evaporator. Finally, the lift-off process is carried out by soaking the chip in acetone overnight and using ultrasonic treatment for 20 minutes.

3.2.3 Local gate chips

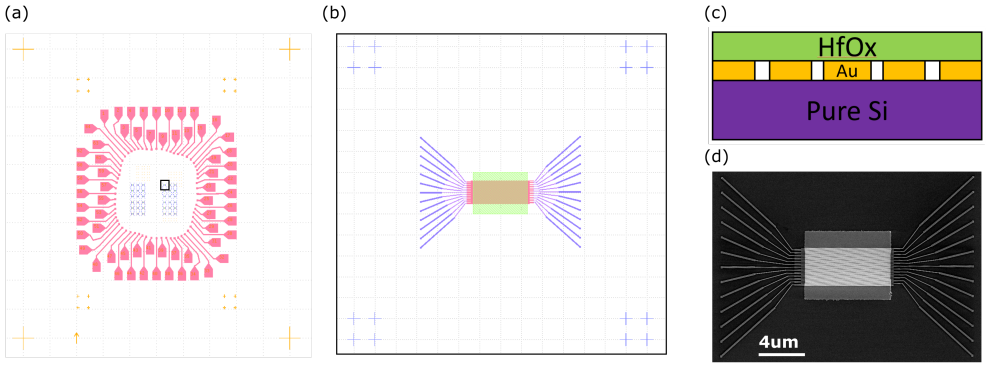

Figure 3.5: (a) Layout design of a local gate chip. (b) Zoom in of the region enclosed by the square box in (a) to show the local gates and markers. (c) Illustration of the local gate chip crosscut. (d) SEM image of the local gates area.

Unlike the global back gate chip, the local gate chip uses EBL-defined metal static electrode gates to fine-tune the nanowires. As a result, the substrate of the local gate chip is pure Si. Due to the sophisticated nature of the gates pattern, even an experienced researcher may experience low yield. Therefore, the writing sequence is swapped. The gates pattern is

created in the cleanroom of CMU using a 100 kV EBL system called EBPG. Different types of gate designs are available to fulfill the requirements of different projects. One common design involves local gates with mixed widths of 80 and 200 nm separated by a distance of 40 nm.

I once attempted to draw the same pattern using a 30 kV EBL, PMMA 950 A1 thin resist, and cold development technique at the University of Pittsburgh, but failed due to a lack of stability while moving the stage between writing fields.

After gate patterning, the wafer is transported back to our cleanroom for metal evaporation of 1.5 nm Ti and 6 nm Au. Good gates should be well isolated from each other to avoid shorting to neighbors. If the pattern looks good under SEM, the wafer is coated with photoresist and exposed with MLA for bonding pads. The optical writing and deposition steps are the same as in 3.2.2. After creating the pads, another photo lithography with MLA is used to define the dielectric layer on the local gates (green region in Fig.3.5 (b) and (c)). The dielectric is 10nm of ALD deposited HfOx. Fig. 3.5(d) shows the SEM image of the local gates ready for nanowire transfer.

3.2.4 Transferring of Nanowires

Our device fabrication process requires the transferring of nanowires from their original substrate to the gate chips. This step is crucial and is carried out using the nanowire manipulation and transferring technique described in [66]. We use Tungsten tips with a radius of 350 nm, which are made by American Probe Inc. These tips are attached to a micro-manipulator arm that is connected to an optical microscope. A video demonstrating the transferring step can be found at [67]. The procedure is as follows:

(1) Focus on the tip and nanowires separately under the microscope to ensure that they are at the same location in the XY plane but with different heights.

(2) Lower the tip to touch the nanowires and then continue to lower it to break the nanowires from their stems. It is important to avoid the tip touching the substrate of the nanowire chips.

(3) Raise the tip and the nanowire should stick to it due to van der Waals force.

(4) Move the stage to position the gate chips under the microscope and find the region where the nanowires should be transferred onto.

(5) Lower the tip and allow the nanowires to make physical contact with the chips. The nanowires will stick to the chips because a larger contact area gives a larger van der Waals force.

There are some tips for transferring nanowires:

(1) Fully clean the gate chips between transfers. Organic contaminants and dirt can prevent the wires from sticking to the chip, and can also affect the functionality of the gates if there is something between the wires and the dielectric.

(2) When picking wires, touch the center of the nanowire. Touching the top or bottom of the wire could cause it to bend or rotate around the tip when breaking the stem.

(3) Sometimes the nanowires may not stick to the bottom of the tips, but rather to the side or top. If the tip is lowered to the gate chip surface but the nanowire does not fall onto the chip, try rotating the tip on the arm. The wire should easily come off when it touches the substrate.

(4) When working with gate chips, the most desired orientation for the nanowires is to have them perpendicular to the gates. Because the z-field in the dilution fridge is fixed, it is also important to have all the nanowires aligned in the same direction. However, the orientation of the nanowires is hard to change once they are stuck to the tips. Therefore, check the wire direction under the microscope, rotate the chip stage to align them before letting the wires and the chips make physical contact. If the wire is still not well aligned, gently pushing it with the tips can help.

(5) Once the manipulator arm is set up, only move the stage if a shift in the XY plane is needed. The manipulator is not stable and will keep vibrating when being controlled.

Sn-InSb wires have a low yield of having good shadow junctions. Therefore, multiple wires on the same gate area should be considered to ensure that there are enough wires for fabrication. If the SEM image shows that the yield is still low, another round of wire transferring should be considered.

3.2.5 Device design

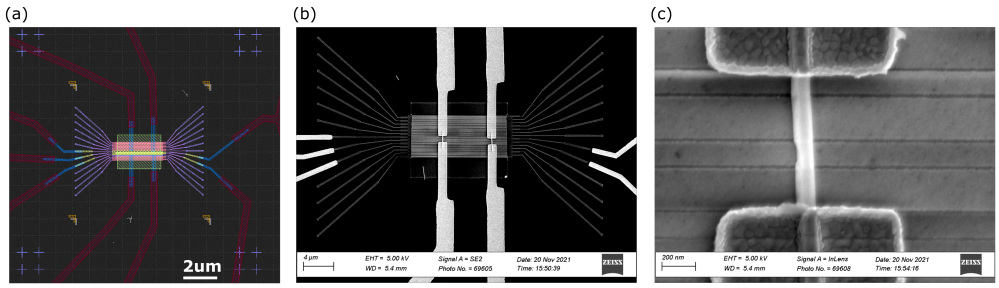

Figure 3.6: (a) Layout design of Joesphson junction devices after importing nanowires. (b) SEM image of the same device after fabrication. (c) Zoom in to show the relative position of shadow junction and bottom local gates.

The layout design of a Josephson junction in a nanowire is a complex process that involves several steps. The first step is to image the nanowires and determine their actual position on the chip, which requires taking an optical or e-beam microscope image of the wires and local gates. This image can then be imported into a layout design program called Klayout, and the markers in the image need to be aligned with the design before the layout can be finalized (see Figure 3.6(a)).

Good layout designs should take into account the accuracy of lithography, possible over- or under-exposure during writing, and misalignment due to equipment setup. In our lab, for instance, my lithography always results in an over-exposure of about 20 to 30 nm at each boundary, likely due to proximity effects and over-developing time. While optimizing the procedure may lead to other issues, leaving a space between each pattern that is larger than 100 nm can help avoid shorts between neighboring pins. Another common issue is that the exposed pattern always shifts in the same direction, even when the alignment is perfect. This is caused by the offset from the stage and the controlling program, and can be especially annoying when fabricating side local gates. However, since the offset is consistent for each exposure, adding a shift towards the opposite direction in the design can help solve this problem.

The process of writing with the EBL program involves cutting the pattern into small

polygon shapes based on the predefined writing field. However, there may be gaps between writing fields due to mechanical issues when moving the stage. To overcome this problem, a good solution is to use double exposure. When designing a large pattern, duplicate the layer and shrink the second layer slightly so that the program cuts it differently and exposes it in a different way. However, double exposure can easily lead to overexposure because the dose is doubled too. Therefore, for smaller patterns where the dose and width are critical, it is recommended to keep the pattern within a single writing field and avoid using the double exposure technique.

3.2.6 Coating, Lithography, and develop in actual fabrication

After imaging the position of the nanowires on the gate chip with SEM, the chip undergoes a cleaning process using Acetone and IPA. The chip is soaked and shaken in the solution for 2 minutes and then blown dry. The coating and writing recipe are the same as the ones discussed in 3.2.2 for EBL lithography.

To align the pattern on the design and the actual sample chip, a step called 3-point alignment is required. This involves screening the crossing markers on the sample chip and matching them to the same markers in the design, allowing EBL to write based on the coordinates of the layout design. When writing finer patterns such as local side gates, a procedure called manually align local markers should be considered. One needs to label the markers that will be used for local alignment. The crossing markers for local alignment have a width of 50 nm and a size of 1 μm by 1 μm. In Fig. 3.6 (a), they are located at each corner of the image, and four local markers define a write field.

After exposure, the sample chip undergoes development by sinking it in MIBK/IPA (1:3) for 1 minute. The development is then stopped by sinking it in IPA solution only for another 1 minute. To ensure that the development solution spreads evenly, the chip is snapped with a carbon tip tweezer and shaken in the solution. The chip is then blown dry with compressed nitrogen gas and cleaned with Oxygen plasma with a power of 50 W for 15 Sec at a pressure of 500 mTorr to remove resist residues.

3.2.7 Surface cleaning, etching, and Contact deposition on nanowires

The key factor for quantum point contacts discussed in 5 is the transparency between metal/superconductor contacts and semiconductor nanowires. A transparent interface can reduce system disorder and eliminate unwanted trivial states like subgap Andreev states. This induces a strong proximity effect, which is fundamental to robust topological superconductivity and Josephson effect. Transparent contacts are desired in my studies to avoid ambiguous interpretation that may arise from strong disorder in the system. Thus, surface cleaning of semiconductor nanowires and contact deposition is always a core issue in the fabrication process. My project consists of fabricating superconductor contacts on bare InSb nanowires and normal contacts on CdTe-InSb/Sn-InSb nanowires. The surface cleaning procedure will be discussed separately.

As previously mentioned in 3.1.1, when exposed to air, InSb nanowires form a native oxide layer all over their surface, mainly composed of In_2O_3[68]. Therefore, surface cleaning of bare InSb nanowires involves two tasks: removing the oxide layer and protecting the nanowires from further oxidation during the transition from the hood to the deposition chamber. Several methods have been tested in our lab[69], among which sulfur passivation is chosen as the standard treatment in the fabrication process. This recipe was first developed for omic contacts on InAs [31] and has been well demonstrated on InSb [70]. Our optimized sulfur passivation recipe involves preparing a freshly saturated ammonium sulfide solution ($(NH_4)_2S_x$) by adding 0.29 g of sulfur powder into 3 mL of commercial ammonium sulfide solution and stirring for 30 minutes. Note that a shield is necessary as the $(NH_4)_2S_x$ will be decomposed by photocatalysis. The solution is then diluted with distilled water at a ratio of 1:200 by adding 1 mL of freshly prepared ammonium sulfide to 200 mL of distilled water. The developed chip is then immersed in the diluted solution, the container covered with aluminum foil, and water-bathed for 30 minutes at 60 °C. The oxygen in the non-conducting oxide layer is replaced by sulfur, resulting in a conducting sulfide layer that prevents further oxidation for a short period if the chip is exposed to air. The chip can then be cleaned with flushing distilled water and dried with compressed nitrogen gas. Once thoroughly dried, it can be directly transferred to the load chamber of an evaporation or

sputtering machine for deposition. A weak argon plasma milling (power = 15 watt, flow of Ar = 5 sccm, flow of N_2 = 45 sccm) for 10 seconds is used to remove sulfur residues from the surface of the nanowires.

On the other hand, CdTe-InSb and Sn-InSb nanowires are each coated with a protective outer shell - CdTe for the former and AlOx for the latter - to prevent oxidation. Removal of these outer shells will expose a fresh InSb/Sn surface that can easily form ohmic contact with the deposited metal leads. Following development, the chip is transferred to the plassys load lock chamber for physical etching via Argon ion milling. The milling process is set to 30 seconds per round for CdTe-InSb and 40 seconds per round for Sn-InSb, with a voltage of 250 V and a current of 15 mA to avoid overheating, which can cause the e-beam resist to melt and damage the pattern. Between milling steps, the Argon gas is pumped out until the chamber pressure reaches 1E-7 mTorr, a process that takes approximately 30 minutes.

When loading the chip, the vacuum of the load lock chamber is broken and must be pumped down, which can take some time. To maintain the deposition chamber at low pressure, it is good practice to pump the load lock for 30 minutes to an hour to reach a pressure of approximately 1E-7 mTorr. This helps to minimize the introduction of particles from the air into the deposition chamber when the shutter between chambers is open, resulting in less disorder at the interface during deposition and physical milling.

Inside the plassys chamber, e-beam evaporation of Au and Ti is used to create metal contacts onto the nanowires, which have a radius ranging from 50 nm to 70 nm. To ensure full coverage of the nanowires with the metal contacts while avoiding deposition of a film thicker than the resist that can cause lift-off issues (the PMMA 950 resist is approximately 300-400 nm), a common procedure is to deposit 10 nm of Ti at a rate of 0.01 nm per second, followed by 140 nm of Au at a rate of 0.05 nm per second.

After depositing the metal, the chip is placed in a beaker of Acetone for lift off and taken to the development hood. To prevent the Acetone from drying out, the beaker should be covered with aluminum foil. Typically, the chip is left in the Acetone overnight to ensure that the resist has fully dissolved, filling the space between the metal film and the chip with Acetone, making it easy to remove unwanted metal. To improve the lift off yield, it's recommended to heat the Acetone to $60°C$ for 30 minutes. The film is then blown with

a 1mL micro-pipette. A good practice is to inspect the sample under a microscope while leaving the chip in a Petri dish of acetone. If the acetone on the chip is dry, the film still on the chip will not be lifted off. Therefore, it's essential to make sure that all patterns are well-defined after lift off. The next step is to move the chip to a beaker of IPA to wash away the Acetone, followed by blowing it dry with a compressed Nitrogen gun.

After lift-off, the device is examined with SEM. Fig.3.6 (b) and (c) display a typical two-terminal Sn-InSb nanowires device on a bottom local gate chip. Each terminal of the device and the local gates under the shadow junction are connected to a bonding pad for measurement. SEM images are used to identify lift-off problems that are not visible under an optical microscope, such as shorts between gates or possible dielectric breaks. Next, the resistance of the devices is measured at room temperature using a probe station under an optical microscope. Thick Tungsten probes with a radius of 7μm are linked to a sensitive resistance reader called "Beeper," and they are in direct contact with the bonding pad to establish a connection. The beeper generates a voltage bias V_{bias} = 10 mV, which is considered as a safe value for the nanowires device.

3.2.8 Wet etching of Tin on nanowires and two-dimensional quantum well

In addition to nanowires, we have recently developed a new method for creating planar Josephson junctions using nanowire shadowing, which we call the "Smash Junction" [71]. To fabricate the "Smash Junction" chip as an actual device, one must first remove the AlO_x capping and superconductor layer while avoiding damage to the resist and semiconductors. The wet etching process for aluminum is well-established in both research and industry, but the etching method for tin on the quantum wire/well is still being explored.

We have proposed a method that involves etching with two highly selective metal-specific reagents. Once development is complete, the chip is submerged in CD26 (diluted 1:20 with distilled water) for 2 minutes. CD26 is a weak acid developer that attacks both Al and AlO_x but results in a smooth etching. When diluted with water, it causes almost negligible damage to the resist and quantum wire/well [72], making it widely used in our fabrication process. The chip is then immersed in a highly diluted HCl solution (HCl:H20 = 1:1000)

for 10 to 30 seconds to remove the Sn. However, we have found that the etching rate of Sn in the diluted HCl solution can be difficult to control and may result in large undercuts of several μm under the resist. To avoid potential undercuts, we carefully examine the results under an optical microscope after etching every 5 seconds.

3.3 Measurement Setup

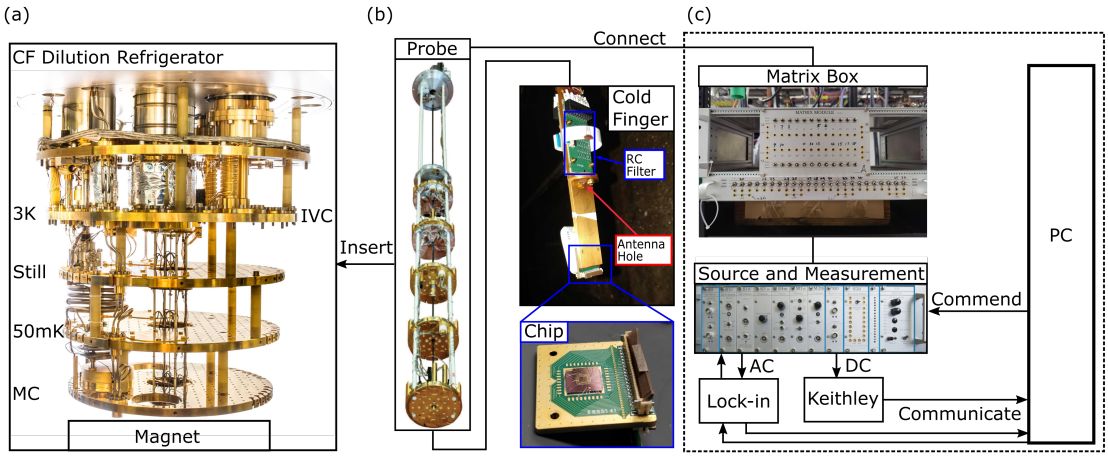

Figure 3.7: A schematic of measurement setup. (a) Inside look of Leiden CF dilution refrigerator. Several plates that are commonly recorded by the program for the cooling performance are labeled. IVC chamber is connected to the 3K plate and have the magnet mount onto it. Mixing chamber is the coldest plate and its temperature is called base temperature. (b) Inside look of a top loading probe. When the probe is inserted in the fridge, several stages of plates are expanded to make thermal contacts with plates of the fridge. Device and RC filter is mounted on the cold finger, cold finger is mounted at the bottom of the probe. (c) Measurement setup. IVVI is controlled by PC, it produces current or voltage source that goes to the matrix box. The matrix is connected to the device by wires that go through the probe.

Cooling down the sample chip to cryogenic temperatures and keeping it at base temperature is a crucial step in quantum transport measurement. Finite temperatures induce

thermal excitation and subgap states that soften the superconducting gap, weakening the superconductivity in the nanowires and leading to ambiguous results. Additionally, the magnet used in the experiment is made with a superconductor coil to withstand large currents of about 100 A. Consequently, both the magnet and the devices are mounted in an equipment called a dilution refrigerator (or fridge) for extreme low temperature measurements.

Figure 3.7(a) depicts an inside look at a top-loading CF series dilution refrigerator that is used in our experiments. The fridge is covered by several chambers to create isolated regions. From the outside to the inside, the first region is called the OVC. The OVC is mounted on the top plate, and the outer part is exposed to the air. To prevent thermal exchange between the inside regions and the air, the OVC is fully vacuumed. The second region is called the IVC, which is mounted on the 3 K plate, and the whole shell is cooled down to about 3 to 4 K. To accelerate the cooling down process, there is usually a small volume of Helium-4 (He^4) left in the IVC, resulting in about 1mbar pressure at room temperature. The lowest plate is called the mixing chamber (MC), and its temperature is called the base temperature, making it the coldest part of the fridge (usually 40 to 50mK with inserted probes, although optimized fridges can achieve 20 mK).

There are two cooling systems used to produce low temperatures in the fridge. One system is called the pulse tube, which uses only He^4 as the refrigerant in the circulation to bring heat out and can only cool the whole system down to 3 K. When measuring the device, another system called the condensing system will have a He^3/He^4 mixture in the circulation to produce cooling power. Several lines in between these stages, labeled in Fig. 3.7(a), are used to circulate the mixture. Both cooling methods use circulated Helium to absorb heat from the system, and the circulation is driven by multi stages of pumps and turbos. In other words, the fridge converts mechanical energy into cooling power in an isolated system to produce extreme low temperatures.

The magnet for external field measurement is mounted on the bottom of the IVC, so it is cooled to the same temperature as the IVC. Because the magnet is made with a Niobium coil and its optimal functioning temperature is below 4.2 K, it is important to maintain the low temperature of the IVC. When cooling down a device, the probe, shown in Fig. 3.7(b), is inserted into the fridge from the top plate. The probe is also made with several stages of

plates that expand to form thermal contact with the plates in the fridge and cool down to the same temperature. A copper part named the 'cold finger' is mounted to the bottom plate of the probe. Devices and filters, called RC filters, are mounted on the cold finger, so they are all cooled down to the base temperature of the MC through physical thermal transmission. Additionally, when the probe is fully inserted, the cold finger's length is designed to have the device stopped at the center of the magnet. So the device is parallel to the z-direction and perpendicular to the x and y directions of the magnet-induced field.

To perform the measurement, we use a Digital-to-analog converters (DAC) system called IVVI (Fig. 3.7 (c)), which is fully controlled by a computer. The source module of the IVVI generates DC voltage bias source, current bias source, and high gate voltage source based on python commands. The Lock-in AC signal can also be added to the source. The measurement module amplifies the measured voltage drop and current value, and sends it to Keithley for DC measurement and Lock-in for AC measurement. All measurement results are then converted back to digital signals and sent to the computer for logging. The IVVI is connected to the pins on the matrix box, and the matrix box is connected to the device through wires in the probe. Electrons at room temperature travel along wires, several filters, and the PCB, and are eventually cooled down to the base temperature. The electrons then tunnel through the device and travel back to the IVVI to give signals.

To reduce noise between 10 MHz to 100 MHz on each DC line, a π filter is applied. On the probe, a copper power filter is used to filter high-frequency noise around several GHz. Furthermore, low-pass RC-filters with a cut-off frequency of 10 KHz can further reduce high-frequency noise and cool down the electron.

4.0 Indium antimonide nanowires with thin tin shells[1]

The Joseph effect is affected by many physical effects. In order to better study the properties related to topological superconductivity with robustness, the disorder caused by the interface defects between semiconductor and superconductor needs to be eliminated. Besides, the recently developed in-situ shell deposition method at cryogenic temperature leads to more smooth and uniform thin superconducting shell on the nanowires, which is the best platform to study Josephson effect. We often say that good food needs the best ingredients. The Sn-InSb nanowires that is introduced in this chapter is the fundamental of all my studies about Josephson junction.

This study focuses on bottom-up grown semiconductor indium antimonide nanowires that are coated with uniform thickness tins shells. The interface between the two materials is abrupt and free of inter-diffusion. Devices for transport are created using in-situ shadowing technique using nearby nanowires as well as flakes, results in etch-free junction. Tin induces a hard superconducting gap of 600-700 μeV and the superconductivity remains up to 4 T magnetic field. The InSb/Sn island also shows the two-electron charging effect, a sign of charge parity stability. These results provide opportunities for superconducting and topological quantum circuits using novel superconductor-semiconductor combinations.

4.1 introduction

The era of intermediate-scale quantum circuits[7, 73] has led to renewed focus on materials considerations, as they impact quantum gate fidelity. Successful solid state approaches are based either on superconductors [74] or on semiconductors [75], with the future topological platform requiring a combination of both [76]. The search for the ultimate material that eliminates the issue of intrinsic decoherence continues. This has led to a push for Majorana

[1]This chapter has been adapted from a collaborative work between our team, UCSB, TU Eindhoven, and Univ. Grenoble, as published in Ref. [33].

qubits, which are expected to be topologically immune to decoherence [77, 78, 79, 80]. The development of high-quality interfaces between superconducting metals and low-dimensional semiconductors has emerged the study of Majorana qubits [32, 81, 82].

Only a few superconductors were explored for Majorana qubits, most notably aluminum, which is also the material of choice for transmon quantum processors [7]. Among advantages of aluminum are self-limiting native oxide and hard induced gap in proximate semiconductors [32, 83, 84]. Due to this, aluminum is widely known to exhibit 2e charging in small islands, a crucial basic property that makes it a low-decoherence superconductor [85, 86, 87, 88, 89, 90, 91]. However, its relatively small superconducting gap that equivalent to 1 K, and low critical magnetic field limit quantum computing to ultra-low temperatures. It further constrains future topological qubit design, as which requires a precise balance of several energy scales [28].

In this study, we present induced superconductivity in InSb nanowires [64, 60] with Sn shells due to proximity effect. InSb has highest electron mobility in the group III-V semiconductor, strong spin-orbit coupling [61], and large Landé g-factors [92] in the conduction band. These are the primary ingredients for having Majorana [15, 16], making it an optimal material for the investigation of induced topological superconductivity [24, 25, 63, 93].

Our study shows that when InSb nanowires are coated with tin, they exhibit a hard induced superconducting gap of up to 700 μeV. Thie superconductivity persists even in the presence of significant magnetic fields, up to 4 Tesla for 15 nm thick Sn shells. Of great significance, small islands of tin display 2e-periodic charging patterns, which is a hallmark requirement for both topological quantum computing and transmon qubits. This effect is crucial for ensuring long quasiparticle stability times. Our findings reveal the potential of more superconductor-semiconductor combinations for quantum computing, offering exciting possibilities for future hetero-structure tailoring and high-fidelity quantum circuits.

4.2 Hard superconducting gap and magnetic field resilient in normal-superconductor device

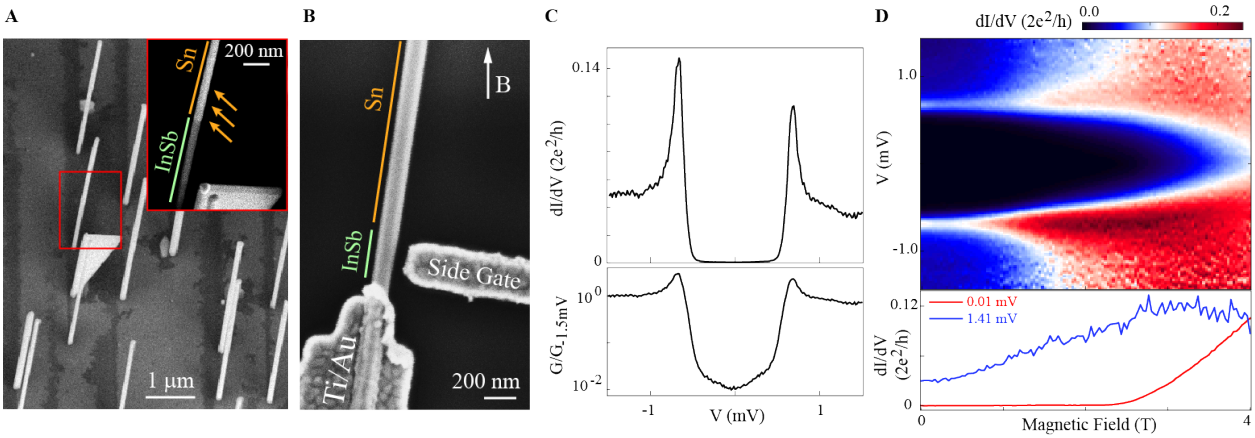

Figure 4.1: (A) Scanning electron micrograph (SEM) showing a triangular InSb flake that stood in the path of a beam of Sn atoms, shadowing the InSb nanowire standing behind. Dark streaks on the InSb substrate are also due to shadowing of the Sn beam by nanowires and flakes. The inset shows the direction of Sn beam and indicates the shadowed and exposed segments of the nanowire. (B) SEM of an N-S device (device A) with a flake-shadowed InSb/Sn nanowire and Ti/Au contacts and a side gate. Magnetic field is applied vertically. (C) Zero magnetic field tunneling conductance spectrum of device A in linear scale (top) and logarithmic scale (bottom), $V_{BG} = 7.5$ V, $V_{SG} = -0.4$ V. (D) Magnetic field evolution of the spectrum in panel (C). Bottom part contain linecuts along dashed lines in the top part. Line traces are at low and high V.

Our first goal is to study electron tunneling from InSb into Sn in a normal metal-superconductor (N-S) configuration. To accomplish this, we require a nanowire with only one end covered by tin. The uncovered end will serve as a tunneling barrier and N-contact. To avoid damaging the InSb during the removal of part of the Sn shell through etching, we utilize an in-situ nanoscale shadowing technique [94, 91] using an InSb flake [95]. During the deposition of Sn in ultra-high vacuum, the InSb flake acts as a shield, standing in front

of the nanowire, to shadow the bottom of the wire (Fig. 4.1(A)).

The tin-coated nanowire is then positioned onto a doped Si/SiOx substrate(Fig. 4.1(B)), which is used as a global back gate chip that discussed in 3.2.2. A side gate is employed with EBL technique that is discussed in 3.2.6,and it is used to define and adjust the tunneling barrier near the edge of the tin-free segment. The tunneling spectrum reveals a two-orders-of-magnitude suppression in conductance around zero bias (Fig. 4.1(C)). This is a hard gap, it indicates the elimination of decoherence pathways due o disorder and spurious subgap states. The superconducting tunneling peak at ± 680 μeV is comparable to the gap of tin. The hard gap persists beyond 2 Tesla in magnetic field, "softening" at higher fields but fully closing around 4 Tesla (Fig. 4.1(D)). The resilience to the external magnetic field is an indicator of a thin uniform shell, and it is another advantage of Sn shell. Because topological superconducting, spin and some novel superconducting qubits are operated at high magnetic fields.

4.3 Transparent Josephson junction defined by in-situ shadow technique

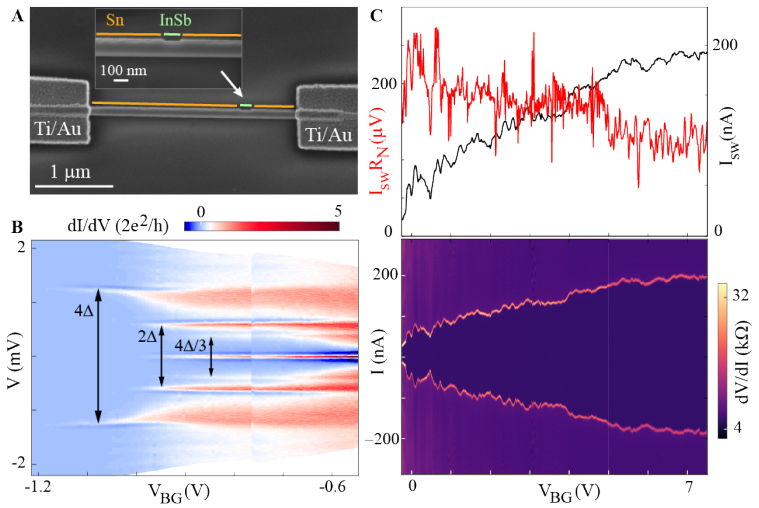

Figure 4.2: (A) SEM of Device B (S-S device). Inset zooms in the shadow junction where Sn shell is visible. (B) Differential conductance as a function of source-drain voltage bias V and back gate voltage, V_{BG}. The double arrows mark resonances 4Δ, $4\Delta/2$ and $4\Delta/3$. (C) Differential resistance as a function of current bias I and V_{BG} (bottom). Top panel shows extracted switching current I_{sw} (black) and $I_{sw}R_N$ (red) as a function of back gate voltage.

In this section, we focus on superconductor-superconductor (S-S) devices with tin covering both ends of the nanowire and a narrow break in the shell serving as an InSb weak link (as shown in Fig. 4.2(A)). To achieve this, we utilize a previously developed shadowing technique for Sn flux by criss-crossing nanowires [94]. We first examine the tunneling between two tin islands (depicted in Fig. 4.2(B)). Our observations reveal a smooth nanowire pinch-off free of any accidental quantum dot states. Three finite-bias resonances are observed and marked as 4Δ, $4\Delta/2$ and $4\Delta/3$ in Fig. 4.2(B). This sequence is a result of multiple Andreev reflection processes, which are a characteristic of transparent S-S junctions. These resonances correspond to 615 μeV $\pm$ 10 μeV, which is somewhat smaller than the gap observed in the N-S device (as shown in Fig. 4.1(C)). At $V_{BG} < -1$ V, only the 4Δ resonance is present, which we interpret as the superconducting tunneling regime. Because the S-S tunneling resonance is a peak in current, it appears as a peak-dip structure in conductance.

The zero-bias resonance peak in Fig. 2B represents the Josephson supercurrent, which is best studied in the current-bias configuration (as shown in Fig. 4.2(C)). The switching current (I_{sw}), which indicates the transition from superconducting to normal state, is depicted as a peak in differential resistance (dV/dI). I_{sw} decays smoothly with more negative V_{BG}. The current-voltage characteristics exhibit weak hysteresis, as reflected in the asymmetry of I_{sw} in positive and negative current biases. In the presence of a magnetic field, the Josephson effect can be observed up to 1.5 T and remains significant with sharp switching up to 0.5 T (as shown in the 4.7). This significant broad range of magnetic fields is a positive development for schemes that require coupling and decoupling of topologically superconducting islands in finite magnetic fields for Majorana fusion or braiding [96, 97]. Measurements on continuous-shell nanowires without shadow junctions resulted in supercurrents ranging from $20-30$ μA, corresponding to a critical current density of 2×10^6 A/cm^2 (as shown in the 4.7). The extracted products of $I_{sw}R_N$ (where R_N represents the normal state resistance) range from $125-225$ μeV, which is significant, and of the same order of magnitude as the gap.

4.4 Parity transition in Tin island

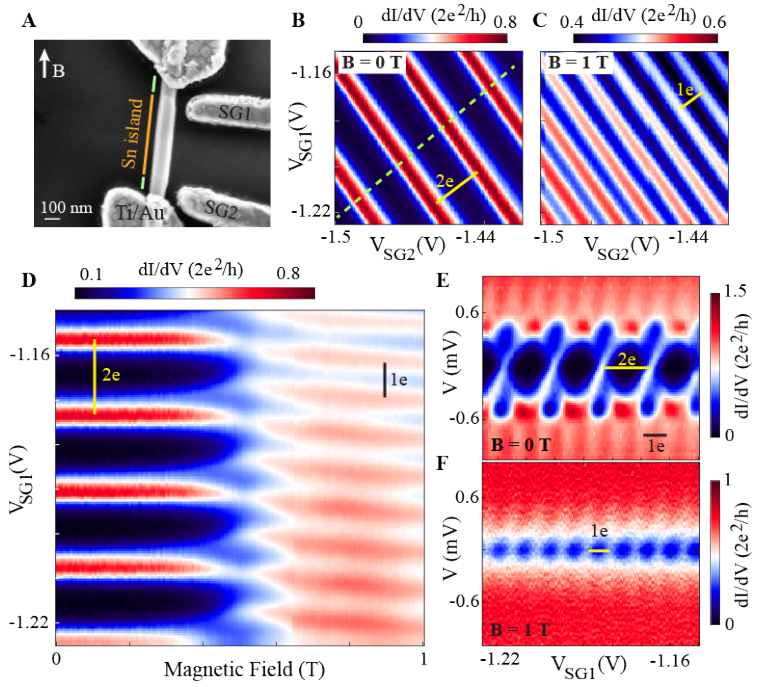

Figure 4.3: (A) SEM of device C showing the Sn island, two shadow junctions with bare InSb, side gates SG1 and SG2 and Ti/Au source-drain contacts which cover the outside Sn segments and suppress superconductivity there. (B) and (C): 2e and 1e tunneling conductance resonances measured at $V = 0$ at B = 0 T and B = 1 T, respectively. (D) Magnetic field evolution of conductance along the dashed cut in panel (B). (E) and (F): V vs gate spectroscopy at B = 0 T and B = 1 T, respectively.

In Fig. 4.3, we present the key findings on the 2e charging of a tin island in the N-S-N geometry, which is defined between two nanowire-shadow junctions (as shown in Fig. 4.3(A)). At zero magnetic field, we observe a single family of Coulomb peak resonances that are consistent with charging the entire island (as shown in Fig. 4.3(B)). However, at a finite magnetic field of 1 T, the frequency of Coulomb resonances doubles (as shown in Fig. 4.3(C) and 4.3(D)). We attribute the data at zero field to 2e charging and the data at finite field to 1e charging. The transition from 2e to 1e is due to the superconducting gap or the lowest subgap state dropping in energy below the charging energy, which we estimate to be

0.3 meV (as shown in Figs. 4.3(E) and 4.3(F)). At finite magnetic field, it is less energy-intensive to add electrons to the island one-by-one, whereas near zero field, due to hard gap superconductivity, it is more advantageous to add electrons in pairs.

The two-electron charging effect is crucial for topological quantum computing, as the states of a topological qubit are distinguished by the even or odd charge parity of the island. If only 1e charging periodicity were observed, it would indicate that despite the presence of a well-defined superconducting gap, electrons can be added to the island one at a time, thus scrambling the ability to distinguish the states of a topological qubit. This is also harmful for transmon qubits, where single electron tunneling acts as a decoherence mechanism [98].

4.5 Interface characteristics between Sn and InSb

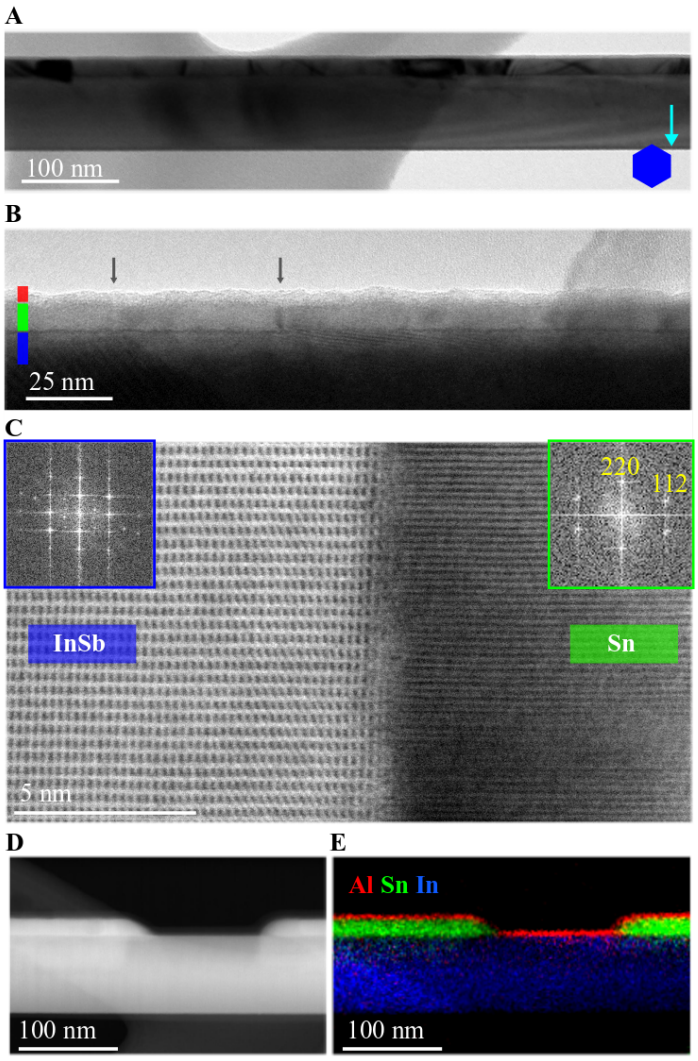

Figure 4.4: (A) Side-view TEM image along the ⟨112⟩ zone axis showing a homogeneously thin shell. (B) Higher magnification TEM of the AlO_x (red) - Sn (green) - InSb (blue) stack. The Sn grain boundaries are highlighted by arrows. (C) HR-STEM image of the Sn-InSb interface. The insets show Fourier transforms to the left and to the right of the interface. (D) High-angle annular dark-field STEM image of a shadow junction. (E) EDX elemental mapping of the shadow junction in (D). The Al-rich layer (red) corresponds to AlO_x, oxygen not shown for clarity.

Tin is an unusual material that undergoes a phase transition at 13°C, with two distinct crystal phases. The low-temperature phase, α-Sn, has a diamond cubic lattice and is a semimetal that can also be a topological insulator in monolayer form [99, 100, 101]. On the other hand, β-Sn, which is tetragonal, is a metal with a superconducting transition temperature of 3.7 K.

The structural properties and elemental distribution of tin on InSb nanowires were analyzed using Transmission Electron Microscopy (TEM) as depicted in Fig. 4.4. The TEM images show a polycrystalline Sn shell of uniform thickness surrounding the InSb nanowire (Fig. 4.4(A)). The grain size of the Sn shell ranges from 25x25 nm to 50x60 nm, and the Sn-InSb interface is abrupt, with some Sn grains demonstrating epitaxial relationship with InSb (as shown in the 4.7). The high-resolution annular bright field-scanning TEM image (Fig. 4.4(C)) depicts a section of the interface where the {111} planes of the zinc-blende InSb are aligned with the lattice planes of a Sn grain, with a lattice distance of 2.04 Å, matching the {220} interplanar distance of β-Sn. Out of the 13 grains analyzed along the same nanowire, 11 were identified as β-Sn from the fast Fourier transform analysis of the interplanar distances (Fig. 4.4(C), inset), with only two showing preferential epitaxial relationship with InSb. On the other hand, α-Sn is lattice-matched to InSb and can grow epitaxially [102]. The presence of predominantly α-Sn shell at room temperature, as seen in the TEM analysis, is in line with the superconductivity observed at low temperatures, suggesting that no phase transformation of Sn took place during device cooldown.

In addition to having a uniform shell thickness, the nanowire shadow junctions used in the S-S and N-S-N devices are sharply defined, with Sn islands abruptly delimited on either side of the junction (Fig. 4.4(C)). Energy-dispersive x-ray spectroscopy (EDX) analysis confirms the isolation of the Sn islands from one another and the absence of inter-diffusion between Sn and In (Fig. 4.4(D)). A uniform, 3-nm-thick AlOx passivation layer covers the entire nanowire, and while oxidation at the Sn-InSb interface has not been detected, it cannot be completely excluded (see 4.7.1).

4.6 Conclusion

Our findings demonstrate that the attainment of robust, hard-gap, field-resilient superconductivity and two-electron charging does not strictly require defect-free epitaxial wire-shell interfaces or single vacuum cycle growth of nanowires and shell. Instead, the key factors in achieving this are (1) removal of the native oxide from the InSb nanowire using atomic hydrogen before Sn growth, (2) cooling the nanowires with liquid nitrogen during the metal evaporation process to create a uniform ultrathin shell, and (3) immediate passivation of the wire-shell hybrid with a stable dielectric material. These steps are further discussed in 4.7.1.

The next steps in this line of research should involve a deeper exploration of the formation of Sn and InSb interfaces and the search for robust signatures of topological superconductivity through experiments in the Majorana geometry. The Sn/InSb nanowire system holds potential for use in transmon and topological qubits, and there is potential to explore other metals as replacements for Al in an effort to find materials that result in decoherence-free qubits. However, it should be noted that further study of the dominant decoherence mechanisms may be needed to establish the requirements for fully functional topological qubits.

4.7 Supplementary materials and Methods

4.7.1 Method

4.7.1.1 Nanowire growth.

InSb nanowires are grown using the vapor-liquid-solid technique in a horizontal metal-organic vapor phase epitaxy reactor. The first nanowires used in this work are stemless InSb nanowires with flakes as shadow objects (Fig. 4.1(A)) [60, 95]. Both InSb nanowires and flakes are grown on an InSb (111)B substrate with a selective-area mask and gold as catalyst. The second type of nanowires, shown in Figs. 4.2(A) and 4.3(B) are shadowed by other nanowires [94]. The InP (100) substrates are etched to expose the two {111}B facets,

on which gold particles are deposited with an offset on the two opposing facets of a trench. Nanowires grow towards each other, such that the front wire shadows the back wire. InSb wires are grown on InP stems.

4.7.1.2 Sn shell growth.

After transit in air, nanowire chips as grown are loaded into vacuum for subsequent growth of Sn shells. The chips are gallium bonded to molybdenum blocks. Atomic hydrogen cleaning is performed at 380°C (thermocouple temperature) for 30 minutes, at an operating pressure of 5×10^{-6} Torr consisting primarily of hydrogen ambient. Once cleaned, the samples are transferred in-vacuo to an ultra-high vacuum chamber dedicated for metal evaporation (base pressure $< 5 \times 10^{-11}$ Torr). Here, the nanowire samples are cooled to 85 K (-188°C) for 2 hours, prior to tin evaporation. 15-nm-thick tin is then evaporated from an effusion cell at a growth rate of 7.5 nm/hr and an evaporation angle close to 60° from sample normal. This shallow evaporation angle aids in-situ formation of Sn islands with nanowire or flake shadows. After Sn evaporation, while the sample is still expected to be at cryogenic temperatures (due to the thermal mass of the molybdenum block), a 3-nm-thick shell of AlO_x is electron-beam evaporated onto the nanowire sample, at normal incidence. The samples are then allowed to warm up to room temperature in vacuum.

4.7.1.3 Device fabrication and measurements.

Device fabrication is similar to previous work on wires with epitaxial Al film [94]. Wires are transferred onto doped and thermally oxidized Si substrates using a micromanipulator under an optical microscope. Contacts and gates are patterned by electron-beam lithography by curing the resist at room temperature in vacuum to avoid nanowire heating and potential interdiffusion of Sn and In. Ar ion milling is performed to remove the AlO_x layer before evaporating 10/150 nm of Ti/Au. Measurements are performed in a dilution refrigerator with a 30 mK base temperature using a combination of direct current and lock-in techniques. All voltage bias data are two-terminal measurements. A series resistance of $\approx 5k\Omega$ due to measurement setup was taken into account in calculating conductance in all figures as well

as renormalizing V axis in Figs 4.2(B). TEM studies were performed using a probe corrected microscope operated at 200 kV, equipped with a 100 mm^2 EDS detector.

4.7.2 Supplementary Materials

4.7.2.1 Zero bias peak in S-NW-S device E

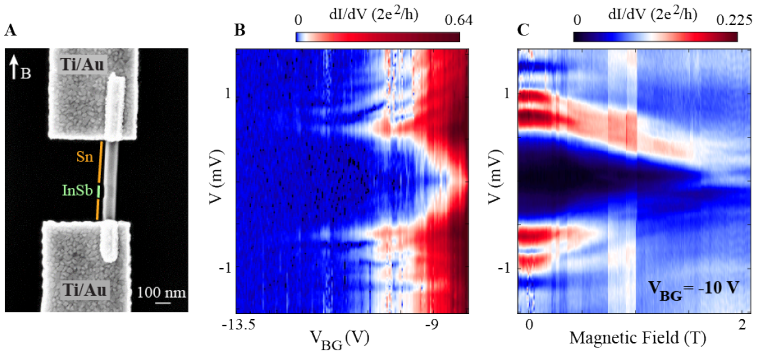

Figure 4.5: (A) SEM image of device E, a single shadow S-S device. The nanowire is aligned parallel with magnetic field. (B) Differential conductance as a function of bias and back gate voltages. V axis is as measured and not renormalized due to series resistance. (C) Magnetic field evolution of conductance at $V_{BG} = -10$ V. Near B = 1.75 T a zero bias conductance peak emerges from coalescence of two higher bias resonances. At these high magnetic fields the induced gap is soft, allowing for conductance at low bias, including the zero bias. The zero-bias peak is approximately 0.1 $2e^2/h$. We attribute this peak to a trivial zero-bias crossing by subgap Andreev states.

4.7.2.2 Full shell Sn-InSb device

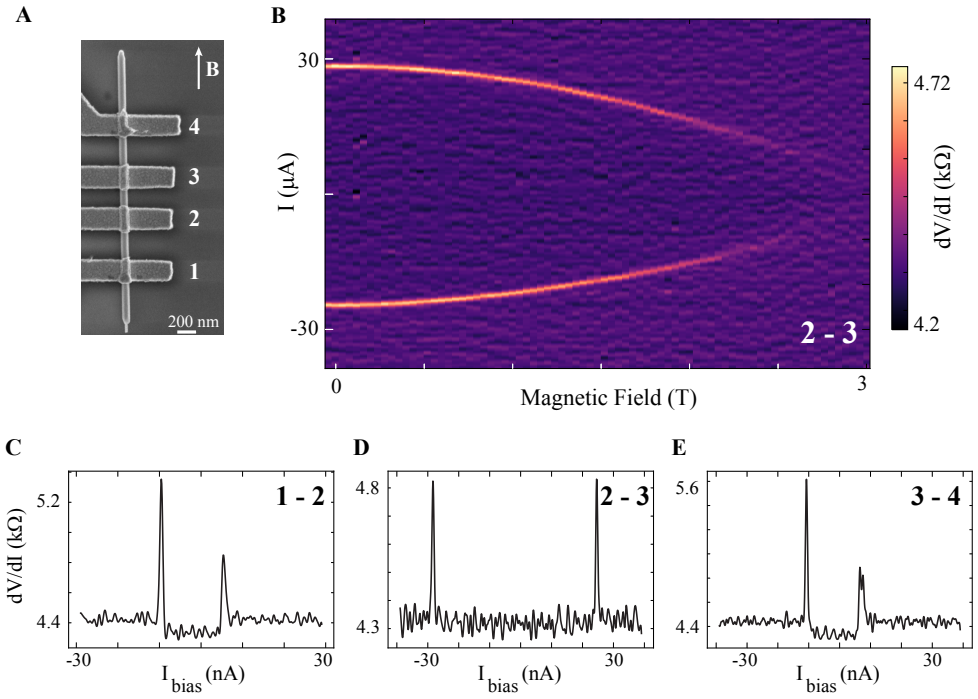

Figure 4.6: Device G has an uninterrupted Sn shell on an InSb nanowire without any shadows. The nanowire is grown on an InP stem. (A) SEM image showing 4 Ti/Au contacts labeled 1 to 4 noting different configurations for 2-terminal current bias measurements. (B) 2-terminal differential resistance as a function of bias current and magnetic field. Supercurrent persists up to 3 T, magnetic field is aligned parallel with the nanowire. (C-E) Differential resistance at zero magnetic field from different 2 terminal configurations. A variation in critical currents is observed along the shell with critical current being the highest in the central region of the nanowire. One possible explanation is the presence of grains of α-Sn which are not superconducting, with a random distribution along the nanowire.

4.7.2.3 Sn grains in the shell

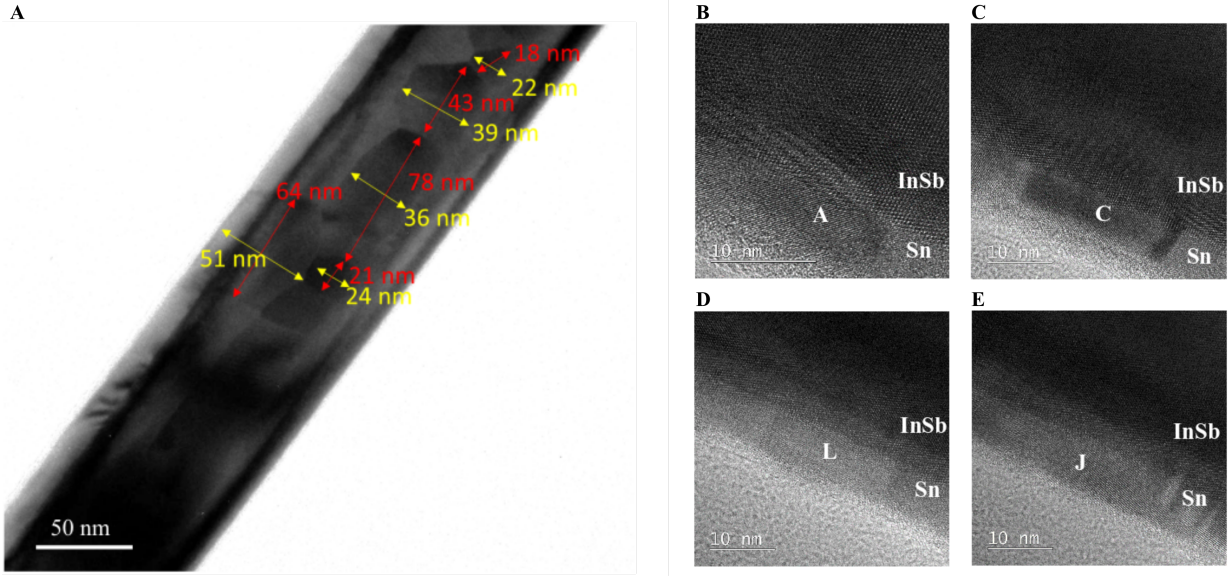

Figure 4.7: (A)Side view bright field TEM image acquired along the ⟨110⟩ zone axis showing multiple Sn grains in the shell. Arrows and numbers are used to indicate the sizes of grains. (B)-(E) Side view TEM images of the core-shell interface, displaying four of the Sn grains listed in Table 4.1. (B) Grain A, which cannot unambiguously be assigned to either α-Sn or β-Sn. (C) Grain C, β-Sn grain epitaxially related to the InSb lattice. (D) Grain L, α-Sn. (E) Grain J, β-Sn.

Grain	d_{hkl} (exp)	hkl β	d_{hkl} β (lit)	% deviation from lit β	hkl α	d_{hkl} α (lit)	% deviation from lit α	epitaxy
A	0.198	211	0.2010	-1.2%	311	0.1956	+1.5%	
C	0.209	220	0.2065	+1.0%	311	0.1956	+6.7%	YES
D	0.203	220	0.2065	-1.4%	311	0.1956	+4.1%	
		211	0.2010	+1.3%	-	-	-	
E	0.206	220	0.2065	-0.4%	311	0.1956	+5.1%	
F	0.205	220	0.2065	-0.5%	311	0.1956	+5.0%	
G	0.274	101	0.2772	-1.3%	211	0.264	+3.7%	
I	0.282	101	0.2772	+1.7%	211	0.264	+6.7%	
J	0.277	101	0.2772	-0.0%	211	0.264	+5.0%	
K	0.203	220	0.2065	-1.8%	311	0.1956	+3.7%	
L	0.267	101	0.2772	-3.7%	211	0.264	+1.1%	
M	0.280	101	0.2772	+1.2%	211	0.264	+6.2%	
N	0.287	200	0.2920	-0.8%	-	-	-	
R	0.204	220	0.2065	-1.2%	-	-	-	
	0.149	112	0.1472	+1.3%	-	-	-	

Table 4.1: Phase identification based on lattice spacings dhkl of 13 Sn grains imaged using high-resolution TEM. All dhkl values are determined from Fast Fourier Transform patterns constructed from the HRTEM images. All patterns were calibrated by InSb lattice spacings present in the same images. The 211α spacing is not allowed based on crystal symmetry but can appear in HRTEM images. The experimental inaccuracy in the dhkl values is estimated to be 2.0 percent considering the limited number of pixels in the FFT patterns. Based on this criterion, all grains can be assigned to the β-Sn phase apart from grains A and L. Grain R is presented in Fig. 4.4 (C).

5.0 Supercurrent in first electron transverse mode

Hybrid superconductor-semiconductor materials are fueling research in mesoscopic physics and quantum technology. Recently demonstrated smooth β-Sn superconductor shells, due to the increased induced gap, are expanding the available parameter space to new regimes. Fabricated on quasiballistic InSb nanowires, with careful control over the hybrid interface, Sn shells yield critical current-normal resistance products exceeding temperature by at least an order of magnitude even when nanowire resistance is of order 10kΩ. In this regime Cooper pairs travel through a purely 1D quantum wire for at least part of their trajectory. Here, we focus on the evolution of supercurrent in magnetic field parallel to the nanowire. Long decay up to fields of 1T is observed. At the same time, the decay for higher occupied subbands is notably faster in some devices but not in others. We analyze this using a tight-binding numerical model that includes the Zeeman, orbital and spin-orbit effects. When the first subband is spin polarized, we observe a dramatic suppression of supercurrent, which is also confirmed by the model and suggests an absence of significant triplet supercurrent generation.

5.1 Introduction

Semiconducor nanowire-based Josephson junctions (JJs) have been explored as elements for superconducting transmon qubits [103, 104] and Andreev qubits [105]. The same one-dimensional(1D) super-semi hybrid system also fulfills basic requirements for emerging topological superconductivity and Majorana bound states (MBS) at nanowire ends [15, 16, 106]. Attempts at exploring MBS in nanowire JJs were through the search for factional a.c Josephson effect [107, 108, 109]. Topological qubits based on nanowire JJs containing MBS have been proposed theoretically [96, 80]. In the simplest and purest form, Majorana modes are envisioned in a single-subband nanowire.

While studies of supercurrents in nanowires or point contacts have led to an array of

interesting discoveries so far [107, 37, 110, 111, 34, 112, 35], one outstanding challenge remaining is that supercurrent in the last occupied transverse mode (single subband) is strongly suppressed. It is either not observed or provides with a single too low to enable detailed studies [113, 114, 115, 112]. The reasons for this are not fully understood, however they are likely related to either finite interface transparency such as in devices involve ex-situ shell deposition, smaller induced gap such as in Al-InAs structures, residual scattering or other effects.

Our approach is to combine InSb nanowires with Sn shells. Through advances in vapor-liquid-solid growth quasi-ballistic InSb nanowires were achieved [59, 60]. Quantized non-superconducting conductance has been established in InSb nanowires with normal metal electrodes [116, 70]. The recently introduced superconducting Sn shells facilitate transparent contacts, and critical current-normal state resistance products exceeding temperature and those previously available in Al-based nanowire junctions [33]. Junctions in the Sn shell are defined on InSb nanowires by nanowire shadowing, which reduces processing and increases the likelihood of ballistic devices. Junction made with InSb nanowires and NbTiN leads are studied with same method, and the measurement results are compared with that in Sn-InSb devices as additional supplementary materials.

Subband-resolved transport is verified through the measurements of conductance at finite bias, and the evolution of it with gate voltage, source drain bias voltage and magnetic field. In the gate voltage and conductance range that corresponds to the first occupied transverse mode, we observe supercurrents as high as 20 nA. We investigate the gate voltage and magnetic field evolution of supercurrents in several nanowire devices both in the single-mode and in the multi-mode regimes.

The mechanisms of decay of supercurrent with magnetic field are studied including the relative contributions of orbital interference phenomena, residual disorder, spin-orbit and Zeeman effects by comparing the data to a tight-binding model. The spin-polarization of the first subband at finite field suppressed supercurrent dramatically, leading us to conclude that no triplet supercurrent was generated.

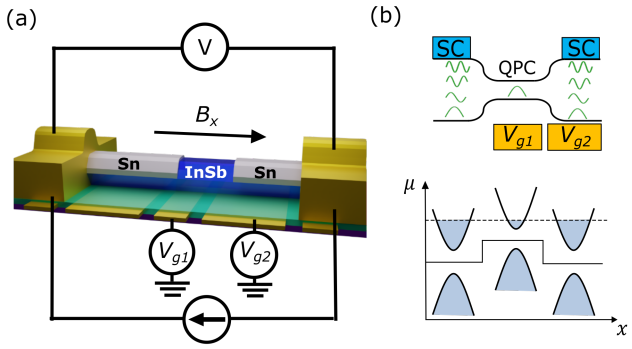

Figure 5.1: (a) Schematic of a shadow nanowire Josephson Junction device. The wire is along $\hat{x}$ which is also the direction of external magnetic field B_x. (b) Cartoon of a single-mode junction controlled by electrostatic gates V_{g1} and V_{g2}. The leads are shown with higher subbands occupied. The lower panel corresponds to a chemical potential profile μ(x) used in tight-binding simulations.

5.2 Device description

Fig. 5.1(a) presents a schematic diagram of the nanowire Josephson junction device. An InSb nanowire (blue) is half-covered by a Sn shell (silver) and positioned above local gate electrodes (gold), with Ti/Au contacts (gold). In order to prepare the junction itself, standing InSb nanowires approximately 100 nm in diameter are coated with a 15 nm layer of Sn [33]. In front of the nanowire, another nanowire shadows the flux of Sn to create two disconnected Sn segments. Nanowires with such shadow-defined junctions are transferred onto chips patterned with local electrostatic gate electrodes covered by HfOx dielectric. Contacts to wires are made using standard electron beam lithography and thin film deposition of Ti/Au layers.

The supercurrent flows along the $\hat{x}$ direction, and an external magnetic field, B_x, is applied parallel to the wire. A current bias, I_{bias}, is applied across the device (illustrated by a black arrow), and the voltage across the device is measured using DC and AC multimeters in a two-point measurement setup. Two local bottom gates, V_{g1} and V_{g2}, are located beneath

the junction region. Measurements are performed in a dilution refrigerator with a base temperature of ∼50 mK equipped with a 3D vector magnet.

Figure 5.1(b) uses cartoons to demonstrate the control of transverse mode numbers in the nanowire by local bottom gates during experiments, as well as the definition of local chemical potential in simulations. In the illustration, gate voltage V_{g1} precisely adjusts the number of conduction channels, resulting in a single occupied transverse mode in the region labeled QPC (quantum point contact). Meanwhile, gate voltage V_{g2} tunes one of the adjacent region which can have a higher subband occupancy. To emulate the realistic conditions in numerical simulations, we use two chemical potential μ settings, one for leads and one for the QPC.

5.3 Supercurrent in the first electron mode

In Fig. 5.2(a) we plot two gate traces of conductance, one at zero magnetic field and one at large magnetic field (B=8T). The zero-field trace contains non-monotonic resonances due to quantum interference caused by backscattering, as well as charge jumps. This is in line with previous reports of quantum point contact behavior in nanowires [116, 70]. Backscattering can be suppressed by large magnetic field, therefore the high magnetic field trace demonstrates a sequence of spin-resolved plateaus at $G_0/2 = 1 \times e^2/h$ values. Using the high magnetic field trace as reference, we approximately identify the gate voltage interval that corresponds to the single occupied mode at B=0 ($V_{g1} < 1.1$ V, green dashed line), around conductance value of $G_0 = 2e^2/h$. For the data shown, we estimate the highest conductance to be $6G_0$, corresponding to a maximum of 6 transverse modes. Comprehensive evidence of QPC behavior in device A is obtained from the magnetic field evolution of finite-voltage bias conductance maps for various gate voltage settings, which demonstrate diamond-shaped regions of relatively flat conductance in bias-gate space, and Zeeman splitting of these plateaus (see supplementary materials and Fig.5.3).

In Fig. 5.2(b) we plot the current bias data that closely corresponds to the conductance traces from panel (a). The supercurrent appears as dark-blue regions around zero bias.

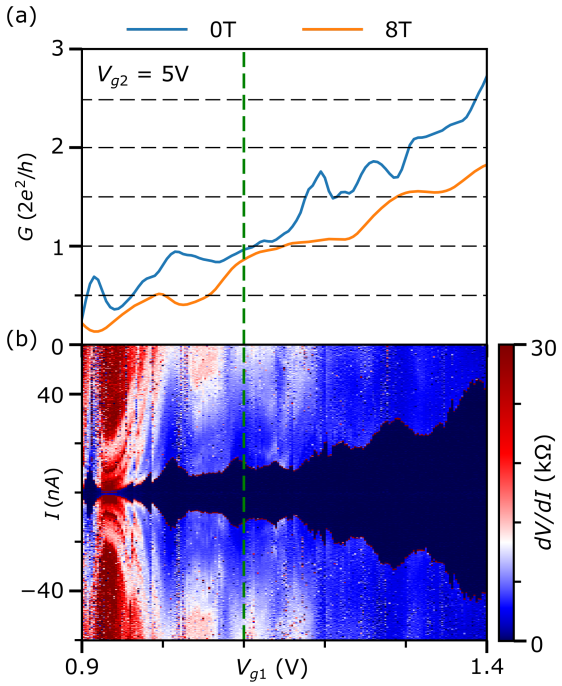

Figure 5.2: (a) Differential conductance $G(dI/dV)$ taken at finite bias V_{bias}=2mV at B=0T and at zero bias for B=8T. (b) Current bias measurement of differential resistance $R(dV/dI)$ showing the evolution of supercurrent at B=0T. In this figure $V_{g2} = 5$V. Green dashed line is used to indicate the approximate boundary between the first mode and higher modes based on conductance. Panels (a) and (b) are from separate measurements on Device A.

On the left side of the green line, for more negative gate voltages, supercurrent is carried by the first transverse mode. The magnitude of the first mode switching current I_{sw} in these and other data is from 10 to 20 nA. Given the normal state resistance around 13 kΩ ($1G_0$), the $I_{sw}R_N$ product falls within the range of 150-250 μeV(Fig. 5.18). This value somewhat suppressed compared to the more open regime, but is of the same order as the superconducting gap gap of Sn ($\Delta = 650$ μeV) and is consistent with values reported in previous studies [33, 35]. Thus signal levels allow for a deeper investigation of supercurrent in the few-subband regime.

5.4 Suppression of supercurrent in the spin-polarized regime

The first question we investigate is the evolution of supercurrent as spin polarization develops in the QPC region, when the plateau $G_0/2 = 1 \times e^2/h$ develops at finite magnetic field. The emergence of the plateau is demonstrated in Fig. 5.3(a) in the transconductance map - the characteristic "V"-shaped region corresponds to the spin-polarized plateau. Spin polarization becomes resolved at fields between 0.5-1.0T, while supercurrents are generally observed up to 2T. This allows for the study of the effect of spin polarization on supercurrent.

Fig. 5.3(b) shows supercurrents extracted from gate voltage sweeps at fields between 0 and 2T. A switching current I_{sw} is a current at which finite voltage develops across the junction, this may or may not closely follow the Josephson critical current which is a measure of Josephson coupling energy. In data processing, switching current is defined as I_{bias} for which differential resistance exceeds 2kΩ. We superimpose the boundary of the spin-polarized region, extracted from panel (a) using peak finding (green squares). Note that panel (a) is at $V_{bias} = 2\ mV$ while panel b is at zero voltage, meaning the boundaries may be shifted. To quantify the decay rate of I_{sw} in magnetic fields and compare it for different gate voltages, we normalize the magnitude of the switching current as $NorI_{sw}(B, V) = I_{sw}(B, V)/I_{sw}(B = 0, V)$ and plot it as a function of B_x and V_g.

Overall, the first mode supercurrent exhibits a slow, long decay up to $B_x = 1$T, eventually disappearing as the system transits to the normal state. However, we found no supercurrent

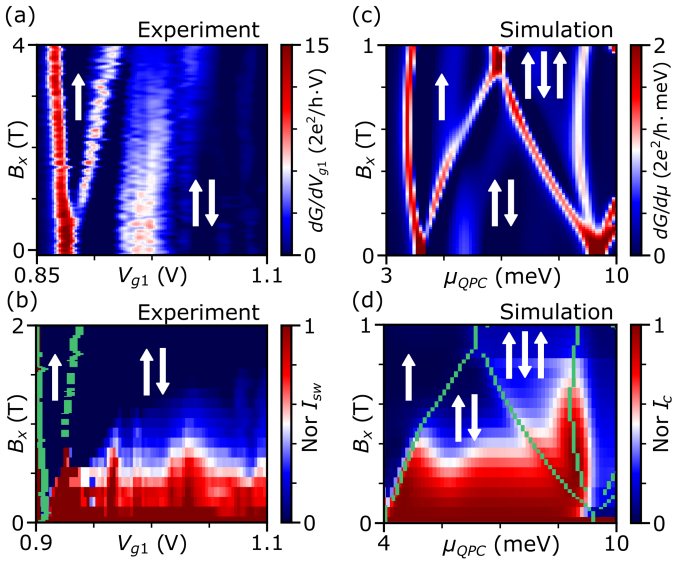

Figure 5.3: Comparison between experiment (a, b) and simulation (c, d): (a, c) Transconductance dG/dV_{g1} vs B_x and V_{g1} (μ_2) is measured at V_{bias} = 2mV (0mV for simulation). V_{g2} = 5 V. The electron spin at each mode is indicated with white arrows. (b, d) Normalized I_{sw}/I_c (Experiment/Simulation) is plotted as a function of B_x and V_{g1} (μ_2). The boundary between the lowest spin-full mode and spin-polarized mode, extracted from (a), is indicated with a green line. The chemical potential under the leads, $\mu_1, \mu_3 = 20\ meV$, allows for a maximum of 6 available subbands through the leads. Other simulation parameters include spin-orbit strength $\alpha = 100nm \cdot meV$, Zeeman g-factor ($g = 50$), effective mass $m_{eff} = 0.015m_e$, temperature $T = 100mK$, site disorder $\delta U = 0meV$.

within the spin-up band, or at least the signal is rapidly suppressed in that region. At the same time, supercurrent found in the region of the phase diagram directly adjacent to the spin-polarized "V". This serves as an additional confirmation that it corresponds to the single subband regime with two spin channels.

We conduct a numerical investigation of the system's microscopic properties using a tight-binding model that mirrors the experimental geometry, as shown in Fig.5.1(b). This model was designed to study supercurrent interference in nanowires using KWANT [117, 118, 34]. It includes the effects of spin-orbit interaction, the orbital vector potential, Zeeman splitting, electron temperature, and on-site disorder. To reproduce the quantized conductance results observed in our experiment, no disorder is considered here ($\delta U = 40meV$), same as what the initial version of the model did [34].

The new aspect here is the varied chemical potential along the nanowire, allowing for the possibility that the number of occupied subbands is not constant throughout the device. For the results in Fig. 5.3(c) we set chemical potentials in both the leads to $\mu_{lead} = 20meV$, corresponding to a few occupied subbands ($\approx$6), we then vary μ_{QPC}. The boundary between the lowest spin-full and spin-polarized modes is extracted from the conductance calculation and plotted alongside the normalized I_c in Fig.5.3(d) in a manner similar to how the experimental data are presented. The electron spin in each mode is labeled with white arrows. It should be noted that the values in the simulation do not exactly correspond to those in the experimental device but serve as indicators. For example, the boundary between G_0 and $1.5G_0$ converges at $B_x = 0.9T$ in the simulation, whereas they never intersect in the experiment, even up to $B_x = 8T$. In the $1.5G_0$ mode, we find that the supercurrent persists to a larger field compared to the first mode supercurrent, which is not observed experimentally but is likely due to microscopic details of the simulation.

In agreement with the experimental finding, the normalized I_c does not survive in the spin-polarized regime at $0.5G_0$. This indicates that the model correctly captures the system and does not predict triplet supercurrent under the most basic conditions. Experiments on superconductor-ferromagnet-superconductor structures found that in junctions with pristine interfaces supercurrent vanishes in shorter junctions, while counterintuitvely it survives to in longer junctions when interfaces are disordered [119]. A disordered interface is believed

to facilitate spin flipping into triplet state and flipping back to singlet at the second interface. It is worth investigating if interface roughness, in combination with spin-orbit interaction and/or magnetic impurities culd extend supercurrents into the spin-polarized regime in superconductor-semiconductor junctions, hinting at the generation of triplet supercurrents.

5.5 Single-mode versus multi-mode regimes

Earlier work on nanowires suggested that the single-mode supercurrents are unique, because without other occupied subbands there is no inter-subband interference. This interference was associated with rapid decay of supercurrents in magnetic field, and therefore a slower decay is expected for a single-subband junction [34].

In Fig. 5.4 we show switching current maps in gate-field space from three devices. Device A is the source of data in Figs. 5.2 and 5.3, where the few mode regime was carefully explored. Devices B and C are fabricated using the same Sn-InSb nanowires and in the same geometry (see supplementary materials for device images and additional data). While conductance steps are observed, the QPC evidence is less comprehensive in devices B and C. On the other hand, B and C are studied into the more open regime. The number of occupied subbands is estimated from conductance and indicated above the figures.

In all three junctions, supercurrents grow at more positive gate voltages that correspond to higher subband occupations [Figs. 5.4(a)(b)(c)]. In magnetic field, signal is observed up to, and occasionally beyond B=2T. The magnetic field decay rate of switching current can be explored in maps normalized to zero-field values [Figs. 5.4(d)(e)(f)]. Devices B and C clearly exhibit a more rapid relative decay of switching current in the multi-mode regime, compared with the 1-2 mode regime. The rapid decay takes place at fields below approximately 0.5T followed by a persistent lower signal. In the single-mode regime, no rapid decay is observed, yet the overall signal level is smaller and comparable to that seen at higher fields in the multi-mode regime (see supplementary information for detailed magnetic field dependences of current-voltage characteristics for all three devices.) Results in device A do not extend to more modes, but from the data available they are not in contradiction with findings from B

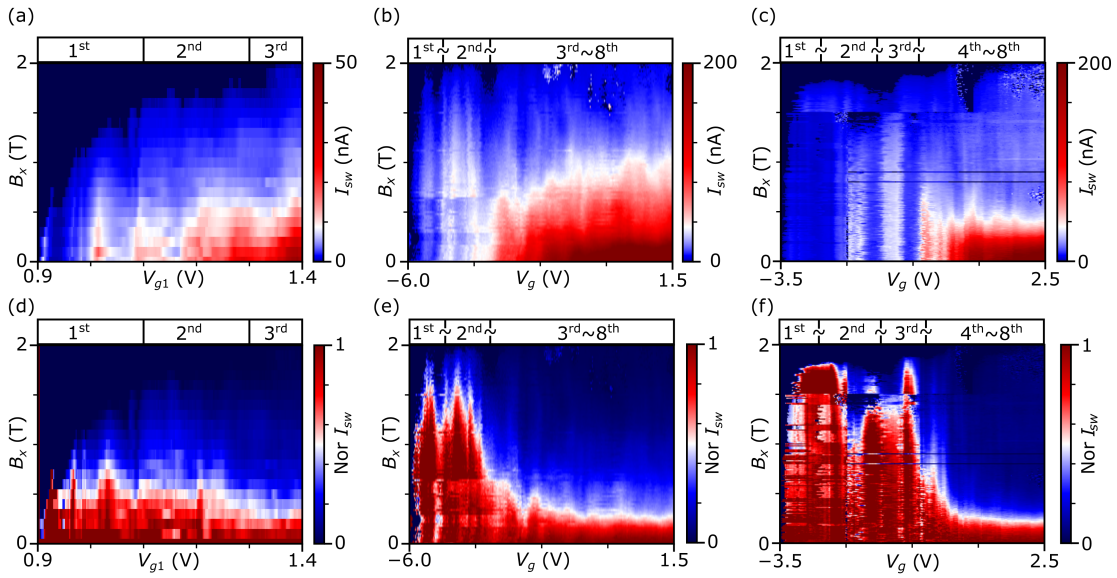

Figure 5.4: (a)-(c) Magnitude of switching current I_{sw} extracted for gate scans and plotted as a function of gate voltages V_g and parallel external field B_x measured in Device A, B, and C. (d) Additional data for Fig. 5.3(b) (Device A) is presented, showcasing normalized I_{sw} at higher gate voltages (more modes). (e) and (f): Normalized I_{sw} as a function of B_x and V_g is measured in Device B and Device C. The boundary between different subbands are extracted at zero field and indicated by the yellow dashed line. The number of the highest transverse mode being occupied is labeled above each panel.

and C.

We discuss the decay rates of supercurrent in magnetic field from the experimental and theory points of view. On the experiment side, one concern that should be mentioned is that smaller switching currents can deviate substantially from the actual Josephson critical currents. At the same time, in these junctions signficant $I_{sw}R_N$ products exceeding temperature by an order of magnitude are not expected to result in significant premature switching in junctions. Another experimental concern is that the shapes of $I_{sw}(B)$ can be affected by presence of finite voltage resonances such as due to Multiple Andreev Reflections (MAR) frequently observed in these junctions leading to peculiar non-monotonic field dependences (see supplementary information for examples.)

5.6 Tight-binding simulation of junction with leads

On the theoretical side, we started with a basic assumption of only a single mode occupied in the device. While this may be the case in the middle of the junction, the leads may have higher subband occupations. Interference between supercurrents carried by different subbands can take place in the leads and result in faster decay. The earlier model did not include this consideration, so we address it here.

Using KWANT, we numerically calculate the evolution of I_c in the parallel field B_x [Fig.5.5]. The chemical potential in the leads and junction region is locally adjusted to 5 meV (one mode) or 20 meV (six modes). Spin-orbit interaction and Zeeman effect are present in all calculations. The effects of small disorder are explored in the supplementary information. In agreement with earlier results [34], the model demonstrates the slowest decay when both the leads and the QPC region are set to one occupied subband. The decay is more rapid when the leads are set to 6 subbands, and opening the QPC to 6 subbands accelerates the decay further. The difference between QPC and 1 and at 6 is not dramatic when the leads are open.

Experimentally it is much more challenging to realize a device where the entire nanowire is in the single subband regime, compared with realizing a short QPC region. Supplementary

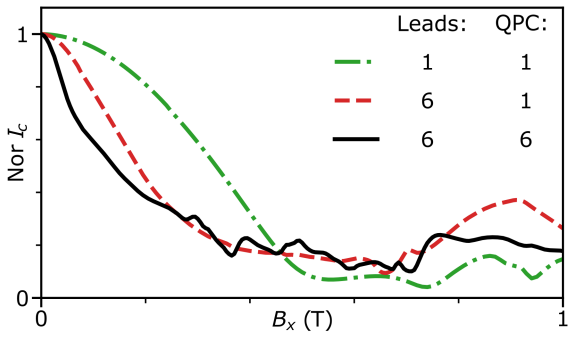

Figure 5.5: Normalized critical current as a function of parallel field B_x for different combinations of terms in the Hamiltonian of the numerical model. The Zeeman effect ($g = 50$) and spin-orbit strength $\alpha = 100nm \cdot meV$ are present in all curves. The local chemical potential and corresponding number of conduction channels in the leads and QPC region are illustrated with a small diagram in each panel. $\mu = 5$ and 20 meV result in one and six spin-full transverse modes in the nanowires, respectively. The other simulation parameters are consistent with those used in Fig. 5.3 (b) and (d).

information shows more maps for different settings of V_{g2} for device A. More negative settings of V_{g2} result, in principle, in a lower subband occupation in one of the leads. While the decay rates become more uniform at negative V_{g2}, the limited range of V_{g1} and the inability to tune the second lead region prevent us from concluding on the origins of this effect and whether the numerical simulations explain it. Since single-mode nanowires are desirable for Majorana zero mode experiments, future work should focus on realizing this regime and the insights obtained in the present work may be helpful.

5.7 Supplementary Materials

5.7.1 Fabrication and Measurements

Sn-InSb devices Nanowires are transferred onto a silicon (Si) chip with predefined local gates. These electrostatic local gates are patterned using 100 keV Electron Beam Lithography (EBL) on undoped Si substrates. The local gates feature mixed widths of 80 and 200 nm and are separated by a distance of 40 nm. The gates are metalized through electron beam evaporation of 1.5/6 nm Ti/PdAu and subsequently covered by a 10 nm ALD HfOx dielectric layer.

According to the Scanning Electron Microscope images of all devices examined in this report, the lengths of the Josephson junctions (JJs) created with Sn-InSb nanowires range from 120 to 150 nm. The junction width is consistent with the nanowire width, which is approximately 120 nm. After positioning the nanowires onto the gates, the entire chip is coated with PMMA 950 A4 electron beam resist. The resist is dried at room temperature using a mechanical pump in a metal desiccator for 24 hours. EBL is then employed to define normal lead patterns. Following development, resist residue is cleaned in an oxygen plasma asher. Within the electron beam evaporator, an in-situ ion mill is initially used to remove the AlOx capping layer from the nanowires in the contact area, after which 10 nm/130 nm Ti/Au is deposited on the chips.

Two-point transport measurements are conducted using a current source and a parallel

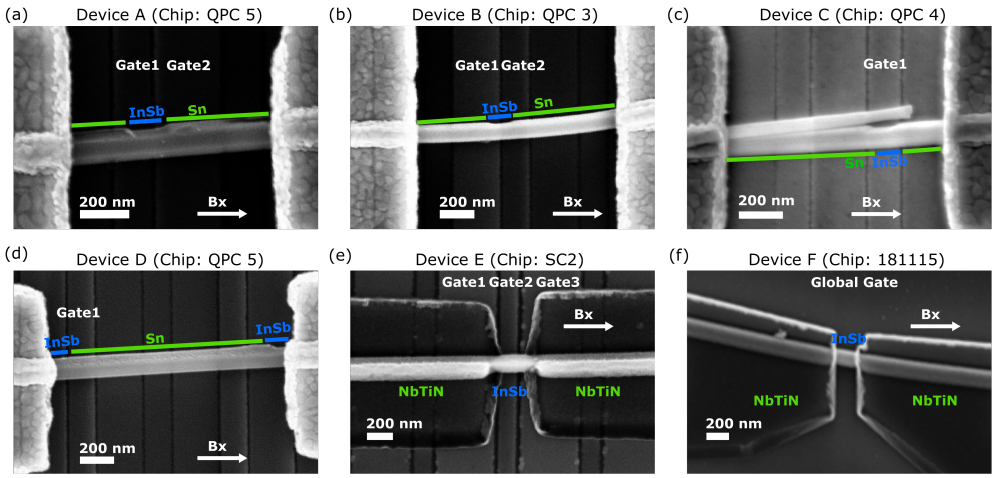

Figure 5.6: Scanning electron microscope (SEM) images of devices measured in reports, listed as Device name and (Chip name). Sn-InSb devices: (a) Device A (QPC5). (b) Device B (QPC3). (c) Device C (QPC4). (d) Device D (QPC5). NbTiN-InSb devices: (e) Device E (SC2). (f) Device F (181115). The direction of applied magnetic field B_x is indicated with white arrows.

voltage measurement model, with multiple filtering stages placed at different temperatures. Series resistance from the filter and the measurement model in V_{source}-$I_{measure}$ scan is R_{in} = 7.04 kΩ. In I_{source}-$V_{measure}$ scan, R_{in} = 4.04 kΩ.

NbTiN-InSb devices In Device E (SC2), InSb nanowires are transferred onto a Si chip with predefined local bottom gates(Fig. 5.6 (e)). The chip shares the same geometry as those used for Sn-InSb devices. Device F (181115) is fabricated using highly-doped Si chips that employ the entire substrate as global bottom gates(Fig. 5.6 (f)). The global gate chip is covered by a 285nm SiOx dielectric layer.

After transferring the nanowires, the entire chip is coated with PMMA 950 A4 electron beam resist and baked for 15 minutes at 175 °C to dry out the resist. The superconducting contacts are defined by EBL. Following development, a sulfur passivation technique is used to remove the oxide layer from InSb nanowires [31]. In the film deposition sputtering system, a smooth in-situ ion mill with argon plasma is utilized to eliminate sulfur and resist residue for 10 seconds at 15 W, after which 10 nm/140 nm NbTi/NbTiN is deposited onto the chips. Unwanted patterns are removed by soaking in acetone overnight and performing lift-off with a pipette to blow away the resist.

According to the SEM images, the length of the JJs in Device E and F are approximately 200 nm. The junction width is consistent with the nanowire width, and is similar to the Sn-InSb devices.

5.7.2 Full data in Device A

5.7.2.1 Evidence of Quantum Point Contacts

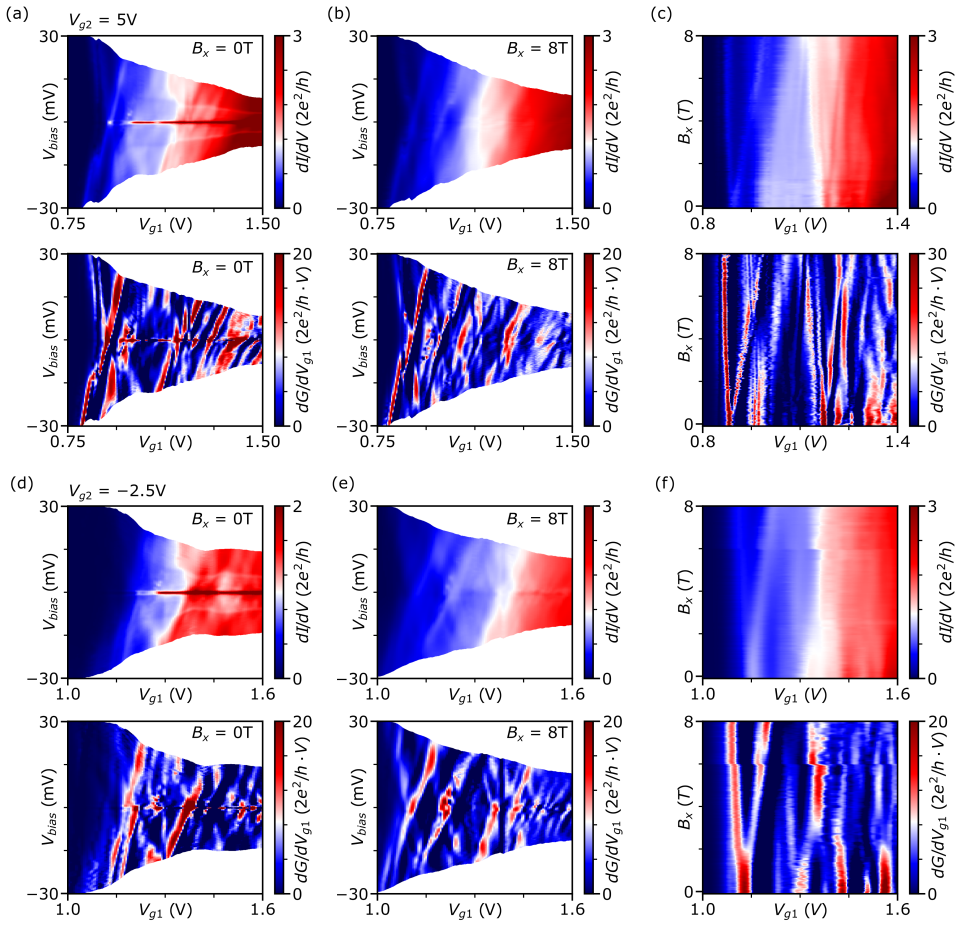

Figure 5.7: (a) Upper: Differential conductance $G = dI/dV_{bias}$ as a function of junction gate voltage V_{g1} and voltage across the device V_{bias} measured at lead gate voltage $V_{g2} = 5$ V and external field $B_x = 0$ T, a series resistance $R_{in} = 8.7$k Ω is used to calculate the conductance and extract from $Vbias$ while plotting. Lower: Transconductance dG/dV_{g1} as function of V_{g1} and V_{bias} plotted with same data to show the boundary of conductance plateau. (b) Similar as (a) but external field $B_x = 8$ T. (c) Upper: G as a function of V_{g1} and B_x. Lower: Full data of Fig. 5.3(a), transconductance dG/dV_{g1} as function of V_{g1} and B_x. (d)-(f) similar as (a)-(c) but the lead gate voltage V_{g2} = -2.5 V.

The devices initially undergo characterization by sweeping the gate voltages (V_g) at a fixed voltage bias across the device (V_{bias}), while concurrently measuring the current (I) passing through the device as a function of V_g. The series resistance R_s, used for calculating the differential conductance, comprises two components: R_in from various filtering stages (refer to Sec. 5.7.1), and $R_contact$ at the Au-Sn and Sn-InSb interface. The magnitude of R_s is derived from the I-V_g trace, where R_s equals V_{bias} (10mV) divided by I_{max}. When the current no longer increases with rising gate voltage, it implies that all conduction channels in the nanowire junction are fully open, signifying device saturation. At this point, only the series resistance acts as a transport barrier.

Evidence of quantum point contacts (QPC) construction within our nanowire Josephson junction is demonstrated by plotting the differential conductance G (dI/dV) against the voltage across the device (V_{bias}) and the junction gate voltage (V_{g1}), with an external field B_x = 0 T/8 T and lead gate voltage V_{g2} = 5 V (see Fig. 5.7 (a) and (b)). We used a series resistance R_s = 8.7 kΩ to calculate the differential conductance, subtracting its voltage drop contribution from V_{bias} during plotting. Comparison reveals a diamond-shaped region with quantized conductance in units of $2e^2/h$ ($1G_0$) at 0 T, alongside an extra region with conductance corresponding to $1e^2/h$ ($0.5G_0$) at 8 T and a smaller G_0 region. Transconductance dG/dV_{g1} over the junction gate voltage marks each quantized conductance region's boundary with red lines.

Fig. 5.7(c) illustrates a scan of G as a function of B_x and V_{g1} at a fixed voltage bias V_{bias} = 2 mV. Here, we observe the emergence of a spin-polarized regime ($G = 0.5G_0$) due to Zeeman splitting. To account for the Josephson current at zero voltage bias and Andreev states at a voltage bias smaller than 2Δ potentially resulting in higher conductance than the normal state conductance corresponding to the conduction mode, V_{bias} is set higher than 2Δ, where Δ is the gap of Tin (approximated as 650 μeV). A segment of the transconductance region from the Zeeman effect scan is used in Fig. 5.3 in the main text to differentiate between the spin-degenerate and spin-polarized regions.

In Fig. 5.7 (d) to (f), we replicate the same scans as in panel (a) to (c), but with a different lead gate voltage setting V_{g2} = -2.5 V. We discovered that the lead gate voltage value does not influence the presence of the quantized conductance region and the Zeeman

effect. In Fig. 5.8, we present additional conductance plots at varying lead gate voltages, thus demonstrating that the QPC in the junction region remains unaffected by changes in the lead gate voltage V_{g2}. This finding highlights the stability of our constructed QPCs within the nanowire Josephson junctions, regardless of variations in lead voltage settings.

5.7.3 Gate dependence of Conductance

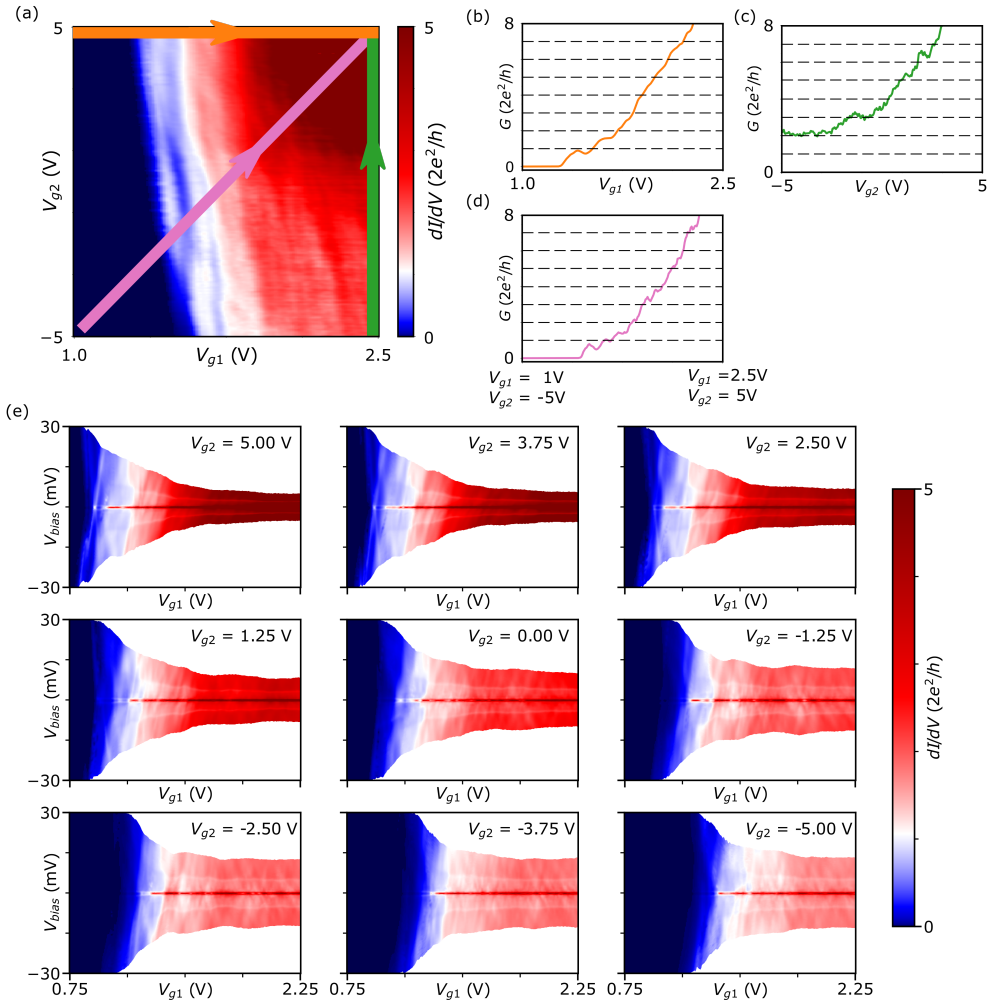

Figure 5.8: (a) Differential conductance dI/dV as a function of junction gate V_{g1} and contact gate V_{g2}, measured with fixed voltage bias $V_{bias} = 2$mV and external field $B_x = 0$T. (b)-(d) Three line cuts taken from (a): (b) Conductance as a function of V_{g1} at $V_{g2} = 5$V. (c) Conductance as a function of V_{g2} at $V_{g1} = 2.5$V. (d) Conductance as a function of V_{g1} and V_{g2} when both gates are varying. (e) G as a function of V_{g1} and V_{bias} at $B_x = 0$T and a series of different V_{g2}.

In Fig. 5.8, we explore the gate dependence in Device A. According to Fig. 5.8 (a), the lead gate voltage V_{g2} exhibits a relatively minor effect in modulating the conduction channels

and cannot independently close the nanowires within the measurable range of -5 V to 5 V. However, the gate voltage range of V_{g1}, where only a single mode is available in the junction, is still influenced by the lead gate V_{g2}. This aspect is taken into account when analyzing the impact of the orbital and Zeeman effects on the supercurrent across different modes.

In Fig. 5.8 (e), we present a conductance scan as a function of V_{bias} and V_{g1} at varying lead gate voltages V_{g2}, but with a fixed external field $B_x = 0$ T. We observe distinct diamond-shaped conductance plateaus across all V_{g2} values. This serves as evidence that the lead gate does not disrupt the ballistic transport and electron confinement within the nanowire junction region.

5.7.4 Extended Normalized switching current map

The effects of junction gate voltage on superconductivity in the presence of an external field are discussed in Fig. 5.4 and explored via simulations that consider both the chemical potential in the junction and the lead regions. These simulations are depicted in Fig. 5.5 in the main text. We conclude that the orbital effect is the primary factor leading to the suppression of the Josephson current, and the chemical potential under the leads also influences superconductivity, even when the conduction channels in the nanowires remain the same. Here, we present extended data to further substantiate our interpretation.

In Fig. 5.9 (a), we provide several raw data sets from gate scans of the Josephson current at various external field strengths. The deep blue represents the zero resistance state when a current bias is applied across the device. We observe that the switching current I_{sw} at higher gate voltages decays more rapidly compared to the I_{sw} at lower gate voltages. The I_{sw} at different gate voltages does not maintain a consistent magnitude at high fields, illustrating that the supercurrent is continuously tunable by the gate voltage. This suggests that it is not contributed by a continuous shell but by the nanowire junction. These types of gate scans are the source of all I_{sw} maps presented in this paper. We extract the magnitude of I_{sw} and plot them as functions of B_x and V_g.

In Fig. 5.9 (a), we present diffraction pattern of first mode supercurrent when the contact gate voltage V_{g2} is fixed at 5 V to have totally six full transverse mode occupied in the

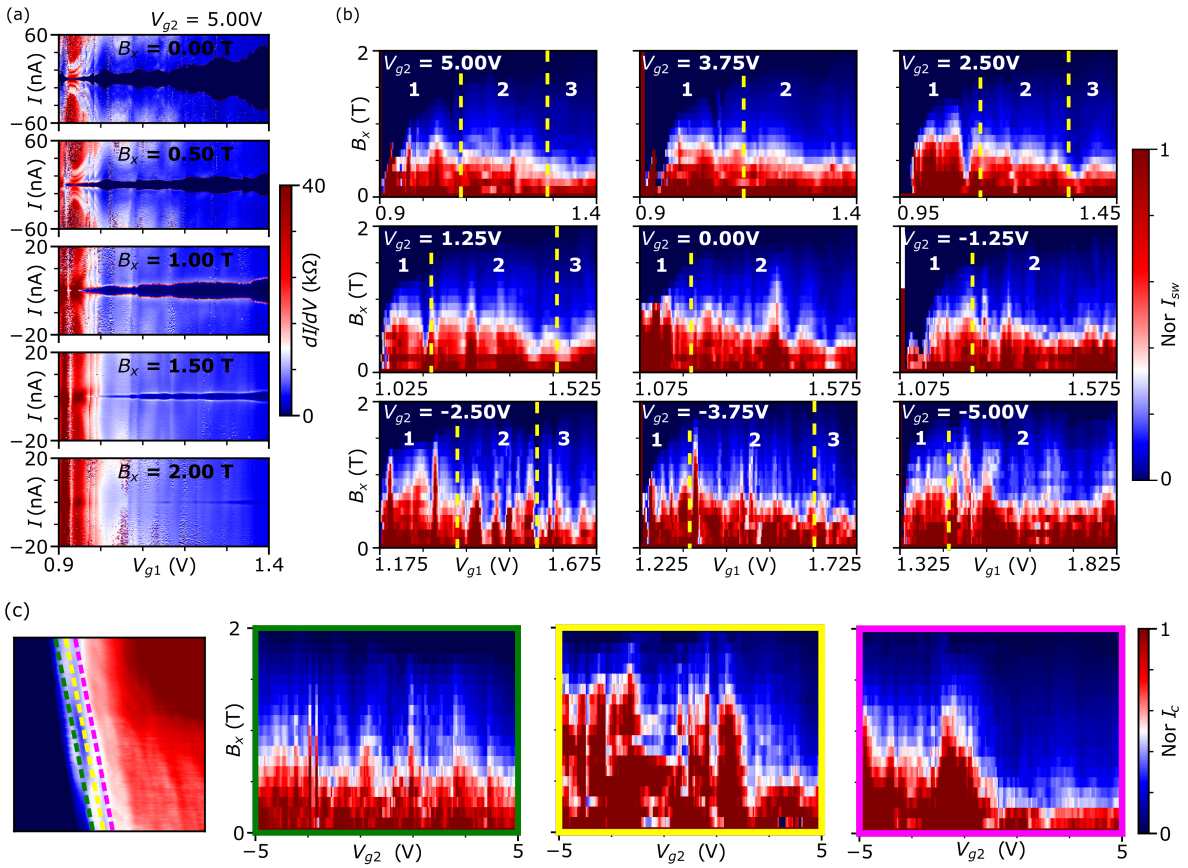

Figure 5.9: (a) Gate scan of supercurrent at a series of external B_x, the lead gate voltage V_{g2} is 5 V. (b) Normalized I_{sw} as a function of junction gate V_{g1} and external field B_x, the voltage applied to V_{g2} is labeled in each panel. The boundary between how many modes are occupied in the junction region is indicated with yellow dashed line and the number of conduction channels is labeled with white numbers. The number of occupied modes is derived from Fig. 5.7. (c) Normalized I_{sw} map as a function of B_x while both gate voltages V_{g1} and V_{g2} are varying to along three dashed line in the gate versus gate scan adapted from Fig. 5.8 (a) to stay in the first mode. The color of the square box is corresponding to the voltage tuning trace dashed line.

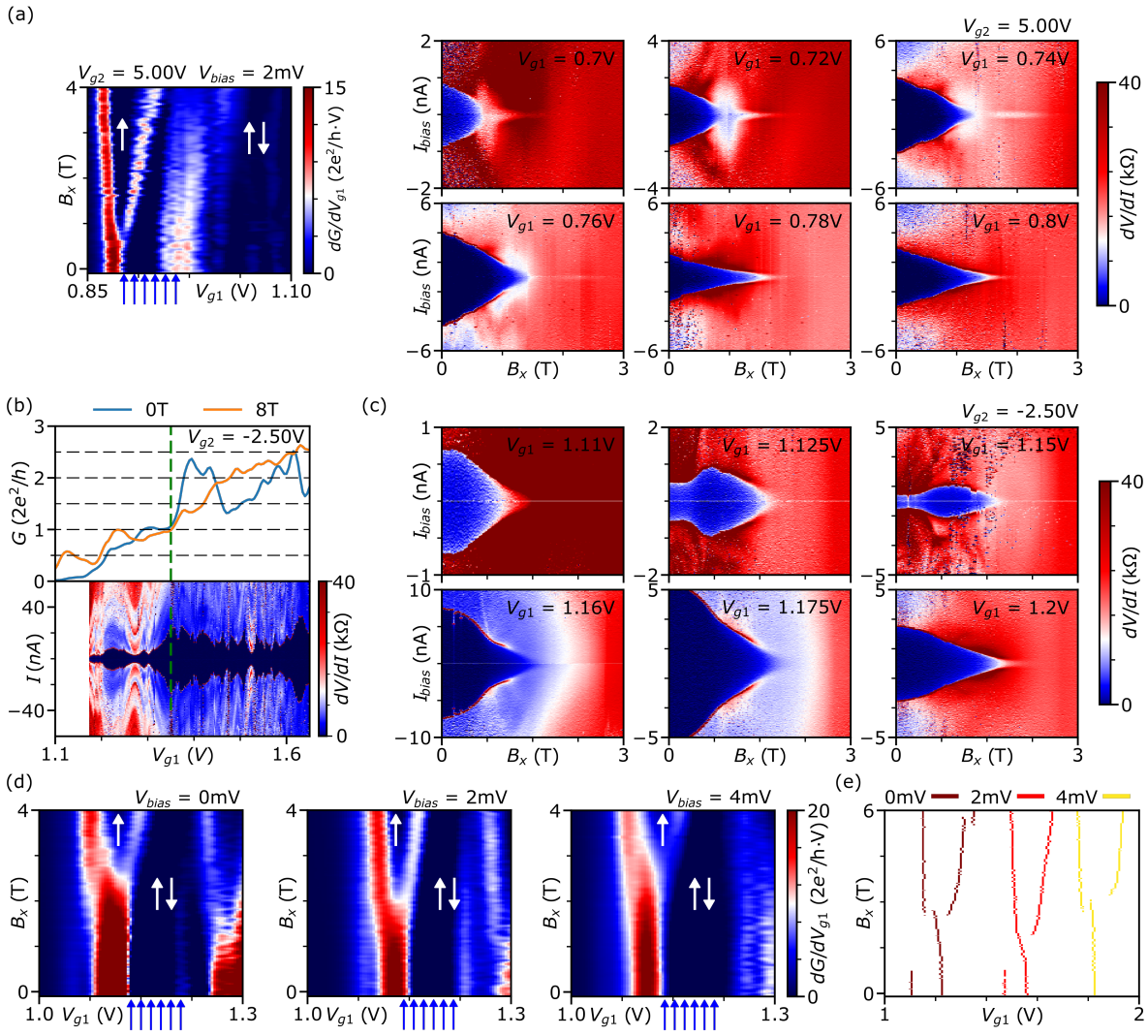

Figure 5.10: (a) Differential resistance $R = dV/dI$ as a function of current bias and external parallel field B_x. (b) Gate dependence of conductance and critical current plotted side by side to identify where the first mode supercurrent is. (c) Same as (a) but the contact gate voltage is fixed at V_{g2} = -2.5 V (d) Transconductance as function of B_x and junction gate voltage V_{g1} at fixed V_{g2} = -2.5 V, taken at different voltage V_{bias}. Blue arrows are used to illustrated where diffraction pattern are taken. (e) Extracted boundary between spin-polarized and spin-degeneracy region from (d), plotted with offset equals to 0.3 mV for each V_{bias}.

contact region. The junction gate V_{g1} varies for each panel but are all in the voltage range corresponding to the first mode. A transconductance plot is used to illustrate where the diffraction pattern is taken with blue arrows, with the indicated V_{g1} all shifted +0.2 V due to gate dopping over measurements.

In Fig. 5.9 (b), we present extended I_{sw} maps at various lead gate voltages V_{g2}. The conductance trace is extracted from Fig. 5.7 (d) and (e) by taking line cut at $V_{bias} = 2$ V at $B_x = 0$ T plot and $V_{bias} = 0$ V at $B_x = 8$ T plot. Similar to Fig. 5.2 in main text but the V_{g2} = -2.5 V. to have three full transverse mode occupied in the contact region. The number of conduction channels, modulated by the junction gate V_{g1}, is marked in each plot. From this panel, we observe electron spin-polarization suppression across most V_{g2} values, akin to Fig. 5.3. For those not exhibiting suppression, we attribute this to the range of V_{g1} being insufficient to encompass the entire first mode supercurrent. By comparing these plots, we note that the decay rate of I_{sw} is relatively slower when V_{g2} is smaller, aligning with the simulation results in Fig. 5.5 in the main text. These simulations demonstrate that a larger chemical potential in the lead region can induce a faster decay of I_{sw} when the junction mode is fixed at one.

In Fig. 5.9 (c), we studied lead gate voltage effect by varying V_{g1} and V_{g2} together, keeping the junction in the first mode, to observe how different lead gate voltages affect the transport of the Josephson current. We conducted three scans following three dashed line traces, all maintaining a global electron mode equal to one. The panels in the yellow and pink boxes align with our interpretation that a higher gate voltage results in stronger suppression of I_{sw} in the presence of an external field. However, the panel in the green box did not exhibit such results. As per Fig. 5.8 (a), we observe that the conductance region corresponding to the first mode is not smooth and flat. This can be attributed to the nanowires not being purely ballistic, and the potential for a quantum dot to be driven by the gate, thereby inducing varying scatterings. Consequently, the I_{sw} map might reflect superconducting behavior in a quantum dot regime rather than the first mode regime.

5.7.5 Diffraction pattern of first mode supercurrent

In Fig.5.10, we present the diffraction pattern of the first mode supercurrent current in a parallel magnetic field. Fig. 5.10(a) shows measurements taken at $V_{g2} = 5$ V across various V_{g1} values. On the right side of panel (a), we have displayed the transconductance again (adapted from Fig. 5.3 and Fig. 5.7) to highlight where the diffraction pattern is taken. The local bottom gate V_{g1} shifts over time, which we attribute to the doping of the dielectric layer during the measurements. At the time the diffraction pattern was taken, the gate voltage corresponding to the first mode supercurrent ranged from 0.7 to 0.9 V, whereas during the conductance plot acquisition, it ranged from 0.9 to 1.1 V. Therefore, we conclude the gate shifts approximately 0.2 V during the measurements.

Comparing the boundaries between the spin-polarized and spin-degenerate regions in the transconductance plot and the diffraction pattern, we observe that although the decay rate of I_{sw} doesn't have a significant difference, the superconductivity does disappear more rapidly at relatively smaller gate voltages. This can be attributed to the suppression from the polarization of electron, which is better elucidated in Fig. 5.3. We note a dip in the differential resistance beyond the critical field at $V_{g1} = 0.74$ V, which we currently do not have a clear interpretation for.

Fig. 5.10(b) is similar to Fig. 5.2 in the main text but at a different gate voltage, $V_{g2} =$ -2.5 V. We concurrently plot the gate dependence of the differential conductance and the switching current, using the magnitude of G as a guide to pinpoint the gate range where the supercurrent flows through a single conduction channel. In Fig. 5.10(c), we display several diffraction patterns of I_{sw} at various V_{g1} values at a fixed $V_{g2} =$ -2.5 V. These diffraction patterns were measured immediately after the conductance scan, so no shift of gate voltage was observed.

We measured the transconductance as a function of B_x and V_{g1} at $V_{g2} =$ -2.5 V at several different voltage biases V_{bias}. We acknowledge that the Zeeman scan cannot provide an accurate boundary between the spin-polarized and degenerate regimes as the charging energy from V_{bias} also plays a role. Nevertheless, we found that the scans we took were not comprehensive enough to rule out the effect from V_{bias} and to accurately define the voltage

range where the supercurrent reaches the spin-triplet regime.

5.7.6 Measurement results in Device B

5.7.6.1 Gate dependence

Device B, is fabricated on chip QPC3, exhibits both junction gate V_{g1} and lead gate V_{g2} as effective controls of the conduction channels in the nanowires (Fig. 5.11 (a) - (d)). However, both gates need to be lower than the safe voltage range (-5 V to 5 V) to fully pinch-off the junction, potentially leading to over-doping of the dielectric layer and leakage between the gate and the junction. Consequently, Device B's gate continually shifted during the measurements, making it difficult to pinpoint a region corresponding to a single or few-mode regime. Hence, this device is not using for studying electron transport in specific electron modes.

In Fig. 5.11(e) to (g), we present 2D scans of the differential conductance G at zero external field as a function of both gates, only V_{g1}, and only V_{g2}. A series resistance R_{in} = 7.1 kΩ is subtracted from $Vbias$ in the plot. We observe that the gate voltage region corresponding to the first mode while varying both local bottom gates V_{g1+g2} is shifted compared to panels (a) and (d). However, the conductance region remains quantized in units of $1G_0$. In panel (h), we scan conductance as a function of V_{bias} and V_{g1+g2} at a parallel field B_x = 4 T, but we do not observe a clear diamond-shaped conductance plateau with a magnitude of $0.5G_0$. In panel (i), we fail to detect the Zeeman split and emergence of a half-integer plateau corresponding to the spin-polarized regime. In panel (j), we note a slight shift in gate dependence of conductance from panel (a), but no evidence of a spin-polarized state is found.

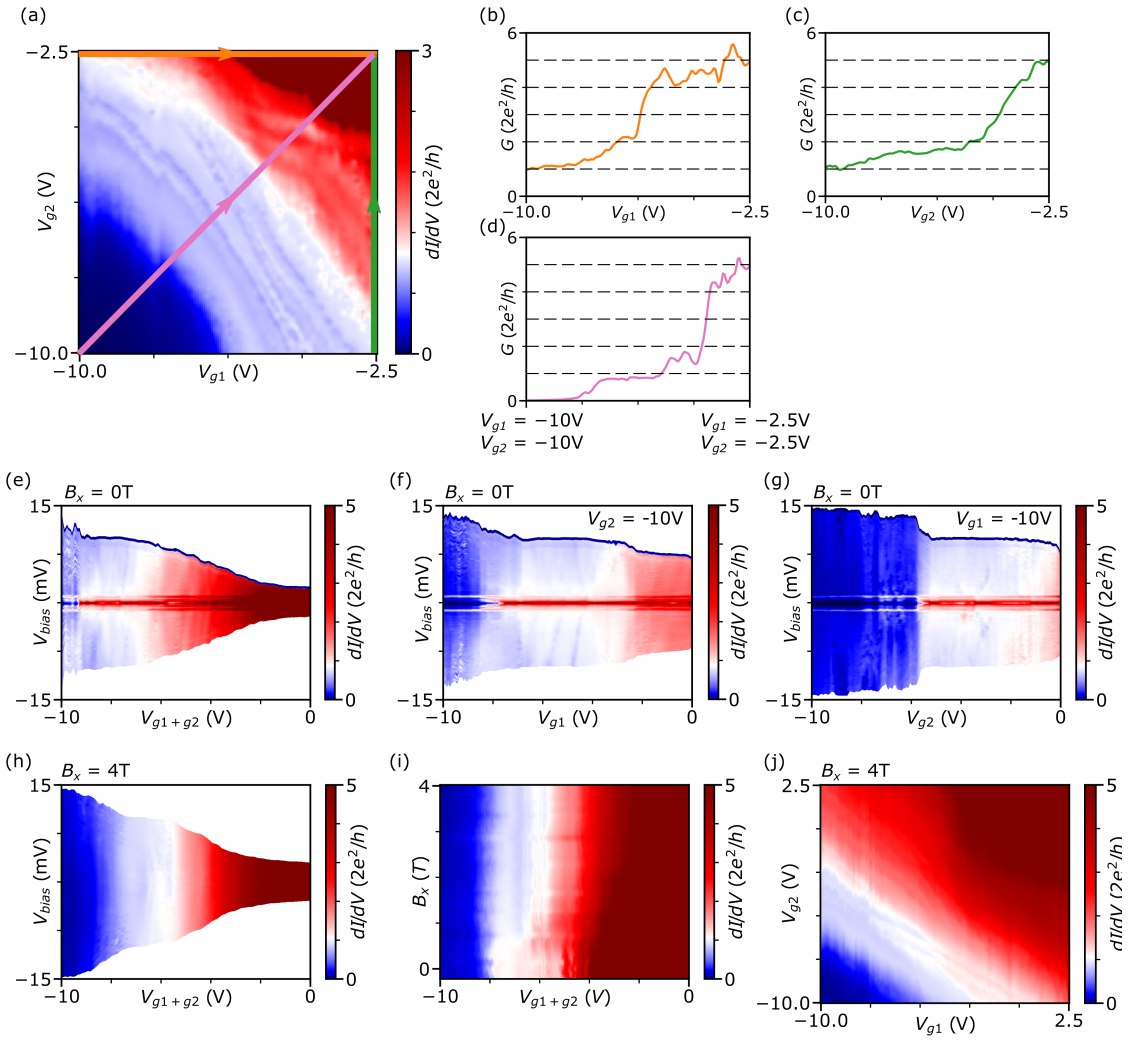

Figure 5.11: (a) Differential conductance $G = dI/dV$ as a function of junction gate V_{g1} and contact gate V_{g2}, measured with fixed voltage bias $V_{bias} = 2$mV and external field $B_x = 0$T. (b)-(d) Three line cuts taken from (a). (e) G as a function of $V_{g1} + V_{g2}$ (Varying both gates with same voltage) and V_{bias}. (f)/(g) G as a function of V_{g1}/V_{g2} and V_{bias} at fixed V_{g2}/V_{g1} = -10 V. (h) Similar to (e) but at fixed parallel field $B_x = 4$ T. (i) G as function of parallel field B_x and $V_{g1} + V_{g2}$, measured at $V_{bias} = 2$ mV. (j)Similar to (a) but at $B_x = 4$T.

5.7.7 Diffraction pattern of switching current

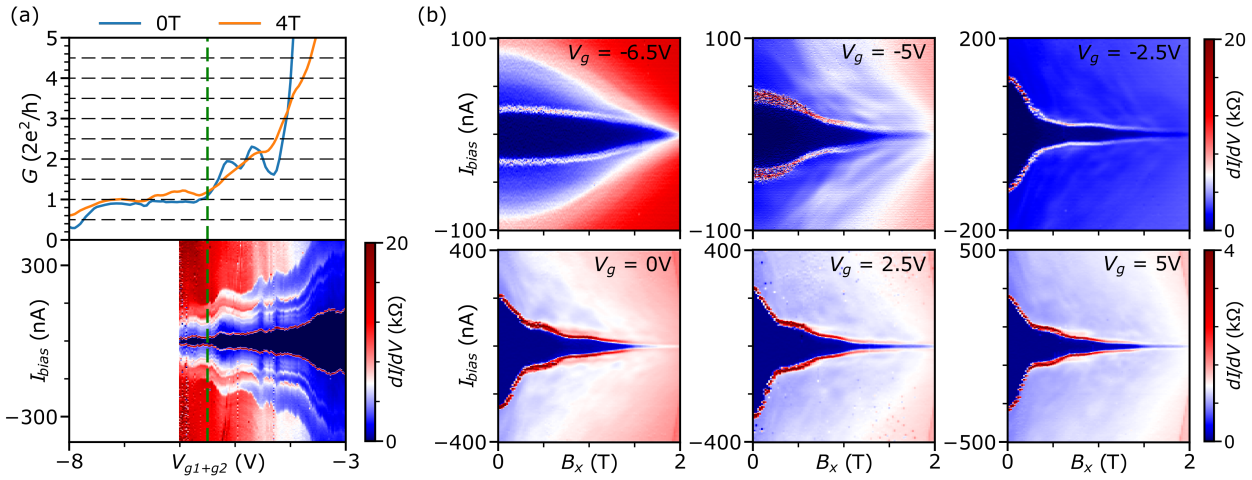

Figure 5.12: (a) Gate dependence of conductance and switching current plotted side by side. The conductance trace is extracted from Fig. 5.11 (e) and (h) by taking the line cut at $V_{bias} = 2$ mV at $B_x = 0$ T and $V_{bias} = 0$ mV at $B_x = 4$ T. The boundary between first mode and higher modes is labeled with green dashed line. (b) Diffraction pattern of supercurrent in parallel field B_x at different fixed gate voltage V_g (V_{g1+g2}).

In Fig. 5.12 (a), we present side-by-side plots of conductance and switching current I_{sw} as functions of gate voltage, which allow us to identify the gate voltage range where only the first mode supercurrent is transported through the junction. In panel (b), we display supercurrent diffraction patterns at various fixed gate voltages, where V_g represents all gates tuned together to the same value, identical to V_{g1+g2}. When V_g = -6.5V, the junction has only one conduction channel and one spin-full transverse mode available, and the supercurrent decays more slowly compared to larger gate voltages. However, we observe that the critical field at which superconductivity disappears remains the same across all gate voltage values.

5.7.8 Full measurement data of Device C

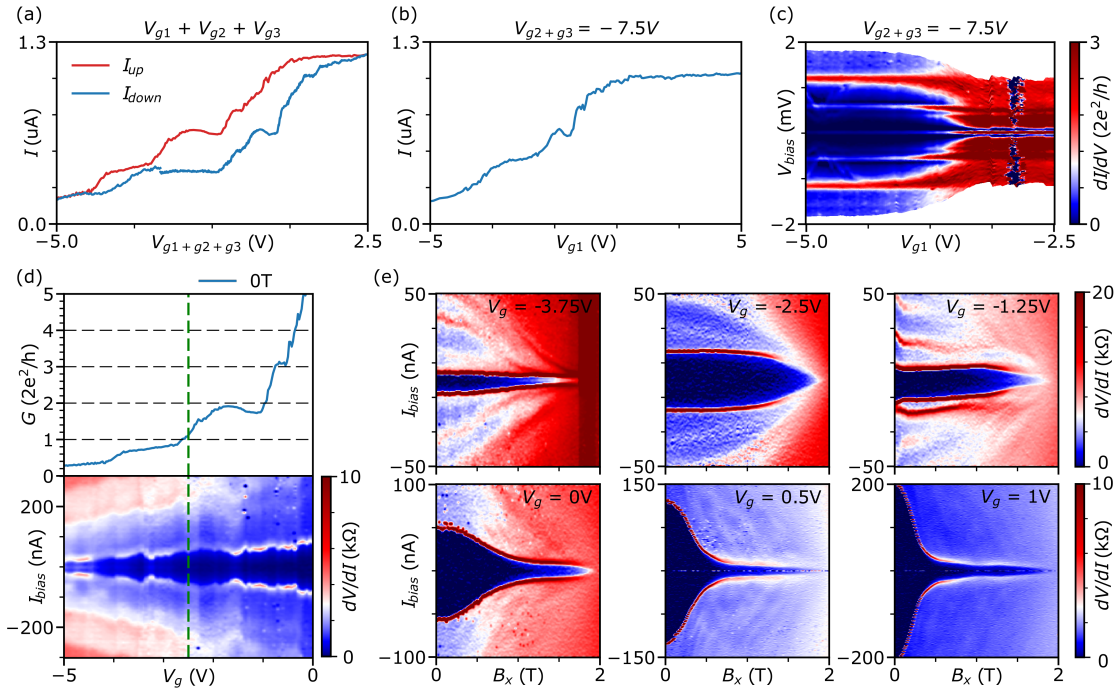

Figure 5.13: Full measurement Data in Device C. (a)-(b)Current through the device as a function of all gate voltage (a), V_{g1} that is under the junction region (b). (c) G as a function of V_{bias} and V_{g1} when other two gates V_{g2} and V_{g3} are set to be -7.5 V. (d) Gate dependence of conductance and switching current are plotted side by side. The conductance trace is converted from the red I-V_g trace in panel(a) with a sereis resistance $R_s = 7.1\text{k}\Omega$ is used in calculation. All three gate voltages are set to be the same value and labeled as V_g in panels. (e) Differential resistance as function of I_{bias} and B_x.

Similar to Device B, the tunnel junction in Device C cannot be fully closed by the local gates within the safe voltage range, and we observed more serious leakage when V_g falls below -5 V. Consequently, this device was not used for QPC studies, although we identified well-defined multiple Andreev states, indicating a lack of scattering in the system. As a result, we cannot confidently assert the exact number of modes at each gate voltage. However, estimations based on the pinch-off trace in Fig. 5.13 (a), combined with resistance measurements from the normal state in diffraction pattern plots, assist in determining the

number of transverse modes in Fig. 5.4(c) in the main text.

In Fig. 5.13 (d), we attempted to identify the gate voltage region associated with the first mode supercurrent. In Fig. 5.13 (e), we present several diffraction patterns of I_{sw} when a parallel field is applied. When V_g = -2.5 V, both conductance and normal state resistance indicate that only one transverse mode is available, and we observe a slower supercurrent compared to the higher gate voltage regime. These findings align with the I_{sw} map in the main text (Fig. 5.4) and the phenomena we observed in Device B.

5.7.9 Full measurement data of Device D

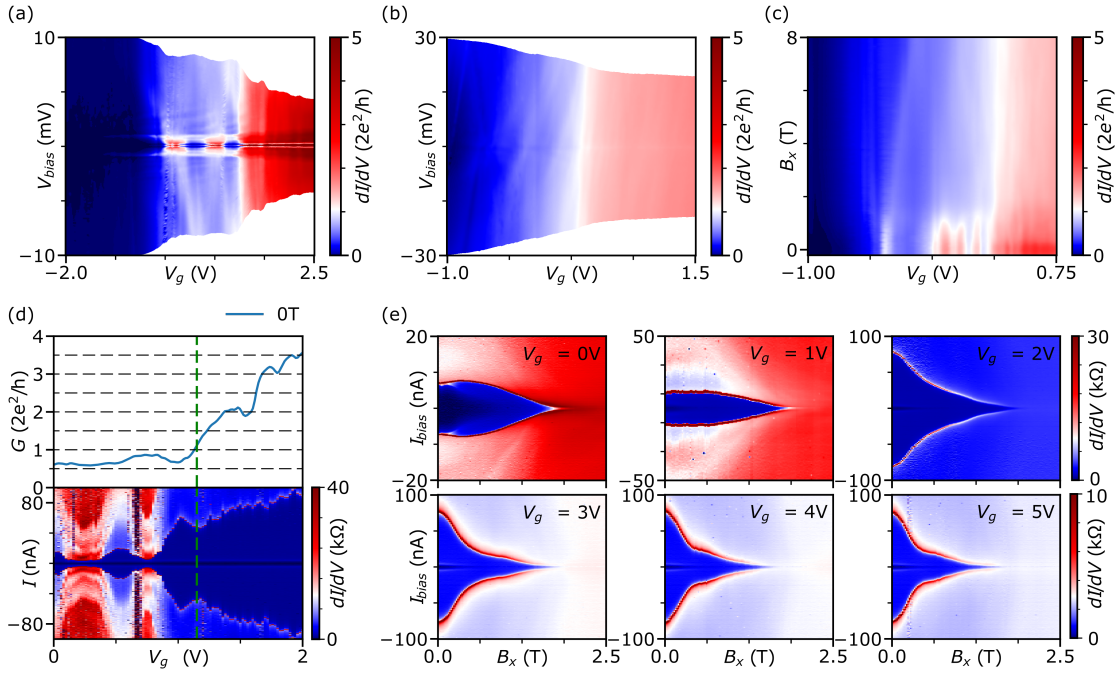

Figure 5.14: Full measurement Data in Device D. (a), (b) Differential conductance $G = dI/dV$ as a function of V_g and V_{bias} at external field $B_x = 0$ T and 8 T. A series resistance $R_{in} = 4.1$ kΩ is used to calculate the conductance and subtracted from the V_bias. (c) G as a function of of V_g and B_x, Voltage bias is set to be $V_{bias} = 0$ mV. (d) Gate dependence of conductance and switching current are plotted side by side. The conductance trace is extracted from the panel(a) by taking linecut at $V_{bias} = 2$ mV. (e) Differential resistance as function of I_{bias} and B_x. V_{g2} Varies to different values.

Device D only has one gate that can adjust the chemical potential in the nanowire junction and it looks like a N-S-N island device under SEM (see Fig. 5.6). Nevertheless, sharp transitions in the differential resistance 2D scan signify the presence of a switching current. At a parallel field $B_x = 0$ T, there is a conductance region with an almost quantized magnitude of $1G_0$ for gate voltages ranging from 0 to 1 V (Fig.5.14 (a)). At a parallel field $B_x = 8$T, an additional conductance region appears with a magnitude of $0.5G_0$(Fig. 5.14 (b)).

In Fig. 5.14 (c), we plot G as a function of V_g and B_x and observe a transition between a spin-degeneracy-only state and a spin-polarized regime, indicating a Zeeman split as evidence of a QPC. However, we detect two switching current peaks across all gate voltages, with the first transition being non-adjustable. Given the device's geometry seen in the SEM image, which more closely resembles an island device than a Josephson junction device, we have treated data from this device as supplementary material rather than incorporating it into the main text.

In Fig. 5.14 (e), we present several diffraction patterns of the switching current at different gate voltages when a parallel field is applied. At gate voltages $V_{g1} = 0$ V and 1 V, both the conductance and the normal state resistance indicate the presence of only one available transverse mode in the nanowire junction. Interestingly, we observe a slower I_{sw} decay compared to patterns taken at higher gate voltages.

5.7.10 Full measurement data of Device E (NbTin-InSb naowires)

5.7.10.1 QPC in Device E

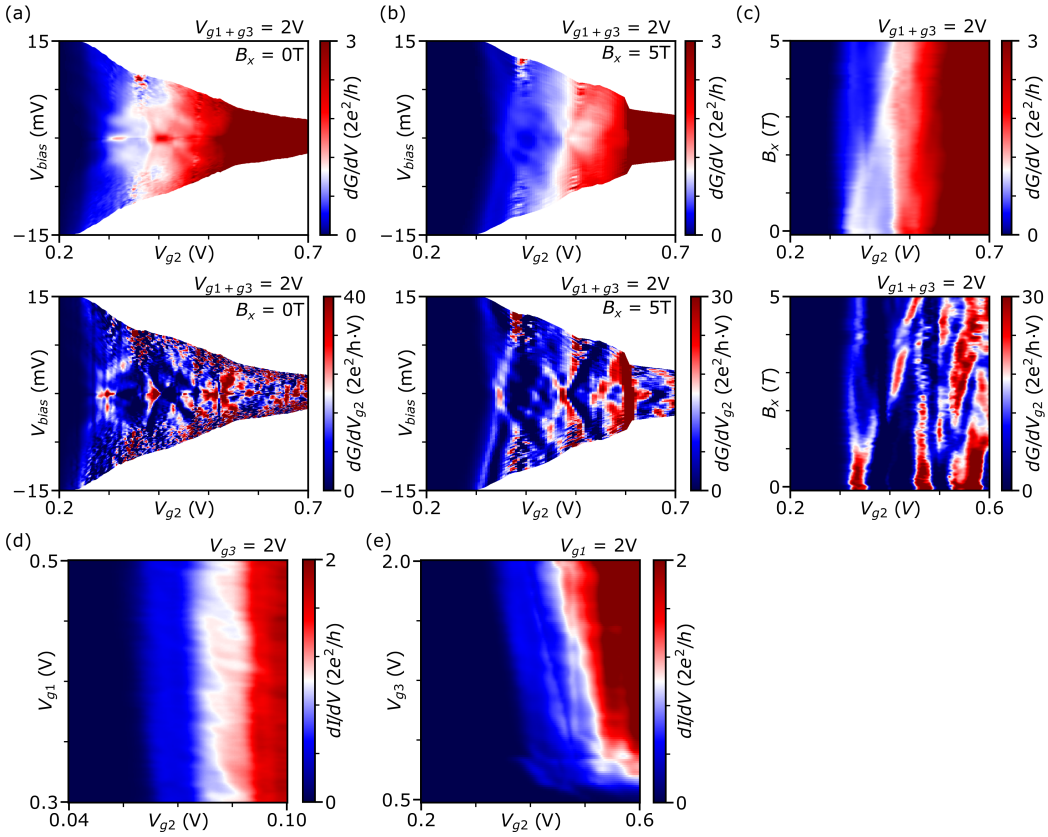

Figure 5.15: QPC and gate dependence in Device D. (a), (b)Upper: Differential conductance $G = dI/dV$ as a function of V_g and V_{bias} at external field $B_x = 0$ T and 5 T, contact gate voltages are set to be V_{g1} and $V_{g3} = 2$V. A series resistance $R_{in} = 6.5\text{k}\Omega$ is used to calculate the conductance and subtracted from the V_bias. Lower: Transconductance by taking dG/dV_{g2} from upper plot for the boundary of quantized conductance region. (c) Upper: G as a function of of V_{g2} and B_x, Voltage bias is set to be $V_{bias} = 2$ mV, V_{g1} and $V_{g3} = 2$V. Lower: Transconductance by taking dG/dV_{g2} from upper plot. (d) Left: Differential conductance dI/dV as a function of junction gate V_{g1} and contact gate V_{g2}, measured with fixed voltage bias $V_{bias} = 2\text{mV}$, $V_{g3} = 2$ V and external field $B_x = 4$ T. (e) G as a function of junction gate V_{g3} and contact gate V_{g2}, measured at $V_{g1} = 2$ V and $B_x = 4$ T.

Devices E and F were fabricated by ex-situ depositing an NbTiN film onto InSb nanowires to form superconducting leads. The NbTiN shell is not as smooth as that of Tin, but the bulk NbTiN has a significantly higher critical temperature and field compared to Tin or Aluminum. Device E was fabricated on a local bottom gate chip, which is why we have better control of the junction and are able to observe the QPC in this device, unlike in Device F.

Fig. 5.15 provides evidence of a QPC in Device E. Panel (a), taken at $B_x = 0$ T, reveals a diamond-shaped conductance region with a uniform magnitude of $1G_0$. Taking the derivative with respect to the gate voltage V_{g2} clearly demonstrates the boundaries of this quantized conductance region. In panel (b), the scan conducted at $B_x = 5$ T shows a diamond-shaped conductance region of roughly the same size as the plateau at 0 T, but with a conductance magnitude of $0.5G_0$, which indicates this is corresponding to the spin-polarized regime

In panel (c), we hold V_{bias} constant at 2 mV and plot G, observing the transition between the spin-degeneracy and spin-polarized regimes. Panels (d) and (e) explore the effects of the lead gate voltages V_{g1} and V_{g3}. We find that both contribute weaker effects compared to the junction gate voltage V_{g2}. Therefore, to avoid scattering from the quantum dot, they are both set to their highest positive value of 2 V.

5.7.11 Supercurrent in Device E

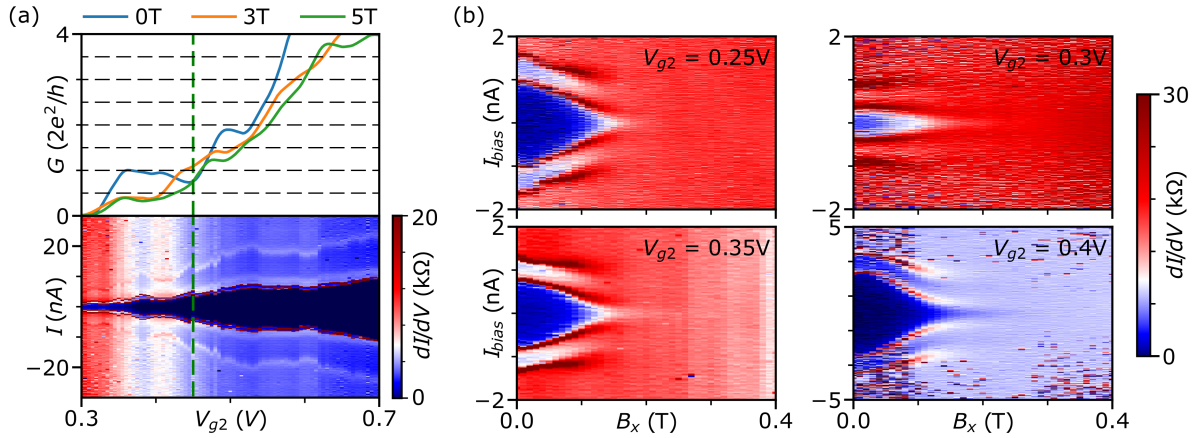

Figure 5.16: (a) Differential conductance $G(dI/dV)$ taken at normal state as functions of V_{g2} at 0 T/3 T/5 T and gate sweep of I_{sw} at 0T are plotted next to each other, extracted from Fig. 5.15 (c) by taking line cuts. Gate scan of supercurrent is plotted side by side.Green dashed line is used to indicate the boundary between first mode and more modes. (b) Differential resistance as function of I_{bias} and B_x. V_{g2} Varies to different values but in the voltage range that corresponding to first electron mode. Contact gates voltage are fixed to V_{g1} and $V_{g3} = 2$ V.

Fig.5.16 presents both gate and field scans of supercurrent in Device E. In panel (a) we study the gate range for first mode supercurrent. Here, we find that a gate voltage V_{g2} from 0.3 V to 0.45 V corresponds to the presence of only one conduction channel in the nanowire device with supercurrent transport through the junction.

In panel (b), we study diffraction patterns of supercurrent at several fixed gate voltages within the first mode range. We observe that although the supercurrent decays more slowly, it has a much smaller critical field compared to the nanowire junctions in Ref. [34] and Device F.

5.7.12 Full measurement data of Device F (NbTin-InSb naowires)

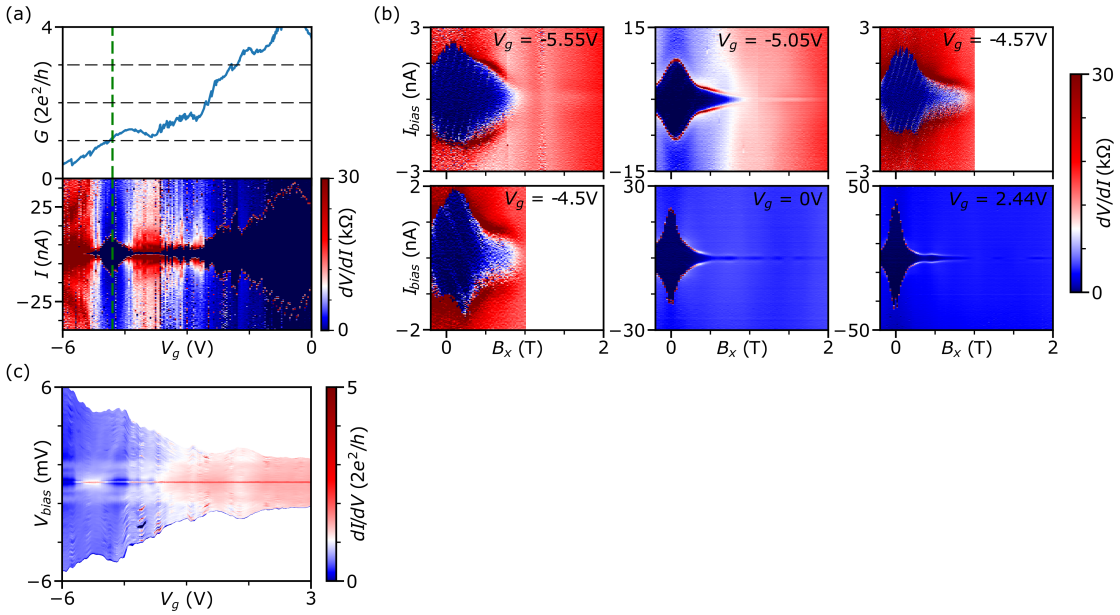

Figure 5.17: Full measurement Data in Device F. (a) Current through the device as a function of global gate voltage V_g. (b) Differential conductance $G = dI/dV$ as a function of V_g and V_{bias} at external field $B_x = 0$ T. A series resistance $R_{in} = 13.9\text{k}\Omega$ is used to calculate the conductance and subtracted from the V_{bias}. (c) Differential resistance as function of V_g and I_{bias} for the gate sweep of I_{sw} at 0T. (d) Differential resistance as function of I_{bias} and B_x. V_g Varies to different values in each panel.

Device F is the only device fabricated with a bottom global back-gate chip (see Fig. 5.6 (f)). The chemical potential across all regions of the devices is tuned simultaneously. As there is no conductance plateau quantized to $1G_0$ at zero parallel field (Fig. 5.17 (a) and (c)), we do not have a quantum point contact (QPC) for precise control over the number of electron transverse modes in the nanowires.

In panel (a), we identify the gate voltage range where both resistance and conductance indicate the presence of only one conduction channel in the nanowires and there is supercurrent within this range. Upon setting the gate voltage V_g to a value in this range, we observe that the supercurrent decays more slowly compared to the diffraction pattern mea-

sured at higher gate voltages. Additionally, an irregular disappearance and reappearance of supercurrent is observed at $V_g = 0$ V and 2.44 V, which is similar to the findings reported in Ref. [34].

5.7.13 Switching current Normal resistance product comparison between all devices

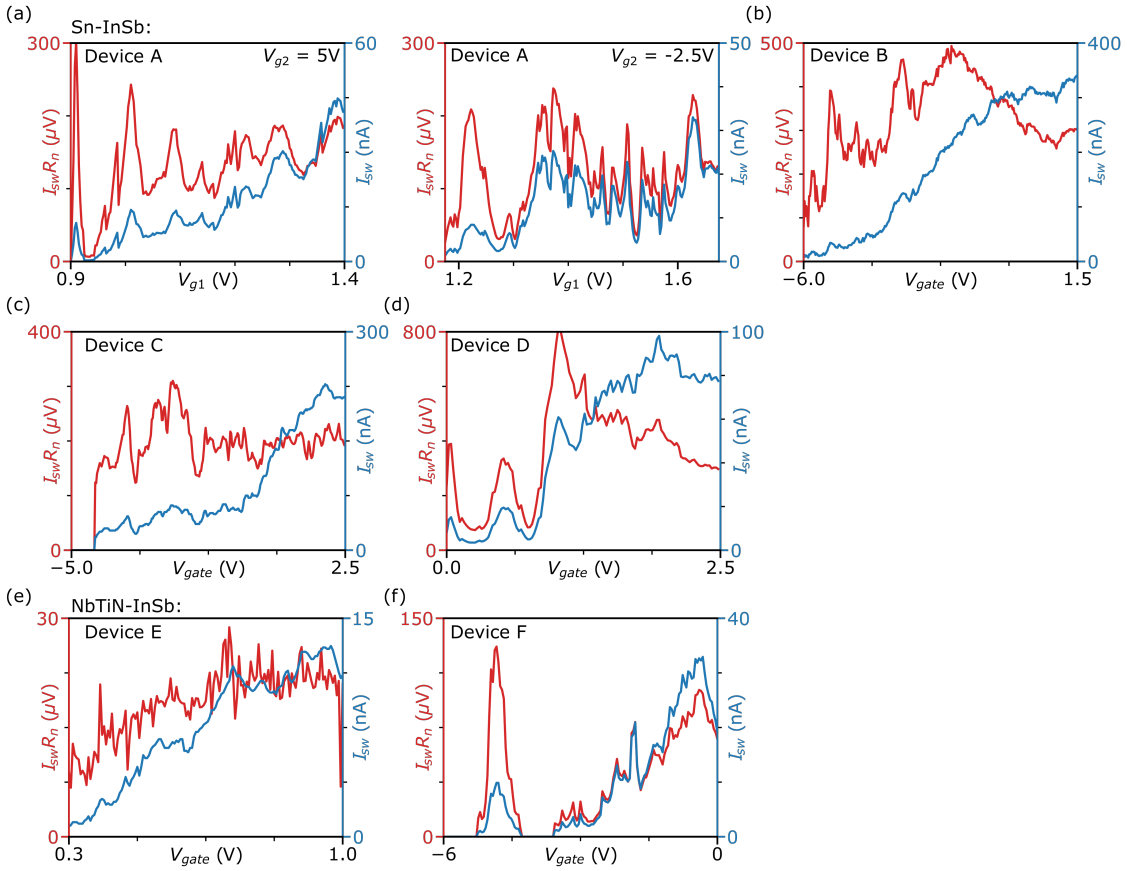

Figure 5.18: Critical current Normal state resistance product $I_{sw}R_N$ as a function of gate voltage measured in each devices. (a)-(f) Device A - F.

The strength of the Josephson effect in the nanowire junction, induced by the proximity effect, is quantified using the product of the switching current and normal state resistance, $I_{sw}R_n$, as shown in Fig. 5.18. In panel (a), we present the measurement results at two different lead gate voltages, $V_{g2} = 5$ V and -2.5 V. The normal state resistance is taken from the QPC scans in Fig. 5.7. The magnitude of the switching current I_{sw} is extracted from Fig. 5.2 (5 V) and Fig. 5.10(b) (-2.5 V) by tracking from the zero current bias and identifying the first point where the differential resistance exceeds 2 kΩ at positive and negative bias for each gate voltage. The plot reveals that at both lead gate voltages, the $I_{sw}R_N$ product

is smoothly vibrating around 200 μV, comparable to the energy gap of Tin ($\Delta \approx 650$ μeV).

The normal state resistance in panels (b), (c), and (d) is obtained from Fig. 5.11 (d), Fig. 5.13 (d), and Fig. 5.14 (a). The magnitude of supercurrent is read from Fig. 5.12(a), Fig. 5.13(d), and Fig. 5.14(d), respectively. Their $I_{sw}R_n$ products are larger than Device A, indicating a stronger Josephson effect in the junction, and all comparable to the energy gap of Tin.

Conversely, Devices E and F, fabricated with NbTiN and InSb nanowires, show a relatively smaller $I_{sw}R_n$ product and weaker Josephson effect in panels (e) and (f), despite NbTiN having a larger superconducting gap and higher critical temperature. In panel (e), we derive the normal state resistance from Fig. 5.15 (a) and the magnitude of I_{sw} from Fig. 5.16(a), the $I_{sw}R_n$ product approximates 20 μV. In panel (f), we extract both the R_n and I_{sw} from the conductance trace in Fig. 5.17 (a), the conductance trace is based on an I-V_g trace measured at a fixed $V_{bias} = 10$ mV and zero field. There is a high peak of $I_{sw}R_n$ around $V_g =$ -5 V, and the $I_{sw}R_n$ product is not stable, varying with the gate voltage. We believe this instability is due to the gate being unstable, shifting between the I-V_g measurement and the gate scan of I_{sw}. Nonetheless, the maximum magnitude of $I_{sw}R_n$ does not grow significantly, remaining considerably smaller than the energy gap of NbTiN ($\Delta >$ 3 meV).

In conclusion, upon examining the $I_{sw}R_n$ products, we find that the superconductivity induced by the thin Sn shell in InSb nanowires is much stronger than that in NbTiN-InSb devices. As we've stated in the main text, stronger induced superconductivity is crucial for achieving topological states, as it must counteract the suppression from the Zeeman effect and orbital effect in the presence of a field. In our case, Sn-InSb nanowires present a more robust and consistent magnitude of $I_{sw}R_n$ across the gate voltage range. Furthermore, the Josephson current is well adjusted by the gate, making it a superior platform for studying Majorana-related Josephson effects.

5.7.14 Simulation model

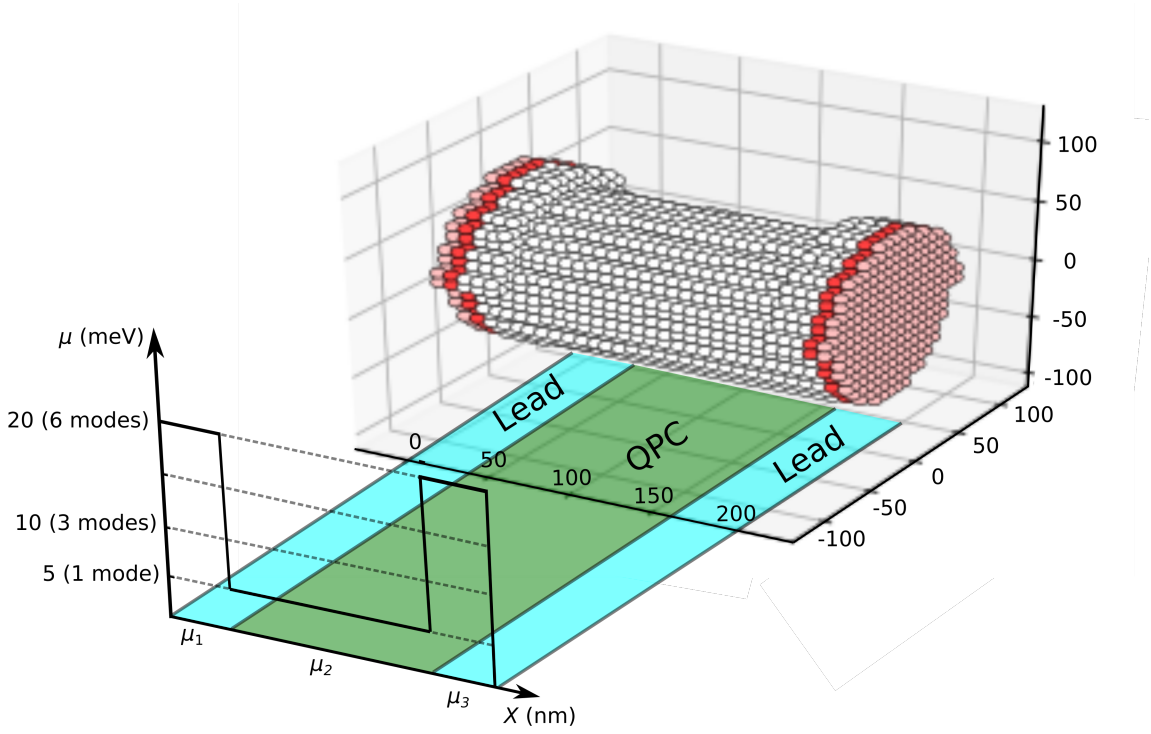

Figure 5.19: . Tight-binding model generated by the simulation. Red dots represent the infinite leads. Lattice constant is 8 nm. Shell is covering the nanowires to make contact with length of 24 nm at each end. Uncovered nanowires is 160 nm long. Three chemical potentials are defined locally at leads and junction regions. In this figure we are presenting the condition where we set $\mu_{leads} = 20$ meV for six spin-full transverse mode and $\mu_{QPC} = 5$ meV for one transverse mode.

To numerically simulate the superconductor-semiconductor-superconductor nanowires Josephson junction in the presence of external parallel magnetic field, we consider the following Hamiltonian for a nanowire that is covered by superconductor lead at both ends:

$$H = \left(\frac{\mathbf{p}^2}{2m^*} - \mu(x) + \delta U \right) \tau_z + \alpha(p_x\sigma_y - p_y\sigma_x)\tau_z + g\mu_B \mathbf{B}\cdot\hat{\sigma} + \Delta\tau_x, \tag{5.1}$$

where τ_i and σ_i are Pauli matrices act on particle-hole and spin space, respectively. $\mathbf{p} = -i\hbar\nabla + e\mathbf{A}\tau_z$ is the canonical momentum, and the magnetic potential $\mathbf{A}$ is chosen to

be $[B_y z - B_z y, 0, B_x y]^T$, so that it is invariant along the $x-$direction. Further, m^* is the effective mass, μ is the chemical potential and δU represent the onsite disorder inside the nanowires. The Zeeman effect is given by $g\mu_B \mathbf{B} \cdot \hat{\sigma}$ and the Rashba spin-orbit coupling is given by $\alpha(p_x\sigma_y - p_y\sigma_x)$. Finally, Δ is the superconducting pairing potential.

Chemical potential is defined locally, where we have:

$$\mu(x) = \begin{cases} \mu_1 & \text{if } 0 < \text{x} < l_{leads} \\ \mu_2 & \text{if } l_{leads} < \text{x} < l_{leads}+l_{junction} \\ \mu_3 & \text{if x} > l_{leads}+l_{junction} \end{cases} \tag{5.2}$$

The geometry of the simulation model is plotted in Fig. 5.19. In the simulation, we give same value to the μ_1 and μ_3 and call them lead chemical potential, μ_2 is the chemical potential of QPC. As this is a microscopic model, it facilitates the computation of electron hopping between neighboring sites. The process of deriving the critical current from the Hamiltonian is discussed in Ref.[35].

5.7.15 Parameter dependence of QPC

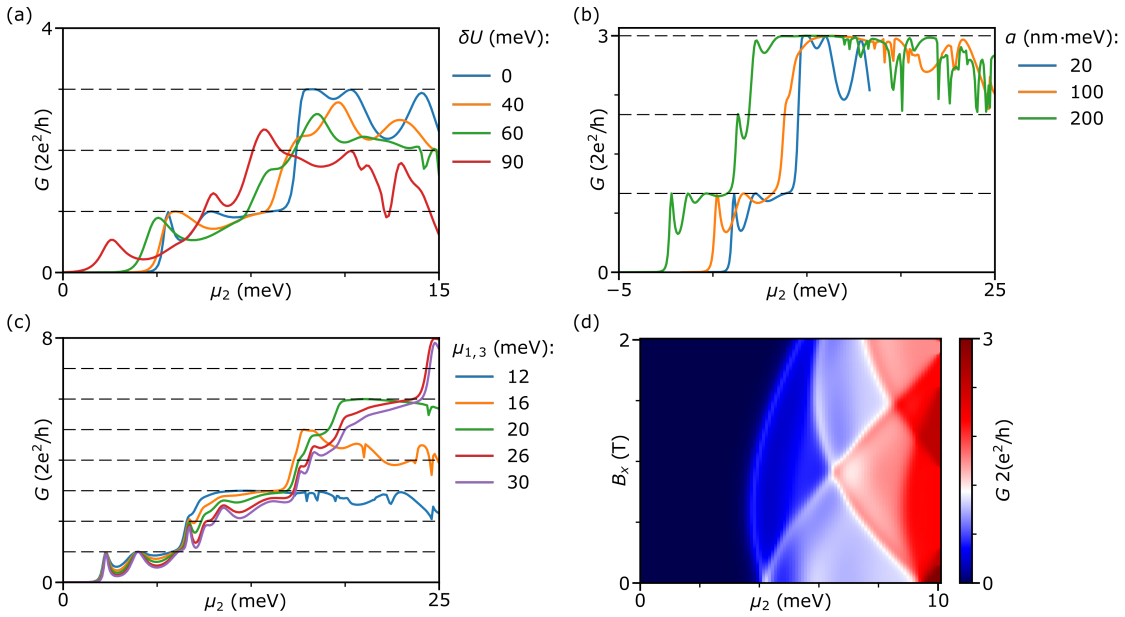

Figure 5.20: . Parameters dependence of constructing QPC in the simulation. (a) Disorder strength (δU) dependence. (b) Spin-orbit effect Strength (α) dependecne. (c) Lead chemical potential μ_{lead} dependence. In panel (a)-(c), if not studied for dependence, the parameters are set to be: $\mu_{1,3} = 10$ meV, $\alpha = 100$ nm $\cdot$ meV, temperature $T = 0.1$ T, disorder δU= 0 meV. (d) Full conductance scan as function of μ_2 and parallel field B_x presented in Fig. 5.3 (c) in the main text.

The parameters used in the simulation are analyzed from two perspectives: their impact on the construction of the Quantum Point Contact (QPC) and their influence on the supercurrent field evolution. This section primarily discusses the QPC dependency.

In Fig. 5.20(a), we investigate the effect of disorder on the QPC conductance dependence, while keeping all other parameters constant.

We focused on the first plateau, which corresponds to a single spin-full transverse mode with a magnitude of 2 e^2/h or $1G_0$. Our findings suggest that quantized first plateaus (in the unit of G_0) are only achievable when the disorder strength δU is less than 40 meV. An increase in disorder reduces the transmission rate between two leads, subsequently lowering

the magnitude of conductance G and introducing additional plateaus.

It's worth noting that our simulation lacks the plateaus of $2G_0$ and $4{,}5G - 0$, potentially due to the subband's degeneracy at zero field, as discussed in Ref. [70]. In our simulation, disorder is introduced by randomly mapping local defects into the junction, causing scattering during electron transportation. Ref. [34] determined the disorder parameter by calculating the corresponding mean free path l_{mfp} for different δU strengths. They selected δU = 90 meV, yielding l_{mfp} = 250 nm, which aligns closely with the mobility and mean free path characterized in InSb nanowires [59]. However, the QPC is highly influenced by disorder distribution. In our case, it suggests a junction that is nearly disorder-free in the junction region. Therefore, we selected $\delta U = 0$ meV for the spin-polarization studies in Fig. 5.3 in the main text to match the interpretation about 1st mode supercurrent in Ref. [34], and $\delta U = 40$ meV for discussion in Fig. 5.21, which satisfies both the real-world condition of quasi-ballistic nanowires and the simulation condition of having a quantized plateau.

Fig.5.20(b) discusses the effect of spin-orbit interaction strength on the QPC. We observe small difference in the conductance trace shape as a function of μ_2, but it shifts towards a more negative chemical potential side as α increases. In Ref. [35], we studied how α impacts the supercurrent diffraction pattern and determined that the magnitude of approximately 100 nm $\cdot$ meV is necessary to produce the skewed shape. As this research shares the same wires and chips as the current project, we conclude that α = 100 nm $\cdot$ meV should be continuously used for the project's simulation.

In Fig.5.20(c), we explore the influence of the lead chemical potential $\mu_{1,3}$ on the QPC and the number of transverse modes in the junction. When $\mu_{1,3}$ varies, the conductance trace is not shifted with respect to the QPC chemical potential μ_2, but it only affects the maximum mode occupied in the Josephson Junctions (JJs). We employ the same method to identify how the chemical potential controls the available modes in the junction and conclude that μ = 5, 10, 20meV correspond to 1, 2, 3 occupied modes, respectively.

Fig. 5.20(d) presents the Zeeman scan results from the simulation, incorporating parameters from the previous discussions. In this plot, we have a disorder of $\delta U = 0$ meV, a spin-orbit interaction strength of α = 100 nm $\cdot$ meV, and a lead chemical potential $\mu_{1,3}$ = 20 meV. We observe a quantized plateau of $1G_0$ at zero field, which splits into two

plateaus of $0.5G_0$ and $1G_0$ due to the Zeeman effect. By taking the derivative with respect to the chemical potential μ_2, we obtain the transconductance plot presented in the main text, Fig. 5.3(c).

5.7.16 Parameter dependence of supercurrent in simulation

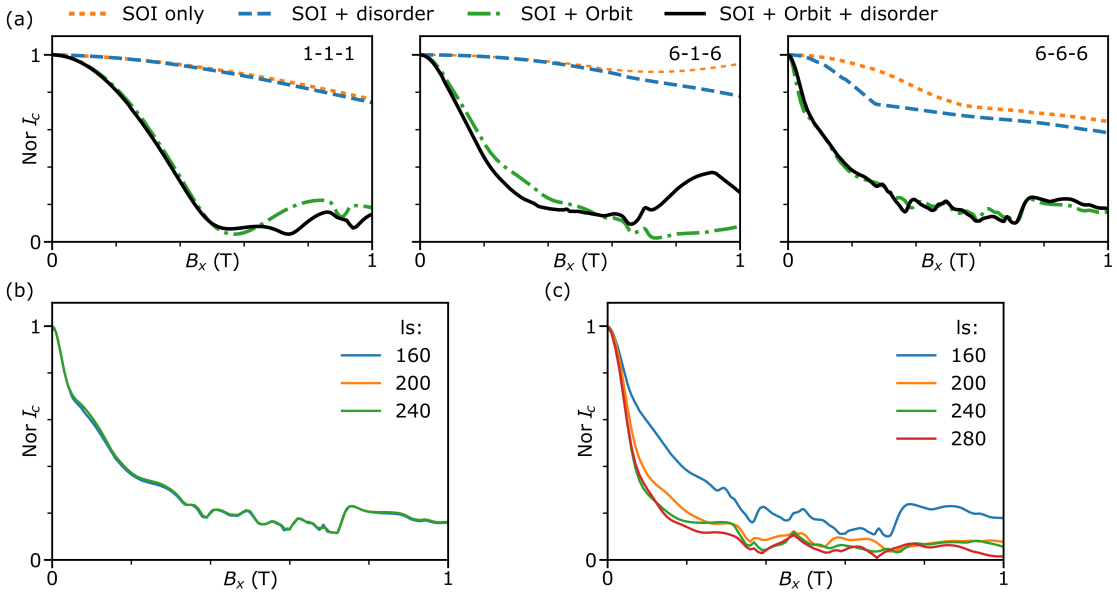

Figure 5.21: . Parameters dependence of switching current diffraction pattern in the simulation. (a) Normalized critical current as a function of parallel field B_x calculated with different parameter combination, the parameter space are same as Fig. 5.5 in the main text. The available modes in the lead/QPC/lead are labeled with number in each plot. (b) Junction length effect when there is no disorder distributed in the system ($\delta U = 0$). (c) Junction length effect when there disorder is distributed in the system ($\delta U = 40$ meV). In (b) and (c), all three local chemical potential are set to be 20 meV.

n Fig. 5.21, we study the impact of physical effects on supercurrent diffraction in the presence of an parallel field. Panel (a) displays the I_c pattern when different parameter combinations are included in the simulation. The results that take into account spin-orbit interaction (SOI), orbital effects, and disorder are used to plot Fig. 5.5 in the main text, as these closely resemble real-world measurements.

In Fig. 5.21(b) and (c), we investigate how the length of the junction influences Orbital and Interference effects when the junction is adjusted to a fully open regime ($\mu_1, \mu_2, \mu_3 =$ 20 meV, all corresponding to six spin-full transverse modes). In panel (b), we did not introduce local disorder (setting $\delta U = 0$) and found that the diffraction pattern of I_c remains consistent for all junction lengths l_s. Thus, we conclude that the orbital effect is not influenced by the junction length. In panel (c), we introduced site disorder $\delta U = 40$ meV and observed a faster decay of I_c with larger junction lengths. This supports our argument regarding the distribution of disorder: electron transport in a longer junction is likely to encounter more scattering due to an increased number of defects introduced into the system, resulting in stronger suppression when a parallel field is applied.

6.0 phi0-Josephson junction in Sn-InSb nanowires[1]

We study Josephson junctions based on InSb nanowires with Sn shells. We observe skewed critical current diffraction patterns: the maxima in forward and reverse current bias are at different magnetic flux, with a displacement of 20-40 mT. The skew is greatest when the external field is nearly perpendicular to the nanowire, in the substrate plane. This orientation suggests that spin-orbit interaction plays a role. We develop a phenomenological model and perform tight-binding calculations, both methods reproducing the essential features of the experiment. The effect modeled is the ϕ_0-Josephson junction with higher-order Josephson harmonics. The system is of interest for Majorana studies: the effects are either precursor to or concomitant with topological superconductivity. Current-phase relations that lack inversion symmetry can also be used to design quantum circuits with engineered nonlinearity.

6.1 Introduction

Interest in superconductor-semiconductor hybrid structures is along two directions. On the one hand, they are explored as materials for quantum technologies, such as superconducting qubits [103, 104]. On the other hand, they are a platform with high potential for the discovery of topological superconductivity [106].

In semiconductor nanowires, a combination of induced superconductivity, spin-orbit interaction and spin splitting can famously induce Majorana modes and topological superconductivity [15, 16]. The same ingredients can induce an anomalous Josephson effect, known as φ_0-junction [36]. The primary characteristic of a Josephson junction is the current phase relation (CPR) [9]. The most common CPR is a sinusoidal function $I(\phi) = I_c \sin(\phi)$, where $I(\phi)$ is the Josephson supercurrent, ϕ is the phase difference between superconducting leads, and I_c is the critical current. In a φ_0-junction, $I(\phi = 0) \neq 0$, which is

[1]This chapter has been adapted from a collaborative work between our team, UCSB, and Univ. Grenoble, as published in Ref. [35].

equivalent to a phase offset φ_0 in a sinusoidal CPR [120, 121, 122, 123, 124, 125, 36, 126, 127, 128, 129, 130]. The φ_0-junction state can be accompanied by bias direction-dependent critical current [36, 126, 127, 128], which was dubbed the "supercurrent diode effect" [131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142].

A related effect is the π-junction effect where the additional phase shift is equal to π [143]. Note that the π-junction is not a special case of a φ_0-junction. The π-junction can be realized under more basic conditions, for instance without any spin-orbit interaction [144].

Attempts were made to detect the phase shift φ_0 in superconducting quantum interference devices (SQUIDs) [37, 145]. However, large magnetic fields were used. These fields were in the SQUID plane in order not to induce flux in the loop. However, at high fields of hundreds of milliTesla to a few Tesla, and given the SQUID area in the tens of square microns, multiple flux quanta thread the SQUID due to fringing fields and imperfect alignment even when the utmoust effort is applied to ensure strictly in-plane applied fields. Furthermore, Josephson junctions based on semiconductor nanowires are gate-tunable. This is typically thought of as an advantage due to an extra control knob. But the electric field from the gate changes the path of supercurrent in the nanowire, and with it the enclosed flux in the SQUID. A change by a fraction of a flux quantum is plausible for a 100 nm nanowire in a field of hundreds of mT. This shifts the SQUID interference pattern due to extra flux and not due to the intrinsic spin-orbit interaction and the associated φ_0-junction effect.

We use supercurrent diffraction patterns as means of investigating the φ_0-junction state [131]. The diffraction pattern is the evolution of the critical current in magnetic field. It can reveal exotic effects such as d-wave superconductivity in corner junctions [146], the presence of edge states in planar junctions [147], higher-order Josephson harmonics [49]. The fields at which the effect manifests are as low as 10-20 mT, smaller than in previous works [37, 145] but large enough to dominate over possible self-field effects.

In InSb-Sn nanowire junctions, we observe skewed diffraction patterns. When the magnetic field is perpendicular to the nanowire and in-plane (along the $\hat{x}$-direction), the switching current I_c is inversion symmetric with respect to flux and current bias. The pattern is nearly-symmetric along the out-of-plane direction ($\hat{y}$) and along the current flow direction ($\hat{z}$) [Fig. 6.2(a)]. The effect is observed over wide ranges of gate voltage, which works

against a fine-tuning explanation. At the same time, no consistent effect of gate voltage on the skew magnitude is observed. To interpret our results, we develop two models. The first is a phenomenological model that illustrates how a two-component CPR with φ_0 can result in a skewed diffraction pattern. The second is a numerical tight-binding model which yields the φ_0-junction. Using realistic junction parameters, the numerical model is capable of reproducing the key experimental observations.

6.2 Phenomenological model for skewed pattern

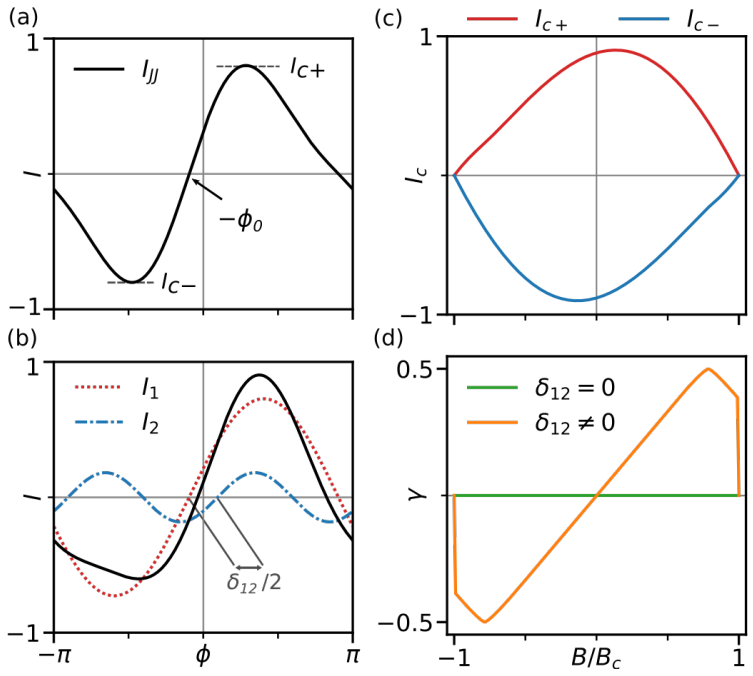

Figure 6.1: A phenomenological model for the skewed diffraction pattern: (a) CPR of a ϕ_0-Josephson junctions ($\delta_{12} = 0$) at an external field $B = 0.5B_c$ with $\phi_0 = B$. Local maximum and minimum of CPR are taken as critical current flow through positive and negative bias I_{c+} and I_{c-}. In this configuration we have $|I_{c+}| = |I_{c-}|$. (b) CPR of first (red dotted), second harmonic (blue dot-dashed), and their sum (black solid) at external field $B = 0.5B_c$. The second harmonic has a shift of ground-state phase $\delta\phi$ from the first order with a magnitude of $\delta\phi = \delta_{12}/2$. (c) Skewed diffraction pattern generated with our phenomenological model. (d) Coefficient γ as a function of field B_x when $\delta_{12} = 0$ and $\delta_{12} \neq 0$, respectively.

We present a phenomenological model capable of reproducing skewed diffraction patterns due to the φ_0-junction effect. This is not a microscopic model, but we also perform microscopic tight-binding calculations further below. In this model, we postulate a CPR with the first and second sinusoidal harmonics. In addition to a variable phase across the junction ϕ, we allow for two phase offsets: the global parameter φ_0 and the relative phase offset between the first and the second harmonics, δ_{12}:

$$I(\phi) = I_1 \sin(\phi + \varphi_0) + I_2 \sin(2\phi + 2\varphi_0 + \delta_{12}) \tag{6.1}$$

where I_1 and I_2 are the amplitude of each harmonic at zero external field.

We first explain how this CPR realizes the so-called supercurrent diode effect. If $I_2 = 0$, the CPR exhibits $I(\phi = 0) \neq 0$ with the trace shifted by φ_0 [Fig. 6.1(a)]. This offset can, in principle, be detected in a SQUID, but not in a single junction measurement. This is because $I_{c+} = I_{c-}$ for the supercurrent flow through the positive and negative bias direction. The same is true if $I_2 \neq 0$, but $\delta_{12} = 0$. However, if a phase offset between the first and the second harmonics $\delta_{12} \neq 0$, we get $I_{c+} \neq I_{c-}$, and the current-voltage characteristic of the junction becomes shifted upwards or downwards [Fig. 6.1(b)].

This is the supercurrent diode effect. In a single junction, the phase ϕ is free to adjust until the maximum supercurrent is reached, detected by a switch into the finite voltage state. If the CPR has at least two components with a phase offset between them, the switching current is different for positive and negative bias directions. Note that the diode effect is not to be confused with hysteretic supercurrent in underdamped junctions.

6.3 Device fabrication and skewed diffraction pattern

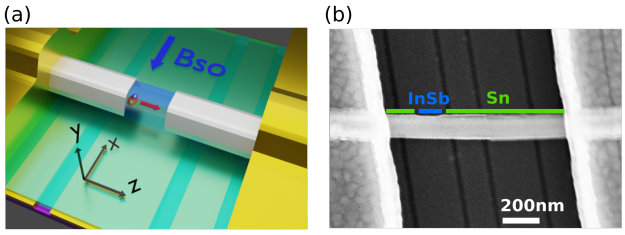

Figure 6.2: (a) Cartoon of a shadow nanowire Josephson Junction device. Effective spin-orbit magnetic field (B_{so}) is indicated. (b) Scanning Electron Microscope image of Device A.

Junctions are prepared by coating the standing InSb nanowire with a 15 nm layer of Sn [33]. In front of the nanowire, another nanowire shadows the flux of Sn to create two

disconnected Sn segments. Shadow junction wires are transferred onto chips patterned with local gates, contacts to wires are made using standard electron beam lithography and thin film deposition. Measurements are done in a dilution refrigerator with a base temperature of ∼50 mK equipped with a 3D vector magnet. Experimental panels ploting switching current are extracted from current-voltage measurements.

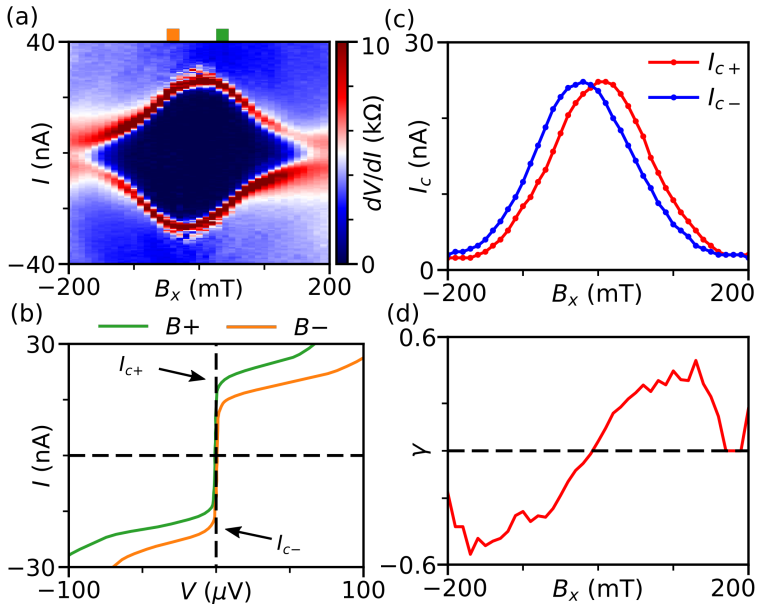

Figure 6.3: Skewed critical current diffraction pattern in device A. (a) At gate voltage $V_{gate} = -2$V. The normal resistance is 4 kΩ. (b) Line-cuts from (a) labeled with color squares. Critical current at positive and negative bias are labeled as I_{c+} and I_{c-}. (c) Upper panel: switching currents extracted from panel (a), Lower panel: Coefficient γ calculated from panel (c).

Fig. 6.3 shows a representative skewed diffraction pattern from device A. The field is applied along $\hat{x}$. In Fig. 6.3(a) the switching current is where the differential resistance dV/dI changes from zero (dark blue) to a finite value. In data processing, we treat current source that gives voltage drop across the device smaller than 10μV as superconducting regime and vice versa. The switching currents I_{c+} and I_{c-} extracted from panel (a) exhibit maxima displaced to positive and negative fields respectively [Figs. 6.3(b),6.3(c)]. By taking I-V traces at $B_x = 50$ mT and $B_x = -50$ mT, we get $\Delta I_c = 5 - 8$ nA [Fig. 6.3(b)], which is

about 30% of $|I_c|$. The maxima of $I_{c\pm}$ are at $B_x = \pm 20$ mT. The coefficient γ peaks at a higher field of order 100 mT right before the collapse of I_c at higher fields.

Supercurrent is not hysteretic in this regime. A hysteresis would manifest in a vertical shift in the γ dependence which would not be inversion-symmetric. In section 6.11, we discuss data acquisition and processing in the underdamped regime. A 10 mT hysteresis in magnet field is found in the measurements and considered in our discussion.

6.4 Field direction dependence of the skew

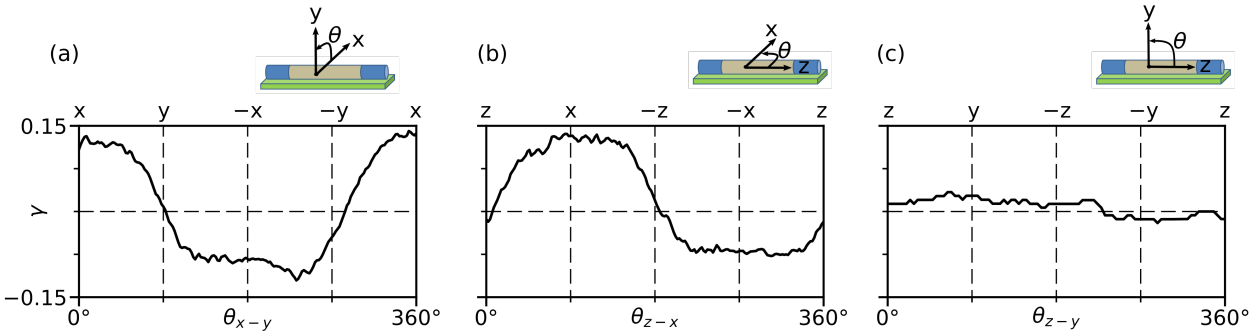

Figure 6.4: Field rotation in Device B. Coefficient γ as a function of angle when the field is rotating in three orthogonal planes: x-y(a), x-z(b), and y-z(c) with fixed strength $|B| = 50$ mT. In (a) the external field is along the $\hat{y}$-axis when $\theta_{xy} = 90°$ and 270°. In (b) the external field is along $\hat{x}$-axis when $\theta_{z-x} = 90°$ and 270°.

Device B has the same geometry as device A and its SEM picture can be found in Fig. 6.7(c). We measure device B in the external field $|B| = 50$ mT and rotate the field in three orthogonal planes. Critical current are traced from zero bias and extracted at where current bias gives differential resistance larger than 2 kΩ. Coefficients γ are calculated based on extracted I_{c+} and I_{c-} [Fig. 6.5(a)-(c)]. γ in x-y and x-z planes reach zero when the external field is aligned to the $\hat{y}$ or $\hat{z}$ axis, and is large along $\hat{x}$. In the y-z plane, γ is significantly reduced. More critical current diffraction patterns in fields at a different angle

in the x-y plane can be found in Fig. 6.15. Device A has its Sn shell on the bottom and device B has the Sn shell on the side [Fig. 6.8]. Nevertheless, the same general behavior, with skew coefficient γ being largest along $\hat{x}$ is observed in all devices (see section 6.10).

6.5 Simulation based on Tight-binding model

We numerically study the microscopic properties of the system within a tight-binding model that has the same geometry as experiments (see section 6.12 for the description of the 3D model). This model was developed to study supercurrent interference in nanowires using KWANT [117, 118, 34]. In that project, the field orientation along the nanowire was primarily investigated. Here, we rotate the field. We can toggle on and off spin-orbit interaction (α), the orbital vector-potential effect of external field ($\mathbf{A}$), while Zeeman effect and disorder always remain on. For details of this model and parameter choosing, see section 6.11 and 6.13.

In Fig. 6.5(a) we reproduce a skewed diffraction pattern within the tight-binding model for fields oriented along $\hat{x}$. Fig. 6.5(b), we illustrate the role of spin-orbit interaction. The characteristic peak-antipeak structure is present whenever $\alpha \neq 0$. The coefficient γ remains zero when only Zeeman effect of magnetic field is included.

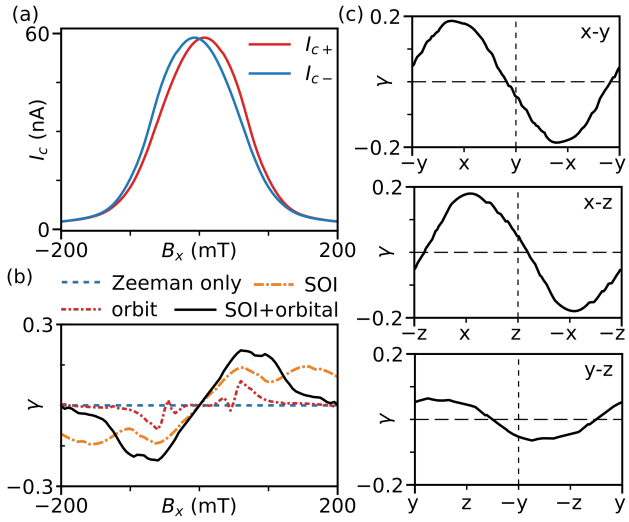

Figure 6.5: Numerical simulation results: (a) Critical currents (I_{c+} and I_{c-}) as a function of magnetic field B_x. The chemical potential is set to two transverse or four spin-full modes ($\mu = 8$meV). (b) Coefficient γ as a function of B_x corresponding to different combinations of terms in the Hamiltonian (see legend). (c) Coefficient γ as a function of angle θ when the external field is rotating in three orthogonal planes with fixed strength $|B| = 50$ mT. The Zeeman effect (g = 50) is present in all the results. Other parameters used in the simulation are $\alpha = 200$ nm $\cdot$ meV, $m_{eff} = 0.015m_e$, temperature $T = 100$ mK. The lattice constant $a = 8$ nm, the nanowire diameter $d_1 = 120$ nm, the outer diameter (with Sn shell) $d_2 = 140$ nm and the coverage angle $\phi = 180°$.

Orbital effect only ($\alpha = 0$, $\boldsymbol{A} \neq 0$) yields a similar structure (see $B_x = 80$mT), limited in magnitude and field. We believe this is a simulation artefact that appears when the external field is perpendicular to the line connecting the center of the wire and the center of the shell. With all contributions toggled on, we reproduce the magnetic field anisotropy of coefficient γ, compare Fig. 6.4 and Fig. 6.5(c).

The tight-binding model allows us to generate CPR, which exhibit φ_0 shifts as well as higher order harmonics and an extra δ_{12} emerge and increase when field is along $\hat{x}$ [Fig. 6.25]. This agrees with the phenomenological model of Fig. 6.1. Some of the parameters used in the model, such as spin-orbit strength, exceed those previously reported for InSb nanowires [61],

however we cannot claim that matching this model to data is a reliable way of extracting spin-orbit interaction strength.

6.6 Gate voltage dependence of the skew

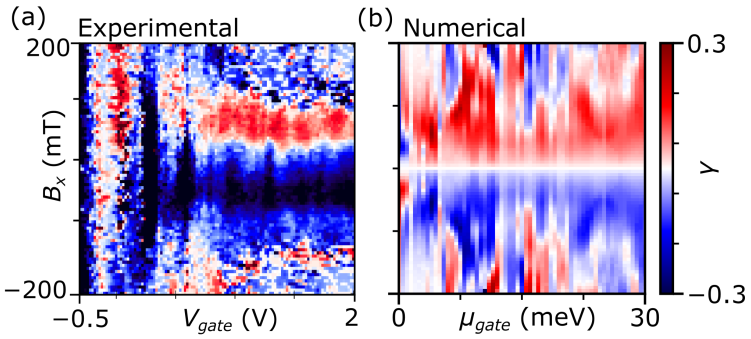

Figure 6.6: Comparison between the experiment from device B (a) and the numerical simulation (b). Coefficient γ versus external field B_x and gate voltage (chemical potential μ) are plotted as 2D maps to study skew shape as function of gate voltage (μ in simulation). Parameters used for the simulation are the same as in Fig. 6.5. Based on the discussion in Supplementary Section V, the gate voltage range in our experiment is corresponding to chemical potential μ = 15-30 meV in the simulation. Another 2D map derived from Device C can be found in Fig. 6.25.

For device B we take gate sweeps of the supercurrent in a series of external fields that are along the $\hat{x}$-axis [Fig. 6.6(a)]. We observe that for $V_{gate} > 0$, γ has a characteristic peak-antipeak shape in magnetic field which describes the skewed diffraction pattern. The behavior is observed over a significant range of gate voltages, from near pinch-off to near saturation of normal state conductance. The less regular traces at negative gate voltages are too close to pinch-off where supercurrent is small, where extracted magnitude of I_c are highly affected by the measurement noise.

The data demonstrate that skewed diffraction patterns do not appear only at fine-tuned values of gate voltage. On the other hand, there is no clear gate voltage dependence of the

magnitude of magnetic field extent of γ. The behavior looks qualitatively similar in the tight-binding simulation [Fig. 6.6(b)]. Given the gate voltage range, we do not expect being able to significantly tune the bulk Rashba spin-orbit coefficient in these InSb nanowires.

6.7 interpretation and Conclusion

Skewed diffraction patterns were observed for decades in Josephson junctions due to self-field effects, where current through the junction generates flux in the junction. This effect is more pronounced in wide junctions with high critical current density. We estimate the magnetic field generated by current flow through a nanowire with the Biot-Savart Law. With current I = 300 nA, nanowire radius r = 60 nm and Junction width L = 120 nm, we get self induced field B $\sim$ 1 μT at the surface. In Fig.2 (a) and (c), the maximum and minimum of I_c are achieved at $|B|$ = 20 mT, which is thousands of times larger than the self-induced field. Therefore, the self-field effect is not enough to explain the skewed pattern we observe. Furthermore, the skew due to self-fields should generally manifest for external fields along both $\hat{x}$ and $\hat{y}$, and be sensitive to the shell orientation, while the skew reported here is strongest along $\hat{x}$ for two different shell orientations.

Skewed diffraction patterns, observed in our experiment, are reproduced using two theoretical models. The phenomenological model, and the tight-binding model, both agree that the imbalance between I_{c+} and I_{c-} and the critical current maxima displaced for zero field are related to the CPR with two Josephson harmonics, and a phase-shift between them. The tight-binding model yields phase-shifts φ_0 and δ_{12} due to strong Rashba spin-orbit interaction. Experiment shows that skew in diffraction pattern is largest when the field is oriented along $\hat{x}$, the likely orientation of spin-orbit effective field in nanowires. The effects are observed in multiple nanowires and require no fine-tuning with gate voltages.

6.8 Fabrication method and Measurement setup

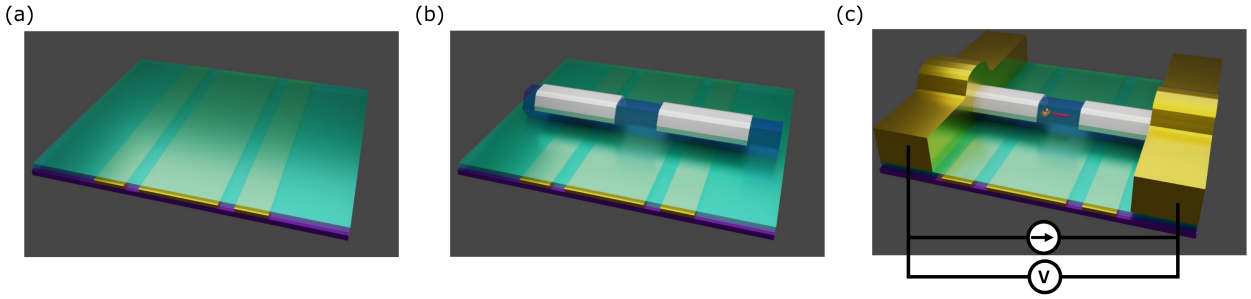

Figure 6.7: Fabrication steps in making nanowires Josephson junction (a) Local gate chips made on a Si substrate (purple). Ti/AuPd gates (gold) are covered by HfOx dielectric (Green) (b) InSb shadow nanowires that are half-covered by Sn shells are transferred onto the chips. (c) Metal leads made with Ti/Au are connected to the shell to form a Josephson junction.

Nanowires are placed onto a Si chip that has predefined local gates. Electrostatic local gates are patterned by 100 keV Electron Beam Lithography (EBL) on undoped Si substrates 3.2.3. Local gates have mixed widths of 80 and 200nm and are separated with a distance of 40 nm. Electron beam evaporation of 1.5/6nm Ti/PdAu is used to metalize the gates which are covered by 10nm of ALD HfOx that serves as a dielectric layer [Fig. 6.7(a)].

Based on the Scanning electron microscope images of all devices that are studied in this report, the length of the JJs made with Sn-InSb nanowires is 120-150nm. The width of the junction is the same as the width of the nanowires, which is 120nm. After placing nanowires onto gates [Fig. 6.7(b)], we cover the whole chip with PMMA 950 A4 electron beam resist. Resist is dried at room temperature by pumping with a mechanical pump in a metal desiccator for 24 hours. Then we use EBL to define normal lead patterns. After development, we clean the residue of resist in an oxygen plasma asher. In the electron beam evaporator, we first use an *in-situ* ion mill to remove AlOx capping layer from the nanowires in the contact area, after which we deposit 10nm/130nm Ti/Au on the chips. [Fig. 6.7(c)].

Details of fabrication method can be found at 3.2.

Transport 2-point measurements with currents source and voltage measurement model in parallel are used, with several stages of filtering placed at different temperatures. Details of measurement setup can be found at 3.3.

6.9 Device list and shell orientation

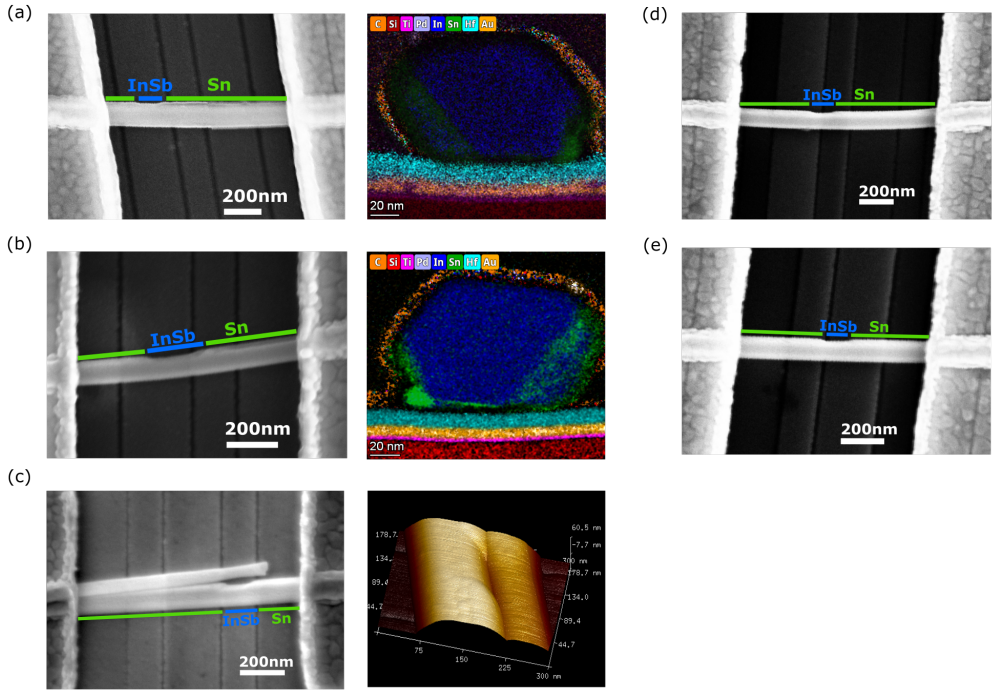

Figure 6.8: Scanning electron microscope (SEM) image of of Devices measured in report. (a) Right: SEM image of Device A (Chip: QPC2). Left: Scanning transmission electron microscopy (STEM) based Energy-dispersive x-ray spectroscopy (EDS) spectroscopic elemental image of Device A. (b) Right: SEM image of Device A1 (Chip: QPC2). Left: STEM based EDS spectroscopic elemental image of Device A1. (c) Right: SEM image of Device B (Chip: QPC4). Left: Atomic force microscopy (AFM) image of Device B. (d) SEM image of Device C(Chip: QPC3) (e) SEM image of Device C1 (Chip: QPC3)

3 chips are studied in this project. Each chip contains multiple devices. Among these chips, 5 devices demonstrate sharp critical currents that are tuned by the gates. Skewed diffraction patterns taken from these devices are all plotted and posted in this report. In the main text, we present skewed diffraction patterns from device A [Fig. 6.3]. In device B, we study field direction dependence by rotating fields in different planes and study gate voltage and field effect on the skewed diffraction pattern with a 2D map [Fig. 6.4 and 6.6].

Devices A and A1 are on Chip QPC2. The EDX results show InSb nanowires and Sn shells. No ferromagnetic materials were found in the junction. Sn shells are half-covering the nanowires from the bottom side and are in touch with the HfOx dielectric layer.

Device B is on Chip QPC4. The shell orientation of the device is studied with Atomic Force Microscopy [Fig. 6.8(c)]. Based on the AFM images, we conclude that the Sn shell is on the side.

Devices C and C1 are on Chip QPC3. The shell orientations are not studied.

6.10 Diffraction pattern at different gates in filed along three axes

6.10.1 Diffraction pattern measured in Device A

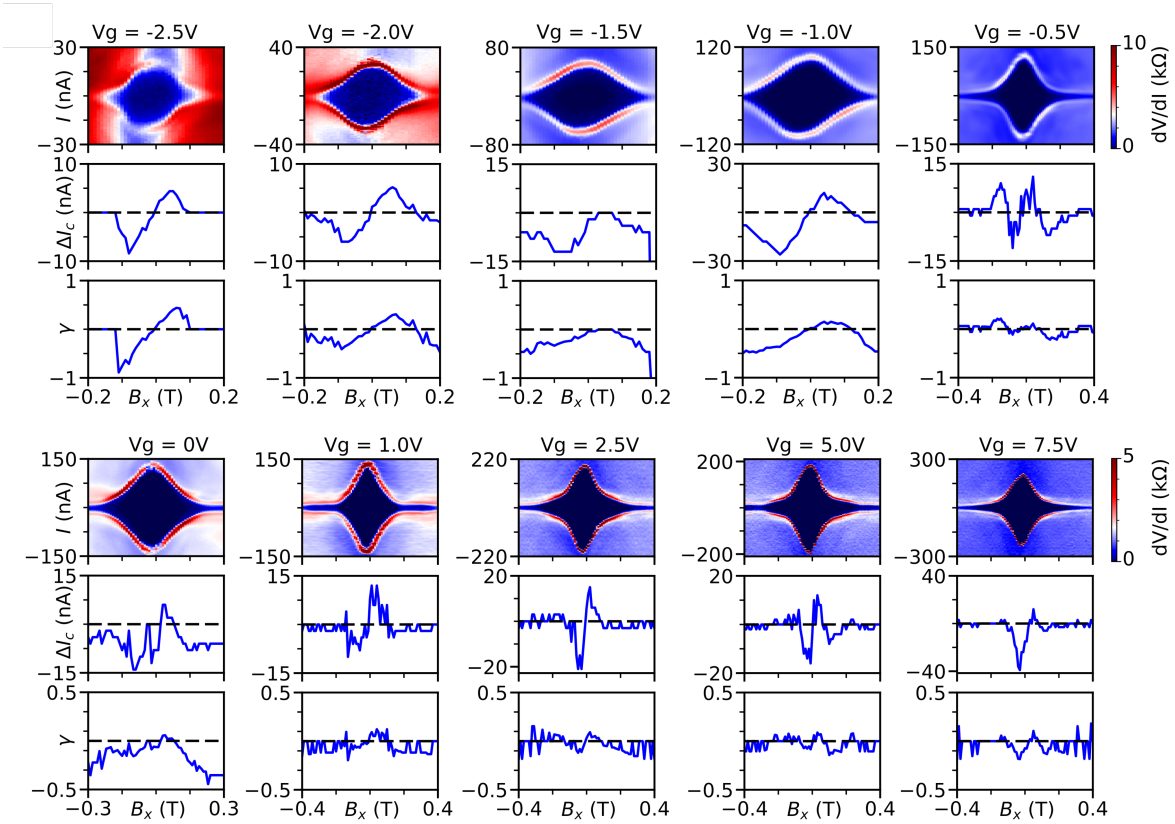

Figure 6.9: Diffraction patterns at different gates in the field along x-axes, measured in Device A (QPC2).

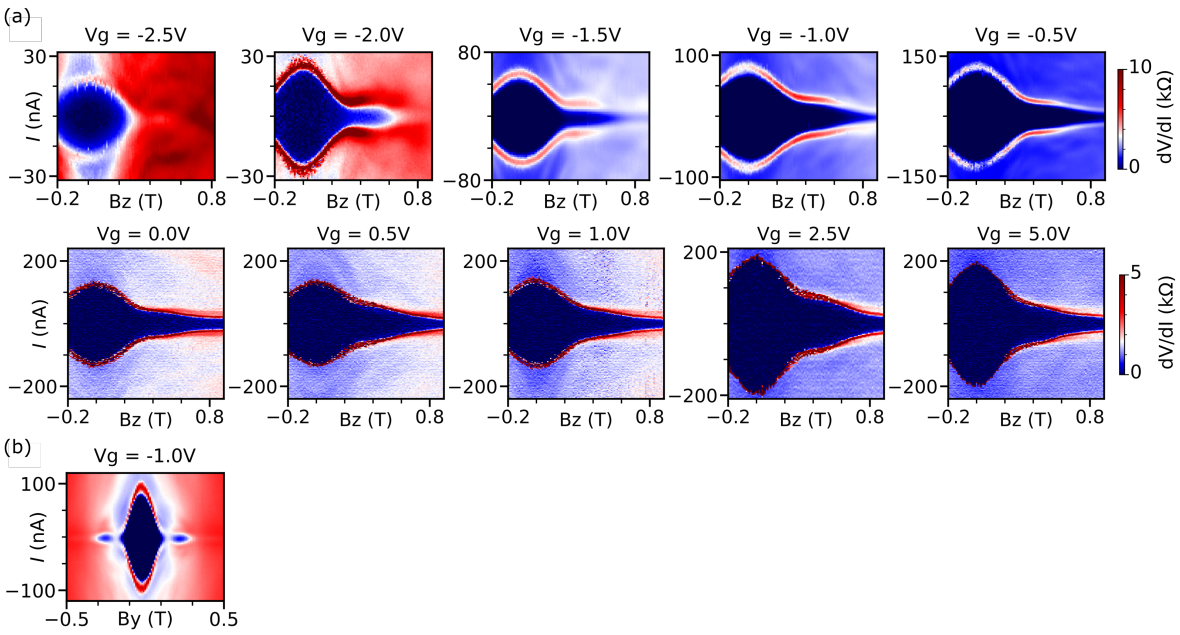

Figure 6.10: Diffraction patterns at different gates in the field along y-axes (a) and z-axes (b), measured in Device A (QPC2).

6.10.2 Diffraction pattern measured in Device A1

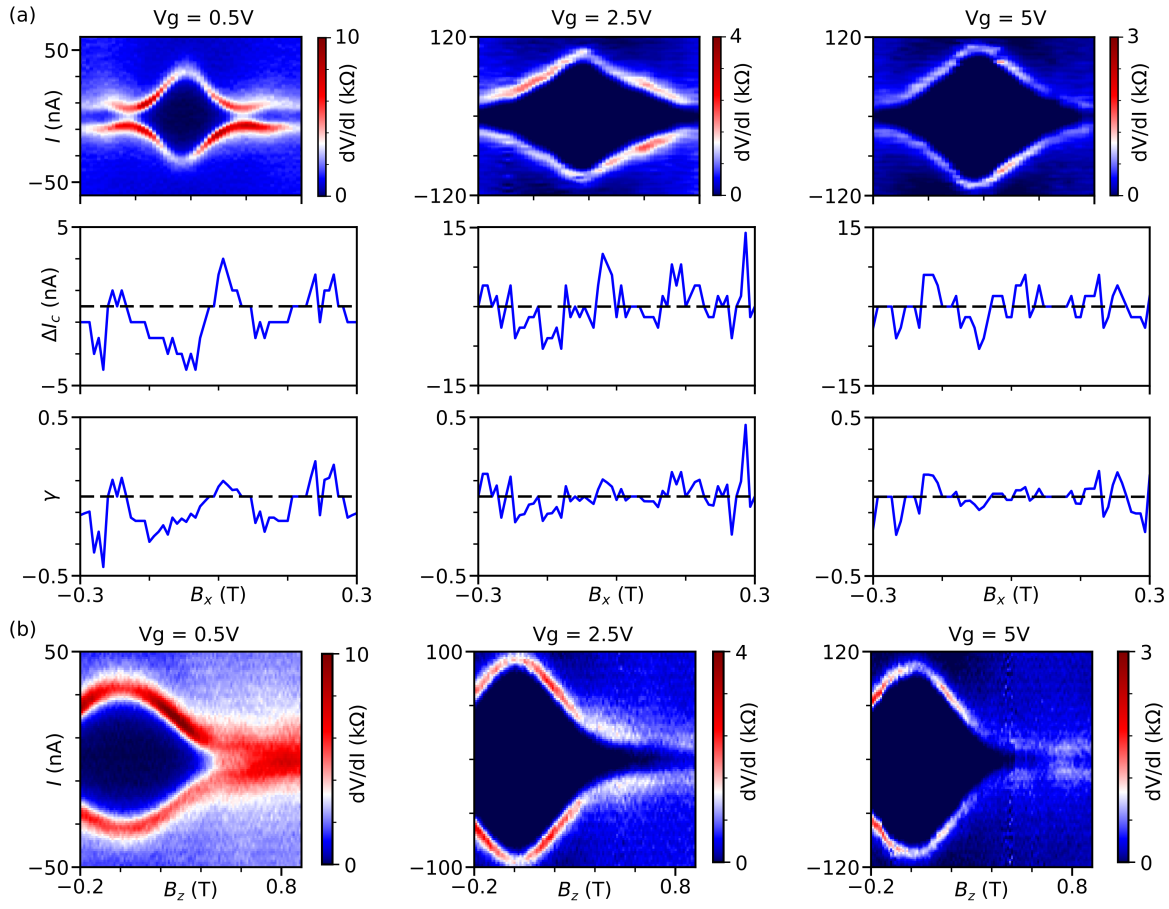

Figure 6.11: Diffraction patterns at different gates in the field along $\hat{x}$ and $\hat{z}$ axes, measured in Device A1 (QPC2). (a) dV/dI differential resistance as function of $\hat{x}$-direction field B_x and current bias. γ is calculated with the extracted magnitude ΔI_c. (b) Diffraction pattern when the field is applied parallel to the nanowires, along $\hat{z}$-direction.

6.10.3 Diffraction pattern measured in Device B

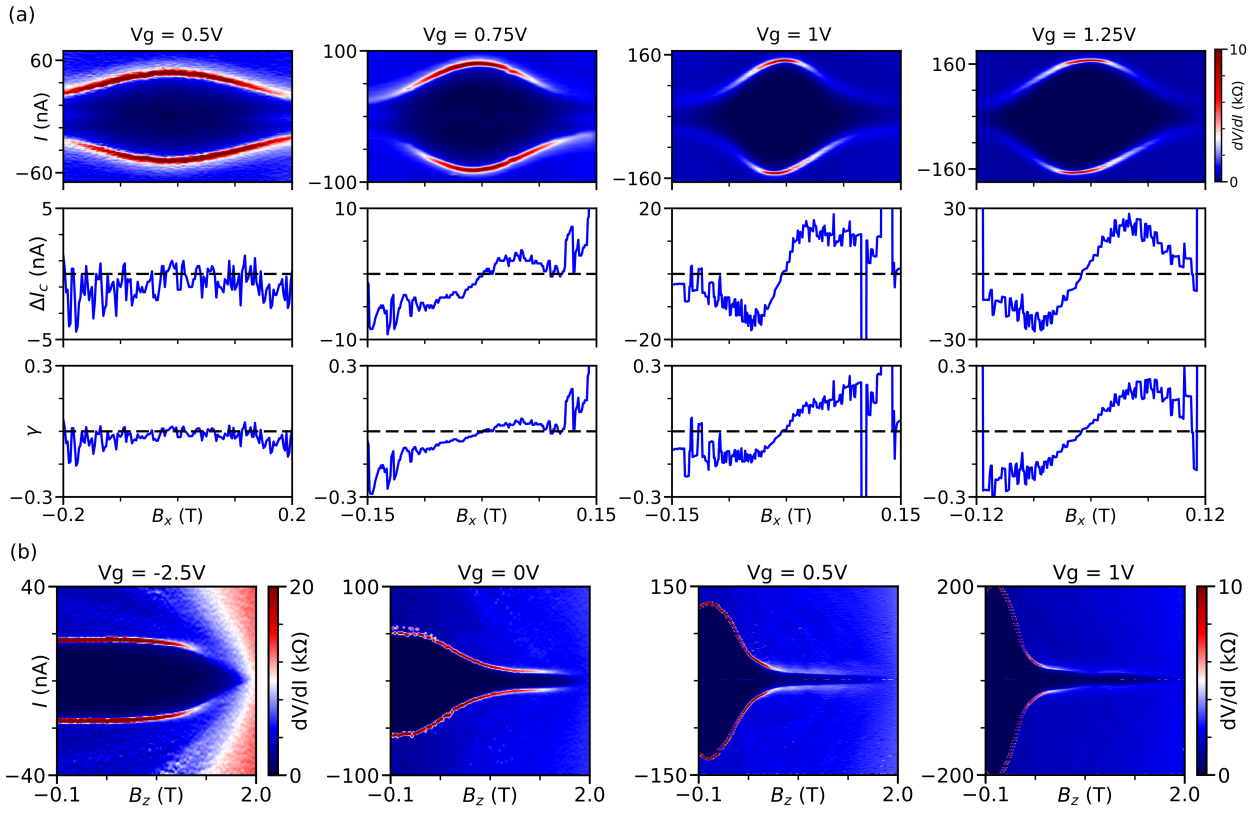

Figure 6.12: Diffraction patterns at different gates in the field along $\hat{x}$ and $\hat{z}$ axes, measured in Device B (QPC4). (a) dV/dI differential resistance as function of $\hat{x}$-direction field B_x and current bias. γ is calculated with the extracted magnitude ΔI_c. (b) Diffraction pattern when the field is applied parallel to the nanowires, along $\hat{z}$-direction.

6.10.4 Diffraction pattern measured in Device C

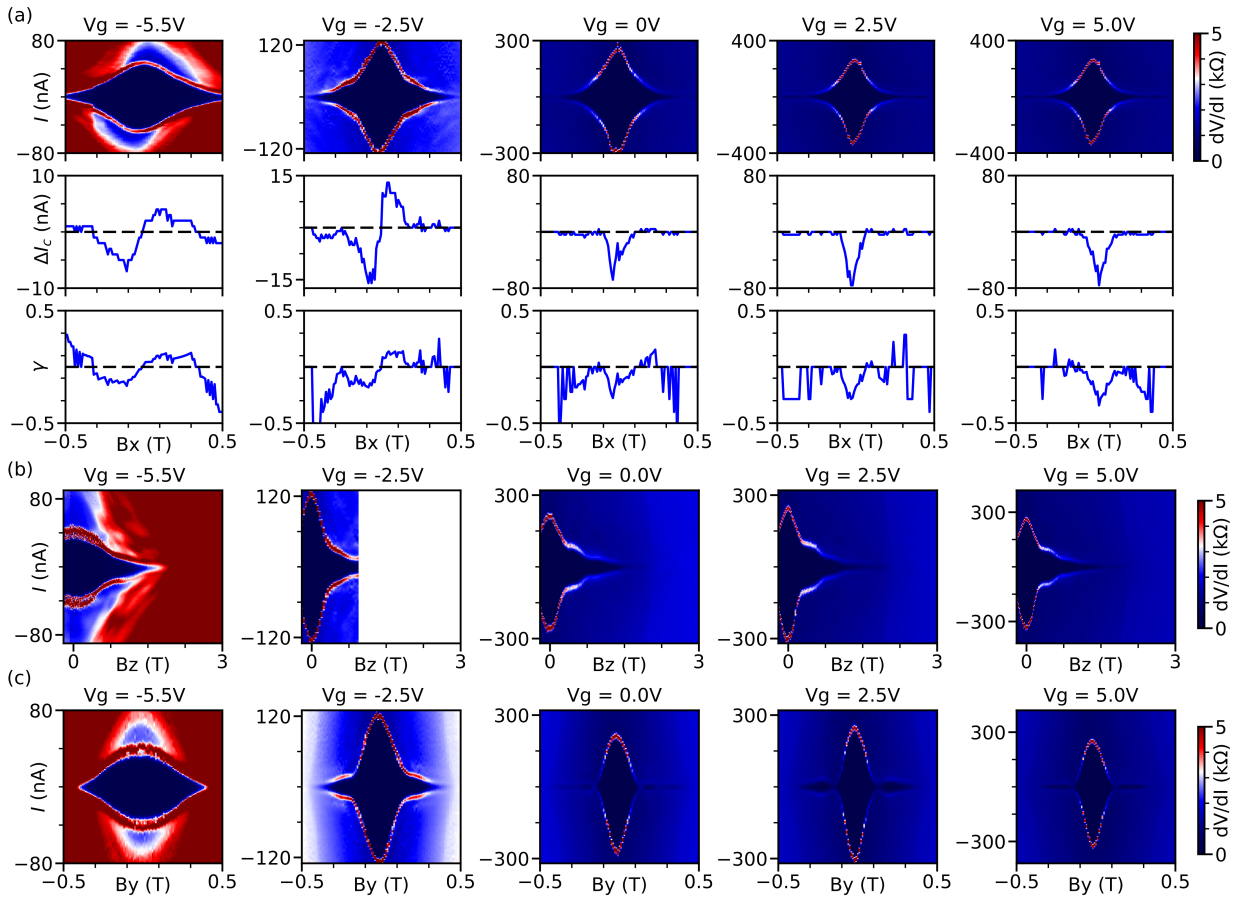

Figure 6.13: Diffraction patterns at different gates in the field along three axes, measured in Device C (QPC3)(a) dV/dI differential resistance as function of $\hat{x}$-direction field B_x and current bias. γ is calculated with the extracted magnitude ΔI_c. (b) Diffraction pattern when field is applied parallel to the nanowires, along $\hat{z}$-direction. (c) Diffraction pattern when the field is applied out of substrate plane, along $\hat{y}$-direction.

6.10.5 Diffraction pattern measured in Device C1

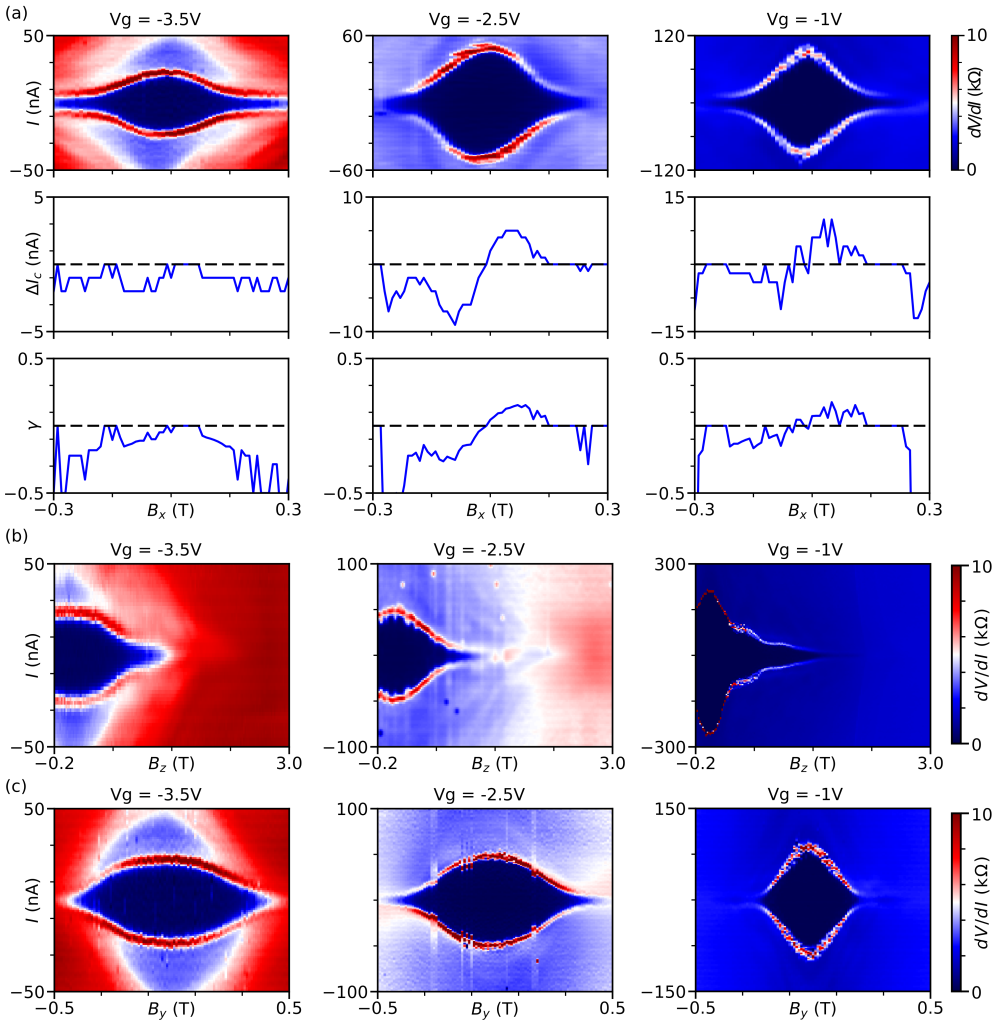

Figure 6.14: Diffraction patterns at different gates in the field along three axes, measured in Device C1 (QPC3) (a) dV/dI differential resistance as function of $\hat{x}$-direction field B_x and current bias. γ is calculated with the extracted magnitude ΔI_c. There is a shift of gate, so strength of I_c may be different from scans with other two fields directions. (b) Diffraction pattern when field is applied parallel to the nanowires, along $\hat{z}$-direction. (c) Diffraction pattern when the field is applied out of substrate plane, along $\hat{y}$-direction.

6.10.6 Diffraction pattern at x-y plane, Device C

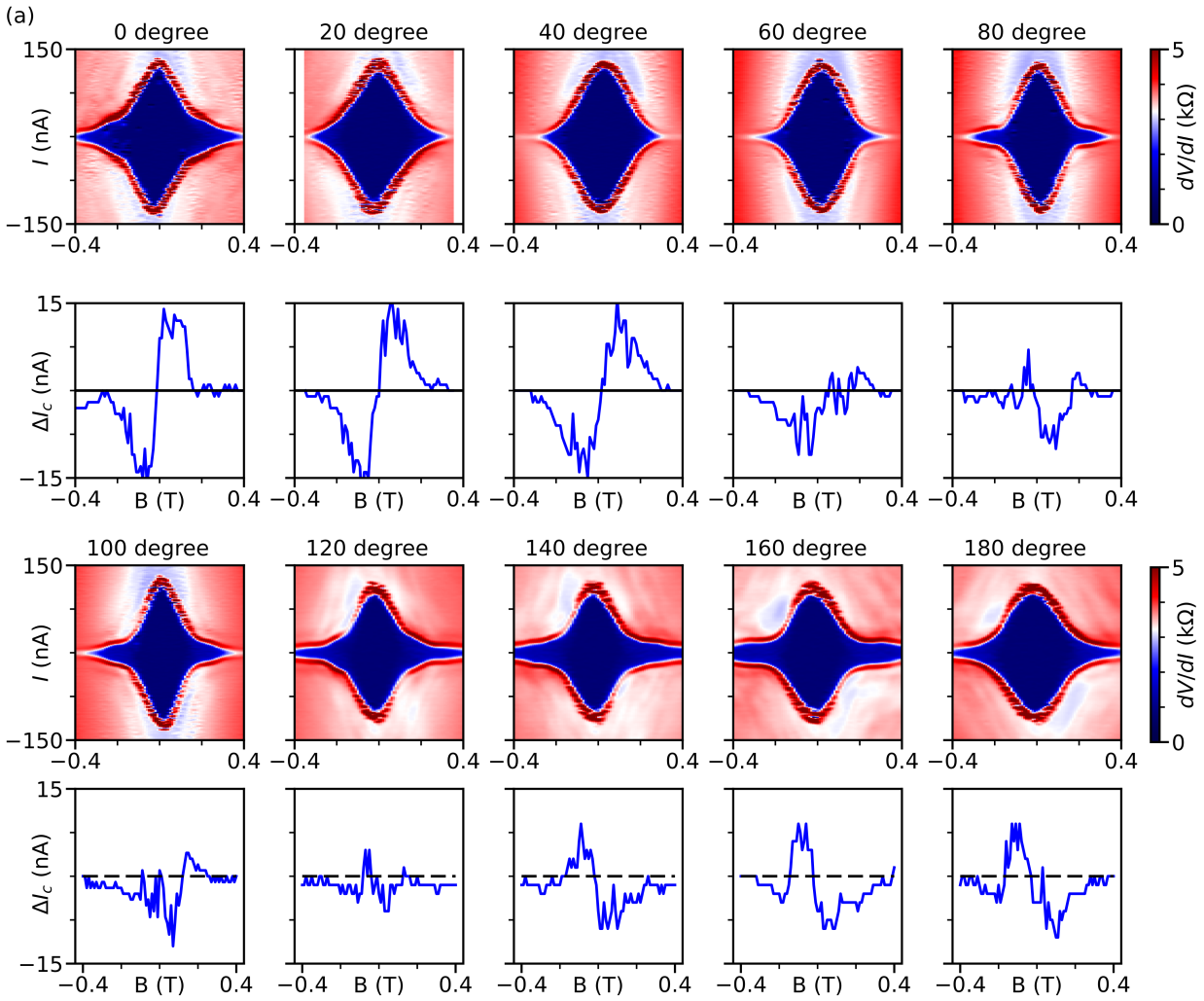

Figure 6.15: Diffraction pattern at the x-y plane, the field is applied along angle θ_{x-y} between 0° to 180°, measured in Device C. Critical current difference ΔI_c is extracted from measurement data using a peak finder Python script.

6.11 Characteristics of the Junctions and hysteresis in the measurement setup

The gate effect is studied by applying a bias voltage across the device $V_{bias} = 10mV$. Conduction channels in Device A [Fig. 6.16(a)] can be fully closed by the tunnel gate. While

Devices B and C [Fig. 6.16(d),(g)] cannot be fully closed. The Josephson effect at zero magnetic field is best studied in the current-bias configuration [Fig. 6.16(c),(f),(i)]. The switching current from superconducting to normal state regime is demonstrated with a read peak in differential resistance (referred to in other Figures as I_c). The magnitude of I_c is calculated with $|I_c| = (|I_{c+}| + |I_{c-}|)/2$, where I_{c+} and I_{c-} are extracted with a peak finder Python script by finding the two of largest differential resistance at each gate voltage. I_c increases at more positive gate voltage, while the extracted products $I_c R_N$ (R_N is the normal state resistance) are in the range of 200-300 $\mu \cdot eV$.

6.11.1 Chemical potential used in simulation and corresponding gate voltage in experimental measurements

In an attempt to establish additional correspondence between experiment and theory, we study conductance as a function of chemical potential μ in the simulation [Fig. 6.16(j)]. The normal state resistance read from skewed pattern in Fig. 6.3(a) in main text is 4 kOhm, which is close to two transverse modes or four spin-full modes. So we choose $\mu = 8$ meV to study the skew shape in Fig. 6.5. When studying the direction-dependent supercurrent transport as function of field direction, we get the normal state resistance about 1.5-2 kOhm. Which is corresponding to six to eight transverse modes or twelve to eighteen spin-full mode, and chemical potential $\mu \approx 20meV$ in the simulation.

The skew map presented in Fig. 6.6 in main text is measured from Device B. By comparing normal state conductance G as a function of V_{gate} in simulation and measurement data [Fig. 6.16(j)], we conclude the range used in Fig. 6.6, which is -0.5V to 2V, is corresponding to chemical potential $\mu = 15 - 60meV$. Another skew map measured with Device C in Fig. 6.25(c) has gate voltage range from -3V to 2V, which is corresponding to $\mu = 30 - 60meV$.

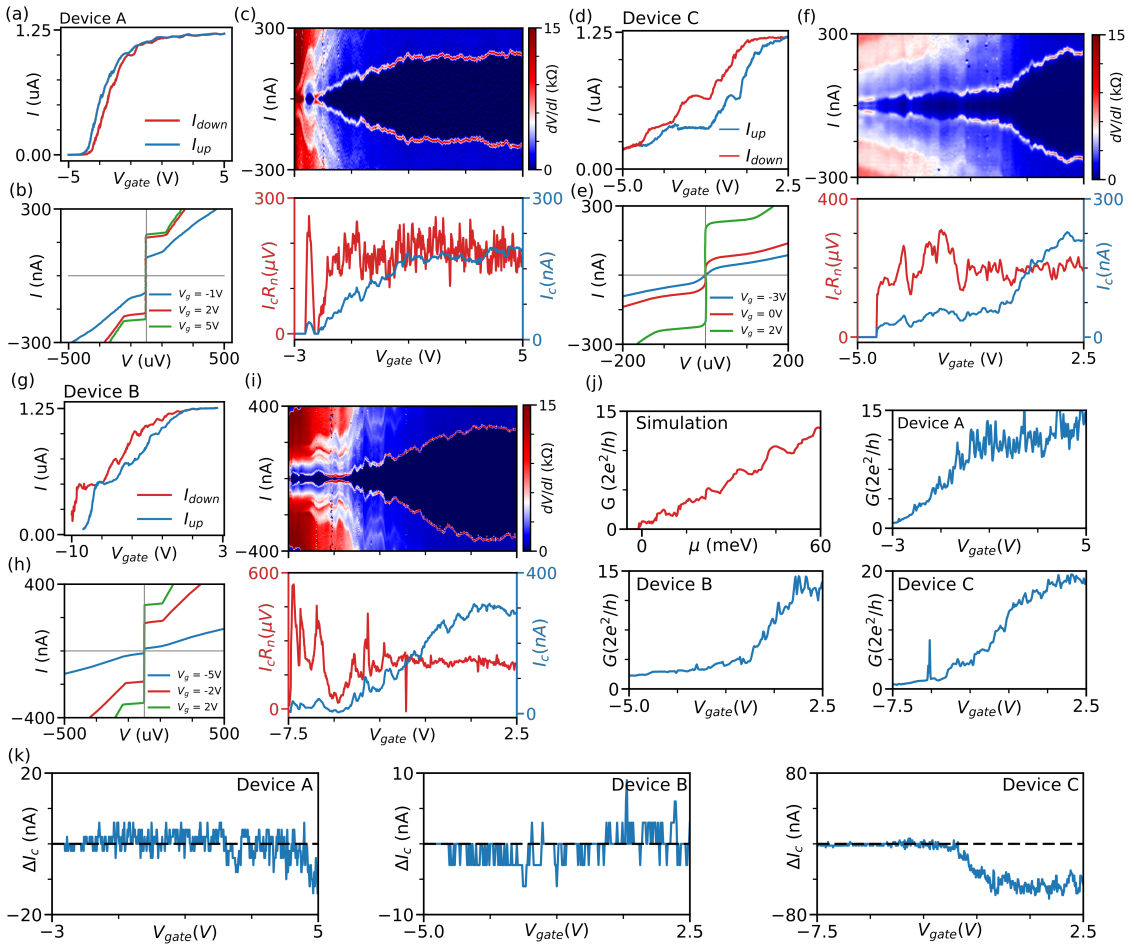

Figure 6.16: Gate dependence taken at external field $|B| = 0$, measurement data are taken from Device A (a-c), Device B (d-f) and Device C (g-i). (a,d,g) Current through the JJs as function of gate voltage V_{gate} when bias voltage is set to be $V_{bias} = 10\text{mV}$. (b,e,h) V-I characteristics taken at different gate voltages. (c,f,i) Upper panel: dV/dI differential resistance as a function of current source and V_{gate}. Lower panel: extracted critical current I_c (blue) and I_cR_N product (red) as functions of V_{gate}.(j) Electrical conductance of the junction in the unit of quantum conductance $(2e^2/h)$ as a function of chemical potential μ when simulating with parameters used in other figures. Followed by normal state conductance as a function of gate voltage V_{gate} measured in device A, B, and C, respectively. Differential resistance are extracted from (c,f,i) and converted to conductance for plotting. (k) Critical current difference calculated with ΔI_c as functions of gate voltage at zero field, measured in device A, B, and C. I_{c+} and I_{c-} are extracted from (c,f,i)

6.11.2 Hysteresis in the Josephson junction

Hysteresis in the current-voltage characteristics is studied by extracting $\Delta I_c = |I_{c+}| - |I_{c-}|$ from devices A, B, and C and plotting them as a function of gate voltage at zero magnetic fields [Fig. 6.16(k)]. We find the magnitude of I_{c-} is larger than I_{c+} at more positive gate voltage in Devices A and C. When extracting ΔI_c from skewed diffraction patterns [Figs. 6.9(b), 6.13(c)], it is also easy to see the critical current is larger at negative bias, which results in the gamma as a function of the B_x field that is no longer inversion symmetric about zero fields, zero current. While in Device B, we didn't see the obvious difference between I_{c+} and I_{c-}.

There are two methods used in current configuration measurements: 1. Unidirectional current sweeps, either from positive to negative, or from negative to positive bias. This method is used in Devices A and C. Which results in the hysteresis in current bias.

2. Sweep from zero bias. At a fixed gate voltage or field, scan from zero current bias to the positive and negative side respectively (0 to I_+ and 0 to I_-). So one data set only records scans with I larger than zero and vice versa. Then we combine two datasets to get a full scan. By doing this, we can get rid of the hysteresis because only switching currents are measured. This method is used in device B and the results are plotted in [Fig. 6.4, 6.6].

In the main text, the skewed diffraction pattern from Device A are studied at a smaller gate voltage, $V_{gate} = -2V$ [Fig.6.3]. At this gate voltage, hysteresis in the junction is not observed.

6.11.3 Hysteresis in the superconducting magnet

The effect of magnet hysteresis is studied by scanning the field in two opposite directions, from positive to negative and from negative to positive, respectively. When comparing the extracted critical current difference ΔI_c between positive and negative bias [Fig. 6.17(b)], we can see there is a shift between the two traces. The value of hysteresis can be read from where $\Delta I_c(B) = 0$, and the value here is around 10 mT. This effect can influence angle rotation sweeps, though they are done at fields that are higher than the offset.

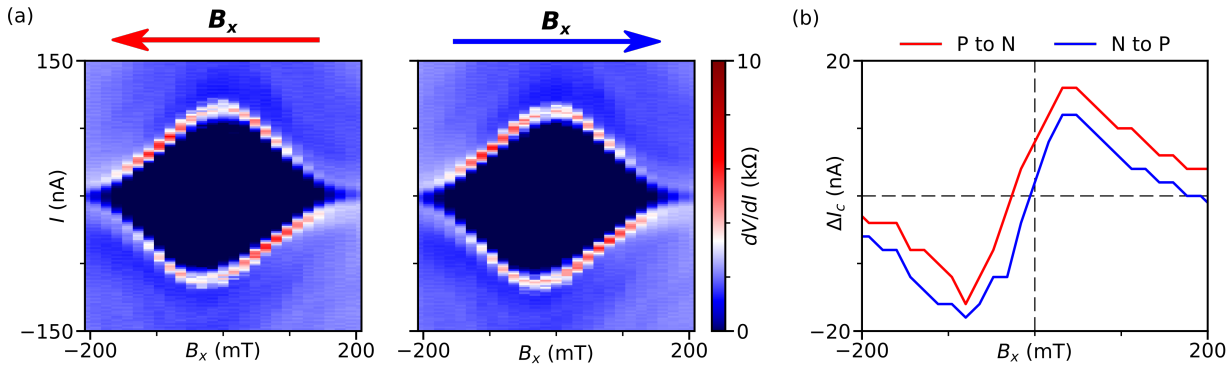

Figure 6.17: (a) Skewed critical current diffraction patterns, field is scanned from positive to negative and from negative to positive direction in adjacent panels. Device A is used in this scan and gate voltage is set to be V_{gate} = -1V for this scan. (b) Extracted critical current difference ΔI_c is plotted as a function of $\hat{x}$-field from two scans in (a).

6.12 Model used in simulation

To simulate the superconductor-nanowire-superconductor Josephson junction in the presence of external magnetic field, we consider the following Hamiltonian for a nanowire that is covered by superconductor lead at both ends.

$$H = \left(\frac{\mathbf{p}^2}{2m^*} - \mu + \delta U\right)\tau_z + \alpha(p_z\sigma_x - p_x\sigma_z)\tau_z + g\mu_B\mathbf{B}\cdot\hat{\sigma} + \Delta\tau_x, \tag{6.2}$$

where τ_i and σ_i are Pauli matrices act on particle-hole and spin space respectively. $\mathbf{p} = -i\hbar\nabla + e\mathbf{A}\tau_z$ is the canonical momentum, and the magnetic potential $\mathbf{A}$ is chosen to be $[0, B_z x - B_x z, -B_y x]$, so that it is invariant along the $x-$direction. Further, m^* is the effective mass, μ is the chemical potential and δU represent the onsite disorder inside the nanowires. The Zeeman effect is given by $g\mu_B\mathbf{B}\cdot\hat{\sigma}$ and the Rashba spin-orbit coupling is given by $\alpha(p_x\sigma_y - p_y\sigma_x)$. Finally, Δ is the superconducting pairing potential.

We first construct a tight-binding model based on the Hamiltonian (6.2), then the critical current under different parameter configurations can be obtained from the imaginary part of the Green's function. These Green's functions can be obtained by using the KWANT package. We explain the code in detail below.

The first step is to construct a system with the scattering region and leads. Here we use the function *kwant.continuum.discretize* to convert the 3D translational symmetric Hamiltonian (6.3) into a tight-binding system (Figure 6.18).

$$H = \left(\frac{\hbar^2(p_x^2 + p_y^2 + p_z^2)}{2m^*} - \mu + \delta U \right) \tau_z + \alpha(p_x\sigma_y - p_y\sigma_x)\tau_z + g\mu_B \mathbf{B} \cdot \hat{\sigma} + \Delta\tau_x, \tag{6.3}$$

Here the Hamiltonian does not contain the orbital effect because *kwant.continuum.discretize* cannot handle the systems with lower symmetry. To include the orbital effect, we need to apply the Peierls substitution to the hopping term. The hopping between two sites $\vec{x}$ and $\vec{x}_0$ becomes $t \to te^{i\phi}$, where $\phi = -e\mathbf{A} \cdot (\vec{x} - \vec{x}_0)/\hbar$.

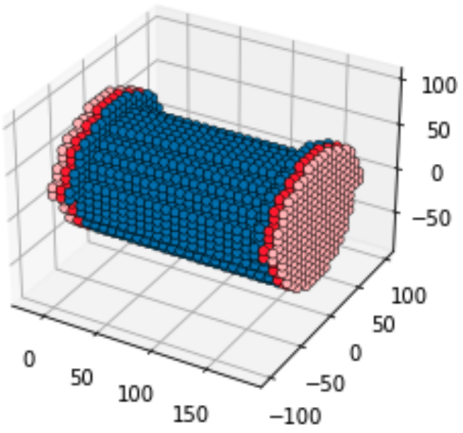

Figure 6.18: Tight-binding model generated by the function *kwant.continuum.discretize*. Red dots represent the infinite leads.

In order to calculate the critical current, besides normal leads and superconducting leads (red region in Fig. 6.18), we need to add a virtual self-energy lead to this system. Here we attach the lead in the middle of the nanowire (yellow region in Fig. 6.19). Notice this self-energy lead is not connected to external devices, and is only used to calculate the Green's

function. Usually, the Green's function of an infinite system contains infinite entries. But now we can divide this nanowire into two parts: self energy lead (L) and the other region (R). Then, we have

$$\begin{pmatrix} G_L^r & G_{LR}^r \\ G_{RL}^r & G_R^r \end{pmatrix} = \begin{pmatrix} E + i\eta - H_{Lead} & H_C \\ H_C^\dagger & E + i\eta - H_R \end{pmatrix}^{-1}, \tag{6.4}$$

where H_C and $H_C^\dagger$ are the hopping between the lead and the rest of the nanowire. By solving this equation we get

$$G_L^r = \left(E - H_{Lead} - H_C^\dagger (E - H_R)^{-1} H_C^\dagger\right)^{-1}. \tag{6.5}$$

Thus the Green's function of the finite self energy lead contains the information about the whole system.

In the KWANT package, the retarded Green's function of the self-energy lead can be obtained by using the function *kwant.solvers.greens_function*. We first calculate the Green's function $G_L^r(0)$ without the phase difference between the two superconducting leads. Then the Green's function with the phase difference φ can be obtained by modifying the Hamiltonian H_{Lead} in equation (6.5). To be more precise, we change the hopping term t to $te^{i\varphi}$, where t is the hopping from the left side of the self-energy lead to the right side.

Critical current under finite temperature T can be calculated by using the imaginary Green's function. Consider the self-energy lead as a subsystem. The current equals the change in the number of electron on the left side of the lead.

$$I = ie \left\langle \sum_{i \in L} \frac{\mathrm{d}n_i}{\mathrm{d}\tau} \right\rangle = \frac{ie}{\hbar} \left\langle \sum_{i \in L} [c_i^\dagger(\tau) c_i(\tau), H_{Lead}] \right\rangle. \tag{6.6}$$

Here we consider the imaginary time evolution and i runs through the positions to the left of the self-energy lead. For any diagonal term $c_j^\dagger c_j$ in H_{Lead}, we have

$$[c_i^\dagger c_i, c_j^\dagger c_j] = 0. \tag{6.7}$$

For $j, k \neq i$, we have

$$[c_i^\dagger c_i, c_j c_k] = [c_i^\dagger c_i, c_j^\dagger c_k] = [c_i^\dagger c_i, c_j c_k^\dagger] = 0. \tag{6.8}$$

Therefore, to have the non-zero commutator, we need at least one operator c_j or $c_j^\dagger$ such that $j \in L$. Suppose $j, k \in L$, then we have

$$[c_j^\dagger c_j, c_j^\dagger c_k] = c_j^\dagger c_j c_j^\dagger c_k - c_j^\dagger c_k c_j^\dagger c_j = c_j c_k - 0 = c_j^\dagger c_k \tag{6.9}$$

$$[c_k^\dagger c_k, c_j^\dagger c_k] = c_k^\dagger c_k c_j^\dagger c_k - c_j^\dagger c_k c_k^\dagger c_k = 0 - c_j c_k = -c_j^\dagger c_k \tag{6.10}$$

These two term cancel each other, thus only hopping between the left side and right side of the lead contribute to the critical current. Then the equation (6.6) simplifies to

$$I = \frac{ie}{\hbar} \left\langle \sum_{i\in L, j\in R} [c_i^\dagger(\tau) c_i(\tau), t_{ji} c_i^\dagger(\tau) c_j(\tau) - t_{ij} c_j^\dagger(\tau) c_i(\tau)] \right\rangle \tag{6.11}$$

$$= \frac{ie}{\hbar} \sum_{i\in L, j\in R} (t_{ji} \langle c_i^\dagger(\tau) c_j(\tau)\rangle - t_{ij} \langle c_j^\dagger(\tau) c_i\rangle(\tau)) \tag{6.12}$$

By using the definition $G(\tau, \tau')_{ij} = \langle\langle c_i^\dagger(\tau) c_j(\tau')\rangle\rangle$ for $\tau > \tau'$ we have

$$I = \frac{ie}{\hbar} \sum_{i\in L, j\in R} (t_{ij} G(\tau, \tau')_{ij} - t_{ji} G(\tau, \tau')_{ji}). \tag{6.13}$$

Then by apply the inverse Fourier transformation on the right hand side of this equation and take the limit $\tau - \tau' \to 0^+$, we get

$$\begin{aligned} I &= \frac{ie}{\hbar} \sum_{i\in L, j\in R} \sum_{n\in Z} k_B T (t_{ji} e^{i\omega_n(\tau-\tau')} G(i\omega_n)_{ij} - t_{ij} e^{i\omega_n(\tau-\tau')} G(i\omega_n)_{ij}) \\ &= \frac{iek_BT}{\hbar} \sum_{n\in Z} \sum_{i\in L, j\in R} (t_{ji} G(i\omega_n)_{ij} - t_{ij} G(i\omega_n)_{ij}) \\ &= \frac{-4ek_BT}{\hbar} \sum_{n\in N} \mathrm{Im}\{\mathrm{Tr}\,(T_{RL} G(i\omega_n)_{LR} - T_{LR} G(i\omega_n)_{RL})\} \end{aligned} \tag{6.14}$$

where T_{LR} and T_{RL} are the hopping matrices from left (right) to right (left), $\omega_n = (2n + 1)\pi k_B T$ is the n-th Matsubara frequency for electron. Factor 4 on the last line comes from positive-negative symmetry when sum over all the integers and particle-hole symmetry of the system.

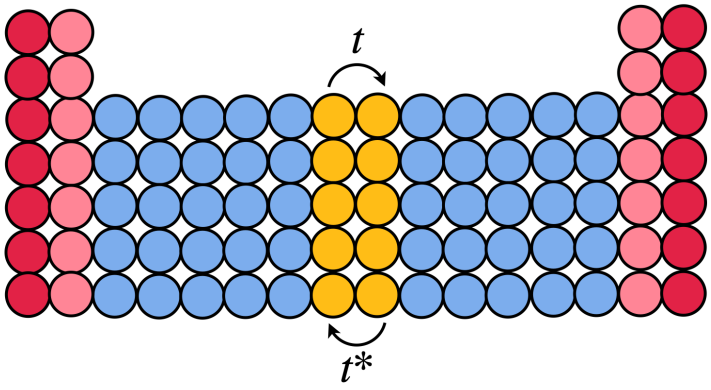

Figure 6.19: Cross section of the nanowire. Here we add a two-layer self energy lead in the middle of the wire, where t is the hopping term from the left side of self energy lead to the right side.

6.13 Parameters used in the simulations

In this section, we discuss the strength of parameters used in the simulation that give the best match to experimental data.

6.13.1 Temperature

In the measurements, lattice temperature can only be estimated by reading the temperature from the sensor on the dilution refrigerator mixing chamber plates and it is varying from 50 to 60 mK while scanning the external field. However, electron temperature is the relevant parameter for the simulation. In our case, electrons are cooled down from room temperature to base temperature by several stages of filters, especially the cooper powder filter. However, the temperature of electrons is usually a bit higher than the device temperature. So we simulate the skewed shape in different temperatures (Fig. 6.20) and choose 100mK for all the simulation results presented in the main text.

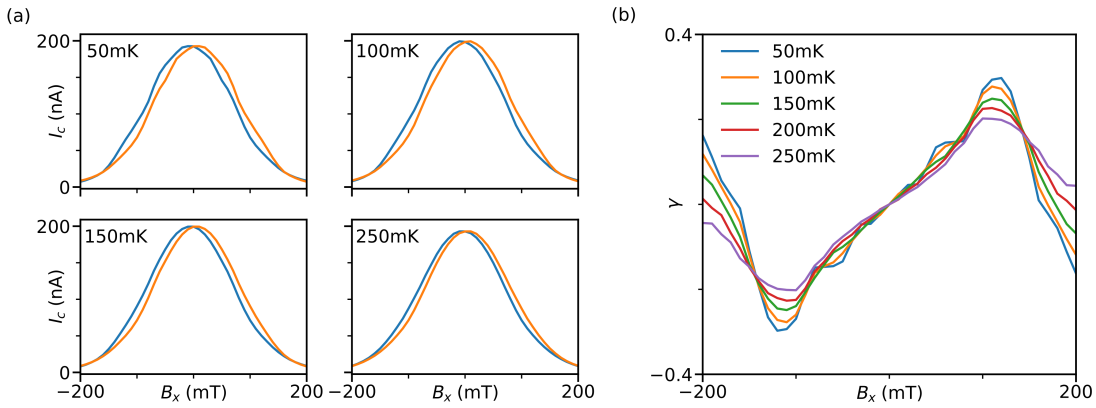

Figure 6.20: (a) Skewed diffraction pattern from simulation when temperature T = 50mK, 100mK, 150mK and 250mK, respectively. (b) Coefficient γ as function of B_x at different temperatures.

From the simulation results, we also find that the maximum and minimum value of coefficient γ become smaller at higher temperature. This is consistent with our temperature dependence measurement results [Fig. 6.24].

6.13.2 Strength of Spin-orbit interaction

The strength of Spin-orbit coupling is estimated by studying the critical current diffraction pattern and choosing the one which best reproduced the experiment results. We set chemical potential $\mu = 8$ meV, which is corresponding to two transverse or four spin-full modes, same value is used in the [FIg. 6.5] in the main text. The skew shape we observe experimentally has two features that we aim to reproduce: 1) the largest critical current I_c is not located at zero field; 2) the largest critical current difference is around $B_x = \pm 50mT$. Based on the skewed shape simulated with different strengths of spin-orbit coupling, we find the skew is best reproduced with $\alpha = 200nm \cdot meV$. So we choose $\alpha = 200$ for all simulation results in the main text. Note that the true strength of spin-orbit interaction in nanowires may differ from the parameters in a tight-binding simulation.

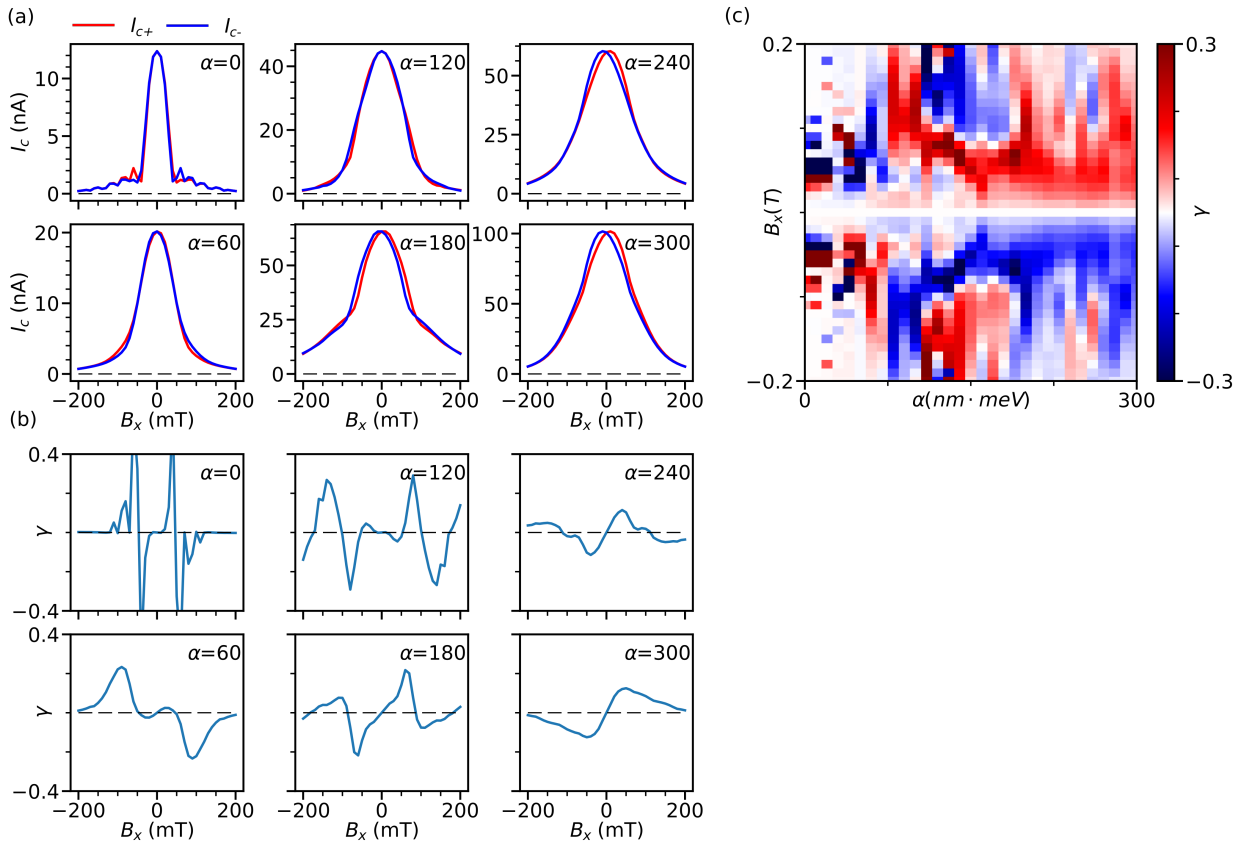

Figure 6.21: (a)Critical current as function of $\hat{x}$-field when strength of spin-orbit interaction $\alpha = 0, 60, 120, 180, 240, 300 nm \cdot meV$. The chemical potential $\mu = 8meV$. (b) Coefficient γ are extracted from (a) and plotted as function of B_x simulated with different α. (c)At same chemical potential, plot coefficient γ versus perpendicular field B_x and spin-orbit strength α as a 2D map to study how alpha affect skew shape.

6.13.3 Skew shape and field rotation simulation at another chemical potential

In the main text we present skewed diffraction pattern from Device A and rotation from Device B (field rotation was not performed for device A). Thus simulation at two separate chemical potential should be considered in preparing this report. To maintain consistency of simulation, we choose $\mu = 8$meV for the simulation in the main text, Fig. 6.5. Here we

show simulation results at $\mu = 20$meV here.

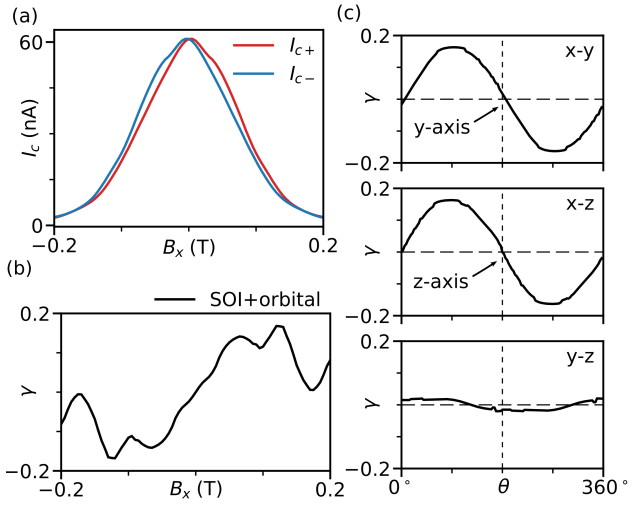

Figure 6.22: Numerical results from the KWANT simulation with same parameters used in Fig. 6.5 but with another chemical potential $\mu = 20meV$. This chemical potential is corresponding to four transverse or eight spin-full modes. (a) Critical current flow through each polarization as a function of magnetic field B_x. (b) Coefficient γ as a function of B_x, the magnitude of I_c is derived from (a). (c) Coefficient γ as a function of angle θ when the external field is rotating in three orthogonal planes with fixed strength $|B| = 50$mT.

6.14 Current phase relation derived from simulation results

The current phase relation (CPR) is studied within the model and its parameters suggested by comparison with experiment. We plot the CPR curve when the strength of the external field is 0T, 0.05T, 0.1T in B_x, B_y and B_z directions [Fig. 6.23]. Parameters used in this simulation is same as that in Fig. 6.5 in main text. In Fig. 6.23(a), we find that only when the external field is along $\hat{x}$-direction, there is a shift of the ground state phase in CPR. The numerical CPR curves are similar to those postulated in the phenomenological model (Eq. 6.1 and Fig. 6.1).

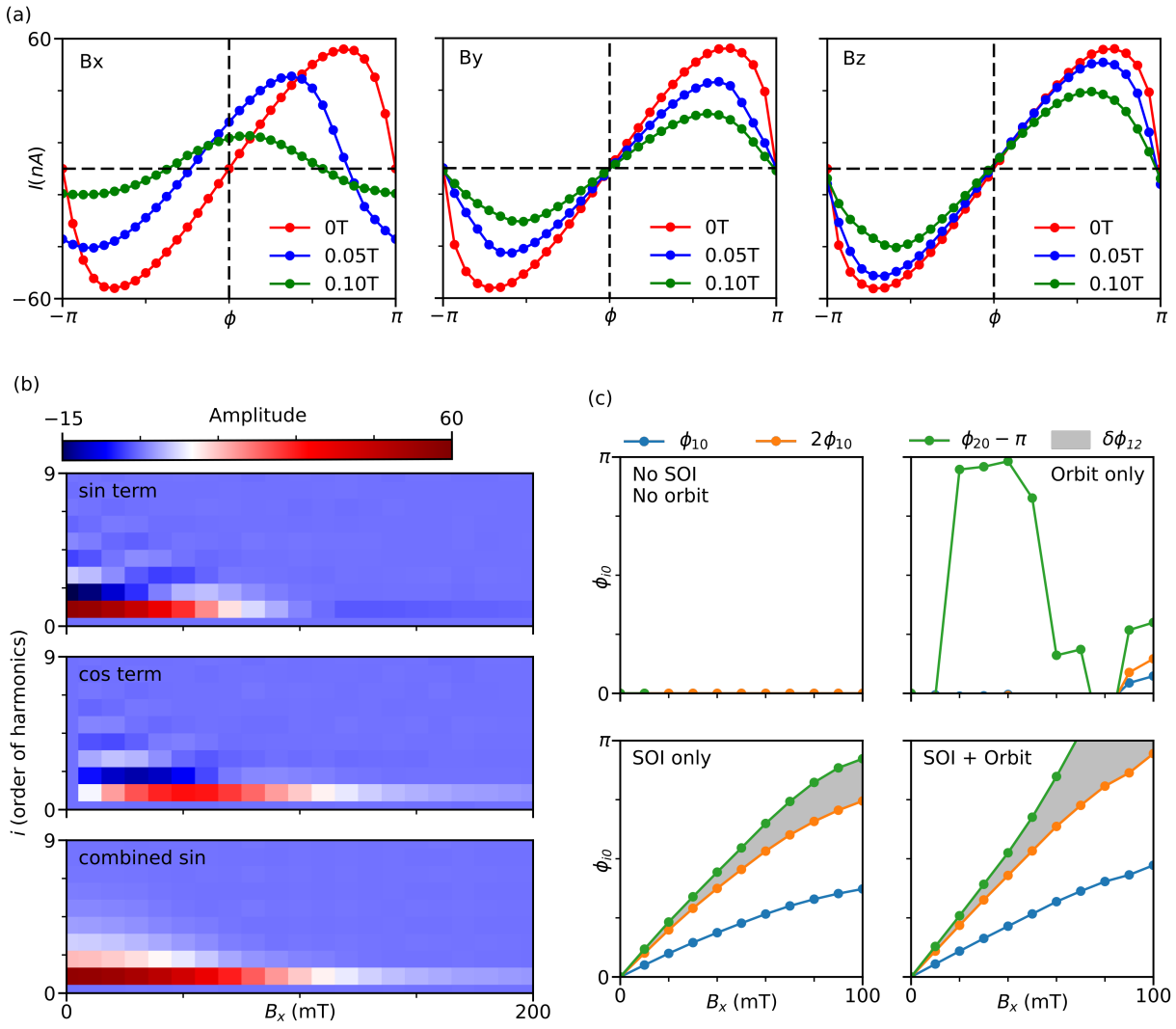

Figure 6.23: (a) CPR when external field is along three directions related to the device at field strength equals to 0T, 0.05T and 0.1T. (b) Amplitude of Sine and Cosine terms that are derived from Fourier expansion of CPR when external field is along $\hat{x}$-direction. The combined sine term is plotted as function of B_x field and order of harmonics. (c) Ground state phase ϕ_{n0} at the first and the second order of combined sin harmonics as function of external field B_x. A constant π was subtracted from all second order harmonics but has no effect as second order harmonic has a period of π.

To study how the time-reversal symmetry is broken when external field is along $\hat{x}$-

direction. We first perform a Fourier expansion with the simulated CPR [Fig. 6.23(b)]. We find there is a significant second order sin term in the simulation. What's more interesting is the first and second order cos terms are also large compared to the sin term and they are first increasing when field is applied but decreasing at higher field. This explains why the phase of ground state shift by such a large value. It is known that harmonics functions can be combined into a sine using the following:

$$\sum_{i=1} A_i \sin(i\phi) + \sum_{i=0} B_i \cos(i\phi) = \sum_{i=1} A'_i \sin(i\phi + \phi i0) + Constant \tag{6.15}$$

Here we find constant is contributing less than 2% of the combined function in any case, so we drop it. We find the amplitude of first and second order of combined sin function has a ratio about 4:1 when field strength is near zero. This ratio is used in the minimal model presented in the main text.

Another interesting result is when we study the ground state phase ϕ_{i0} in the first and second harmonics, we find they are increasing linearly with B_x field within the range 0-100mT. This was mentioned in [36] but here we provide more details. Based on the simulation, we get $\phi_{20} > 2\phi_{10}$ and the grey shadow region is indicating the δ_{12} increase in with field. Hence we can confirm there is a $\delta\phi$ term in the CPR from the simulation. How this $\delta\phi$ related to the strength of spin-orbit interaction is worth a further discussion in future works.

6.15 Temperature dependence of skewed diffraction patterns

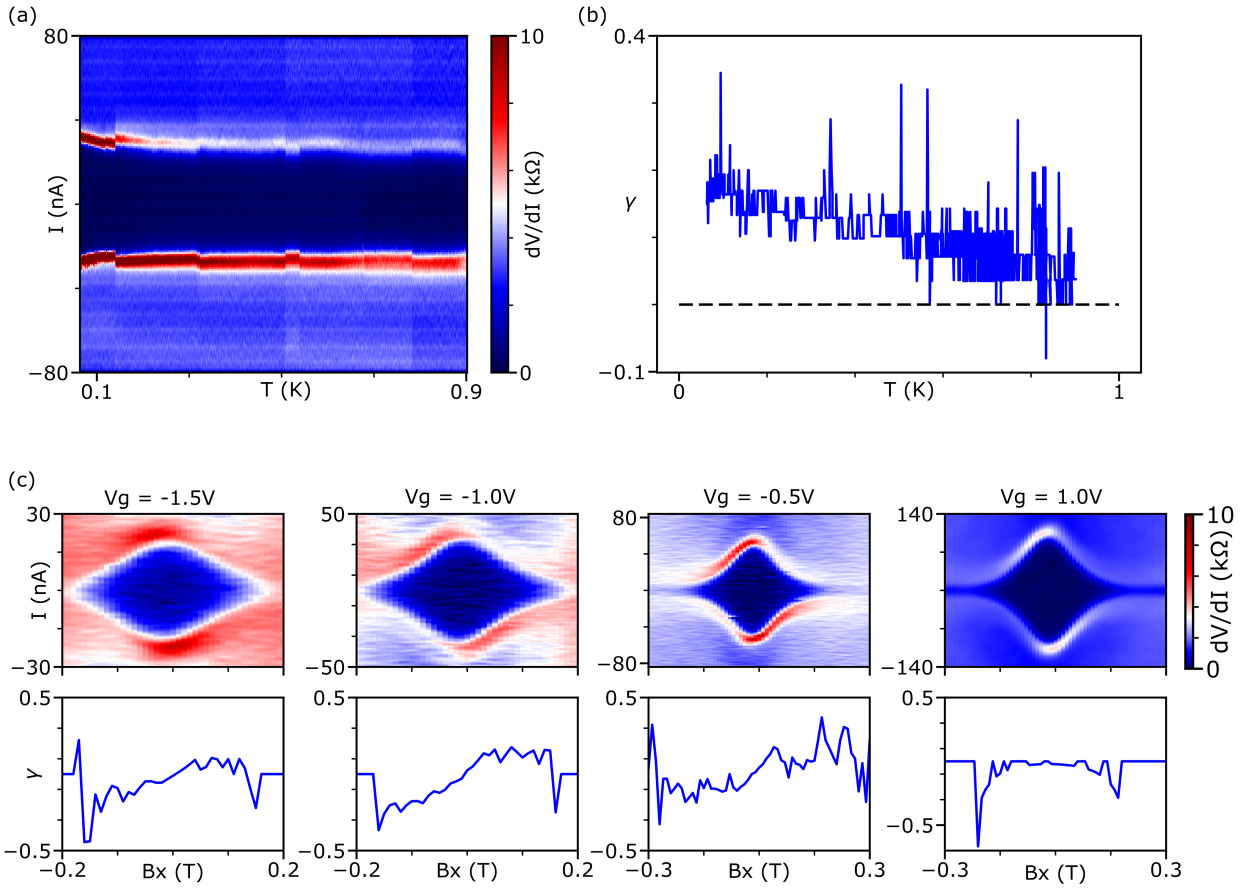

Figure 6.24: Temperature dependence in Device A. (a) For $V_{gate} = -2V$ and external field $B_x = 50mT$. dV/dI differential resistance is plotted as function of current source I and temperature T. (b) Coefficient γ is plotted as function of temperature T. (c) Diffraction patterns taken at T=1.1K, γ is extracted from 2D scan results and plotted as function of B_x

6.16 Gate dependence of skew in device C

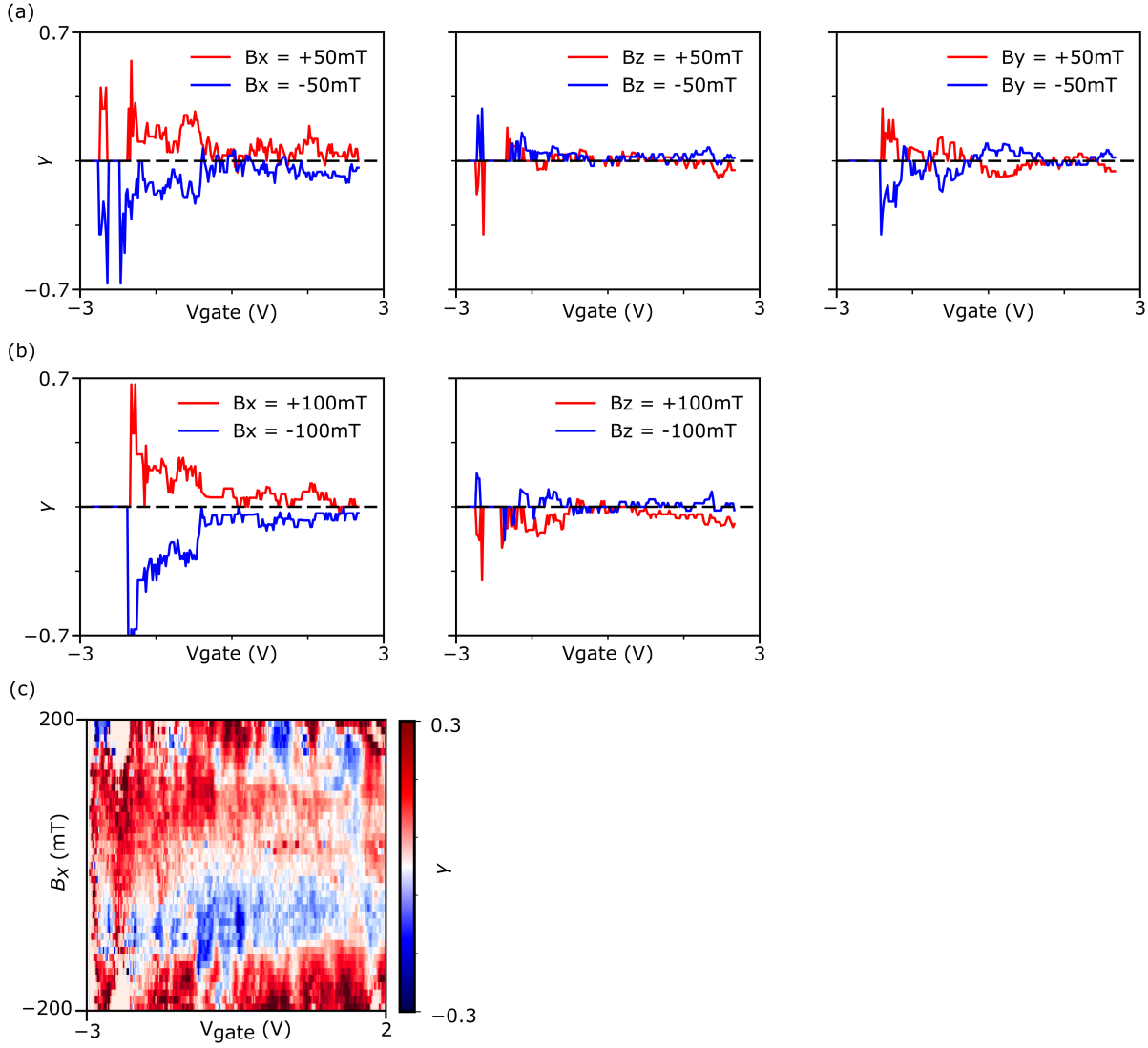

Figure 6.25: Coefficient γ as function of V_{gate} in different external field B. (a) External field with fixed strength $|B| = 50mT$ and along $\hat{x}$, $\hat{y}$, and $\hat{z}$ axis. (b) External field with fixed strength $|B| = 100mT$ and along $\hat{x}$ and $\hat{z}$ axis. (c) The 2D B_x versus V_{gate} map of coefficient gamma of Device C. The gate voltage range is corresponding to the chemical potential $\mu = 6 - 30meV$

7.0 CdTe-InSb nanowires[1]

Indium antimonide (InSb) nanowires are used as building blocks for quantum devices because of their unique properties, that is, strong spin-orbit interaction and large Landé g-factor. Integrating InSb nanowires with different materials could potentially lead to innovative devices with distinct functionalities. A notable instance is the combination of InSb nanowires with superconductors in the magnetic field for the topological research. This study examines the combination of II–VI cadmium telluride (CdTe) and III–V InSb in the form of core-shell (InSb–CdTe) nanowires, exploring potential applications based on the electronic structure of the InSb–CdTe interface and the epitaxy of CdTe on InSb nanowires. The electronic structure of the InSb–CdTe interface is determined using density functional theory, revealing a type-I band alignment with a small conduction band offset ($\leq$ 0.3 eV). These findings suggest potential applications of these shells for surface passivation or as tunnel barriers in conjunction with superconductors. Regarding structural quality, it is shown that lattice-matched CdTe can be grown epitaxially on InSb nanowires without interfacial strain or defects. As evidenced by the comparable field-effect mobility measured for both uncapped and CdTe-capped nanowires, these shells do not introduce disorder to the InSb nanowires.

7.1 Introduction

Semiconductor nanowires with strong spin-orbit coupling and a large Landé g-factor have opened up novel research pathways in quantum transport, spanning from spin phenomena [149, 150, 151, 152] to quantum computing circuits [153, 103, 154] and, more recently, the pursuit of topological particles [24, 155, 156]. Among these semiconductors, indium antimonide (InSb) boasts the highest bulk electron mobility, largest Landé g-factor, and strongest spin-orbit coupling compared to other III-V materials [157, 158]. However, the

[1]This chapter has been adapted from a collaborative work between our team and TU Eindhoven, as published in Ref. [148].

realization of defect-free and strain-free heterostructures of InSb with other materials has been challenging due to the large lattice constant of InSb.

In this context, cadmium telluride (CdTe) is an interesting material candidate, as it nearly matches the large lattice constant of InSb, with a lattice mismatch below 0.05% at room temperature. Additionally, their thermal expansion coefficients are comparable [159]. CdTe has a large bandgap compared to InSb, making it an attractive option for device applications such as quantum-well lasers, high electron mobility transistors, and infrared detectors [160, 161]. Despite the nearly perfect lattice match, the growth of CdTe-InSb heterostructures remains complicated due to preferential interface reactions that lead predominantly to the formation of an indium-tellurium-rich interface region [162]. The formation of such a layer is undesirable since different compositions of this indium telluride compound have different lattice constants and bandgaps [162]. The ease of twin formation in CdTe crystals [163, 164], further complicates the realization of defect-free interfaces.

In this study, we combine InSb and CdTe in a core-shell (InSb-CdTe) configuration for potential applications, focusing on the electronic structure of the InSb-CdTe interface, structural quality, and epitaxy of CdTe shells on InSb nanowires. We use density functional theory (DFT) calculations to investigate the electronic structure of InSb-CdTe, extracting both the bandgaps and band-edge alignment at the interface. We demonstrate that the InSb-CdTe interface's electronic structure is well-suited for passivating the InSb surface through type-I band alignment and serving as a tunnel barrier when positioned at the interface between the InSb nanowire and a metal or superconductor, due to a small conduction band offset of approximately 0.3 eV.

In the context of engineering topological superconductors using super-semi nanowire hybrids, a CdTe tunnel barrier could potentially minimize disorder and address the strong-coupling issue between the superconductor and nanowire. Disorder in these nanowire hybrids can mimic the signatures of topological particles [28, 165], and an overly strong coupling may overshadow the semiconducting nanowire's intrinsic properties, possibly rendering topological superconductivity inaccessible [166, 167]. Growth of CdTe shells at the interface between the nanowire and a superconductor with the extracted conduction band offset could modulate the superconductor-semiconductor coupling strength.

Aside from the electronic structure of the InSb-CdTe interface, the crystal quality of the interface and CdTe shells is crucial for device applications. Defected shells could induce strain in the InSb nanowire and introduce new sources of disorder, potentially impairing the performance of core-shell nanowires [168, 169]. Consequently, we demonstrate the growth of defect-free, epitaxial CdTe shells with a smooth and abrupt interface to InSb nanowires. Optimized growth parameters suppress interface reactions, preventing the formation of interface layers.

Furthermore, the CdTe shell prevents oxidation of the InSb nanowire surface, eliminating the need for harsh chemical treatments to remove surface oxides during device fabrication. We determine that the CdTe shells are chemically stable against oxidation, remaining oxide-free for at least three weeks. This property simplifies device fabrication, especially in devices where CdTe needs to be contacted, such as tunnel barrier devices. In these cases, the metal or superconductor can be directly deposited on the CdTe without exposure to etchants and harsh chemicals. We validate the quality of the grown shells through transport measurements, obtaining comparable electron mobility values for both bare, uncapped, and CdTe-capped InSb nanowires, confirming that these shells do not introduce additional disorder to the nanowires.

7.2 Electronic structure of the InSb-CdTe interface

The electronic structure across the interface between InSb and CdTe is characterized using ab initio DFT calculations. The atomic structure of the interface (i.e., the supercell) and selected results from the DFT calculations are graphically presented in Fig. 7.1(b). Based on experimental inputs derived from the structural and composition analysis of the grown shells, the supercell, shown in the middle panel of Fig. 7.1(b), is created. Accordingly, the interface is oriented perpendicular to the <110> crystal direction, consistent with the CdTe coverage of the six equivalent {220} facets outlining the hexagonal cross-section of an InSb nanowire (Fig. 7.1). The supercell also accounts for the polarity of the InSb-CdTe interface, as discussed in Sec. 7.4, with Cd taking the position of In, and Te that of Sb.

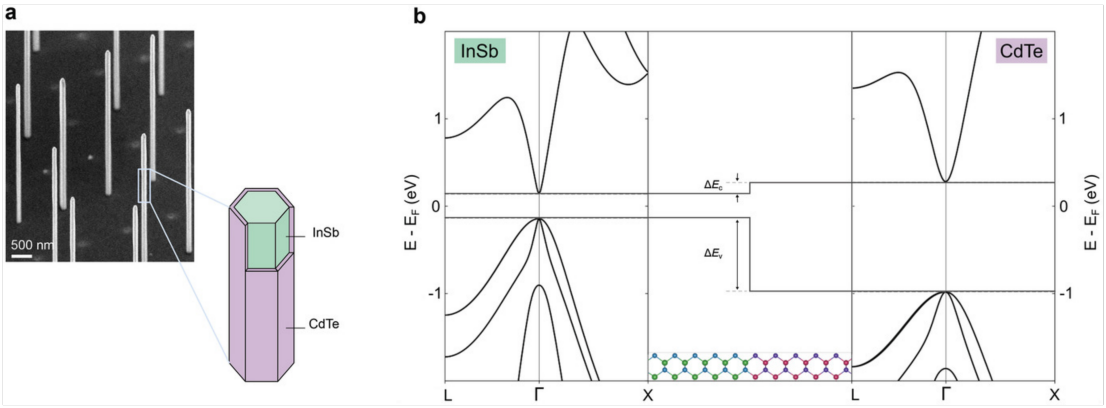

Figure 7.1: CdTe-capped InSb nanowires and the electronic structure of the InSb–CdTe system. (a) CdTe shells on InSb nanowires imaged at a 30°-tilt with a scanning electron microscope (SEM). The schematic highlights the InSb core (green) surrounded by a CdTe shell (purple). For illustration purposes, the CdTe shell is removed on two facets to expose the InSb. (b) On the left and right are the bulk band structures of InSb and CdTe, respectively, as obtained from density functional theory. In the central panel, the supercell composing the InSb–CdTe interface is shown with the band alignment. The potential difference between both materials is extracted from the averaged local electrostatic potential and is used for the alignment of both bandgaps at the interface. The band edge alignment has a conduction band offset ΔE_c = 0.15 eV and a valence band offset ΔE_v = -0.84 eV

The nearly perfect lattice match allows for the assumption that both InSb and CdTe have the same lattice constant. This is substantiated by our observations of the absence of strain in the grown shells (see Sec. 7.4). Therefore, an ideal interface is assumed, with the supercell's lattice constant set to the experimental value of CdTe. Additional calculations, details, and results are provided in Section S1, Supporting Information.

The results in Fig. 7.1(b) display the individual bulk bandgaps of both InSb and CdTe, as well as the band alignment at the heterostructure interface, i.e., the supercell. The potential difference at the interface, calculated from the local electrostatic potential of the supercell, is used to shift the InSb and CdTe bands, resulting in the shown alignment. This alignment is commonly referred to as type-I, with the InSb band-edges lying between those of CdTe. From the band-edge alignment, a conduction band offset ΔE_c = 0.15 eV and valence band offset ΔE_v = -0.84 eV are extracted. Since the bandgap of CdTe is slightly underestimated compared to experimental values, ΔE_c is correspondingly underestimated by approximately 0.2 eV. In contrast, the valence band offset is in good agreement with reported experimental values and theoretical calculations [162, 170, 171, 172]. However, there has been little consensus on the accurate value of the conduction band offset. Estimations based on the electron affinity rule give an offset of roughly 0.3 eV [173, 174].

7.3 Oxidation of InSb

The InSb nanowires studied here were grown using the vapor-liquid-solid technique on masked InSb (111) B substrates with gold catalysts defined by electron-beam lithography, as described in [60]. This results in uniform arrays of nanowires, as shown in Fig. 7.1(a). To prevent the InSb nanowires from oxidizing, we first attempt to transfer them from the metal-organic vapor phase epitaxy (MOVPE) growth environment to the molecular beam epitaxy (MBE) cluster, where CdTe is deposited, under nitrogen overpressure. Unfortunately, the nitrogen environment with low oxygen levels ($<$ 1 ppm) is insufficient to prevent InSb nanowire oxidation.

This oxidation is evidenced by a dark contrast layer between the InSb core and CdTe shell

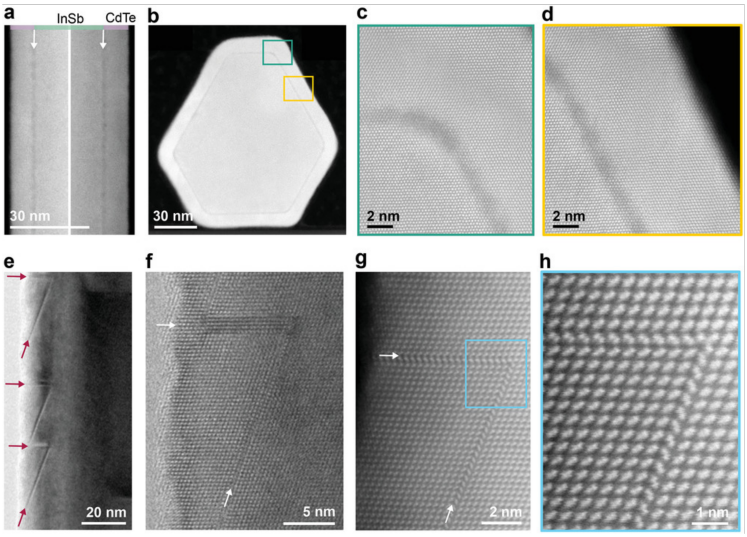

Figure 7.2: The impact of interfacial oxides. (a) STEM images of the two opposing sides of the same nanowire imaged along the <112> zone axis show a dark layer between the CdTe shell and the InSb core, indicated by the arrows. The dark layer is attributed to InSb oxides, appearing darker because they are of a lower electron density. (b) A cross-section of a nanowire imaged along the <111>zone axis shows this oxide layer is all-around, where high magnifications of the interface in (c) and (d) indicate that the limited thickness of this oxide layer still allows for epitaxy between InSb and CdTe. (e) Despite epitaxy, defects in the CdTe shell are detectable (indicated by arrows) with high-resolution transmission electron microscopy (TEM) along the <110> zone axis. Two directions of planar defects are present, both parallel to {111} B planes: orthogonal to the long axis and at roughly 19° from the long axis. Different combinations of twinned layers in each direction occur. (f) In the orthogonal direction four twinned layers are visible and in the inclined direction only a single pair of twin boundaries. (g) Pairs of twin boundaries in each direction. HAADF-STEM scans show that the defect starts at a specific point and then expands by two double {111} twin planes at a 71° angle. (h) A high-magnification scan of the starting point of the defect clearly reflects the interrupted crystal structure by the two twins.

in scanning transmission electron microscopy (STEM) images (Fig. 7.2(a)-(d)) and leads to defect formation (Fig. 7.2(e)-(h)). The high defect density observed in the CdTe shell of Fig. 7.2(e)-(h) is consistent with reports of oxide presence on InSb surfaces affecting CdTe layer quality [175]. The nanowire cross-section in Fig. 7.2(b), which displays a uniformly thick CdTe shell of 7 nm, suggests that this dark-contrast oxide layer is present all around the InSb nanowire. However, high-magnification images of the interface near a corner and parallel to a facet (Fig. 7.2(c), (d)) indicate that the oxide layer is not fully formed, as local atomic column continuity from the core to the shell is still visible. Moreover, the oxide layer is not thick enough to disrupt the epitaxial connection.

Despite the limited thickness of this oxide layer, it still triggers twin defects in the CdTe shell. As shown in Fig. 7.2(e)-(h), the twin defects are oriented parallel to {111} planes, either perpendicular or inclined by approximately 19° with respect to the nanowire's long axis. In either direction, twinned layers appear in pairs or multiples, maintaining the lattice orientation. Furthermore, high-angle annular dark field (HAADF) STEM scans (Fig. 7.2(g), (h)) reveal that the defect expands from a given point by double {111} twin planes forming a 71° angle.

7.4 Epitaxy of CdTe Shells

To prepare InSb nanowires for defect-free epitaxial CdTe shells, it is crucial to remove any surface oxides. In this study, we clean the InSb nanowires with atomic hydrogen in an MBE chamber before growing the CdTe shells. Atomic hydrogen is known to effectively eliminate surface oxides from III-V semiconductors without altering stoichiometry or inducing roughness [176, 177]. In addition to preserving the pristine quality of the InSb nanowires, atomic hydrogen cleaning within an MBE system offers the benefit of ultra-high vacuum conditions throughout the entire process, from cleaning to CdTe growth, ensuring that the nanowires remain oxide-free after cleaning.

The parameters used for oxide removal with atomic hydrogen must be carefully adjusted, as improper parameter selection can negatively impact the quality of both the InSb nanowires

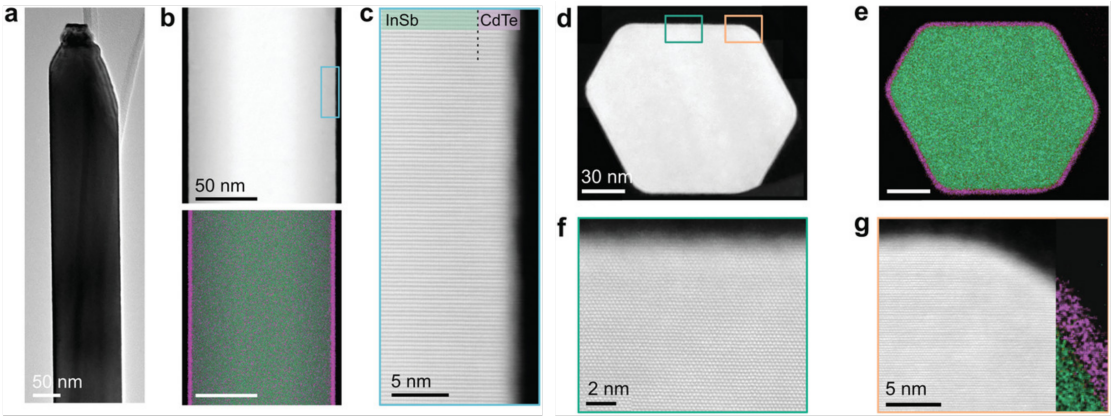

Figure 7.3: Growth of epitaxial uniform CdTe shells. (a) A representative CdTe-capped InSb nanowire imaged with TEM along the <112>zone axis. (b) A HAADF scan of a nanowire segment (<112>zone axis) along with an energy dispersive X-ray (EDX) map of a uniform CdTe shell (purple) around an InSb nanowire core (green). (c) A zoom-in on the framed region conveys epitaxy from core to shell, where the interface is virtually indistinguishable. (d) A cross-sectional HAADF scan accompanied by (e) an EDX map shows a 2.5 nm full shell and two high magnification images, (f) parallel to a facet and (g) along the corner. Both reveal the abrupt interface and epitaxy between the InSb and the CdTe. In (g), an EDX map is overlaid to identify the CdTe and the In.

and the deposited CdTe shells. On one hand, relatively low temperatures ($< 200°C$) are insufficient to fully remove the native oxides, resulting in the growth of defective CdTe shells. On the other hand, higher temperatures ($> 300°C$) can compromise the quality of the InSb nanowires by causing surface roughness (see Figure S1, Supporting Information). Optimized cleaning parameters enable the growth of defect-free epitaxial shells without interfacial oxides, as demonstrated in Fig. 7.3. Detailed information on atomic hydrogen cleaning can be found in Section S2, Supporting Information.

Following oxide removal, CdTe is deposited from two separate cells: a Cd effusion cell and a Te cracker cell. The base pressure in the chamber during growth is approximately 1×10^{-9} Torr. To suppress the formation of interface reactions, which can result in Te-rich interface layers, three key considerations are necessary.

First, the nanowires are exposed to a Cd flux for 3 minutes before introducing Te. Second, growth proceeds under Cd-rich conditions with a II/VI flux ratio of 3. It is important to note that a high II/VI flux ratio alone is not sufficient to prevent the formation of Te-rich compounds at the core-shell interface. Specifically, shells deposited without pre-exposure to Cd exhibit a Te-rich interface layer, as measured by atom probe tomography (APT) (see Section S3, Supporting Information). These Cd-rich conditions do not affect shell stoichiometry due to the low sticking coefficient of Cd and its high vapor pressure, which is four orders of magnitude higher than Te [162].

Third, relatively low growth temperatures ($T\approx120–150°C$) are employed to ensure that interdiffusion processes do not occur between the InSb and deposited CdTe. Additionally, to promote smooth CdTe shell growth, low Cd and Te fluxes are used, resulting in a growth rate of ≈0.002 monolayers s^{-1}. Higher growth rates lead to defective and rough shells. While higher temperatures improve selectivity due to longer adatom diffusion lengths—evidenced by the absence of CdTe deposition on the silicon nitride mask covering the nanowire substrate—they cause thermal etch pits in both the InSb nanowires and substrate. The formation of these etch pits in InSb surfaces at elevated temperatures has been reported and can be minimized with an antimony overpressure [178]. The thermal etch pits formed in the nanowires compromise their structural integrity, causing them to bend (Figure S3, Supporting Information). Consequently, low growth temperatures and fluxes are used to achieve

defect-free epitaxial CdTe shells.

For example, Fig. 7.3(a) displays an overview bright field transmission electron microscopy (BFTEM) image of an InSb-CdTe core-shell nanowire. The virtually indiscernible interface between the InSb and CdTe in HAADF-STEM imaging (Fig. 7.3(b), (c)) is attributable to not only the absence of any interface layers but also the similar atomic numbers of all the constituent elements—indium, antimony, cadmium, and tellurium—in both the core and shell. As a result, EDX spectroscopy mapping (Fig. 7.3(b)) is employed to determine the thickness of the grown shells. The thickness of this specific shell is 2.5 nm and is uniform along the entire nanowire length. Furthermore, Fig. 7.3(c) reveals the defect-free epitaxy extending from core to shell. Cross-sectional studies of the nanowire allow for the investigation of shell quality orthogonal to the long axis, as shown in Fig. 7.3(d)-(g). The accompanying EDX map demonstrates the uniform CdTe shell thickness on all six facets. This uniform, full shell is achieved by rotating the substrate during CdTe growth. High-resolution imaging along the <111> zone axis confirms the high quality and defect-free epitaxy in the middle of a facet and at a corner. It is worth emphasizing that no visible contrast exists between the core and shell, indicating abrupt epitaxy between InSb and CdTe without an interfacial layer.

7.5 Atomic analyze of CdTe

The epitaxy is clearly detectable in the high-magnification scans taken along the <110> zone axis of the HAADF scanning mode, as shown in Fig. 7.4(a), where both InSb and CdTe exhibit recognizable zinc blende structures. Atomic-resolution composition mapping of the shell, obtained through atomic-resolution EDX in Fig. 7.4(b), displays the positions of the core and shell elements. These mappings demonstrate that the CdTe mirrors the polarity of the InSb nanowire. Specifically, the (111) B layers orthogonal to the growth direction are terminated by antimony atoms, consistent with the (111) B substrate orientation. Correspondingly, the (111) B planes of the shell are terminated by Te atoms, with Cd assuming In's position (Fig. 7.4(b)). This polarity is further evidenced by atomic profiles taken along

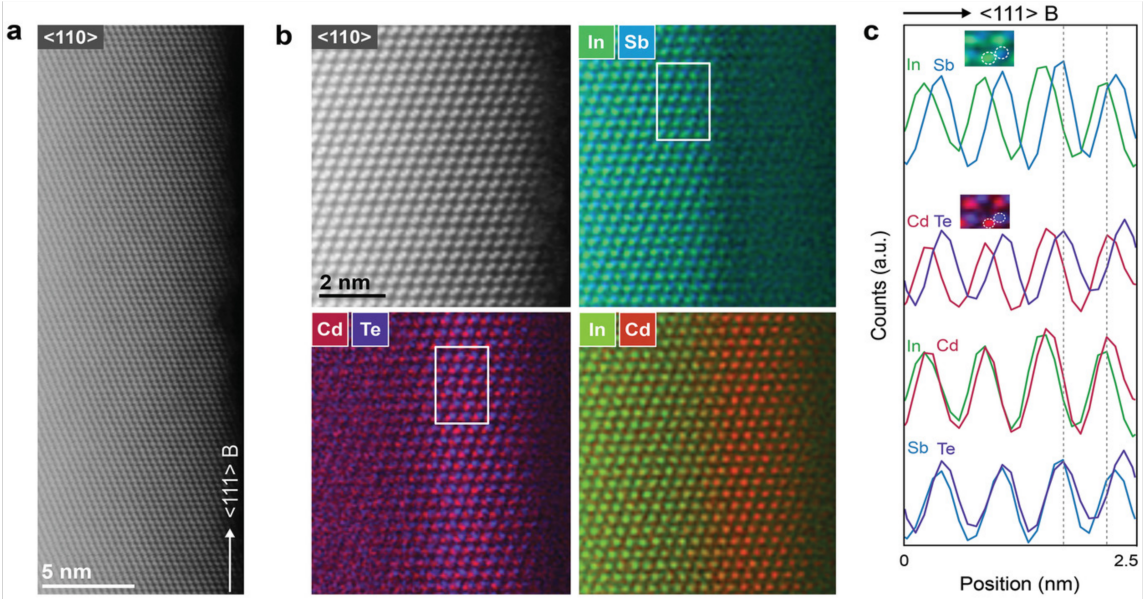

Figure 7.4: Atomic structure and composition of the CdTe shells. (a) An InSb nanowire covered with a 2.5 nm CdTe shell imaged with HAADF-STEM along the <110> zone axis, as specified. (b) A high magnification scan of (a) demonstrates the ABC stacking of the zinc blende crystal of both InSb and the epitaxial CdTe. Accompanying atomic resolution EDX maps reveal the positions of the elements composing the CdTe shell and InSb core along the <111> B growth direction. (c) Framed regions in (b) indicate along which areas the atomic profiles are taken. Integrating over the region yields the projection of the atomic positions on one line along the <111> B. Inset are two high magnification images of the atomic resolution EDX maps, InSb and CdTe, to highlight the atomic positions of the elements in the core and shell. The atomic resolution EDX maps and the atomic profiles display the polarity of the shell with respect to the core, with Cd taking the position of In and correspondingly, Te that of Sb. This is further demonstrated by the absence of a shift in the line profiles of In (Sb) and Cd (Te), as highlighted by the vertical dashed lines.

the InSb core and the CdTe shell, where the projection of atomic positions along the <111>B direction indicates spatial overlap between In and Cd, as well as Sb and Te in Fig. 7.4(c).

Upon close examination, the shells show no signs of oxidation (scans taken at least three weeks after shell growth), as evidenced by the absence of atomic columns bound by low-electron density material or amorphous structures. The inert nature of CdTe contrasts sharply with InSb, which is highly susceptible to oxidation even at very low oxygen levels. This susceptibility highlights the significance of the shells, as they effectively prevent the formation of surface oxides around the InSb nanowires.

The structural quality of these shells is assessed for strain. As anticipated due to the near lattice match, the shells are relaxed, as confirmed by strain mapping provided in Figure S4 of the Supporting Information. A relaxed shell suggests a large critical thickness, on the one hand, which is consistent with defect-free shells for the range of studied thicknesses up to 15 nm. On the other hand, the non-strained interface further confirms the absence of interface layers, since the commonly formed interfacial indium- and tellurium-rich compounds exhibit a lattice mismatch of approximately 5% with InSb [162].

Adjusting the CdTe shell thickness is easily achieved by modifying the growth time, with a linear approximation of the growth rate yielding approximately 5.4 nm h^{-1}. We investigate shells with thicknesses ranging from 2.5 to 12 nm. It should be noted that for shell thicknesses exceeding 5 nm, slight roughness is observed with TEM along the <110> zone axis (Figure S5, Supporting Information). Imaging the same shell along the <112> zone axis does not reveal this roughness, as images are taken parallel to a roughly 100-nm-long nanowire facet, projecting aggregated nanoscale roughness onto the image plane. In contrast, viewing along the <110> zone axis generates an image of the corner between two facets, exposing any atomic scale roughness at the corners. This roughness appears in projections at edges orthogonal to a <111> direction. Although the precise topography and features of this roughness cannot be determined, it may be related to CdTe's tendency to form {111} facets with increased layer thickness, as described in [179, 180].

Ultimately, growth is halted by closing both the Cd and Te shutters, allowing the cool down process to proceed without any fluxes. In fact, cooling down under a Te flux at low growth temperatures, such as 120–150°C, results in the deposition of Te-rich CdTe globules

on the nanowire facets, as shown in Figure S6 of the Supporting Information.

7.6 Electric Characterization of the InSb–CdTe Core–Shell Nanowires

The effectiveness of the epitaxial CdTe capping is assessed by conducting electron transport measurements on the core-shell nanowires. It is important to note that we have not evaluated the tunnel barrier properties of the shell but have instead examined the basic field-effect transistor (FET) characteristics of the core-shell wires. While there are limitations to mobility extraction from FET measurements in nanowires, which could result in imprecise mobility values [181, 182], FET measurements remain a widely used technique for characterizing nanowires [183, 184, 185, 59]. We perform FET measurements at 4 K to determine the mobility μ, with a typical device shown in the inset of Fig. 7.5(a). Approximately 60 FET devices are fabricated with core-shell nanowire diameters of around 120 nm. Degenerate p-doped silicon substrates covered with silicon oxide (SiO2) and hafnium oxide (HfOx) function as a global back gate, while titanium/gold contacts serve as the source-drain electrodes.

Directly depositing the source-drain contacts onto the CdTe shells, for the studied shell thicknesses of 4 to 12 nm, results in an open circuit, indicating that these shells act as effective insulators. Therefore, before depositing the source-drain electrodes, the CdTe is locally etched using argon milling to establish contact with the conductive InSb core. Additional details on device fabrication are provided in Section S8 of the Supporting Information. The source-drain contact separations are $L = 1$, 2, 3, and 5 μm to ensure the long-channel diffusive transport regime. Moreover, these large separations ensure that any damage caused by the argon milling near the source-drain contacts is eliminated, and the measurements reflect the behavior of the segment between the contacts. Back-gate voltage sweeps $I(V_{BG})$ for the studied channel lengths and a fixed CdTe shell thickness of 4 nm are illustrated in Fig. 7.5(a). Field-effect mobility values are extracted from fits of the pinch-off curves (Section S9, Supporting Information). The majority of the obtained mobility values range from 1.0 to $2.7{\times}10^4$ cm$^2/V \cdot s$, and no significant difference is observed compared to uncapped, bare

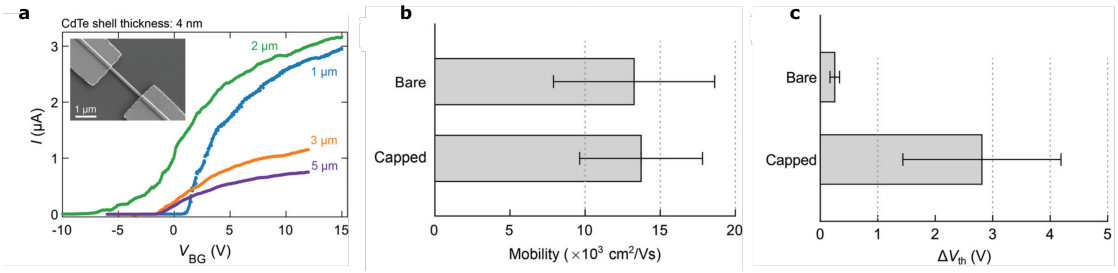

Figure 7.5: Mobility in CdTe-capped nanowires. (a) FET measurements at a bias voltage V_{dc} = 10 mV for four core–shell nanowires (CdTe thickness = 4 nm) with channel lengths L = 1, 2, 3, and 5 μm. Fitting these pinch-off curves yields mobility μ = 21.5, 26, 14, and 17×10^3 cm$^2/V \cdot s$ for 1, 2, 3, and 5 μm, respectively. Inset: SEM of a nanowire device. (b) The average mobility for 4-nm CdTe capped and bare InSb nanowires. Mobility is averaged for 1- and 2-μm channel devices. (c) Average hysteresis measured in 4-nm CdTe capped and bare nanowires and is averaged for 1- and 2-μm channel devices. Hysteresis is quantified by the threshold-voltage difference ΔV_{th} between the forward and backward gate-voltage sweeps.

InSb nanowires (Fig. 7.5(b)).

The comparable equivalent mobilities of CdTe-shelled and uncapped InSb nanowires suggest that the CdTe shell does not introduce additional disorder, thereby preserving the inherent properties of InSb nanowires. It is possible that thicker shells ($>$ 12 nm) may be necessary to passivate the nanowire surface and further confine electrons, akin to InSb quantum wells, where barrier layers of over 50 nm are needed to achieve high mobility [185]. However, thicker shells would be incompatible with a tunnel barrier at the interface between a semiconducting nanowire and a superconductor, as tunneling probability decreases exponentially with barrier thickness.

Although mobilities are similar for both CdTe-capped and uncapped InSb nanowires, a larger hysteresis is observed between forward and backward gate-voltage sweeps for the CdTe-capped wires, as demonstrated in Fig. 7.5(c). The hysteresis's origin is uncertain but could be attributed to point defects at the interface and within the CdTe shells, known to trap charges [186, 187]. Point defects lack lattice structure and are thus undetectable in our TEM analysis of CdTe shells. The relatively low substrate temperatures during CdTe growth could contribute to point defect formation, as could atomic hydrogen cleaning of the InSb surface, leading to point defects at the InSb-CdTe interface. Notably, extending the device space pumping duration from 24 to 96 hours slightly reduces hysteresis and marginally increases fitted mobility (Figure S7, Supporting Information). This modest improvement implies that the hysteresis is predominantly influenced by inherent features of the interface and CdTe shells, such as adsorbates associated with point defects and the point defects themselves.

7.7 Conclusion

We investigated the InSb-CdTe material system in a core-shell nanowire configuration for potential applications in surface passivation and tunnel-barrier devices. The suitability of these heterostructures for the intended applications was assessed based on the electronic structure of the InSb-CdTe interface and the quality of CdTe epitaxy on InSb cores. Notably, the prospect of employing these CdTe shells in hybrid superconducting-semiconducting

nanowire devices is proposed, owing to the high-quality InSb-CdTe interfaces and the small conduction band offset at this interface. Furthermore, the comparable field-effect mobilities of both uncapped and CdTe-capped nanowires indicate the CdTe shells' potential to modulate superconductor-semiconductor coupling without introducing disorder to the device.

Although we anticipated improved electron mobility in CdTe-capped nanowires compared to uncapped InSb wires, given the type-I band alignment of the InSb-CdTe interface, nearly perfect epitaxy, and high-quality interfaces, the observed similar mobility values suggest that thicker CdTe shells (> 12 nm) might be necessary to confine electron wavefunctions to the InSb core and achieve higher mobility. While thicker shells might be required for surface passivation, they are incompatible with tunnel-barrier devices due to the exponential decrease in tunneling probability as a function of barrier thickness. Combining both functionalities—surface passivation and tunnel barriers—in a single nanowire device could be achieved by growing asymmetrically thick shells, where the portion of the CdTe shell in contact with the metal or superconductor is thin, and the remaining nanowire facets are covered by a thick CdTe shell. Such hybrid nanowire devices, which would combine reduced disorder and improved mobility with tunable superconductor-semiconductor coupling, could potentially pave the way for a new generation of topological nanowire devices.

7.8 Supplementary Information

7.8.1 Density Functional Theory Calculation

All density functional theory (DFT) calculations are performed using the Vienna ab initio simulation package (VASP) [191]. These calculations employ the VASP implementation of the generalized Kohn-Sham scheme with the projector augmented-wave (PAW) method [192]. A plane-wave cutoff of 274.3 eV is utilized, and spin-orbit coupling is included in all calculations. While the results presented in the main text are obtained using the Heyd-Scuseria-Ernzerhof (HSE06) hybrid exchange-correlation functional [193], this section considers additional exchange-correlation (XC) functionals: Perdew-Burke-Ernzerhof

XC functional	E_g (InSb)	E_g (CdTe)	ΔE_v	ΔE_c
PBE	0.0	0.49	-0.63	-0.14
mBJ	0.24	1.57	-0.65	0.68
lmBJ	0.21	1.54	-0.68	0.65
HSE06	0.28	1.27	-0.84	0.15
experimental	1.45	0.49	-0.87	0.34*

Table 7.1: Bulk band structures and band offsets. Values are given in electron Volts (eV). Experimental bandgaps are obtained from [188, 189, 190]. The valence band offset is estimated from x-ray photoelectron spectroscopy in [160]. The asterisk signifies that the experimental ΔE_c is calculated from the experimental bandgaps and ΔE_v.

(PBE) [194], modified Becke-Johnson (mBJ) [195], and local mBJ (lmBJ) [196] (see Table. 7.1). For the bulk calculations, the lattice constants of InSb and CdTe are set to the experimental values of 6.479 °A and 6.482 °A, respectively [163]. These calculations provide the bulk bandgaps (E_g) of both materials. For the supercell calculation, each material is represented by 10 monolayers, i.e., 40 atoms in total, connected at a non-polar (110) plane, and the Brillouin zone is sampled using a Γ-centered $6 \times 6 \times 2$ k-point grid. The tabulated valence and conduction band offsets—ΔE_v and ΔE_c, respectively—are extracted using both the individual bulk calculations and the supercell calculation [197]. Specifically, from the supercell calculation, the potential offset, ΔV, between InSb and CdTe is obtained using a macroscopic average of the electrostatic potential. This value is then used to align the energy levels obtained from the two separate InSb and CdTe bulk calculations.

As illustrated in Table. 7.1, the PBE functional predicts InSb to be a metal, i.e., with a zero bandgap, and thus this standard exchange-correlation functional cannot be used to describe the system. The mBJ, lmBJ, and HSE functionals provide results that agree well with experimental values. In particular, HSE offers an accurate valence band offset compared to experiments but underestimates the bandgap of CdTe and accordingly ΔE_c by approximately 0.2 eV. Generally, the mBJ and lmBJ exchange-correlation functionals are

Parameter	Value
Substrate temperature	250°C
Hydrogen flow	20 sccm
Filament temperature	1200°C
Chamber pressure	2.5×10^{-5} Torr
Cleaning duration	45 minutes

Table 7.2: Atomic hydrogen cleaning parameters. The substrate temperature is measured on the surface of the temperature-reference chip. During the entire cleaning procedure the holder is rotated. When idle, the chamber pressure is roughly 6×10^{-10} Torr.

known to accurately describe bandgaps while being more numerically feasible than hybrid functionals, which holds true for InSb and CdTe. However, both underestimate ΔE_v and correspondingly overestimate ΔE_c by roughly 0.3 eV, consistent with calculations in [171].

7.8.2 Atomic Hydrogen Cleaning

Before depositing CdTe shells, it is crucial to remove the native oxides surrounding the nanowires to ensure epitaxy. Nanowire chips are initially adhered to a molybdenum holder alongside a gallium arsenide (GaAs) temperature-reference chip. The holder undergoes a two-hour degassing process at 300°C to eliminate water molecules and undesired adsorbates. Following degassing, the holder is placed in the cleaning chamber, with Table II outlining the pertinent cleaning parameters. Once the oxide is removed, the nanowire chips remain in the chamber until they cool down to 80°C and the chamber pressure reaches 3×10^{-9} Torr. The nanowire chips are subsequently transferred to the growth chamber through an ultra-high vacuum transfer tube.

A range of cleaning durations and substrate temperatures have been investigated, as illustrated in Fig. 7.6. Excessively high temperatures (> 300°C) result in roughness and damage to the InSb nanowire surfaces, while low temperatures prove insufficient for native

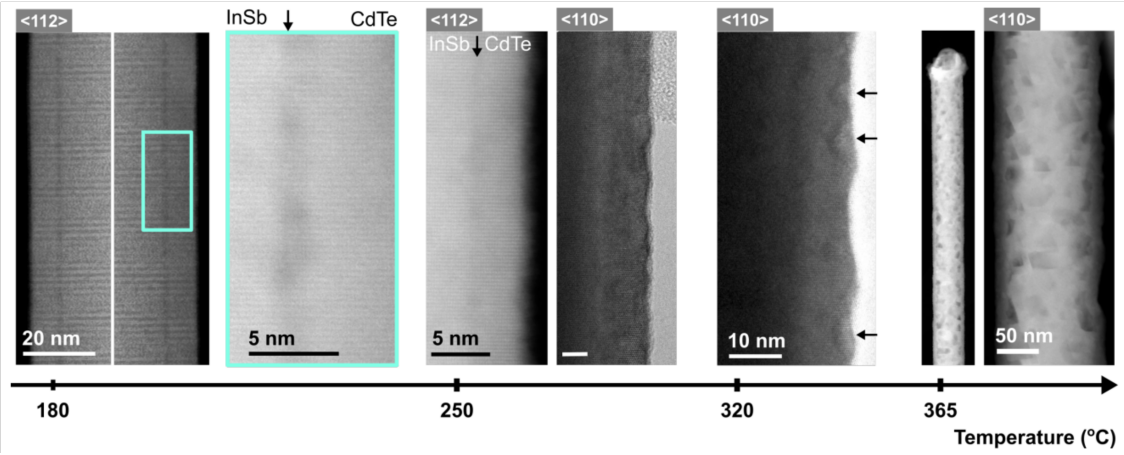

Figure 7.6: Effect of substrate temperature during atomic hydrogen cleaning of core-shell nanowires. Hydrogen cleaning of the InSb core at 180°C does not fully remove the oxide, as evident by the dark layer at the InSb-CdTe interface. A high magnification of the interface shows that this oxide layer is not of uniform thickness. At 250°C, this oxide layer is barely discernible and along the <110> zone axis, the shell is defect-free signifying that the oxides are mostly removed. While 320°C instigates the onset of roughness in the InSb, at 365°C structural damage of the nanowire is detectable. In high-angle annular dark field imaging at both the <112> and <110> zone axes, damage manifests as pits on the nanowire surface.

oxide removal. Residual oxides appear as a dark contrast at the InSb-CdTe interface in high-angle annular dark field (HAADF) imaging, indicative of a low electron-density material when compared to InSb and CdTe. Consequently, higher temperatures and extended cleaning durations have been employed to entirely eliminate the oxide, as the cleanliness of the InSb surface significantly impacts the quality of the grown CdTe shells [175]. Although defect density in CdTe shells is considerably reduced with optimized atomic hydrogen cleaning temperature and duration, signifying successful native oxide removal, a subtle dark interface contrast persists irrespective of cleaning conditions (Fig. 7.6: 250°C).

The enduring presence of this interface layer leads to the hypothesis that it may be arsenic (As) originating from the GaAs temperature-reference chip. Specifically, during atomic hydrogen exposure, the GaAs chip is also cleaned, potentially releasing As at these temperatures, which is then redeposited on the InSb nanowires. To verify the presence of As at the InSb-CdTe interface, atom probe tomography studies are utilized to examine the nanowires, as this interface layer is not detectable with elemental dispersive x-ray (EDX) spectroscopy.

7.8.3 Atom Probe Tomography Analysis

For the atom probe tomography studies, InSb nanowires were cleaned using atomic hydrogen at a substrate temperature of 250°C for 20 minutes, followed by the growth of a 50-nm CdTe shell. These shells were grown with a Cd/Te ratio of 3 and a Cd pre-exposure time of one minute. These cleaning and growth conditions produce results similar to those in Fig. 7.6: 250°C, exhibiting a very subtle dark contrast in high-angle annular dark field (HAADF) imaging. Consequently, we utilize the atom probe tomography results to refine the growth conditions and determine the origin of this darker interface layer to ultimately eliminate it. The atom probe tomography analysis results, presented in Fig. 7.7, confirm the presence of As at the InSb-CdTe interface. Additionally, extremely low levels of oxygen (approximately 0.03%) are detected. Notably, the dark interface layer is primarily attributed to a tellurium-rich layer, possibly Sb2Te. As depicted in Fig. 7.7(d), this Sb2Te concentration extends into the InSb, verifying the existence of a Te-rich interface region.

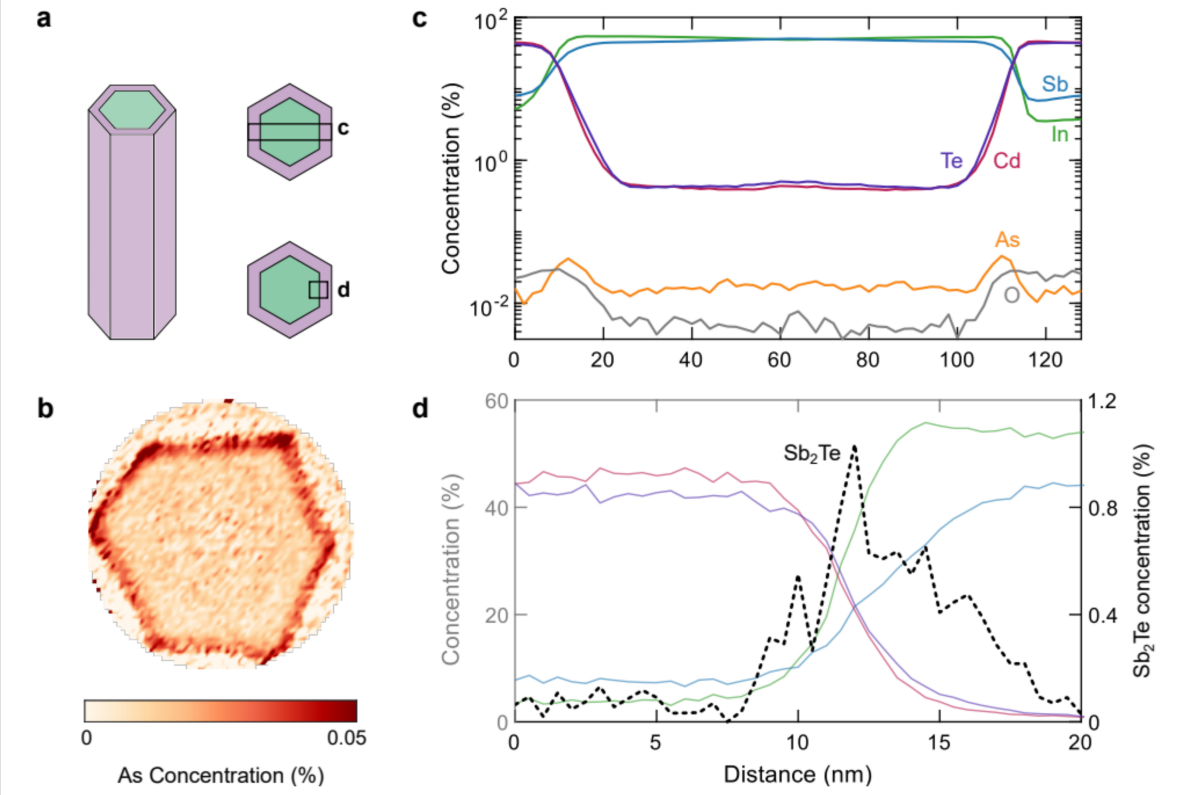

Figure 7.7: (a) A schematic of an InSb core (green) and a CdTe shell (purple) and two top-view images showing the analyzed profiles in c. and d., a rectangular profile along the entire diameter and an interface profile, respectively. (b) Two-dimensional mapping of the arsenic concentration, reflecting a slight enrichment at the core-shell interface. (c) This arsenic concentration is also visible along the rectangular profile with two peaks at the interface of about 0.04%. Roughly 0.03% of oxygen is also present at the interface. The overlapping regions between the InSb and the CdTe are not due to inter-diffusion but just peak overlaps. Within the detection resolution of roughly 0.1-1% limited by these peak overlaps, there is no measurable inter-diffusion. (d) An interface profile spanning a 20-nm region shows that Sb and Te are clustering up at the interface, forming a 3-4 nm thick layer. This layer contains Sb2Te ions created during atom probe tomography indicating a mixed interface region/layer that incorporates both Sb and Te atoms rather than an abrupt interface between InSb and CdTe.

To address the arsenic issue, a 50 nm silicon nitride mask is applied to cover the GaAs temperature-reference chip. This mask prevents the release of arsenic from the GaAs surface, thus minimizing arsenic re-deposition on the nanowire surfaces during atomic hydrogen cleaning. Concerning the oxygen levels, the cleaning duration is increased from 20 minutes to 45 minutes to ensure complete native oxide removal. To suppress the formation of the Te-rich interface layer, the growth chamber is flushed with Cd before introducing Te, as detailed in the main text. These optimizations in cleaning and growth parameters result in clean, smooth, and abrupt InSb-CdTe interfaces, as demonstrated by epitaxial shells devoid of dark-contrast interfacial layers, as discussed in the main text.

7.8.4 CdTe Growth

The growth of CdTe shells occurs at relatively low temperatures, for example, 120°C, since higher temperatures ($\approx$ 250°C) lead to rough and defected shells (Fig. 7.8) and are known to encourage interface reactions between InSb and CdTe. Temperatures exceeding 300°C jeopardize the structural integrity of the InSb nanowires. As illustrated in Fig. 7.8, high temperatures trigger the release of Sb from the nanowires and the InSb substrate. This Sb liberation manifests as pits in both the nanowires and the substrate, causing the nanowires to bend. These elevated temperatures also increase the adatom surface-diffusion length, which is evident by the absence of deposition on the masked substrate surface. In contrast, at the optimal growth temperature of 120°C, the substrate surface is coated with a CdTe layer.

7.8.5 Strain Mapping

The InSb-CdTe core-shell nanowires are characterized to assess whether the interface is under strain.

For this, an atomic resolution HAADF-STEM image is used where two $< -111 >$ reflections in the fast Fourier transform (FFT) diffraction patterns are selected. The strain maps along the x and y directions, the e_{xx} and e_{yy} images respectively, do not show any clear edges at the interface and the signal fluctuation is less than 0.5% from the average (Fig. 7.9).

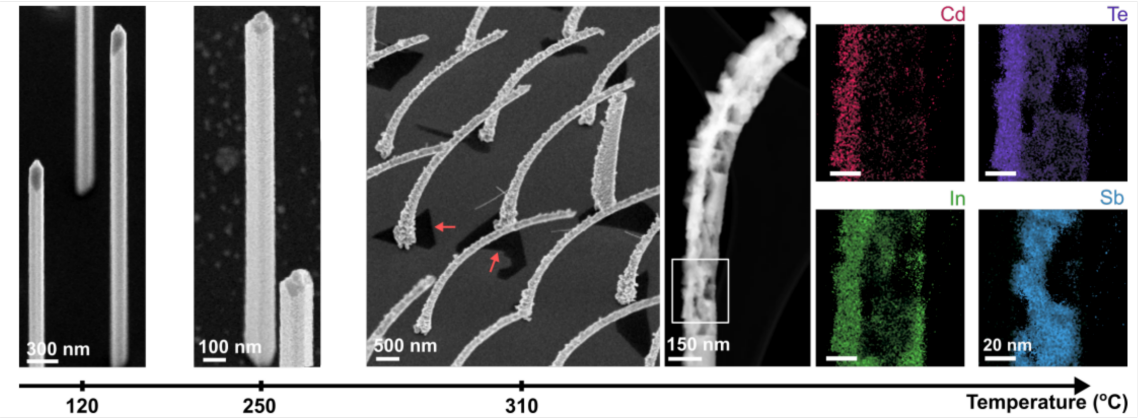

Figure 7.8: CdTe shell growth at different temperatures. Shell growth at 120°C yields smooth shells and a complete layer on the mask. At 250°C, roughness is already detectable within the resolution of the scanning electron microscope. Parasitic growth on the substrate reflects an increased diffusion length, resulting in islands rather than a complete layer. Even more roughness is induced at 310°C in addition to thermal etch pits in the substrate (tiny red arrows) and the nanowires are bent. A close examination of a single nanowire shows that the bending is instigated by pits in the nanowires. These voids are additionally visible in elemental dispersive x-ray mapping. The clustering of In towards the shell (overlapping with Te) signifies that possibly In2Te3 reactions took place at these temperatures.

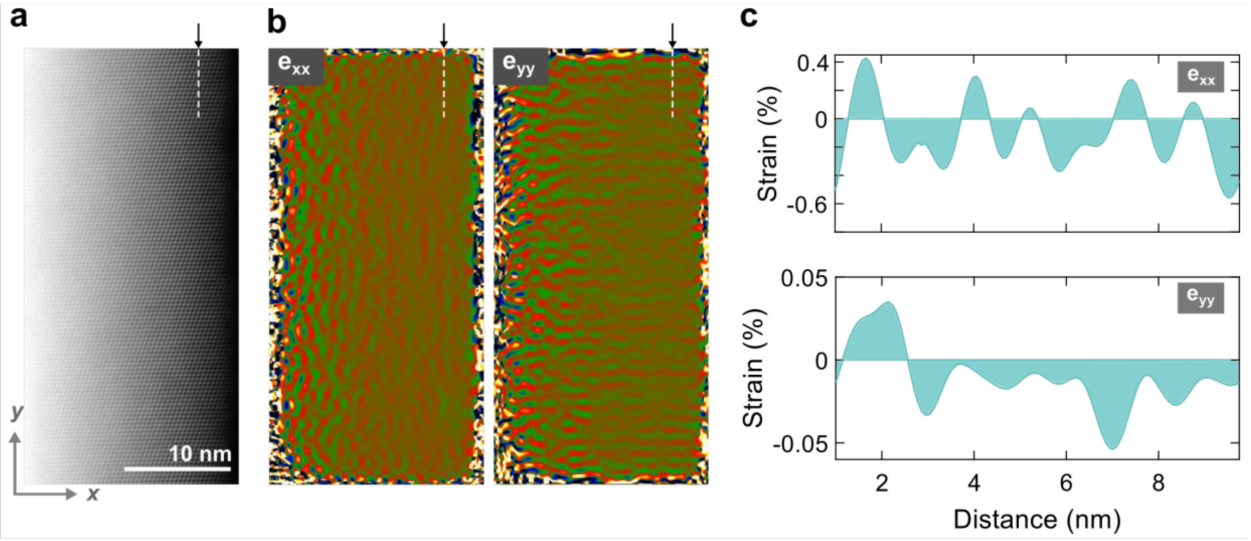

Figure 7.9: Strain mapping. (a) HAADF-STEM image of an InSb-CdTe nanowire taken along the <110> zone axis with the interface indicated by an arrow. (b) The strain mapping of lattice spacing differences along the x and y directions for the HAADF-STEM image shown in (a) indicates a strain-free interface. (c) Line profiles of the strain maps in (b) show signal fluctuations below 0.5% from the average, thus confirming the absence of strain. The indiscernible InSb-CdTe interface in the strain maps further substantiates a relaxed and epitaxial interface.

There is thus no clear indication of strain, within the detection limit of this technique. The absence of strain is consistent with the almost perfect lattice match between InSb and CdTe.

7.8.6 Nano-scale Roughness Along The 110 Zone Axis with Increasinh shell thickness

Tuning the CdTe shell thickness is simply achieved by varying the growth time. For an increasing shell thicknesses (greater than 5 nm) very slight roughness is observed in the shell along the <110> zone axis with transmission electron microscopy (Fig. 7.10). Imaging the same shell along the <112> zone axis does not reveal this roughness, since the nanowire is imaged parallel to a roughly 100 nm long nanowire facet, where a summation of nanoscale roughness is projected in the image plane. In contrast, in the <110> zone axis the nanowire is viewed at the corner between two facets, thereby exposing any atomic scale roughness. This roughness shows up in projection at edges orthogonal to a <111> direction. Although the exact topography and features of this roughness cannot be extracted, it could be due to an increased tendency of CdTe to form {111} facets with increased layer thickness, as already disclosed [179, 180].

7.8.7 Cool Down under Te flux

CdTe shell growth is terminated by closing both the Cd and Te shutters. However, in experiments where a Te flux is supplied during the substrate cool-down for 15 minutes, Te-rich CdTe globules are deposited on the CdTe shell (Fig. 7.11). In contrast, for shells grown at higher temperatures (200°C), these globules are absent, likely due to an increased diffusion length.

7.8.8 Device Fabrication

The fabrication process for mobility devices is described in Chp. 3.2.

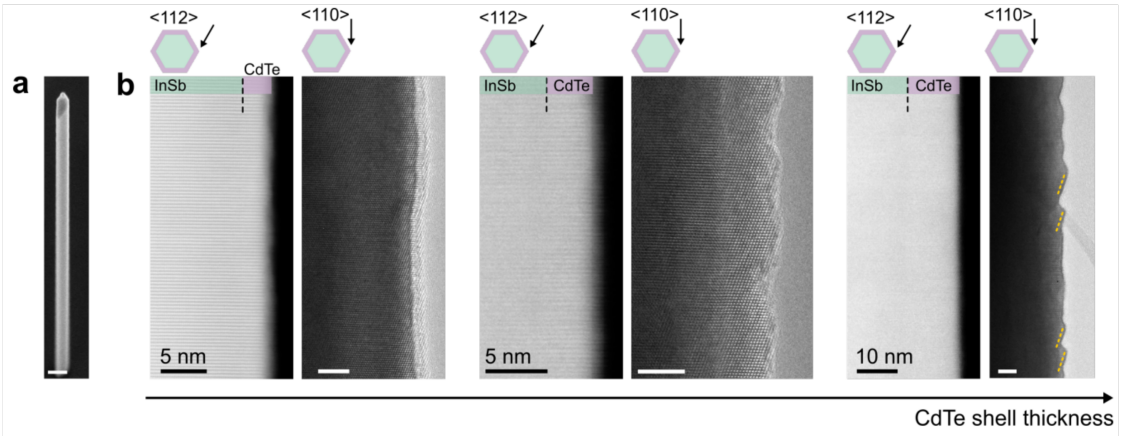

Figure 7.10: Propensity to form nanofacets with increased CdTe thickness. (a) An SEM image of single InSb nanowire covered with a CdTe shell. Scale bar is 200 nm. (b) HAADF scans and bright-field TEM images taken along the specified zone axes of nanowires with differently thick CdTe shells of 2.7 nm, 4 nm and 12.5 nm, respectively. Along the <112> zone axis, the CdTe shells appear atomically flat. Along the <110> direction, however, slight roughness is discernible and develops into well-defined non-vertical edges for the thickest shells. The roughly 13 nm shell is most likely terminated by {111} planes, as indicated by the yellow dashed lines.

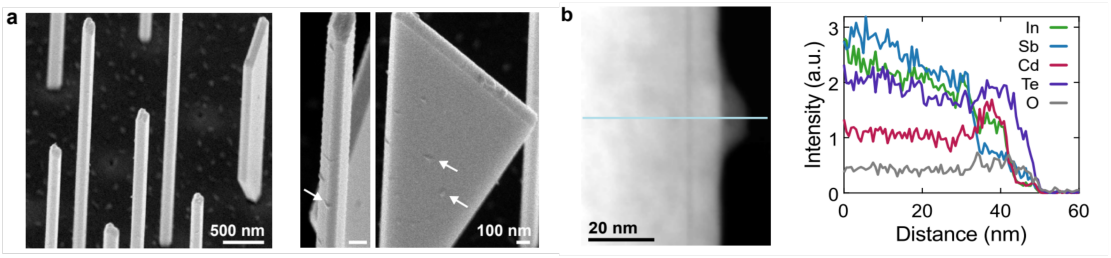

Figure 7.11: Cool-down under Te flux. (a) SEM images taken at 30°-tilt showing tiny globules on the substrate surface and on top of the CdTe shells. Arrows point to representative globules on a nanowire and a nanoflake (scale bar: 100 nm). (b) HAADF-STEM image displaying an area with a globule. An EDX line scan is acquired along the blue line. The composition profile indicates the globule has a higher Te content compared to the CdTe shell.

7.8.9 Mobility Measurements

For the study of field-effect mobility (μ), nanowire field-effect transistor (FET) devices were fabricated as described in Section VIII. The diffusive long-channel regime is assumed based on the channel lengths (L) used. Consequently, the current (I) as a function of back-gate voltage (V_{BG}) can be modeled by Equation:

$$I(V_{BG}) = \frac{V_{dc}}{\frac{L^2/\mu C}{V_{BG}-V_{th}} + R_c} \tag{7.1}$$

where Vdc is the bias voltage. The saturation current is limited by the series resistance (R_c), which includes contact, filter, and line resistances. Current pinch-off is reached at the threshold voltage (V_th). The capacitance (C) value is evaluated using a 3D Laplace solver for a typical nanowire device geometry, assuming a core-shell nanowire diameter of 120-140 nm and accounting for the 15-nm hafnium oxide layer. In this finite-element model, the InSb nanowire is treated as a metal [59]. Capacitance values for bare InSb nanowires and various CdTe shell thicknesses are provided in Table. 7.3. All measurement data, logs, I-V curves, and codes used to extract mobility are publicly available on Zenodo at

CdTe thickness	1 μm	2 μm 3 μm	5 μm	
0 nm	36.8	85.8	134.8	232.8
2 nm	37.9	87.8	137.9	238.1
4 nm	37.2	86.8	136.0	235.1
7 nm	37.1	86.5	135.9	235.0
12 nm	36.6	85.6	134.8	233.1

Table 7.3: Capacitance values used for mobility fitting. The device capacitance is evaluated for different channel lengths and CdTe shell thicknesses. Capacitance values are given in aF.

https://doi.org/10.5281/zenodo.5592057. All FET nanowire devices for mobility extraction are measured using a dip-stick in helium at T = 4.2 K. Before cooling down, the sample space is evacuated at room temperature for 24, 48, and 96 hours to effectively desorb adsorbates from the nanowire surface.

Fig. 7.12(a) and (b) present devices that have been pumped for 24 and 96 hours to evaluate the effect of sample space evacuation on device performance. Notably, a slight increase in mobility, from 1.57 $\times$ 10^4 $cm^2/V \cdot s$ to 1.93 $\times$ 10^4 $cm^2/V \cdot s$, is observed for devices evacuated for 96 hours compared to 24 hours (Fig. 7.12(a)). The data in Fig. 7.12(a) represents devices with a 4-nm CdTe shell. Longer sample space evacuation also reduces the measured hysteresis between forward and backward back-gate voltage sweeps for the CdTe-capped wires, as shown in Fig. 7.12(b). Hysteresis is quantified by determining the difference in threshold voltages (ΔV_{th}) between both sweep directions. The devices studied in Fig. 7.12(b) reveal that, on average, hysteresis decreased from 3.21 V to 2.49 V as a function of longer sample evacuation.

The presence of such significant hysteresis is associated with the CdTe shells, as hysteresis is nearly absent in uncapped, bare InSb nanowires (Fig. 7.12(c)). Furthermore, the slight improvement in hysteresis for longer sample space evacuation suggests that the hysteresis is predominantly caused by something inherent to the shell and only partially by charges in the surrounding environment. While the origin of the hysteresis remains unknown, it

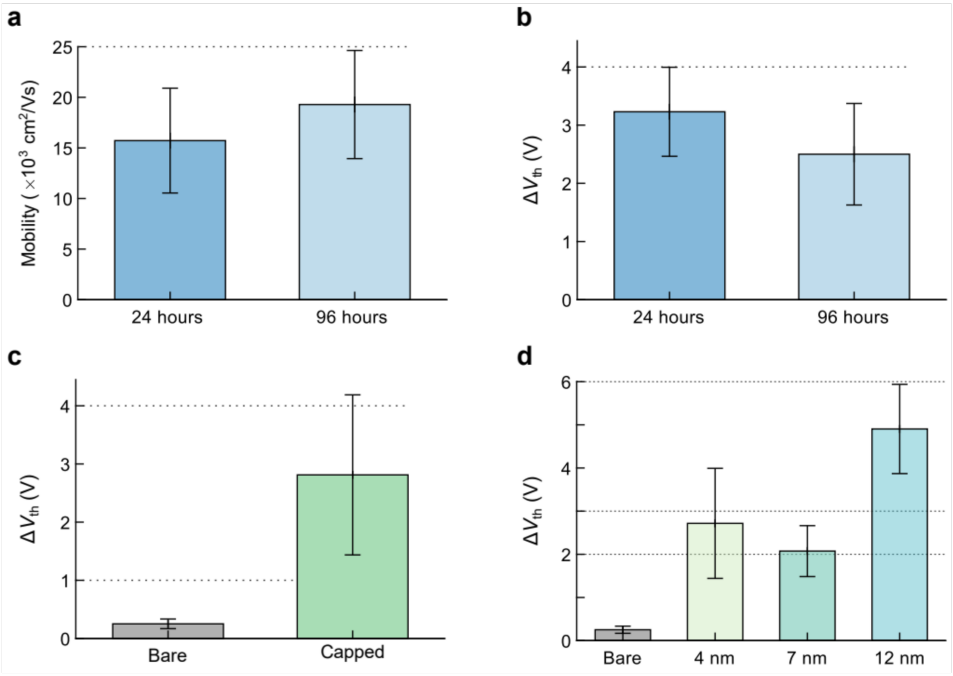

Figure 7.12: Effect of sample space evacuation on mobility and hysteresis. (a) and (b) FET nanowire devices with a 4-nm CdTe shell are evacuated for 24 and 96 hours. (a) A longer evacuation leads to a slight mobility enhancement going from 1.57×10^4 cm$^2/V \cdot s$ to 1.93×10^4 cm$^2/V \cdot s$. (b) A decrease in hysteresis from $\Delta V_{th} = 3.21$ V to 2.49 V, is noted for a 96-hour evacuation, compared to 24 hours. Hysteresis is quantified by the threshold-voltage difference ΔV_{th} between the forward and backward gate-voltage sweeps. (c) CdTe-capped wires show a much larger hysteresis compared to uncapped, bare InSb nanowires. (d) Hysteresis varies with CdTe shell thickness, with the largest hysteresis present for the 12-nm CdTe shell nanowires.

is likely attributed to trapped charges within the shell (point defects in the CdTe shell) or at one of the interfaces (the InSb-CdTe interface or the CdTe-dielectric interface). We expect trapped charges in the CdTe shell to cause larger hysteresis for thicker CdTe shells, as thicker shells would host more point defects. Conversely, trapped charges at the InSb-CdTe interface would be unaffected by CdTe shell thickness, resulting in similar hysteresis for all CdTe thicknesses. Trapped charges at the CdTe-dielectric interface are expected to result in smaller hysteresis for increasing shell thickness, as charges are kept away from the InSb core for thicker shells. While the results in Fig. 7.12(d) show that the largest hysteresis exists for the thickest studied CdTe shells (12 nm), suggesting that trapped charges are within the CdTe shells, this trend is not very conclusive. In large part, this is because we have more data on 4-nm CdTe shell nanowires compared to 7-nm and 12-nm shell wires. Accordingly, the shown trend is likely not representative.

8.0 Conclusions and outlook

8.1 Introduction

In this thesis, our primary focus is on proximity-induced superconductivity in Sn-InSb nanowires and the Josephson junction devices fabricated using this type of hybrid nanowires. Our ultimate goal is to establish an optimized platform for realizing Majorana bound states (MBS) in superconductor-semiconductor hybrid systems, which are believed to lead to fault-tolerant topological quantum computing. The emergence of MBS is predicted by theory when a system is in a topological superconducting state, but requires an elegant balance of various physics effects [16, 15]. Numerous experimental attempts have been made to detect MBS in mesoscopic devices, but convincing evidence of MBS has remained elusive due to factors such as material defects, suppression of superconductivity before reaching the topological regime, ambiguous results from Andreev bound states.

Our efforts in this thesis are organized into four parts. In Chapter 4, we report our recent progress in growing Sn-InSb nanowires. By applying an in-situ shadowing technique, we enhance proximity-induced superconductivity in InSb semiconductor nanowires using a thin Tin shell. In Chapter 5, we investigate how orbital effects and interference between transverse modes suppress Josephson current under external fields. We also explore whether tuning the system into a few-mode regime can minimize these effects, providing a larger parameter space for studying Majoranas. In Chapter 6, we study skewed critical current diffraction patterns and their relationship with spin-orbit interaction in our devices lacking inversion symmetry. We utilize two models to demonstrate the anomalous Josephson effect is actually a ϕ_0 junction with higher-order harmonics. Finally, in Chapter 7, we delve into the electronic structure and transport properties of a novel combination: CdTe/InSb shell/core nanowires. The CdTe layer serves a dual purpose as both a tunnel barrier between the super-semi materials and a protective layer to prevent InSb from oxidation, suggesting a potential path for future devices geometry in Majorana-related studies.

8.2 Chp4: Sn-InSb nanowires

In this chapter, we investigate Sn-InSb nanowires. Firstly, InSb nanowires are grown in Eindhoven and transported to UCSB. The oxidation layer is removed through hydrogen cleaning, followed by the growth of a Sn shell at cryogenic temperatures. Junctions are formed using an in-situ shadow technique. Upon material analysis, we discover that the shell has a uniform thickness but forms grains at the interface between Sn and InSb. Both alpha-type and beta-type Sn are found in these grains, while only the non-superconducting alpha-tin is epitaxial on the InSb nanowires. Transport results demonstrate strong superconductivity in InSb, which is proximity-induced by the Sn shell, even though the superconducting beta-tin is not epitaxially grown on the nanowires. The induced superconducting gap is free of subgap states, and the superconductivity is resilient to external magnetic fields up to 4 T. In Josephson junctions, the I_cR_n product has a value at the same scale when compared to the gap energy of Sn (see Fig. 4.2, 5.18, 6.25). In N-S-N island devices, parity transitions of electrons driven by the external field are observed, which is an essential feature for building transmon and Majorana qubits. This work challenges conventional thinking in material choices for Majorana studies, as epitaxial growth has long been believed to be necessary for inducing strong superconductivity in semiconductor nanowires, and Al-InAs has been the only choice due to its close lattice constant. Recent works also demonstrates that Nb, Pd,Ta, and Va on InAs nanowires yield promising results [198, 91]. In Al-InAs nanowires, the parameter space is highly restricted by the intrinsic energy gap of Al, which is incapable of reaching the proposed topological state at external fields up to 1 T [20, 16, 15]. By demonstrating that epitaxial growth is not required, we show that more super-semi hybrid combinations can be considered in the exploration of MBS, especially those superconductors with higher critical temperatures.

Based on the current conclusions drawn from Sn-InSb, there are several ideas worth exploring. One is to investigate whether alpha or beta tin is the primary origin of superconductivity in InSb nanowires and if we can control growth parameters to achieve pure alpha or beta tin shells on nanowires while maintaining uniform thickness and a smooth interface. This work is partially discussed in Ref. [199] but requires further exploration. We also take

note of the recently developed shadow wall technique for device fabrication [200]. It offers etching-free formation of junctions with controllable lengths. As some theories argue that in a N-S-N three terminal device, a longer region covered by the Sn shell should be considered to effectively isolate Majorana pairs while maintaining their coupling strength [201], growing Sn shells with this technique is underway in and warrants further investigation [202]. Another advantage of Al compared to Sn is the existence of a well-established Al etchant that is less harmful to other materials, acting as a selective etchant. For Sn, such a chemical etchant is still missing but should be explored.

8.3 Chp5: Supercurrent in first electron transverse mode

In this chapter, we fine-tune the conduction channel in Sn-InSb nanowire Josephson junction quantum point contacts (QPC) and observe supercurrent that transports through nanowires while only one transverse mode is occupied. From previous studies, we know that the orbital effect and interference between transverse modes can significantly suppress superconductivity in the presence of an external field [118, 34], thereby driving the system away from the intriguing topological regime. We observe a long decay of superconductivity up to fields of 1 T. Simultaneously, the decay for higher occupied subbands is notably faster in some devices but not in others. We analyze this using a tight-binding numerical model that includes the Zeeman, orbital, and spin-orbit effects, all of which indicate that suppression from orbital and interference can be reduced when only one conduction channel is open. When the first subband is spin-polarized, we observe a dramatic suppression of supercurrent, which is also confirmed by the model and suggests an absence of significant triplet supercurrent generation.

As we conclude that the parameter space for topological studies is expanded by driving the global modes to one, our next goal is to study Majorana signatures with our QPC devices. The AC Josephson effect with RF microwaves should be considered. If there is a transition of junction phase periodicity from 2π to 4π, which behaves like the absence of odd-numbered Shapiro steps, then it could be evidence of realizing MBS in nanowire Josephson junctions

and used as for braiding quantum circuit [80].

8.4 Chp6: Evidence of phi-0 junction

In this chapter, we study Josephson junctions based on InSb nanowires with Sn shells. We observe skewed critical current diffraction patterns, with maxima in forward and reverse current bias occurring at different magnetic flux values. The skew is greatest when the external field is nearly perpendicular to the nanowire, in the substrate plane. This orientation suggests that spin-orbit interaction (SOI) plays a role. We develop a phenomenological model and perform tight-binding calculations, with both methods reproducing the essential features of the experiment. The effect modeled is the ϕ_0-Josephson junction with higher-order Josephson harmonics. The system is of interest for Majorana studies, as the effects are either precursors to or concomitant with topological superconductivity.

As we already discussed in that chapter, current-phase relations lacking inversion symmetry can also be used to design quantum circuits with engineered nonlinearity [203]. The skew can be utilized to study the control of spin-orbit effects. One possible design involves having two side gates on each side of the junction. We already know that both the chemical potential and junction size can be tuned by the gate voltage, so two gates can maintain the global electric field at the same magnitude but with a rotated angle. Based on the definition of Rashba SOI, the effective field should also rotate along with the electric field, which can be detected and quantified with the field direction dependence of the skew. SOI is essential for realizing MBS; quantifying how the effective field is driven by the gate voltage would be a significant advancement.

8.5 Chp7: CdTe-InSb nanowires

In this chapter, we study InSb nanowires fully covered by a thin CdTe shell. The surface of InSb is cleaned with hydrogen milling using the same technique used in Chapter 4. TEM

analysis reveals that no oxidation layer is present between InSb and CdTe, and the interface is epitaxial. Electronic structure studies are conducted using density functional theory, which finds that the thin CdTe does not bring significant changes to the bandgap of InSb—a result also confirmed by transport measurements. The CdTe functions as a protective layer on the InSb, preventing oxidation of the InSb nanowires. In-situ removal of the CdTe shell with argon gas plasma milling, followed by the deposition of normal contacts, is used to fabricate devices for mobility measurements. Transport measurements at liquid helium temperatures demonstrate mobility at the same scale as previously established results [59]. As evidenced by the comparable field-effect mobility measured for both uncapped and CdTe-capped nanowires, these shells do not introduce disorder to the InSb nanowires.

As proposed in Chapter 7, CdTe can function as a tunnel barrier between superconductor leads and semiconductor nanowires, operating similarly to a tunnel gate but without asymmetry. The coupling strength can be adjusted by changing the thickness of the CdTe shell. Based on our findings in Chapter 4, epitaxy between nanowires and the superconductor is not necessary for Majorana related studies. Transport results for superconductor-CdTe-InSb nanowires will be an interesting area for future research.

Appendix Appendix: List of Publications

1. "Parity-preserving and magnetic field–resilient superconductivity in InSb nanowires with Sn shells". M. Pendharkar†, B. Zhang†, H. Wu†, A. Zarassi†, P. Zhang†, P. Dempsey, J. S. Lee, S. D. Harrington, G. Badawy, S. Gazibegovic, R. L. M. Op het Veld, M. Rossi, J. Jung, A.-H. Chen, M. A. Verheijen, M. Hocevar, E. P. A. M. Bakkers, C. J. Palmstrøm, S. M. Frolov , **Science** 372, 508 (2021)
2. "Electronic Structure and Epitaxy of CdTe Shells on InSb Nanowires". G. Badawy, B. Zhang, T. Rauch,J. Momand, S. Koelling, J. Jung, S. Gazibegovic, O. Moutanabbir, B.J. Kooi, S. Botti, M. A. Verheijen, S. M. Frolov, E. P. A. M. Bakkers. **Advanced Science**, 2105722 (2022).
3. "Evidence of ϕ_0-Josephson junction from skewed diffraction patterns in Sn-InSb nanowires". B. Zhang, Z.li, V.Aguilar, P. Zhang, M. Pendharkar, C. Dempsey, J. S. Lee, S. D. Harrington, S. Tan, J.s. Meyer, M. Houzet, C.J. Palmstrøm, S.M. Frolov. Arxiv.org/abs/ 2212.00199.
4. "Planar Josephson junctions templated by nanowire shadowing". P. Zhang, A. Zarassi, M. Pendharkar, J.S. Lee, L. Jarjat, V. Van de Sande, B. Zhang, S. Mudi, H. Wu, S. Tan, C.P. Dempsey, A.P. McFadden, S.D. Harrington, B. Shojaei, J. T. Dong, A.-H. Chen, M. Hocevar, C.J. Palmstrøm, S.M. Frolov. Arxiv.org/abs/2211.04130.
5. "Role of a capping layer on the crystalline structure of Sn thin films grown at cryogenic temperatures on InSb substrates". A.-H. Chen, C.P. Dempsey, A. Sharma, B. Zhang, S.M. Frolov, C.J. Palmstrom, E. Bellet-Amalric, M. Hocevar. Arxiv.org/abs/2301.12424.
6. "Supercurrent through a single transverse mode in nanowire Josephson junctions". B. Zhang, Z.li, H, Wu, M. Pendharkar, C. Dempsey, J. S. Lee, S. D. Harrington, C.J. Palmstrøm, S.M. Frolov. Arxiv.org/abs/2306.00146.

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