IMPROVEMENTS IN VOLTAGE CONTROL AND DYNAMIC PERFORMANCE OF POWER TRANSMISSION SYSTEMS USING STATIC VAR COMPENSATORS (SVC)

by

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Flexible AC Transmission System (FACTS) controllers, such as the Static Var Compensator (SVC), employ the latest technology of power electronic switching devices in electric power transmission systems to control voltage and powerflow, and improve voltage regulation.

Given a profit-driven, deregulated electric power industry coupled with increased load growth, the power transmission infrastructure is being stressed to its upper operating limits to achieve maximum economic returns to both generator and transmission system owners. In such an environment, system stability problems such as inadequate voltage control and regulation must be resolved in the most cost-effective manner to improve overall grid security and reliability.

Static Var Compensators are being increasingly applied in electric transmission systems to economically improve voltage control and post-disturbance recovery voltages that can lead to system instability. An SVC provides such system improvements and benefits by controlling shunt reactive power sources, both capacitive and inductive, with state-of-the-art power electronic switching devices. This thesis will discuss and demonstrate how SVC has successfully been applied to control transmission systems dynamic performance for system disturbances and effectively regulate system voltage. System and SVC modeling will also be discussed.

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PREFACE

I would like to thank my wife, Susan, and my three sons Daniel, Nathan, and Andrew for their support and patience during the research and preparation of this thesis.

I am also very grateful to Dr. Kusic, Dr. Colclaser, John Paserba, Ron Pape, Dr. Greg Reed, Doug Jackson, and Dave Borneman for the technical support and guidance they have provided to me during the writing of this thesis and throughout the pursuit of my Masters degree. Thank you all.

1.0 INTRODUCTION

The focus of this thesis and research is on the application of Static Var Compensator to solve voltage regulation and system dynamic performance deficiencies. SVC is a mature thyristor-based controller that provides rapid voltage control to support electric power transmission voltages during and immediately after major system disturbances.

Since the advent of deregulation and the separation of generation and transmission systems in the electric power industry, voltage stability and reactive power-related system restrictions have become an increasingly growing concern for electric utilities. With deregulation came an “open access” rule to accommodate competition that requires utilities to accept generation and load sources at any location in the existing transmission system. This “open access” structure has challenged transmission owners to continually maintain system security, while at the same time trying to minimize costly power flow congestion in transmission corridors. When voltage security or congestion problems are observed during the planning study process, cost effective solutions must be considered for such problems. Traditional solutions to congestion and voltage security problems were to install new costly transmission lines that are often faced with public resistance, or mechanically-switched capacitor banks that have limited benefits for dynamic performance due to switching time and frequency.

One approach to solving this problem is the application of “Flexible AC transmission System” (FACTS) technologies, such as the Static Var Compensator (SVC). FACTS technologies are founded on the rapid control response of thyristor-based reactive power controls.

Over the last several years, there were numerous installations of FACTS in the United States and around the world [1] [2]. FACTS have proven to be environmental friendly and cost-effective solutions to a wide range of the power system needs. FACTS have given utilities the option to delay new transmission line construction by increasing capacity on existing lines and/or providing dynamic control and compensation of the system voltages [3] [4] [5]. FACTS controllers are available in different forms such as static VAR compensators (SVCs), thyristor controlled series capacitors (TCSCs), static reactive compensators (STATCOMs), and unified power flow controllers (UPFCs).

Some of the technical/economic "attractiveness" of SVC are highlighted in the Table 1-1.

Table 1-l. Comparison of Var Compensation Methods Incorporating Both Technical and Economic Merits (extracted from [11])

Function	Technical/economic attractiveness of reactive comp. means				
	Shunt react.	Shunt cap.	Sync. comp.	SVC	Series cap.
Steady-state voltage control an stability:					
- Coarse reactive power balance and voltage control	AAA	AAA	–	–	A
- High-performance voltage control	–	–	AA	AAA	–
Dynamic voltage control for large disturbances	–	–	AA	AAA	–
Reduction of temporary over-voltages	AA	–	AA	AA	A
Improving first-swing transient stability	–	–	–	AA	AAA
Damping of power oscillations	–	–	A	AA	–

The Static Var Compensator is the first generation of FACTS devices that has been in use in transmission systems worldwide since the 1970's and in North America since the late 1970's. Figure 1-1 presents the approximate number of transmission SVC installed in both North America and worldwide.

From Figure 1-1, a hypothesis can be drawn that from 1998 to 2003 the North American SVC market was significantly stagnant most likely due to the uncertainties of the impact deregulation in the power industry. Then in 2004 deregulation in the electric utility industry became better implemented, and SVC offered a cost-effective and environmentally friendly solution to system problems that could in some cases delay the need for new transmission line.

The installation of transmission lines typically requires clearing of vegetation and trees from the area under/near the transmission line towers or poles.

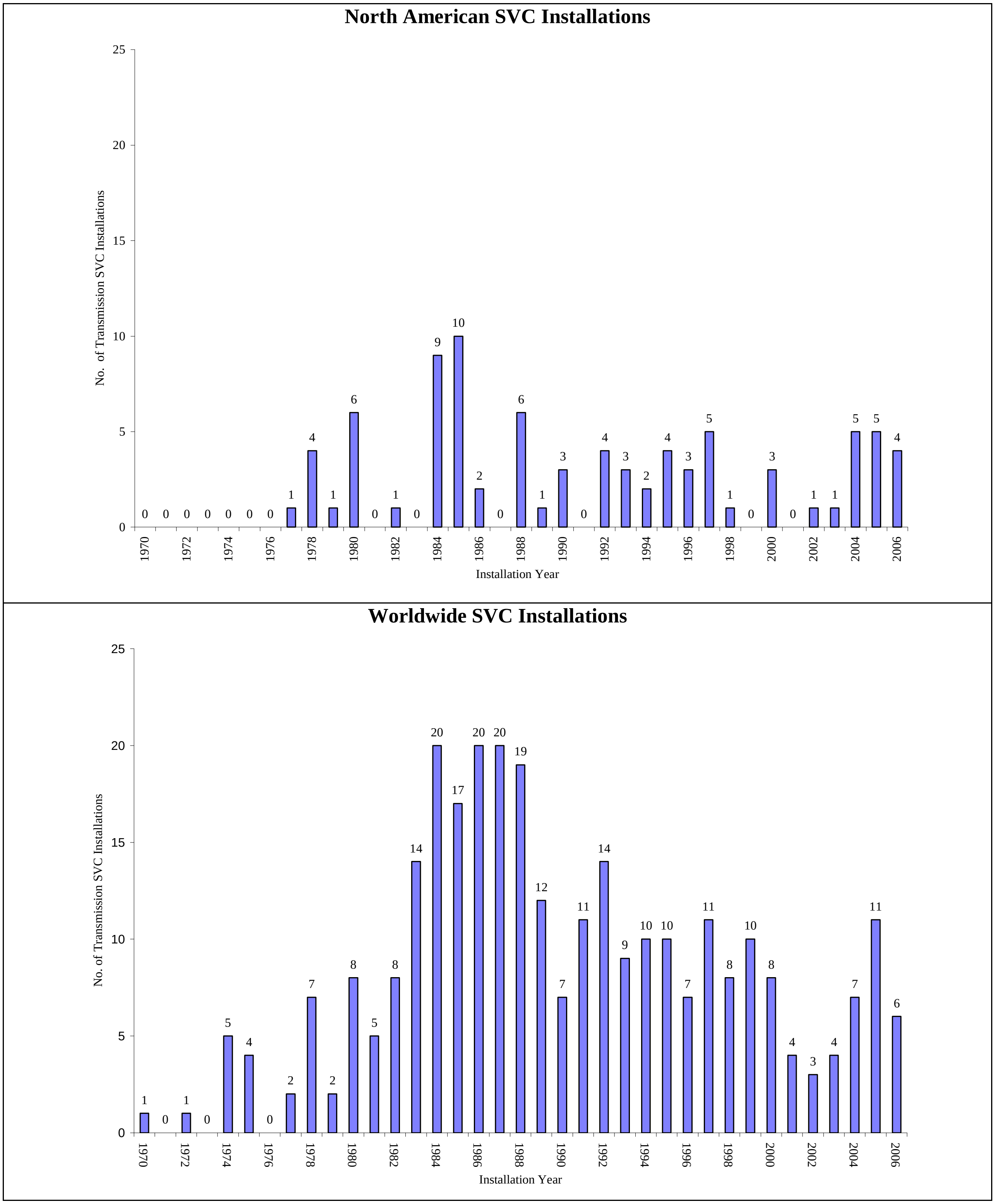


Figure 1-1. Approximate number of Transmission SVC installations from 1970 to 2006.
(based on 2004 List compiled by IEEE Working Group I4 on SVC and other manufacturers data)

The SVC provides an excellent source of rapidly controllable reactive shunt compensation for dynamic voltage control through its utilization of high-speed thyristor switching/controlled reactive devices.

An SVC is typically made up of the following major components:

- Coupling transformer
- Thyristor valves
- Reactors
- Capacitors (often tuned for harmonic filtering)

In general, the two thyristor valve controlled/switched concepts used with SVCs are the thyristor-controlled reactor (TCR) and the thyristor-switched capacitor (TSC). The TSC provides a "stepped" response and the TCR provides a "smooth" or continuously variable susceptance.

Two "common" main SVC circuit arrangements shown in Figure 1-2 are:

"FC/TCR"–fixed capacitor(filter)/thyristor(phase angle)-controlled reactor (Config A)

"TSC/TCR"–thyristor-switched capacitor/thyristor-controlled reactor (Config B)

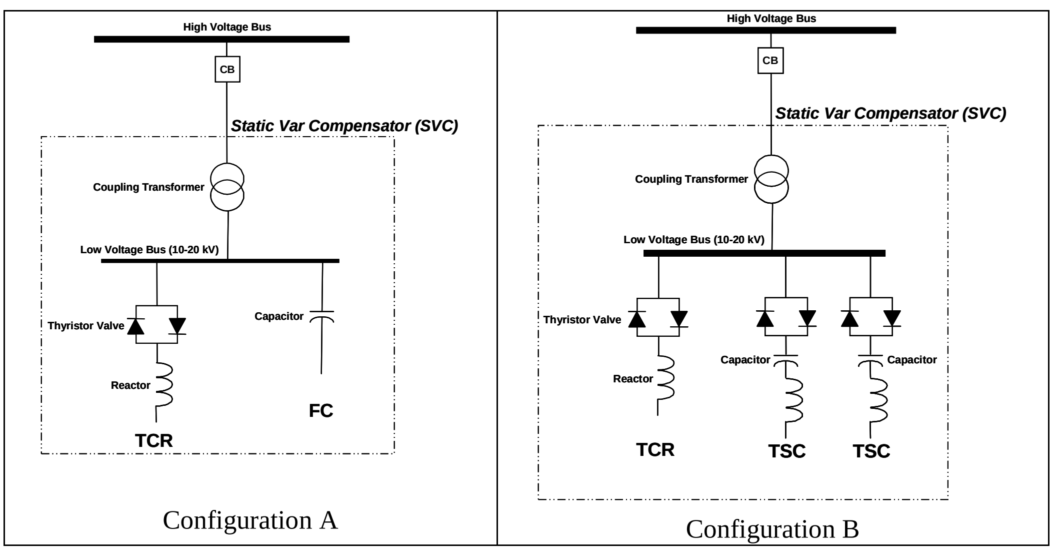


Figure 1-2. Common SVC main configurations.

An SVC is a controlled shunt susceptance (B) as defined by the SVC control settings that injects reactive power (Q) into the system based on the square of its terminal voltage. Figure 1-3 illustrates a TCR/FC SVC, including the operational concept. The control objective of the SVC is to maintain a desired voltage at the high-voltage bus. In the steady-state, the SVC will provide some steady-state control of the voltage to maintain it the high-voltage bus at a pre-defined level.

If the high-voltage bus begins to fall below its setpoint range, the SVC will inject reactive power (Q_{net}) into the system (within its controlled limits), thereby increasing the bus voltage back to its desired voltage level. If bus voltage increases, the SVC will inject less (or TCR will absorb more) reactive power (within its controlled limits), and the result will be to achieve the desired bus voltage. From Figure 1-3, $+Q_{cap}$ is a fixed capacitance value, therefore the magnitude of reactive power injected into the system, Qnet, is controlled by the magnitude of $-Q_{ind}$ reactive power absorbed by the TCR.

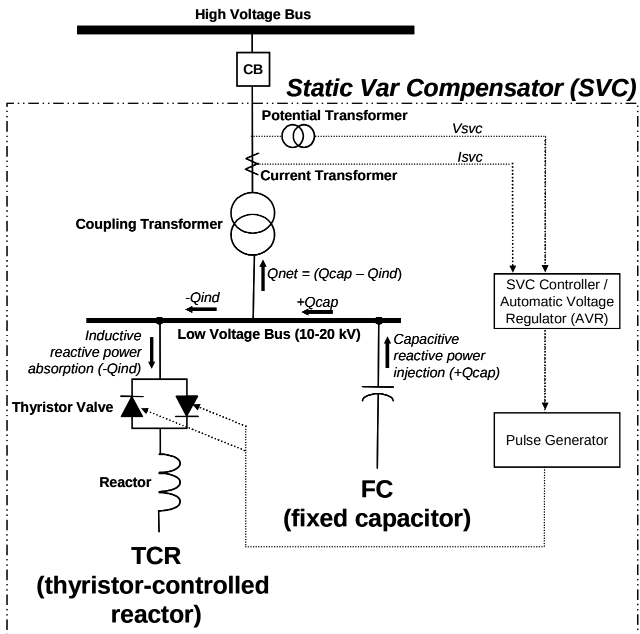


Figure 1-3. SVC with control concept briefly illustrated.

The fundamental operation of the thyristor valve that controls the TCR is described here. The thyristor is self commutates at every current zero, therefore the current through the reactor is achieved by gating (or firing) the thyristor at a desired conduction angle (or firing angle) with respect to the voltage waveform. Figure 1-4 describes the relationship between the fundamental frequency TCR current and firing angle.

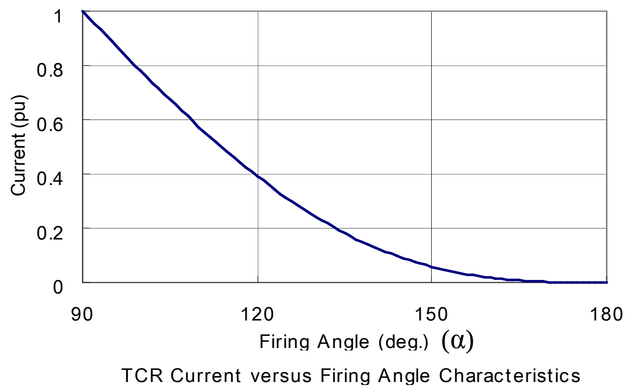


Figure 1-4. Illustration of the relationship between TCR current and firing angle.

Figure 1-5 further illustrates the thyristor valve operating characteristics of a thyristor-controlled reactor. The firing pulses are on the order of 10 μs. So it is concluded that as the firing angle increases above 90 degrees, the current in the TCR is reduced. Referring back to Figure 1-3, the "Pulse Generator" block after the AVR block utilizes the concepts discussed here and illustrated in Figures 1-4 and 1-5 to determine the firing angle for the thyristor valve controlling the reactor.

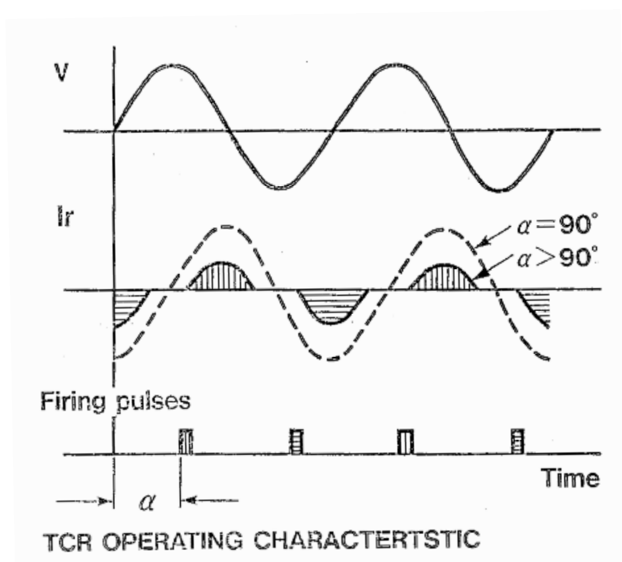


Figure 1-5. Illustration of the relationship between TCR current and firing angle (or conduction angle).

This thesis gives details of an 87 Mvar, 115 kV SVC installed in a transmission system. The SVC will effectively solve the voltage regulation problem in the study area and delay the costly construction of a new 40 mile, 230 kV transmission line. Budgetary cost of an 87 Mvar SVC is around $8 million, where a 40 mile 230 kV transmission line is approximately $19 million.

2.0 LITERATURE SURVEY

In this section, published literature from international electrical engineering groups such as the Institute of Electrical and Electronics Engineers (IEEE), the International Council on Large Electric Systems (CIGRE) were reviewed with important relevant subjects related to voltage control, var compensation, and static var compensators briefly discussed and identified.

2.1 HISTORY AND BACKGROUND OF SVCS

Static var compensators, regarded as the first FACTS controllers, have been used in North American transmission systems since late 1977 in western Nebraska [6]. The aforementioned transmission SVC device was installed to provide "automatic, continuous voltage control." Since then, there have been about 300 transmission SVCs commissioned around the world, and about 90 transmission SVCs applied in North America [7]. The term "transmission system SVC" is used because SVCs are also applied at the distribution level to compensate for local voltage fluctuation problems due to industrial load operation [9].

The heart of the SVC is an a.c. power semi-conductor switch commonly known as the "thyristor valve" that is used in principle to replace mechanical switches to achieve rapid, repetitive, and in some cases continuous control of the effective shunt susceptance at a specific location in a transmission system by a set of inductors and capacitors [8]. For example, as shown in Figure 1-3, the fixed capacitor (FC) in parallel with a thyristor-controlled reactor (TCR), the valve continuously and "smoothly" controls the reactor to achieve a "net susceptance" that is varied to maintain the transmission system voltage to a desired value or range. The SVC configuration described in this example is known as FC/TCR.

The overall steady-state characteristics of the SVC are described in the form of a volt-current (VI) curve, as illustrated in [10] [11] [12]. An automatic voltage regulator with a transfer function of [K * 1/(1+sTp)] is often used.

Reference [10] provides an excellent application-oriented and often referenced book by Dr. Hingorani and Dr. Gyugyi that "emphasizes physical explanations of the principles involved" in FACTS applications.

2.2 VOLTAGE CONTROL AND DYNAMIC PERFORMANCE

References [14] [15] provide in-depth and comprehensive explanations and application examples associated with voltage stability and system stability and control. Additionally, references [14] [11] [25] discuss how and when SVC application can:

(1) effectively improve voltage control and dynamic performance

(2) be a cost-effective solution

The influence on voltage control capabilities of reactive compensation devices such as mechanically-switched capacitors (MSC), SVC, voltage-source converters (STATCOM), and thyristor controlled series capacitors (TCSC) are compared in [12]. This IEEE paper compares the ability of the aforementioned devices to influence the transient voltage stability of a transmission system, and their ability to maintain security under contingency conditions. SVCs with "smooth" control can solve transient voltage stability and regulation problems that cannot be solved by MSCs due to the limitations of switching speed and switching frequency of MSC. However, MSC can be economically used together with SVCs to provide a static var system for voltage control.

References [11] [12] discuss how reactive compensation such as SVC is often applied in or around load centers (with remote generation) where the system connecting the load center to the generation source can become relatively weak under certain contingency conditions leading to voltage control or collapse problems.

The CIGRE report in [13] discusses the results of an electric utility survey on the practices that utilities use for transmission operational planning studies with respect to voltage limits and reactive margins to ensure adequate system security and reliability. This report outlines the general process that utilities use to determine system voltage limits and reactive power margins required to prevent voltage collapse (for example) for different system conditions such as peak and light loading, and contingency outages of transmission lines and/or generators. System and device modeling is also discussed in this report.

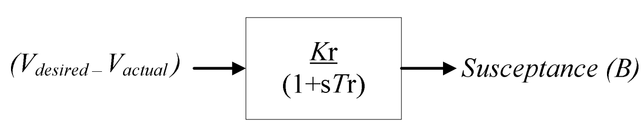
2.3 MODELING FOR DYNAMIC PERFORMANCE ANALYSES ASSOCIATED WITH SVC APPLICATIONS

When studying system dynamic performance and voltage control, system modeling is an important aspect especially in and around the specific area of study [13] [16] [17]. It is typical for many electric utilities to share large system models made up of thousands of buses representing the interconnected system (i.e., western US interconnection, eastern US interconnection). Then utilities in specific areas include more accurate modeling of their specific area or territory that is under study. This is done with the understanding that influence of models outside the specific area of study decreases as you move away from the study area.

Details on modeling "system" elements such as transformers, generators, transmission lines, and shunt reactive devices (i.e., capacitors, reactors), etc., for short-term stability analyses are discussed in [15].

An important and continually debated modeling aspect is the "load" model. For short-term stability analyses, loads are modeled with both static (e.g., real power, reactive power) and dynamic characteristics. Much information on load modeling can be found in [14] [15] [18] [19] [20] [21].

Of particular interest in this thesis is the dynamic SVC model used for voltage regulation. A key part of most SVC models is the automatic voltage regulator (AVR) control block that operates on a voltage error signal. The generic AVR control block is defined by the transfer function:



where *Kr* is the gain and *Tr* is a time constant.

Additional information on other commonly used control block functions with SVC dynamic models such as slope setting, maximum and minimum susceptance limits, thyristor firing transport lag, voltage measurement lag, etc., can be found in [22] [23] [24].

2.4 PERFORMANCE CRITERIA

Each electric utility or in some cases oversight groups such as the Western Electric Coordinating Council (WECC), define specific reliability criteria that outlines the system performance requirements with respect to voltage control and dynamic performance for both normal and contingency operations. Information and examples regarding system performance criteria can be found in references [14] [15] [26].

As discussed in [25], the SVC performance criteria is typically defined by the outcome of various SVC planning and application studies. Reference [27] provides guidance on preparing a specification for a transmission SVC, and suggests the type of information that should be needed to help define various types of criteria for the SVC.

2.5 STATEMENT OF PROBLEM AND THESIS OBJECTIVE

The objective of this thesis is to solve the problem of poor dynamic performance and voltage regulation in a 115 kV and 230 kV transmission system by applying a Static Var Compensator. When fault disturbances occur in the system that result in transmission line tripping, a load center (or substation) is partially disconnected from the source of power over the tripped transmission line. This condition leaves inadequate reactive power to maintain voltage levels, and in the future may result in fast voltage collapse of the entire system. The problem and solution will be discussed and illustrated by dynamic simulation plots and data tables through a dynamic performance analysis.

The voltage collapse problem in future years (i.e., future load levels of 2012) will be illustrated, along with an SVC solution. Then, a complete dynamic performance analysis examines a wide range of system disturbances under peak and light system load levels of year 2005 to verify that the SVC adequately controls the system's dynamic performance and system voltage. The analysis examined both the system performance and the SVC performance.

3.0 DYNAMIC PERFORMANCE ANALYSIS

The dynamic performance analysis discussed in this section will demonstrate through simulation how a modern static var compensator is applied to resolve a voltage regulation problem in a 115/230 kV transmission system.

3.1 INTRODUCTION AND BACKGROUND OF ANALYSIS

As illustrated in Fig. 3-1, the study area is served by two 230/115 kV substations (bus 156 and bus 2316) and two 230 kV lines. Single line equivalents are used to represent the three-phase 230/115 kV transmission lines. The 230 kV line, approximately 40 miles in length, from bus 118 to bus 156 (including one tap point/bus) is a significant source of power for the study area. The steady-state power flow under 2005 peak loading conditions on this line is 127 megawatts (MW). The other 230 kV line, approximately 80 miles in length, serving the study area is from bus 157 to bus 2316 with power flow of 87 MW under 2005 peak loading conditions. By 2005, an outage of the either 230 kV line will result in voltages in the study area below 0.9 p.u. Around the year 2012, pre-contingency voltages in the area will be unacceptable (< 0.95 p.u.). The study area needs either a traditional improvement such as a costly new 230 kV transmission line to provide a third feed into the area or a reactive support device to provide voltage control in the area.

The purpose of this analysis was to verify that a 0 to 87 Mvar SVC installed in a 115 kV power system in the year 2005 controls the system's dynamic performance during system disturbances and meets the performance criteria. The basis for rating the SVC at 87 Mvar is discussed in Appendix A.

The expected benefits of the SVC, in priority order, are:

- Steady state voltage regulation under transmission element out conditions
- steady state voltage regulation with all elements in service
- voltage recovery enhancement (fault-induced delay)

The analysis is to determine if the SVC adequately controls the system's dynamic performance and the system voltage. By examining a wide range of system disturbances at various locations, under both peak and light load conditions for the 2005 system, the performance of the SVC is tested to ensure it meets all the utility's performance criteria.

3.2 2005 STUDY MODEL USED FOR THE DYNAMIC PERFORMANCE ANALYSIS

3.2.1 2005 SYSTEM MODEL

The simulation program used for the modeling and analysis of the utility's power system was the Power Technologies Inc.'s (PTI) Power System Simulator for Engineering (PSS/E) program. PSS/E is an industry standard for large-scale power system load flow and stability simulation. Additional information on loadflow and stability can be found in [15] [28].

The analysis was performed using PSS/E load flow and stability models encompassing the Eastern USA Interconnection. As briefly discussed in [16] [17], it is typical for many electric utilities to share large system models made up of thousands of buses representing the interconnected system (i.e., western US interconnection, eastern US interconnection). Generally, utilities in specific areas include more accurate modeling of their specific area or territory that is under study. This is done with the understanding that the influence of models outside the specific area of study decreases as you move away from the study area.

Both peak and light load conditions were studied for the 2005 system since this is expected to be the first year this device is needed, as will be shown later in this analysis. The PSS/E load flow models consisted of the general characteristics described in the following subsections.

3.2.1.1 2005 Peak Load Network. The single-line diagram for the 2005 peak loading case is shown in Figure 3-1 with the total study area load of 232.2 MW**.**

For all dynamic simulations, a PSS/E complex load model represents the loads in the study area, such that the total load in the load flow model at the respective buses is a composite model of large and small induction motors, and other distribution level equipment (explained further in Section 2.1.3). Other dynamic load models are discussed in [16] [17] [18] [19]. The static loads modeled at buses 839 and 840 are represented as 100% constant power with a maximum net load at bus 840 (as seen by the "system") of 75 MW and 45 Mvar. The remaining loads in areas surrounding the study area are modeled as 10% constant power and 90% constant current according to the following algebraic equations:

$$P = P_0 (P_G V^2 + P_I V + P_S)$$

$$Q = Q_0 (Q_G V^2 + Q_I V + Q_S)$$

Transmission line shown as dotted lines in Figure 3-1 is normally open, and only closed in emergency or short-duration maintenance.

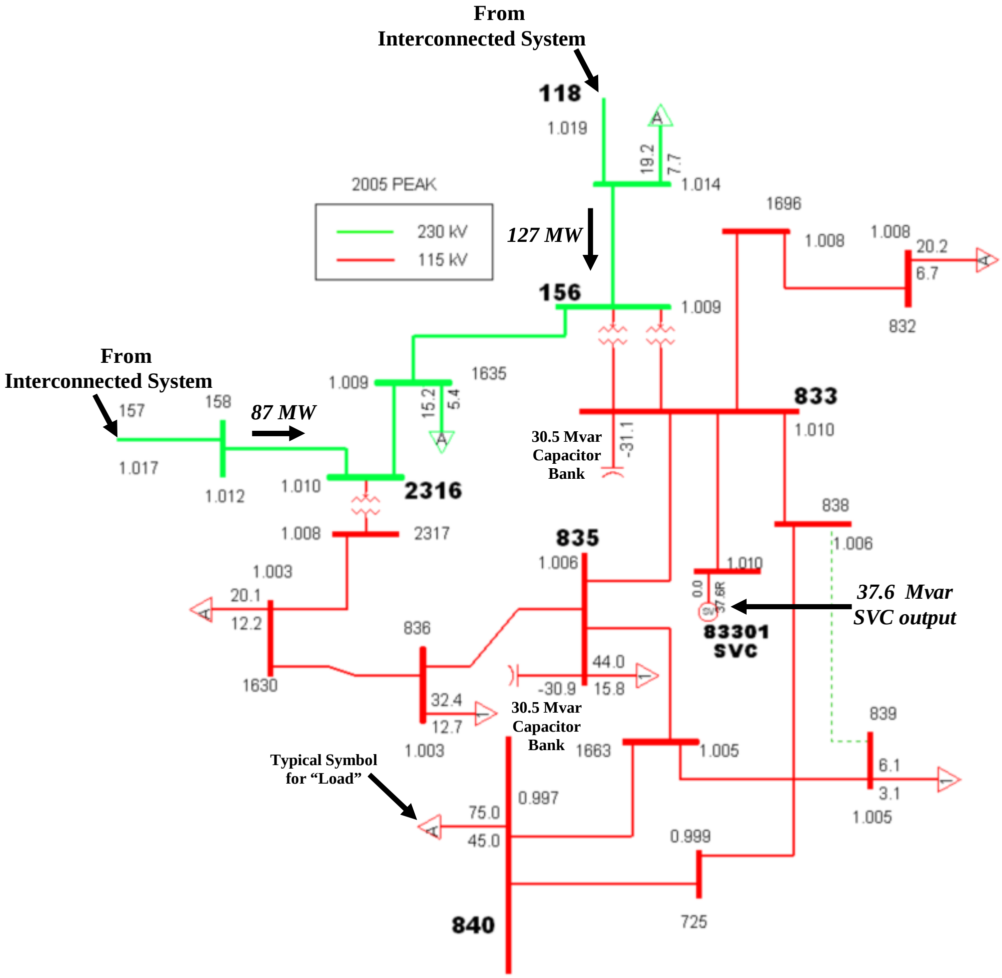


Figure 3-1. PSS/E one-line diagram for 2005 study area peak load flow case with the SVC.

3.2.1.2 2005 Light Load Network. The single-line diagram for the 2005 light load loading case is shown in Figure 3-2 with the total study area load 136.7 MW.

For all dynamic simulation, a PSS/E complex load model represents the loads in the study area, such that the total load in the load flow model at the respective buses is a composite model of large and small induction motors, and other distribution level equipment. The load at bus 840 is 55 MW and 45 Mvar modeled as 100% constant power, and the remaining loads in areas surrounding the study area are modeled as 10% constant power and 90% constant current. Other dynamic load models are discussed in [16] [17] [18] [19].

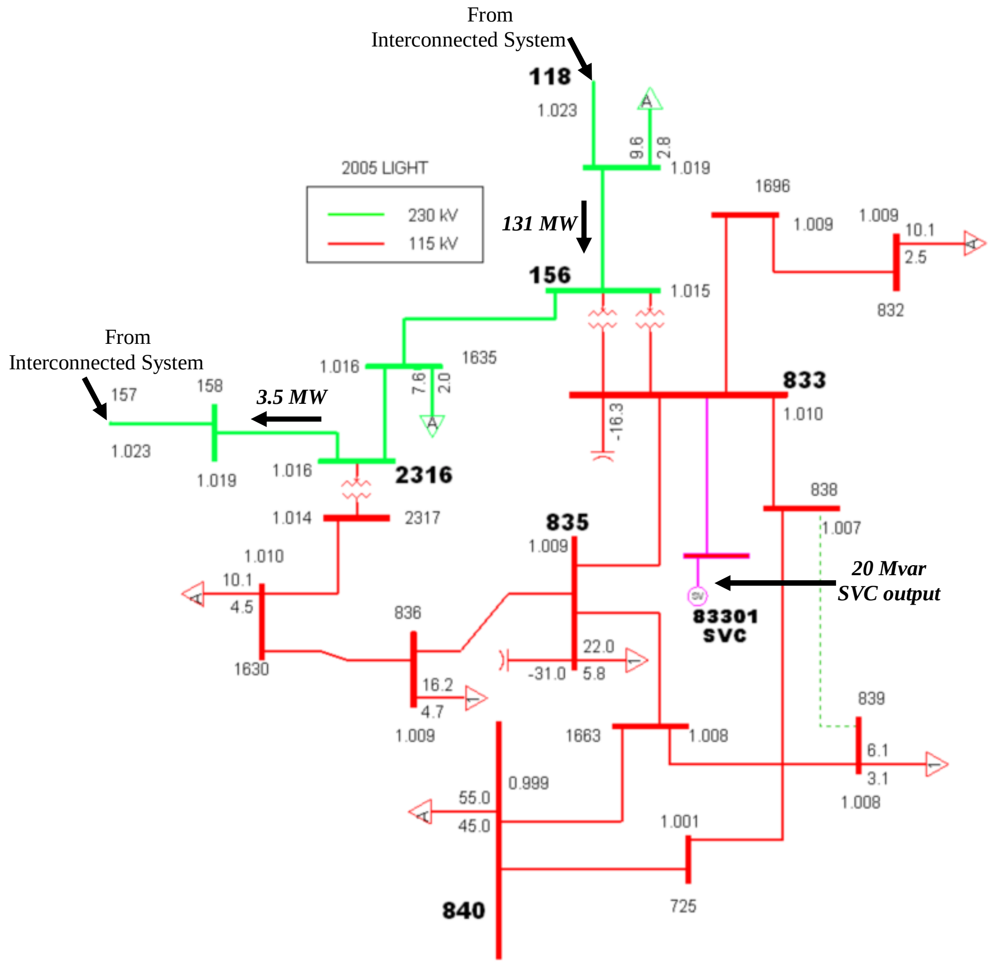


Figure 3-2. PSS/E one-line diagram for 2005 study area light load flow case with the SVC.

3.2.1.3 Dynamic Complex Load Model. As previously mentioned, a percentage of the load in the study area is modeled as a "complex load model" for the dynamic analysis, which is the utility's typical practice. In PSS/E, the dynamic load library model CLODZN was used to represent a composite load of induction motors, lighting, transformer, and transformers/lines. This model is intended for situations where it is desirable to represent loads as non-linear at the dynamic level, as distinct from the constant real and reactive power models used in load flow.

Figure 3-3 illustrates how the load is represented at each load bus in the study area, including the input data for the CLODZN model. This model uses a specific "small motor" performance curve to represent the desired percentage of small motor load.

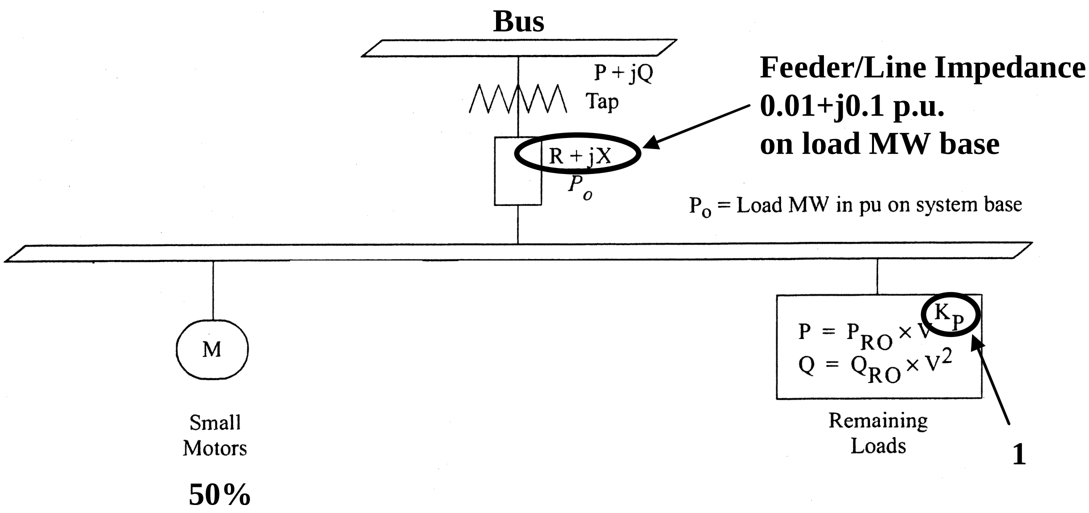


Figure 3-3. PSS/E dynamic load representation for the study area. (from PSS/E v.29 software manual)

The CLODZN dynamic model actually replaces all constant MVA, current, and admittance load (i.e., static load in loadflow model) with a composite load that is represented by 50% small motors, 0.01+j0.1p.u. distribution transformer and line impedance, and remaining P Q load as defined. In this case, the remaining 50% of the load at each bus in the study area are 100% constant current for P and 100% constant impedance for Q.

3.2.2 0 to 87 MVAR SVC MODEL AT 115 KV BUS 833

The 0 to 87 MVAR SVC at 115 kV bus 833 is a shunt device operated to provide rapid voltage control and dynamic reactive power support. Figure 3-4 shows the key components of the FC/TCR configured SVC device and its connection to the power system (i.e., bus 833 in the model) which are:

- thyristor-controlled reactor (TCR)
- fixed capacitors tuned for harmonic filtering
- coupling (step-up) transformer

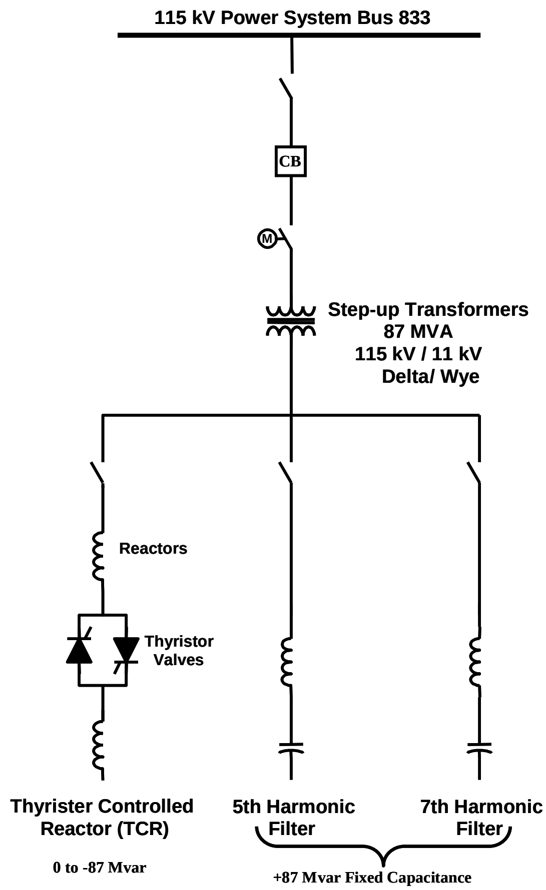


Figure 3-4. SVC configuration.

The SVC is operated as a shunt device at 115 kV bus 833 in the network model to provide capacitance for voltage support or inductance to reduce the bus voltage. The primary purpose of the fixed capacitors that make up the 5th and 7th harmonic filters in Figure 3-4 are to provide the capacitive Mvars to the system. The fixed capacitors are tuned to absorb the harmonics generated by the TCR operation. Although the SVC can provide support for short-term stability (system synchronizing torque) and power oscillation damping (system damping torque), its main function for this application is to provide voltage support and dynamic reactive power.

An SVC in principle is a controlled shunt susceptance (+/-B) as defined by the SVC control settings that injects reactive power (+Q) or removes reactive power (-Q) based on the square of its terminal voltage.

$$Q=B*V^2$$

In this application here, L and C are components are sized such that $Q \geq 0$ is the only operating range. The simplified block diagram for the SVC dynamic model is shown in Figure 3-5. The automatic voltage regulator (AVR) in the form of proportional and integral control, operates on a voltage error signal as computed in the summing block below

$$Verror = Vref - V - (Isvc * Xsl)$$

There are also measurement lags (Td) and thyristor firing transport lag (T1). The output B of this control block diagram feeds into the pulse generator controller that generates the required thyristor firing signal for the light-triggered thyristors controlling the reactor (TCR). Additional information on SVC models can be found in [22] [23] [24].

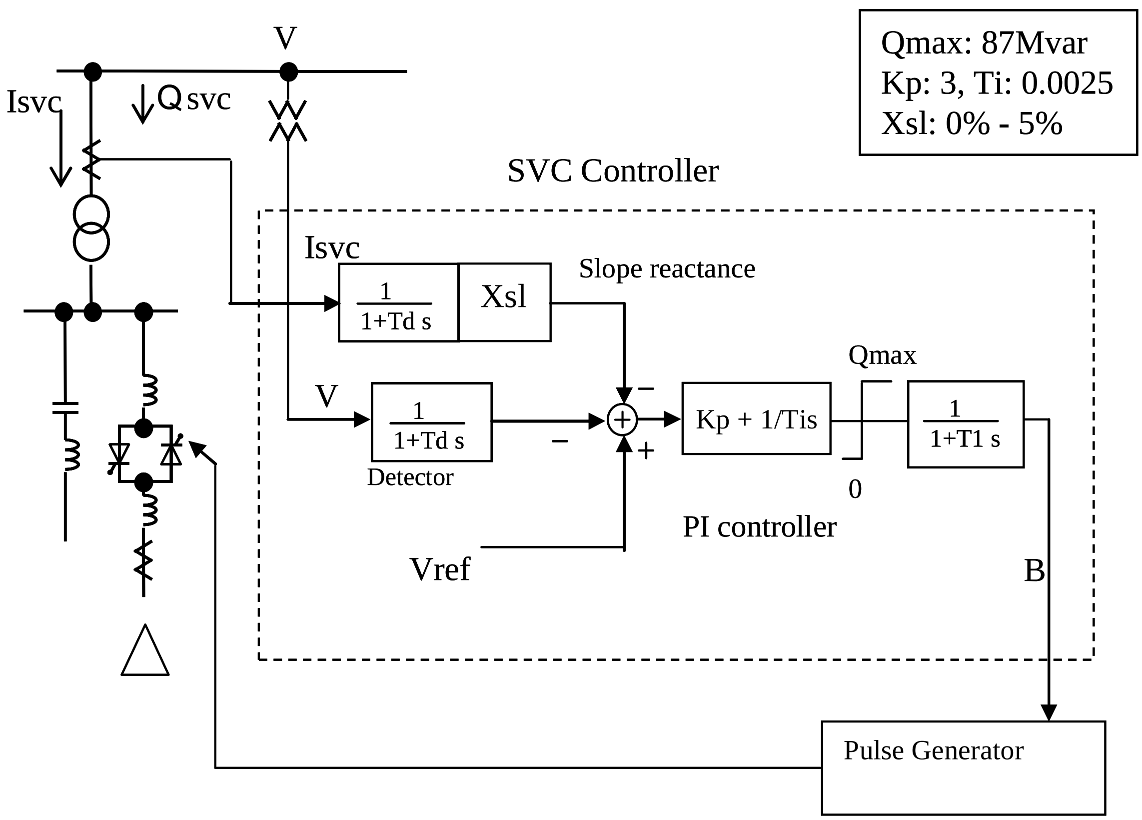


Figure 3-5. Detailed SVC block diagram.

The control objective is to maintain the system voltage at 115 kV bus 833 at 1.01 p.u. voltage. If the bus 833 begins to fall below 1.01 p.u., the SVC will inject reactive power (Q) into the system (within its controlled limits), thereby increasing the bus voltage back to its desired 1.01 p.u. voltage according to its slope setting, Xsl. On the contrary, if bus 833 voltage increases, the SVC will inject less (or TCR will absorb more) reactive power (within its controlled limits), and the result will be the desired bus voltage at bus 833.

The SVC's steady-state response will follow the V-I characteristic curve shown in Figure 3-6. The VI curve is used to illustrate the SVC rating and steady-state performance with the typical steady-state operating region being based primarily on the Vref, Xslope setting, and the system's impedance.

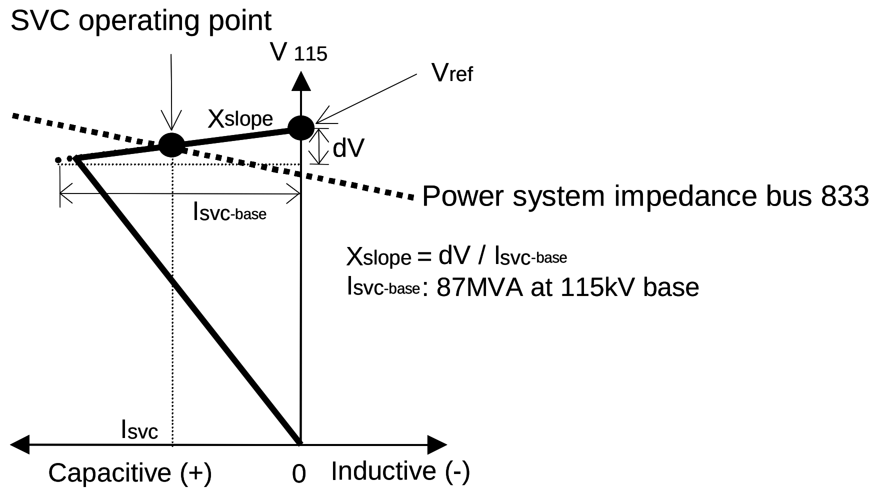


Figure 3-6. Steady-state volt-current (V-I) characteristics of the SVC.

The SVC's connectivity in the substation at bus 833 is illustrated in Figure 3-7, which shows two 230 kV buses and two 115 kV buses with the SVC connected to 115 kV Bus #1. The capacitors associated with the filters provide a source of leading reactive power that can be injected into the system, while the TCR branch controls the quantity of this reactive power delivered to the power system.

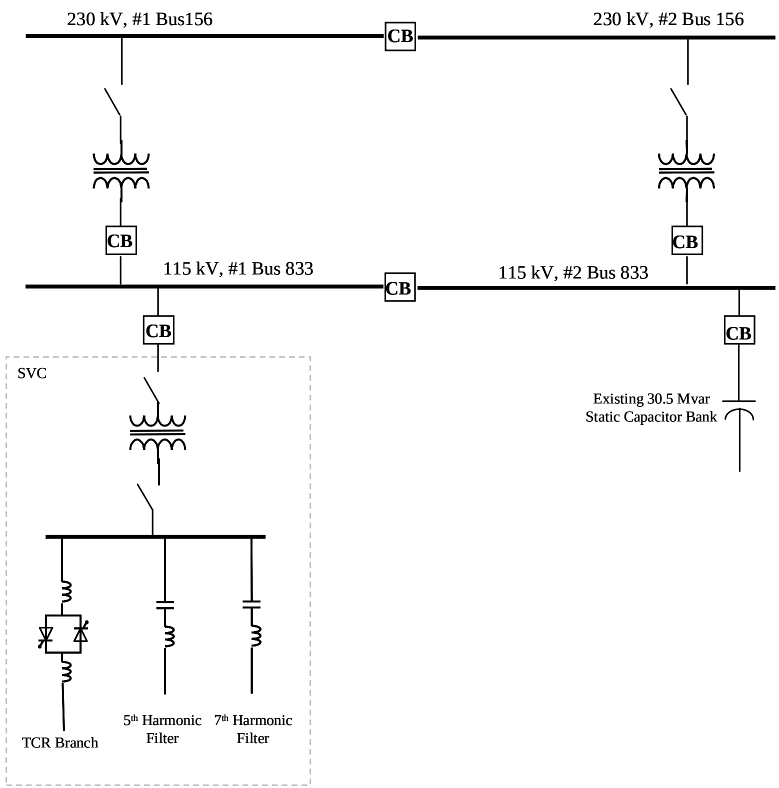


Figure 3-7. Substation one-line showing SVC connectivity.

3.2.3 PERFORMANCE CRITERIA

Specific performance criteria are defined to ensure adequate voltage regulation maintained in the study area. These criteria are used to determine that the SVC is adequately controlling the system's voltage and dynamic performance. The SVC is designed to ensure the following system performance criteria are maintained under peak and light load conditions.

<u>Post-Contingency Voltage Magnitude</u>

All post-contingency, steady-state transmission level voltages (Vss final) in the study area under N-1 contingency conditions must meet the following criteria:

- For peak loading condition and bus 840 net load of 75 MW and 45 Mvar

$$0.90 \text{ p.u.} < Vss\ final < 1.05 \text{ p.u.}$$

- For light loading condition and bus 840 net load of 55 MW and 45 Mvar

$$0.95 \text{ p.u.} < Vss\ final < 1.05 \text{ p.u.}$$

Vss final is the calculated voltage at the end of the dynamic time simulation.

Additionally, all voltages following a disturbance in the study area must recover and cross their steady-state post-contingency voltage magnitude within 3 seconds.

Percent Voltage Deviation

- For capacitor switching at buses 833 and 835, the steady-state voltage deviation should be 2.5% or less.
- The desired voltage deviation performance requirements for regulated and unregulated buses are :
    1) For voltage recovery following a disturbance, voltage should not exceed 5% deviation for *un-regulated* transmission buses, and 8% deviation for *regulated* transmission buses. Bus 840 and 839 are un-regulated buses, and the remaining buses in the study area are regulated.

Figure 3-11 shows the device rating and transient calculation of a sample dynamic simulation plot, and identifies the monitored parameters used in building the data tables and to determine if the simulation results meet the performance criteria.

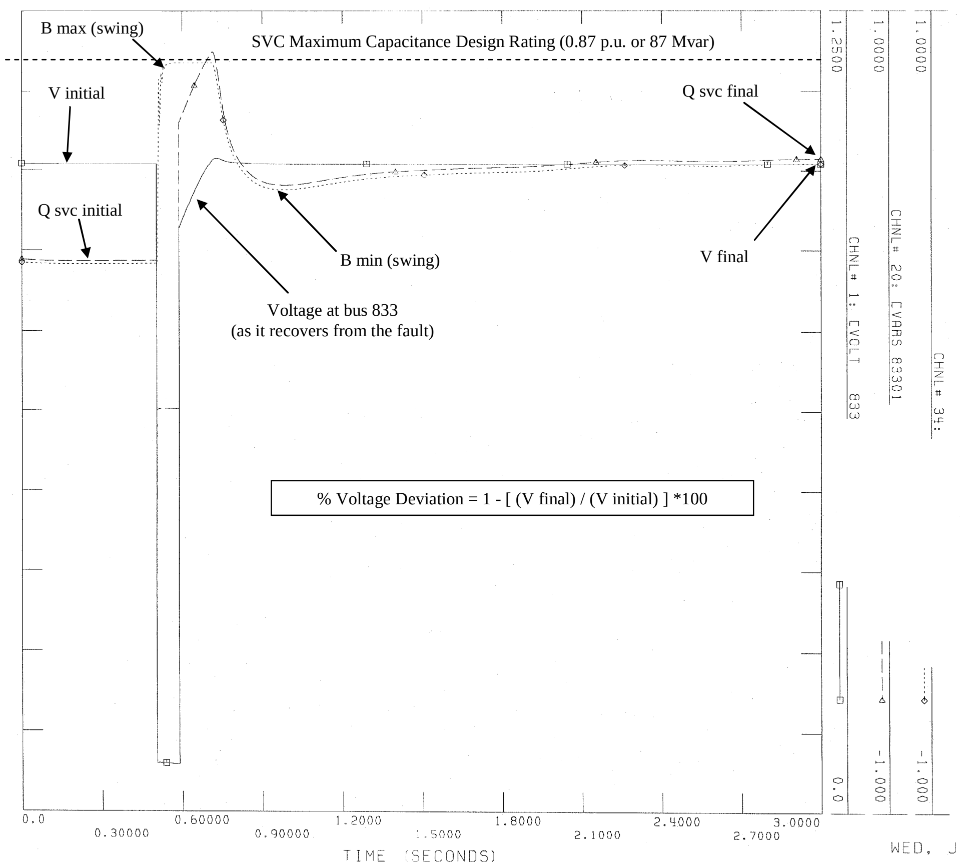


Figure 3-8. Example of dynamic simulation identifying monitored parameters to ensure compliance with performance criteria.

3.3 APPROACH AND RESULTS OF THE DYNAMIC PERFORMANCE ANALYSIS

This section explains the system dynamic performance analysis of the power system with and without the 0 to 87 Mvar, SVC at the 115 kV bus 833. The results of this study were compared to the utility's performance criteria.

For this dynamic performance analysis, eleven fault cases and four capacitor bank switching cases were analyzed for both peak and light load conditions for the 2005 system. The fault locations that were studied are identified in Figure 3-9. In addition, two of the most limiting cases with the SVC for peak and light condition were simulated with no SVC to quantify the improvement of the power system with the SVC in-service.

This analysis does not directly report on fault current sensing and circuit breaker operation to clear faults. Only the time for protection and circuit breaker operation, fault location, and line cleared/opened are considered when analyzing the ***system's response*** *to a disturbance and the* ***SVC's response*** *to a disturbance.*

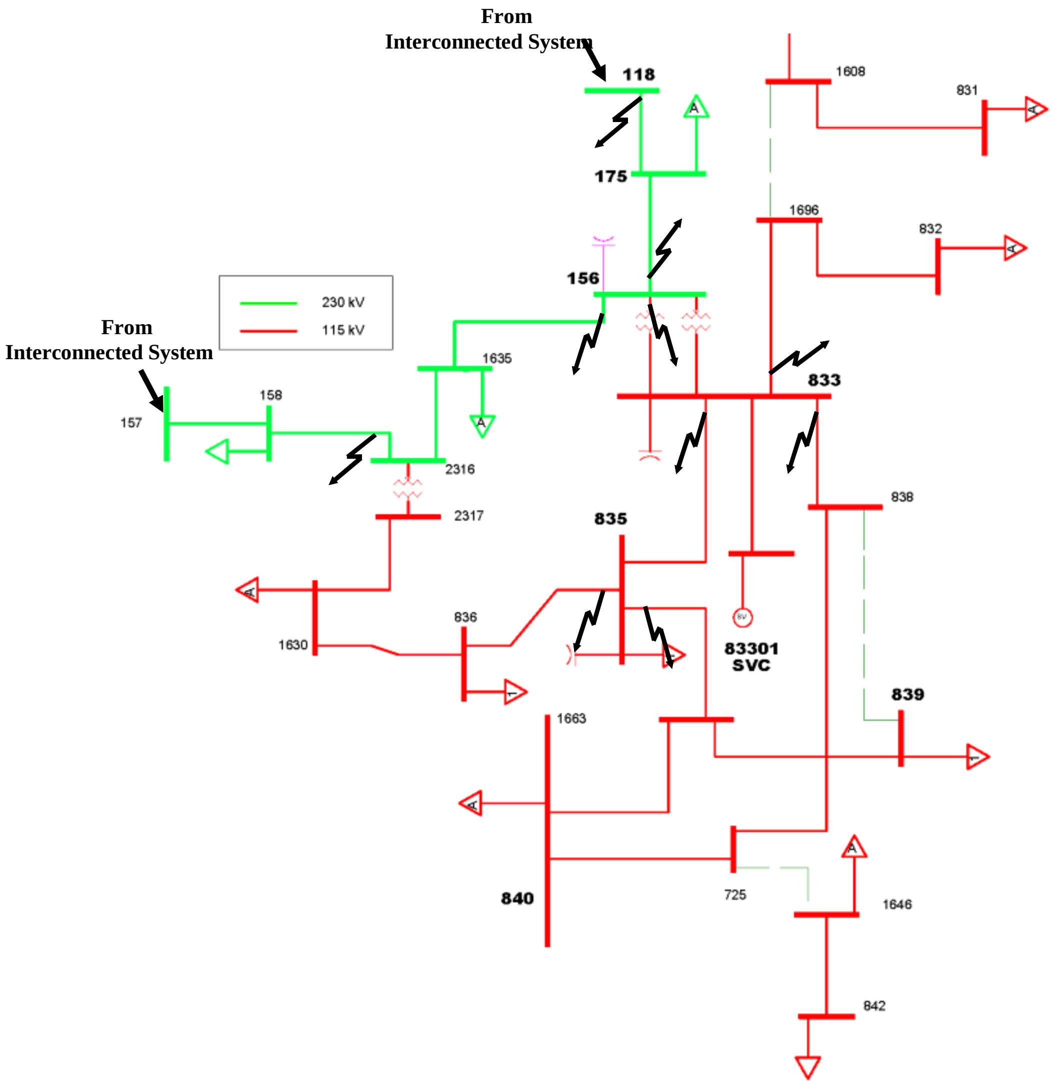


Figure 3-9. Fault locations analyzed for the system dynamic performance analysis.

3.3.1 2005 PEAK LOAD ANALYSIS

Bus loads are assigned to their 2005 peak MW and Mvar values and a steady-state calculation of the network voltages and power flows are obtained. In the load flow for all peak cases, the capacitor banks at the bus 833 and bus 835 are ON to maintain the voltage in the steady-state load flow case. The dynamic analysis was conducted by first considering fault cases local SVC connection point (i.e., the 115 kV bus 833). For example, a dynamic simulation case was conducted for a 3-phase fault at the bus 833 end of each 115 kV transmission line connected to this bus. The fault was cleared in the simulation by tripping the transmission line (or branch) according to the fault clearing data, and the simulation result was analyzed by extracting information from the simulation plot, as illustrated in the example in Figure 3-8. This information was tabulated in data tables to allow for clear comparison of the simulation result to the performance criteria. A separate simulation was analyzed for each branch connected to bus 833.

After considering all faults local to bus 833, wide area faults were investigated based on the suggested cases and clearing times.

Additionally, four capacitor bank switching case were investigated by switching the capacitor banks at bus 833 and 835.

3.3.1.1 Results for Peak Load Conditions - NO SVC. To quantify the improvement of the power system with the SVC in-service, two cases were simulated with NO SVC. Table 3-1 provides a description of each NO SVC peak load simulation case by identifying such items as the casename, base network condition, loading information, location of the fault event, branch (i.e., transmission line, transformer) cleared as s result of the fault, and the clearing time (i.e., time to remove fault and trip transmission line).

Table 3-1. Description of 2005 Peak Load Fault Cases With NO SVC

CASE	BASE CONDITION	BUS 840 LOAD (net load-as seen by the System)	EVENT	BRANCH(ES) CLEARED	VOLTAGE LEVEL	CLEARING TIMES (cycles)
P05X75S3q	2005 PEAK NO SVC	75 + j45	3-PH LINE FAULT at Bus 118	Bus 156 - Bus 118	230 kV	6 [1]
P05X75S9a	2005 PEAK NO SVC	75 + j45	3-PH BUS FAULT at Bus 156	Bus 156 TX	230 kV	6.5 [1]

(1) Clearing time includes a 2 cycle margin

In Figure 3-10 below is the time domain simulation plot for case P05X75S3q, as described in Table 3-1, of the voltage at buses 833, 839, and 840 on a per unit scale (with a voltage base of 230 kV). The first ½ second of the simulation shows the initial, pre-disturbance voltage to be very near 1.0 p.u. Then at 0.5 seconds the fault is applied resulting in a significant drop in voltage to approximately 0.2 p.u. for the time the fault is applied (6 cycles). At time 0.6 seconds in the simulation (0.5 sec + 6 cycles) the fault is removed and the 230 kV transmission line from bus 156 to bus 118 is cleared. After the fault is cleared, the voltage attempts to recover back to its initial condition, but only reaches to about 0.87 p.u. to 0.89 p.u. This reduced voltage level is present because the loss of the 230 kV line from bus 118 to 156 (with 127 MW line flow) created a “weak” connection to remote generation source(s) that was providing power to the loads in this study area.

The information identified in Figure 3-10 was extracted for the simulation plot and incorporated into Table 3-2 for casename P05X75S3q. This same process was repeated for casename P05X75S9a.

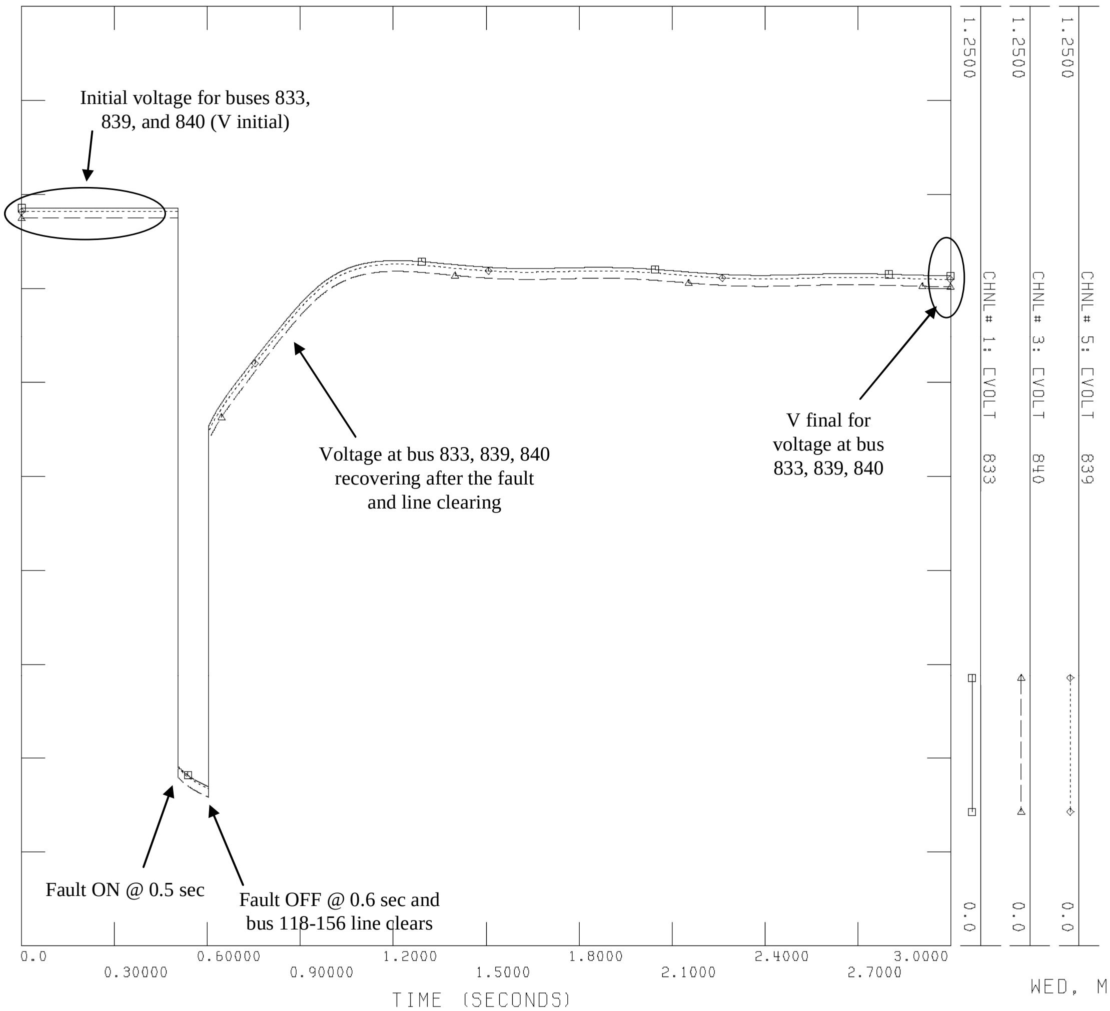


Figure 3-10. Dynamic simulation plot for the NO SVC case P05X75S3q.

It is shown here that 1 of the 2 the dynamic simulations with 2005 peak load case do not meet the performance criteria since the voltages at buses 833, 839, 840 are less than the performance criteria that requires the voltage to be above 0.90 p.u. Since 2005 is first year that the SVC is needed, and therefore the year of its installation, it is expected that the performance criteria is only slightly violated. This simulation case verifies that dynamic voltage support is needed for the 2005 peak case.

Table 3-2. Simulation Results of 2005 Peak Load Fault Cases With NO SVC

	PRE-CONTINGENCY				POST-CONTINGENCY						
Case	Q svc initial (mvar)	V initial (p.u.) regulated bus Bus 833	V initial (p.u.) unregulated bus Bus 840	V initial (p.u.) unregulated bus Bus 839	V final (p.u.) regulated bus Bus 833	V final (p.u.) unregulated bus Bus 840	V final (p.u.) unregulated bus Bus 839	Meet all voltage deviation criteria? regulated bus < 5% un-regulated bus < 8%	Meet steady-state voltage criteria? 0.90 < Vss final < 1.05	Q svc final (mvar)	SVC Swing Bmax-Bmin
P05X75S3q	no SVC	0.98	0.97	0.98	0.89	0.87	0.88	NO	NO	no SVC	no SVC
P05X75S9a	no SVC	0.98	0.97	0.98	0.97	0.95	0.96	YES	YES	no SVC	no SVC

3.3.1.2 Results for Peak Load Conditions With SVC. Table 3-1 provides a description of each peak load simulation case with the 0 to 87 Mvar SVC modeled by identifying such items as the casename, base network condition, loading information, location of the fault event, branch (i.e., transmission line, transformer) cleared as s result of the fault, and the clearing time (i.e., time to remove fault and trip transmission line). Four capacitor bank switching cases were simulated for events at bus 833 and bus 835.

Table 3-3. Description of 2005 Peak Load Fault Cases With SVC

CASE	BASE CONDITION	BUS 840 LOAD (net load-as seen by the System)	EVENT	BRANCH(ES) CLEARED OR CAP BANK SW	VOLTAGE LEVEL	CLEARING TIMES [1] (cycles)
P05S75F01	2005 PEAK	75 + j45	3-PH LINE FAULT at Bus 2316	Bus 2316 - Bus 157	230 kV	5
P05S75F02	2005 PEAK	75 + j45	3-PH LINE FAULT at Bus 156	Bus 2316 - Bus 156	230 kV	4
P05S75F03	2005 PEAK	75 + j45	3-PH LINE FAULT at Bus 156	Bus 156 - Bus 118	230 kV	4
P05S75S3d	2005 PEAK	75 + j45	3-PH LINE FAULT at Bus 156	Bus 156 - Bus 118	230 kV	6
P05S75F04	2005 PEAK	75 + j45	3-PH LINE FAULT at Bus 835	Bus 2316 - Bus 835	115 kV	4
P05S75F05	2005 PEAK	75 + j45	3-PH LINE FAULT at Bus 156	Bus 835 - Bus 156	115 kV	4
P05S75F06	2005 PEAK	75 + j45	3-PH LINE FAULT at Bus 835	Bus 835 - Bus 840	115 kV	4
P05S75F07	2005 PEAK	75 + j45	3-PH LINE FAULT at Bus 156	Bus 156 - Bus 840	115 kV	4
P05S75F08	2005 PEAK	75 + j45	3-PH LINE FAULT at Bus 156	Bus 156 - Bus 832	115 kV	4
P05S75F09	2005 PEAK	75 + j45	3-PH BUS FAULT at Bus 156	Bus 156 TX	230 kV	4.5
P05S75S9a	2005 PEAK	75 + j45	3-PH BUS FAULT at Bus 156	Bus 156 TX	230 kV	6.5
P05_SWCPON_833	2005 PEAK	75 + j45	ENERGIZE CAP BANK	Bus 156	115 kV	NA
P05_SWCPOF_833	2005 PEAK	75 + j45	DEENERGIZE CAP BANK	Bus 833	115 kV	NA
P05_SWCPON_835	2005 PEAK	75 + j45	ENERGIZE CAP BANK	Bus 835	115 kV	NA
P05_SWCPOF_835	2005 PEAK	75 + j45	DEENERGIZE CAP BANK	Bus 835	115 kV	NA

(1) The design clearing times for the standard protection in cases P05S75F01 through P05S75F09 is between 4 and 5 cycles as shown in Table 3-3. The utility specification for the Static Var System describes cases P05S75F03 and P05S75F09 with a 2 cycle margin in addition to the design clearing time. This is the basis for cases P05S75S3d and P05S75S9a, which are also shown in Table 3-3.

In Figure 3-11 below is the time domain simulation plot for case P05S75S3d, as described in Table 3-3, of the voltage at bus 833, the SVC susceptance, and the SVC reactive power output on a per unit scale (with a base voltage 115 kV and an MVA base of 100 MVA). The first ½ second of the simulation shows the initial, pre-disturbance voltage to be 1.01 p.u., the SVC susceptance (B) at 36, and the SVC reactive power (Q) output at 37 Mvar. The voltage is 1.01 p.u. because this is the desired operating voltage for bus 833 (also referred to as the reference voltage), therefore the SVC will adjust it susceptance to regulate the voltage at this desired value. Then at 0.5 seconds the fault is applied resulting in a significant drop in voltage and a very fast response of the SVC to increase its susceptance to its maximum rated limit of 87 Mvar (0.87 p.u.). (Note that an increase in susceptance translates to an increase capacitance because the thyristor valve firing angle is increases causing the TCR to absorb less of the fixed capacitor Mvars). The reactive power of the SVC shown in Figure 3-11 is the square of the bus 833 voltage times the SVC susceptance. At time 0.6 seconds in the simulation, the fault is removed and the 230 kV transmission line from bus 156 to bus 118 is cleared. After the fault is cleared, the voltage at bus 833 recovers rapidly since the SVC is at its maximum limit until the voltage reaches the reference voltage. Once the reference voltage is reached, the SVC begins to vary is output to regulate the bus voltage at 1.01 p.u. At the end of the simulation, the voltage and SVC output is recorded in Table 3-4. As mentioned in section 3.3.1.1, clearing the 230 kV transmission line between buses 118 and 156 creates a "weak" connection to generation sources, however the SVC provides the necessary reactive power to rapidly support and regulate the study area voltages following this major disturbance.

The information identified in Figure 3-10 was extracted from the simulation plot and incorporated into Table 3-4 for casename P05S75S3d. This same process was repeated for all cases described in Table 3-3 with results indicated in Table 3-4.

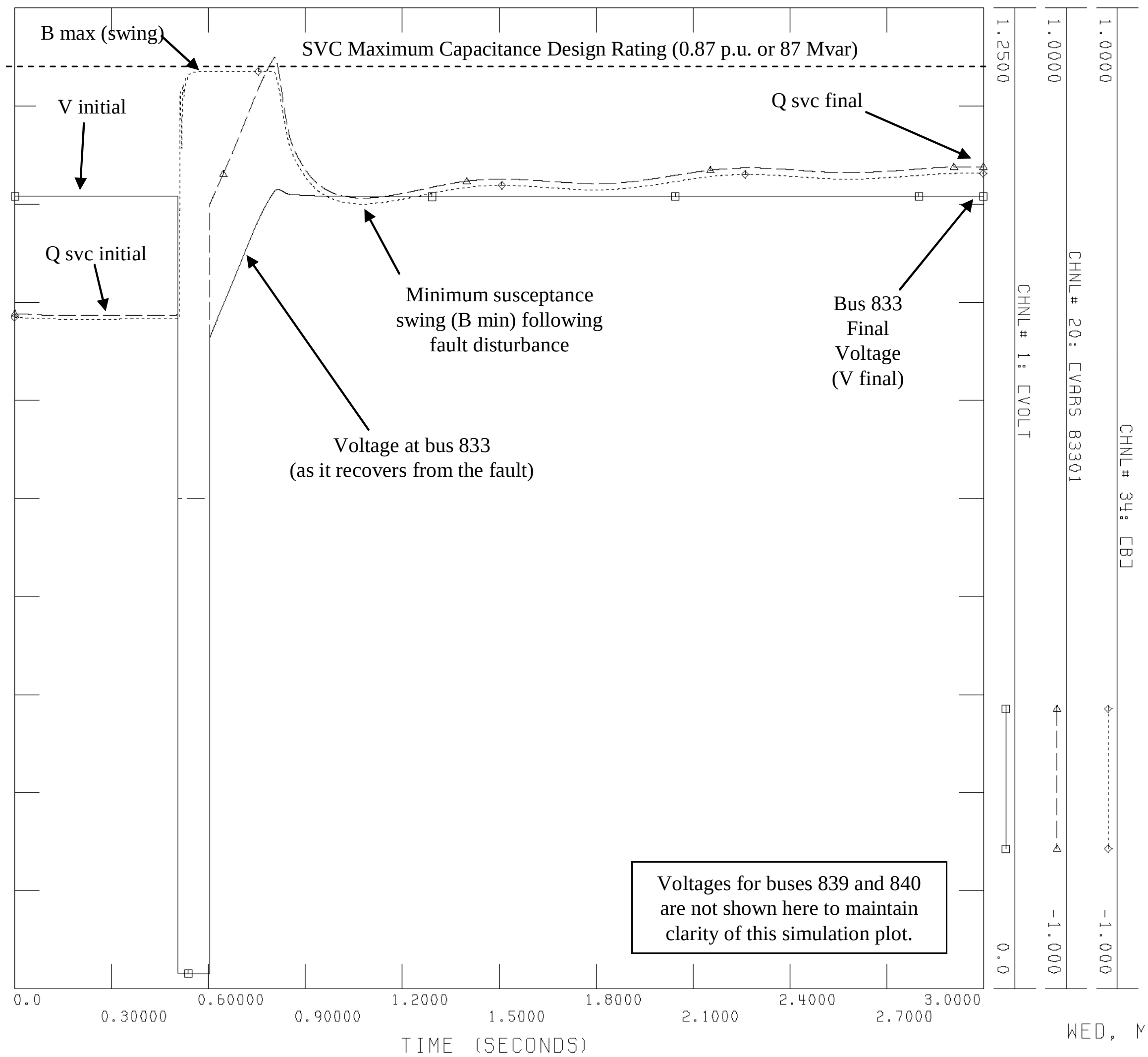


Figure 3-11. Dynamic simulation plot including 0 to 87 Mvar SVC for fault case P05S75S3d

A review of Table 3-4 indicates that a the to 87 Mvar SVC located at bus 833 provides voltage support and regulation to meet all the performance criteria for the 2005 peak load conditions over a range of major system disturbances.

Table 3-4. Simulation Results of 2005 Peak Load Fault Cases With SVC

	PRE-CONTINGENCY				POST-CONTINGENCY						
Case	Q svc initial (mvar)	V initial (p.u.) regulated bus Bus 833	V initial (p.u.) unregulated bus Bus 840	V initial (p.u.) unregulated bus Bus 839	V final (p.u.) regulated bus Bus 833	V final (p.u.) unregulated bus Bus 840	V final (p.u.) unregulated bus Bus 839	Meet all voltage deviation criteria? regulated bus < 5% un-regulated bus < 8%	Meet steady-state voltage criteria? 0.90 < Vss final < 1.05	Q svc final (mvar)	SVC Swing Bmax-Bmin
P05S75F01	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	63	87-55
P05S75F02	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	35	87-27
P05S75F03	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	67	87-62
P05S75S3d	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	67	87-60
P05S75F04	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	9	87-5
P05S75F05	37	1.01	0.99	1.00	1.01	0.98	1.00	YES	YES	34	87-28
P05S75F06	37	1.01	0.99	1.00	1.01	0.98	0.98	YES	YES	36	87-30
P05S75F07	37	1.01	0.99	1.00	1.01	0.98	cleared	YES	YES	39	87-33
P05S75F08	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	26	87-20
P05S75F09	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	42	87-38
P05S75S9a	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	44	87-32

The system dynamic performance results for all peak cases show that the initial output of the SVC (or steady-state, all elements in service) is 37 Mvar. The most limiting fault case from the system dynamic performance results is case P05S75F03d with the final SVC output at 67 Mvar. This case applies a fault at the bus 156 end of the 230 kV line between bus 156 and 118, and clears the line in 6 cycles. Therefore, this case is categorized as the most limiting case.

The results of the capacitor bank switching cases essentially show a displacement of Vars based on whether the 30.5 Mvar capacitor is switched ON or OFF. For example, in case P05_SWCPON_833, the capacitor bank at bus 833 is in the OFF state, and the SVC Q output is 68 Mvars. Then when the capacitor bank is switched to the ON state, the SVC Q output is reduced by approximately 30.5 Mvars while meeting the same control voltage objectives at bus 833. Therefore there is no voltage rise due to capacitor bank switching, as shown in Table 3-5 when the SVC is in-service.

Table 3-5. Capacitor Bank Switching Simulation Results of 2005 Peak Load Fault Cases With SVC

	PRE-CONTINGENCY				POST-CONTINGENCY						
Case	Q svc initial (mvar)	V initial (p.u.) regulated bus Bus 833	V initial (p.u.) unregulated bus Bus 840	V initial (p.u.) unregulated bus Bus 839	V final (p.u.) regulated bus Bus 833	V final (p.u.) unregulated bus Bus 840	V final (p.u.) unregulated bus Bus 839	Meet all voltage deviation criteria? V rise < 2.5%	Meet steady-state voltage criteria? 0.90 < Vss final < 1.05	Q svc final (mvar)	SVC Swing Bmax-Bmin
P05_SWCPON_833	68	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	37	67-35
P05_SWCPOF_833	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	68	68-36
P05_SWCPON_835	68	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	38	66-35
P05_SWCPOF_835	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	67	67-36

3.3.2 2005 LIGHT LOAD ANALYSIS

An analysis almost identical to that conducted for the 200 peak load conditions was conducted for the 2005 light load conditions to verify the 0 to 87 Mvar SVC at bus 833 adequately regulates system voltage and controls the system's dynamic performance in the study area. The light load case had a total study area load of 136 MW as opposed to the peak load case of 232 MW. Although the power in transmission line from bus 118 to 156 increased from the peak case to the light case, the total decrease in load in the study area presented the SVC with a "gentler" system to control the voltages. Therefore, the peak load case is considered the limiting case and results for the light load confirmed that the 87 Mvar SVC at bus 833 adequately controlled the system's dynamic performance and met all the performance criteria.

3.3.3 IMPACTS OF DELAYED FAULT CLEARING FOR THE 230 KV TRANSMISSION LINE BETWEEN BUS 156 AND BUS 118

The purpose of this subsection is to discuss and illustrate the impacts of delayed fault clearing for faults on the 230 kV transmission line close to bus 156 or bus 118 for peak and light loading conditions. For a fault close to one end of the 230 kV transmission line between bus 156 and 118, there may be a delay in tripping the circuit breaker furthest from the fault location based on the existing protection scheme. This general concept is illustrated in Figure 3-12.

Since a fault on this transmission line may be cleared after a delay time, it is expected to be more stability-limited than the standard protection clearing time of 6 cycles. This investigation discusses clearing faults on the bus 156-118 line when the fault occurs close to either end of the transmission line, exhibiting a delayed clearing time.

- For a 3-phase fault close to bus 156 end of the line, the fault is cleared by the circuit breaker at bus 156 in 4 cycles (6 cycles with margin), and cleared by the circuit breaker at bus 118 in a maximum delay time of 28 cycles.
- For a 3-phase fault close to bus 118 end of the line, the fault is cleared by the circuit breaker at bus 118 in 4 cycles (6 cycles with margin), and cleared by the circuit breaker at bus 156 in a maximum delay time of 28 cycles.

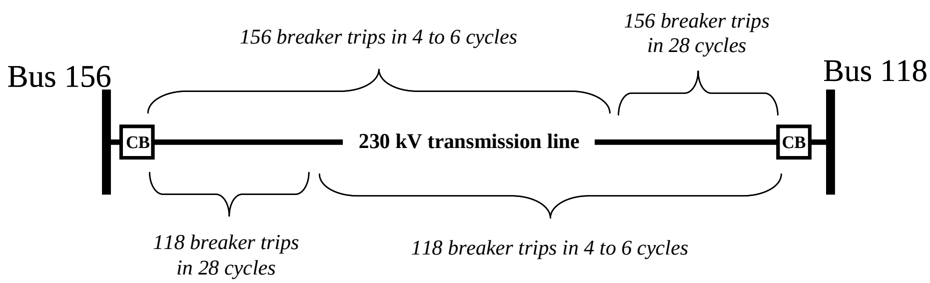


Figure 3-12. Protection scheme for clearing faults on the 230 kV transmission line between bus 156 and bus 118

3.3.3.1 Delayed Fault Clearing (bus 156-118) Under 2005 Peak Load Conditions

Two fault cases were simulated with NO SVC as shown in Table 3-6, to show the response of the system without an SVC. The dynamic simulation results are tabulated in Table 3-7

Table 3-6. Description of 2005 Peak Load Delayed Fault Clearing Cases With NO SVC

CASE	BASE CONDITION	BUS 840 LOAD (net load-as seen by the System)	EVENT	BRANCH(ES) CLEARED	VOLTAGE LEVEL	CLEARING TIMES (cycles)
P05X75S3h	2005 PEAK NO SVC	75 + j45	3-PH LINE FAULT at Bus 156	Bus 156 - Bus 118	230 kV	Bus 156 = 6 cycles Bus 118 = 28 cyc
P0X75S3m	2005 PEAK NO SVC	75 + j45	3-PH LINE FAULT at Bus 118	Bus 156 - Bus 118	230 kV	Bus 156 = 28 cycles Bus 118 = 6 cycles

Table 3-7. Simulation Results of 2005 Peak Load Delayed Fault Clearing Cases With NO SVC

	PRE-CONTINGENCY				POST-CONTINGENCY						
Case	Q svc initial (mvar)	V initial (p.u.) regulated bus Bus 833	V initial (p.u.) unregulated bus Bus 840	V initial (p.u.) unregulated bus Bus 839	V final (p.u.) regulated bus Bus 833	V final (p.u.) unregulated bus Bus 840	V final (p.u.) unregulated bus Bus 839	Meet all voltage deviation criteria? regulated bus < 5% un-regulated bus < 8%	Meet steady-state voltage criteria? 0.90 < Vss final < 1.05	Q svc final (mvar)	SVC Swing Bmax-Bmin
P05X75S3h	no SVC	0.98	0.97	0.98	0.89	0.88	0.89	NO	NO	no SVC	no SVC
P05X75S3m	no SVC	0.98	0.97	0.98	0.89	0.88	0.89	NO	NO	no SVC	no SVC

The results shown in Table 3-7 verify that dynamic voltage support is needed for the 2005 case to meet the required the system performance criteria. When the 230 kV transmission line from bus 156 to bus 118 opens, a significant source of power (~127 MW) are lost and the system voltages then become slightly depressed. For this delayed clearing time, the system voltages recover to levels that violate the performance criteria only slightly since 2005 is the first year that the SVC is needed.

Identical fault cases were simulated with the SVC in service with their corresponding case names P05S75S3h and P05S75S3m. Dynamic simulation plots of cases P05S75S3h and P05S75S3m are shown in Figure 3-13 through 3-16 for a 3-phase fault at each end of 156-118 transmission line under peak 2005 load conditions, with delayed clearing on the line end opposite of the fault. In comparing the simulation plots in Figures 3-13 and 3-15, it is evident that case P05S75S3m (fault at 118) is more stressful on the system than case P05S75S3h (fault at 156). The fault near bus 118 shown in Figures 3-15 and 3-16, occurs close-in to the substation at bus 118. This causes the standard protection for the breaker at bus 118 to clear in 6 cycles (includes 2 cycle margin) and delayed clearing of the circuit breaker at bus 156 in 28 cycles. This limiting fault holds bus 833 voltage to less than 0.90 p.u. for 1.3 seconds. Still, this case meets the performance criteria and will cause no problems with the operation of the SVC. This case is the most limiting case. The results of cases P05S75S3h and P05S75S3m are summarized in Table 3-13.

Table 3-8. Simulation Results of 2005 Peak Load Delayed Fault Clearing Cases With SVC
(Case Descriptions same as those shown in Table 3-6 except SVC is modeled)

	PRE-CONTINGENCY				POST-CONTINGENCY						
Case	Q svc initial (mvar)	V initial (p.u.) regulated bus Bus 833	V initial (p.u.) unregulated bus Bus 840	V initial (p.u.) unregulated bus Bus 839	V final (p.u.) regulated bus Bus 833	V final (p.u.) unregulated bus Bus 840	V final (p.u.) unregulated bus Bus 839	Meet all voltage deviation criteria? regulated bus < 5% un-regulated bus < 8%	Meet steady-state voltage criteria? 0.90 < Vss final < 1.05	Q svc final (mvar)	SVC Swing Bmax-Bmin
P05S75S3h	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	68	87-39
P05S75S3m	37	1.01	0.99	1.00	1.01	0.99	1.00	YES	YES	68	87-55

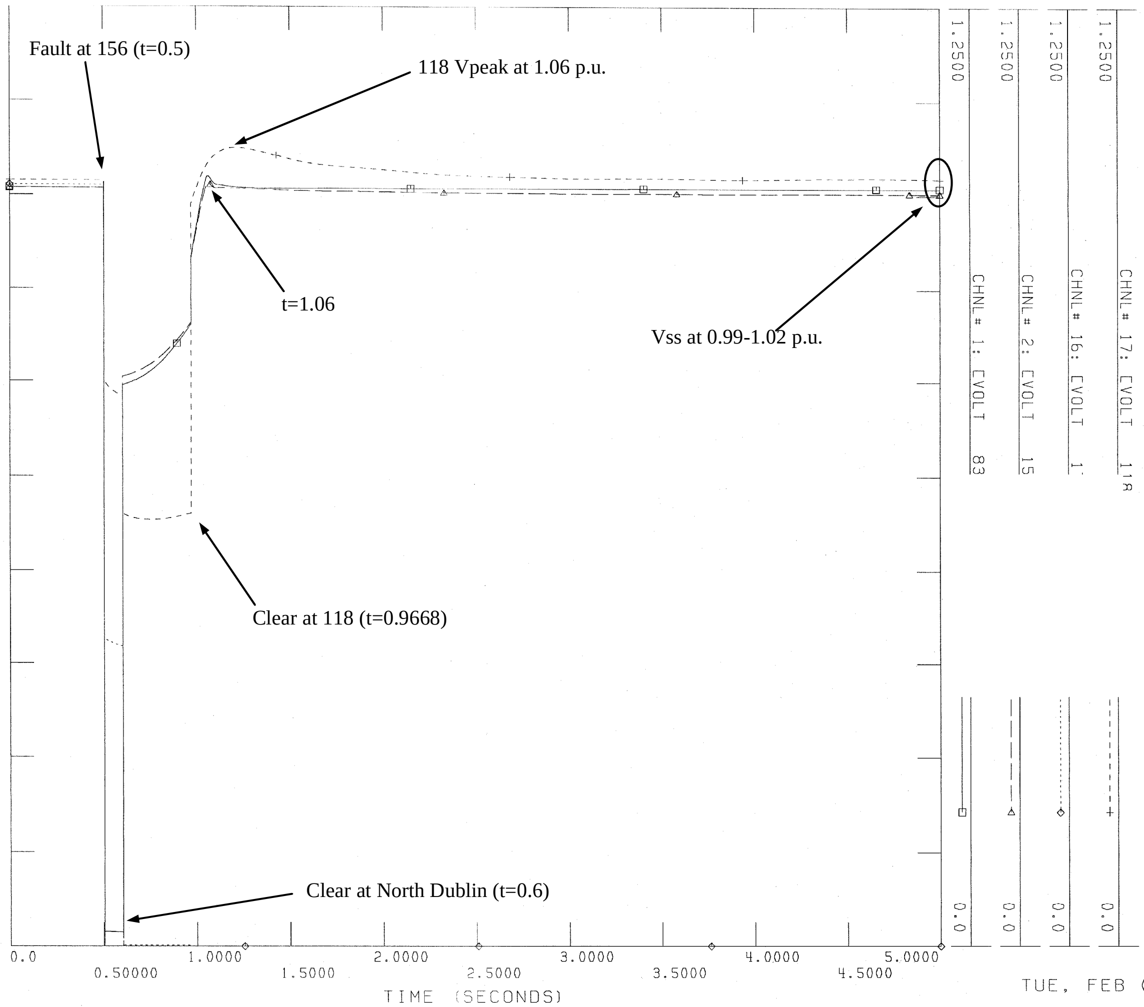


Figure 3-13. Voltage response for delayed clearing of 156-118 230 kV transmission line for a fault at 156 end for peak load conditions. (Clear 156 in 6 cycles and 118 in 28 cycles.)

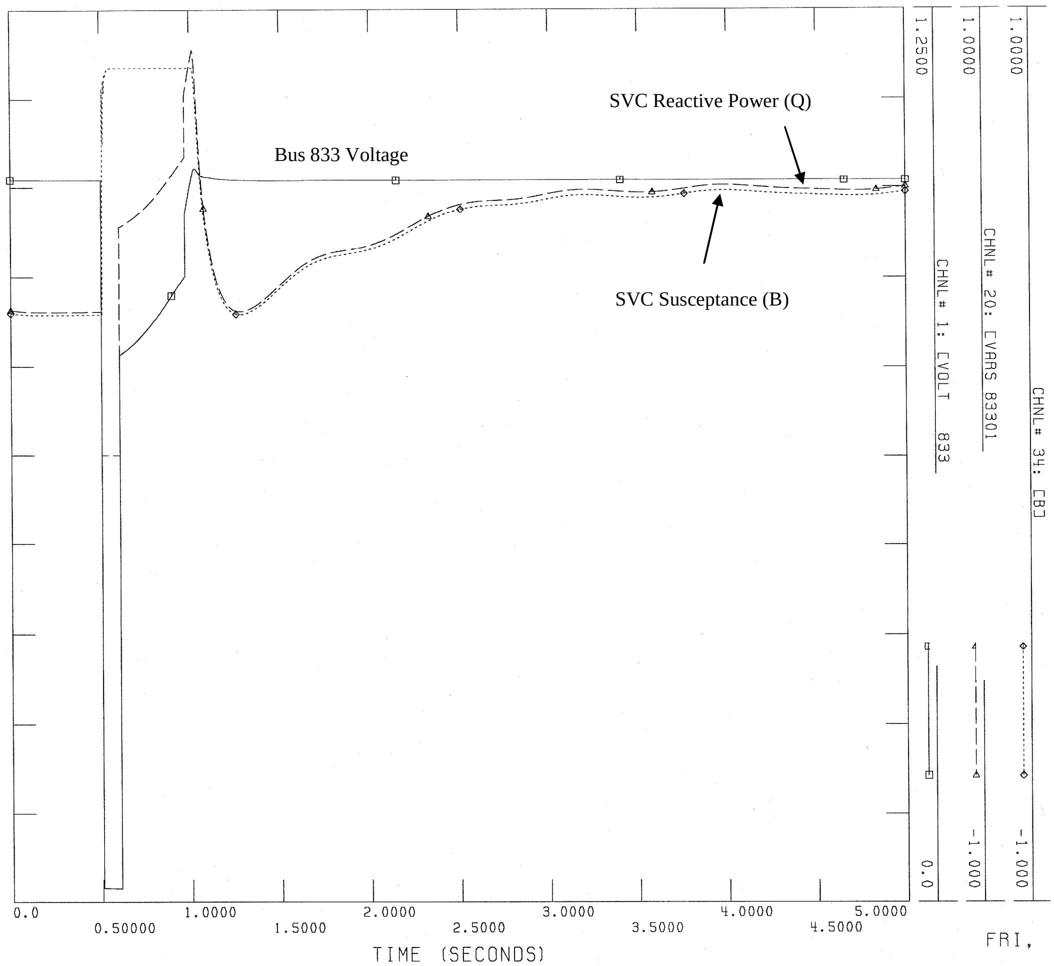


Figure 3-14. SVC response for delayed clearing of 156-118 230 kV transmission line for a fault at 156 end for peak load conditions. (Clear 156 in 6 cycles and 118 in 28 cycles.)

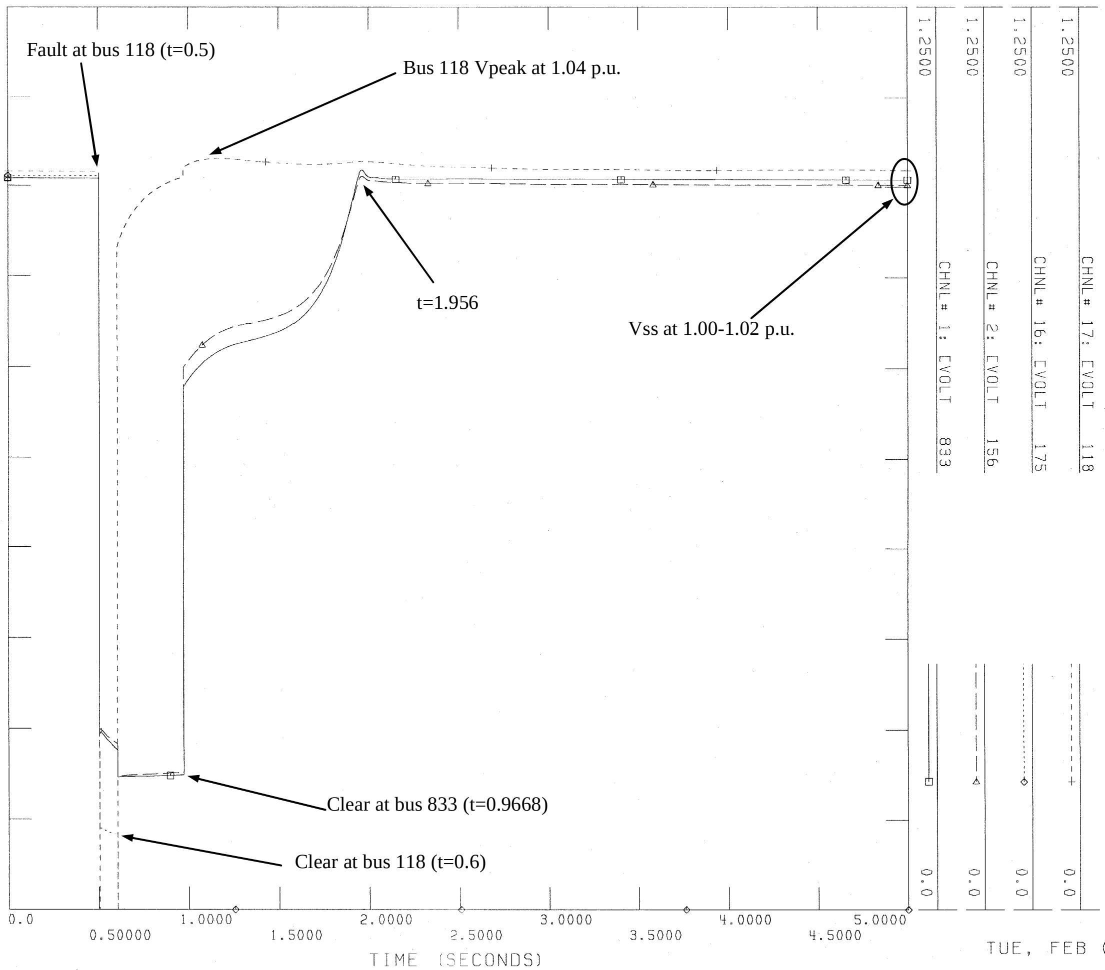


Figure 3-15. Voltage response for delayed clearing of 156-118 230 kV transmission line for a fault at bus 118 end for peak load conditions. (Clear bus 156 in 28 cycles and bus 118 in 6 cycles.)

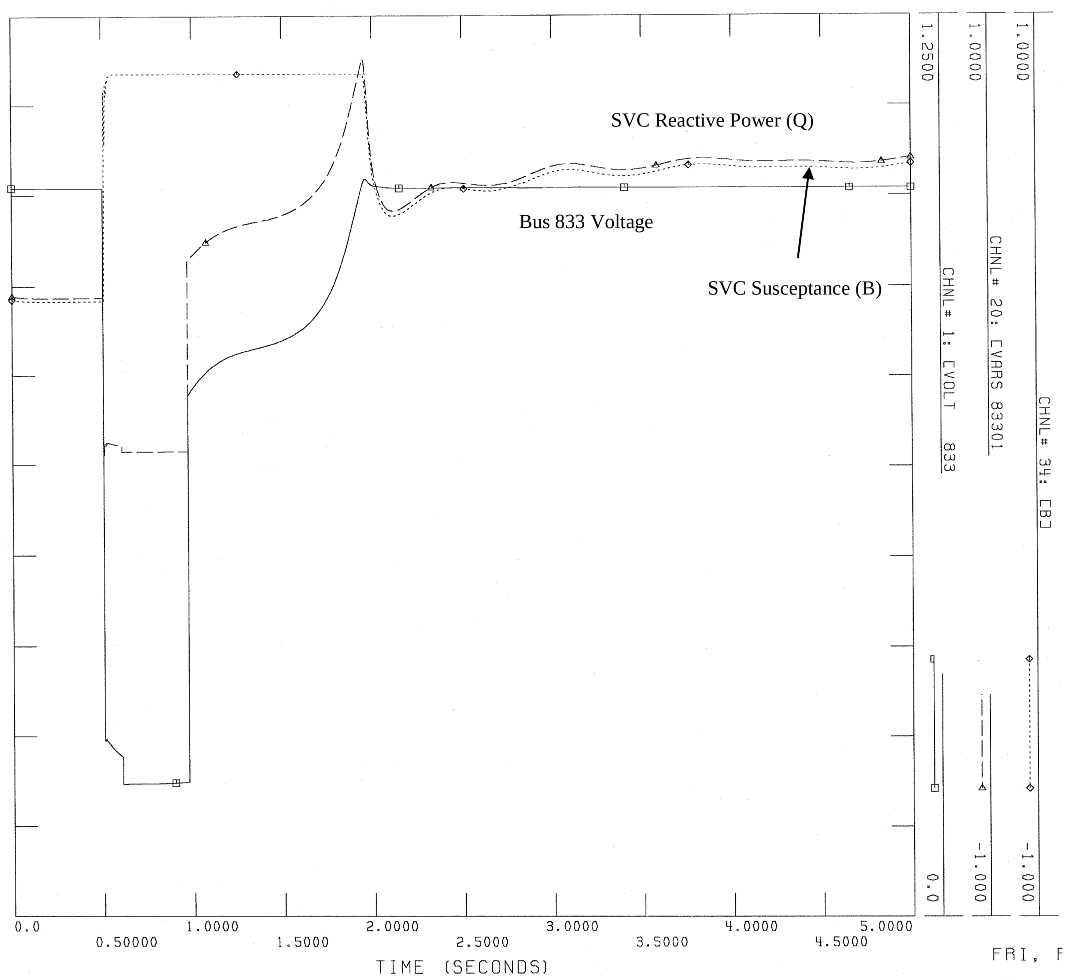


Figure 3-16. SVC response for delayed clearing of 156-118 230 kV transmission line for a fault at 118 end for peak load conditions. (Clear 156 in 28 cycles and 118 in 6 cycles.)

3.3.4 SUMMARY

This section presented the methodology, performance criteria, and results for the dynamic performance analysis for the 2005 system with the 0 to 87 Mvar SVC applied at bus 833 in the model discussed in this analysis. The results of the analysis showed that the SVC controls the system's dynamic performance during system disturbances for both 2005 peak and light load conditions, in addition to re-confirming the need for additional reactive power reinforcement. The most limiting case was identified as a loss of the 230 kV transmission line between bus 156 and bus 118, which resulted in a post-contingency, final SVC output of 67 Mvars under 2005 peak loading to maintain the dynamic performance criteria.

Delayed clearing of faulted transmission lines was investigated for the 2005 peak load case since these loading conditions provide the stability-limited results.

- **Delayed fault clearing on the 156-118, 230 transmission line**

  Results: Delayed fault clearing for a fault at the 118 end of the 156-118 230 kV transmission line was determined as the most limiting fault due to holding the bus 833 115 kV voltage to less than 0.90 p.u. for 1.3 seconds. Although this case is stressful on the system, it meets the system performance criteria and will cause no problems with the operation of the SVC under peak load conditions.

3.4 OVERALL CONCLUSIONS OF ANALYSIS

This analysis has verified that the 0 to 87 Mvar SVC at 115 kV bus 833 controls the system's dynamic performance and meets performance criteria during a wide range of disturbances for both 2005 peak and light load conditions.

The limiting case was identified as delayed clearing of a 3 phase fault at the bus 118 end of the 230 kV transmission line from bus 156 to bus 118.

4.0 CONCLUSION

This thesis research and analysis has demonstrated that modern transmission static var compensators can be effectively applied in power transmission systems to solve the problems of poor dynamic performance and voltage regulation in a 115 kV and 230 kV transmission system. Transmission SVCs and other FACTS controllers will continue to be applied with more frequency as their benefits make the network "flexible" and directed towards an "open access" structure.

Since SVC is a proven FACTS controller, it is likely that utilities will continue to use the SVC's ability to resolve voltage regulation and voltage stability problems. In some cases, transmission SVCs also provide an environmentally-friendly alternative to the installation of costly and often un-popular new transmission lines.

Dynamic performance and voltage control analyses will continue to be a very important process to identify system problems and demonstrate the effectiveness of possible solutions. Therefore, continual improvements of system modeling and device modeling will further ensure that proposed solutions are received by upper management with firm confidence.

In terms of cost effectiveness, the complete installation of the SVC is on the order of $8,000,000 compared to a new 230 kV transmission line from bus 118 to bus 156 which is on the order $19,000,000.

4.1 FUTURE WORK

Future work related to the study and analysis of voltage regulation and voltage stability should be focused in the area of load modeling. In particular, the static load characteristics and percentage of dynamic motor load needs to more accurately reflect what is in the "real system" under study. The load model has significant influence on the system's response to disturbances, and therefore significantly influences the rating of any proposed solution.

APPENDIX A

BASIS FOR SVC MVAR RATING

The network conditions of year 2012 provide the basis for the SVC rating of 0-87 Mvar. The total 2012 peak load for the study area is 267 MW as compared to the 2005 peak load of 232 MW. From Figure A-1, it is observed that the 230 kV transmission line from bus 118 to bus 156 carries a significant source of power to the area under study.

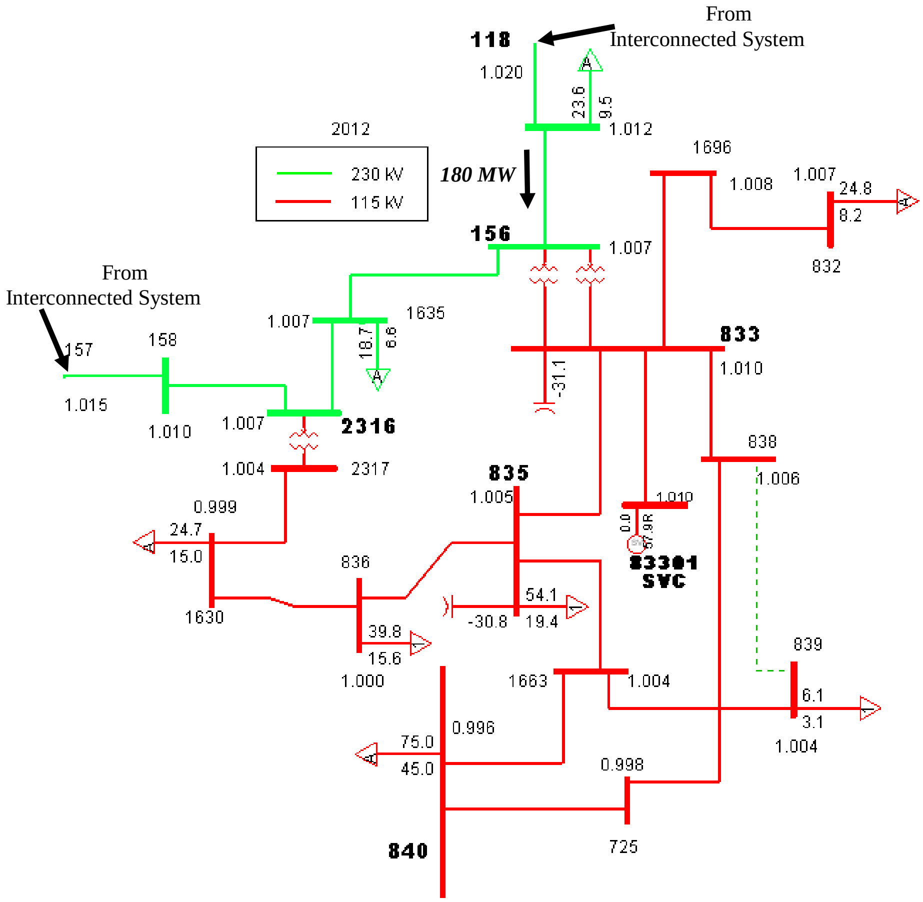


Figure A-1. PSS/E one-line diagram for 2012 study area peak load flow case with the SVC.

To determine if the rating of the SVC that meets the performance criteria, a dynamic simulation is run for a three-phase fault at bus 156 with subsequent line clearing between buses 156 and 118. After iterative simulations, the result is shown in Figure A-2 that compares the simulation run with and without the SVC in the system. A depressed voltage level at bus 833 of 0.82 p.u. (or 82% nominal) after this system disturbance is an unacceptable operating voltage level.

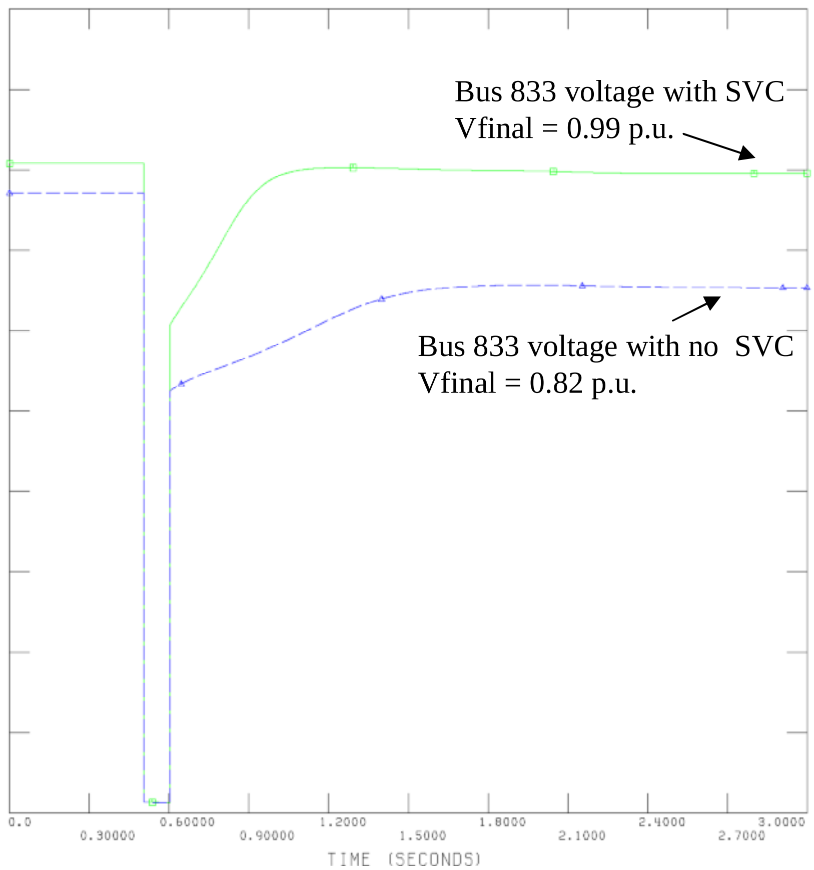


Figure A-2. Dynamic simulation plot comparing the bus 833 voltage with and without the SVC

Figure 3-2 illustrates that an 87 Mvar SVC connected to the 115 kV bus 833 improves the system voltage response from a final value of 0.82 p.u. to 0.99 p.u. The fault induced recovery time is significantly reduced by the rapid response of the SVC as seen by the voltage recovery in the first 1/2 second after fault clearing. In the year 2012, an outage of the 87 Mvar SVC will become the limiting contingency (in place of the bus 156 to 118 transmission line outage) that will demand the construction of another main source of power into this area such as a new 230 kV transmission line.

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