ASSET TRACKING USING A REAL-TIME LOCATING SYSTEM EMPLOYING A NOVEL LOCATION DETERMINATION METHOD

by

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Real-Time Locating Systems (RTLS) belong to a class of locating systems capable of remotely determining the location of tagged assets in an environment within a relatively short time frame (real-time). Signals from tags are received wirelessly by readers, which use information about the signal, to continuously determine the location of the tag relative to each reader. Using readers positioned at several locations around a tag offers multiple location readings, which can be compiled together at a central host to estimate the location of a tag in a two or three dimensional space. Location information from several vantage points also reduces the chance of false location estimates of a tag when one or more readers' location estimates contain some error.

Indoor asset tracking is a unique specialty of many types of RTLS, as Global Positioning Systems (GPS) have difficulty providing asset locations within buildings. RTLS deployments generally address the problems of determining the location of equipment and products in a warehouse or even tracking employees and files in an office. The most common RTLS uses a Wi-Fi infrastructure to determine the location of tagged assets. These systems employ Time-of-Arrival (ToA) or Received Signal Strength Indication (RSSI) techniques to wirelessly determine asset location. Scaling up a system that uses a Wi-Fi infrastructure to localize large numbers of tags introduces a significant wireless traffic burden, reducing data throughput for other users of the same Wi-Fi network. Both ToA and RSSI methods of localization suffer from significant

inaccuracies in reported location of assets and often are unable to determine which room an asset resides.

This thesis presents a new method for determining asset location that offers better accuracy than systems using ToA and RSSI techniques, and an RTLS that uses existing Wi-Fi infrastructures and commercial off-the-shelf parts (COTS) without placing excessive need on the Wi-Fi networks.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

PREFACE

I would like to express my gratitude to Dr. Marlin Mickle and Dr. Peter Hawrylak for their invaluable support and guidance. I am forever grateful for their help and the opportunities that they have given me.

1.0 INTRODUCTION

Increased commercial demand to improve processes, monitor patients and situations, and track people and assets has given Real-Time Locating Systems (RTLS) a unique set of problems to which they can offer solutions[13][14][15]. Real-Time Locating Systems offer the ability to remotely track people and assets. The following subsections will introduce RTLS, and some competing location determination technologies used in RTLS, as well as a novel method to determine the location of tagged assets, which is implemented and demonstrated in the RTLS development presented in this thesis.

1.1 BACKGROUND

One application in particular for RTLS is during crisis situations. An RTLS can be used to monitor first responders arriving at an incident such as a fire or bomb threat. The RTLS allows a situation commander to monitor the locations of the first responders within a building in real-time; accounting for first responders that become lost or having the location of an injured or fallen first responder. The RTLS in these situations can be used for planning actions based on real-time information of the whereabouts of the first responders, effectively allowing the situation commander to direct them to specific locations within a building, minimizing lost time during a crisis.

Public buildings, such as schools and office buildings, are ideal locations for RTLS deployment. Ultimately, tracking all people in these buildings would allow first responders, that arrive to a crisis situation, to have an accurate mapping of the location of students, personnel, etc. within the building. This would allow first responders to manage their efforts to where they would be needed most, and allow recovery of lost or trapped individuals far more quickly than in a sweeping search.

1.2 EXISTING RTLS TECHNOLOGIES

There are many unique methods that explore the problem of location determination in Real-Time Locating Systems; by far, the most commonly employed methods use Wi-Fi as the backbone by which a location-determining solution is designed [20][22][23][24]. Typically, these systems steal unused Wi-Fi cycles on a network, and for a relatively few number of tags (less than one-hundred), this does not adversely affect data traffic and throughput.

Typical Wi-Fi network infrastructures can support data traffic and an RTLS on a small scale, but scaling the system to track a greater number of tags (e.g. several hundred), will reduce the available bandwidth of the network for data traffic users and degrade system throughput. This dual-purpose usage of the Wi-Fi infrastructure also presents problems for accurate location determination, preventing sufficiently quick updates of tag locations [21].

Of the location-determination methods used in Wi-Fi based RTLS, the Time-of-Arrival (ToA) and Received Signal Strength Indicator (RSSI) are the most popular. The dynamics of the Radio Frequency (RF) environment are subject to changes from a variety of factors, including temperature, humidity, and objects within the propagation environment. These factors can cause

significant errors in location determination for whatever location determination method that is being used, including ToA and RSSI based systems. Many methods have been investigated to improve the accuracy in light of these factors, but they require complex signal processing and mathematical models which take time, adding overhead to location determination and reducing throughput of the system [16][17][18]. The following subsections will explore these popular techniques of location determination as well as the novel approach employed in the Real-Time Locating Systems designed and developed, which are the basis of this thesis.

1.2.1 Time-of-Arrival (ToA) and Received Signal Strength Indicator (RSSI)

While not the only location-determination techniques used in RTLS, Time-of-Arrival (ToA) and Received Signal Strength Indicator (RSSI) are certainly two very popular methods that Wi-Fi-based RTLS use to determining the location of a tag. The ToA location determination method makes use of the time that it takes for a signal, with a known velocity, to arrive at the destination or to return back to the source. The RSSI location determination method determines the amount of power in the received signal. Both methods are widely used, but as described in the introduction of Section 1.2, they can suffer from a variety of problems. The novel location determination method proposed in this thesis offers a competing method of location determination whose viability as a location determination method is assessed in the results (Section 9.0) of the RTLS designed with the novel location determination method. The overall system architecture for an RTLS implementing the ToA and RSSI methods of location determination is illustrated in Figure 1. This system architecture uses the Wi-Fi system (pictured as the wireless access point in the figure) as the interface to the transmitter. Computing the

location estimate of a transmitter is accomplished using the resources of the wireless access point.

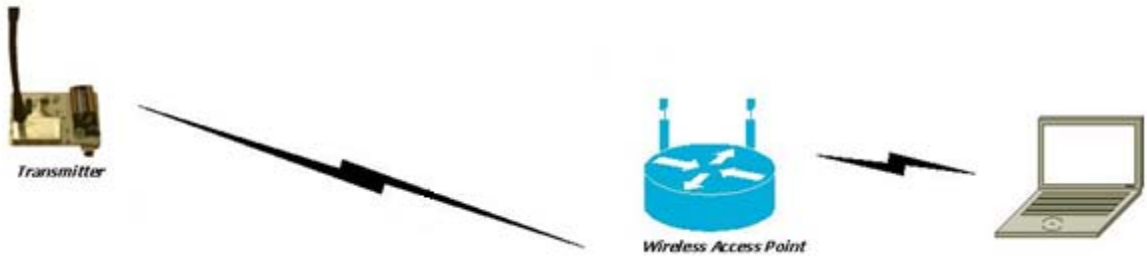


Figure 1: RTLS Architecture for ToA and RSSI Wi-Fi Based Systems

1.2.2 Receiver Sensitivity

The receiver sensitivity location determination method is a novel approach to tracking tags. With this method, the sensitivity of the receiver is adjusted in intervals – the intervals effectively create thresholds which represent boundaries. These boundaries represent incrementally differing degrees of receiver sensitivity – the closer a boundary is to the receiver, the poorer the receiver sensitivity is, while the converse is true – the farther away a boundary is from the receiver, the better the receiver sensitivity. The RTLS described in this thesis will explore the hardware and software necessary to implement this location determination method by establishing boundaries in which the asset is located.

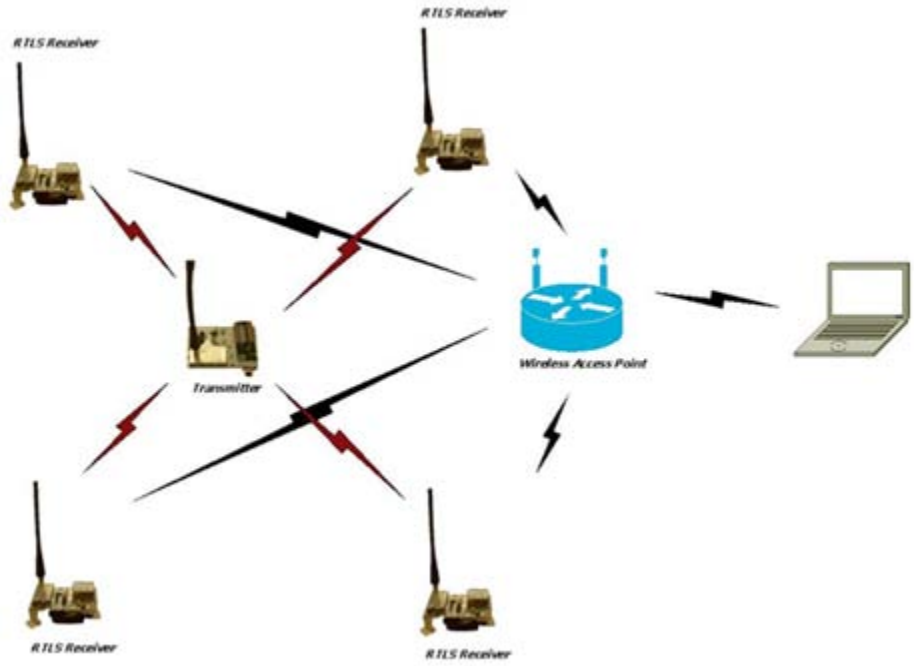
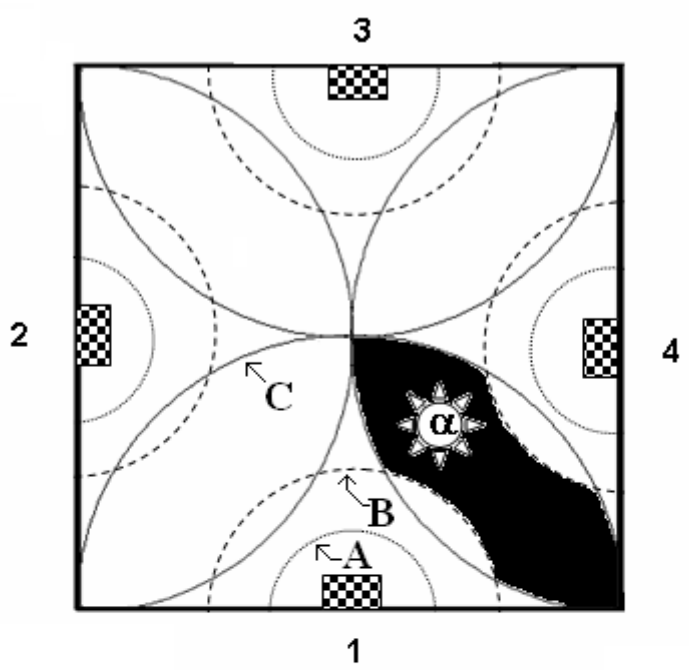


Figure 2: RTLS Architecture with Receiver Sensitivity Location Determination Method

The overall system architecture of an RTLS implementing the receiver sensitivity location determination method is illustrated in Figure 2. Unlike an RTLS implementing the ToA and RSSI methods of location determination, this type of RTLS uses receiver units as interfaces between the transmitter and wireless access point, providing three major advantages. Firstly, computing the location estimate of a transmitter is done solely on the receiver unit, using the Wi-Fi network only when reporting the location estimates back to the host computer, reducing the burden on Wi-Fi network resources. Secondly, the interfaces between the wireless access point and transmitters allow far greater freedom in system development, providing freedom of frequency band of operation, modulation technique, and location determination algorithm. And finally, an RTLS implemented this way has the unique advantage of allowing the host computer to map the location estimates made by each receiver unit into a truth table, where each Boolean sequence corresponds to a final location estimate of a tag at the host computer using the location

estimates reported by each receiver unit. Illustrated in Figure 3, is a tag (denoted by α), that is bounded by threshold boundaries created by each receiver unit. In this figure, the tag has been estimated in the 'C' boundary of receiver units '1' and '4', creating the Boolean sequence '1001'. At the host computer, this sequence will appear in a four-term (one for each receiver unit) truth table, which relates the sequence to a location to plot the tag in the Graphical User Interface (GUI) of the host computer.



Tag Location Estimate Truth Table					
		Receiver Unit #			
		1	2	3	4
Threshold Boundaries	A	0	0	0	0
	B	0	0	0	0
	C	1	0	0	1

Figure 3: Threshold Boundaries Mapped in Truth Table for Tag Location

2.0 PROBLEM STATEMENT

The Real-Time Locating System (RTLS) to be designed and developed has the task of providing a centralized location with location information of all of the assets that it tracks. The RTLS must be reliable in that tracking tags must be timely (seconds) and accurate, but these two requirements manifest their own set of hurdles which must be considered for the real-world implementation of the RTLS. The following subsections address these problems (as goals and requirements of the system) that inevitably influence the design and implementation of the RTLS.

2.1 GOALS AND REQUIREMENTS

RTLS have two primary goals: first to determine the location of tags in real-time and secondly, to be scalable to track a large number of tags. Location determination can be accomplished in any number of ways, employing the popular location determination methods mentioned in Section 1.2.1 or any other working method. The scalability of the system should be sufficient enough to track thousands of tagged assets, which can place a significant burden on system bandwidth and performance if the system is used for other applications or not properly designed for large traffic volume.

The RTLS presented in this thesis was designed with a set of requirements in mind. The following subsections detail the requirements by which the RTLS in this thesis was designed to conform to.

2.1.1 Location Accuracy to Room Level

The first requirement of the RTLS presented in this thesis requires the RTLS to be able to determine what room or area a tag resides in. Location determination accuracy has been previously reported to be on the order of several meters [16][17][18][19] , so an accuracy of one to two meters would be a goal for improvement – with most rooms in buildings being greater than several meters in length and width, this degree of accuracy would provide even small rooms with a fair number of location estimate points.

2.1.2 Scalable to Track Thousands of Tags

The scalability of the RTLS has three facets: the infrastructure, frequency usage, and economic standpoints. The infrastructure scalability of the RTLS refers to the system making use of existing communication and electrical infrastructures. This also ties closely into the frequency usage of the RTLS: the system must share the frequency bands with other systems in the infrastructure, but the RTLS must not reduce the data throughput of other systems sharing the frequency bands and when scaling up the RTLS, it must maintain a real-time quality of location determination. Economically, the price of the devices that perform location estimation (readers) must be cost effective – a proposed cost of each unit is to be under $100 USD.

2.1.3 Throughput to Provide Locations of Tags Quickly

Throughput of the system is critical. Locating all assets or people quickly in a crisis situation is absolutely paramount. The throughput of the system represents the maximum time to provide location information for all tags. Frequent and timely location information of all tracked units in a crisis situation allows for rescue teams to have real-time data of anything being tracked. The throughput of the RTLS must be maintained even if the system bandwidth is being shared by other applications, e.g., Wi-Fi, and the RTLS must not monopolize the bandwidth such that it reduces throughput of these other applications.

2.1.4 An Efficient Location Determination Algorithm

An efficient location determination algorithm is directly related to the throughput requirement of the RTLS. The simpler the location determination algorithm is, the less processing that is required, and subsequently the greater the throughput of the RTLS. The algorithm should be distributable in terms of load to the units that perform the location determination – this allows for the burden of computation to be performed in the local area units, rather than burdening any existing communication infrastructure with the task of performing location determination of tags. A location determination algorithm implemented in this way reduces the amount of communication necessary in addition to the existing communication infrastructure and the amount of computation necessary at a centralized location.

2.1.5 A Fault Tolerant System

Because the RTLS detailed in this thesis is intended to be implemented in hazardous conditions, which can be any type of crisis situation including fires, which are likely to damage components or entire reader units, it is important that removing readers in the system does not cause the entire system to fail. This is the essence of the fault tolerance of the RTLS detailed in this thesis: destruction of units will only cause a localized degradation in determined location information and not affect the entire system in any way.

2.2 STATEMENT OF THE PROBLEM

Development of an RTLS to fulfill the goals and requirements detailed in the above sections requires a number of problems to be solved. The following is a summary listing of the problems addressed in this thesis. Each point in the listing defines a major component of the RTLS design to be developed to meet the goals and requirements of set forth.

- Transmitter Unit Design, Development and Testing
- Receiver Unit Design, Development and Testing
    - Locate and Integrate a Digital Step Attenuator (DSA) into the Receiver
    - Establish an Integrated WiPort (Wi-Fi Network Communication) Interface in the RTLS Receiver Unit
- Software Design
    - Establish and Integrate a Receiver Unit Location Determination Algorithm
    - Develop the Host Computer Interface (GUI)
- Wireless Communication
    - Provide Efficient Communication Between the Receiver Unit and Transmitter Unit Only
    - Develop the Wi-Fi Link Between Receiver Unit and Host Computer Only
- Overall RTLS Deployment and Usage
    - Choose and Demonstrate the System in a Candidate Room Layout
    - Demonstrate the Locations Mapped to Host Computer Interface

3.0 THEORY AND OPERATION

RTLS design selections and the associated limitations, problems, and expected behavior of selections can be understood by examining the basic theory governing the dynamics behind RTLS designs. The following subsections will examine the propagation effects of electromagnetic waves and what problems they can create, antenna types for radiating and collecting electromagnetic waves, and popular location determination methods employed in RTLS designs. The theoretical topics covered in this section cover the main points needed to understand the design decisions and evolution of the RTLS designs in this thesis.

3.1 LOCATION DETERMINATION METHODS

For RTLS, several well-known techniques exist for location determination. These include: RSSI of Arrival (RoA), Angle of Arrival (AoA), Time of Arrival (ToA), and Time Difference of Arrival (TDOA) [8]. AoA location determination techniques utilize a known distance between readers, which calculate the angle of the received signal from the tag. Meanwhile, TDOA refers to a location determination method that focuses on the concept that signals from a tag will arrive at readers at different times. Each reader, potentially, in an environment will receive the signal from a tag at different times, using these multiple

measurements to triangulate a location [11]. Specifically, ToA and RSSI based location determination methods will be examined, along with the novel location determination method presented for this thesis.

3.1.1 Time-of-Arrival

Time of Arrival (ToA), also known as Time of Flight (ToF), involves measuring the distance from an object to a point using knowledge of the velocity of the signal traveling between the point and the object. The time that it takes for the signal to travel between the object and the point at the known velocity of the signal equates to the distance away that the object is from the point. Calculation of the ToA is accomplished using precision clocks capable of sufficient resolution for the velocity of the signal in question. Indirect signals received at the reader from the tag by way of reflections of the signal off of surfaces in the environment provide challenges for systems employing ToA methods of location determination because these indirect signals will arrive at the reader at some time after a line-of-sight path from the tag to the reader [11].

3.1.2 Received Signal Strength Indicator

Systems using the Received Signal Strength Indicator (RSSI), also known as RSSI of Arrival (RoA), take advantage of the fact that the intensity of a signal from a source will diminish the further away from the source that the signal is received. Knowing the strength of the transmitted signal, a correlating function can estimate the distance between a tag and reader.

For example, in free space, a radio transmission from a source will emit a signal with an intensity that diminishes proportionally by a factor of $1/r^2$ for a point, at a distance r from the transmitting source [11].

3.1.3 Novel Location Determination Method

As described in Section 1.2.2, the receiver sensitivity of a receiver can be adjusted in such a way to where it can be useful in calculating the location of a tag. The virtual boundaries created by the thresholds set-up by the receiver sensitivity adjustment intervals, as discussed in Section 1.2.2, serve as cut-off regions (boundaries) by which the sensitivity of the receiver can be adjusted to find the virtual boundaries at the brink of where the transmissions from the tag can and cannot be received, which happens when the receiver sensitivity is adjusted to be too poor to receive transmissions. Figure 4 illustrates this concept of adjusting the sensitivity levels such that boundaries are introduced which can be used to determine at which boundary, if the receiver sensitivity were reduced more, then data from the tag (denoted as α in this figure) would not be successfully received by the receiver because of the receiver sensitivity being too poor. The overlapping threshold boundaries created by nearby receiver units allows for segmenting these boundaries into smaller, more precise, regions that the tag can be estimated to reside within.

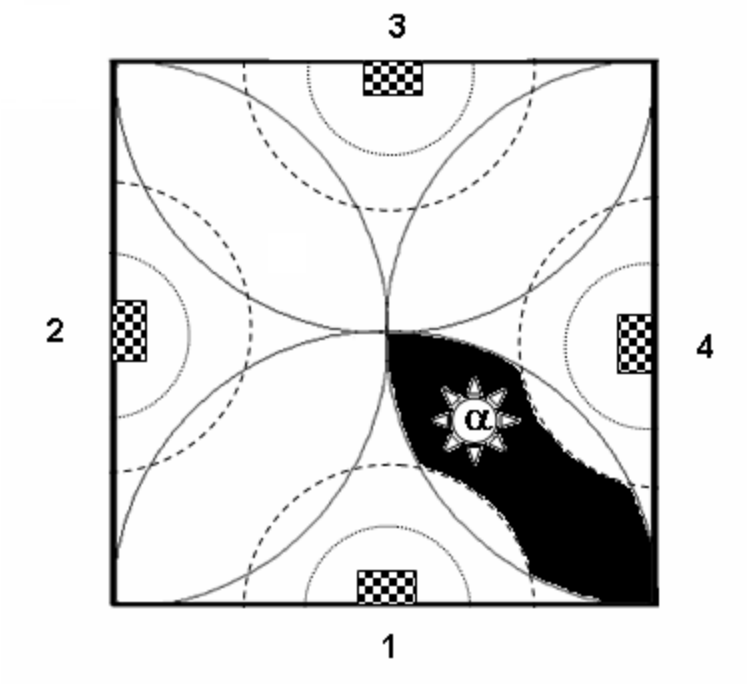


Figure 4: Illustrating Threshold Boundaries Created by Receiver Units (Checkered box)

The receiver sensitivity method of obtaining a location estimation can be paired with a way of determining the quality of the communication link established between a transmitter and receiver. Determining the quality of a communication link requires ascertaining how often data packets, that are sent from transmitter to receiver, are received in error. The greater the number of packets received in error, the more packets that will need to be re-sent, thus, this is a way of determining the quality of the communication link. This method of determining the number of packets received in error verses the number of packets received properly is known as the bit error rate (BER). The bit error rate of a communication link depends on many different factors, which will be discussed further in this section. In the receiver sensitivity method of location determination, ascertaining the BER allows the system to establish how good/poor the quality of communication is for a particular boundary. Because the receiver sensitivity of the receiver can be adjusted to a degree where transmissions from the transmitter can and cannot be received by

the receiver in quick succession, a consistently large increase in BER at a specific boundary over several location estimations indicates a severe degradation in the quality of the communication link, allowing the system to declare a cut-off region where the receiver can and cannot receive transmissions from the transmitter. Declaring the cut-off region allows the system to establish an estimate for how far the transmitter resides from the receiver when the distance that each boundary covers is known. Further details regarding this implementation are discussed in the hardware and software design of the RTLS presented in this thesis.

3.2 FREQUENCY, MODULATION, AND INTERFERENCE

The effects of frequency, modulation, and interference are all intertwined. Understanding the role of frequency and modulation on the degree and types of interference that can arise will aid in the selection of each for the design of the RTLS.

3.2.1 System Dependence on Frequency

The concept of free-space propagation to a communication system generally assumes that the system functions in an ideal environment free from causes of interference such as absorption, reflection, diffraction, and scattering. In practice, communication systems near ground level are subject to these forms of interference [6].

Reflection can be defined as the process that occurs when an electromagnetic wave impinges on a surface whose dimensions are large relative to the wavelength of the electromagnetic wave signal. Likewise, diffraction occurs when a dense object, whose

dimensions are large relative to the wavelength of the electromagnetic signal, appears in the line-of-sight path between transmitter and receiver, effectively obstructing this line-of-sight signal path. The diffraction phenomenon occurs when the large dense object obstructing the line-of-sight signal path causes secondary waves to form behind the object. Finally, scattering occurs when an electromagnetic wave impinges on a surface whose dimensions are small relative to the wavelength of the electromagnetic wave signal causing the impinging signal to spread out/reflect in all directions. Because scattering occurs when the electromagnetic wave impinges on a surface small relative to the wavelength of the impinging electromagnetic wave, this means that any rough surface, whose undulating/jagged surface is composed of many small surfaces, can effectively scatter an electromagnetic wave [7]. By selecting a lower frequency (larger wavelength) of operation for the RTLS, two of the three contributing factors to interference in a wireless channel (due to reflection and diffraction) detailed here can be reduced.

3.2.2 The Multipath Problem

In communications, when objects between and around a transmitter and receiver exist, they can obstruct the line-of-sight path of signal propagation. Even without obstructing the line-of-sight path, the occurrence of such objects in the environment of the transmitter and receiver contribute to the multipath propagation.

Multipath propagation refers to the situation by which the electromagnetic waves transmitted are received by way of paths other than the line-of-sight path. Signals at the receiver that are received by multipath propagation of the transmitted signal arrive by way of reflection and diffraction of the electromagnetic waves of the signal. Reflection, which is the bouncing of electromagnetic waves off of objects, and diffraction, is the bending of electromagnetic waves

around objects, producing a multitude of potential signal paths. Significant signals can often be received by the receiver from more than one of these paths. The multiple waves arriving at the same receiver location introduce the possibility of constructive or destructive interference, where the wave amplitudes add in time, sometimes producing nulls. Multipath propagation is a form of interference that can cause errors. These errors manifest themselves in the form of intersymbol interference, which will be discussed in Section 3.2.4 [37].

3.2.3 Modulation's Effect on System Performance

Modulation can be defined as "the process by which some characteristic of a carrier wave is varied in accordance with an information-bearing signal" [38]. By this, the information signal is actually the modulating signal (i.e. binary information to be transmitted) which varies the carrier wave, and the output of the effect of this process of modulation is the modulated signal. Modulation is performed by a transmitter and can be referred to as the modulator. Accordingly, a receiver is used to demodulate the modulated signal that the receiver receives back into the information-bearing signal [38].

Modulation can be used in several ways to benefit wireless communication systems: first, to shift the spectral content of the information-bearing signal to a part of the frequency spectrum for wireless communications; secondly, to present the information-bearing signal for communication in a form that is less susceptible to noise and interference; and lastly, modulation techniques allow for multiple users of a channel through multiple-access techniques. Of these benefits of modulation, the ability for modulation to allow for the transmission of information in a way that makes it less susceptible to noise and interference will be especially important as seen through the design iterations of the RTLS, in the subsections of Section 4.0 [1].

The subsections of Section 4.0 present RTLS iterations where the first of the iterations used an Amplitude Modulation (AM) Scheme called On-Off Keying (OOK); whereas, the latter iterations use a Frequency Modulation technique called Frequency Shift Keying (FSK). The modulation technique used in the first iteration suffered from interference problems that the latter iterations addressed. The change of modulation schemes between iterations comes from the fact that frequency modulation allows for an improved signal-to-noise ratio (SNR) at the output of the receiver for exchange of an increase in the bandwidth over which the information is transmitted[39]. It can be said that unlike AM transmission bandwidth, for an increase in the FM transmission bandwidth, a quadratic increase in the SNR is observed at the output of the receiver[39]. This is a significant point, as this means that the bit error rates (BER) observed using AM and FM techniques will be different, thus directly affecting the number of redundant data packet transmissions to ascertain a BER for a threshold in the receiver sensitivity method of location determination, which relates to the determined location of a tag.

3.2.4 Intersymbol Interference (ISI) and Symbol Rate

Noise in communication systems can come from a variety of sources. These sources can include both man-made and natural sources. Interfering noise signals are generally uncontrollable and unwanted electrical signals that interfere with a signal of interest. Interference levels caused by noise are what sets the minimum power level acceptable to receive a signal, and directly influences the reliability of the communication link and whether symbols can be properly demodulated [5].

Intersymbol Interference (ISI) occurs when any part of a pulse, or symbol, "smears" into adjacent pulse intervals; the smearing is frequently seen as the tails of these pulses encroaching

on the interval of another pulse [3]. A wireless channel has memory due to the multiple signal paths that exist from transmitter to receiver (multipath interference, Section 3.2.2), which can manifest errors in the form of ISI [4]. Most modulation schemes are affected by the ISI problem, and it is a major obstacle in achieving high-speed symbol rates in limited bandwidth systems [3].

Often, radio electronics will modulate and/or filter communication signals in order to satisfy some sort of bandwidth requirement. Filtering can be characterized by various reactive circuit elements such as inductors and capacitors. This filtering occurs throughout both the baseband and wireless aspects of communication systems such as in the transmitters and receivers and even the wireless channel. Baseband filtering occurs, such as in a cable, from distributed capacitances that distort pulses, while pulse distortions in wireless systems can be characterized by fading channels. Intersymbol interference issues interfere with the detection of pulses/symbols and can degrade error performance even with the absence of noise in a communication system. The effects of filtering and fading still can lead to ISI [2].

Nyquist determined that the theoretical minimum bandwidth of a channel for detecting N symbols without ISI, must be N/2 Hz. This is only realizable when we consider the frequency response of the system to be an ideal Nysquist filter (a rectangular filter), which are not practically realizable. This being said, a variety of other techniques for reducing ISI are used, which will not be covered in this thesis, as the RTLS designed in this thesis uses inexpensive COTS transmitters and receivers which do not explicitly mention the use of specialized techniques[2].

From Nyquist's theoretical minimum bandwidth for detecting a number of symbols in a channel, it can be intuitively determined that to achieve the highest possible symbol rate, the bandwidth of the system should be maximized. When designing a system whose transfer

function is not known, maximizing the bandwidth of the system followed by experimenting with various symbol rates allows for selecting a reasonably fast symbol rate for the given bandwidth.

3.3 ANTENNAS AND RADIATION PATTERNS

Antennas are a crucial component to any radio system. Antennas convert conducted electromagnetic waves to freely propagating electromagnetic waves and vice versa. That is, antennas are intended to efficiently radiate and collect electromagnetic waves[41]. When selecting an antenna for an application, it is important to consider the aspects of: radiation pattern, power gain, directivity, and polarization. Each of these characteristics of an antenna is useful to understand when selecting an antenna for an application. For an RTLS, the selected antenna will affect many aspects of the overall system. For example, a highly directive antenna on a transmitter will exhibit more gain in one direction as opposed to others meaning that a reader in direct line of the most directive portion of the antenna will receive a very strong signal. Meanwhile, another reader at an equal distance away from the transmitter as the other reader, but in direct line of a lesser directive portion of the antenna, will receive a signal at a signal at a different and lesser strength.

3.3.1 Radiation Pattern, Gain, Directivity, and Polarization

Radiation patterns are 3-D plots characterizing the spatial radiation exhibited by antennas. The radiation pattern gives a visual depiction of this radiation pattern far from the antenna. Power gain is a ratio characterizing the input power to the antenna relative to the power

output from the antenna [41]. Directivity describes an antenna's ability to concentrate radiated power in a specific direction, and in reality, all antennas exhibit some form of directivity. Polarization refers to the orientation of electromagnetic waves radiated from an antenna [41].

When it comes to the RTLS design, all of these factors are important to consider, and in particular, their relation to each other. As described earlier in Section 3.3, antenna directivity directly influences the gain of a transmitted or received signal depending on the location of either the transmitter or receiver in relation to the directive regions of the antennas being used. As such, when considering the environmental layout of the RTLS, the use of an antenna with an omni-directional radiation pattern, that is, an antenna that radiates equally in all directions, will offer a signal strength that, for the most part, is equal for a radius around an antenna. This is useful considering that moving out of line with a highly directive lobe of an antenna will show a sudden decrease in the strength of the signal received.

3.3.2 Common Antenna Types

The following subsections will examine common antennas types and assess their usefulness for an RTLS. As described in Section 3.3.1, the antenna selected that will be most useful for the RTLS in this thesis will have an omni-directional radiation pattern. This will be important to keep in mind for the following subsections on antenna types and their associated radiation patterns.

3.3.2.1 Isotropic

An isotropic antenna is an antenna whose radiation pattern extends equally in all directions. Isotropic antennas are only theoretical, and have never been built, and as such,

cannot be used in the RTLS, but they are the basis by which antenna standards are measured. Figure 5 illustrates the isotropic radiation pattern from an isotropic antenna – it is a spherical pattern emanating from a radiating element (pictured as a black point)[40].

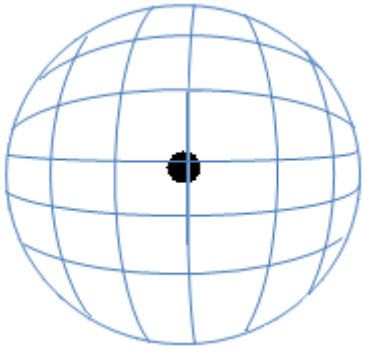


Figure 5: Isotropic Radiation Pattern

3.3.2.2 Dipole

Dipole antennas are considered the most elementary realizable antennas. The most common type of dipole found is the half-wave dipole[42]. A dipole antenna is not a directive antenna in two dimensions; the radiation pattern of the dipole antenna exists 360-degrees around the antenna perpendicular to the long axis of the radiating elements of the antenna [41]. This radiation pattern is illustrated in Figure 6. The two black rods represent the half-wave dipole antenna elements and the cylindrical tube encircling the antenna's elements represents the radiation pattern. The dipole antenna exhibits a radiation pattern that appears omni-directional in one plane. This means that the dipole antenna is a good candidate for the RTLS, but what can be seen in the following section about monopole antennas, is that the two dimensional radiation pattern of monopole antennas is the same as a dipole (except for the ground plane in a monopole antenna arrangement which does not permit the radiation pattern to extend in the direction of the

ground plane), while the monopole is smaller in size, making it best for size-concerned applications like an RTLS.

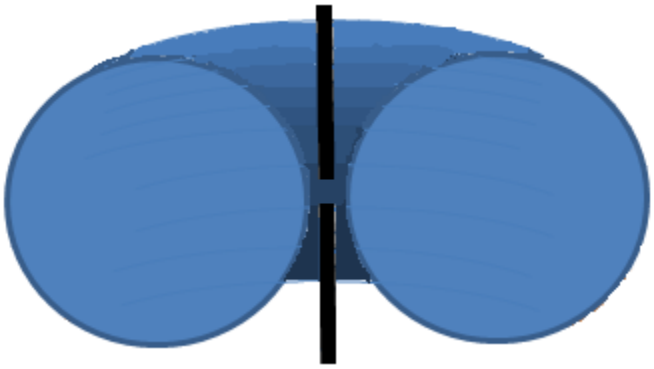


Figure 6: Dipole Radiation Pattern

3.3.2.3 Monopole

A monopole antenna is formed by replacing one of the halves of a dipole antenna with a ground plane perpendicular to the length axis of the other half of the antenna. This produces an effective quarter-wave radiating antenna over a conductive ground plane. When implemented this way, the radiation pattern of the quarter-wave monopole antenna has a radiation pattern exactly like a half-wave dipole antenna [42]. Figure 7 illustrates the quarter-wave monopole antenna with conductive ground plane underneath, perpendicular to the antenna; the black rod represents the quarter-wave monopole antenna and the cylindrical tube encircling the antenna represents the radiation pattern. There is, of course, no radiation into the ground plane space. The monopole antenna exhibits an omni-directional radiation pattern in one plane, making it useful in an RTLS. The advantage that a monopole has over a dipole is that it has the same 360-degree radiation pattern as a dipole (but without radiation into the ground plane space), but in a

smaller size. This advantage makes the monopole an ideal candidate for an RTLS implementation.

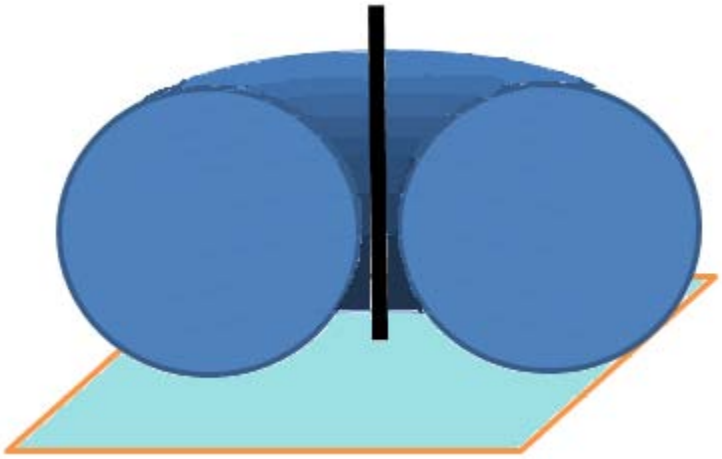


Figure 7: Monopole Radiation Pattern

3.3.2.4 Yagi

Yagi antennas are a common type of directional antenna. Illustrated in Figure 8 is the Yagi antenna with the antenna elements as black rods and with its associated radiation pattern pictured as various sized ovals (lobes) – the largest lobe of the radiation pattern illustrates how most of the gain of the antenna is in only one direction, with smaller lobes at the rear of the antenna. While only one element of the antenna rods pictured in the Yagi antenna is driven to transmit signals, the number of non-driven elements determines the gain and directivity of the Yagi antenna [41]. The Yagi antenna, because of its size and inherent directivity make it a poor choice for an RTLS, as the RTLS will perform best with an omni-directional antenna.

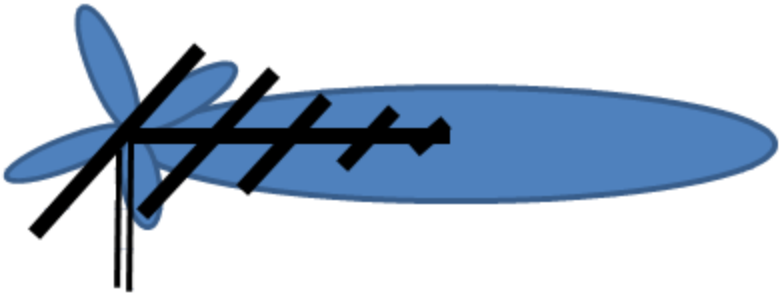


Figure 8: Yagi Radiation Pattern

4.0 SOLUTION EVOLUTION AND ITERATIONS

The RTLS presented in this thesis has gone through several design and specification iterations. Each subsequent iteration was developed to work around problems from which the iteration before it suffered. Each iteration experimented with different frequency bands and/or modulation techniques while still adhering to the goals of the design. While both the modulation scheme and frequency band are open for selection, the usable frequency bands were restricted to the Industrial, Scientific, and Medical (ISM) radio bands, which include a wide range of frequency bands. Namely, the tests performed used bands with center frequency of 433.92 MHz and 915 MHz. Additionally, the testing environment of the RTLS iterations contained many objects within close proximity of, and between, both the tag and the reader, making the RTLS environment highly prone to multipath interference.

The first iteration, named the Alpha-Test, was developed using an On-Off-Keying Modulation scheme with a 433.92 MHz center frequency. The next two iterations were part of the Beta-Test. The first of the Beta-Test iterations, Beta-Test I, used a Frequency Shift Keying (FSK) modulation scheme, with a 915 MHz center frequency. Meanwhile, the second of the Beta-Test iterations, Beta-Test II, also used an FSK modulation scheme, but at a center frequency of 433.92 MHz. Additionally, the Alpha-Test and the Beta-Test I used a Universal Serial Bus (USB) cable (and related controller hardware and software) to interface a host computer to each reader in order to simplify the design to create an RTLS capable of

demonstrating the novel location determination method (receiver sensitivity) – the intent was to demonstrate this first and to worry about removing the USB tether later. This USB cable link was removed for the Beta-Test II, as the RTLS presented in this thesis has a requirement to use a Wi-Fi interface to relay reach reader's location estimate of the tag to the host computer.

Because the design goals of each iteration remained the same, the following descriptions will detail how each iteration differs from the others as well as how each subsequent iteration improved upon the previous one. Because transmitters are not the primary design focus, and novel location determination is the primary goal of this thesis, which is performed by readers, the following sections will provide figures picturing the designed readers for the respective RTLS iteration. Additionally, the results of the Beta-Test II are detailed in Section 9.0 .

4.1 ALPHA-TEST

The Alpha-Test was the first iteration of the RTLS designed for this project. This RTLS ultimately suffered from long periods of time to determine a location of a tag falling short of the goal of scaling the system up to determining the location of many tags. Additionally, this iteration was unable to provide accurate locations of a tag, and the error in the location was far too large to be competitive with other RTLS designs [16][17][18][19]. Figure 9 illustrates a reader designed for the Alpha-Test iteration. Encircled in white, in this figure, is the USB interface described in the previous section. Additionally, it should be pointed out that the reader unit is inside of an aluminum enclosure, which serves as the shielding discussed in Section 6.1.2.6.1.

Figure 9: Alpha-Test RTLS Reader; USB Interface Circled in White

4.1.1 System Details

The Alpha-Test iteration used an On-Off Keying (OOK) modulation scheme with a 433.92 MHz center frequency. The OOK Modulation scheme is the simplest form of Amplitude Modulation (AM), simply turning on or off the carrier frequency to transmit a binary 1 or 0 symbol. This modulation scheme uses a narrow bandwidth, with a single carrier frequency at 433.92 MHz.

This system utilized a location determination algorithm as detailed in Section 3.1.3, where the Bit Error Rate (BER) is computed through redundant transmission of data packets to the reader from the tag, which gives a BER for a specified threshold.

4.1.2 Results

The Alpha-Test suffered from significantly long periods of time to determine the location of a tag. This prevented the system from being capable of being scaled up to track many tags. Additionally, the accuracy of the system was not sufficiently better than competing designs [16][17][18][19]. Reasons for these inaccuracies can be related to the OOK modulation scheme used in the Alpha-Test. In a highly multipath environment, the constructive and destructive inference produced can cause the incorrect detection of binary symbols, which is referred to as frequency selective fading. One method to reduce the effects of frequency selective fading is by applying some form of diversity; in the case of modulation schemes, frequency diversity can be employed. Frequency Diversity makes use of transmitting the message over more than one frequency, effectively increasing the bandwidth over which the message is transmitted, which will become a factor in the design of the Beta-Test iterations.

4.2 BETA-TEST I & II

The Beta tests (Beta-Test I & II) are subsequent experimental versions of the RTLS with the latter version (Beta-Test II) improving upon the flaws of the former (Beta-Test I). The Beta-Test II was started as a result of empirical evidence from tests with the Beta-Test I that resulted in significant problems for location determination.

4.2.1 Beta-Test I (915 MHz Band RTLS)

The Beta-Test I was an experimental RTLS designed for the 915 MHz band. Despite the previous iteration, the Alpha-Test, being designed for the 433 MHz band, and understanding that, in the same environment, a higher frequency, with a smaller wavelength (discussed in Section 3.2.1), will reflect off more objects as opposed to using a lower frequency with a larger wavelength (and subsequently more nulls from the constructive and destructive interference occurring more often with smaller wavelengths), the Beta-Test I was designed for the 915 MHz band. It was not known if this move to a higher operational frequency would affect RTLS performance, but reasons for this changed are discussed further in the Beta-Test I's System Details Section. Additionally, this iteration of the RTLS used a different modulation scheme, Frequency-Shift Keying (FSK) because of the inherent problems found with Amplitude Modulation (AM) techniques as used in the Alpha-Test. The picture in Figure 10 is the Beta-Test I reader with the USB interface circled in white. Note the use of PCB board-level shielding of only specific components (the RF components and transmission lines), instead of the entire circuit board.

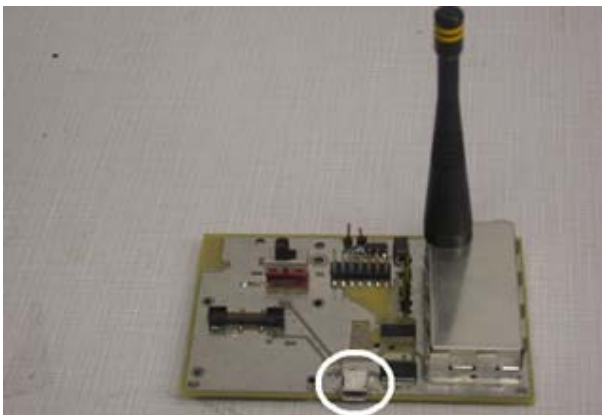


Figure 10: Beta-Test I Reader; USB Interface Circled in White

4.2.1.1 System Details

The Beta-Test I primary goal was to experiment with the benefits of using an FSK modulation scheme over the Amplitude Modulation (AM) scheme, On-Off Keying (OOK), used in the Alpha-Test RTLS. As discussed in Section 3.2.3, increasing the bandwidth over which the information signal is transmitted is favorable in terms of providing an increase in the SNR which can be easily achieved by selecting a modulation scheme such as FSK. This iteration of the RTLS exploits this benefit and uses an FSK modulation scheme over the previous iteration's OOK modulation scheme.

The Beta-Test I operated in the 915 MHz band. The reason for switching from the 433 MHz band in the Alpha-Test, to the 915 MHz band in the next iteration, the Best-Test I, was because a COTS radio-frequency integrated circuit (RFIC) could not be obtained from the manufacturer of the RFIC used in the Alpha-Test that operated in the 433 MHz band but instead with an FSK modulation scheme. Using the same manufacturer reduced the development time as a simple change in the operational frequency band and modulation scheme for RFIC's from the manufacturer used in the Alpha-Test required small changes in package dimensions, keeping interfacing to the RFIC essentially the same.

4.2.1.2 Results

The Beta-Test I suffered excessively from multipath issues. Utilizing the same location determination algorithm as used in the Alpha-Test (location determination algorithm from Section 3.1.3), the Beta-Test I suffered from significant ISI problems manifested by multipath interference. This was not surprising, as discussed in Sections 3.2.1, 3.2.3, and 3.2.4. The smaller the wavelength, the larger an object becomes relative to the wavelength of the electromagnetic wave resulting in a greater chance for multipath interference. These results, as

indicated, are not surprising, but experimentally indicate that there is a need to avoid designing the RTLS in the higher frequency bands.

4.2.2 Beta-Test II (433.92 MHz Band RTLS)

The Beta-Test II was the final iteration of the RTLS project. This iteration improved on the problems seen with the first two iterations addressing the issues of frequency band of operation and modulation scheme to maximize system performance. The Beta-Test II RTLS makes use of a Wi-Fi communication link instead of the USB cabled link, as seen in the first two iterations, for communicating location information about a tag to the host computer. The remaining sections in this thesis explore the detailed design of all aspects of the Beta-Test II RTLS. Figure 11 illustrates the Beta-Test II reader.

Figure 11: Beta-Test II Reader

5.0 SYSTEM SPECIFICATIONS

The system consists of a number of receiver units (readers) which determine the location of a number of transmitter units (tags). Transmitter units continuously transmit. Each receiver unit will adjust its own receiver sensitivity, allowing the receiver unit to determine the location of a transmitter by creating gain thresholds intervals, which correspond to the location of the transmitter with respect to the receiver. The receiver units continuously collect location information about a transmitter and then relay this information to a central host computer, which aggregates these relative locations determined by each receiver unit to determine a best possible location estimate of a transmitter unit.

Figure 12 illustrates a mock-up of the receiver units in a perfectly square room, with the receiver units located in the middle of each wall. This figure also illustrates the threshold boundaries, as concentric half-circles, that each receiver unit conceptually creates as a result of the receiver sensitivity location determination process. Likewise, Figure 13 illustrates this same set-up with a transmitter in the layout; the concentric thresholds create bounds where a transmitter (denoted as α in Figure 13) can be estimated to reside within (denoted by the dark shaded region).

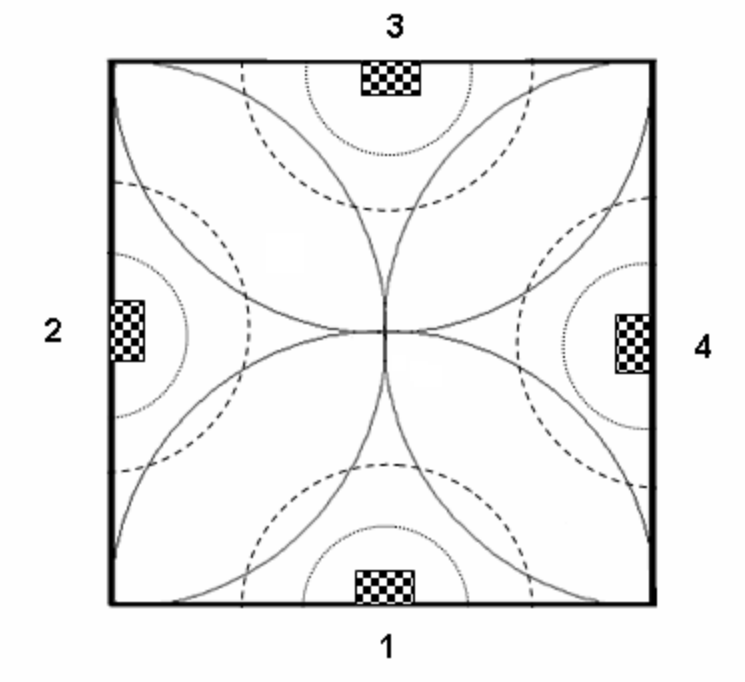


Figure 12: Receiver Units in a Square Room Illustrating Threshold Boundaries

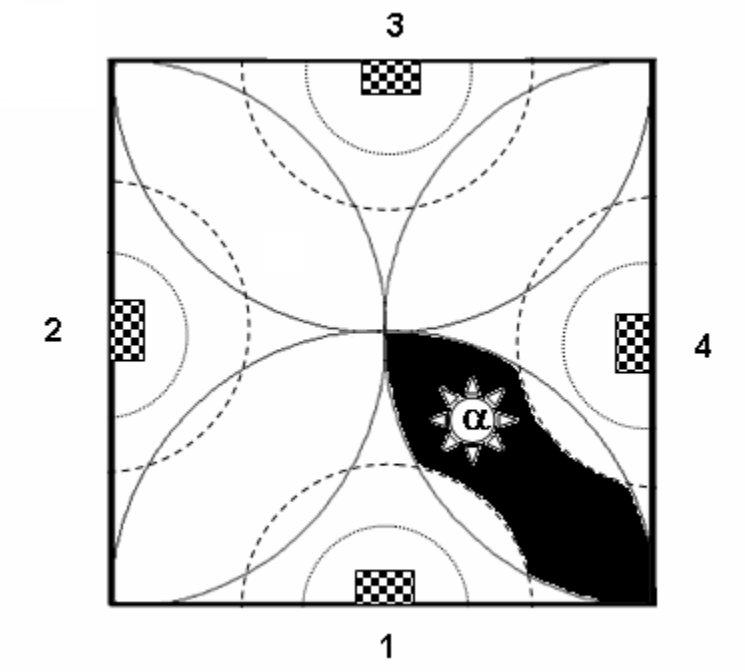


Figure 13: Transmitter Bounded by the Threshold Boundaries Created by Each Receiver Unit

5.1 TRANSMITTER UNIT (TAG) SPECIFICATIONS

The following subsections present the specifications of the transmitter (tag) in the RTLS. The subsections will explore the architecture of the hardware and software of the transmitter at a high level. The transmitter in the RTLS is a simple beacon – always transmitting a known sequence, which in this case, is a simple 50% duty cycle square wave signal. This square wave signal was chosen to simplify the demodulation process and processing done within the location determination algorithm used on the RTLS receiver unit as discussed in Section 3.1.3.

5.1.1 Transmitter Unit Hardware Architecture

This subsection details the hardware architecture of the transmitter unit used in the RTLS. The hardware architecture presented is a high-level view of the transmitter unit detailing the major hardware components and their interaction with each other as can be seen in Figure 14. Following this figure are brief explanations of the role that each hardware component plays in the transmitter design.

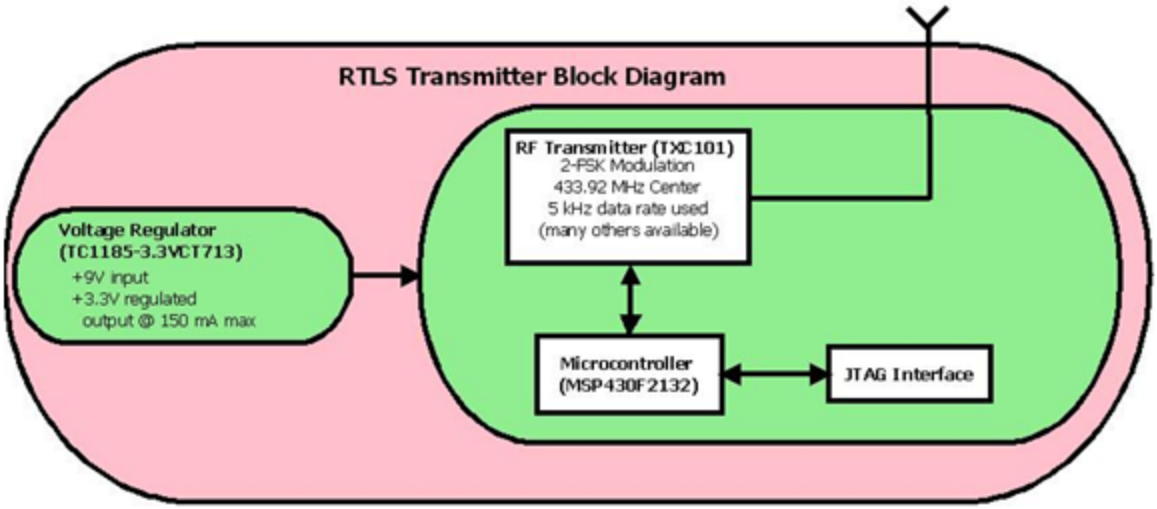


Figure 14: Hardware Architecture of Transmitter Unit

Microcontroller The Microcontroller serves the purpose of controlling all other integrated circuits in the transmitter unit design as well as timely dealing with information/data that any integrated circuit may send to the microcontroller for further processing.

Radio Frequency (RF) Transmitter The Radio Frequency (RF) Transmitter wirelessly transmits data that it receives from the microcontroller. The transmitter operates in a narrow frequency band using a Frequency Shift Keying (FSK) modulation scheme. The transmitter also drives a quarter-wave monopole antenna to accomplish wireless data transmission.

Voltage Regulator The voltage regulator has the purpose of providing a constant voltage supply to all components and integrated circuits in the transmitter unit. The regulated voltage supply takes a voltage input greater than the regulated voltage to be output. When a battery is used to power a circuit, the output voltage of the battery (for some battery types) slowly decreases as the battery

is drained. Using a voltage regulator alleviates this problem by keeping the supply voltage to the entire circuit at a constant voltage regardless of how low the voltage supplied by the battery drops (as long as it is greater than the output voltage from the regulator).

JTAG Interface The JTAG interface allows for loading and debugging code on the microcontroller. This is useful for stepping through code to see how memory and registers change as a result of external interrupts to the microcontroller and the general execution of code.

Antenna The antenna used on the transmitter unit is driven by the RF transmitter. This allows for the transmitter to transmit data wirelessly, which will be received and processed by the receiver unit. The particular antenna used on the transmitter unit is a quarter-wave 433 MHz monopole antenna designed for narrowband transmissions.

5.1.2 Transmitter Unit Software Architecture

The transmitter software architecture subsection details a high-level view of the flow of the software onboard the microcontroller used on the transmitter unit, which is illustrated in Figure 15. The software controlling the transmitter unit simply needs to configure the RF transmitter for data transmission and then send along data to the RF transmitter for wireless transmission of the data. Because the data to be sent to the RF transmitter by the microcontroller needs only to be a 50% duty cycle square wave, this means that the microcontroller simply toggles a data control line at a constant interval.

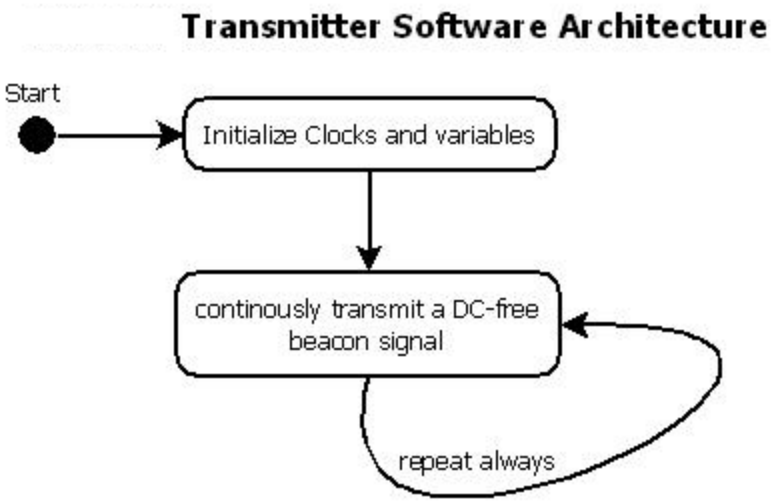


Figure 15: Transmitter Unit Software Architecture

5.2 RECEIVER UNIT (READER) SPECIFICATIONS

Hardware and software architecture specifications of the receiver units (readers) are presented in the following subsections. The receiver units are placed in a room and continuously determine the locations of tags. The relative positions of receiver units to one another are known by the host computer which use the locations determined by each receiver unit to estimate a location of a transmitter unit.

5.2.1 Receiver Unit Hardware Architecture

Figure 16 illustrates a high-level functional block diagram of the receiver unit. This figure shows the directional interaction between functional blocks at a high level, which correspond to the major functional units of the overall receiver unit system. Following are brief

descriptions of each functional block, some of which are also detailed in the Transmitter Hardware Architecture Section (5.1.1) but are reproduced here for convenience.

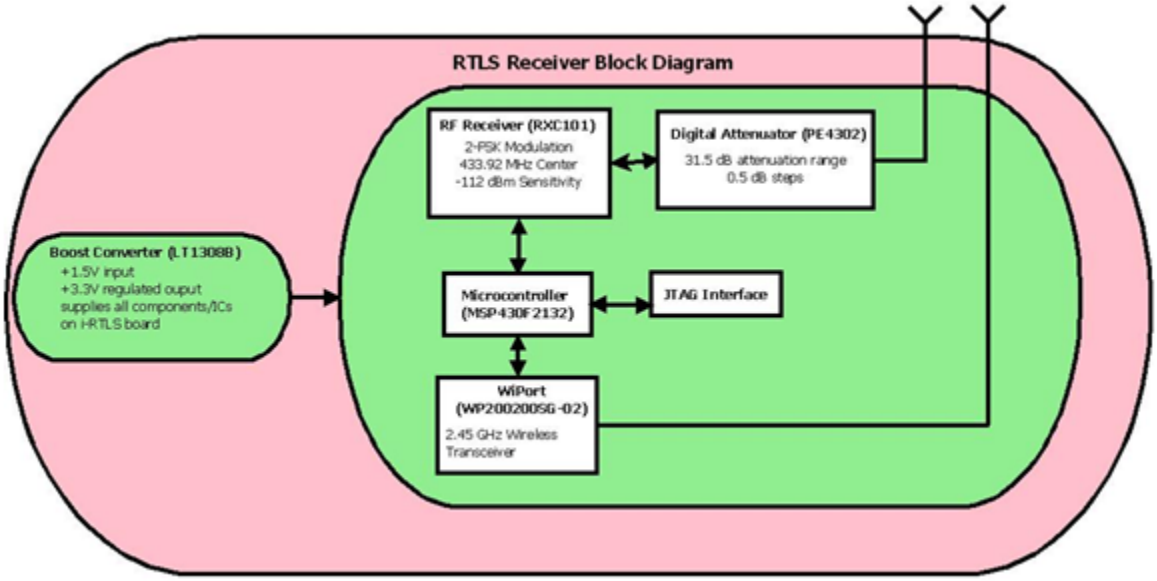


Figure 16: Receiver Unit Hardware Architecture

Microcontroller The Microcontroller serves the purpose of controlling all other integrated circuits in the transmitter unit design as well as timely dealing with information/data that any integrated circuit may send to the microcontroller for further processing.

Radio Frequency (RF) Receiver The Radio Frequency (RF) receiver receives the attenuated signal from the output of the Digital Step Attenuator (DSA). The receiver on the receiver unit demodulates the incoming electromagnetic signals that were wirelessly transmitted by the transmitter unit, and then sends the demodulated data to the microcontroller for processing (implementing the novel algorithm for location determination for the RTLS detailed in this thesis).

Digital Step Attenuator (DSA) The Digital Step Attenuator (DSA) is controlled by the microcontroller. The microcontroller selectively controls the DSA to add or remove attenuation to/from incoming signal path, and outputting the attenuated signal. The DSA is used to create threshold boundaries, which are vital to implementing the novel algorithm of the RTLS presented in this thesis.

WiPort The WiPort takes serial data input and transmits it wirelessly over an 802.11 b/g network. The WiPort is the means by which a central host computer can gather and aggregate the location estimates of each transmitter unit calculated relatively by each receiver unit. Each receiver unit sends its location estimate of a tag via the WiPort over the Wi-Fi network which the central host computer compiles with the other receiver unit location estimates to form a best estimate of the location of a tag.

Boost Converter The boost converter works like the voltage regulator used in the transmitter unit's design except that the boost converter outputs a regulated voltage at a higher voltage than the voltage input to the boost converter. Boost converters can be used to deeply drain a battery as when the voltage of the battery drops from being drained over time. The boost converter can continue to boost the dropping voltage to the regulated voltage (this is possible only until a certain point).

JTAG Interface The JTAG interface allows for loading and debugging code on the microcontroller. This is useful for stepping through code to see how memory and registers change as a result of external interrupts to the microcontroller and the general execution of code.

Antennas The antenna used on the transmitter unit is driven by the RF transmitter. This allows for the transmitter to transmit data wirelessly, which will be received and processed by the receiver unit. The particular antenna used on the transmitter unit is a quarter-wave 433 MHz monopole antenna designed for narrowband transmissions.

5.2.2 Receiver Unit Software Architecture

The receiver unit software architecture, as illustrated in Figure 17, illustrates at a high-level, the major aspects of the receiver software. This figure shows how the receiver, from a high level, simply adjusts the receiver sensitivity by adjusting the attenuation amount imparted by the DSA on the received signal and then collecting the demodulated binary data from the transmitter at each of these threshold levels to finally use the collected information to calculate a best estimate of the location of the transmitter unit relative to the RTLS receiver unit.

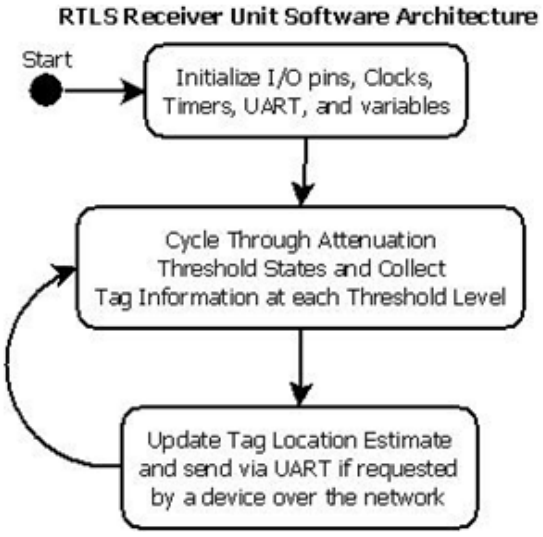


Figure 17: Receiver Unit Software Architecture

5.3 HOST COMPUTER SPECIFICATIONS

The host computer aggregates the relative location estimates for a tag from each reader and compiles them into a best location estimate. The host computer software architecture is presented in the next section. The flow chart in the next section will investigate the path of the software proceeding directly to collecting location information as operating the software in any other way will not put the software into the mode to collect this information. Section 8.7 details how to operate the software to collect tag location information as well as ways that will not lead to this outcome, requiring the program to be exited. The host computer software is interfaced to a graphical user interface (GUI).

5.3.1 Host Computer Software Architecture

Figure 18 illustrates the software architecture of the host computer software in flow chart form to best illustrate the basic progression of the software. A more detailed understanding of the host computer software is detailed in Section 7.3.

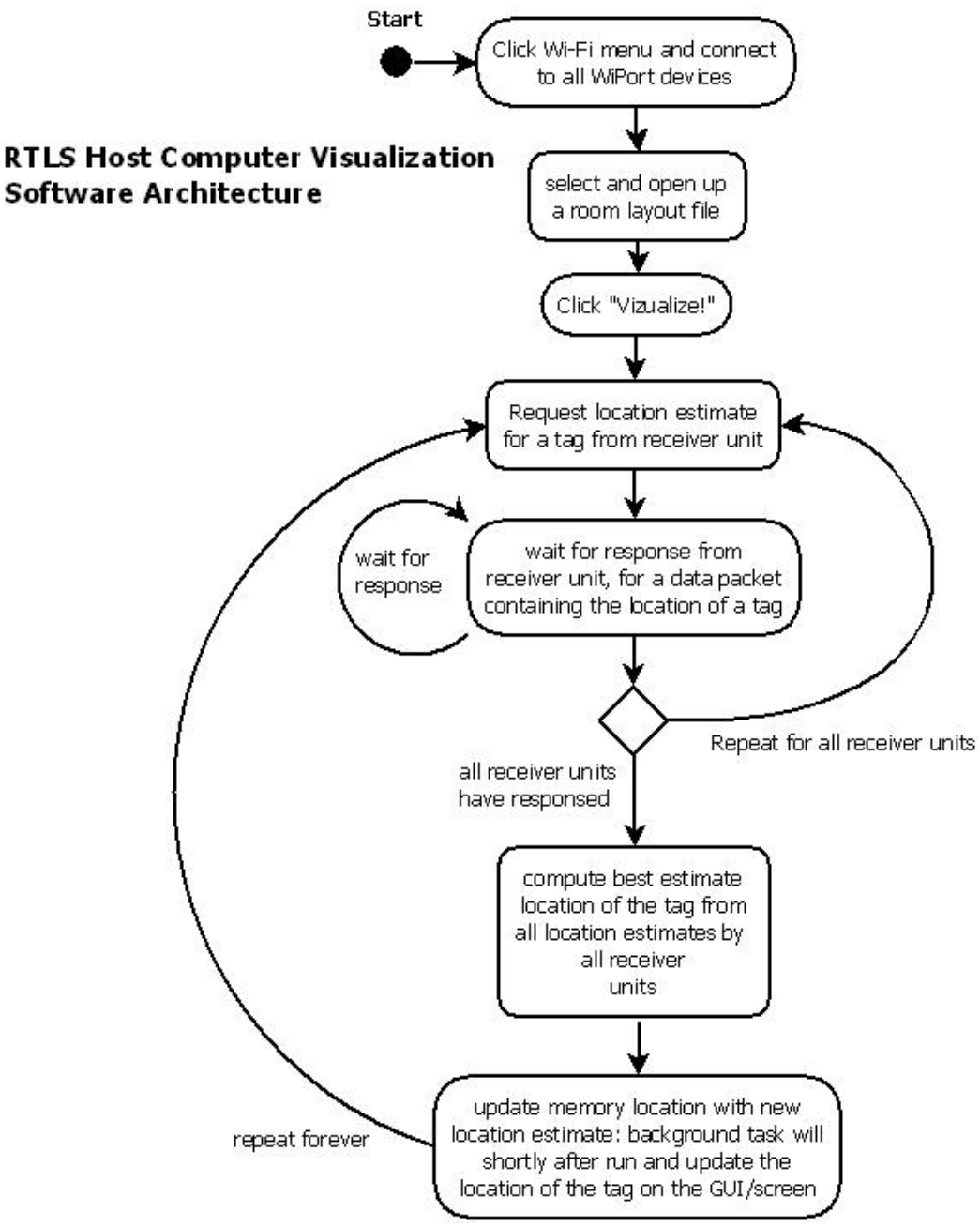


Figure 18: Host Computer Software Architecture

6.0 HARDWARE DESIGN

The hardware design section of this thesis provides an in-depth examination of the hardware components of the RTLS receiver and transmitter units. The following subsections will examine each hardware component of the receiver and transmitter units, which involves the way each component interfaces to other parts and components including pin connections and schematics.

6.1 TRANSMITTER UNIT (TAG) HARDWARE DESIGN

The following subsections detail the hardware design of the transmitter, starting with a description of the overall hardware's operation and followed by specific detailed descriptions of hardware components in the transmitter unit.

6.1.1 Transmitter Unit (Tag) Description of Operation

The RTLS System is intended to be used to track transmitter units in real-time. The methodology behind the system’s operation is that each receiver in the system will reduce its own receiver sensitivity to the point where the sensitivity level will only permit a transmitter to be detected within a narrow distance threshold away from the receiver, and then repeating the

process from a higher sensitivity to a lower sensitivity continuously to ascertain the location of the transmitter as it moves. At a greater sensitivity level, the receiver has the capability of detecting a transmitter further away than at a lower sensitivity level. Once it is determined at what threshold point the receiver unit can and cannot "see" the transmitter, information is then reported to a centralized location for processing over a Wi-Fi network.

6.1.2 Detailed Functional Block Descriptions

The follow subsections of the transmitter hardware design contain detailed descriptions of the functional block diagrams of the system as detailed in Section 5.1.1.

6.1.2.1 Microcontroller

The microcontroller used on each transmitter unit carries the duty of controlling transmission of data to the RF transmitter and configuring of the RF transmitter. The microcontroller used is the MSP430f2132 by Texas Instruments [25]. The microcontroller is a 16-bit Architecture design with 264 KB of Flash Memory and 512 B of RAM. It uses a 16 MHz external crystal as the main clock and is programmed/debugged through a JTAG interface.

A total of ten pins are configured as General Purpose Input/Outputs with all of them interfaced to the RF transmitter for controlling/programming it via its SPI interface and sending along data transmitted wirelessly. Also, six pins are used for programming (loading program code) and debugging (halting code, stepping into code, etc.) via the JTAG interface. Seven pins in total are used from the JTAG interface – one for a common ground and six interfaced to the microcontroller.

Figure 19 shows the schematic of the microcontroller and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 1, is an elaboration of each pin and an explanation of what interfaces to it.

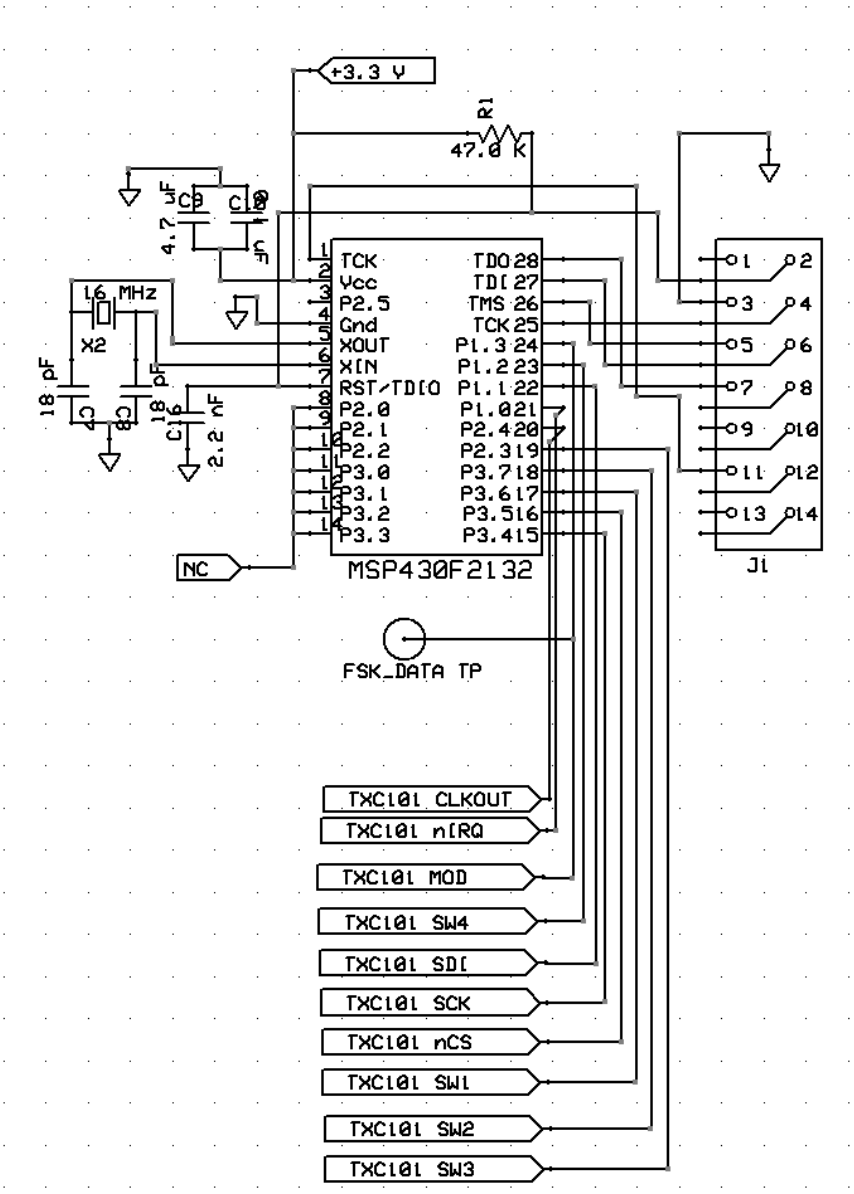


Figure 19: Schematic of MSP430F2132 Microcontroller as it Interfaced to Other Components

Table 1: Elaboration of Each Pin Connection on the MSP430F2132 Microcontroller

Pin #	Name	Description
1	TCK	This pin is connected to pin 11 of the JTAG interface connection.
2	Vcc	This is the power pin of the microcontroller. This pin requires a +3.3V input. Bypass capacitors are added as close as possible to this pin for power supply noise filtering.
3	NC	Not Connected
4	Gnd	This pin is connected to the board's common ground.
5,6	Xout, Xin	These pins are connected to an external crystal which serves as the main clock of the microcontroller. A 16.0 MHz clock is used in this case with two 18 pF loading capacitors connected to the crystal.
7	RST	This pin requires a 47.0K Ohm pull-up resistor (because the pin is active low) to reset the device when re-programming the microcontroller and a 2.2 nF filter capacitor. The value of the resistor is provided in the datasheet for the microcontroller.
8-14	-	Not used/connected
15	SCK	SPI Data Clock.
16	nCS	Connect to TXC101's Chip Select Input. Selects the chip for an SPI data transaction. Active Low for a 16-bit read or write function
17	SW1	Connect to TXC101's SW1. Not used, but connected in schematic.
18	SW2	Connect to TXC101's SW2. Not used, but connected in schematic/
19	SW3	Connect to TXC101's SW3. Not used, but connected in schematic.
20	ClkOut	Connect to TXC101's ClkOut. Not used, but connected in schematic.
21	nIRQ	Connect to TXC101's nIRQ. Not used, but connected in schematic.
22	SDI	SPI Data in.
23	SW4	Connect to TXC101's SW3. Not used, but connected in schematic.
24	MOD	Data to be transmitted is sent on this pin
25	TCK	Used for JTAG Communication. The Test Clock (TCK) pin is used to synchronize the state machine used in programming the microcontroller.
26	TMS	Used for JTAG Communication. The Test Mode State (TMS) determines the next state by sampling on the rising edge of TCK.
27	TDI	Used for JTAG Communication. The Test Data In (TDI) pin is used to shift data into the device's programming logic.
28	TDO	Used for JTAG Communication. Test Data Out (TDO) pin is used to shift data out of the device's programming logic

6.1.2.2 Radio Frequency (RF) Transmitter

Each transmitting unit has been designed with a commercial off-the-shelf (COTS) RF transmitter, TXC101 by RFM [26]. The transmitter is capable of using four frequency bands of which the 433.92 MHz band is used for this design. The transmitters use a 2-FSK modulation scheme with a variable channel bandwidth (the FSK deviations from center frequency) over which it transmits data wirelessly.

The transmitter uses a 10 MHz external crystal and requires several discrete components for matching the RF-positive and RF-negative pin input impedances to 50 Ohms at 433.92 MHz. The transmitter and accompanying software have been configured to operate with the transmitter having a constant +3.3VDC power supply (differing from this will change the operational characteristics). Additionally, the transmitter is programmed using an SPI bus interface to three of its pins from the microcontroller.

Figure 20 shows the schematic of the RF Transmitter and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 2, is an elaboration of each pin and an explanation of what interfaces to it.

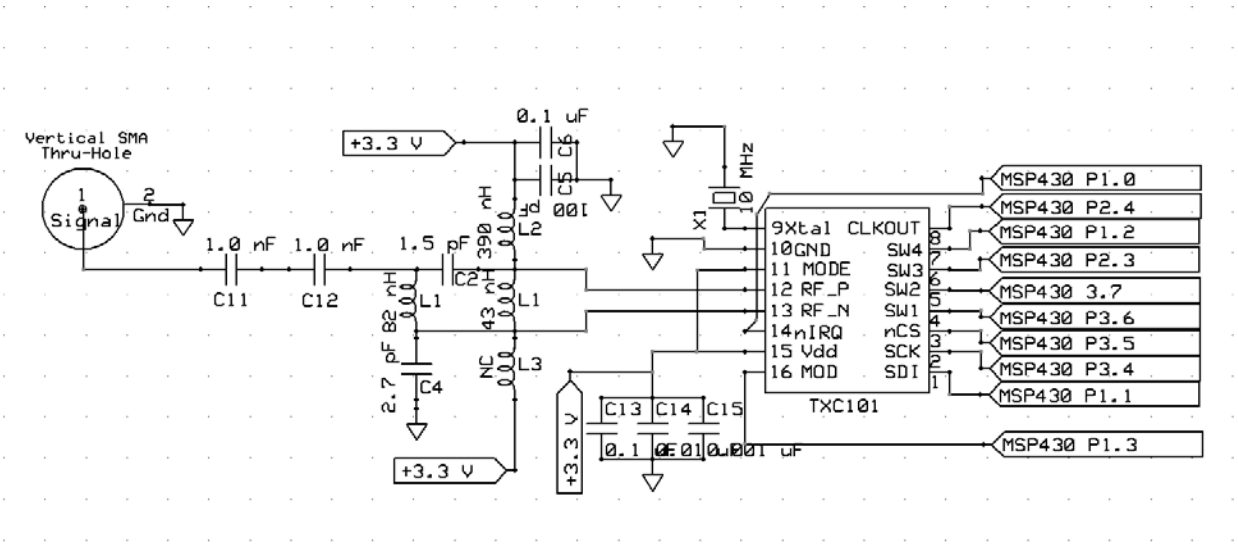


Figure 20: Schematic of RF Transmitter as it Interfaces to Other Components

Table 2: Elaboration of Each Pin Connection on the TXC101 RF Transmitter

Pin #	Name	Description
1	SDI	SPI Data in.
2	SCK	SPI Data Clock
3	nCS	Chip Select Input. Selects the chip for an SPI data transaction. Active Low for a 16-bit read or write function
4	SW1	Switch or Push Button Input 1. Not used, but connected in schematic.
5	SW2	Switch or Push Button Input 2. Not used, but connected in schematic.
6	SW3	Switch or Push Button Input 3. Not used, but connected in schematic.
7	SW4	Switch or Push Button Input 4. Not used, but connected in schematic.
8	ClkOut	Optional clock output for host processor. Not used, but connected in schematic
9	Xtal	Connect 10 MHz crystal. The crystal requires a series capacitance load, which is set programmatically in the Configuration Register of the TXC101
10	GND	Connect to common ground
11	Mode	Connect to Vdd for use with an external processor
12	RF_P	RF Differential I/O.
13	RF_N	RF Differential I/O.
14	nIRQ	Interrupt Request Output and Status Register Data Read Output. Not used, but connected in schematic.
15	Vdd	+3.3V Power. Three decoupling capacitors are used to filter out power supply noise
16	MOD	Data to be transmitted is sent to this pin

6.1.2.3 Voltage Regulator and Power Considerations

The voltage regulator used in the transmitter unit design must be capable of powering all IC's and peripheral circuitry. Every IC in this design can operate at +3.3V. To do this, a step-down linear voltage regulator was used. The voltage regulator used in this design is an LP2992 by Texas Instruments [27]. It is capable of taking as much as a +16 V input and producing a +3.3V output ,and it is able to source up to 250 mA. For the sake of using a standard package battery with a nominal voltage greater than the output voltage of the regulator, a +9V battery was selected, as it is compact, easy to find, and +9V batteries are capable of continuously sourcing the current that the circuit will require for testing purposes.

Figure 21 shows the schematic of the Voltage Regulator and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 3, is an elaboration of each pin and an explanation of what interfaces to it.

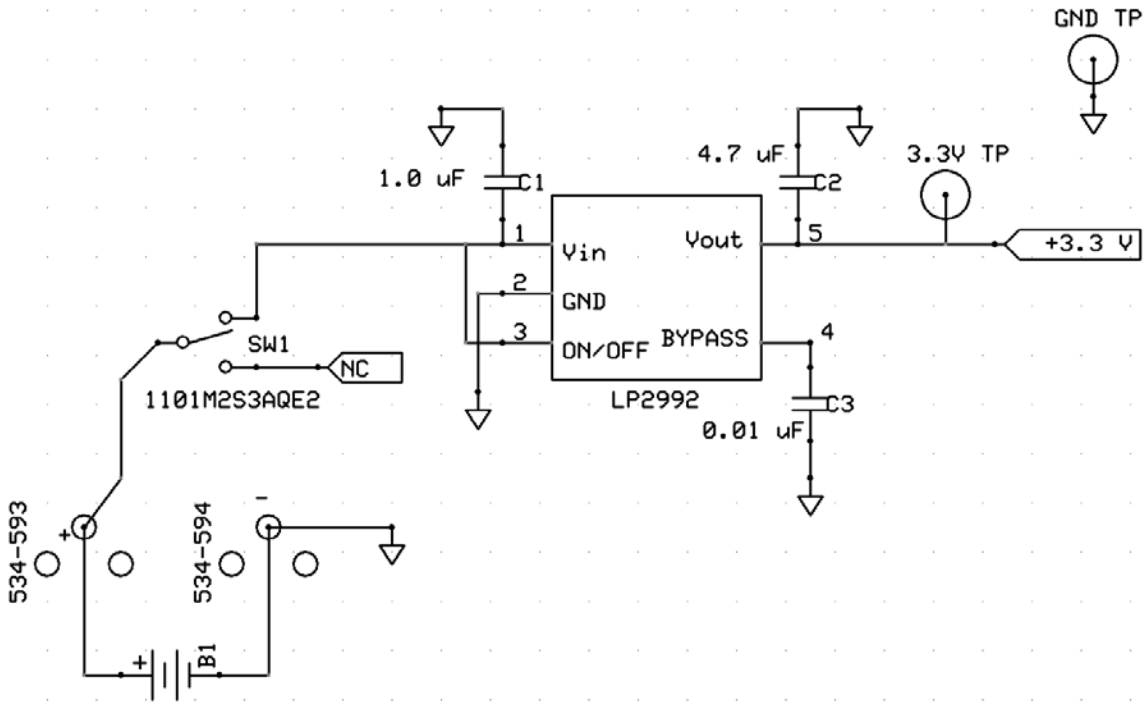


Figure 21: Schematic of Voltage Regulator as it Interfaces to Other Components

Table 3: Elaboration of Each Pin Connection on the LP2992 Voltage Regulator

Pin #	Name	Description
1	Vin	Voltage input pin. Connect +9V from battery here. 1.0 uF bypass capacitor is placed here.
2	GND	Connected to ground.
3	ON/OFF	Used for turning on or off the regulator. This option is not used in the schematic, so it is tied to Vin
4	BYPASS	Connect 0.01 uF bypass capacitor here for best performance
5	Vout	Output voltage of a regulated +3.3V is sourced from here at a maximum 250 mA. 4.7 uF bypass capacitor is placed here.

6.1.2.4 JTAG Connection

Programming and debugging of the microcontroller is accomplished through a 6-pin JTAG interface, using a MSP-FET430 Flash Emulation Tool (FET) by Texas Instruments [36]. A seventh pin to serve as a common ground between the programmer and each transmitter unit is also required. The FET loads code developed for the microcontroller into the microcontroller memory where the code can be debugged by stepping through code line-by-line and viewing memory and registers as a result of code execution.

Figure 22 shows the schematic of the JTAG Connection and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 4, is an elaboration of each pin and an explanation of what interfaces to it.

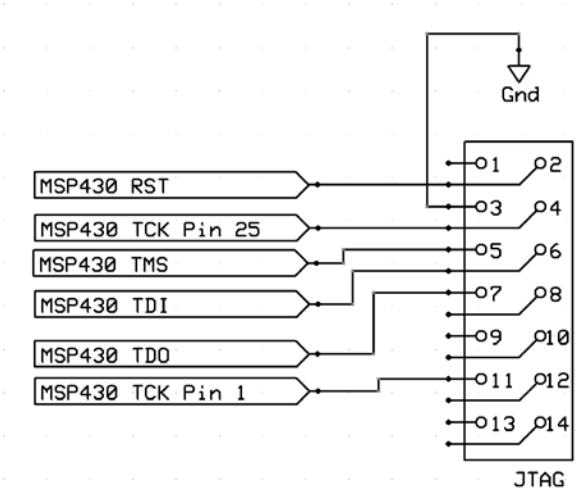


Figure 22: Schematic of JTAG Connection as it Interfaces to Other Components

Table 4: Elaboration of Each Pin Connection on the JTAG Connection

Pin #	Name	Description
1	-	Not Connected.
2	RST	The debugger uses the RST pin to reset the device (microcontroller). The debugger assets the RST pin when the debugger is started and when programming the device (microcontroller).
3	GND	This pin is available to provide a common ground between the host computer/laptop and the board
4	TCK	This pin is the Test Clock of the JTAG connection. It synchronizes internal state machine operations
5	TMS	This pin is the Test Mode State of the JTAG connection. It is sampled at the rising edge of TCK to determine the next state.
6	TDI	This pin is the Test Data In of the JTAG connection. It represents the data shifted into the device's test or programming logic. It is sampled at the rising edge of TCK when the internal state machine is in the correct state
7	TDO	This pin is the Test Data Out of the JTAG connection. It represents the data shifted out of the device's test or programming logic and is valid on the falling edge of TCK when the internal state machine is in the correct state
8	-	Not Connected.
9	-	Not Connected.
10	-	Not Connected.
11	TCK	This pin is the Test Clock of the JTAG connection. It synchronizes internal state machine operations
12	-	Not Connected.
13	-	Not Connected.
14	-	Not Connected.

6.1.2.5 Antenna

A ¼ wavelength monopole whip antenna designed for a center frequency of 433.92 MHz is used for each transmitter unit. The antenna chosen, ANT-433-CW-QW [31], is by Linx Technologies, Inc.

6.1.2.6 Additional Hardware Aspects of the Transmitter Unit (Tag)

6.1.2.6.1 Board-Level Shielding

A PCB-level enclosure, by LeaderTech, Inc., was chosen as tests during the alpha test version indicated that shielding was vital to isolating the circuitry from picking up unwanted transmissions from the transmitter (the antenna should be the only point for picking up transmissions). As such, the PCB shielding was used with the transmitter. The shielding serves the purpose of ensuring that the antenna is the only element radiating.

The shielding part number is 48-CBSFN-1.0x2.0x.40 by LeaderTech, Inc. [43] and the assembled enclosure lid with fence is 1.0" x 2.0" x 0.4" (LxWxH) made with 0.015" pre-tin plated steel. For shielding, each enclosure requires an aluminum fence that allows for the lid (enclosure) to be easily attached and removed.

6.1.2.6.2 Printed Circuit Board

The printed circuit board (PCB) is the medium in which all components and integrated circuits reside and interface with each other. The PCB is made of a 0.062 inch thick FR-4 epoxy glass substrate; the PCB is a 2-layer design, meaning that it has a top and bottom metalized copper layer. Conversely, a 4-later or greater design has metalized copper layers sandwiched between FR-4 layers (as well as with the top and bottom copper layers). Approximately 1 ¼ ounce of copper is distributed over the collective top and bottom layers, giving about 0.0017 inches of copper thickness in each layer. Connecting components and integrated circuits is accomplished using metalized traces acting as conductors which route power and signals to and from these components and integrated circuits. Routing and mounting of any components and integrated circuits can be done on either or both top and bottom copper layers.

6.2 RECEIVER UNIT (READER) HARDWARE DESIGN

The following sections detail the hardware design of the receiver unit, starting with a description of the overall hardware's operation followed by specific detailed descriptions of hardware components in the receiver unit.

6.2.1 Receiver (Reader) Description of Operation

The RTLS Receiver System is used to track a transmitter in real time. The methodology behind the system's operation is that each receiver in the system will reduce its own receiver sensitivity to the point where the sensitivity level will only permit a transmitter to be detected within a narrow distance threshold away from the receiver and then repeating the process from a higher sensitivity to a lower sensitivity continuously to ascertain the location of the transmitter as it moves. At a greater sensitivity level, the receiver has the capability of detecting a transmitter further away than at a lower sensitivity level. Once it is determined at what threshold point an RTLS Receiver Unit can and cannot "see" the transmitter, information is then reported to a centralized location for processing over a Wi-Fi network.

6.2.2 Detailed Functional Block Descriptions

The following subsections of the receiver hardware design contain detailed descriptions of the functional block diagrams of the system as detailed in Section 5.2.1.

6.2.2.1 Microcontroller

The microcontroller used on each receiver unit is required to control the digital step attenuator (DSA), the RF receiver, and data communication on the Wi-Fi network via the WiPort. The microcontroller used is the MSP430F2132 by Texas Instruments [25]. The microcontroller used on each receiver unit is the same as the one used on the transmitter unit. It uses a 16-bit Architecture design with 264 KB of Flash Memory and 512 B of RAM. It is outfitted with a 16 MHz external crystal as the main clock and is programmed/debugged through a JTAG interface. The onboard 16-bit hardware timers are used for interrupting in the software and capturing demodulated data from the RF receiver. The Universal Serial Interface Controller (USIC) serves as a serial transmitter/receiver interface to the WiPort for transmitting and receiving data on an 802.11b/g wireless network.

A total of twelve pins are configured as General Purpose Input/Outputs, with six used for controlling the attenuation setting of the DSA. The remaining six are used for controlling and interfacing to the RF receiver. Additionally three more pins are used; two for transmitting/receiving data via the WiPort, and the third interfaces to a capture register of a hardware 16-bit timer, which captures the time of a rising or falling edge. This is used for determining the length of a bit period between successive edges on the demodulated data line from the RF receiver. Lastly, six pins are used for programming (loading program code) and debugging (halting code, stepping into code, etc.) via the JTAG interface, as is done for the microcontroller on the transmitter unit. Seven pins in total are used from the JTAG interface – one for a common ground and six interfaced to the microcontroller.

Figure 23 shows the schematic of the microcontroller and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 5, is an elaboration of each pin and an explanation of what interfaces to it.

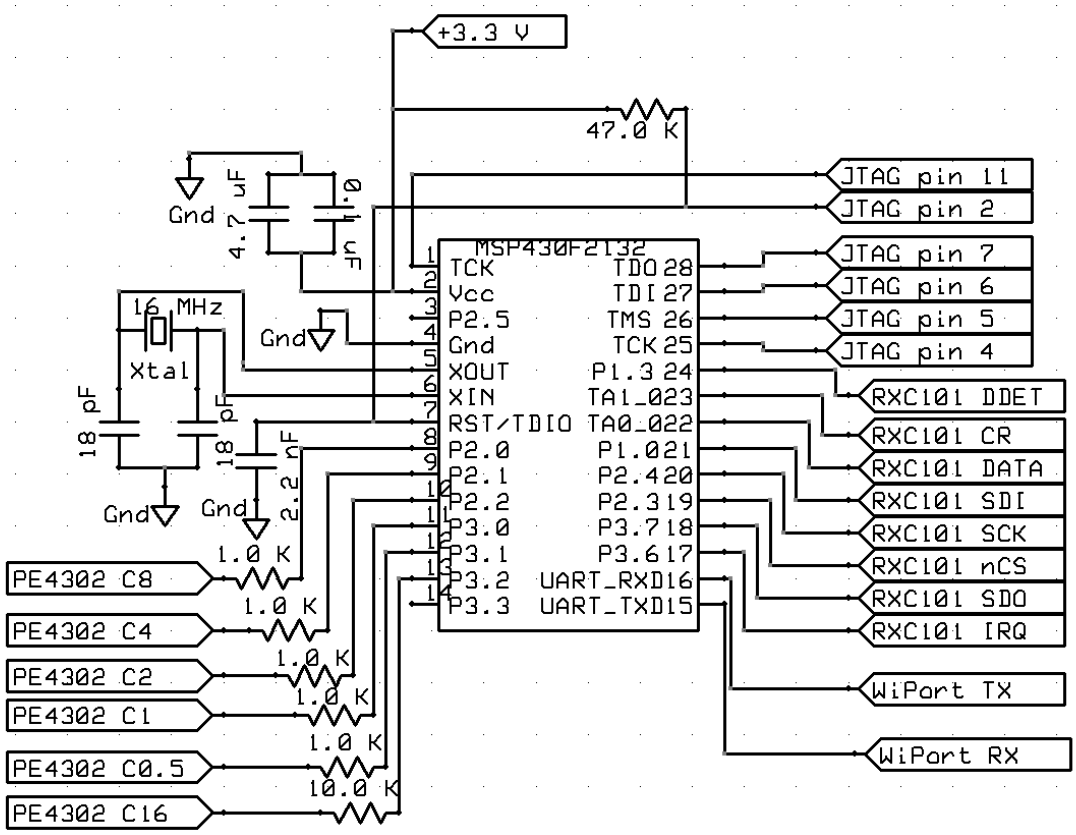


Figure 23: Schematic of MSP430F2132 Microcontroller as it Interfaced to Other Components

Table 5: Elaboration of Each Pin Connection on the MSP430F2132 Microcontroller

Pin #	Name	Description
1	TCK	This pin is connected to pin 11 of the JTAG interface connection.
2	Vcc	This is the power pin of the microcontroller. This pin requires a +3.3V input. Bypass capacitors are added as close as possible to this pin for power supply noise filtering.
3	NC	Not Connected
4	Gnd	This pin is connected to the board's common ground.
5,6	Xout, Xin	These pins are connected to an external crystal which serves as the main clock of the microcontroller. A 16.0 MHz clock is used in this case with two 18 pF loading capacitors connected to the crystal.

Table 5 (continued)

7	RST	This pin requires a 47.0K Ohm pull-up resistor (because the pin is active low) to reset the device when re-programming the microcontroller and a 2.2 nF filter capacitor. The value of the resistor is provided in the datasheet for the microcontroller.
8	C8	Controls pin C8 of the Digital Step Attenuator (DSA). Attenuates incoming signal to the DSA by an additional 8 dB.
9	C4	Controls pin C4 of the Digital Step Attenuator (DSA). Attenuates incoming signal to the DSA by an additional 4 dB.
10	C2	Controls pin C2 of the Digital Step Attenuator (DSA). Attenuates incoming signal to the DSA by an additional 2 dB.
11	C1	Controls pin C1 of the Digital Step Attenuator (DSA). Attenuates incoming signal to the DSA by an additional 1 dB.
12	C0.5	Controls pin C0.5 of the Digital Step Attenuator (DSA). Attenuates incoming signal to the DSA by an additional 0.5 dB.
13	C16	Controls pin C16 of the Digital Step Attenuator (DSA). Attenuates incoming signal to the DSA by an additional 16 dB.
14	-	Not used/connected.
15	SCK	SPI Data Clock.
16	nCS	Connect to TXC101's Chip Select Input. Selects the chip for an SPI data transaction. Active Low for a 16-bit read or write function
17	SW1	Connect to TXC101's SW1. Not used, but connected in schematic.
18	SW2	Connect to TXC101's SW2. Not used, but connected in schematic/
19	SW3	Connect to TXC101's SW3. Not used, but connected in schematic.
20	ClkOut	Connect to TXC101's ClkOut. Not used, but connected in schematic.
21	nIRQ	Connect to TXC101’s nIRQ. Not used, but connected in schematic.
22	SDI	SPI Data in.
23	SW4	Connect to TXC101's SW3. Not used, but connected in schematic.
24	MOD	Data to be transmitted is sent on this pin
25	TCK	Used for JTAG Communication. The Test Clock (TCK) pin is used to synchronize the state machine used in programming the microcontroller.
26	TMS	Used for JTAG Communication. The Test Mode State (TMS) determines the next state by sampling on the rising edge of TCK.
27	TDI	Used for JTAG Communication. The Test Data In (TDI) pin is used to shift data into the device’s programming logic.
28	TDO	Used for JTAG Communication. Test Data Out (TDO) pin is used to shift data out of the device’s programming logic

6.2.2.2 Radio Frequency (RF) Receiver

Each receiver unit has been designed with a commercial off-the-shelf (COTS) RF receiver, RXC101 by RFM [28]. The RF receiver is capable of four frequency bands of which the 433.92 MHz band is used for the RTLS. The receivers use a 2-FSK modulation scheme with a variable channel bandwidth (the FSK deviations from center frequency) to receive the transmitted wireless signals. The RF receiver's input comes from the output of the DSA and the demodulated data line from the receiver is fed as an input to the microcontroller.

The RF receiver is outfitted with a 10 MHz external crystal and requires several discrete components for matching the RF-positive and RF-negative pin input impedances to 50 Ohms at 433.92 MHz. The RF receiver and accompanying software to control it have been configured to operate with the RF receiver having a constant +3.3VDC power supply (differing from this will change the operational characteristics), just as with the RF transmitter. Additionally, the RF receiver is programmed using an SPI bus interface to four of its pins from the microcontroller.

Figure 24 shows the schematic of the RF receiver and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 6, is an elaboration of each pin and an explanation of what interfaces to it.

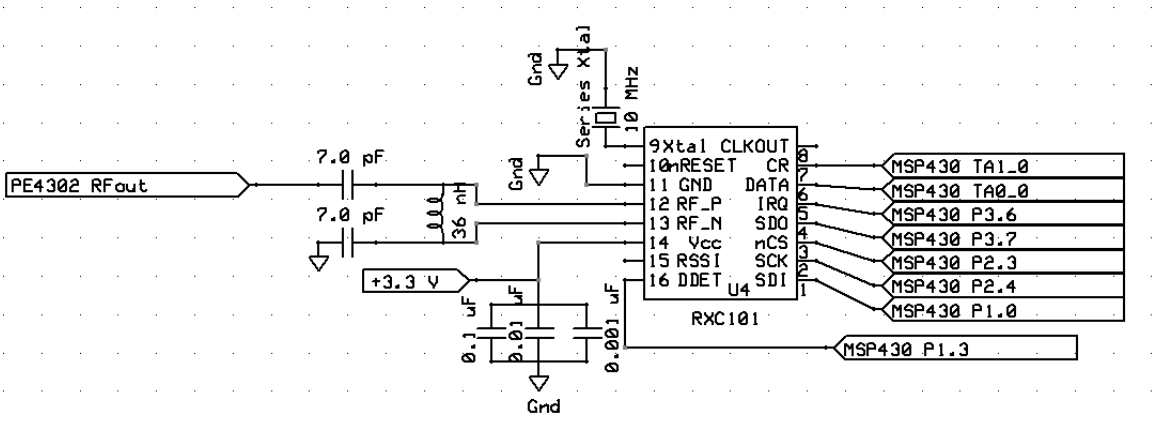


Figure 24: Schematic of RXC101 RF Receiver as it Interfaced to Other Components

Table 6: Elaboration of Each Pin Connection on the RXC101 RF Receiver

Pin #	Name	Description
1	SDI	SPI Data in
2	SCK	SPI Data Clock
3	nCS	Chip Select Input. Selects the chip for an SPI data transaction. Active Low for a 16-bit read or write function
4	SDO	Serial Data Out. Used to read out the Status Register contents
5	IRQ	Interrupt request Output - Not Used
6	DATA	Data Output. When FIFO buffer is not used, data can be taken from this pin.
7	CR	Data Recovery Clock Output. Recovered Data clock Output when FIFO. Not used.
8	ClkOut	This pin is connected to a +3.3V power line. No further decoupling capacitors are needed to reduce power supply noise
9	Xtal	Connect 10 MHz crystal. The crystal requires a series capacitance load, which is set programmatically in the Configuration Register of the RXC101
10	nRST	Reset output. Active Low. Not used
11	GND	Connect to common ground
12	RF_P	RF Differential I/O.
13	RF_N	RF Differential I/O.
14	Vdd	This pin is connected to a +3.3V power line. Three decoupling capacitors are used to filter out power supply noise
15	RSSI	Analog RSSI Output. Not used.
16	DDET	Valid Data Detector Output. Not used.

6.2.2.3 Digital Step Attenuator (DSA)

Reducing each receiver unit's receiver sensitivity is vital to the methodology of the receiver unit's functionality as detailed in Section 1.2.2 and 3.1.3. The digital step attenuator (DSA), by Peregrine Semiconductor PE4302 [29], is a step attenuator covering a 31.5 dB attenuation range in 0.5 dB steps. The DSA creates threshold boundaries which create regions (boundaries) where the receiver unit can and cannot demodulate the incoming electromagnetic signals, which allows for the system to estimate where a transmitter unit is located.

Figure 25 shows the schematic of the digital step attenuator and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 7, is an elaboration of each pin and an explanation of what interfaces to it.

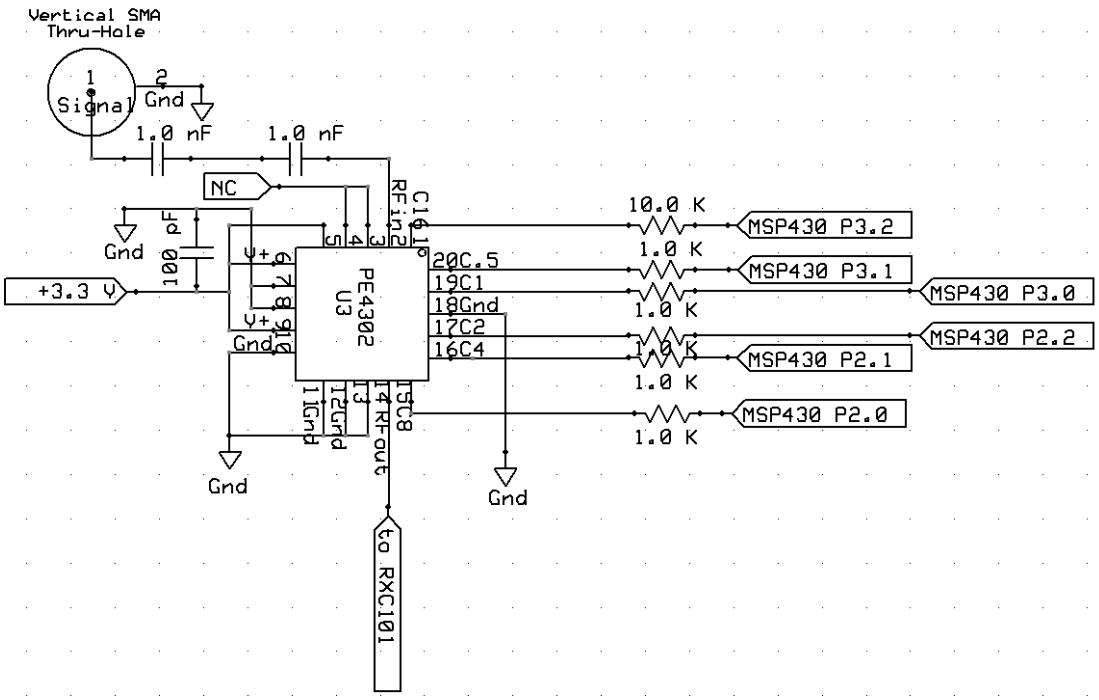


Figure 25: Schematic of PE4302 Digital Step Attenuator (DSA) Interfaced to Components

Table 7: Elaboration of Each Pin Connection on the Digital Step Attenuator (DSA)

Pin #	Name	Description
1	C16	Attenuation control bit line. Attenuates incoming signal to the DSA by an additional 16 dB. A current limiting resistor (10.0 K) is placed in series with this line and the MSP430 I/O line that controls this attenuation control bit line.
2	RFin	This is the pin that the antenna is connected to. This serves the purpose of providing the RF input to the attenuator from a Vertical SMA Thru-Hole connector via a 50 Ω transmission line
3	-	Not used/connected.
4	-	Not used/connected.
5	LE	The Latch Enable (LE) pin is active low, and is connected to Vdd because parallel programming mode is used.
6	Vdd	Power supply pin. Connected to a 3.3V supply, along with a bypass capacitor for reducing power supply noise
7	Vdd	Power supply pin. Connected to a 3.3V supply, along with a bypass capacitor for reducing power supply noise
8	Vdd	Power supply pin. Connected to a 3.3V supply, along with a bypass capacitor for reducing power supply noise

Table 7 (continued)

9	Vdd	Power supply pin. Connected to a 3.3V supply, along with a bypass capacitor for reducing power supply noise
10	GND	Connected to ground.
11	GND	Connected to ground.
12	GND	Connected to ground.
13	P/S	Parallel/Serial Mode Section bit line. Connect to ground to set LOW to use Parallel Mode.
14	RFout	This pin is connected via a 50Ω transmission line to the receiver. This pin outputs the attenuated RF signal as a result of the attenuation added as selected using the attenuation control bit lines.
15	C8	Attenuation control bit line. Attenuates incoming signal to the DSA by an additional 8 dB. A current limiting resistor (1.0 K) is placed in series with this line and the MSP430 I/O line that controls this attenuation control bit line.
16	C4	Attenuation control bit line. Attenuates incoming signal to the DSA by an additional 4 dB. A current limiting resistor (1.0 K) is placed in series with this line and the MSP430 I/O line that controls this attenuation control bit line.
17	C2	Attenuation control bit line. Attenuates incoming signal to the DSA by an additional 2 dB. A current limiting resistor (1.0 K) is placed in series with this line and the MSP430 I/O line that controls this attenuation control bit line.
18	GND	Connected to ground.
19	C1	Attenuation control bit line. Attenuates incoming signal to the DSA by an additional 1 dB. A current limiting resistor (1.0 K) is placed in series with this line and the MSP430 I/O line that controls this attenuation control bit line.
20	C0.5	Attenuation control bit line. Attenuates incoming signal to the DSA by an additional 0.5 dB. A current limiting resistor (1.0 K) is placed in series with this line and the MSP430 I/O line that controls this attenuation control bit line.

6.2.2.4 WiPort

The serial (RS-232) to Wi-Fi converter device, a WP200200SG-02, WiPort by Lantronix [34], allows the RF receiver unit to transmit and receive serial data via Wi-Fi over 802.11 b/g networks. The WiPort replaces the Serial-to-USB converter used in the Alpha-Test and Beta-

Test I versions of the RTLS system, which was used to relay information back to the host computer for location estimation of a tag, and the WiPort communicates over a local network via an access point. Additionally, the WiPort requires a 40-pin surface mount-to male-micro-header-pin connector, FTMH-120-03-F-DV-ES by Samtec [44].

Figure 26 shows the schematic of the WiPort and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 8, is an elaboration of each pin and an explanation of what interfaces to it.

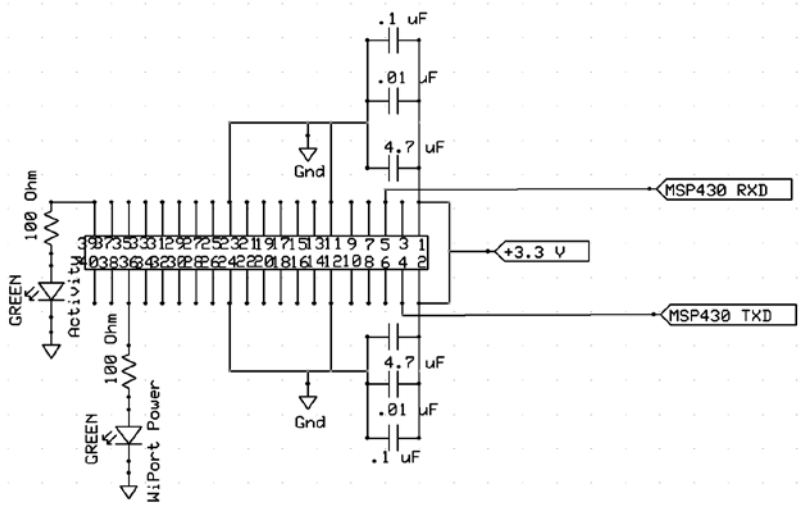


Figure 26: Schematic of WP200200SG-02 WiPort as it Interfaced to Other Components

Table 8: Elaboration of Each Pin Connection on the WP200200SG-02 WiPort

Pin #	Name	Description
1,2	3.3V Power	These pins take a +3.3V source and require several bypass capacitors at each pin
3	-	Not Used/Connected.
4	RXD0	This pin connects to the TXD pin of the MSP430 microcontroller. The receive and transmit pins on each device are connected so that the information transmitted from one device is received by the other.

Table 8 (continued)

5	TXD0	This pin connects to the RXD pin of the MSP430 microcontroller. The receive and transmit pins on each device are connected so that the information transmitted from one device is received by the other.
6 - 10	-	Not Used/Connected.
11,12	GND	Connected to ground.
13-22	-	Not Used/Connected.
23,24	GND	Connected to ground.
25-35	-	Not Used/Connected.
36	Reserved	This pin is active high on the WiPort B model and active low on the WiPort G model. This pin indicates the power status of the WiPort.
37,38	-	Not Used/Connected.
39	WLAN Activity LED	This pin is active high on the WiPort B model and active low on the WiPort G model. This pin indicates the WLAN activity of the WiPort.
40	-	Not Used/Connected.

6.2.2.5 Boost Converter and Power Considerations

The motivation for using a boost converter in the design of each receiver unit comes from the large amount of current necessary to operate the circuitry of the unit, mostly coming from operation of the WiPort, which requires upwards of 1.2W when transmitting continuously. To continuously supply a 3W load for the entire board (at maximum), it became necessary to find a battery type that could supply a large amount of continuous current. Reasonable considerations for batteries that can source large amounts of current without being overly large in size are the standard AA cell and 9V cell batteries. The current capacity of these two cell types differs among manufacturers, but comparing a standard Alkaline AA cell with a standard Alkaline 9V cell from the same manufacturer, the AA cell has nearly five times the current capacity (mAh) than that of a 9V cell for the same current load [45][46]. The Alkaline AA cell can source continuously 500 mA and even higher for instantaneous loads. At 1.5 V (nominal) per AA cell

with a 500 mA continuous draw, the RTLS receiver unit will need four AA cells in parallel. With a 3W load, using four Alkaline AA cells, the batteries can theoretically power the receiver units for almost 3 hours [46]. If a 9V battery were used to power the same 3W load, the circuit load would be 333 mA, which would theoretically provide just over 1.2 hours of battery life [45]. Using more than one 9V battery to increase the battery life using 9V cells quickly becomes a size problem, particularly for finding suitable battery holders. It is for these reasons, that the RTLS receiver units were designed to be powered using AA cells.

Presented with the problems of needing batteries capable of sourcing high amounts of continuous current, the necessary 3.3V operating voltage for all parts on the receiver unit, and the problem that a battery's voltage under a load will drop as the battery is drained, it becomes apparent that if our battery supply is over 3.3 V, we will need a step-down voltage regulator, and if the voltage of the battery supply is lower than the 3.3Vs necessary to run the receiver unit, then some sort of step-up DC-DC converter is necessary. Because the configuration (four AA cells in parallel) for the batteries being used will still be below the 3.3V's necessary, a step-up DC-DC converter is necessary. The variant of a step-up DC-DC converter suitable for this application is the boost converter. The boost converter will step up the input voltage to a voltage above the input voltage. As the input voltage drops (which happens over time as a cell is drained), the output voltage from the boost converter will be held constant (this does not hold true once the input voltage drops below a certain level – in the case of this design, a voltage lower than about 1.1 V cannot be sufficiently boosted to +3.3V to supply a 3W load). The boost converter used in this design, the LT1308B, by Linear Technologies [30], is a high current, 600 kHz fixed frequency DC-DC converter.

Figure 27 shows the schematic of the boost converter and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 9, is an elaboration of each pin and an explanation of what interfaces to it.

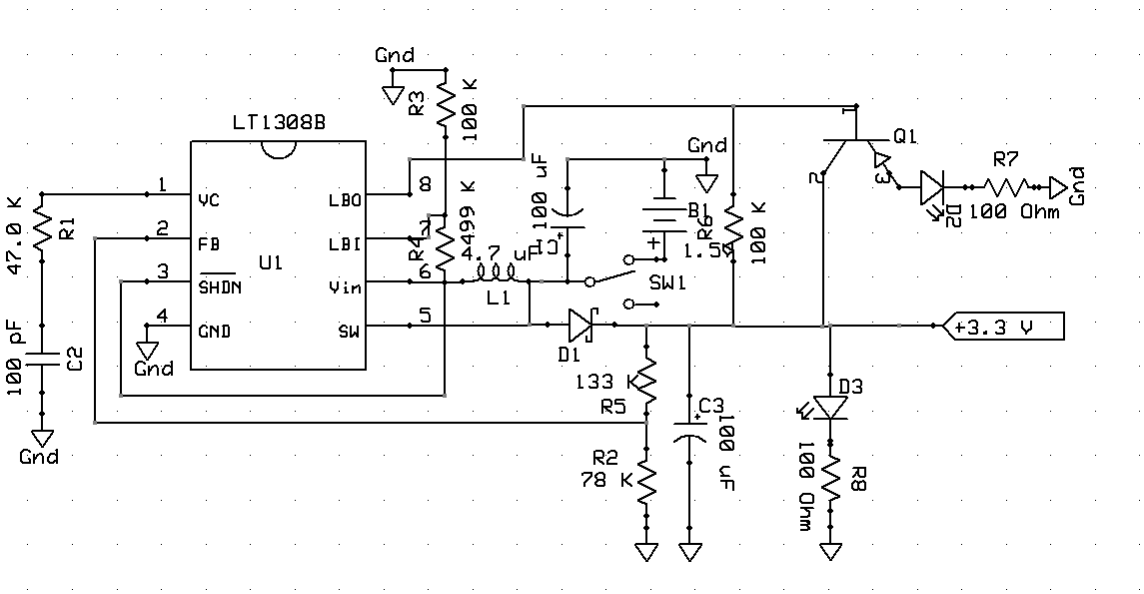


Figure 27: Schematic of LT1308B Boost Converter as it Interfaced to Other Components

Table 9: Elaboration of Each Pin Connection on the LT1308B Boost Converter

Pin #	Name	Description
1	Vc	Compensation Pin for Error Amplifier. Requires a series RC from this pin to ground (typically 47 kΩ and 100 pF). Minimize trace area
2	FB	Feedback pin. Reference voltage is 1.22 V. Connect resistive divider tap here and minimize trace area at this pin. Resistive divider is set according to: $Vout = 1.22V(1 + R1/R2)$
3	SHDN	Shutdown. Ground this pin to turn off the IC. To enable tie this pin to 1V or higher (SHDN does not need to be at the same potential as Vin to enable the device).
4	GND	Ground. PCB copper connected to ground will also function as a heat sink.
5	SW	Switch Pin. Connect inductor/diode here. Minimize trace area at this pin to reduce EMI

Table 9 (continued)

6	Vin	Supply pin. Connect 1.5 V input here. Must have a local bypass capacitor at this pin connected directly to ground
7	LBI	Low-Battery Detector Input. Low-Battery detector does not function when SHDN is grounded. Float LBI pin is not used. 200mV reference. LBI voltage must stay between -100 mV and 1V
8	LBO	Low-Battery Detector Output. Open collector – can sink 50 uA. A 100 kΩ should be used here

6.2.2.6 JTAG Connection

Programming and Debugging of the microcontroller is accomplished through a 6-pin JTAG interface using a MSP-FET430 Flash Emulation Tool (FET), by Texas Instruments [36]. A seventh pin to serve as a common ground between the programmer and each RTLS Receiver Unit is also required. The FET facilitates loading the code developed for the microcontroller into the microcontroller's memory where the code can be debugged by stepping through code line-by-line and viewing memory and registers as a result of code execution.

Figure 28 shows the schematic of the JTAG Connection and functionally where each pin connects/interfaces to other modules and peripheral circuitry. Below this figure, in Table 10, is an elaboration of each pin and an explanation of what interfaces to it.

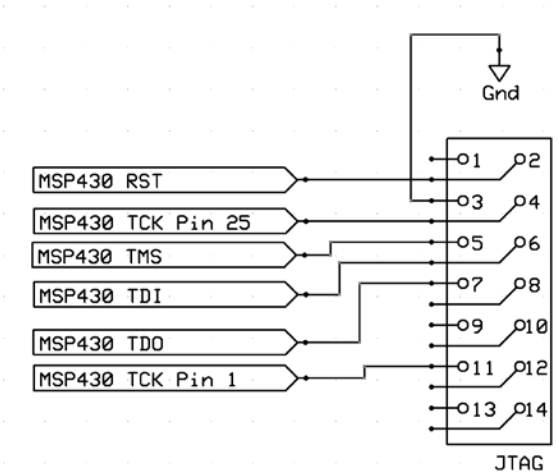


Figure 28: of JTAG Connection as it Interfaces to Other Components

Table 10: Elaboration of Each Pin Connection on the JTAG Connection

Pin #	Name	Description
1	-	Not Connected.
2	RST	The debugger uses the RST pin to reset the device (microcontroller). The debugger assets the RST pin when the debugger is started and when programming the device (microcontroller).
3	GND	This pin is available to provide a common ground between the host computer/laptop and the board
4	TCK	This pin is the Test Clock of the JTAG connection. It synchronizes internal state machine operations
5	TMS	This pin is the Test Mode State of the JTAG connection. It is sampled at the rising edge of TCK to determine the next state.
6	TDI	This pin is the Test Data In of the JTAG connection. It represents the data shifted into the device's test or programming logic. It is sampled at the rising edge of TCK when the internal state machine is in the correct state
7	TDO	This pin is the Test Data Out of the JTAG connection. It represents the data shifted out of the device's test or programming logic and is valid on the falling edge of TCK when the internal state machine is in the correct state
8	-	Not Connected.
9	-	Not Connected.
10	-	Not Connected.
11	TCK	This pin is the Test Clock of the JTAG connection. It synchronizes internal state machine operations
12	-	Not Connected.
13	-	Not Connected.
14	-	Not Connected.

6.2.2.7 Antennas

A ¼ wavelength monopole whip antenna designed for a center frequency of 433.92 MHz is used for each RTLS Receiver Unit. The antenna chosen, ANT-433-CW-QW [31], is by Linx Technologies, Inc.

A small size 2.45 GHz PCB [32] antenna is placed on the PCB to function as an antenna at 2.45 GHz for each WiPort to use for Wi-Fi communication over 802.11b/g networks.

6.2.2.8 Board-Level Shielding

Board-level shielding on the transmitter units also appears on the receiver units. The same shielding and fence enclosure is used for the receiver units as the transmitter units. The information regarding the board-level shielding is reproduced here for convenience. A PCB-level enclosure, by LeaderTech, Inc., was chosen as tests during the alpha test version indicated that shielding was vital to avoid picking up transmissions from the local antenna. As such, the PCB shielding was used with the transmitter. The shielding serves the purpose of ensuring that the antenna is the only element radiating.

The shielding part number is 48-CBSFN-1.0x2.0x.40 by LeaderTech, Inc. [43] and the assembled enclosure lid with fence is 1.0" x 2.0" x 0.4" (LxWxH) made with .015" pre-tin plated steel. For shielding, each enclosure requires an aluminum fence that allows for the lid (enclosure) to be easily attached and removed.

6.2.2.9 Printed Circuit Board

The same circuit board type used for the transmitter unit was used for the receiver unit. For convenience, the information regarding the circuit boards is reproduced here. The printed circuit board (PCB) is the medium that all components and integrated circuits reside and

interface with each other. The PCB is made of a 0.062 inch thick FR-4 epoxy glass substrate. The PCB is a 2-layer design meaning that it has a top and bottom metalized copper layer. Conversely, a 4-layer or greater design has metalized copper layers sandwiched between FR-4 layers (as well as with the top and bottom copper layers). Approximately 1 ¼ ounce of copper is distributed over the collective top and bottom layers giving about 0.0017 inches of copper thickness in each layer. Connecting components and integrated circuits is accomplished using metalized traces acting as wires which route power and signals to and from these components and integrated circuits. Routing and mounting of any components and integrated circuits can be done on both top and bottom copper layers.

7.0 SOFTWARE DESIGN

The software design for the RTLS was created in two Software Development Kits (SDK): Code Composer Essentials v3.1 (CCE3.1) and Microsoft Visual Studio 2008. The specific SDK used to develop each software application of the RTLS is discussed further in Section 8.0 . The software designed for the RTLS units will be onboard the microcontrollers of the receiver units and the transmitter while a host computer will have a graphical user interface (GUI) to communicate over a Wi-Fi 802.11 b/g network with the receiver units. The following subsections explore the software designed for the transmitter units, receiver units, and host computer, respectively. Each subsection elaborates on the designs to detail the flow of the software and major aspects of the flowcharts detailed below, which can be drawn from the system specifications from Section 5.0 .

7.1 TRANSMITTER/TAG SOFTWARE DESIGN

The following subsections detail the specifics of the transmitter unit's software starting with a description of operation followed by a step-by-step description of the flowchart illustrating the software execution process.

7.1.1 Transmitter/Tag Software Description of Operation

The software onboard the transmitter's microcontroller controls the RF transmitter, configuring it and sending data to it for wireless transmission. The software for the transmitter is quite simple in that the transmitter will be always on and need to continuously transmit a constant square wave. This makes the software for the transmitter very simple. Some simple initializations, configuring the RF transmitter, and then continuously toggling a data line to the RF transmitter.

7.1.2 Transmitter/Tag Software Flowchart

Figure 29 illustrates the flow of the transmitter software. When the software begins execution, the master clock is configured first, as this is important for configuring the RF transmitter via the SPI interface, which requires precise clocking. Next, the RF transmitter is configured for the data rate and source of data control all through the SPI interface. Finally, the data line to the transmitter is continuously toggled at a precise and constant interval to make the 50% duty cycle square wave.

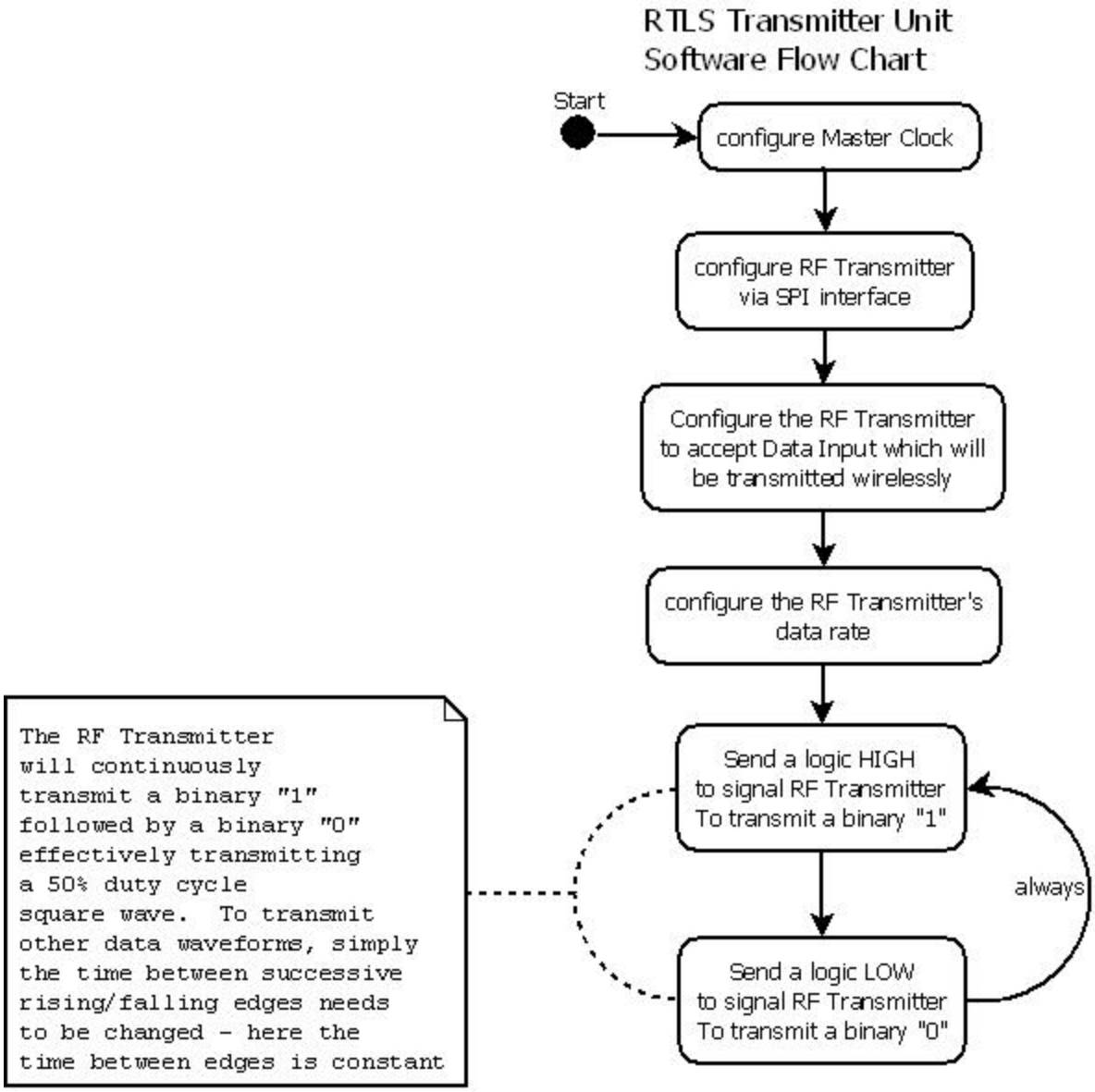


Figure 29: Transmitter Unit Software Flow Chart

7.2 RECEIVER/READER SOFTWARE DESIGN

The following subsections detail the specifics of the receiver unit software, starting with a description of operation followed by a step-by-step description of the flowchart illustrating the software's execution process.

7.2.1 Receiver/Reader Software Description of Operation

The software onboard the receiver unit microcontroller has the primary function of controlling the digital step attenuator (DSA) processing the incoming demodulated data from the receiver, and determining a best estimate location of a transmitter while arbitrating Wi-Fi network requests for the determined location of the transmitter. The software for the receiver is highly dependent upon hardware timers and interrupts which allow for the arbitration of threads that can request resources at any time.

7.2.2 Receiver/Reader Software Flowchart

Figure 30 illustrates the flow of the receiver unit software. When the software begins execution, the program starts with an RF receiver configuration routine via the SPI interface followed by configuring many of the I/O pins. After this, the hardware timers and clocks are configured which will be used for processing incoming demodulated data from the RF receiver. Following this, all global interrupts are enabled and the bulk of the program begins execution. At this point, requests though the Universal Serial Communication Interface can be made at any point from the host computer, which makes requests for the tag location over the Wi-Fi network.

If a request is made, the current value (in memory) of the tag location will be reported. If the program has not gathered information for all threshold levels in order to update the tag location estimate, then this value in memory will reflect the last location estimate before all of the new information has been gathered [and likewise, before the program has completed this process for the first time, the value in memory is an arbitrary value].

The bulk of the program begins execution with the bit-select lines on the DSA being cleared (effectively setting the DSA to introduce no attenuation of the incoming signal) – the program will not return to this state until it has finished gathering all information at each of the attenuation thresholds. The program will then continuously check to see if it has gathered all of the information it needs at the current threshold level. This statement will evaluate to false for one of two possible reasons; (1) if the program has not set the next attenuation state and enabled the hardware to process the incoming demodulated data from the RF receiver, or (2) if the program is still processing the incoming demodulated data from the RF receiver. When this statement evaluates to false, the program will check to see if the next attenuation state has been set. If it has not, the program will set it and then enable the hardware timers that will process the incoming demodulated data and then return to continuously checking if all processing is done at the current threshold level. Otherwise if the next attenuation state was already set, the program will likewise return to checking if all processing has completed at the current threshold level. Once processing at the current threshold level has completed, the program will check to see if processing has been completed for all threshold levels. If not, then the program will start once again from the point of checking if the program has finished gathering all information at the current level (which will not have been completed yet, upon first checking this after the test for being finished at all levels fails).

Once processing for all threshold levels has been completed, the system will disable all hardware interrupts to prevent overwriting of the gathered data. After this, the system will calculate a best estimate location of the tag and update this value in memory for whenever the latest location estimate is requested by the host computer over the Wi-Fi network.

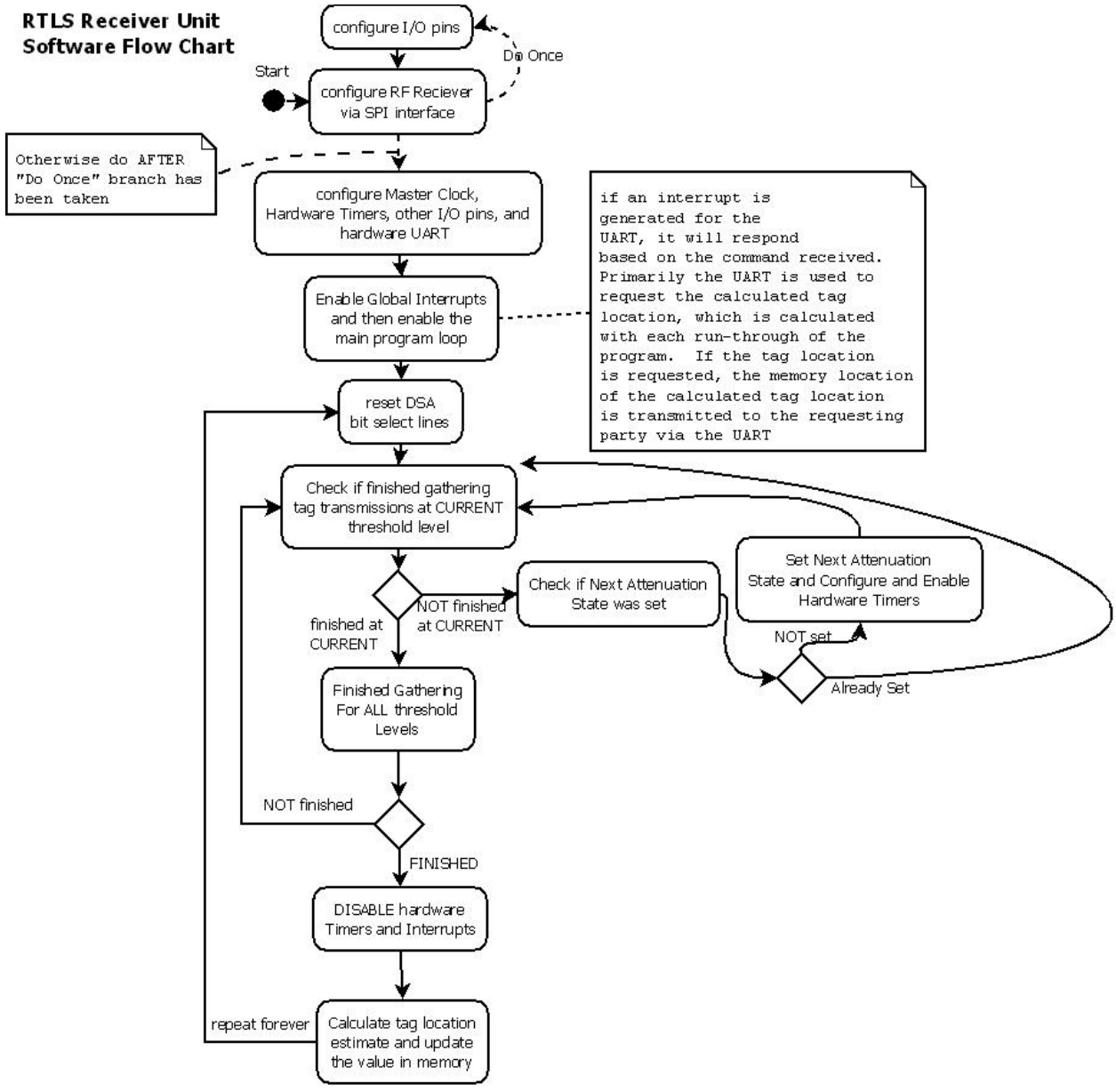


Figure 30: Receiver Unit Software Flow Chart

7.2.3 Digital Step Attenuator (DSA) Steps (Threshold Levels)

Each attenuation state is chosen to be a change in the attenuation from the previous state, with a state of no attenuation for the initial state. The amount of attenuation and number of attenuation steps (threshold levels) is subject to the precision desired in the RTLS design. Too many threshold levels and the variation between one threshold level to the next will not be significant to interpret a change; choosing step sizes that allow for one to observe a marked change in the bit error rate (BER) is the first design parameter when choosing step sizes – one can use very large step sizes, but this will also reduce the precision of the system. For the RTLS presented in this thesis, the step sizes were simply chosen such that there would be a large enough change from one step to the next once the transmitter moved a large enough distance – while precision is an important factor, the reliability and consistency of the implementation was most important for the prototypes developed so the step sizes were chosen to be arbitrarily large enough to see consistent results.

7.2.4 Location Determination and Bit Error Rate (BER)

Location estimates are computed by processing the incoming demodulated data from the receiver. This means that the location is determined by the received symbols, more specifically, the quality of the receiver symbols. Just because a symbol is received intact does not mean that there exists a reliable communication link between the transmitter and receiver. Because of this, the bit error rate (BER) is most useful when ascertaining the quality of the information (moreover, the communication link) that is being received. If the BER increases to an unacceptable degree at a threshold level, then it can be said that the transmitter's information

cannot reliably be delivered to the receiver, indicating that the transmitter is out of range. This is the process by which a threshold is determined indicating the location of the transmitter with respect to the receiver unit.

7.3 REMOTE HOST SOFTWARE DESIGN

The remote host software has the task of aggregating the location estimates determined by each receiver unit for the relative distance away that a tag is from each respective receiver unit. Once this information is aggregated, a best estimate location is calculated based on *a priori* knowledge of the relative locations of receiver units to each other and the threshold boundary ranges of each receiver unit.

Figure 31, Figure 32, and Figure 33 (the same sequence diagram split into three parts/figures) illustrate the software interaction with the graphical user interface (GUI) to operate the software following a sequence diagram. First, as the program is opened, the program form GUI will initialize and be presented on the screen. Secondly, the user will click on “Wi-Fi” and then “Connect” where the visualization software will then attempt to connect to each WiPort over the Wi-Fi network. If all devices could be connected, then a message box will be presented stating that all devices could be connected. Otherwise, an error message box will display stating that there is a connection issue, which the user will need to attend. After this, the user will need to click on “Open” and then “Layout” to open up a room layout file. Once the user navigates to the room layout file to open, then visualization software will read the file, and display the information contained within the file, including walls and receiver units, on the GUI form on the screen for the user to see. After this, the user simply needs to click “Visualize!” and then the

program will begin to interrogate the receiver units for the locations of tags that each receiver unit has calculated. From here, the visualization software will send a request for a tag location to the first WiPort device on a receiver unit, the software will wait for the WiPort to respond back with a data packet containing the location information of a tag. After this, the visualization software will repeat this process for all WiPorts on receiver units in the RTLS. Once each receiver has reported a location estimate for a tag, the visualization software will take this information and calculate a best estimate location of the tag. Before this best estimate location is reflected on the GUI, it must be noted that a timer has been constantly going off as a background task that will update the GUI with the location of a tag. If the memory value of the location of a tag is overwritten with a new value, then the next time this background task runs, it will update the GUI with the new location of a tag. This process repeats forever until the user exits (clicks the “Quit” menu button) the software.

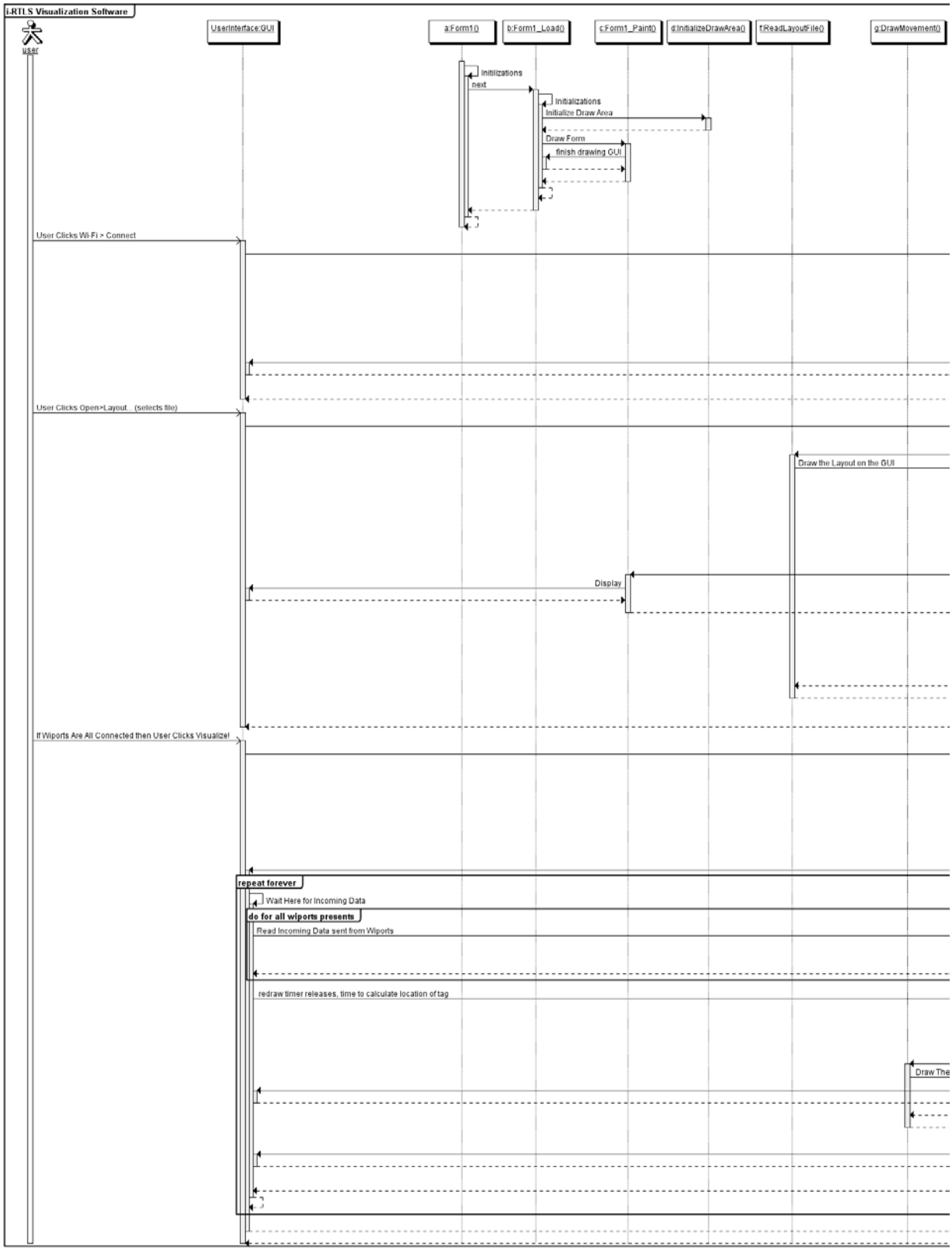


Figure 31: RTLS Visualization Software Sequence Diagram - Part 1

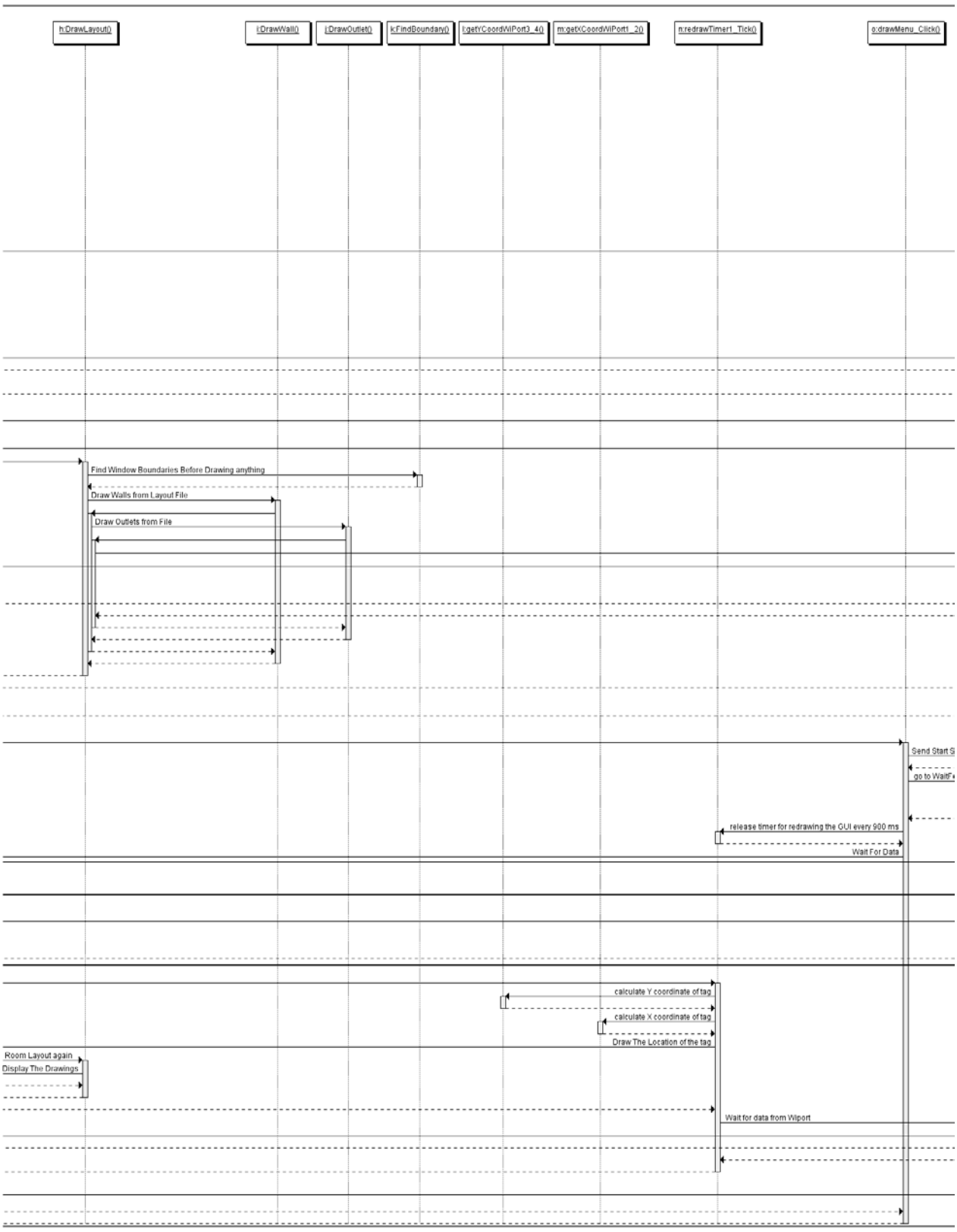


Figure 32: RTLS Visualization Software Sequence Diagram - Part 2

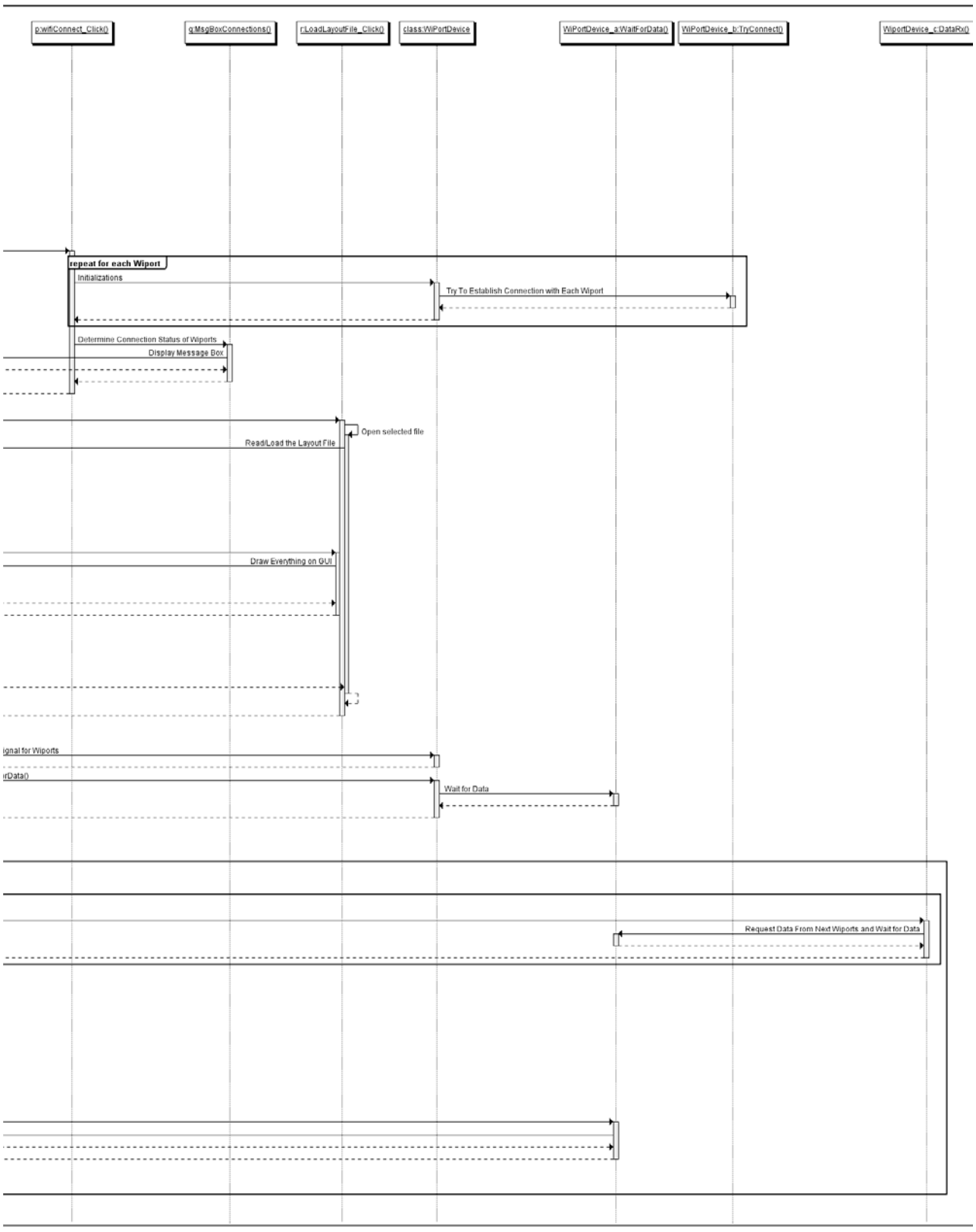


Figure 33: RTLS Visualization Software Sequence Diagram - Part 3

8.0 UNIT PROGRAMMING, ASSEMBLY, AND SET-UP

Proper assembly and set-up of the system ensures that the system will perform according to the results detailed in Section 9.0 . Figure 34 and Figure 35 show the fully assembled transmitter and receiver units, respectively. The following subsections will explore how the transmitter and receiver units were programmed along with their assembly (populating the boards) and some basic set-up.

Figure 34: Fully Assembled Transmitter Unit

Figure 35: Fully Assembled Receiver Unit

8.1 PROGRAMMING THE UNITS

The transmitter and receiver units' microcontrollers were programmed in C/C++ using Texas Instruments' Code Composer Essentials v3.1. The transmitter and receiver units are connected through the 14-pin male header connection on the PCB using the JTAG programmer as shown in Figure 36 and Figure 37, respectively.

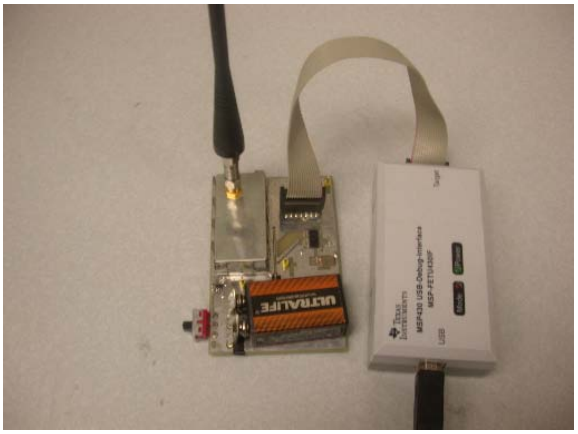


Figure 36: Transmitter Unit connected with JTAG Connection

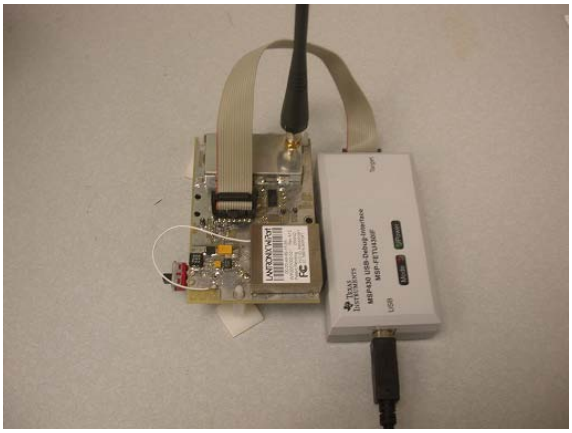


Figure 37: Receiver Unit connected with JTAG Connection

8.2 PRINTED CIRCUIT BOARD (PCB) AND OVERALL SCHEMATIC

The printed circuit boards (PCB) allow for all components and circuitry to be mounted and connected in an organized way. The PCB's are first designed by creating a schematic representation of the circuit to be implemented on a PCB and then linking this schematic to the

PCB layout making the routing of components and traces a more organized process. Both the schematic and PCB layouts were designed using ExpressPCB's software. ExpressSCH version 7.0.2 was used to design the schematics of the transmitter and receiver units and ExpressPCB version 7.0.2 was used to design the PCB layouts of the units.

The following subsections detail the overall schematics and PCB layouts of the transmitter and receiver units. The overall schematics are the combination and interfacing of the components detailed in the hardware design (Section 6.0) of the units and the PCB layouts are the physical implementations of the schematics.

8.2.1 Transmitter Unit Circuit Board and Overall Schematic

Illustrated in Figure 38 is the PCB layout of the transmitter unit along with the schematic associated with this layout in Figure 39. Clearly illustrated in the PCB layout is the PCB Board-Level Shielding where the PCB shield's fence is soldered along with the location where the battery is situated, which are all discussed further in the subsections below.

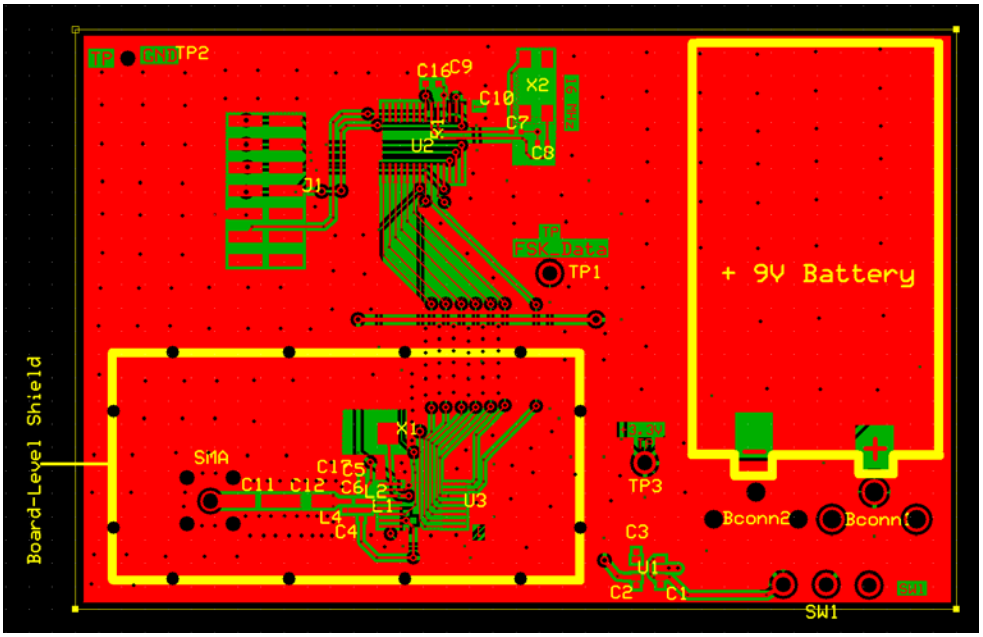


Figure 38: PCB Layout of the Transmitter Unit

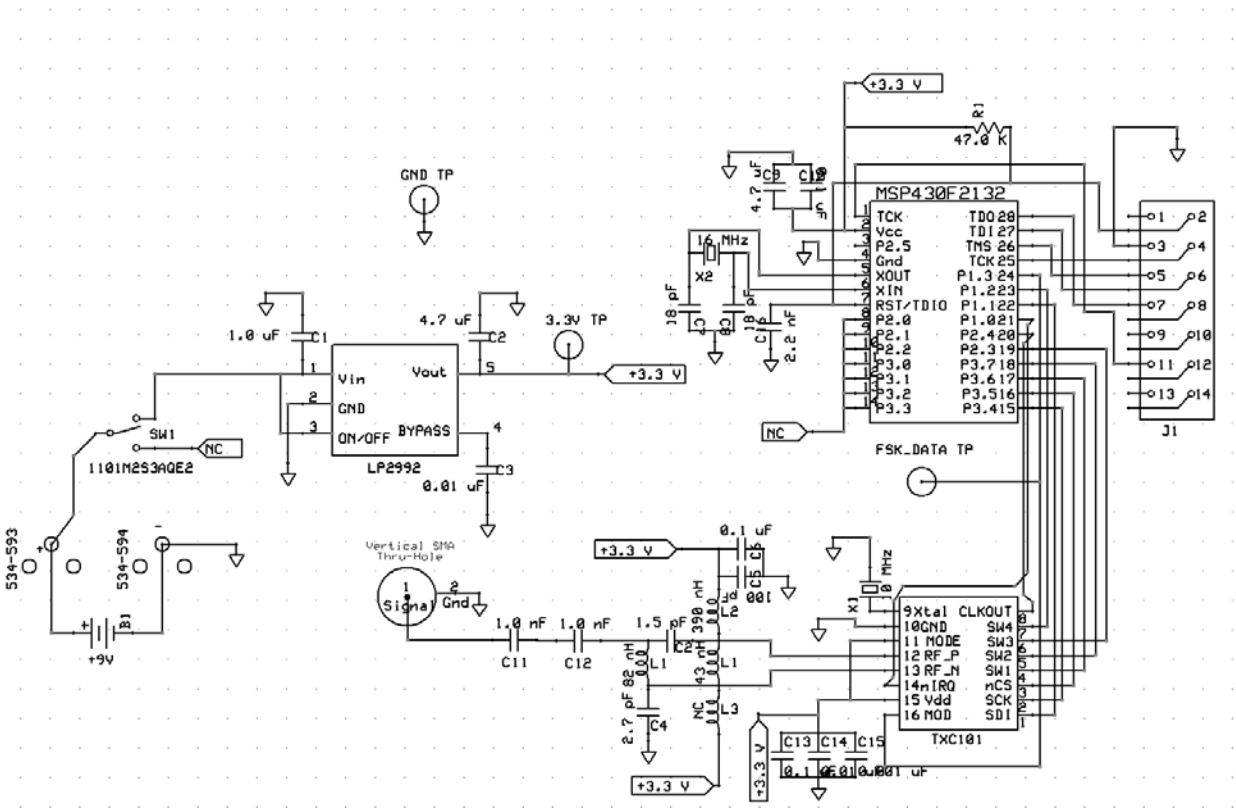


Figure 39: Schematic of the Transmitter Unit

8.2.2 Receiver Unit Circuit Board and Overall Schematic

Illustrated in Figure 40 is the PCB layout of the receiver unit, along with the schematic associated with this layout, in Figure 41. Clearly illustrated in the PCB layout is the PCB Board-Level Shielding where the PCB shield's fence is soldered along with the location where the battery is situated, which are all discussed further in the subsections below.

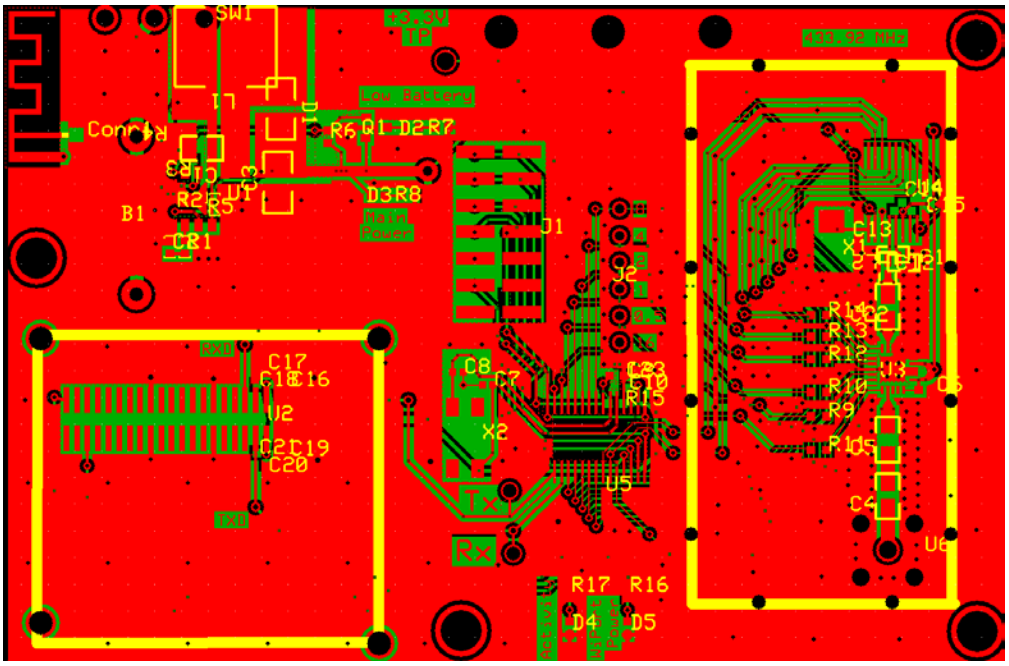


Figure 40: PCB Layout of the Receiver Unit

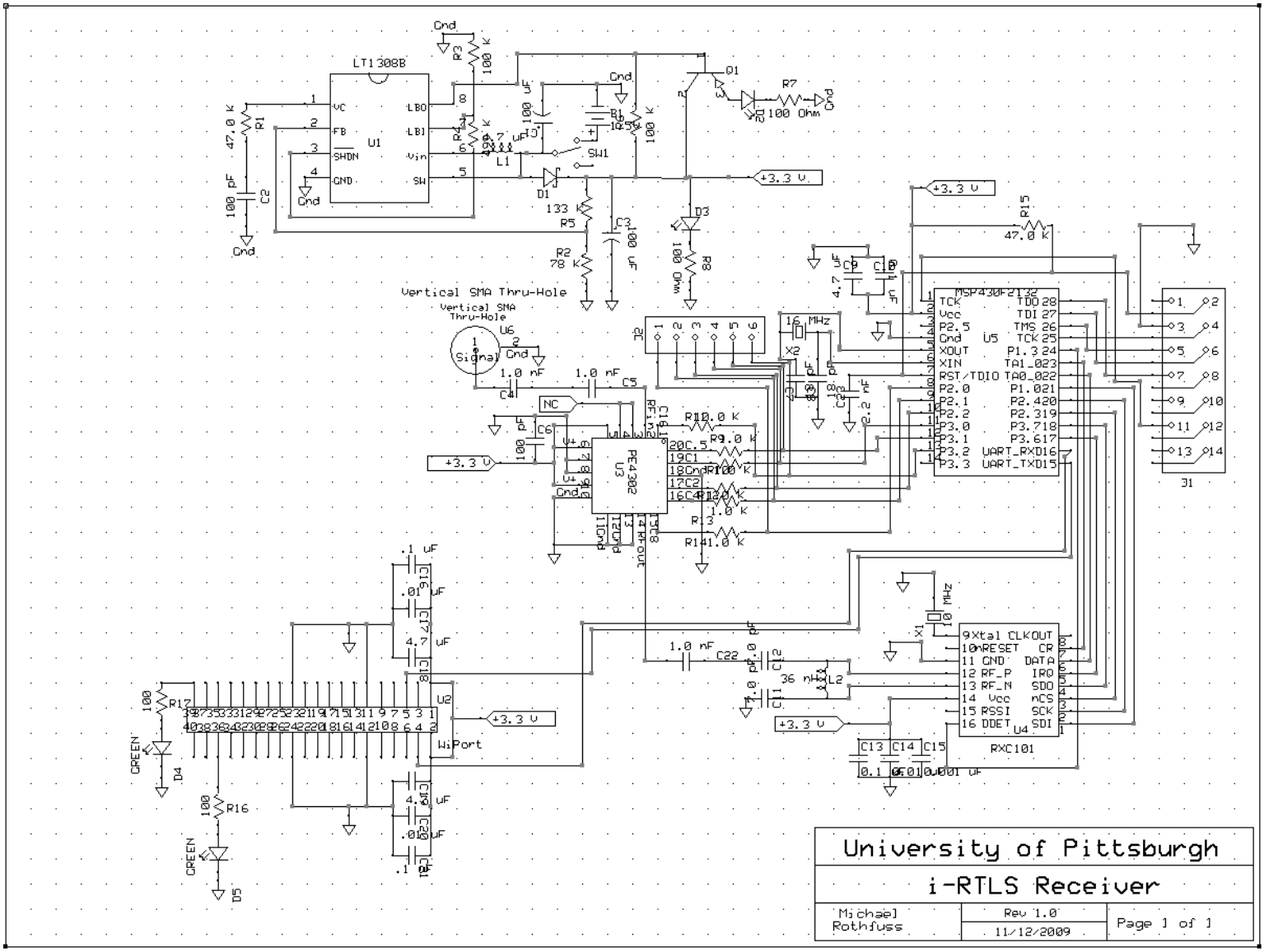


Figure 41: Schematic of the Receiver Unit

8.2.3 PCB Board-Level Shield

PCB Board-Level shielding is required for both the transmitter and receiver units as described in the transmitter and receiver unit hardware design Sections 6.1.2.6.1 and 6.2.2.8 respectively. Assimilating the PCB Board-Level Shield into the transmitter and receiver unit designs requires some light machining: the fence of the shielding enclosure must be soldered in place as shown in Figure 42 and Figure 43, for the transmitter and receiver units, respectively, and a hole must be drilled slightly greater than the diameter of the SMA connector that 433 MHz ¼ wave whip antenna screws onto for the shielding lid to properly isolate the RF electronics of the transmitter and receiver units. The shielding lid will rest in the crenellations of the fence shielding.

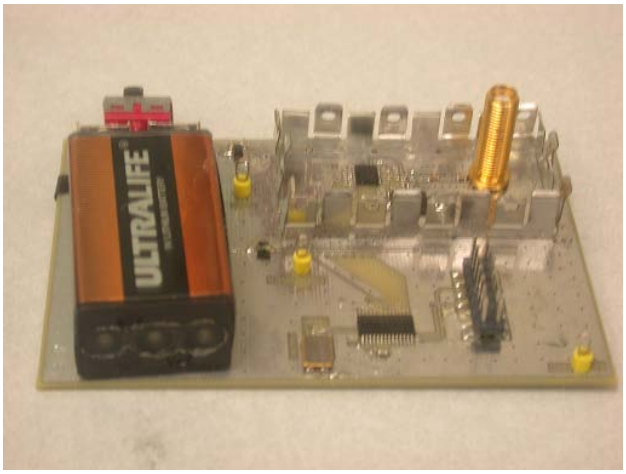


Figure 42: Transmitter Unit Showing Exposed Fence of the PCB Board-Level Shield

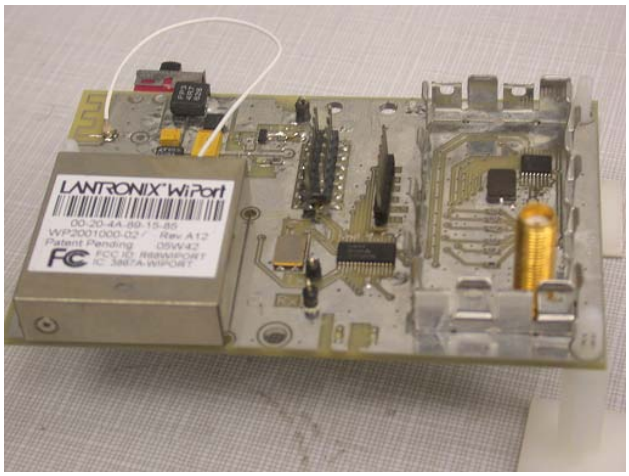


Figure 43: Receiver Unit Showing Exposed Fence of the PCB Board-Level Shield

8.3 ANTENNAS

The transmitter and receiver units' antenna set-ups differ in that the transmitter unit uses a single antenna while the receiver unit uses two antennas. The transmitter and receiver units use the same ¼ wave whip antenna, with the receiver unit using an additional planar PCB printed antenna.

8.3.1 Transmitter Unit Antenna

The transmitter unit antenna uses a 433 MHz ¼ wave monopole that connects to the through-hole SMA connector protruding through the PCB Board-Level Shield on the transmitter unit. Mating this antenna to the SMA connector requires an SMA male to Reverse Polarity SMA female adapter, which can be seen encircled in white as it is used in Figure 44.

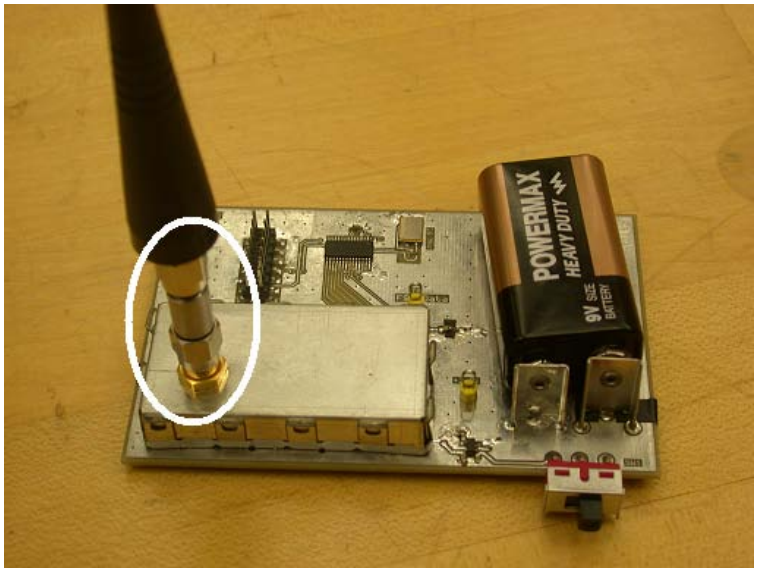


Figure 44: Transmitter Unit Showing Antenna Connected with a SMA Adapters

8.3.2 Receiver Unit Antennas

The RTLS receiver uses two antennas. One is a 433 MHz ¼ wave monopole antenna that connects to the through-hole SMA connector. This requires mating the antenna to the through-hole SMA connector with an SMA male to Reverse Polarity SMA female adapter as seen encircled in white as used in Figure 45.

The second antenna is a planar 2.45 GHz Wi-Fi antenna. Mating to the antenna requires a U.FL connector, by Hirose Electric Co., Ltd. The manufacturer part number for it is U.FL-R-SMT(10) [35] , and it is soldered in place appropriately at the feed-point of the antenna. Each WiPort will have to be opened up and outfitted with a U.FL to U.FL mini coaxial cable. One end of this cable will connect inside of the WiPort and the other end will connect to the U.FL connector that was soldered to the feed-point of the planar Wi-Fi antenna as shown encircled in white as used in Figure 46.

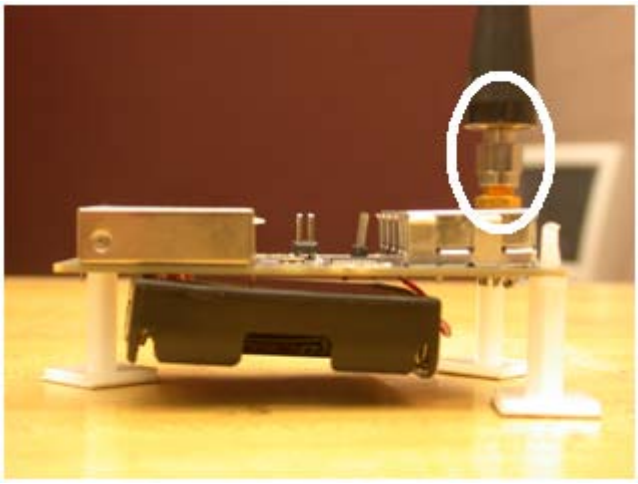


Figure 45: Receiver Unit Showing Antenna Connected with a SMA Adapters

Figure 46: WiPort mating to Planar PCB Antenna Using U.FL mini coaxial cable

8.4 BATTERIES AND STAND-OFFS

8.4.1 Transmitter Unit Battery and Battery Holder

The battery holder for the transmitter unit uses simple metalized connectors to hold the +9V battery. The battery simply connects to these contacts and rests on the PCB. Figure 47 illustrates the metalized connectors, which are circled in white in this figure.

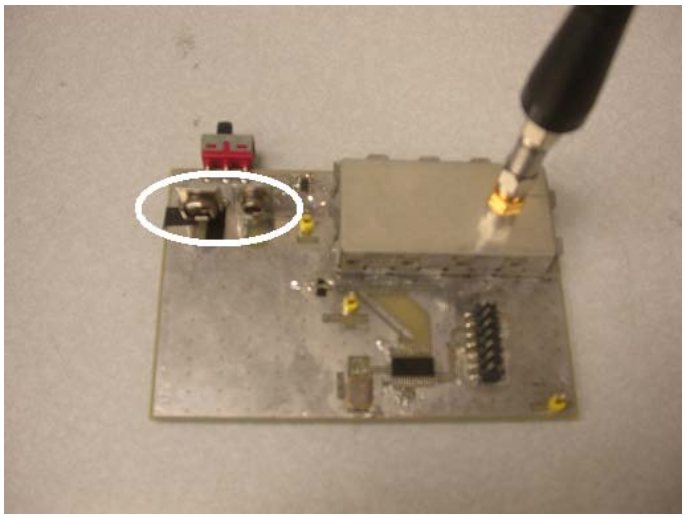


Figure 47: Transmitter Unit Showing +9V Battery Connectors Circled in White

8.4.2 Receiver Unit Battery, Battery Holder, and Stand-Offs

The battery holder being used needs to be modified. The AA battery holder used to hold four batteries needs to be modified to place all of the AA cells in parallel because the holder is intended to currently place each AA cell in series with another. To accomplish this, wires are soldered across the four terminals on each end of the holder. A point to note here is that the

batteries, when placed in the holder, will all need to face the same direction (all polarities must be the same on either end of the holder). Thus, it is wise to prune/clip the springs that are used to hold the batteries in place because the batteries will not all be in the intended orientations. This process is necessary because a suitable battery holder for four AA cells in parallel could not be found.

Also, the side of the holder to which the positive terminals of the batteries will be oriented needs to be soldered to the round through-hole as encircled in yellow in Figure 49, while the negative terminal side of the holder should be soldered to somewhere on the ground plane. It is important to note that when soldering the negative terminal, one should take great care in choosing a spot to solder because a poorly chosen current return path can cause problems when powering the receiver unit because of the constantly changing load. This is especially noticeable when powering the device from a digital power supply. A good choice for soldering the negative terminal is the location on the board where there are three large vias, as encircled in white in Figure 49.

Lastly, three plastic stand-offs are inserted into the large via holes on the board to give the receiver unit a sturdy and uniform base. Figure 48 illustrates how the battery holder and plastic stand-offs are connected on the PCB board.

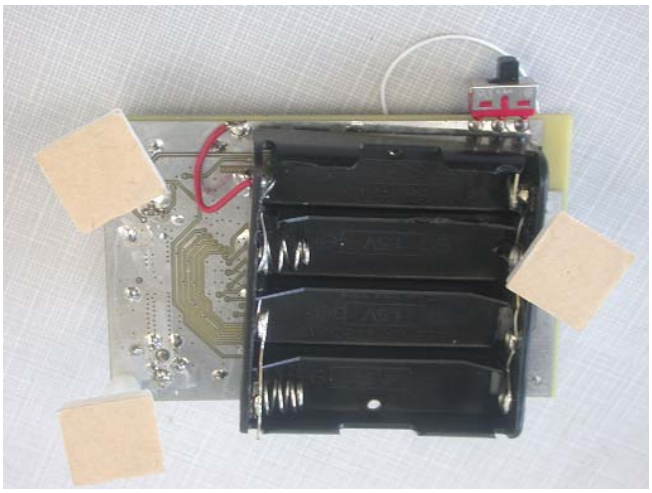


Figure 48: Receiver Unit Showing The Four-AA Cell Battery Holder and Stand-Offs

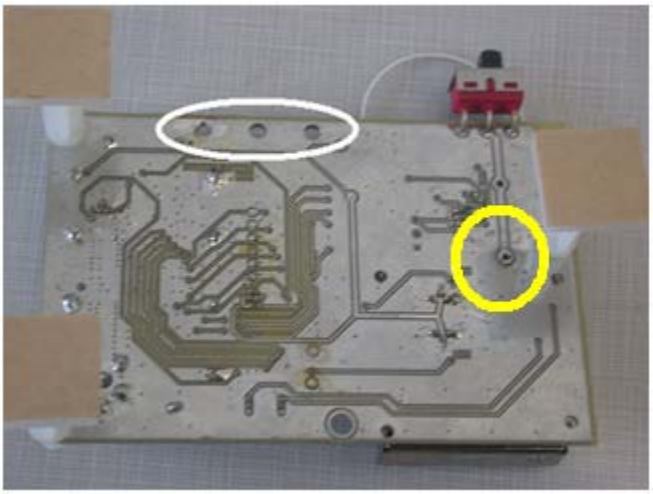


Figure 49: Positive Connection Hole (Yellow) and Negative Connection Holes (White)

8.5 WI-FI NEWORK SET-UP AND PROGRAMMING

Proper configuration of the wireless infrastructure and devices that communicate on it are paramount to location determination using the RTLS presented in this thesis. The wireless

network allows each receiver unit's tag-location estimate to be collected by a host computer to process to come up with a best-estimate location of a tag being tracked.

8.5.1 Wireless LAN

The wireless LAN used for the RTLS presented in this thesis is an 802.11 b/g wireless LAN operated in infrastructure mode. Each device on the network will need to be configured to operate in this mode: all traffic will go through a wireless access point. Figure 50 illustrates the communication links in the wireless LAN. The transmitter units are able to transmit signals to the receiver units, while the host computer has access to the receiver units (and vice versa) through the wireless access point to gather location information about the tag calculated by each individual receiver unit.

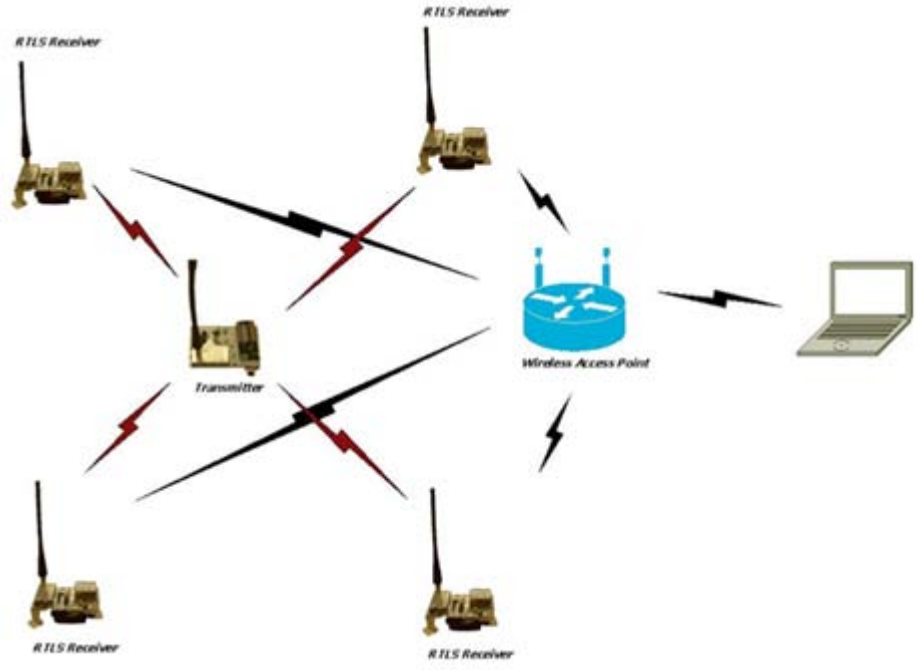


Figure 50: Illustration of the Communication Links in the RTLS with the wireless LAN

8.5.1.1 Setting Up a Network for the RTLS

To set up a wireless LAN for the RTLS presented in this thesis in accordance with the topology illustrated in Figure 50, the following subsections should be followed to configure and set-up each device properly.

8.5.1.1.1 Remote Host and Receiver/Reader Set-Up for Wireless LAN

Using the host machine software requires several steps. Firstly, because the Beta-Test II system is completely wireless, the host PC's wireless Network Interface Card (NIC) must be configured to have a static IP address and corresponding subnet mask. The value that these are set to depends on the IP address and subnet mask of each WiPort device onboard each receiver unit as well as the IP address and subnet mask of the access point.

The physical topology of the RTLS system (Figure 50) requires a wireless access point through which the host machine and the receiver units communicate. The access point functions as a central point through which two-way communication takes place.

As stated previously in this section, proper configuration of IP addresses and the subnet mask is imperative for communication to take place between devices on the network. Because the access point is the point by which all traffic must go, IP addresses and subnet masks must be created accordingly. For example, if the IP address of the access point is set to 169.254.1.100 and then the subnet mask is set to 255.255.0.0, then both the NIC of the host machine and the WiPorts on the receiver units should have an IP address of the type 169.254.XXX.YYY, where XXX and YYY represent any number between 1 and 255, and then the subnet masks should be 255.255.0.0, which is the same for everything communicating in this network scheme. (Note: changes to any IP addresses should be reflected in the Host Machine software's code, which initiates and arbitrates communication to/from the WiPorts via the access point.)

8.5.1.1.2 Configuring the WiPorts

Configuring the WiPorts is a fairly simple task as long as no changes are made to the code on the microcontroller and the host machine regarding their protocols for transmitting and receiving packets. To configure a WiPort for integration into the system, refer to Appendix A. In Appendix A, one will see how one of the WiPorts used in the RTLS system has been configured. To configure each new WiPort, one only needs to change the **bold underlined** portions. It is important to make the bold underlined portions in Appendix B unique to that WiPort being configured because failure to do so will cause a conflict in the system.

The portions in Appendix A that are *italic underlined* are portions that need to be the same across all WiPorts used in the system. These points are shortcuts for reference when configuring the WiPorts. A more in depth look at configuring the WiPorts can be found in the Wiport User's Guide [34].

8.5.1.1.3 Creating a Room Layout File

When using the RTLS visualization software, it must be pre-loaded with the layout representation of the physical room being used for the experiment. To do this, one must click Load > Layout and then select the file for the room layout (a room layout file is listed in Appendix B). To make a new room layout, only four different types of parameters need to be used. Upon looking at the room layout file, one can see a numerical list from 0 through 4 as the first number on each line down through the file. A 0 corresponds to the maximum X and Y boundaries of the program window, a 1 corresponds to the start of a wall of the room, a 2 corresponds to the start of any *next/intermediate* wall in the room, and a 3 corresponds to the end point of a series of interconnected walls. A 4 corresponds to a receiver unit. Each line starts with the 0 through 4 number as just described. The next two numbers are numbers that represent

the X and Y coordinates of that particular component (wall/receiver/window boundary) being defined. The numbers can be as precise as two decimal places, and each number must be one space apart from each other and each new component (wall/receiver/window boundary) must be on a new line. Also, upon looking at the room layout file, it is evident that the walls have been drawn such that they are offset from the program window boundary so that when the red circle is drawn, part or all of the circle doesn't appear if it is drawn near the boundaries of the room.

8.6 ENVIRONMENTAL LAYOUT CONSIDERATIONS

The environmental layout for this RTLS system focused on a simple 2-D square-like virtual room. Figure 51 shows the 2-D virtual room layout within a room. The receiver units are positioned in a "cross" pattern and they are 65" apart from each other. Figure 52 illustrates this where each solid red dot indicates the placement of a receiver module while the black lines represent the boundaries of the actual room's walls. Figure 53 illustrates the RTLS visualization software localizing the transmitter to the center of the virtual room (this corresponds with the location of the transmitter in Figure 51 in the virtual room). The RTLS system is meant to be capable of functioning in any environment, but a point must be made about the necessity to calibrate the receivers for each environmental set-up in which the receivers will reside. By calibration, what is meant is that the maximum thresholds must be measured in terms of the room boundaries as well as to ensure that the RTLS receivers are not positioned too close to large metal objects, which could adversely affect the performance of a receiver unit.

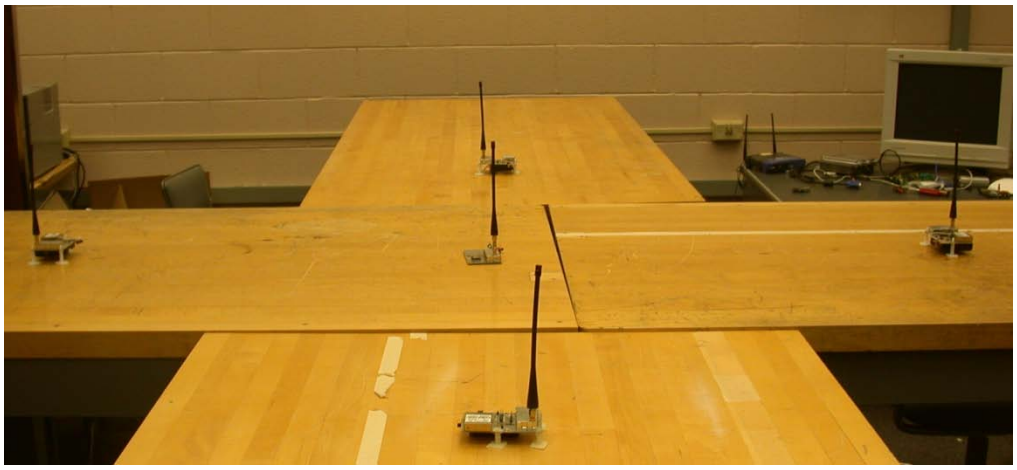


Figure 51: 2-D Virtual Room

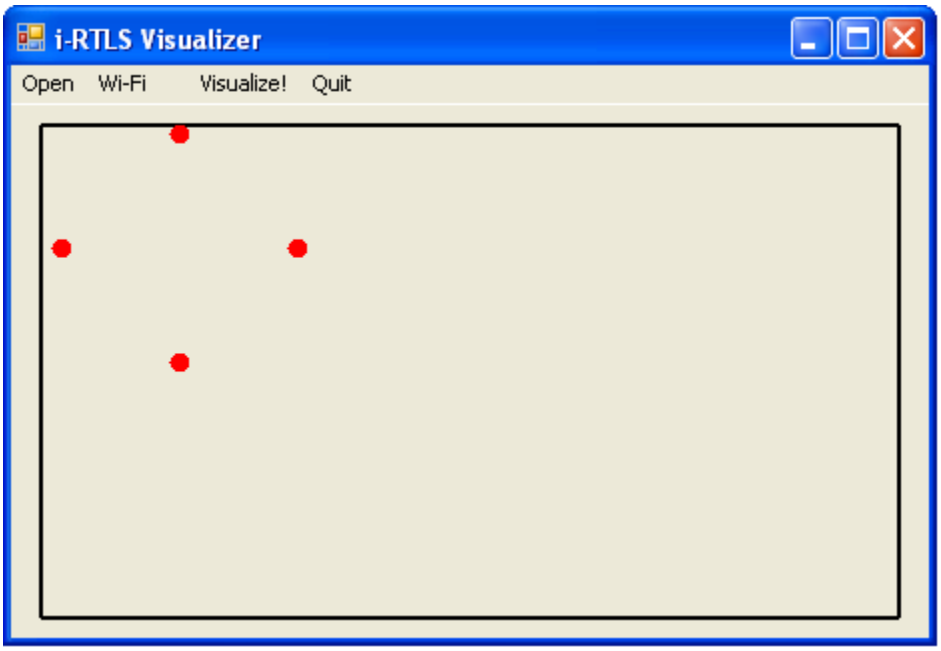


Figure 52: Room Layout in the Visualization Software

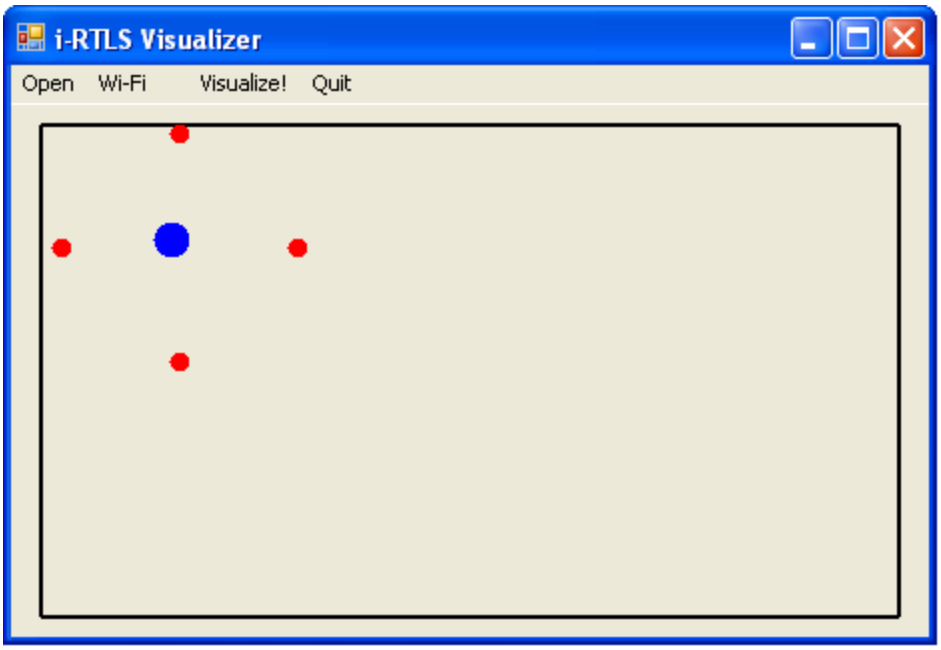


Figure 53: Large Circle Indicates Estimate of Transmitter's Location in the Virtual Room

8.7 OVERALL SYSTEM DEMONSTRATION AND USAGE

With the environmental layout considerations in mind, to demonstrate and use the RTLS presented in this thesis, one must have assembled, programmed, and set-up the system as per the guidelines in Section 8.0 . With everything configured and set-up properly, the system can be operated by running the RTLS visualization software and operating it according to the steps illustrated in the flowchart of Figure 54. The user will need to connect to the WiPorts via the wireless LAN by clicking the "Connect" option under the "Wi-Fi" menu. Once the host computer has successfully established a communication link with all WiPorts in the system, a message box will be displayed stating which WiPorts the host machine has successfully connected to (conversely, if there is an error in connecting to even just one WiPort, a message

box will be displayed stating that there is a connection error requiring the user to find the connection issue and try again). Next, the user must open a room layout file by clicking the "Layout" option under the "Open" menu. After selecting the room layout file, the mapping of the room will be displayed in the RTLS Visualization software's GUI. Finally, the user must simply click the "Visualize!" menu button; from here, the GUI will update with a tag's location relative to the receiver units. To see the tag location change, the user simply moves the transmitter within the confines of the virtual room designated by the set-up of the receiver units (Section 8.6). The GUI will update the location of the tag in real-time. At any point when running the RTLS Visualization software, if the user clicks the "Quit" menu button, the program will exit as illustrated in Figure 54.

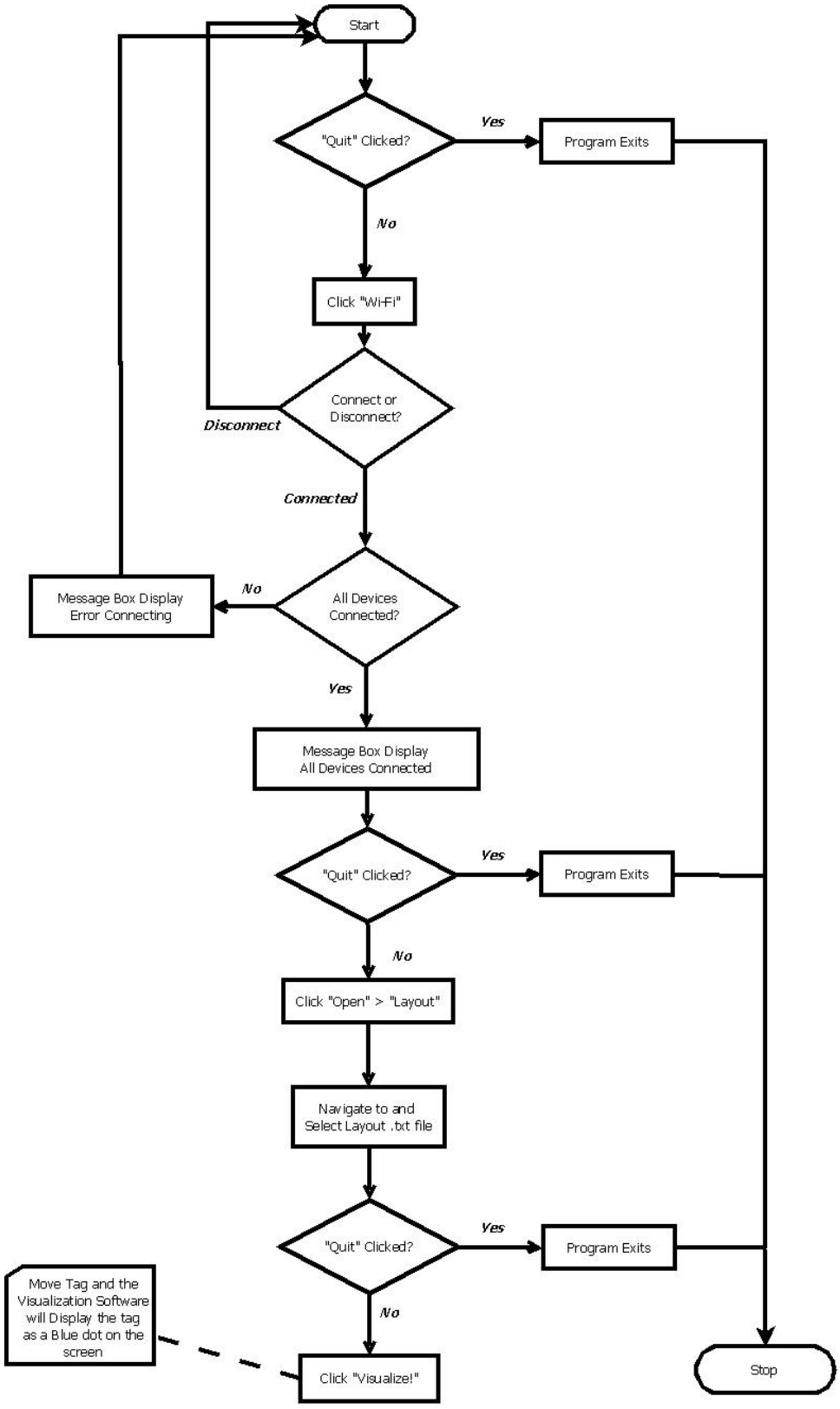


Figure 54: Flow Chart Illustrating how to Operate RTLS Visualization Software

9.0 RESULTS

The RTLS described in this thesis is capable of locating one tag in real-time for the Beta-Test II demonstrations. The future revisions in Section 11.0 discuss reasons for this and what will need to be done to allow the system to locate many tags in real-time. The accuracy of the system presented in this thesis can have at best 2 inches of resolution. This resolution is not uniform across the entire virtual room designated by the receiver units. With the receiver units placed 65 inches apart in a cross shape as detailed in Section 8.6, a total of five positions between receiver units placed across from each other (65 inches apart) can be achieved.

To first illustrate the resolution of the system, Figure 55 details the measured distances between the threshold boundaries around a receiver unit. Figure 56 illustrates the host interface with a single receiver determining the location of a single transmitter as it moves further away from the receiver. The measured distances in Figure 55 correspond to numeric references that the receiver reports to the host computer interface, which correspond to the threshold boundary within which a tag resides, shown in Figure 57. The numeric references in Figure 57 manifest an X,Y coordinate in the GUI, which can be seen to change as the receiver unit updates the tag location as it moves across threshold boundaries, in Figure 55. A point to note about Figure 57 is that while a localization of '5' corresponds to up to 32 inches, the receivers can also report a value of '3' for a location number. The value of '3' corresponds to the tag being outside of the maximum thresholding capability of the receiver unit. The '5' and '3' boundaries are somewhat

blurred together in that an edge between a '5' and '3' threshold is vague. For the data presented in Appendix C, a location estimation of '5' or '3' corresponds to the same location estimate.

Using only one receiver unit, as detailed in Figure 55, Figure 56, and Figure 57 only provides a 1-dimensional location-view of the tag. Using more receiver units provides more frames of reference for the location estimate of a tag, which create a 2-dimensional location-view of the tag. Receiver units were placed in a room as shown in Figure 58 . The receiver units each have threshold boundaries as detailed in Figure 55 and Figure 58. The threshold boundaries, as illustrated here show that segments created by overlapping semicircles (threshold boundaries) from receiver units cannot be considered precise, as a tag can lie anywhere within this created segment, and furthermore, when no overlapping segments are created, the tag can lie anywhere within the area of the estimated location by the receiver unit, as seen in the shaded regions of Figure 57. As such, with the receiver units placed 65 inches apart, the concentric rings will for the most part not create segments, but the maximum threshold boundaries (represented as a '5' and a '3') of the receivers correspond to overlapping segments at the middle of the layout, as shown in Figure 58 .

Figure 58 also illustrates the notion that without overlapping boundaries, an arbitrary location in a threshold boundary must be assumed (the two locations closest to the receiver units), and with overlapping boundaries, a location within the created segment must be arbitrarily chosen (the middle location, equidistant from all receivers in the middle of the room). Additionally, Figure 59 shows the five possible locations between receivers across from each other, for a total of nine possible locations with the four receiver units.

Detailed and illustrated in Appendix C is the collection of data from RTLS receiver units by the host computer, along with the accompanying final location estimate in terms of an X, Y

coordinate (which corresponds to the region on the GUI to draw the new location of the tag). The color coding in Appendix C makes it easier to examine the collected data, which is a numeric value derived from the thresholding boundaries detailed in Figure 57, and the tag location on the room layout as a result of the collected data.

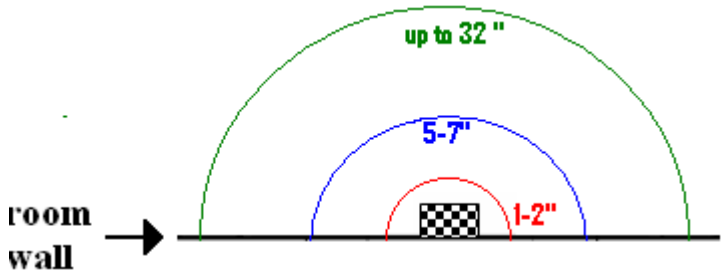


Figure 55: Threshold Boundaries of a Receiver Unit Presented in this Thesis

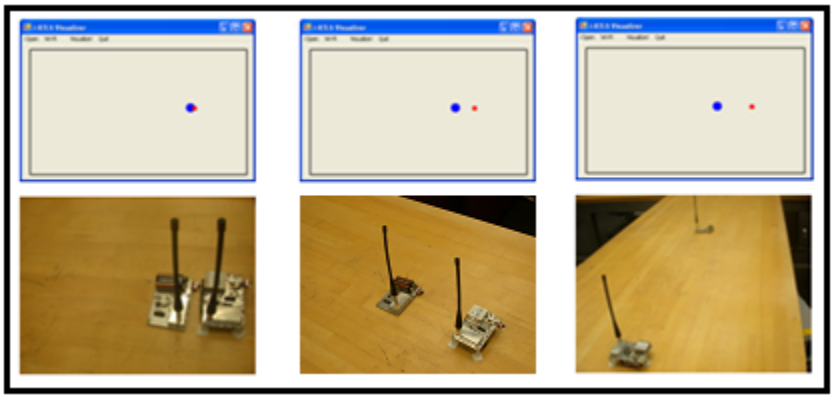


Figure 56: Single Receiver Unit (Small Dot) Localizing Tag (blue) Through Thresholds

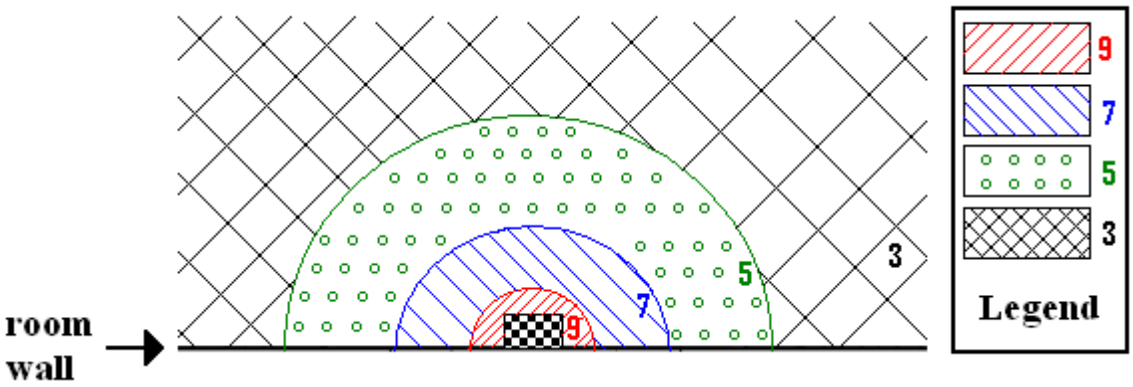


Figure 57: Numeric Values Reported by a Receiver Unit for a Threshold Boundary

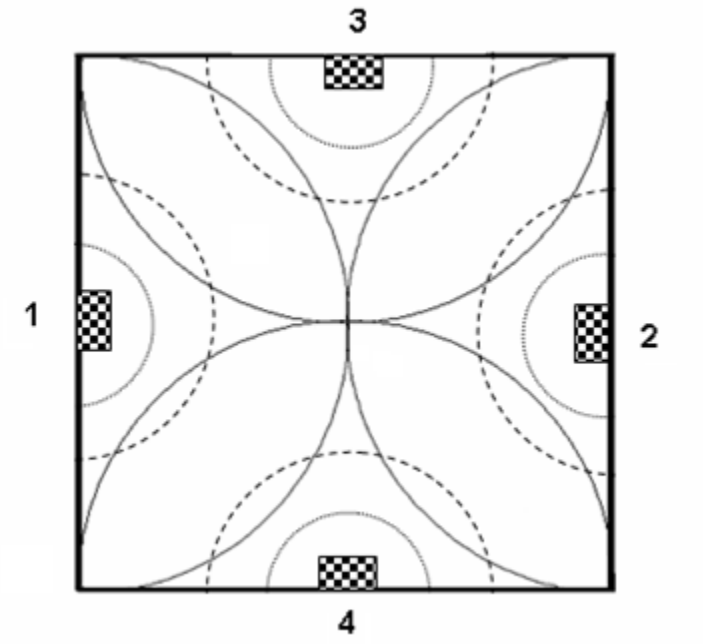


Figure 58: Receiver Units Illustrating Threshold Boundaries

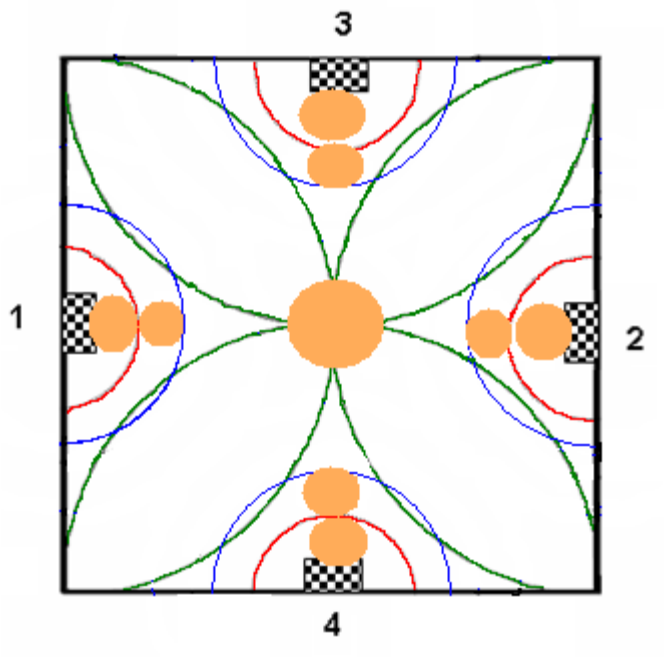


Figure 59: Receiver Units with All Possible Tag Locations (Large Circles)

10.0 CONCLUSIONS

The RTLS presented in this thesis is a viable step in the direction for meeting the goals and requirements of Section 2.1. The goals and requirements set out for the Beta-test II RTLS were met. Certain goals for the ultimate system are yet to be completely assessed. First, the location accuracy to a single room has been met. This is perhaps the most critical and has been done in the most critical environment, i.e. short distances. Second, the scalability to track thousands of tags is an open question that still remains for a larger study. The future work mentioned in Section 11.0 , specifically is dependent on the data rate. With a higher data rate, a BER could be assessed more quickly and thus reduce the time to determine a tag location as was required in the Beta-Test II prototypes. Third, the throughput of the system cannot be entirely assessed without scaling the system up to track many tags involving a much more expensive trial. Fourth, the location determination algorithm is certainly efficient and simple, but the BER portion of the method for location determination could be problematic for tracking greater numbers of tags if the data rate being used is too low. Finally, the fault tolerance of the system presented in this thesis could not be assessed because there were not nearly enough receiver units in the system to allow for some units to be disabled and still provide a still-relatively working prototype because this was a prototype. The fault tolerance was understood to be assessed when the system is to be implemented on a larger scale. If further development with regard to the

details presented in the Future Work section (Section 11.0) is pursued, then an RTLS utilizing the novel location determination method presented in this thesis can be expected to be a significant competitor in the RTLS market especially based on the resolution that has been obtained using this novel method of location determination.

11.0 FUTURE WORK

As mentioned in Section 8.6, each RTLS is placed 65” apart. This distance is dictated by the ability of the RTLS receiver unit to attenuate the signal that it is receiving, as mentioned in the Results (Section 9.0). So in order to increase the distance that each RTLS receiver unit can determine the location of a tag, one can incorporate more DSA's in series to increase the maximum amount of attenuation that can be added to the incoming signal to the receiver. With the addition of more hardware, more PCB real estate will be needed likely requiring a change in the size (namely length) of the PCB board-level shielding. Also, the DSA in this design operates in parallel mode using six bit select lines (one I/O pin from the microcontroller for each attenuation bit select line on the DSA). When using more than one DSA, this can require an unruly amount of I/O pins on the microcontroller. One solution to this problem is to use the serial select line on each DSA effectively reducing the number of I/O lines from the microcontroller to one per DSA for selecting an amount of attenuation. Doing this will also require creating a software serial transmitter routine to transmit serial data on each line to a DSA because undoubtedly there will not be enough UARTs on a microcontroller for controlling several DSAs.

The symbol rate employed in the RTLS presented in this thesis is 5 kHz. This symbol rate was selected because empirically it was noticed that a faster symbol rate, the greater the BER on the receiver side. This error was likely caused by the quality of the hardware being used

(transmitter and receiver), as the increase in BER for symbol rates greater than 5 kHz was observed in both an anechoic chamber and outside of an anechoic chamber indicating that multipath interference was not the reason. Employing higher quality hardware (transmitter and receiver) would be expected to ameliorate this problem but will also come at the expense of raising the price of each unit.

APPENDIX A

RTLS WIPORT CONFIGURATION PROFILE

Appendix A details the configuration profile of a WiPort as mentioned in Section 8.5.1.1.2 . This profile was retrieved from the WiPort by accessing Setup Mode in serial mode with the WiPort plugged into the Evaluation Board. To access everything seen below, reference the WiPort User's Guide [34].

MAC address 00204AB30763
Software version V6.6.0.0 (080107)
Press Enter for Setup Mode

*** basic parameters
Hardware: Ethernet TPI, WLAN 802.11bg
Network mode: Wireless Only
IP addr 169.254.223.80, no gateway *set,netmask 255.255.0.0*
DNS Server not set

*** Security
SNMP is enabled
SNMP Community Name: public
Telnet Setup is enabled
TFTP Download is enabled
Port 77FEh is enabled
Web Server is enabled
Web Setup is enabled
ECHO is enabled
Enhanced Password is disabled
Port 77F0h is enabled

*** Channel 1
Baudrate 9600, I/F Mode 4C, Flow 00

Port 50220
Connect Mode : D5
Send '+++' in Modem Mode disabled
Show IP addr after 'RING' disabled
Auto increment source port disabled
Remote IP Adr: 169.254.1.100, **Port 50320**
Disconn Mode : 01
Flush Mode : 80
Pack Cntrl : 30
SendChars : 6E 40

*** Channel 2
Baudrate 9600, I/F Mode 4C, Flow 00
Port 10002
Connect Mode : C0
Send '+++' in Modem Mode enabled
Show IP addr after 'RING' enabled
Auto increment source port disabled
Remote IP Adr: --- none ---, Port 00000
Disconn Mode : 00
Flush Mode : 00

*** Expert
TCP Keepalive : 45s
ARP cache timeout: 600s
CPU performance: Regular
Monitor Mode @ bootup : enabled
HTTP Port Number : 80
SMTP Port Number : 25
MTU Size: 1400
Alternate MAC: disabled
Ethernet connection type: auto-negotiate

*** E-mail
Mail server: 0.0.0.0
Unit :
Domain :
Recipient 1:
Recipient 2:

- Trigger 1
Serial trigger input: disabled
Channel: 1
Match: 00,00
Trigger input1: X
Trigger input2: X
Trigger input3: X

Message :
Priority: L
Min. notification interval: 1 s
Re-notification interval : 0 s

- Trigger 2
Serial trigger input: disabled

Channel: 1
Match: 00,00
Trigger input1: X
Trigger input2: X
Trigger input3: X

Message :
Priority: L
Min. notification interval: 1 s
Re-notification interval : 0 s

- Trigger 3
Serial trigger input: disabled
Channel: 1
Match: 00,00
Trigger input1: X
Trigger input2: X
Trigger input3: X

Message :
Priority: L
Min. notification interval: 1 s
Re-notification interval : 0 s

*** WLAN
WLAN: enabled
Topology: Infrastructure
Network name: LinksysTrf

Country: US
Security suite: none
TX Data rate: 11 Mbps auto fallback
Power management: enabled
Soft AP Roaming: disabled

APPENDIX B

RTLS VIRTUAL ROOM LAYOUT FILE

Appendix B contains an example virtual room layout file as detailed in Section 8.5.1.1.3. This file was used in the RTLS detailed in this thesis placing each receiver unit in a cross pattern 65 inches apart from one another. The room layout file below should be copied to a text (.txt) file for loading into the RTLS Visualization software:

```
0 31 28
1 1 1
2 30 1
2 30 27
2 1 27
3 1 1
4 2 8
4 10 8
4 6 2
4 6 14
```

APPENDIX C

COLLECTED LOCATION DATA OF A TAG FROM RTLS RECEIVER UNITS

Appendix C presents data collected from the RTLS receiver units as they determine the location of a tag in Table 11 (Receiver Unit number, from the table, is illustrated in Figure 60 as is the "X,Y Coordinate on GUI," which refers to the distance X [from left] and Y [from top] from the borders of the screen GUI). Table 11 is a result of a user moving a tag around the room layout bounded by the receiver units. Because the transmitter can be moved by a user in any direction at any time, the important point to notice in all of the information contained in the table is how the numeric threshold representations for location estimates by each receiver unit correspond to the threshold boundaries depicted in Figure 60).

Figure 60 and Figure 61 below illustrates the RTLS receiver units with concentric semicircles emanating from each receiver unit. Each concentric semicircle indicates a boundary threshold; more specifically, Figure 61 shows the numbered equivalent of a boundary that the receiver units report to the host computer when a tag resides in the area covered by these numbered boundaries. The shaded circles in Figure 60 show the possible X, Y coordinates that

the collected location estimates from each receiver unit can correspond to. Examining Table 11, it can be seen that the "X, Y Coordinate on GUI" has been shaded to match the shaded circle that the coordinate corresponds to in Figure 60. As mentioned in the Results (Section 9.0), a location estimate of '5' or '3' can be deduced to be the same so that when localizing a tag, a '3' reported as a location signifies that the transmitter is most likely out of the bounds of the thresholding capabilities of the receiver unit, or that the tag resides on the relatively large ambiguous edge between the '5' and '3' thresholds.

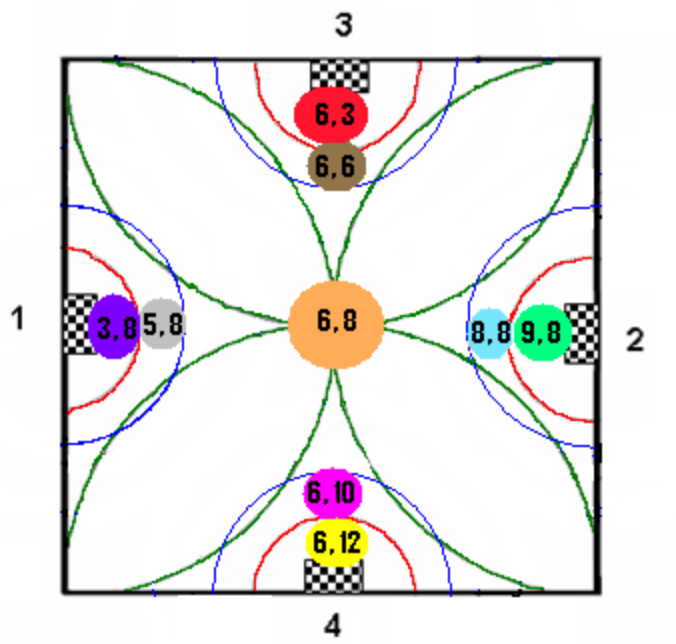


Figure 60: Possible Location Estimates with Receivers Placed 65" Apart in a Cross

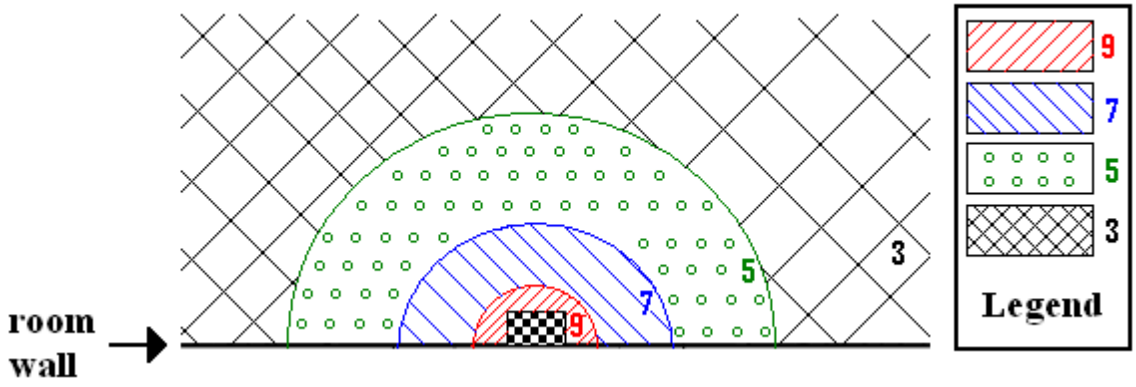


Figure 61: Numeric Values Reported by a Receiver Unit for a Threshold Boundary

Table 11: Location Estimate from Data Collected by Each Receiver Unit (Enumerated)

Receiver Unit #				X,Y Coordinate on GUI	
1	2	3	4	X	Y
3	5	5	5	6	8
3	5	5	5	6	8
3	5	5	5	6	8
3	5	3	5	6	8
3	5	3	5	6	8
3	5	3	5	6	8
3	7	3	5	8	8
3	7	3	3	8	8
3	9	3	3	9	8
3	9	3	3	9	8
3	9	3	3	9	8
3	9	3	3	9	8
3	7	3	5	8	8
3	7	3	5	8	8
3	5	3	5	6	8
3	5	3	5	6	8
3	5	3	7	6	10
3	5	3	7	6	10
3	5	3	7	6	10
3	5	3	7	6	10
3	5	3	7	6	10
3	5	3	7	6	10
3	5	3	7	6	10
3	5	3	7	6	10
3	5	3	7	6	10
3	5	3	7	6	10
3	5	3	9	6	12
3	3	3	9	6	12
3	3	3	9	6	12
3	3	3	9	6	12
3	3	3	7	6	10
3	3	3	7	6	10
3	3	3	5	6	8
3	3	5	5	6	8
3	3	5	5	6	8

Table 11 (continued)

3	3	5	5	6	8
3	3	5	5	6	8
3	3	5	5	6	8
3	3	5	5	6	8
3	3	3	5	6	8
3	5	3	5	6	8
3	3	3	3	6	8
5	3	3	5	6	8
5	3	3	5	6	8
3	3	3	3	6	8
9	3	3	3	3	8
9	3	3	3	3	8
9	3	3	3	3	8
9	3	3	3	3	8
5	3	3	3	6	8
5	3	3	3	6	8
5	5	3	5	6	8
5	3	3	3	6	8
5	3	3	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	9	3	6	3
5	3	9	3	6	3
5	3	9	3	6	3
5	3	9	5	6	3
5	3	7	5	6	6

Table 11 (continued)

5	3	7	3	6	6
5	3	7	3	6	6
5	3	5	3	6	8
5	3	3	5	6	8
5	3	5	3	6	8
5	3	3	3	6	8
5	3	3	3	6	8
5	3	3	5	6	8
5	3	7	5	6	6
5	3	7	3	6	6
5	3	9	3	6	3
5	3	9	3	6	3
5	3	9	3	6	3
5	3	9	5	6	3
5	3	5	3	6	8
5	3	3	3	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8

Table 11 (continued)

5	3	3	5	6	8
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	3	6	8
5	7	3	3	8	8
5	7	3	3	8	8
5	7	3	3	8	8
5	9	3	3	9	8
5	9	3	3	9	8
5	9	3	3	9	8
5	9	3	3	9	8
5	9	3	3	9	8
5	7	3	3	8	8
5	7	3	3	8	8
5	5	3	3	6	8
5	5	3	3	6	8
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	3	6	8
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	3	6	8
5	5	3	3	6	8
5	5	3	3	6	8
9	5	3	3	3	8
9	5	3	3	3	8
9	5	3	3	3	8
7	5	3	3	5	8
7	5	3	3	5	8
7	5	3	3	5	8
5	5	3	3	6	8
5	5	3	3	6	8
5	5	3	5	6	8

Table 11 (continued)

5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	7	6	10
5	3	3	7	6	10
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	5	6	8
5	7	3	5	8	8
5	7	3	5	8	8
5	7	3	5	8	8
5	7	3	5	8	8
5	7	3	5	8	8
5	7	3	5	8	8
5	7	3	5	8	8
5	7	3	3	8	8
5	7	3	3	8	8
5	7	3	3	8	8
5	9	3	3	9	8
5	9	3	3	9	8
5	9	3	3	9	8
5	9	3	3	9	8
5	9	3	3	9	8
5	7	3	3	8	8
5	7	3	3	8	8
5	5	3	5	6	8
5	5	3	5	6	8
5	5	3	3	6	8

Table 11 (continued)

5	5	3	3	6	8
5	5	7	5	6	6
5	5	7	5	6	6
5	5	7	5	6	6
5	5	7	5	6	6
5	5	7	5	6	6
5	5	7	5	6	6
5	5	7	5	6	6
5	5	7	3	6	6
5	5	7	5	6	6
5	5	9	3	6	3
5	5	9	3	6	3
5	5	9	3	6	3
5	5	9	3	6	3
5	5	9	3	6	3
5	5	9	3	6	3
5	5	7	3	6	6
5	5	5	3	6	8
5	3	3	3	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	9	6	12

Table 11 (continued)

5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	9	6	12
5	3	3	7	6	10
5	3	3	7	6	10
5	3	3	5	6	8
5	5	3	3	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	3	6	8
5	5	3	3	6	8
5	5	3	3	6	8
5	5	3	3	6	8
5	5	3	3	6	8
5	5	3	3	6	8
5	3	5	3	6	8
5	3	5	3	6	8
5	3	7	3	6	6
5	3	7	3	6	6
5	3	9	3	6	3
5	3	9	3	6	3
5	3	9	3	6	3
5	3	9	3	6	3
5	3	7	3	6	6
5	3	5	3	6	8
5	3	5	3	6	8
5	3	5	5	6	8
5	3	5	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8
5	3	3	5	6	8

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