NANOELECTRONICS IN OXIDES AND SEMICONDUCTORS

by

Guanglei Cheng

B.S. University of Science and Technology of China, 2003

M.S. University of Pittsburgh, 2005

Submitted to the Graduate Faculty of

the Arts and Sciences in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

University of Pittsburgh

2011

UNIVERSITY OF PITTSBURGH

DEPARTMENT OF PHYSICS AND ASTRONOMY

This dissertation was presented

by

Guanglei Cheng

It was defended on

April 18, 2011

and approved by

Jeremy Levy, Professor, Physics and Astronomy, Arts and Sciences

Xiaolun Wu, Professor, Physics and Astronomy, Arts and Sciences

Hrvoje Petek, Professor, Physics and Astronomy, Arts and Sciences

Scott Mao, Professor, Mechanical Engineering and Materials Science, Arts and Sciences

Robert Griffiths, Professor of Physics, Carnegie Mellon University

Dissertation Advisor: Jeremy Levy, Professor, Physics and Astronomy, Arts and Sciences

NANOELECTRONICS IN OXIDES AND SEMICONDUCTORS

Guanglei Cheng, PhD

University of Pittsburgh, 2011

The success of silicon industry lies on three major properties of silicon, an easily formed oxide layer to allow field effect operation, tunability of carrier density and high device scalability. All these features exist in oxides, together with some novel properties such as ferroelectricity, magnetic effects and metal-insulator transition. With the recent development in material growth method including molecular beam epitaxy (MBE), pulsed laser deposition (PLD) and reflection high energy electron diffraction (REED), atomically engineered oxide interfaces become available, thus opening the door to the novel oxide nanoelectronics. In this dissertation we create and study nanoelectronics in oxides, semiconductors and hybrid of these two. We used a conductive atomic force microscope tip to write single electron transistors in the 3-unit-cell-$LaAlO_3/SrTiO_3$ heterostructure and observed ferroelectric tunneling behaviors. We also fabricated ferroelectric field transistors directly on silicon using strained $SrTiO_3$ ferroelectric film and further confirmed the ferroelectric properties of this device. Meanwhile, we developed an ultrasensitive microwave capacitance sensor to study the electronic properties of self-assembled quantum dots and the switching mechanism of memristive devices. The integration of this sensor to a home made atomic force microscope provides an important tool to study the dielectric properties at nanoscale.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

PREFACE

I have enjoyed nearly every moment of my life here in Pittsburgh, not only because Pittsburgh is ranked as “the most livable city in US”, but also most importantly the people I’m working with.

I gratefully thank my advisor Jeremy Levy. Without his support, guidance, patience, hand-by-hand help and academic intuition I would not have been able to accomplish this dissertation. It is a great fun working with current labmates Patric Irvin, Cheng Cen, Dongyue Yang, Yanjun Ma, Feng Bi, Vanita Srinivasa and Mengchen Huang. Thanks to the easy lab environment, we help each other and improve together. Also many thanks to formal members Hongzhou Ma, Peti Fodor and Daniela Bogorin, they help me a lot with their expertise and warm hearts.

I had great time with the talented guys at HP labs memristor device group. Special thanks to Gilberto Medeiros-Ribeiro, without him I would not have the opportunity for the HP labs experience and accomplish my project.

My Ph.D. committee is a great collection of distinguised professors, they guided me along the proper path using their professional suggestions and care.

Finally I want to thank my family, they have been always supportive and patient.

1.0 INTRODUCTION

Compared to conventional semiconductor silicon or compounds of III-V elements in the periodic table, transition metal oxides exhibit a broad range of novel functionalities such as superconductivity, piezoelectricity and ferroelectricity, high dielectric permittivity, colossal magnetoresistance, ferromagnetism and metal-insulator transitions. These functionalities enable novel device integration of oxide and semiconductor, or the emerging of oxide electronics, an even more ambitious field. With Moore's law foreseeing the scaling limit of conventional electronics, even the silicon industry is trying to find an alternative material system. Motivated by these points, this dissertation studies nanoelectronic devices made of semiconductor, oxides and the hybrid of semiconductor and oxides.

In the following subsections, I will cover some basic physical concepts that are essential to this dissertation.

1.1 QUANTUM DOTS

A quantum dot (QD) is a semiconductor nanostructure in which the electrons are spatially confined in 3 dimensions(*1*, *2*). In other words, the QD is a zero-dimensional system in terms of electron freedom. When then size of a QD is comparable to electron wavelength, the QD shows discrete energy levels similar to that of a hydrogen atom. It is some times referred to as an

"artificial atom". For an array of quantum dots, they can also from an artificial two-dimensional crystal.

Figure 1.1 shows the density of states (DOS) at systems with different dimensions based on basic quantum mechanical calculations. For a 3 dimensional system the density of states *g(E)* for a free electron is given by

$$g(E) = \frac{a^3}{2\pi^2}\left(\frac{2m^*}{\hbar}\right)^{3/2}\sqrt{E} \tag{1.1}$$

where m^* is the effective electron mass, a is the lattice constant of a cubic lattice and $\hbar$ is the reduced Planck constant. And for 2 dimensional electron gas, the DOS is

$$g(E) = \frac{a^2 m^*}{\pi\hbar^2} \tag{1.2}$$

which is not dependent on the energy. For 1 dimensional system like quantum wires, the DOS is

$$g(E) = \frac{a}{\pi}\sqrt{\frac{2m^*}{h^2}}\frac{1}{\sqrt{E}} \tag{1.3}$$

For a zero dimensional system like a quantum dot, the energy spectrum is discrete

$$g(E) = \frac{2}{a^3}\delta(E - E_n) \tag{1.4}$$

Numerous methods are used to confine electrons in 3 dimensions. For example, (CdSe)ZnS core-shell quantum dots buries the CdSe core in a large band gap semiconductor ZnS. Lateral quantum dots confine electrons using depletion gates above 2DEG using lithography techniques. Self-assembled quantum dots (SAQD) are formed by island nucleation for a material grown on a lattice-mismatched substrate by molecular beam epitaxy (MBE). In this dissertation, we study the SAQDs by looking at the capacitance spectroscopy, which reflects the spin information in the SAQDs for quantum information processing.

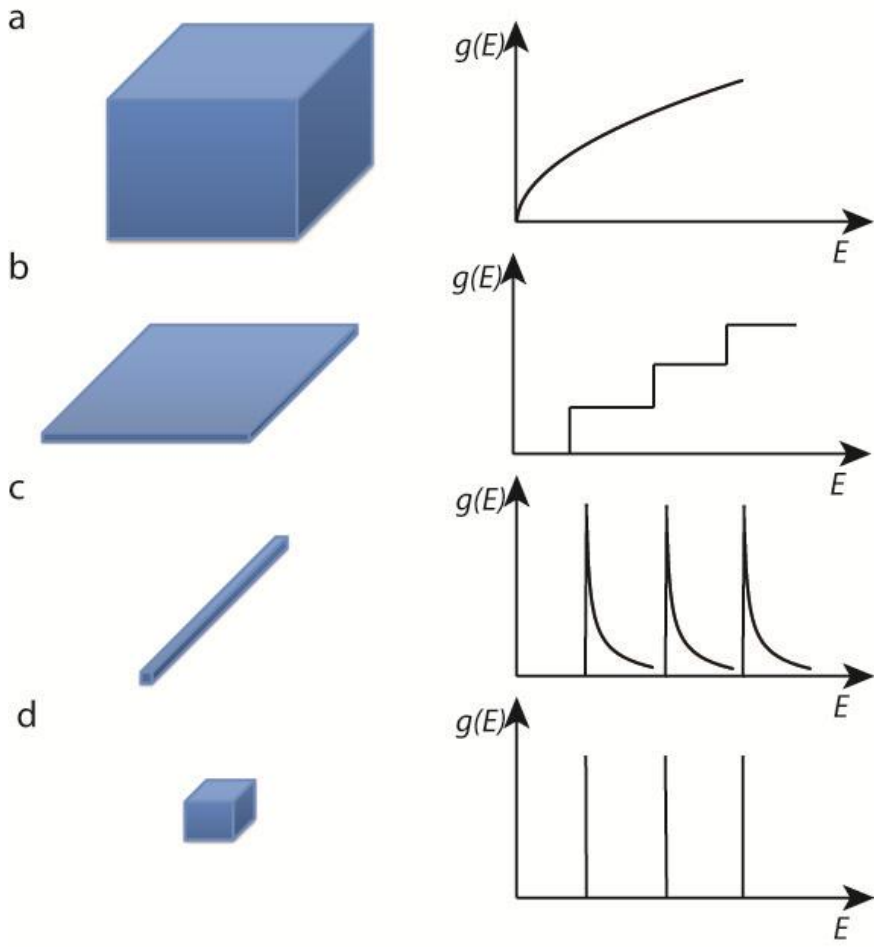

Figure 1.1 Densities of states versus energy at different dimensions. (a)Three dimensions, (b) two dimensions, (c) one dimension, (d) zero dimension.

1.2 MICROWAVE TRANSMISSION LINE

In this dissertation, one important technique that is developed and advanced is microwave capacitance sensing. This capacitance sensor monitors the resonance frequency shifts of a microstrip resonator perturbed by a capacitor attached to it. Here I will briefly review the transmission line theory that forms the basis of this sensor.

1.2.1 Transmission line

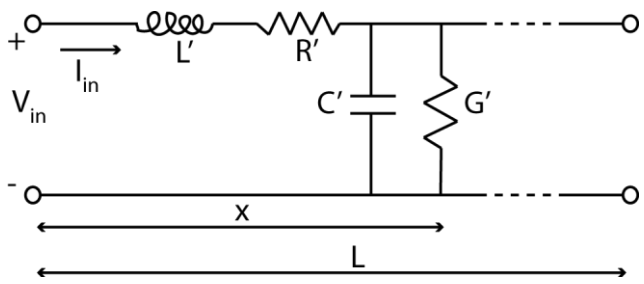

Figure 1.2 Transmission line lumped model

A transmission line is a medium that guides electromagnetic waves. A simple one-dimensional transmission line can be modeled as a composition of distributed lumped elements, as shown in Fig. 1.2. In this model, the transmission line is divided into infinite sections that have length Δx and total length L. Each section has L', R', C' and G' representing inductance per length, resistance per length, capacitance per length and conductance per length respectively. From basic circuit theory, we have

$$\frac{\partial i}{\partial x} = -vG' - \frac{\partial v}{\partial t}C' \tag{1.1}$$

$$\frac{\partial v}{\partial x} = -iR' - \frac{\partial i_{in}}{\partial t}L' \tag{1.2}$$

where i and v are current and voltage in each section. These two equations are often referred as *Telegrapher's Equations*. Differentiating the equations with t and x we get

$$\frac{\partial^2 v}{\partial x^2} = -\frac{R'\partial i}{\partial x} - \frac{L'\partial^2 i}{\partial x \partial t} \tag{1.3}$$

$$\frac{\partial^2 v}{\partial x\,\partial t} = -\frac{R'\partial i}{\partial t} - \frac{L'\partial^2 i}{\partial t^2} \tag{1.4}$$

$$\frac{\partial^2 i}{\partial x\,\partial t} = -\frac{G'\partial v}{\partial t} - \frac{C'\partial^2 v}{\partial t^2} \tag{1.5}$$

$$\frac{\partial^2 i}{\partial x^2} = -\frac{G'\partial v}{\partial t} - \frac{C'\partial^2 v}{\partial t\,\partial x} \tag{1.6}$$

Substituting (1.1) and (1.2) to (1.3), (1.4), (1.5) and (1.6) we have

$$\frac{\partial^2 v}{\partial x^2} = v(R'G') + \frac{\partial v}{\partial t}(R'C' + L'G') + \frac{\partial^2 v}{\partial t^2}(L'C') \tag{1.7}$$

$$\frac{\partial^2 i}{\partial x^2} = i(G'R') + \frac{\partial i}{\partial t}(L'G' + C'R') + \frac{\partial^2 i}{\partial t^2}(L'C') \tag{1.8}$$

The above second-order differential equations have universal solutions with $v(x,t) = v'(x)e^{j\omega t}, i(x,t) = i'(x)e^{j\omega t}$. By substituting these forms to the above equations we get,

$$\frac{\partial^2 v}{\partial^2 x} = v(x,t)[(R' + j\omega L')(G + j\omega C')] \tag{1.9}$$

The solution to (1.9) has form

$$v(x,t) = Ae^{-\gamma x}e^{-j\omega t} + Be^{\gamma x}e^{-j\omega t} \tag{1.10}$$

where the *propagation constant* $\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')}$. It is also written in a complex form $\gamma = \alpha + j\beta$ with α the *attenuation constant* and β the *phase constant*. This solution essentially contains two waves propagating in two opposite directions (+*x*/-*x*). Similarly we have

$$i(x,t) = \frac{-\gamma Ae^{-\gamma x}e^{-j\omega t} + \gamma Be^{\gamma x}e^{-j\omega t}}{(R' + j\omega L')} \tag{1.11}$$

And the *characteristic impedance* Z_0 is defined as the ratio of the voltage and current of a single wave propagating in one direction

$$Z_0 = \frac{v^+(x,t)}{i^+(x,t)} = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \tag{1.12}$$

For a lossless transmission line *R'=G'=0,* so that $Z_0 = \sqrt{L'/C'}$.

1.2.2 Microstrip transmission line

The microstrip is a type of electric transmission line that consists of an upper conductor strip and a ground plane with a dielectric in between. Fig. 1.3 shows the evolution from coaxial transmission system. First the coaxial line in (a) is deformed to a rectangle shape (b), and then

the top conductor is shrunk to a strip (c) while most of the fields are confined between two conductors. Finally the dielectric material with dielectric constant ε is introduced. Due to the inhomogeneity of dielectric medium (air versus dielectric), the effective dielectric constant ε_{eff} or effective microstrip width w_{eff} is often used to describe the characteristics of a microstrip. Analytical expression of characteristic impedance is hard to reach due to this inhomogeneity, an empirical expression from Wheeler(*3*) is often used.

$$Z_m = \frac{Z_0}{2\pi\sqrt{2(1+\epsilon_r)}} \ln\left(1 + \frac{4h}{w_{eff}}\left(\frac{14+\frac{8}{\epsilon_r}}{11}\frac{4h}{w_{eff}} + \sqrt{\left(\frac{14+\frac{8}{\epsilon_r}}{11}\frac{4h}{w_{eff}}\right)^2 + \pi^2\frac{1+\frac{1}{\epsilon_r}}{2}}\right)\right) \qquad (1.13)$$

where Z_0 is the characteristic impedance in air.

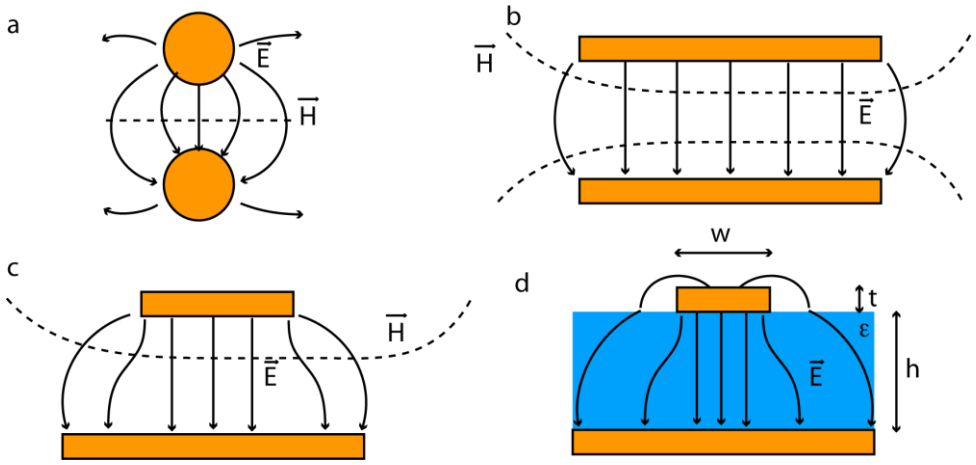

Figure 1.3 Evolution of microstrip transmission line. (Adapted from Ref. (*4*))

1.2.3 Transmission line terminated with a load

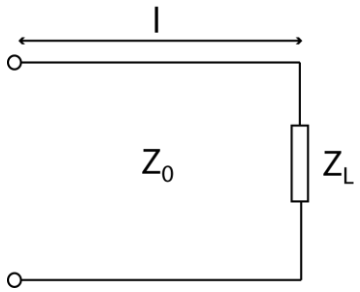

Figure 1.4 Transmission line terminated with a load

The transmission line is often terminated with a load, which perturbs the waves in the transmission line. Writing the solution to the telegrapher's equations with hyperbolic functions, the *generalized impedance* Z_{in} for a transmission with a load Z_L (as shown in Fig. 1.4) is

$$Z_{in} = Z_0\left(\frac{Z_R \cosh \gamma l + Z_0 \sinh \gamma l}{Z_0 \cosh \gamma l + Z_R \sinh \gamma l}\right) \tag{1.14}$$

For a lossless transmission line, attenuation constant α=0, $\gamma = j\beta$ and $\beta = 2\pi/\lambda$.

$$Z_{in} = Z_0\left(\frac{Z_R \cos \beta l + jZ_0 \sin \beta l}{Z_0 \cos \beta l + jZ_R \sin \beta l}\right) \tag{1.15}$$

1.2.4 Scattering parameters

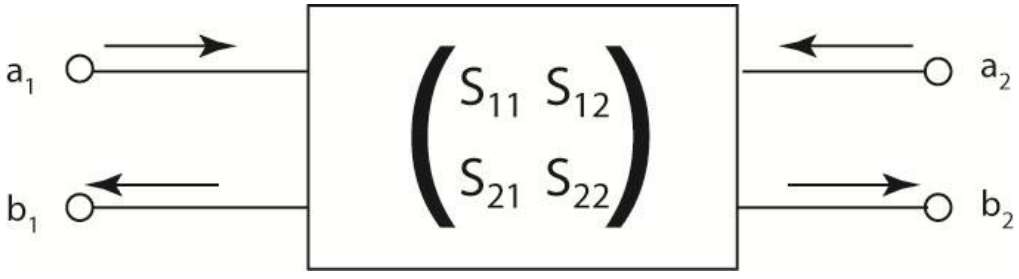

Figure 1.5 2-port network

The scattering parameters (S-parameters) describe the electric behavior of a linear electric network when a signal passes through. It is a transfer matrix that correlates incoming waves and outgoing waves, namely for a 2-port network

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{11} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{1.16}$$

where $\begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$ and $\begin{pmatrix} b_1 \\ b_2 \end{pmatrix}$ are incoming and outgoing waves, and $\begin{pmatrix} S_{11} & S_{12} \\ S_{11} & S_{22} \end{pmatrix}$ are S-parameters.

To be specific, the S_{11} is the input signal reflection coefficient; S_{12} is the reverse gain; S_{21} is the forward gain and S_{12} is the signal reflection coefficient at the output port.

1.3 FERROELECTRICITY

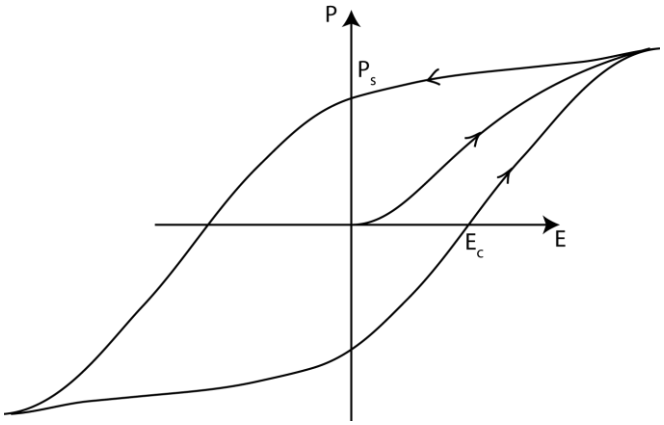

Figure 1.6 P-E loop

Ferroelectricity is a property for materials that have a spontaneous or permanent polarization that can be hysterically reversed by external electric field(*5*). It was first observed by Anderson and Cady in Rochelle salt in 1918(*6, 7*). Later Busch and Scherrer(*8*) observed ferroelectricity in potassium dihydrogen phosphate (KDP) and then extended to all tetragonal

dihydrogen phosphate. Another important discovery of ferroelectricity is among perovskite oxides including $BeTiO_3$(*9, 10*), $PbTiO_3$(*11*), $KTaO_3$(*12*), and $NaVO_3$(*12*). Today, over 700 materials are found ferroelectric and many novel applications are made.

Analogous to ferromagnetism that shows hysteresis behavior under external magnetic field, the ferroelectric polarization is reserved when the external electric field switches direction until it reaches a value E_c that is called *coercive field*. In ordinary dielectric materials, the polarization $\vec{P}$ induced by external field has a simple linear relation with electric field $\vec{E}$ by giving $\vec{P} = \varepsilon_0 \chi \vec{E}$, where ε_0 is the dielectric constant of air and χ is the electric susceptibility of the dielectric. The ferroelectric material, however, does not have a simple analytic relation, as shown in Fig. 1.6.

1.3.1 Origin of ferroelectricity

The origin of ferroelectricity is much more complicated than ferromagnetism. It is widely viewed by a net dipole moment caused by the displacement of atoms under interatomic forces. Under external field, the dipole moment of atoms aligns with it. And after the field is removed, the dipoles still keep the favored polarization, namely the *remnant polarization*. The ferroelectric behavior can be very different even among materials with similar crystalline structures. For example, oxides with perovskite structure all have ABO_3 crystal structure, but the chemically different atoms result in different long-range and short-range Coulomb forces, which stabilizes the atoms in different structural phase. Cohen calculated the electronic structures of $BeTiO_3$ and $PbTiO_3$, the well-known ferroelectric perovskite oxides, using all electron, full potential, linearized augmented plane-wave method(*13*). He revealed that the hybridization of titanium 3d states and oxygen 2p states play an important role in ferroelectricity. The $PbTiO_3$ is stabilized in a tetragonal phase by a large strain from hybridization of lead and oxygen states.

While the $BaTiO_3$ in rhombohedral structure that caused by ionic interaction between barium and oxygen atoms.

A ferroelectric material is often only ferroelectric under certain temperature called Curie temperature T_C, accompanied by a structural phase transition. Above the Curie temperature, the material is *paraelectric*. Multiple Curie temperature can co-exist for one material. For example, $BaTiO_3$ has 3 Curie temperatures, 393 K, 278 K and 183 K. Accompanied phase transitions are cubic to tetragonal at 393 K, tetragonal to orthorhombic at 278 K and orthorhombic to rhombohedral at 183 K.

Beyond bulk ferroelectricity, some thin film materials show ferroelectricity under external strains, which modifies the interatomic forces and produce a net dipole moment. One striking example is $SrTiO_3$ which is not ferroelectric in the bulk, however it shows ferroelectricity when grown on different substrates with epitaxial strain(*14-16*). In this dissertation, I will cover the ferroelectricity of strained $SrTiO_3$ under various circumstances.

1.3.2 Applications

Ferroelectrcity is such a novel property that it finds use in many aspects of device applications(*17*). Ferroelectric random access memories (FeRAM) use the non-volatile remnant polarization to regulate the current floating through the device (ferroelectric field effect transistor) or keep the non-volatile voltage even the external power is shut off (ferroelectric capacitor), making "instant-on" computers possible. The capacitance of a ferroelectric capacitor is tunable under external field by tuning the dielectric constant. The value of the dielectric constant is also considerably huge close to the phase transition compared to regular capacitors, which made it a

smaller size in application. All ferroelectrics are also pyroelectric, and all pyroelectrics are piezoelectric, which provides possibilities for sensor applications.

2.0 EXPERIMENTAL METHODS

In this chapter, I will introduce some important experimental techniques that are important in nanoelectronics. These techniques involve basic electronic characterization of nanoscale devices, nanoscale imaging of topographic and dielectric properties of sample surface as well as sensing ultra small capacitance at microwave frequencies.

2.1 MICROWAVE CAPACITANCE SENSING

In 1964, Radio Corporation of America (RCA) introduced a video play back system called Capacitance Electronic Disc (CED) VideoDisc (Fig. 2.1a). In this system, information (0s and 1s) is encoded in hills and valleys in a plastic disc (Fig.2.1b). A metal stylus moves above the disc and senses the capacitance changes between the stylus and disc. To sense the capacitance change, the stylus is attached to a microwave resonator excited at an off-resonance frequency 915 MHz, as shown in Fig. 2.1c. The resonance frequency of the resonator is perturbed by the capacitance between the stylus to the disc(*18, 19*). The transmitted microwave power is finally detected by a microwave peak detector, converting power to voltage. A small capacitance change will cause the resonance frequency to shift, as well as causing the output voltage to change (Fig. 2.1d). The operating frequency is chosen at the frequency with maximum voltage response, normally at the largest slope of the resonance curve. Owing to the

high operating frequency, the sensitivity of this capacitance sensor is extremely high, typically 10^{-16} ~10^{-19} $F/\sqrt{Hz}$ for RCA sensors.

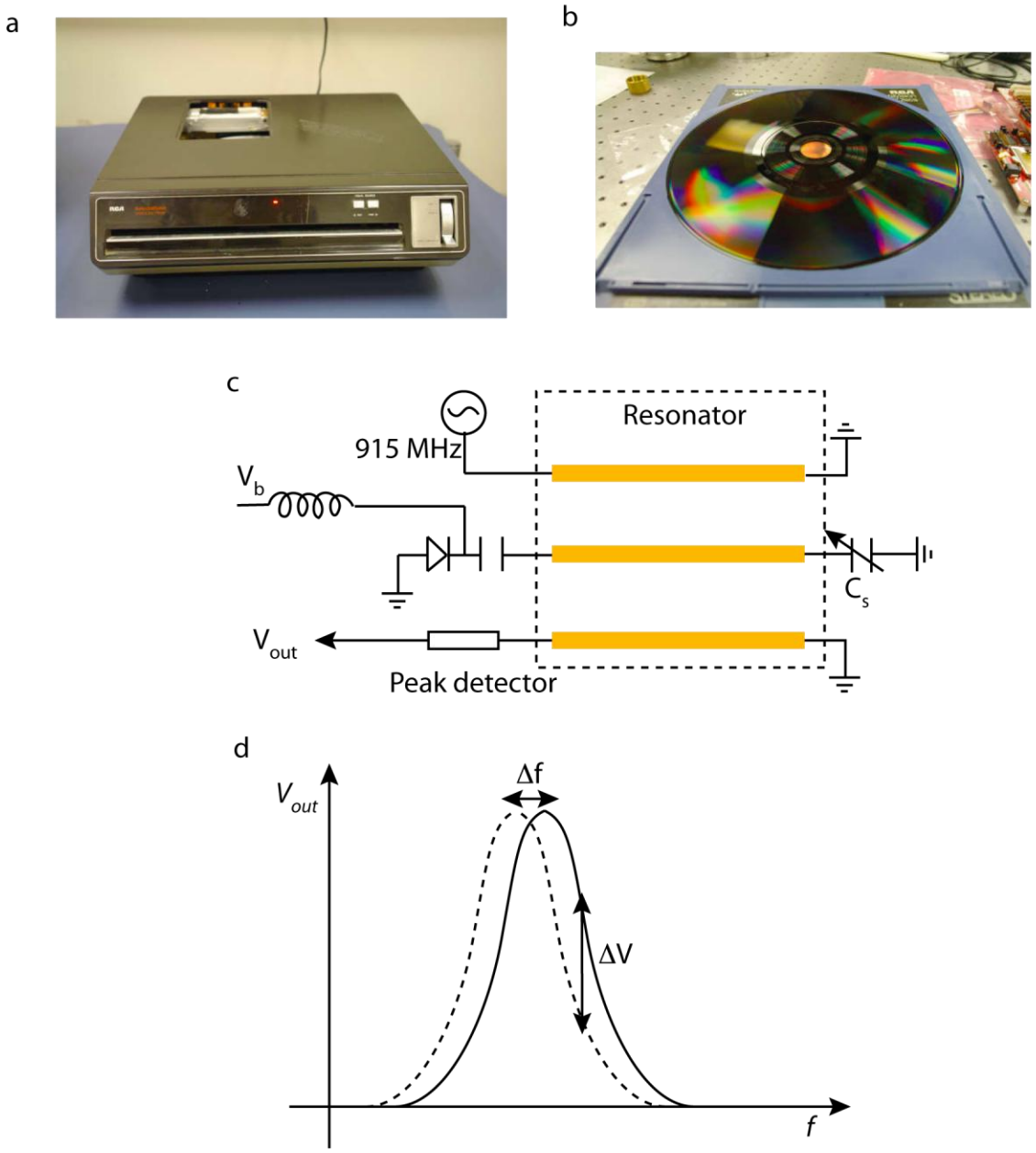

Figure 2.1 Working principle for RCA's CED microwave capacitance sensing. (a) Photograph of RCA CED play back system. (b) Photograph of CED disc. (c) Detection circuit. (d) Capacitance shift causes resonance frequency shift, resulting an ultimate voltage change in the peak detector output.

In this dissertation work, we developed an improved version of RCA sensor to measure the ultra small capacitance of quantum dots and memristive devices. We also integrated this sensor to an AFM for scanning capacitance imaging, as will be introduced in Chapter 5 and Appendix A.

2.2 LOCK-IN DETECTION

In experiment, the real physical signal is often overwhelmed by all kinds of noises, e.g. 60 Hz power line noise, Johnson noises coming from the resistors due to thermal fluctuations, shot noise due to statistical fluctuations of charge carriers and acoustic noise coming from vibration sources etc. The signal to noise ratio can be as small as 10^{-9}, i.e. measuring 1 nV in 1V noise. Since the noises are either random or have specific frequencies, one smart way is to "dye" (modulate) the signal with certain frequency that is away from any noise frequencies, then detect the signal only at that modulated frequency (reference frequency), effectively filtering out the noises. This is the idea of lock-in detection and a lock-in amplifier is used to detect small AC signal. The signal is often modulated by applying a small AC voltage to the source. In other experiments like optical experiment, the laser beam can be chopped so that the light intensity is modulated, resulting a modulated AC signal in the optical detector.

Figure 2.2a shows a simplified schematic of a lock-in amplifier. A small AC signal $\tilde{V} = V_0 \cos(\omega t + \theta_{sig})$ passes through *x* and *y* channel mixers and get mixed with the reference signal with same frequency $\tilde{V}_{ref} = V_{ref} \cos(\omega t + \theta_{ref})$. The output from the *x* channel after the mixer turns into

$$\tilde{V} \otimes \tilde{V}_{ref} = V_0 V_{ref} \cos(\omega t + \theta_{sig}) \cos(\omega t + \theta_{ref})$$

$$= \frac{1}{2} V_0 V_{ref} \cos(\theta_{ref} - \theta_{sig}) + \frac{1}{2} V_0 V_{ref} \cos(2\omega t + \theta_{ref} + \theta_{sig}) \quad (2.1)$$

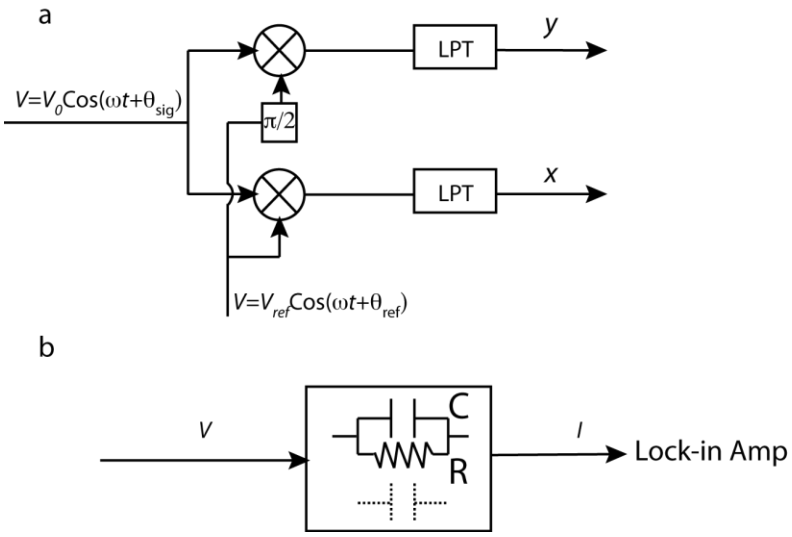

Figure 2.2 Schematic of a lock-in amplifier (a) and measurement setup (b).

After passing through a low pass filter, the second term with 2ω frequency is filtered out and only the DC term $\frac{1}{2} V_0 V_{ref} \cos(\theta_{ref} - \theta_{sig})$ is reserved. Finally the signal is subjected to an amplifier to compensate the term $\frac{1}{2} V_{ref}$ so that the x channel reads

$$X = V_0 \cos(\theta_{ref} - \theta_{sig}) \quad (2.2)$$

Similarly the y channel reads

$$Y = V_0 \sin(\theta_{ref} - \theta_{sig}) \quad (2.3)$$

since the phase of the reference signal in the y channel is shifted by 90 °. Noises with different frequencies will be also filtered out as far as the cut off frequency of the low pass filter is smaller than the difference between noise frequency and reference frequency.

This lock-in technique can be used to measure the capacitance of quantum dots, which can be modeled as a capacitor in parallel with a resistor (Fig. 2.2b). Prior to the measurement, a test capacitor C_0 (dashed object in Fig. 2.2)) is used to adjust the phase $\theta_{ref} = \theta_{sig} + \pi/2$ such that the entire capacitive signal is in *x* channel and resistive signal in *y* channel. This can be seen by calculating the current that is the inputted to the lock-in amplifier

$$I = V_0 \omega C_0 \cos(\omega t + \theta_{sig} + \frac{\pi}{2}) \tag{2.4}$$

After mix with the reference signal $V_{ref}\cos(\omega t + \theta_{ref})$, the *x* channel reads $V_0\omega C_0 \cos(\theta_{sig} + \frac{\pi}{2} - \theta_{ref})$ and *y* channel reads $V_0\omega C_0 \sin(\theta_{sig} + \frac{\pi}{2} - \theta_{ref})$. Setting $\theta_{ref} = \theta_{sig} + \pi/2$ will set *y* channel to zero and *x* channel contains the capacitance information.

Then replace the test capacitor with QD of complex impedance $\frac{R}{1+j\omega CR}$, and the current is

$$I = V_0 \omega C \cos\left(\omega t + \theta_{sig} + \frac{\pi}{2}\right) + \frac{V_0}{R}\cos(\omega t + \theta_{sig}) \tag{2.5}$$

After the *x* channel mixer,

$$I \otimes V_{ref}\cos(\omega t + \theta_{ref}) = \frac{V_0 V_{ref}\omega C}{2}\cos\left(\theta_{sig} + \frac{\pi}{2} - \theta_{ref}\right) + \frac{V_0}{2R}\cos(\theta_{sig} - \theta_{ref}) + f(2\omega)$$

$$= \frac{V_0 V_{ref}\omega C}{2} + f(2\omega) \tag{2.6}$$

Then the *x* channel reads

$$X = V_0 \omega C \tag{2.7}$$

Similarly in *y* channel,

$$Y = \frac{V_0}{R} \tag{2.8}$$

Finally we have the capacitance and resistance in *x* and *y* channels, repectively:

$$C = \frac{X}{V_0 \omega} \tag{2.9}$$

$$R = \frac{V_0}{Y} \tag{2.10}$$

2.3 ATOMIC FORCE MICROSCOPY

The phenomenal success of Scanning Tunneling Microscope (STM) enables people to image individual atoms(*20*) at the first time. However several limitations apply: (a) The sample surface must be conductive to allow tunnel current to occur, and usually it requires ultra high vacuum; (2) Significant forces will act collaterally with the tunnel current. The latter was then speculated that these forces might actually be useful for imaging, i.e. a force microscope. In 1986, Binning (the same inventor of STM) invented atomic force microscope (AFM) by regulating the atomic forces at a constant value above sample surface. With the fact that an individual atom can also interact with the AFM tip, AFM now reaches atomic resolution(*21*).

Nowadays, AFM provides a very important versatile tool to nano-scale sciences not only for basic imaging capabilities, but also it is used for measuring other physical properties like piezoelectricity (peizoresponse force microscopy(*22*)), capacitance(*23*), conductance, manipulating individual atoms and cells, AFM lithography and many more. In this dissertation, I will introduce two AFMs I developed for low temperature application and for capacitance imaging. The instrumentation details can be found in Appendix A, and the applications of AFM are covered in nearly every following chapters. In the following sections, I will introduce some basic concepts as well as the working mechanism on AFM.

2.3.1 Tip-sample interaction forces

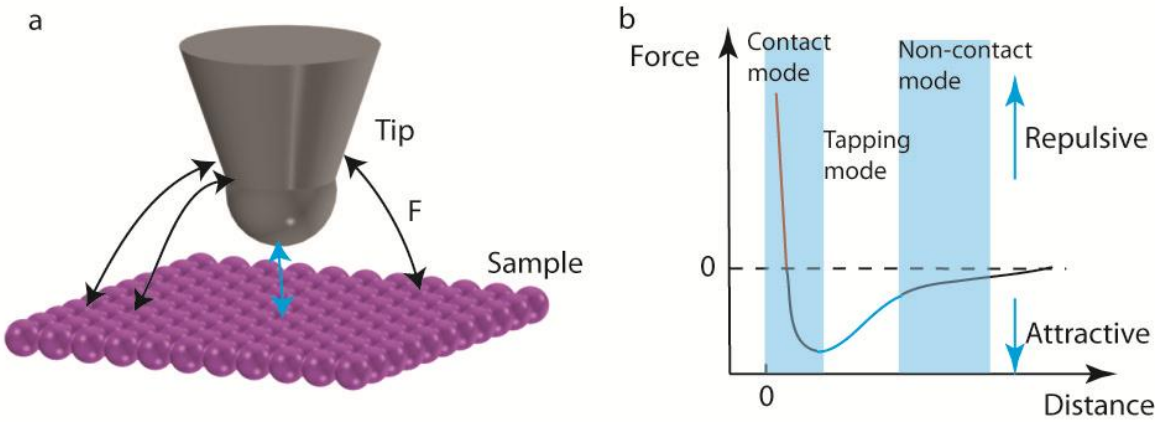

Figure 2.3 Forces between tip and sample. Black and blue arrows indicate long-range forces and short-range forces, respectively. (b) Force curve and imaging modes.

When an AFM tip is brought close to the surface (<100 nm), numerous atomic forces will interact between the tip and sample. Basically there are two types of force, long ranges forces (tens of nanometers range) like Van der Waas forces caused by the fluctuations and electric dipole of atoms and their mutual polarization, electrostatic forces and magnetic forces caused by excess surface/tip charges and magnetic dipoles, and short range force (sub-nanometer) from chemical bonding(*24*) (Fig. 2.3). Figure 2.3b shows the force curve as a function of tip sample distance. Different tip sample distance will induce different types of forces that allow different imaging modes, which will be introduced in Sec. 2.3.3.

2.3.2 Force sensors

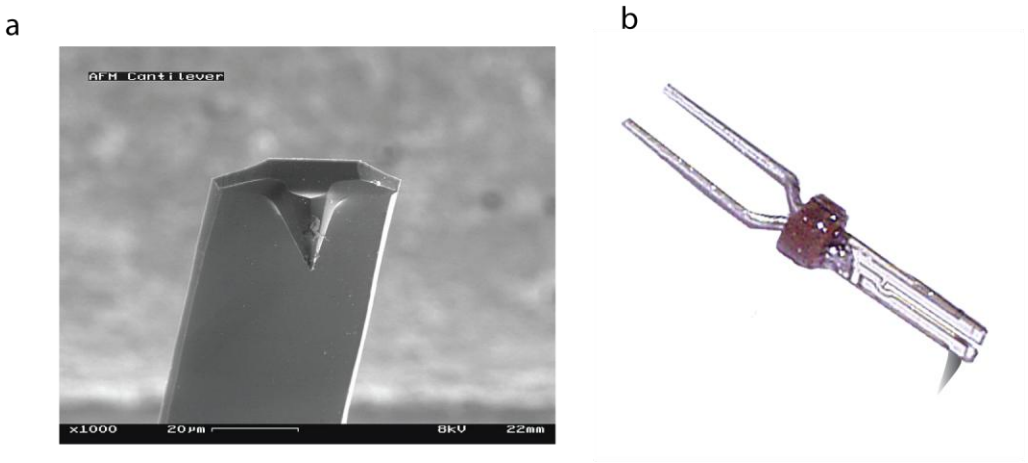

Figure 2.4 Force sensors (a) Cantilever based. (b) Tuning fork based.

The AFM tip is attached to a force sensor that detects the atomic forces. To achieve high resolution, the tip must have a sharp radius to reduce the interaction area on the sample surface; in the mean time the force sensor should be sensitive enough to sense the force changes due to changing of tip-sample separation in a scan. Two types of force sensors are commonly used, cantilever based and tuning fork based (Fig. 2.4). The cantilever beam is usually made by silicon or silicon nitride with various spring constants. A laser beam is focused on the highly reflective backside of the cantilever beam to detect beam deflection caused by atomic forces. With proper setup it can detect forces as small as several piconewtons (10^{-12} N). While the AFM cantilever works by detecting the amplitude of deflection, AFM tip with a tuning fork works totally a different way. A typical tuning fork force sensor is made of quartz, which has very high quality factor (several thousand at room temperature). Owing to this high quality factor, a small perturbation by the atomic forces will cause a significant resonance frequency shift. To recap, the tuning fork is driven by an external piezo stack at a frequency close to resonance frequency. Since quartz is piezoelectric, the external oscillations can induce an electric signal that is picked

up by two prolongs of the tuning fork. This electric signal provides a feed back signal to a phase locked loop (PLL), which actively compensates the frequency shifts caused by the tip-sample separation during a scan. With the frequency shift information, sample topography can be reconstructed.

2.3.3 AFM working principles

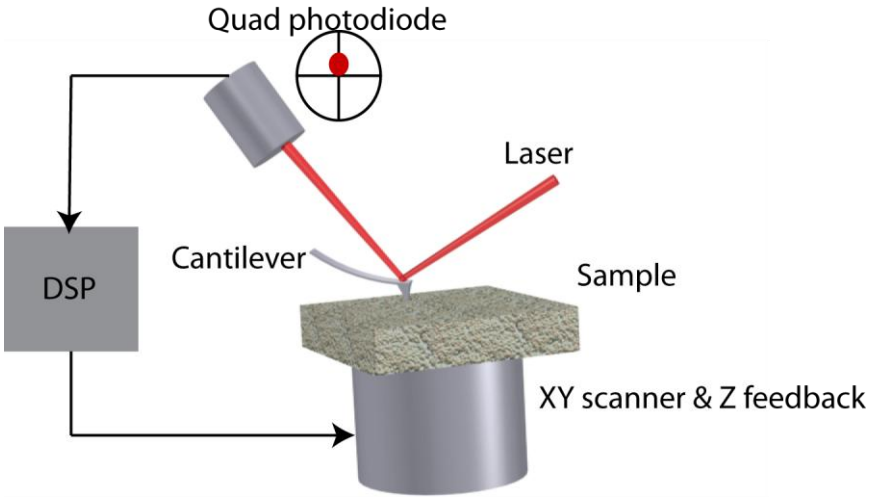

Figure 2.5 AFM working principle

The modern form of AFM comes from Meyer and Amer's approach in 1988(*25*). As shown in Fig. 2.5, a laser beam is focused on the backside of cantilever beam, and the reflected laser beam is detected by a quad photodiode. This photodiode has four quadrature in which the difference between the sum signals of top two and bottom two gives out the cantilever deflection. The deflection signal is then input to a digital signal processor (DSP) that generates real time feedback signals. The feedback signal in turn controls the Z feedback piezo to maintain constant tip-sample separation during a scan. In our home-made AFM, we use a DSP that is found on a sound board (Signal Ranger).

Before scanning, the tip has to be brought close to the sample surface until engaging atomic forces, this procedure is called "touch down". The touch down procedure is done by driving a Z motor to approach either tip or sample to the other, in the mean time the DSP continuously monitor the deflection signal (or resonance frequency if using a tuning fork) to prevent tip crash. When a "set point" is reached, i.e. the cantilever is bent by a preset amount, the tip is touched down. Two types of operation mode are common, contact mode and non-contact mode. In contact mode the cantilever is usually soft and in contact with sample surface. The deflection signal is generated by cantilever bending due to sample topography changes in a scan. In the non-conctact mode, the cantilever is vibrating all the time instead of touching sample surface. The vibrating amplitude serves as feedback signal as atomic forces can dampen it.

2.4 PIEZORESPONSE FORCE MICROSCOPY

Piezoresponse force microscopy (PFM) studies the mechanical response of a piezoelectric material under external electric field. Since all ferroelectrics are piezoelectric, PFM is a powerful tool to image and manipulate the ferroelectric domain walls, encode and read out information(*26*), and even has biological applications(*27, 28*).

During the operation, the tip is in contact with the sample surface. The voltage applied on the tip will cause local deformation of sample due to piezoelectric effect. When the polarization is vertical and pointing down normal to the sample surface, i.e. c- axis, positively applied voltage will cause the material to expand (Fig. 2.6a). And the electromechanical response is in phase with external field (phase $\varphi = 0°$). In the opposite, when the polarization is

along the c+ axis, the material will contract under positive voltage and the electromechanical response is out of phase ($\varphi = 180°$, Fig. 2.6b).

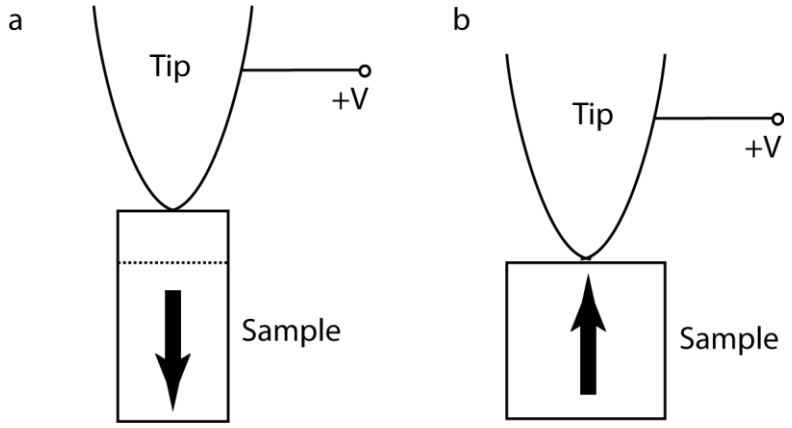

Figure 2.6 Working principle of PFM. (a) Sample expands when the polarization is aligned with external electric field. (b) Sample contracts when the polarization is reversely aligned with external electric field. The arrows in (a) and (b) represent polarization direction.

2.4.1 Piezoelectric effect

The strain effect under the external electric field in piezoelectric materials is described by a rank-3 tensor with relation $S_i = d_{ki}E_k$, where S_i is strain tensor, d_{ki} is piezoelectric tensor and E_k is the electric field. For vertical polarization (c axis) that a typical PFM detects, the corresponding tensor is d_{33}. For example, $BaTiO_3$ has a d_{33} component of 85.6 pm/V, which means under 1 V applied voltage along the c-axis the displacement of the barium atom is 85.6 pm.

The applied voltage usually has a form

$$V = V_{dc} + V_{ac}\cos\omega t \tag{2.11}$$

where V_{dc} is the DC voltage that manipulates the sample polarization and the second term is the AC part that detects the electromechanical response. And the electromechanical response can subsequently written as

$$\Delta = V_{dc}d_{33} + V_{ac}d_{33}\cos(\omega t + \varphi) \tag{2.12}$$

Where φ is the phase that takes values of 0° and 180°.

In real operation, the AC modulation frequency is chosen at the resonance frequency of the tip-sample mechanical system to allow optimal piezoresponse signal.

2.4.2 Application

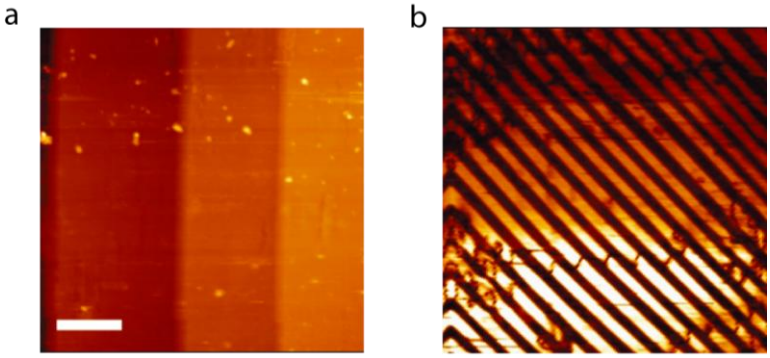

Figure 2.7 Topography (a) and PFM image (b) of BaTiO3. Scale bar: 10 $\boldsymbol{\mu m}$. Images are taken from http://en.wikipedia.org/wiki/File:Bulk_BTO_PFM_scan.png.

Different working modes lead to different applications for PFM. One basic mode is vertical or lateral polarization imaging, in which the tip is only biased by AC modulation during the scan. Figure 2.7 shows vertical PFM imaging of BaTiO3, and in the PFM image the sample shows a series of ferroelectric domain wall strips that does not show up in the AFM topography. AFM lithography is also feasible by manipulating ferroelectric domains with a DC voltage and image at 0 V. Ultra dense ferroelectric memory application (>16 Gbit inch^{-2}) is demonstrated by writing domains on highly strained $BaTiO_3$ film and reading out the polarization dependent

tunnel current(*26*). Instead of scanning, PFM can also working at the spectroscopy mode. In this mode, PFM tip is located at one position while the DC voltage is swept, enabling study of polarization on external field (e.g. *P-E* hysteresis loop). We will use this mode to study the ferroelectricity of strained $SrTiO_3$ sample in chapter 4. PFM also finds use in many other applications, e.g. biological applications to differentiate organic and mineral components of biological systems.

2.5 SCANNING MICROWAVE MICROSCOPY

As introduced in previous sections, sample topography and piezoresponse can be readily mapped out at nano-scale using AFM and PFM. In many cases, sample surface impedance, capacitance and dielectric constants are of great interests. Such material properties can be locally probed by looking at the electromagnetic interaction of microwave between the tip and sample. Integrating the microwave resonator sensor with an AFM, we are capable of doing scanning microwave microscopy (SMM), by which we can map the capacitance information, dopant density and impedance information together with sample topography.

Numerous forms of microwave sensors have been applied to SMM including broadband waveguide, resonant slots(*29*), stripline and microstrip resonators(*30*) and coaxial resonator(*31*). In our case we integrated a microstrip resonator similar to RCA's sensor, which will be covered in Chapter 5 and Appendix A.

3.0 SKETCHED OXIDE SINGLE ELECTRON TRANSISTOR

Devices that confine and process single electrons represent the ultimate scaling of electronics(*32, 33*). Such control has been achieved in a variety of materials(*34-36*), resulting in devices with remarkable electronic, optical and spintronic properties. Oxide heterostructures formed from ultrathin layers of $LaAlO_3$ grown on TiO_2-terminated $SrTiO_3$(*37, 38*), combined with a reversible nanoscale patterning technique(*39*), provide a versatile platform for nanoscale control at the single-electron limit. Here shown in this chapter we use this technique to develop "sketched" single-electron transistors (SketchSET) whose properties are probed through temperature-dependent transport. Shell filling from N=0 up to N=2 electrons by single-electron tunneling can be tuned by both bottom and side gates. Hysteresis in electron occupation is observed and attributed to ferroelectricity within the $SrTiO_3$ tunnel barrier. These single-electron devices may find use as nanoscale hybrid piezoelectric/charge sensors, and as elemental building blocks for solid-state quantum computation and quantum simulation platforms.

3.1 $LaAlO_3/SrTiO_3$ HETEROSTRUCTURE

Recently, a new high-mobility 2 dimensional electron gas (2DEG) was discovered at the interface of two wide-bandgap insulators $LaAlO_3$ and $SrTiO_3$(*37*). Since this discovery,

extensive interests are drawn on this novel material system. The transition between insulating and conducting states in this system is an atomically-sharp function of the number of $LaAlO_3$ unit cells (uc)(*38*). At or below a thickness of 3 uc $LaAlO_3$, the interface is insulating, while for ≥4 uc the interface is conducting. Also this metal-insulator transition can be tuned by applying a large back gate voltage. The conductance of films grown at a critical thickness (3uc-$LaAlO_3$/$SrTiO_3$) can be locally and reversibly controlled using a conductive atomic force microscope (c-AFM) probe technique(*39*). Positive voltages applied to the c-AFM tip locally switch the 3uc-$LaAlO_3$/$SrTiO_3$ interface to a conducting state, while negative voltages locally restore the insulating state. Besides these findings, magnetoresistance effect at the interface of these two non-magnetic perovskites was also observed. Superconductivity with a transition temperature 200 mK further indicates the quantum nature of this 2DEG.

Compared to its semiconductor analogue AlGaAs/GaAs heterostructure, the $LaAlO_3$/$SrTiO_3$ interface has similar electronic properties (Table 3.1). Meanwhile, unlike the AlGaAs/GaAs where the 2DEG globally exist at the interface, the c-AFM lithography technique enables us locally control the conductivity at the interface of 3uc-$LaAlO_3$/$SrTiO_3$, which provides us a versatile template for oxide nanoelectronics. As a result, nanowires(*39*), field effect nano-transistors(*40*), rectified nano-junctions(*41*) and photoconductive switches(*42*) have been realized. Moreover, the quantum nature of the 2DEG brings more possible novel device applications, e.g. single electron transistor that represent the ultimate scaling of electronics.

Table 3.1 Transport parameters of AlGaAs/GaAs and $LaAlO_3/SrTiO_3$ 2DEG.

	AlGaAs/GaAs	$LaAlO_3/SrTiO_3$
Thickness	order of 10 nm	10 nm (4 K) ≤4 nm (300 K)
Carrier density	10^{10}~10^{11} cm^{-2}	10^{13}~10^{14} cm^{-2}
Host layer thickness	Tens of nanometer	≥4 u.c. (1.6 nm)
Mobility	≥ $10^7 cm^2/Vs$ (4 K)	≤10000 cm^2/Vs (4 K)
Effective electron mass	0.03 m_0	3 m_0
Mean free path	order of 100 um	tens of nanometer
Fermi velocity	107 cm/s	0.6-6×106 cm/s
Fermi energy	14 meV	0.4-4 meV
Scattering time	0.38-38 ps	3 ps

3.1.1 Polar catastrophe and interface reconstruction

When expitaxially grow a polar material on a non-polar material, the interface is subject to atomic abruptness, resulting a polar discontinuity. Such discontinuity is unstable and an electronic reconstruction takes place to compensate for it. This process is called "polar catastrophe" and is considered as the mechanism behind the conductivity at the $LaAlO_3/SrTiO_3$ interface(*43*).

The perovskite oxides $LaAlO_3$ and $SrTiO_3$ can be decomposed into a series of alternating planes ($La^{3+}O^{2-}$, $Al^{3+}O^{2-}{}_2$, $Sr^{2+}O^{2-}$, $Ti^{4+}O^{2-}{}_2$) on (001) plane. Among them the $La^{3+}O^{2-}$ and $Al^{3+}O^{2-}{}_2$ planes are polar with +/-1 net charge, while $Sr^{2+}O^{2-}$and $Ti^{4+}O^{2-}{}_2$ planes are neutral.

Figure 3.1 shows two configurations that $LaAlO_3$ is grown on TiO_2 or SrO terminated $SrTiO_3$ substrate. A quick examination to the structure using parallel plate capacitor model can reveal that, if there are no interface charges (Fig. 3.1a and b), unrealistic voltages will accumulate as a function of $LaAlO_3$ thickness. Therefore, interface reconstruction must happen to allow compensate charges to cancel the divergent built-in voltages. For TiO_2 terminated $LaAlO_3/SrTiO_3$ heterostructure, half an electron per unit cell can migrate from $LaAlO_3$ to the interface so that Ti ion at the interface become $Ti^{3.5+}$ (Fig. 3.1c). This electronic interface reconstruction leaves whole structure neutral and an n-type 2DEG at the interface. Such n-type interface was confirmed by transport measurement, as pointed out in the introduction section of this chapter. While for SrO terminated heterostructure, half a hole must be acquired by the SrO to maintain structure neutral and avoid voltage divergence (Fig. 3.1d). Such hole transfer is realized by atomic interface reconstruction, i.e. by moving oxygen vacancy. However, electrically this interface is not conductive, since the mobility of holes is much lower than n-type interface. Further first principle calculation shows that the formation energy of oxygen vacancy is much smaller at the interface than at the $LaAlO_3$ surface. Oxygen vacancies can spontaneously form to compensate the holes at interface, leaving a low density of mobile holes(*44*).

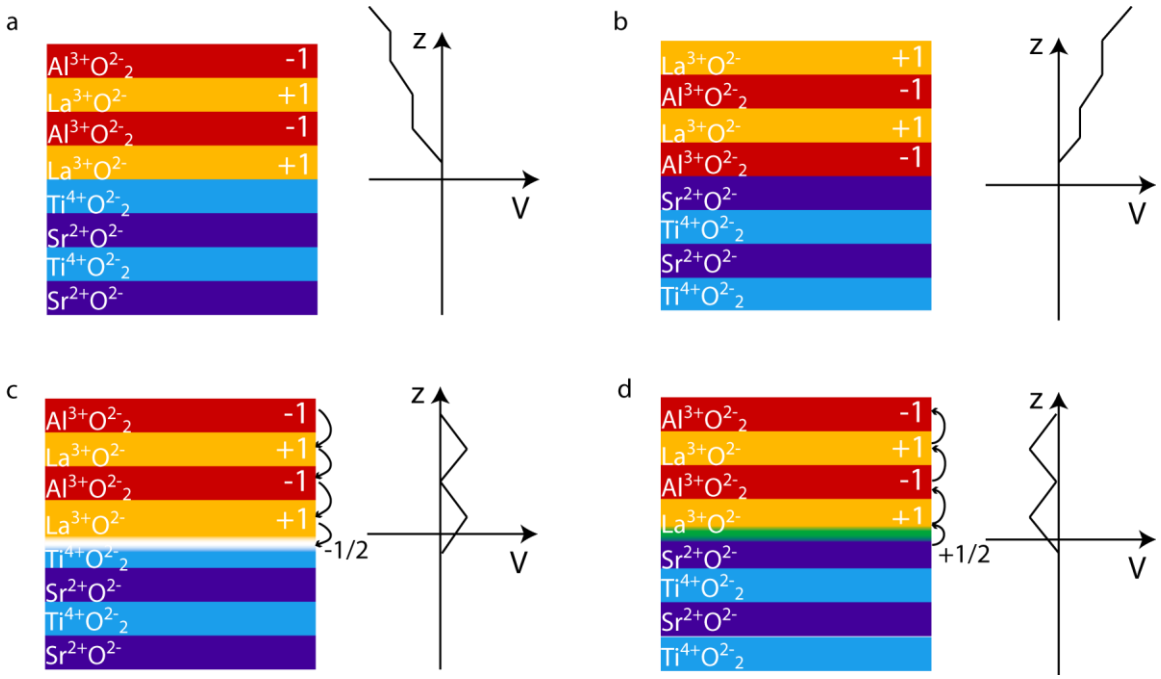

Figure 3.1 Polar catastrophe and interface reconstruction. (a) $LaAlO_3$ is grown on TiO_2 terminated $SrTiO_3$ substrate. Both $SrTiO_3$ and $LaAlO_3$ are decomposed into a series of (001) planes. A potential is built up in the $LaAlO_3$ film due to the non-zero charges of reconstructed planes. (b) $LaAlO_3$ is grown on SrO terminated $SrTiO_3$ substrate. As same as (a), a potential is built up in the $LaAlO_3$ film due to the non-zero charges of reconstructed planes. (c) For TiO2 terminated heterostructure as (a), half electron per unit cell is transferred from $LaAlO_3$ to the interface to compensate the physically unrealistic buit-in potential and keep $LaAlO_3$ crystal neutral. As a result, a two dimensional electron gas forms at the interface. (d) Similarly to (c), half hole per unit cell is acquired by the SrO to maintain structure neutral for SrO terminated heterostructure. However these holes at the interface are not mobile to form a conductive interface.

3.1.2 $LaAlO_3/SrTiO_3$ heterostructure growth

The $LaAlO_3/SrTiO_3$ heterostrucutre samples used in this work were all grown at Chang-Beom Eom's group at University of Wisconsin-Madison using pulsed-laser deposition (PLD).

In the growth, ultrathin layers of epitaxial $LaAlO_3$ were grown on $SrTiO_3$ substrates by PLD system equipped with high-pressure reflection high-energy electron diffraction (RHEED), which enabled the precise layer-by-layer growth of the thin films to be monitored *in-situ*. Before deposition, low miscut (<0.10°) $SrTiO_3$ substrate were etched using buffered HF acid for 30~90 seconds to maintain Ti-termination and the substrates were annealed in oxygen at 1000℃ for 2~12 hours to create atomically smooth surfaces with single unit cell height steps. The film deposition was achieved utilizing a resistive heater. A KrF excimer laser (248 nm) beam was focused on a stoichiometric $LaAlO_3$ single crystal target to an energy density of 2.0~2.5 J/cm^2 and pulsed at 3Hz. Two different growth conditions were used. For the first, the substrate growth temperature was set at 780 ℃ and chamber oxygen background pressure of 7.5×10^{-5} mbar, and the samples were annealed at 600 ℃, 400 mbar for 1 hour. While for the second the substrate growth temperature was set at 550 ℃ and chamber oxygen background pressure of 1×10^{-3} mbar, and samples were cooled down to room temperature. The $LaAlO_3$ RHEED intensity oscillations for the second sample are shown in Fig. 3.2a, which indicated a layer-by-layer mode. The resulting surface of the $LaAlO_3$ thin films were atomically smooth with single unit cell height steps measured by atomic force microscopy (AFM), as seen in Fig. 3.2b.

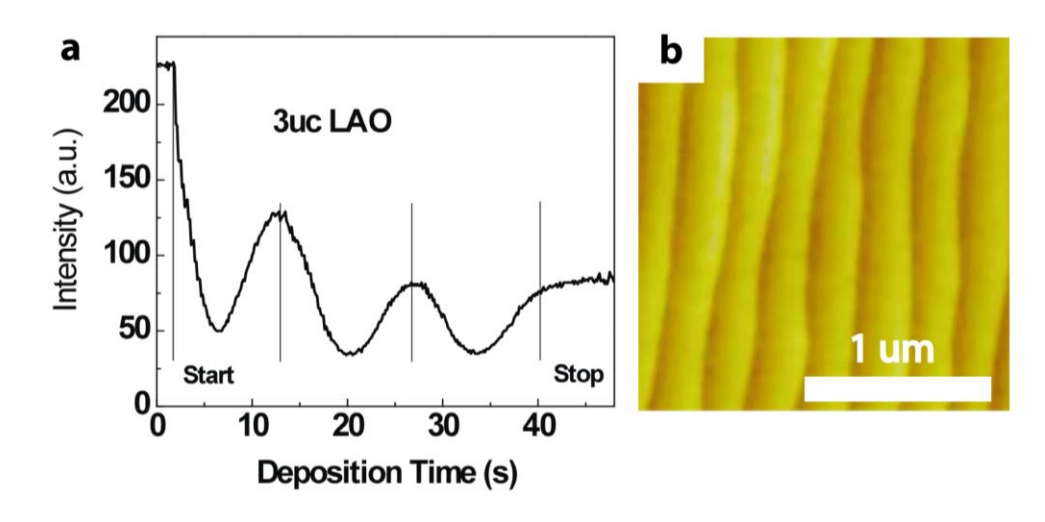

Figure 3.2 Growth of $LaAlO_3$ layer on $SrTiO_3$ substrate. (a), RHEED intensity oscillations of the $LaAlO_3$ film. The vertical dot lines indicate the growth time of $LaAlO_3$ unit-cell layer. (b), AFM images of 3 uc $LaAlO_3$ films on $SrTiO_3$ substrate.

3.2 CONDUCTIVE AFM LITHOGRAPHY

As introduced in Sec. 3.1, the polar catastrophe induces metal-insulator transition at the interface between $LaAlO_3$ and TiO_2 terminated $SrTiO_3$. When the thickness of $LaAlO_3$ is smaller or equal to 3 unit cells, the built in potential is not big enough to induce polar catastrophe. This 3 unit cell thickness is such a critical thickness that external doping of charges on $LaAlO_3$ surface could easily switch the insulating interface to a conducting state. In our previous work, we used a positively biased (8~10 V) AFM tip to locally induce a metal-insulator transition so that conducting nanostructure could be written on demand using this AFM lithography. In the mean time, negative voltages on the tip can erase the nanostructure and restore the insulating state.

Figure 3.3 shows the nanowire writing in the 3 uc $LaAlO_3/SrTiO_3$ heterostructure. The tip is biased with 10 V and slowly dragged from one electrode to the other at 300 nm/s. As soon as the tip reaches the other electrode, the conductance between the two electrodes has several orders of increase, which means a nanowire is written under the tip path. We can also cut the across the wire by with -10 V on tip, and the conductance is found to drop back to the insulating value, effectively creating a nano junction. The wire width is determined to be as small as 2 nm by looking at the sharpness of the conductance decrease. Using this method, we can write a third nanowire perpendicular to the nano junction as a gate to tune the conductance in the junction, effectively creating a field effect transistor(*40*). The nano junction is also found photo sensitive, creating photo current under light illumination, which is essentially a rewritable photodetector(*42*). By applying an asymmetric voltage (triangle function from -10 V to 10 V) to reconnect the nano junction, we can write a diode(*41*).

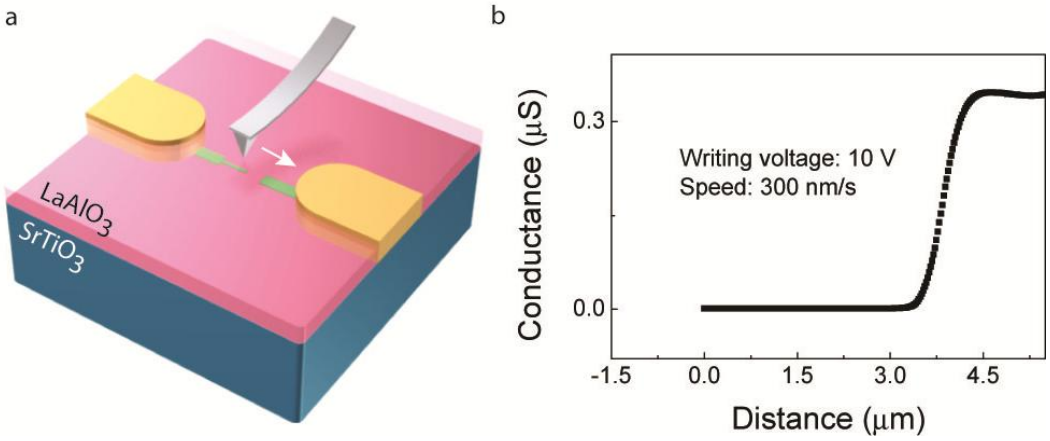

Figure 3.3 Conductive AFM lithography in 3 unit cell $LaAlO_3/SrTiO_3$ heterostructure.

The writing procedure is attributed to a "water cycle" mechanism, as Steve Hellberg (Naval Research Laboratory) suggested in an unpublished work after first principle calculations. In a regular sample environment, the 3-uc $LaAlO_3$ surface is covered by a thin layer of water

molecules. A positively biased tip will break up the bonds between H^+ and OH^- and removes OH^- atoms in a writing process, leaving an excess of H^+ atoms locally charging the surface. Such charged surface will switch the insulating interface to conductive and functions as an effective modulation doping to the interface.

This mechanism was further proved by our group by testing the writing procedure in different environment conditions(*45*). We found that writing in nitrogen gas, dry air helium gas and vacuum environment, no metal-insulator transition was observed. While writing in air with controlled humidity, the writing procedure worked. Furthermore, the written nanostructure preserves much longer in the environment that forbids writing than in air.

3.3 SINGLE ELECTRON TRANSISTORS

For over decades the Moor's law dictates the trend of semiconductor industry development by shrinking device size down at a constant speed. However in the very near future it will meet the scaling limits when the quantum effects emerge. Mesoscopic electron transport study reveals novel phenomena that may lead to future device applications. Single electron transistor (SET) is the striking example that reflects the ultimate scaling of electronics. As the name indicates, a single electron transistor (SET) is an electronic device that allows only one electron to pass through at a time.

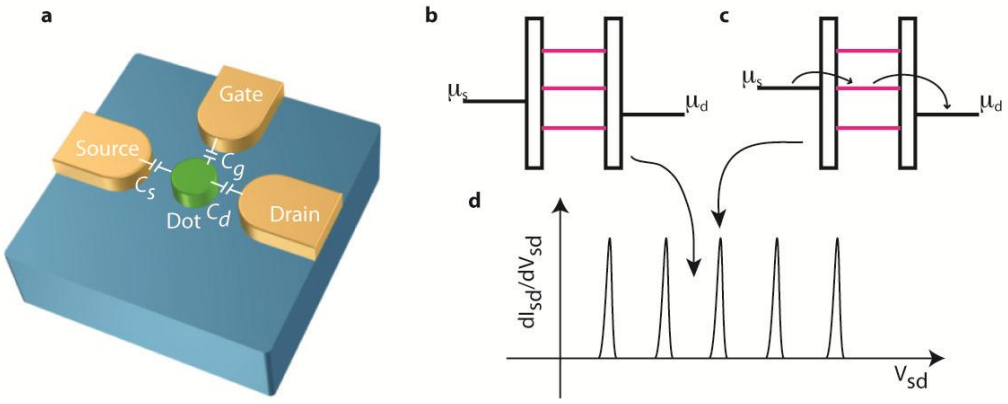

Figure 3.4 Single electron transistor and constant interaction model. (a) Schematic for a single electron transistor. The gate, source and drain electrode are capacitively coupled to the central island. (b) When the electrochemical potential of the quantum dot lies outside the bias window $\boldsymbol{\mu_s - \mu_d}$, the QD is in Coulomb blockade and no current can flow from the source to drain. (c) When the electrochemical potential of the quantum dot aligns with the electrochemical potential of source or drain electrode, resonant electron tunneling is observed and current can flow between source and drain. (d) Differential conductance exhibits a series of Coulomb peaks when resonant tunneling happens.

A typical SET consists of a source, drain and gate electrode as well as an island (quantum dot) that is separated by two tunnel barriers (Fig. 3.4a). The concept of SET is originated from the observation of quantized charges (~e^2/h) in a metal particle surrounded by tunnel junctions back to the 1960s(*46*). Later on the theory of Coulomb blockade was proposed to explain the resonant tunneling behavior, and the SET was realized in silicon MOSFET inversion layer 2DEG and AlGaAs/GaAs 2DEG material systems(*47*). In modern efforts, as more interests were casted on SET, it was reported in numerous material systems like carbon nanotube, graphene and organic molecular(*35, 36, 48*). The function of SET does not only rely on regulating the electron number, but also the SET can serve as an electron thermometer(*49*), transistor memory(*50*), a

device to single-shot read out electron spins(*51*), a nano-mechanical sensor(*52*) and can be integrated to an AFM probe to invasively detect nano-scale electric fields(*53*).

The electronic states of SET is described using constant interaction (CI) model(*54*) (*33, 55*). The model states that electrons can resonantly tunnel through the tunnel barrier once at a time to the quantum dot (QD) when the electrochemical potential of the QD μ_{dot} lies in the bias window, i.e. between the electrochemical potentials of the source (μ_s) or drain (μ_d) electrodes (Fig. 3.4c). In the opposite case μ_{dot} is outside the bias window (Fig. 3.4b), the device is in Coulomb blockade, i.e. electrons can not tunnel through the barriers due to Coulomb repulsion. Two assumptions are made in this model: (a) A single capacitor C is parameterized to describe the Coulomb interaction among the electrons in the QD and between the QD and the environment. Namely as shown in Fig. 3.4a, $C=C_s+C_d+C_g$, where C_s is the capacitance between the source and QD, C_d is the capacitance between the drain and QD, and C_g is the capacitance between the gate and QD. (b) The single particle energy levels in SET are not affected by these interactions. Defining V_s, V_d and V_g as the respective potentials of source, drain and gate, the total energy of $U(N)$ of QD with N electrons can be described as

$$U(N) = \frac{(-|e|(N-N_0)+C_sV_s+C_dV_d+C_gV_g)}{C} + \sum_{n=1}^{N} E_n(B) \tag{3.1}$$

where –|e| is the electron charge, N_0 is the number of electrons at zero external gate voltage and E_n is the single particle level which is a function of external magnetic field B. C_sV_s, C_dV_d and C_gV_g are effective induced charges that can alter the electrochemical potential of the QD.

The electrochemical potential of the QD is defined as

$$\begin{aligned}\mu(N) &\equiv U(N) - U(N-1) \\ &= \left(N - N_0 - \frac{1}{2}\right)E_C - \frac{E_C}{|e|}\left(C_sV_s + C_dV_d + C_gV_g\right) + E_n\end{aligned} \tag{3.2}$$

where $E_c=e^2/C$ is the charging energy and $\mu(N)$ denotes the transition between Nth and (N-1)th ground state.

The addition energy is defined as the spacing of electrochemical potentials of transitions between two successive ground states.

$$E_{add} = \mu(N) - \mu(N-1) = E_C + \Delta E \tag{3.3}$$

where ΔE is the level spacing in the QD. From the equation we can see to add one electron, the required energy has two parts: one is the electrostatic part to charge the dot, the other one is the chemical part that determines the level spacing.

The electrochemical potential of the QD is changed linearly with the gate voltage, and the corresponding proportion factor $\alpha=C_g/C$. This proportion factor directly correlates the Coulomb peak spacing in measurement (specified by voltage) to the addition energy (specified by meV).

3.4 SketchSET DEVICE FABRICATION AND SIZE CHARACTERIZATION

In this section, I will introduce how to create single electron transistors using c-AFM lithography in the 3 uc $LaAlO_3/SrTiO_3$ heterostructure, as well as how to characterize the device size.

3.4.1 Device fabrication

The 5 mm x 5 mm $LaAlO_3/SrTiO_3$ samples are patterned with 6 gold electrodes contacting the interface by ion milling 25 nm and backfilling with 2 nm Ti and 23 nm Au. Device "sketching" is performed using conductive-AFM lithography (c-AFM) in a commercial

AFM system (Asylum MFP-3D). The following procedures are typical in SketchSET fabrication:

(1) *Virtual electrodes writing:* q-2DEG "virtual electrodes" (500 nm wide, ~10 m long) are written in contact with the gold electrodes by applying a 10 V (or 8 V) voltage to the tip and raster scanning at constant (typically 800 nm/s) speed. As a result, a 5 μm × 5 μm working area surrounded by virtual electrodes is defined for fine device writing.

(2) *Source, drain and side gate electrodes definition:* Source and drain virtual electrodes are connected by writing a q-2DEG nanowire using the same parameters. Side-gate nanowires are written either 50 nm away from the center of source-drain nanowire, or directly cross the source-drain nanowire in the perpendicular direction.

(3) *Tunnel barrier and QD creation:* After source, drain and wire electrodes are written, the AFM tip is positioned at the center of source-drain nanowire. A brief negative pulse (-10 V or -8 V, 15 ms to 1000 ms duration) is applied to create a barrier. Writing this barrier typically causes 10% decrease in conductance at room temperature as measured between any two of the electrodes. Finally a subsequent positive pulse with the same magnitude and much shorter duration (2 ms to 20 ms) is applied to create the QD. Detailed parameter values are listed in Table 3.2 and Fig. 3.5. Five devices are fabricated and the results of three devices are discussed in this dissertation.

Table 3.2 Device sketching parameters. Five SketchSET devices as well as a control device are sketched. Device A, B and C are presented in this dissertation.

	Sample growth conditions	Electrodes writing amplitude (V)/width (nm)	Erase pulse amplitude (V)	Erase pulse duration (ms)	Write pulse amplitude (V)	Write pulse duration (ms)	Side gate distance to dot (nm)
Device A	7 80 C° at 7.5×10^{-5} mBar	10/8	-10	1000	10	10	50
Device B		8/5	-8	15	8	2	N/A
Device C		10/8	-10	2000	10	20	50
Device D	5 50 C° at 1.0×10^{-3} mBar	8/3.3	-10	1000	10	5	N/A
Device E		8/3.3	-10	1000	10	1	N/A
Device F		8/3.3	-10	100	N/A	N/A	N/A

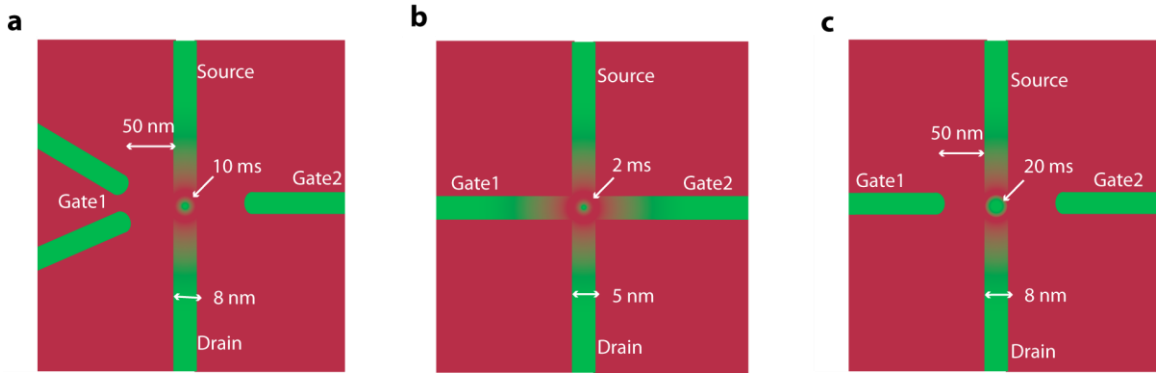

Figure 3.5 Device A, B and C structures. (a), Device A. The side gates are sketched 50 nm away from the QD. (b), Device B. Two crossed nanowires are written first then the barrier and QD are pulsed. (c), Device C. Two side gates are sketched 50 nm from the QD.

3.4.2 Device size characterization

The sizes of the nanowire electrodes, tunnel barrier and the QD are dependent on the writing/erasing parameters, sample growth conditions, sample surface conditions, and relative humidity. We perform a similar calibration method as Ref. (*39*) to estimate the wire width and QD diameter.

To estimate a nanowire width, the AFM tip is slowly moved across the wire (-10 V, 10 nm/s) and the conductance is measured simultaneously as a function of tip position. The full width of half maximum of the deconvolved differential conductance gives out the wire width. For a wire written at 10 V, 800 nm/s speed, the wire width averages 8 nm.

To estimate the QD diameter, an array of dots is written in a 1-μm gap. The spacing between the dots is varied from large to small values until the observance of a steady conductance increase, i.e. the dots connected each other and the gap was filled. 2 ms, 10 ms and 20 ms QD write pulse durations (10 V) will produce QD "diameters" of 0.8 nm, 1.5 nm and 2.8 nm respectively. For a diameter of 1.5 nm, one can roughly estimate the number of electrons able to reside within the QD, based on typical two-dimensional carrier densities for nanoscale writing $n \approx 5\times10^{13}$ cm^{-2} at the 3uc-$LaAlO_3$/$SrTiO_3$ interface: $N=\pi d^2 n/4 \approx 1$ electron. This estimate agrees well with the observed behavior, described in the following sections.

The barrier size is estimated in a reverse way. An array of erase pulses (-10 V) is applied across a predefined rectangle q-2DEG area of 1 um width. For certain pulse spacing the conductance of the rectangle area drops to zero, which means the barriers connects each other and the pulse spacing is the barrier diameter. As a result, a 1 second -10 V pulse creates 6 nm barrier diameter. However, this value is under estimated especially for shorter pulse durations. Since thermally activated carriers can still contribute to the conductance even when the barriers

successfully connects each other, which gives false indication that the area has not been completely cut.

3.5 MEASUREMENT

After AFM lithography, the sample is quickly transferred without to a closed cycle cryostat with careful prevention to light illumination. Then the cryostat is pumped down to vacuum (2×10^{-5} Torr) and no significant conductance drop is observed at room temperature. Low temperature transport measurement is carried out at temperatures varying from 16 K to 40 K, with the differential conductance G_{sd} and capacitance C_{sd} measured using a dual phase lock-in amplifier (Stanford Research SR830, same method as described in section 2.2). In the set up, a DC voltage V_s plus a small ac modulation $V_s+V_{ac}\cos(2\pi ft+\varphi)$ are applied to source electrode through a bias box, where f=25.5 Hz is the modulation frequency and φ is the reference phase. The phase φ is adjusted such that the X channel measures the capacitance of the device and Y channel is measures the differential conductance of the device. Besides temperature sweep, side gate and back gate effects to the single electron charging are also explored.

3.6 RESULTS AND DISCUSSION

In this section, I will discuss the results of electronic characterization of Device A, B and C. Experiments focus on the effect of the side gates (V_{g1} and V_{g2}) and back gate (V_{gb}) on the source-drain differential conductance (G_{sd}) and capacitance (C_{sd}).

We use COMSOL finite element analysis to illustrate the electron energy barriers of the device (Fig. 3.6b). Figure 3.6c shows the differential conductance curve for Device A immediately after cooldown, where the side gates and V_{gb} are all grounded and the drain V_d (where current is measured) is held at virtual ground. For sufficiently small source-drain voltage (V_{sd}), the differential conductance is strongly suppressed, and increases rapidly above a well-defined threshold. Though the structure is nominally symmetric, the threshold for positive and negative V_{sd} is generally different owing to hard-to-control variations at the scale of ~1 nm. Figure 1c shows two clearly resolved "Coulomb peaks" for V_{sd}<0, and other three are observed for V_{sd}>0 before being obscured by the large conducting background. Subsequent voltage cycles result in fewer peaks (see Fig. 3.7). Structures that do not have islands at the intersection (e.g., SketchFET devices) do not exhibit any Coulomb peaks.

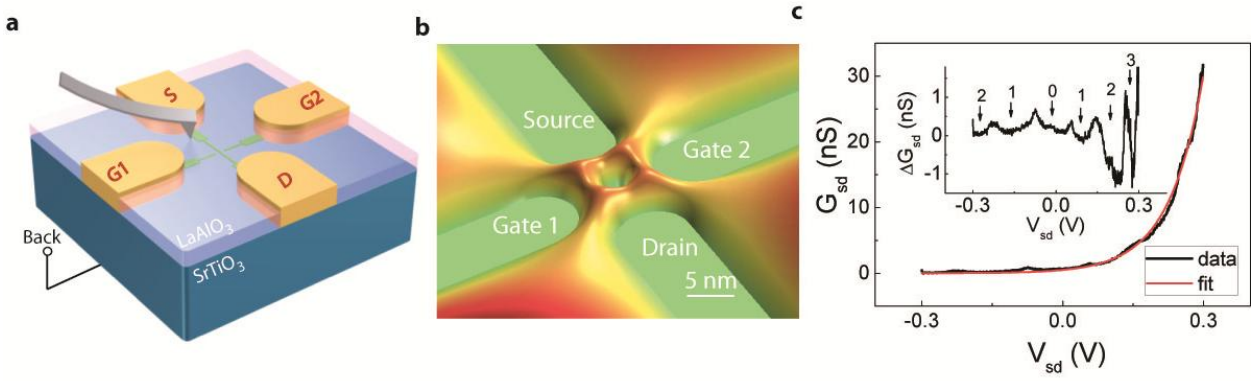

Figure 3.6 SketchSET schematic and transport characteristics. (a) Conductive-AFM sketching of a single-electron transistor device. (b) An energy illustration of the SketchSET device. QD tunnel barriers are created by applying a negative voltage pulse of duration t_b. The QD is formed by applying a positive voltage pulse with duration t_d. (c), Differential conductance G_{sd} from source to drain at T=16 K. The conductance is suppressed at low biases and increases rapidly above a threshold voltage ~0.2 V. The red curve is an exponential fit to the data. The peaks in the inset are Coulomb peaks after subtracting an exponential background; the numbers with arrows indicate electron occupation.

3.6.1 Temperature dependence

Here we focus on transport for SketchSET devices in the low-conductance regime. Figs. 2a,b show the differential conductance G_{sd} and capacitance C_{sd} of Device A as a function of temperature (16 K to 40 K) and source-drain voltage V_{sd} (-0.3 V to 0.3 V), with all three side gates and the back gate grounded. The conductance exhibits distinct Coulomb peaks which are associated with resonant tunneling into the QD. Coinciding with these conductance peaks are abrupt changes in capacitance. Generally, increases in QD occupancy N=1 are associated with roughly constant capacitance jumps C (see also Fig. 3.9). In the blue shadowed regime in Fig. 3.7b, the conductance is negligible and the capacitance $C_{sd}<$ C, is insensitive to V_{sd}. For these reasons, we infer that N=0 electrons are contained in the QD in this regime.

The Coulomb peaks and associated capacitance jump locations exhibit hysteresis with respect to the source-drain voltage sweep direction. The conductance peak position, peak width and hysteresis magnitude vary significantly with temperature. With increasing temperature, the peak position first shifts to more negative V_{sd}, then at T_{C1}=25 K it begins to increase with temperature. The width of the peak increases approximately linearly with temperature; above T=T_{C1}, the slope increases by a factor of five (Fig. 3.7d).

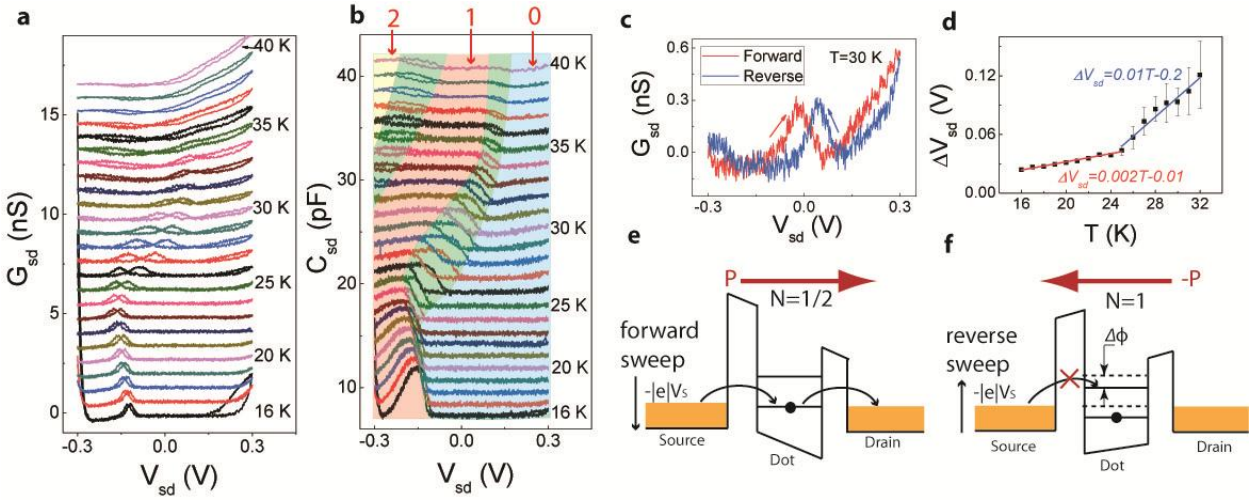

Figure 3.7 Temperature dependent differential conductance and capacitance of Device A. (a), Differential conductance G_{sd} measured at temperatures ranging from 16 K (bottom black curve) to 40 K (top blue curve) in 1 K step. Curves are manually shifted by 0.6 nS for clarity. (b), Source-drain capacitance C_{sd} measured over the same range as a. Curves are shifted by 1.6 pF for clarity. A sharp change in C_{sd} corresponds to a single electron tunneling event. The shadowed blue, red and yellow regions indicate electron occupation of 0, 1 and 2, respectively. The green regions indicate hysteretic regions where electron occupation in the QD changes by N=+/-1. (c), G_{sd} measured at T=30 K for forward (red) and reverse (blue) source-drain bias sweep directions. The Coulomb peaks are shifted by ferroelectric polarization in the $SrTiO_3$. (d), Coulomb peak width vs. temperature. A "kink" is observed at T_{C1}=25 K, coincident with a ferroelectric phase transition in the $SrTiO_3$. (e), Schematic band diagram showing a resonant tunneling at V_{sd}=0 V in the forward sweep direction. The red arrow indicates the ferroelectric polarization direction. (f), For the reverse sweep, the electrochemical potential of the dot is lowered by $\Delta\phi$ so that the system is in the Coulomb blockade regime.

3.6.2 Ferroelectric tunnel barriers

The observed hysteresis in the Coulomb peak position is attributed to ferroelectric switching in the $SrTiO_3$ barrier. The lattice constants of $LaAlO_3$ and $SrTiO_3$ are 3.789 Å and 3.905 Å respectively (3% mismatch), and the 3 uc $LaAlO_3$ is coherently strained biaxially to match the $SrTiO_3$ lattice constant. The profound effect of strain on thin $SrTiO_3$ layers is well known(*14-16, 56*). Field-emission experiments on $LaAlO_3/SrTiO_3$-based SketchFET devices(*57*) show evidence of a diverging dielectric permittivity associated with structural phase transitions in the near-interface $SrTiO_3$ region at T_{C1}= 25 K and T_{C2}=65 K. The hysteretic behavior observed as a function of local in-plane applied electric fields is highly non-monotonic with respect to temperature, and exhibits anomalies at a known structural transition T_{C1}. This hysteresis is qualitatively distinct from hysteretic changes in polarization that have been reported for vertically gated $LaAlO_3/SrTiO_3$ heterostructures(*58*). Hysteresis in both conduction and capacitance as a function of the back gate bias is observed for Device A; however, as noted in Ref. (*58*), it is difficult to distinguish ferroelectric hysteresis from trap charging or other polarization effects in this geometry.

The ferroelectric polarization has a profound influence on the resonant tunneling characteristics of the SketchSET, and is capable of switching the conductance of the source-drain channel between an "on" and "off" state (Fig. 3.7c). At T=30 K, when V_{sd} is swept in the forward direction, resonant tunneling is observed at V_{sd}=0, with G_{sd}=0.3 nS. After sweeping V_{sd} to 0.3 V and returning to V_{sd}=0, the conductance has vanished.

The effect of the ferroelectric polarization on the SketchSET characteristics can be understood qualitatively by expanding the constant-interaction (CI) picture(*33*), in which there are well-defined energy levels in the QD, to include the effect of the ferroelectric polarization.

Single-electron tunneling occurs when an allowed energy state within the QD becomes resonant with the electrochemical potential of either the source lead (μ_s) or drain lead (μ_d). Such a resonant condition is indicated in Fig. 3.7e. Ferroelectric tunnel barriers can shift the chemical potential within the QD (by an amount $\Delta\phi$) such that resonance only occurs for one polarization direction (Fig. 3.7f). The SketchSET can be regarded as a local sensitive detector of polarization in the $SrTiO_3$; however, it is only sensitive when the SketchSET undergoes resonant tunneling.

Within the CI framework, the Coulomb peak spacing ΔV_{sd} can be used to estimate the addition energy E_a by $\Delta V_{sd}=E_a/e\alpha$, where the lever arm $\alpha=C_s/C_{QD}$ is the ratio between the source to QD capacitance C_s and total QD capacitance C_{QD}. The width of the Coulomb peak is expected to broaden linearly with temperature(*48*): $dV_{sd}/dT=3.5k_B/e\alpha$, where k_B is the Boltzmann constant. From Fig. 3.7d, we can estimate α~0.15 for $T<T_{C1}$ and α~0.03 for $T>T_{C1}$, respectively. The addition energy below 25 K cannot be estimated since N=2 states are not observed. As the Coulomb peak shifts to positive values of V_{sd}, a second electron state emerges at T>31 K with spacing ΔV_{sd} ~0.3 V (Fig. 3.7b), which allows for an addition energy to be estimated E_a=9 meV and thus $C_{QD} \geq$18 aF. An upper limit $C_{QD} \leq$40 aF can be inferred from the thermal broadening effect which occurs at T~45K. The energy shift caused by the ferroelectric remnant polarization can be estimated in a similar manner: ΔE_{FE}=2~6 meV.

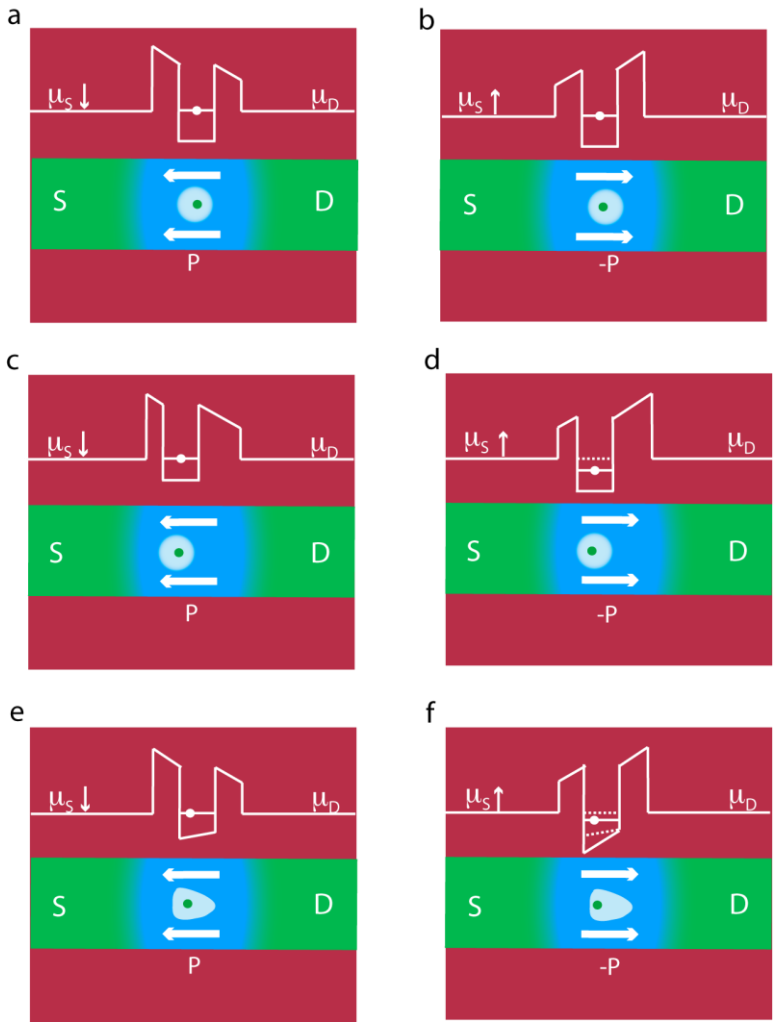

Figure 3.8 Ferroelectric contribution to electron energy shifts in a SketchSET. (a) The QD is surrounded by tunnel barriers of equal thickness. The horizontal white arrows indicate the polarization direction as the source chemical potential is lowered. (b) In the reverse sweep and same geometry as (a), the polarization is switched. No energy shift is observed when μ_s reaches the value in forward sweep. (c) The QD is displaced in the barriers so that polarization is unevenly distributed with respect to the QD. (d) For the reverse sweep and same geometry as (c), the QD level is shifted by the switched polarization. The dashed line represents the QD energy prior to ferroelectric polarization switching. (e) The QD has an asymmetric shape that produces a dipole moment. The bottom of the QD well is tilted to reflect the internal dipole field. (f) The QD energy is shifted by electrostatic coupling of the ferroelectric with the QD dipole.

A QD energy shift ΔE due to coupling to ferroelectric polarization can arise from one of two mechanisms: (1) direct potential shifts due to the ferroelectric polarization, and (2) dipole-dipole coupling between the QD and the FE polarization. These effects are illustrated in Figure S7 below. If the QD is completely symmetric between source and drain, then one does not expect the polarization direction to produce an energy shift, because the two configurations are related by a mirror symmetry (Fig. 3.8a,b). However, if the QD is located off-center or the barrier between the QD and the source is narrower than the drain (Fig. 3.8c,d), the polarization direction will couple directly to the energy of the QD. A second mechanism for coupling between ferroelectric polarization and the quantum dot arises when the QD itself retains a built-in polarization. In this case, dipole-dipole coupling can produce an energy shift (Fig. 3.8e,f). Observation of a hysteretic energy shift does not automatically distinguish between these two coupling mechanisms.

3.6.3 Side gating

Resonant tunneling through the QD can be modified through the application of either side gates or a back gate. The strength of the side-gate coupling can be adjusted by varying the barrier width (controlled by the duration of the erase pulse t_b) or by writing side gates a fixed distance from the QD. Two examples are shown for side gates created close to the island (Device B) and separated by a 50 nm gap (Device A). For Device A (Fig. 3.9a,b), a clearly defined resonance is shifted by V_{sd}=40 mV as the side gate V_g is changed from -0.2 V to +0.2 V, with no evidence of gate leakage. The low coupling factor, V_s/V_g =0.1 in this case, reflects the geometric separation of the side gate. For Device B, the gates are separated by approximately the same distance as the source and drain leads; hence, significant gate leakage is

observed. Sharp resonances are only observed when V_{g1} and V_{sd} have *opposite signs* (Fig. 3.9 c,d). This "differential mode" is more effective in aligning the lowest QD chemical potential level than the "common mode" configurations (Fig. 3.10).

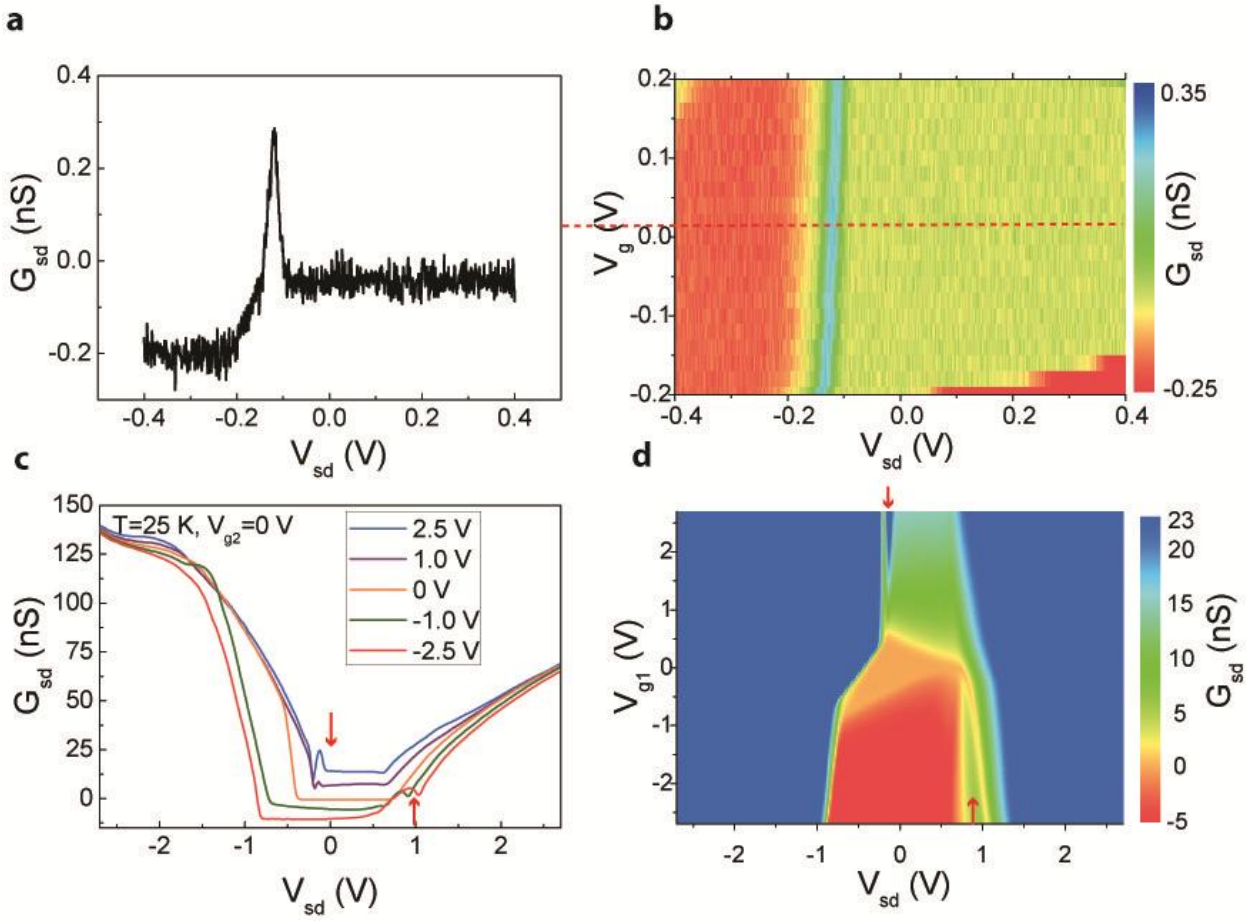

Figure 3.9 Side gating for device A and B at T=25 K. (a) Differential conductance G_{sd} at zero side gate voltage of device A. (b) Intensity plot of differential conductance G_{sd}, the coulomb shifts about 40 mV fro side gate from -0.2 V to 0.2 V. (c) Differential conductance G_{sd} for various side gate voltages V_{g1}=-2.5 V, -1.0 V, 0V, 1.0 V and 2.5 V. The other side gate is grounded: V_{g2}=0 V. (d) 2D plot of G_{sd} versus V_{g1} and V_{sd}. A single Coulomb oscillation is observed only when V_{g1} and V_{sd} have opposite signs. The red arrows in a and b mark the resonant tunneling.

The QD for Device B is written with a brief (t_d=2 ms) pulse at the center; all the nanowire electrode leads including the side gates, source and drain are separated from the QD

with the barrier created by a single negative pulse. In this configuration the side gates are as strongly coupled to the QD as the source and drain electrodes, and therefore, besides electrostatically modulating the energy level in the QD, they can also directly contribute tunneling electrons into the QD. In the gating experiment, V_{g1} and V_{sd} ($V_{sd} \equiv V_s - V_d$) are swept while keeping $V_{g2}=V_d=0$. As shown in Fig. 3.9c,d, the Coulomb peak only emerges in the "differential mode" configuration when V_{g1} and V_s have opposite signs but not in the "common mode" configuration when V_{g1} and V_s have the same sign. The reason is that the differential mode configuration is more effective in aligning one of the four leads with the QD chemical potential. A qualitative energy diagram is shown in Fig. 3.10.

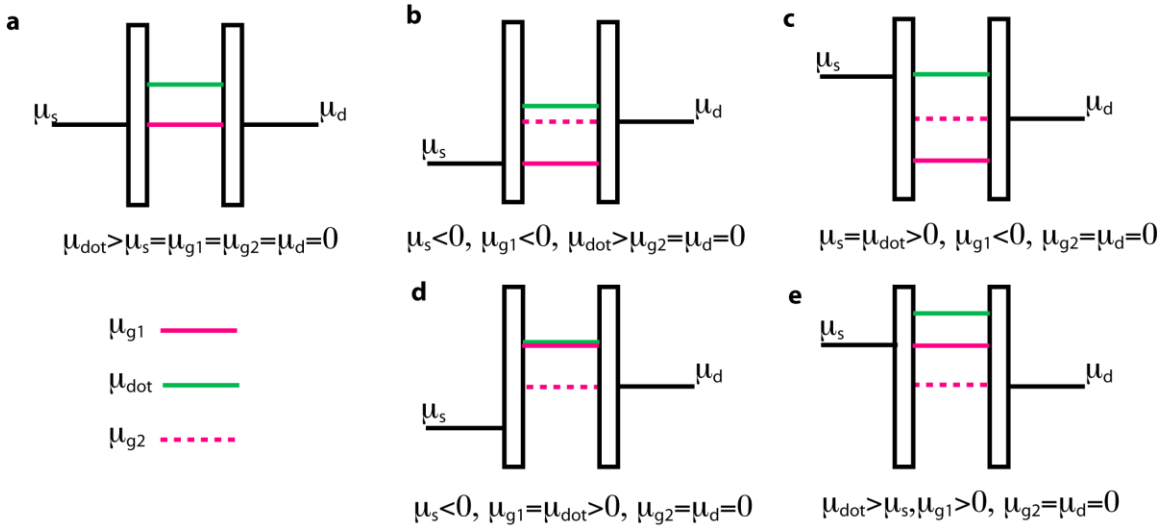

Figure 3.10 Illustration of energy levels for device B at different electrochemical potentials of source and gate1 electrodes. The red, green and dashed red lines represent μ_{g1}, μ_{dot} and μ_{g2} respectively. (a) Initially, all the electrodes are grounded ($\mu_s=\mu_d=\mu_{g1}=\mu_{g2}=0$). For this device, the lowest available electrochemical potential $\mu_{dot}>0$. (b) If both μ_s and μ_{g1} are lowered, μ_{dot} is lowered but is not low enough to reach μ_d; hence no resonance condition is met. (c) μ_s is raised and aligns with μ_{dot}. (d) By approximate symmetry between all four electrodes, if both μ_s and μ_{g1} change sign, μ_{g1} can be made to align with μ_s. e, When both μ_s and μ_{dot} are raised, μ_{dot} is raised further still no resonance is observed.

3.6.4 Back gating

SketchSET structures respond to modest ($|V_{bg}|$<1 V) voltages applied to the bottom of the $SrTiO_3$ substrate. The sensitivity of the SketchSET to back gating, as measured by changes in effective carrier density within the QD, is more than two orders of magnitude larger than what has been reported for back-gate control of the metal-insulator at room temperature(*38*) and superconductivity at low temperature(*59*). The principal reason for the relatively high sensitivity is that the high curvature of the metallic nanostructures focuses the electric flux lines, thereby greatly increasing the electric-field effect at the device.

Figure 3.11 shows the differential conductance and capacitance as a function of back gate bias V_{bg} and source-drain bias V_{sd} for Device C. For the lowest value V_{bg}=-0.4 V, a single resonant peak is observed as V_{sd} is swept from 0 V in either the positive or negative direction. The resonant peaks mark a transition from N=0 electrons in the QD to N=1 electrons. The increase in N is associated with a discrete jump in the measured capacitance (Figs. 3.11c,d), increasing from C_0~2.5 pF for V_{sd}=0 by an amount ΔC_-=3.5 pF (ΔC_+=2.5 pF) for scans with increasing $|V_{sd}|$.

Though the structure is nominally symmetric with respect to source and drain, there are clear asymmetries which result in different thresholds for positive and negative V_{sd}. As V_{bg} is increased, the resonances shift toward V_{sd}=0 V (Fig. 3.11d), and a second resonant peak is observed on the V_{sd}<0 side. The higher stability of the N=2 state, as measured by the strong suppression of the conductance near V_{sd}=-0.18 V, and the greater width of the N=2 plateau in the capacitance, is believed to be a manifestation of the well-known "shell filling effect" that has been observed in 2D quantum dot systems(*60, 61*) and III-V self-assembled QDs(*62*). Higher N

values are not observed because the structure becomes highly conducting outside of the range shown, but a similar non-uniform spacing is apparent in Fig. 3.11c.

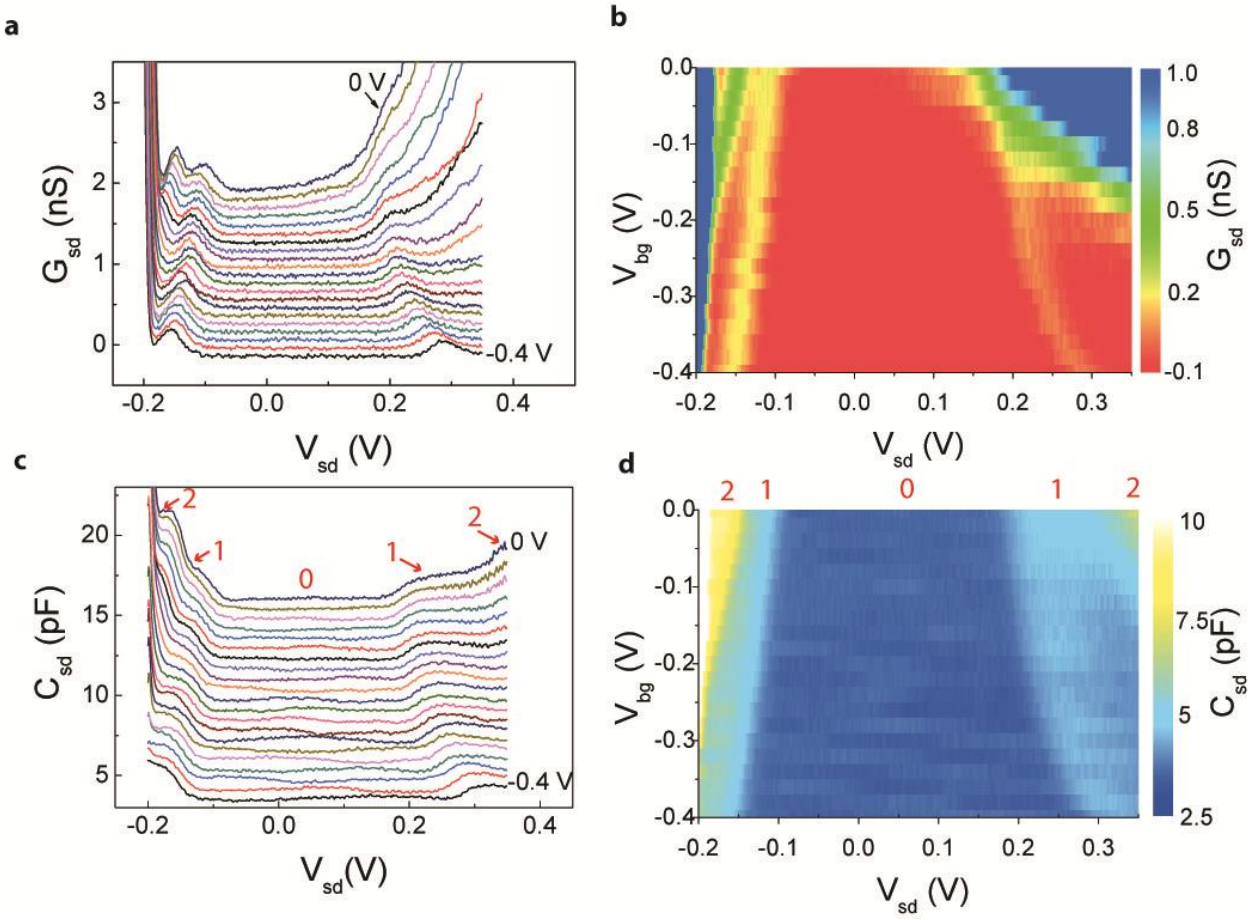

Figure 3.11 Differential conductance and capacitance dependence on the back gate voltage at T=16 K, Device C. (a) differential conductance (G_{sd}) curves at back gate voltages V_{bg} from -0.4 V to 0 V in 0.02 V step. Curves are offset by 0.2 nS for clarity. The second electron emerges at V_{bg}=-0.1 V. (b) Intensity plot of G_{sd}. (c) Capacitance curves at the same gating conditions with a. Curves are offset by 0.3 pF for clarity. The discrete jumps coincide with changes in electron occupancy in the QD. (d) Intensity plot of C_{sd}. The numbers in (c) and (d) indicate the electron occupation N in the QD.

A remarkable feature of the SketchSET is the high sensitivity of the capacitance to changes in electron occupation in the QD. The change in capacitance (~pF) observed during

single electron charging event at the QD is approximately three orders of magnitude too large to be accounted for solely by electrostatic effects. It is well known that $SrTiO_3$ is a high-permittivity incipient ferroelectric with a dielectric constant that can exceed ~10^4 at low temperatures that is easily perturbed by structural deformation, strain and electric fields(*63*). The presence of a single bound electron at the $LaAlO_3/SrTiO_3$ interface is predicted to produce a large distortion of the $SrTiO_3$ octahedra that extends far beyond the location of the charge(*39*). This structural distortion increases the polarizability of the nearby $SrTiO_3$, thus increasing the parasitic capacitance C_p between source and drain (Fig. 3.12). The inferred C_{QD} is roughly four orders of magnitude smaller than the measured capacitance C_p.

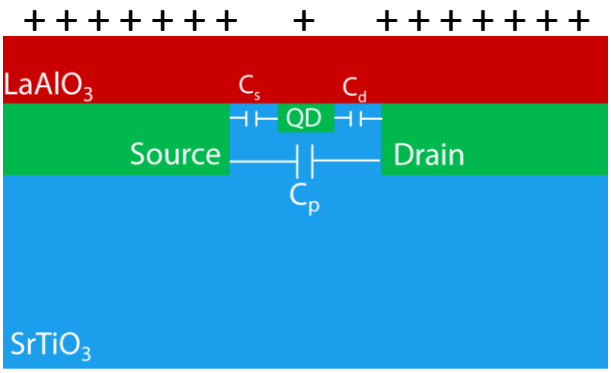

Figure 3.12 SketchSET capacitance model. The source and drain electrodes are coupled by a large parasitic capacitance (C_p~pF) that is strongly affected by single-electron charging of the QD (capacitance $C_{QD}=(C_s+C_d)$~40 aF).

3.7 CONCLUSION AND OUTLOOK

The unique properties of this ferroelectric SketchSET provide new opportunities for combining the ultrahigh electrostatic sensitivity of SET devices with ferroelectric-derived sensitivity at the nanoscale. Because all ferroelectric materials are also piezoelectric, a natural coupling between charge and nanomechanical motion is expected for the SketchSET. Furthermore, a variety of phenomena associated with the spin degree of freedom for single-electron devices(*51, 64*) is expected to hold for these devices. By integrating oxide heterostructures with silicon(*65*), it may be possible to integrate a ferroelectric SketchSET scanning probes that are capable of measuring charge and displacement *simultaneously* at the nanoscale(*66*). The existence of a ferroelectrically programmable SET constitutes a new type of nanoscale memory architecture which could be useful for low power, ultra-high density storage, if the charging energy and ferroelectric polarization could be made to persist to room temperature(*14, 15, 65*). The method for creating a single SketchSET is readily replicated as a 1D or 2D array which may find use in quantum dot-based quantum computation(*67*) or as a versatile solid-state "Hubbard toolbox"(*68*) capable of exploring new artificial quantum states of matter.

4.0 FERROELECTRIC FFIELD EFFECT TRANSISTORS ON SILICON

When the gate dielectric of a conventional metal-oxide-semiconductor field-effect transistor(*69*) (MOSFET) is replaced by a ferroelectric layer, the result is a ferroelectric field-effect transistor(*70*) (FeFET) where the channel conductance state is preserved even when the gate voltage is turned off due to the remnant polarization of the ferroelectric. Recently, room-temperature ferroelectricity was demonstrated in strained strontium titanate ($SrTiO_3$) thin films commensurately grown on and in intimate contact with silicon(*15*). This provides an attractive heterostructure for FeFET applications involving silicon, the backbone of semiconductor technology. In this chapter I will introduce the fabrication and characterization of FeFETs using this $SrTiO_3$/Si system utilizing different ferroelectric film thicknesses and silicon doping. We observe persistent channel conductance modulation of 85% at large gate bias voltages with a thinner silicon channel, and much longer retention time with a thicker, but still commensurate, $SrTiO_3$ film. The realization of this FeFET may improve the retention time in silicon-based nonvolatile ferroelectric memories(*71*), provide an advance for low-power transistor based logic applications(*72*, *73*) and enable high speed non-volatile neural networks(*74*).

4.1 INTRODUCTION

Ferroelectric field-effect transistors(*70, 75-77*) (FeFETs) offer a variety of applications, and are particularly promising candidates for non-volatile memory and logic elements related to the non-volatile information storage provided by the ferroelectric and non-destructive readout through the channel conductance. Ever since FeFETs were first proposed over fifty years ago(*70*), great efforts have been made utilizing numerous material systems including $SrCuO_2$/$Pb(Zr_{0.52}Ti_{0.48})O_3$ (PZT) heterostructures(*78*), all perovskite PZT/$La_{1-x}Ca_xMnO_3$ (LCMO) heterostructures(*79*), $BaTiO_3$/carbon natotube heterostructures(*80*) and organic heterostructures(*81, 82*). The integration of ferroelectrics with silicon has been extensively studied(*83-85*). Fully functional integration is hampered, however, by the lack of an intimate interface between the ferroelectric and silicon(*71*). Reaction between the ferroelectric layer and silicon, and the formation of interface trapping states(*86*) degrade the interface quality if ferroelectric materials are deposited directly on silicon. Another approach of inserting a buffer layer between the ferroelectric layer and silicon improves the interface quality, but at the price of increasing the turn-on gate voltage threshold to polarize the ferroelectric film(*71*). Most silicon devices work, however, at gate voltages $|Vg|<5$ V.

4.2 CHALLENGES IN SILICON FeFET

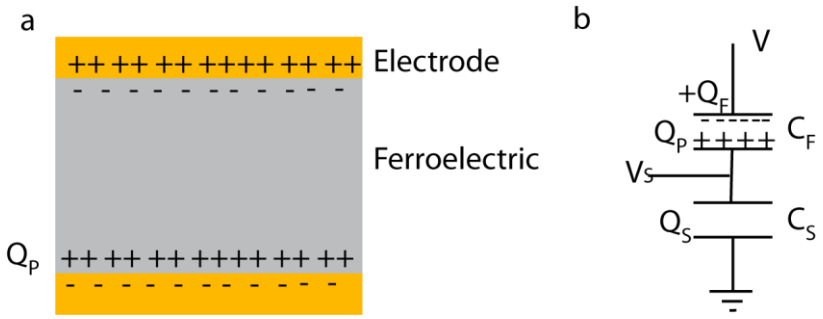

Figure 4.1 (a) Metal-ferroelectric-metal capacitor structure. (b) equivalent circuit model involving ferroelectric polarization.

T.P. Ma summarized two challenges of functional integration of ferroelectrics on silicon, the depolarization field(*87*) and gate leakage current(*88*). Both of the two lead to short retention time in previously studied FeFETs with silicon(*89*).

For a metal-ferroelectric-metal (MFM) structure, another candidate for non-volatile memory application using ferroelectrics, the ferroelectric polarization is completely screened by the metal electrode so that the ferroelectric polarization is stable (Fig. 4.1a). However if the bottom metal electrode is replaced by a semiconductor in a FeFET, there is always a depolarization field. As shown in Fig. 4.1b, the capacitor and charge of semiconductor is noted by C_S and Q_S. The voltage across the ferroelectric is

$$V_F = \frac{C_S V}{C_S + C_F} - \frac{Q_P}{C_S + C_F} \tag{4.1}$$

Where Q_P and C_F are the induced polarization charge and capacitance of ferroelectric film. When the external voltage is zero, we have

$$V = V_F + V_S = \frac{Q_F - Q_P}{C_F} + \frac{Q_S}{C_S} = 0 \tag{4.2}$$

and then the charge on the gate

$$Q_F = \frac{Q_P C_S}{C_S + C_F} \tag{4.3}$$

which leads to a depolarization field

$$E_{dp} = \frac{Q_P C_F}{\varepsilon(C_F + C_S)} \tag{4.4}$$

The other challenge is that the charge traps form at the interface between the ferroelectric and silicon if one directly deposits amorphous ferroelectric onto silicon. In the FeFET device the gate is usually leaky, especially when the ferroelectric film is very thin. So the charge traps can trap electrons due to this gate leakage current. The trapped electrons can locally depolarize the polarization. Assume the charge traps can trap electrons with a trapping probability α and the gate leakage current is I_{leak}. Then the retention time t for a polarization P is

$$t = \frac{P}{I_{leak}\alpha} \tag{4.5}$$

Ma also suggested a solution to these two challenges, which is to grow single crystal ferroelectric on silicon. With such a material system, one expects an ideal ferroelectric polarization with a square shaped *P-E* hysteresis loop. As far as the depolarization field does not exceed the coercive field, it will not depolarize the ferroelectric polarization. In the mean time, the lattice-matched interface is much cleaner in terms of charge traps so that the retention time can achieve an appreciable amount useful for real device applications.

4.3 A FERROELECTRIC FILM ON SILICON

Epitaxial strain is well known a way to produce or enhance ferroelectricity(*14*, *90*). As

introduced in Chapter 1.3, the strain can change the interatomic short-range and long-range forces to produce a net dipole moment in the central atom in the unit cell. One good example is $SrTiO_3$, which is not ferroelectric in bulk and turns ferroelectric when grown on various perovskite substrates. However, grow functional ferroelectrics on silicon has long term been a challenge since the silicon has a diamond shape crystal structure and most of ferroelectrics have other structures like perovskite. In the mean time the silicon surface is very reactive and silicon oxide may form easily if the ferroelectric film has a content of oxygen. Despite these challenges, $SrTiO_3$ thin film has been successfully grown on silicon using molecular beam epitaxy via a kinetically controlled process(*91*). Our collaborator at Cornell University was able to commensurately grow strained $SrTiO_3$ film using same method. Moreover, this strained film was found ferroelectric at above room temperatures when the thickness is below 10 monolayers (ML) in our previous work(*15*). The Curie temperatures for 5 ML and 6 ML are 320 K and 420 K respectively, which possibly means 6 ML is more stable than 5 ML.

This heterostructure fulfills Ma's suggestion to grow a single ferroelectric crystal on silicon and thus provides a possible route towards the development of silicon-based ferroelectric field effect devices. Here we report the development of prototype FeFET devices fabricated from ferroelectric $SrTiO_3$ grown on silicon-on-insulator (SOI) wafers. The thickness of the $SrTiO_3$ (5 and 6 ML) is constrained to be below the critical thickness at which it relaxes, and above the thickness for which room-temperature ferroelectricity is observed. Conducting channels are formed using both *p*-type (31 nm) and *n*-type (200 nm thick) silicon device layers, on top of which coherently strained $SrTiO_3$ films were grown using oxide molecular-beam epitaxy (MBE). The $SrTiO_3$ films were capped *in situ* with 20 nm iron and 25 nm gold. The following two sections are the details of sample growth and device fabrication method.

4.4 SAMPLE GROWTH

The $SrTiO_3$ films were grown on (001) oriented p-type (31 nm) and n-type (200 nm) silicon-on-insulator substrates by molecular beam epitaxy. Prior to the growth, the native SiO_2 layer was thermally removed by a strontium-assisted deoxidation process. An epitaxial (and commensurate) strontium titanate film was grown to the desired thickness (5 ML or 6 ML) by flux-matched codeposition of strontium, titanium and oxygen in installments of one or two molecular layers at a time at a substrate temperature of ~300 ℃ followed by a vacuum anneal to ~550 ℃. This growth process kinetically suppresses the reaction of forming SiO_2 and results in a commensurate $SrTiO_3$ film with an abrupt interface free of silicon oxide as discussed in Ref. (*15*). Details of the growth of $SrTiO_3$/Si, precise control of oxygen and temperature during growth and *in situ* and *ex situ* characterization of the $SrTiO_3$ film and the silicon-$SrTiO_3$ interface can be found in the supporting materials of Ref. (*15*). Following the growth of the $SrTiO_3$ layer, the sample was transferred in ultra high vacuum to a separate growth chamber where an epitaxial Fe layer of ~20 nm thickness was grown on the $SrTiO_3$/Si sample. The Fe layer was grown at a rate of ~0.1 Å/s at a substrate temperature of 300 ℃ and a chamber base pressure of 1×10^{-9} Torr. *In situ* reflection high energy electron diffraction (REED) measurements and *ex situ* x-ray diffraction measurements revealed the epitaxial relationship between the Fe, $SrTiO_3$ and Si to be Si[100] // $SrTiO_3$[110] // Fe [100] indicating that the Fe film grew 45 ° rotated to the in plane $SrTiO_3$ crystallographic directions. The Fe film provided an epitaxial conducting top electrode to probe the ferroelectricity of $SrTiO_3$. The Fe film was capped with a 25 nm gold layer before the sample was removed from the UHV environment of the growth chamber. The *in situ* Au film protected the Fe layer from oxidation and enabled making ohmic contacts to the gate electrode.

4.5 FeFET DEVICE FABRICATION

The FeFET devices were fabricated by standard photolithography and dry/wet etching techniques using the 5 ML $SrTiO_3$/31 nm p-SOI and 6 ML $SrTiO_3$/200 nm n-SOI wafers. The following three steps show the fabrication procedures of p-SOI wafer (Fig. 4.2), and similar procedures apply to the n-SOI wafer.

Channel isolation: At first a 250 um × 800 um silicon channel were defined by photolithography. Outside the silicon channel, the 25 nm top gold layer and 20 nm iron layer were etched away by wet etching (1 min in Transene gold etchant TFA and nickel etchant type I respectively). Then the exposed 5 ML $SrTiO_3$ layer and silicon layer was etched away by buffered HF (30 seconds) and RIE dry etching respectively. As a result, the SiO_2 box layer (green layer in Fig. 4.2a) was exposed to isolate the silicon channel.

$SrTiO_3$ film etching: after channel isolation, the second photolithography step was carried out to define source and drain areas (including the gaps between gate and source/drain). Following the same etching techniques, Au/Fe/$SrTiO_3$ layers were etched under these areas.

Electrodes deposition: Source, drain and gate areas were first defined with photolithography. Then a 100 nm thick aluminum film was deposited to form ohmic contacts to source and drain by sputtering. Finally a 60 nm gold protection layer was deposited. Note that in the gate area the structure counting from top is metal electrodes-5 ML $SrTiO_3$-silicon.

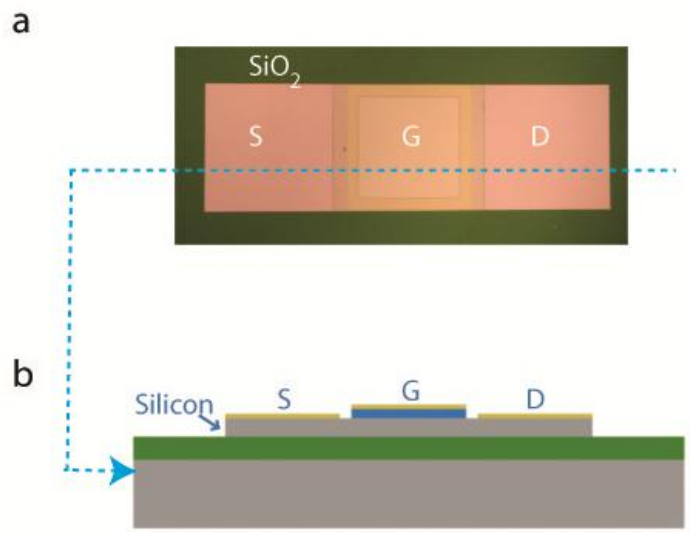

Figure 4.2 FeFET device schematic. (a) Optical graph of a FeFET device. The device is defined by three gold top electrodes and an isolated silicon channel. 5 ML (6 ML) strained $SrTiO_3$ film (blue color) connects the gate electrode and the silicon channel. All the electrodes are of 250×250 μm^2 size, the gaps between adjacent electrodes are 25 μmS, G and D refer to source, gate and drain electrodes. (b) Cross-section view. The blue layer under the gate electrode is $SrTiO_3$ layer.

4.6 MEASUREMENT

The results presented here are based on two representative devices (out of twelve fabricated): device A from the 5 ML $SrTiO_3$/31 nm *p*-SOI wafer and device B from the 6 ML $SrTiO_3$/200 nm *n*-SOI wafer. We applied electric characterization and PFM measurement to study the ferroelectric polarization and ferroelectric field effect.

4.6.1 *I-V* curves

Figure 4.3a shows the FeFET device geometry and measurement setup. The $SrTiO_3$ layer under the source and drain electrodes was etched away so that only the gate electrode has a $SrTiO_3$ film underneath. Figure 4.3b shows the differential current-voltage (differential *I-V*) curves for the silicon channel of device A under different poling conditions for the ferroelectric $SrTiO_3$ film. At a given source-drain bias V_{sd}, the gate was pulsed for 10 seconds with either +5 V or -5 V, and the subsequent drain current was measured one second after the gate voltage was turned off. The existence of two distinct conductance modes in the differential *I-V* curves of +5 V and -5 V gate poling voltages suggests that the channel conductance modulation arises due to the reorientation of the ferroelectric polarization, i.e., a ferroelectric field effect.

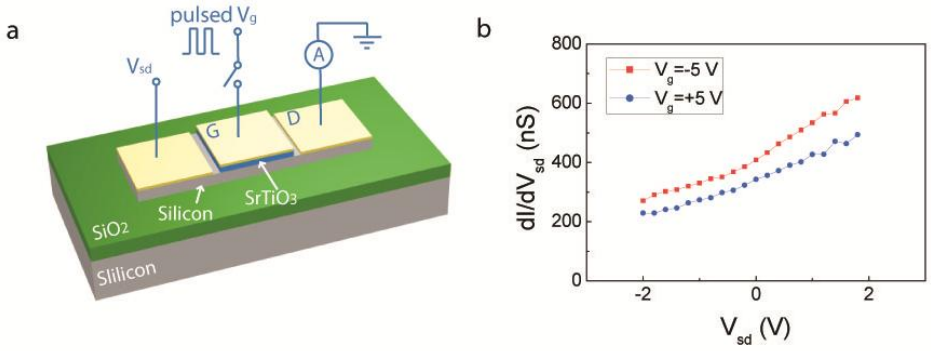

Figure 4.3 Measurement setup and *I-V* curves. (a) Differential *I-V* measurement circuit. (b) Differential *I-V* curves of the silicon channel in device A (5 ML $SrTiO_3$/31 nm p-SOI). Each source to drain current was measured after pulsing either +5 V (red squares) or -5 V (blue circles) poling gate biases V_g for 10 seconds, as shown in the measurement circuit in (a). The dI/dV_{sd} values were calculated subsequently. The difference between the two curves shows the ferroelectric field effect.

4.6.2 PFM measurement

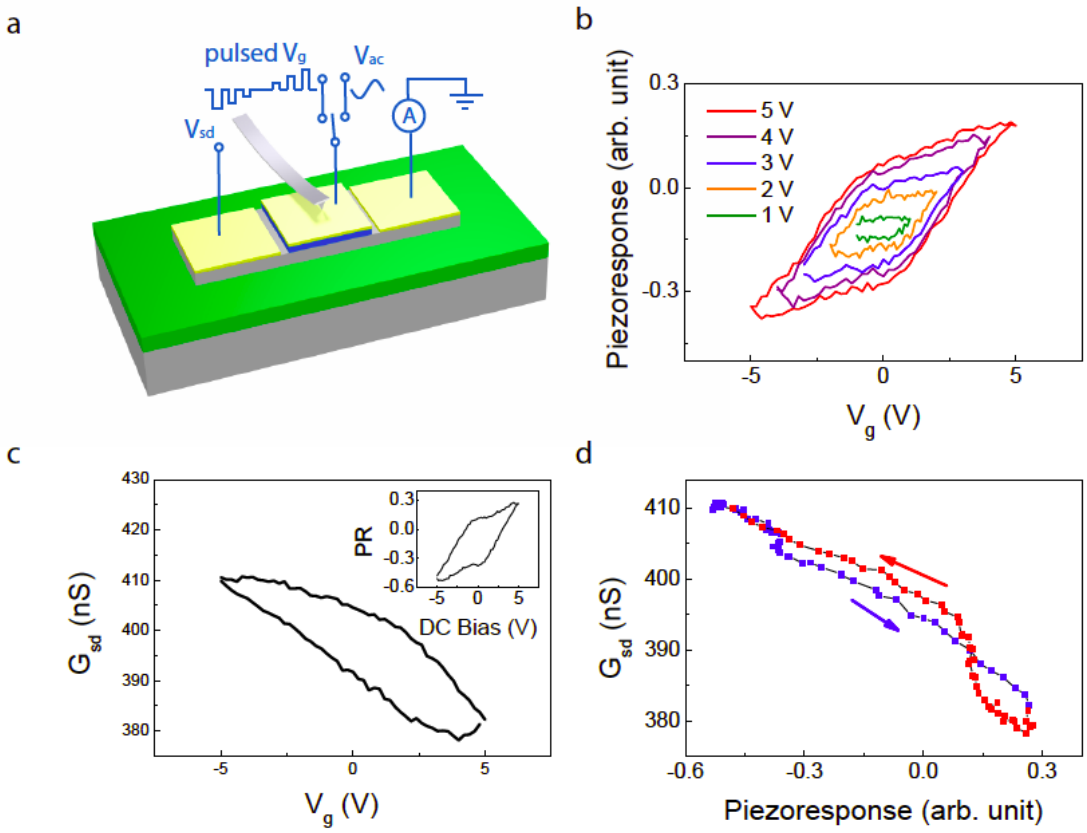

Figure 4.4 Piezoresponse force microscopy study of the 5 ML $SrTiO_3$ film. (a) Measurement circuit diagram. Pulsed poling biases were applied to the gate with maximum amplitudes from 1 V to 5 V. After each pulse, the gate bias was switched to a small AC bias for PFM measurement, then it was turned off to measure channel conductance G_{sd}. (b) Ferroelectric hysteresis loops of device A obtained by PFM with poling amplitudes from 1 to 5 V. (c) Channel conductance G_{sd}. The hysteretic behavior indicates the field effect caused by the remnant ferroelectric polarization field. Inset: The hysteresis loop simultaneously acquired by PFM. (d) Parametric plot of PFM signal with channel conductance in (c).

The ferroelectric nature of the strained $SrTiO_3$ film in the gate layer was investigated using piezoresponse force microscopy(*92*) (PFM). Full technical detail can be found in section 2.4. The AFM cantilever tip (~25 nm tip radius) was touched down in contact mode directly on the gate electrode (Fig. 4.4a), and mechanical displacement of the top electrode due to the piezoresponse in the ferroelectric layer was sensed by measuring the deflection of the laser beam focused on the cantilever for AFM feedback. These PFM measurements are similar to those previously reported(*15*), except that here the AFM tip is electrically isolated and does not couple electrostatically to the $SrTiO_3$ film surface. Rather, the electrical driving of the $SrTiO_3$ film is achieved by directly contacting the top gate electrode. The piezoelectric response of device A (5 ML $SrTiO_3$, *p*-type silicon) as a function of gate voltage (Fig. 4.4b) exhibits a negative offset, consistent with a preferred upward polarization, opposite in sign to that reported previously for ferroelectric $SrTiO_3$ grown on *n*-type silicon(*15*).

To establish a more direct correlation between ferroelectric field effect and piezoresponse, we fixed the source-drain voltage V_{sd}=0.5 V, and simultaneously measured the channel current and piezoresponse while sweeping the pulsed poling biases back and forth (Fig. 4.4c). The hysteretic behavior of the channel conductance shows 8% conductance modulation, corresponding to sheet carrier densities change from 6.5×109 cm^{-2} to 7.1×109 cm^{-2} as a result of ferroelectric field effect(*93, 94*). A parametric plot of piezoresponse and channel conductance as a function of gate bias (Fig. 4.4d) shows an expected linear dependence of channel conductance on piezoresponse. Some local variations are observed, which are attributed to differences between the piezoresponse measurement (which is local) and the channel response that is sensitive to the net polarization over the channel area.

4.6.3 Retention measurement

To determine the temporal stability of poled ferroelectric states, poling pulses with various pulse widths t_p (100 ms to 10 s) and amplitudes (5 V to 40 V) were applied to the gate to polarize the $SrTiO_3$ film, while the channel conductance was monitored as a function of time. Figure 4.5a,b shows the retention behavior of devices A and B, respectively. A positive pulse depletes carriers in the *p*-type silicon channel, reducing the conductance. For the *n*-type silicon channel, the effect is reversed due to the change in carrier sign. For both *n*-type and *p*-type channels, we find that the high-conductance state is more stable than the low-conductance state. That is to say, the down polarization is more stable for the *n*-type channel, while the up polarization state is more stable for the *p*-type channel. We attribute this channel-dependence of the polarization stability to the ability of the carriers to a back-action or reverse field-effect of the carriers on the ferroelectric itself. The more stable state is the one in which the ferroelectric polarization is screened by the carriers in the channel, regardless of their sign.

Figure 4.5c shows the conductance modulation ratios observed for two of the devices (device A and B) as a function of gate bias amplitudes. We define the conductance modulation ratio $r = \frac{G_{max} - G_{min}}{G_{max}}$, where G_{max} and G_{min} are the maximum and minimum channel conductance measured 3 seconds after poling voltages of different signs, respectively. For the 31 nm *p*-type silicon channel (device A), +5/-5 V poling voltages can induce ~7% conductance modulation, and larger +30/-30 V can achieve a modulation ratio as large as 85%. Despite having a more stable ferroelectric state for 6 ML $SrTiO_3$ film(*15*), the conductance modulation of the 6 ML $SrTiO_3$ film on 200 nm *n*-silicon device (device B) is significantly smaller. This is presumably because the silicon channel is much thicker. Hence the apparent ferroelectric field effect over

the entire channel is smaller.

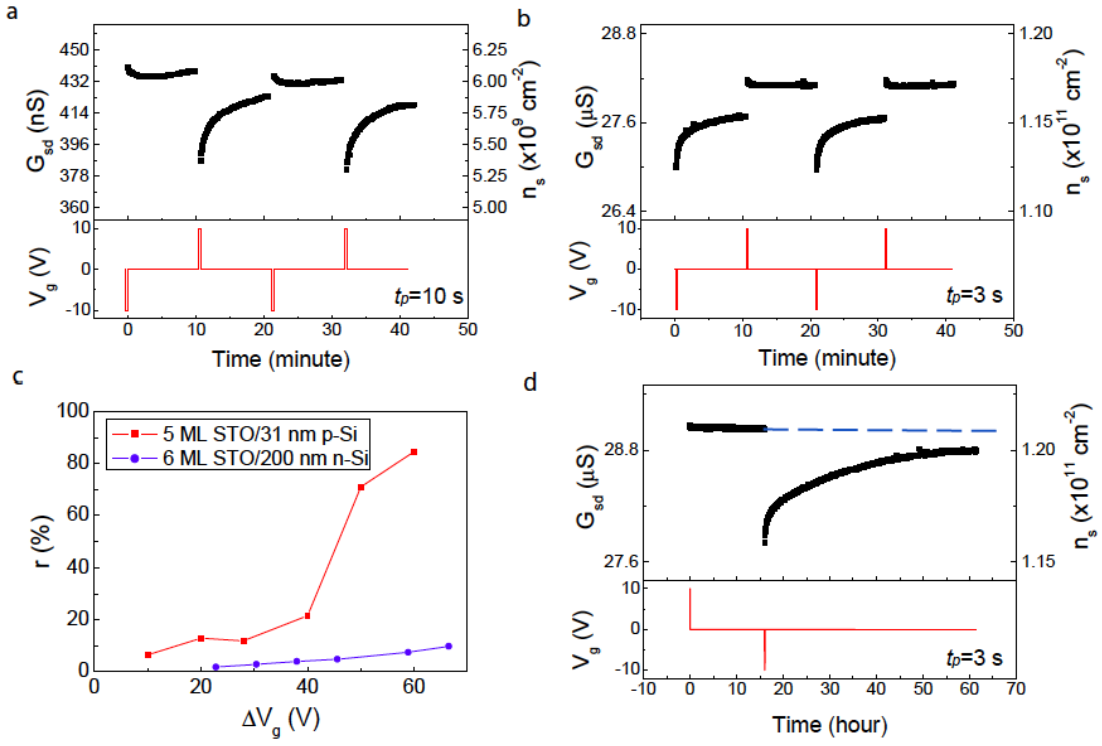

Figure 4.5 Device performance of FeFETs on p-type and n-type silicon. (a) Channel conductance of device A (5 ML $SrTiO_3$/31 nm p-SOI) monitored for 10 minutes after -10/+10 V poling gate pulses (t_p=10 s). 13% conductance modulation ratio was achieved. Bottom: Poling pulse sequences. (b) Channel conductance of device B (6 ML $SrTiO_3$/200 nm n-SOI) monitored for 10 minutes after +40/-30 poling gate pulses (t_p=3 s), showing 12% modulation. c, Conductance modulation ratios of p-type and n-type FeFETs at different poling amplitudes $\Delta V_g = V_+ - V_-$, where V+ (V-) is the positive (negative) bias. (d) Retention study of device B. Channel conductance was first measured for 12 hours after a single 10 V poling pulse, then measured for 46 hours after a -10 V poling pulse. 30% modulation of initial value was preserved after 46 hours. The dashed line is a guide for eyes for the stable high conductance mode.

When the poling pulse width t_p is shorter than 100 ms, we do not observe a ferroelectric field effect. This is mainly due to the large capacitance between the gate and silicon channel. For applications, the device can be downsized to <100 nm, which will decrease the charging time

by 7 orders of magnitude. Thus the response time of a scaled FeFET is expected to be of order ~10 ns.

Retention of the ferroelectric state is significantly longer for the 6 ML $SrTiO_3$ film than for the 5 ML $SrTiO_3$ film. State retention measurements (Fig. 4.5a) on device A, measured via the ferroelectric field effect, show the channel conductance modulation drops to approximately 20% of its initial value after 10 minutes. By contrast, the 6 ML $SrTiO_3$ film, the high conductance state did not change in 24 hours within the error of thermal drift. The channel conductance modulation ratio retained approximately 30% of its initial value after 46 hours (Fig. 4.5d), when the decaying low conductance mode reached a stable value.

4.6.4 Vertical tunneling

In addition to the observed ferroelectric field effect and piezoresponse of the devices, electronic transport through the $SrTiO_3$ film between the silicon channel and gate electrode has also been characterized. In such a measuring geometry (Fig. 4a), the FeFET behaves as a metal-ferroelectric-semiconductor (MFS) tunnel junction(*95*). A low AC tunneling current was measured 3 seconds after a sequence of increasing and decreasing values of V_g (Fig. 4b). Clear hysteresis in the tunneling current was observed, unveiling 2% modulation of tunneling conductance by polarization switching in this device. Other devices showed much larger modulation (as high as 30%), and the overall magnitude is expected to depend sensitively on electrical shorts through the large-area $SrTiO_3$ gate. These results appear to be consistent with the mechanism described by Gajek *et al.*(*96*), in which the ferroelectric polarization modulates the Thomas-Fermi screening length in the silicon channel, thus modifying the effective barrier width and altering the tunneling conductance(*26*, *97-99*).

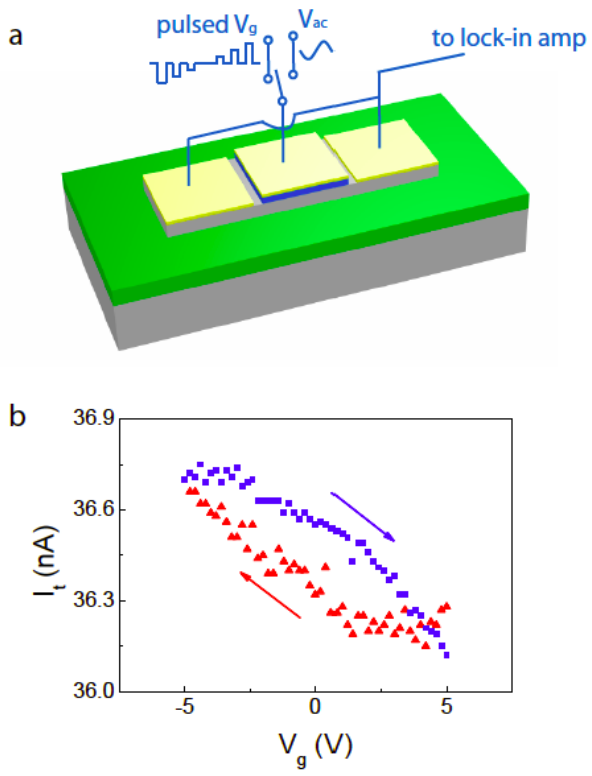

Figure 4.6 Tunneling behavior of the metal-SrTiO3-Si tunnel junction in device A. (a) Measurement circuit diagram. Poling gate bias *Vg* was pulsed and swept in the same manner as Fig. 4.4a. The source and drain electrodes were connected together as a back silicon contact. Small AC bias (100 Hz, 10 mVrms) was applied after *Vg* was turned off, and subsequent tunneling current was measured by a lock-in amplifier connected to the silicon contact. (b) Hysteretic tunneling current shows the tunneling barrier width is modulated by the ferroelectric polarization.

4.7 SUMMARY AND FUTURE WORK

In summary, we fabricated and characterized FeFETs using strained $SrTiO_3$ thin films on *p*-type and *n*-type SOI wafers. A direct correlation between hysteretic piezoresponse of the ferroelectric $SrTiO_3$ and modulation of the channel conductance in the silicon demonstrates the direct ferroelectric field effect. A converse effect, namely, the higher stability of ferroelectric polarization that can be screened by carriers in the silicon, further confirms the strong interplay between these two materials that have been carefully brought into intimate contact to form an atomically abrupt interface using oxide MBE. The results demonstrated here represent an important advance toward the development of transistor-based memory and logic capable of retaining its logical state in the absence of power. Such devices may be compatible with conventional silicon fabrication methods. We note also that ferroelectric gate capacitors similar to the ones investigated here have been proposed for the creation of ultra-low threshold field-effect devices(*72, 99*). Further improvements to the existing structures may be achieved by incorporating standard techniques used in MOSFETs such as complementary doping of source and drain silicon contacts.

5.0 NANOSCALE CHARACTERIZATION BY MICROWAVE CAPACITANCE SENSING

The capacitance is a basic electronic measure of dielectric properties of devices and materials. It gives out the information how well the device or material can hold electrons and store energy. At nanoscale, however, the capacitance is hard to measure due to the ultra-small value. For example, the capacitance of a single self-assembled quantum dot is about several attofarad (aF, 10^{-18} F), which is beyond the ability of any commercial capacitance meters. In this chapter, we use the microwave capacitance sensing technique similar to the RCA capacitance sensor introduced in Section 2.1 to measure the capacitance of self-assembled quantum dots. We also integrate this capacitance sensor to AFMs to enable microwave imaging of sample dielectric properties. This developed technique provides a novel probe for nanoscale electronic characterization besides conductivity measurement.

5.1 MICROSTRIP CAPACITANCE SENSOR

The developed capacitance sensor is based on a microstrip coplanar waveguide that has higher resonance frequency than the RCA capacitance sensor. Other than this, the operating mechanism is similar. As shown in Fig. 5.1a, a microwave signal generator (Wiltron 6668B) feeds ~1.8 GHz microwave signal whose amplitude is modulated at 1 KHz into one side strip of the coplanar waveguide, and this signal is coupled via a gap to the center strip, i.e. the resonator, whose resonance frequency is perturbed by the capacitance of the sample attached to the resonator. The sample is biased by a DC plus AC voltage through an inductor that serves as a RF choker. The AC bias has the same frequency as the microwave amplitude modulation frequency. The power of transmitted microwave signal is detected at the other side strip through a microwave peak detector which we either use a commercial schottky diode detector (Agilent 8373B) or a home-made detector. Finally the voltage output from the peak detector is measured by the lock-in amplifier, which gives out the S_{21} parameter of resonator microwave response.

The resonator was fabricated on a high frequency PC board (Rogers Corporation RO3003, 1.5 mm thick, dielectric constant 3.0) using standard PC board etching technique. The side strips (3.8 mm wide) have 50 Ω characteristic impedance to match the impedance of coaxial cables to minimize microwave reflection. Decreasing the gap width will increase the coupling efficiency from the side strips to the resonator, however it will decrease the quality factor of the resonator. A practical design chooses a trade-off (2.5 mm) between coupling efficiency and quality factor. The resonator works on a quarter-wave mode, and the length of the center strip mainly determines the resonance frequency (24.9 mm for 1.8 GHz resonance frequency). The whole structure is small enough to fit in the AFM for scanning microwave microscopy.

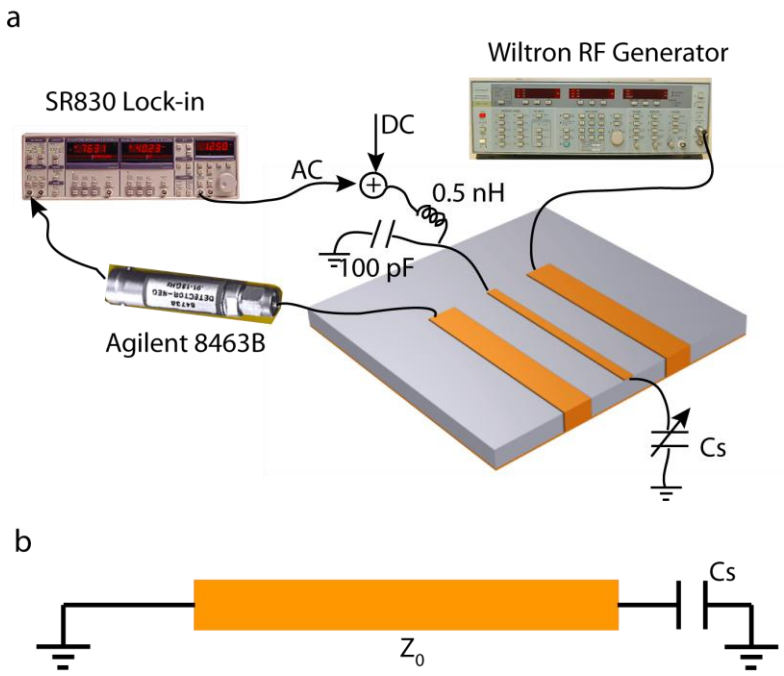

Figure 5.1 Microwave capacitance measurement based on a microstrip resonator. (a) Microstrip resonator and measurement setup. (b) Transmission line model with a capacitive sample attached.

When the resonator is terminated with a capacitor (Fig. 5.1b), the resonance condition is the reactance Im(Z_{in})=0. Recall equation (1.2.15) for the input impedance of a lossless transmission line terminated with a load, we have the resonance equation

$$Im(Z_{in}) = Im(Z_0(\frac{Z_R \cos\beta l + jZ_0 \sin\beta l}{Z_0 \cos\beta l + jZ_R \sin\beta l}))$$

$$= -\frac{\cos\beta l}{\omega C} + Z_0 \sin\beta l = 0 \qquad (5.1)$$

where $Z_R = \frac{1}{j\omega C}$, and $\beta = \frac{2\pi f}{v}$ with v the velocity of microwave in the dielectric. Rearrange the above equation we have

$$\tan\beta l = 1/\omega C Z_0 \qquad (5.2)$$

Assume the resonant frequency of an unloaded resonator is f_0 so that $(\beta l)_0 = \frac{2\pi f_0}{v} = \frac{\pi}{2}$ since the electrical length is $\frac{\pi}{2}$ at resonance. Then the electrical length of a loaded resonator is

$$\beta l(f) = \frac{2\pi f}{v} = \frac{\pi}{2}\frac{f}{f_0} \tag{5.3}$$

From equations (5.2) and (5.3) we can infer the capacitance value *C* is

$$C = \frac{1}{2\pi f Z_0 \tan\frac{\pi f}{2f_0}} \tag{5.4}$$

Differentiate equation (5.2) on both sides we will get the *frequency sensitivity*

$$\frac{df}{dC} = -\frac{1}{1+\beta l(\tan\beta l+\cot\beta l)}\frac{f}{C} \tag{5.5}$$

Plug the electrical length βl and capacitance *C* values from equations (5.3) and (5.4) into (5.5) we have the final form for the frequency sensitivity

$$\frac{df}{dC} = -\frac{2\pi f^2 Z_0 \tan(\frac{\pi f}{2f_0})}{1+\frac{\pi f}{2f_0}(\tan(\frac{\pi f}{2f_0})+\cot(\frac{\pi f}{2f_0}))} \tag{5.6}$$

This frequency sensitivity is a figure of merit measuring how sensitive the resonator can respond to the capacitance change. The negative sign in *df/dC* suggests that larger capacitance will decrease the resonant frequency. To calibrate the frequency sensitivity, a varactor (On Semiconductor, MMBV3102LT1G) and a 0.1 pF capacitor were connected in series to the resonator, as shown in Fig. 5.2(a). By tuning the varactor from 4 pF to 30 pF, which corresponds to an overall series capacitance ranging from 97.56 fF to 99.67 fF, the resonant frequency shifts from 1573.5 MHz to 1566.6 MHz, as shown in Fig. 5.2(b). The frequency sensitivity *df/dC* in this operating region is then determined as 3.3 MHz/fF through these results. The overall sensitivity *dV/dC* can de decomposed to two parts,

$$\frac{dV}{dC} = \frac{dV}{df}\frac{df}{dC} \tag{5.7}$$

The voltage sensitivity *dV/df*, which is a figure of merit of the peak detector, gives the voltage response due to a change in frequency and is determined by measuring the slope of the resonance curve at the working frequency. For fixed input power -20 dbm, the voltage

sensitivity is about 12.5 μV/MHz at -3 db points on the slopes of the resonance curves. Given an overall measured system noise level $V_{noise} = 25\ nV/\sqrt{Hz}$ at 1 KHz, the system sensitivity is calculated to be $\delta C = \frac{V_{noise}}{df/dC \cdot dV/df} = 6.1 \times 10^{-19}\ F/\sqrt{Hz}$.

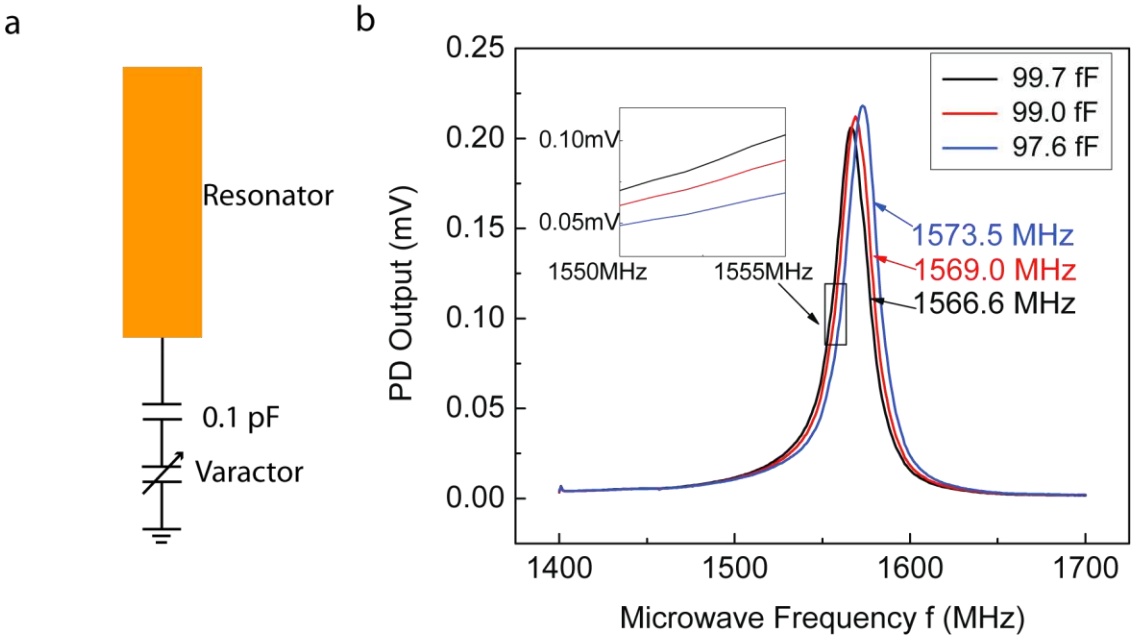

Figure 5.2 Frequency sensitivity measurement. (a) Experiment setup. A 0.1 pF capacitor and a varactor are connected in series to control a small capacitance change. (b) Resonance curves at different capacitance.

5.2 CAPACITANCE SENSING OF SELF-ASSEMBLED QUANTUM DOTS

Self-assembled quantum dots (SAQDs) have achieved extensive interests on potential applications in spin-based quantum information technologies due to their atomic-like quantized energy levels, scalability, and relatively long coherence times. Single spin detection and manipulation in SAQDs have been successfully performed optically using Faraday and Kerr rotation techniques(*100-103*). In those works, single spins are addressed by a laser spot of ~1

μm size and manipulated by picosecond laser pulses in a very low density SAQDs sample. An all-electrical means of information processing that does not require optical preparation, manipulation and interrogation methods may render a particular device more functionality and better perspectives insofar as integration is concerned. One way to electrically address and control single spins is to use a nanometer-scale metallic probe as a top gate and measure the quantum capacitance as a figure of merit for controlling the charge states of electrons in SAQDs.

The capacitance of a single SAQD is normally on the order of 10^{-18} F. Within this regime, conventional capacitance sensors like L-C circuits and capacitance bridges are not sensitive enough. A configuration with leads to a device containing very few SAQDs would also exhibit a parasitic capacitance orders of magnitude larger than the SAQDs capacitance themselves. Using the microwave capacitance sensor would circumvent the stray capacitance and provides the high resolution needed.

5.2.1 Sample growth

Here we investigate the capacitance-voltage characteristics of Metal-Insulator-Semiconductor devices containing SAQDs by a microwave capacitance sensor mentioned above. The samples are grown by molecular beam epitaxy (MBE), consisting of an undoped 1000 nm-thick GaAs buffer layer grown at 600 °C under an As flux of 10^{-6} Torr, followed by an 80 nm Si-doped back contact layer with a nominal concentration of ~$1x10^{18}$ cm^{-3}. The temperature is then lowered to 530 °C, and an undoped GaAs tunneling barrier of thickness t_b=16 nm separates the InAs SAQDs from the back contact. The InAs QDs are subsequently grown by pulsing the In flux at an effective growth rate of 0.01 ML/s until island nucleation. The typical QD density is about $1x10^{10}$ cm^{-2}. Then a 6 nm thick strain-reducing layer (SRL) of

$In_{0.2}Ga_{0.8}As$ is deposited over the SAQDs. At last, an undoped GaAs cap layer is grown and the temperature is ramped up to 600 °C(*104*). Schottky and ohmic contacts with an area of 200×200 μm^2 are also defined by conventional optical lithography processes.

5.2.2 Experiment setup

The experiment setup is similar as shown Fig. 5.1a. The resonant frequency is about f_0=1.85 GHz unloaded (i.e., no sample attached). Connecting the sample directly causes too large of a resonance frequency shift due to the large device capacitance, so a C_0=0.1 pF series capacitor is used to desensitize the resonator. The resonant frequency shifts by about 250 MHz when this capacitor is attached. Operating frequencies between 1.4 GHz to 1.8 GHz are optimal for achieving high measurement sensitivity. A –20 dbm RF signal with fixed frequency is fed from one side of the resonator and the transmitted power is measured by a broadband schottky peak detector (Agilent 8473B) in the other side. A low input RF power is preferred to prevent sample heating. The top gate of the SAQDs structure is connected in series to the 0.1 pF capacitor, which is in turn connected to the central resonator microstrip. The capacitance change ΔC in SAQDs caused by quasi-static DC bias will be also reduced by a factor of $(C_0/C_q)^2$, where C_q is the capacitance of quantum dots. Assuming a typical C_q=10 pF of this sample device, the capacitance change seen by the resonator will be $1/10^4$ of the original quantum capacitance variation. A DC bias voltage with a small AC modulation (10 KHz, 0.05 V_{rms}) is applied through a 100 nH inductor, which can let low frequency AC modulation pass through while still blocking the RF transmission. The output of the peak detector is lock-in detected at 10 KHz modulation frequency. This type of modulation gives a low frequency perturbation on microwave capacitance and the resulting differential dC/dV_b curve can be integrated to yield the

microwave *C-V* response.

5.2.3 Low frequency measurement

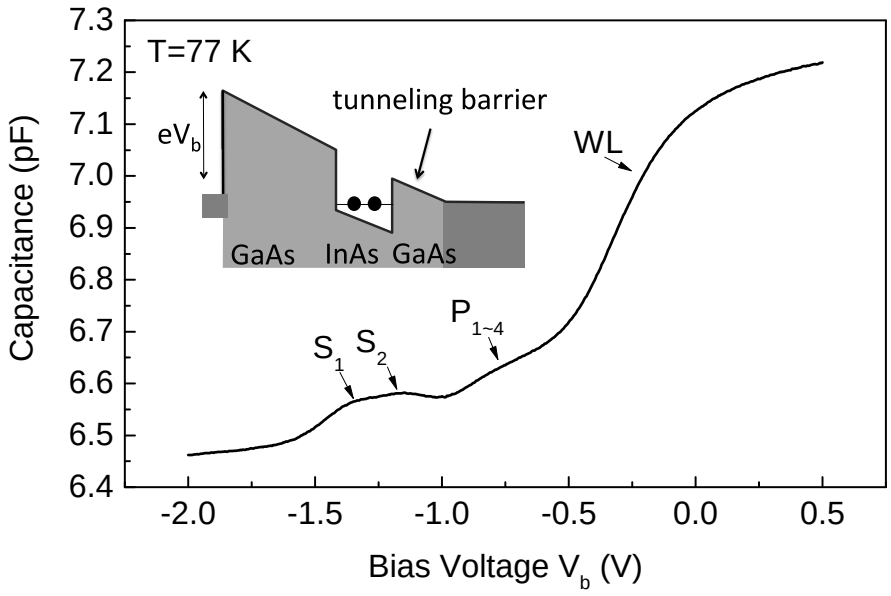

Figure 5.3 Low frequency *C-V* curve. Two *S* states *S*1 and *S*2 are located at -1.365 and -1.165 V. *P* states are degenerated due to SAQDs size dispersion and 106 number of dots probed. The inset shows the band diagram of the SAQDs.

As a reference, we first investigate the conventional low-frequency capacitance-voltage (C-V) spectrum by sweeping the DC voltage V_b with a small AC modulation V_{ac} of frequency f_m, and measuring the in-phase and out-of-phase responses with a dual-channel lock-in amplifier(*105*). Figure 5.3 shows a C-V curve obtained at f_m=5 kHz and temperature T=77 K. The two s-shell states are readily resolved at DC bias voltages V_{s1}= –1.365 V and V_{s2}= –1.165 V respectively. The four p-shell states are located between –0.9 V and –0.5 V, and are not individually resolvable owing to peak broadening caused by quantum dot size dispersion and the large number of dots probed(*106*).

5.2.4 Microwave frequency measurement

The microwave capacitance of SAQDs sample with 16 nm thin tunneling barrier is then measured at T=10 K in a He flow cryostat. Using similar voltage bias scheme as the low frequency measurement, DC bias V_b plus 0.05 V_{rms} AC voltage modulation is applied via the RF choke. To determine the working microwave frequency, V_b is set to –0.3 V, where a maximum slope dC/dV_b is expected according to the low frequency C-V curve (Fig. 5.3). Under this condition, the microwave frequency is then swept to obtain a differential resonance curve dV/df with f the microwave frequency, as shown in the inset of Fig. 5.4a. Two types of information can be extracted from this curve. First it provides a signature for the sensitivity of the resonator. Failure in seeing this curve means the resonator cannot sense the frequency shifts caused by the small AC voltage modulation. In the mean time as a second order effect, it can also represent a loading of the cavity, due to a leaky sample or a sample with very large capacitance. That is why the C_0 capacitor is so important to fine tuning the set up. Secondly, the microwave working frequency can be set at the two extreme values of this curve, which indicate optimal sensitivities. Once the working frequency is determined, the bias voltage V_b is then swept, resulting in a differential dC/dV_b curve (Fig. 5.4a), which can be integrated to obtain the microwave C-V spectrum, as shown in Fig. 5.4b. After a quick comparison between Fig. 5.3 and Fig. 5.4b, a conclusion can be drawn that the C-V spectra are almost frequency independent from KHz to GHz regime for this SAQDs sample, which contrasts previous results with thicker tunneling barriers(*105*). In a similar measurement for SAQDs sample with a thicker barrier of 40 nm, we can't even retrieve the differential resonance curve, which indicates that the tunneling barrier thickness strongly influences the microwave response of the electrons since the tunneling time is exponentially dependent on tunneling barrier thickness

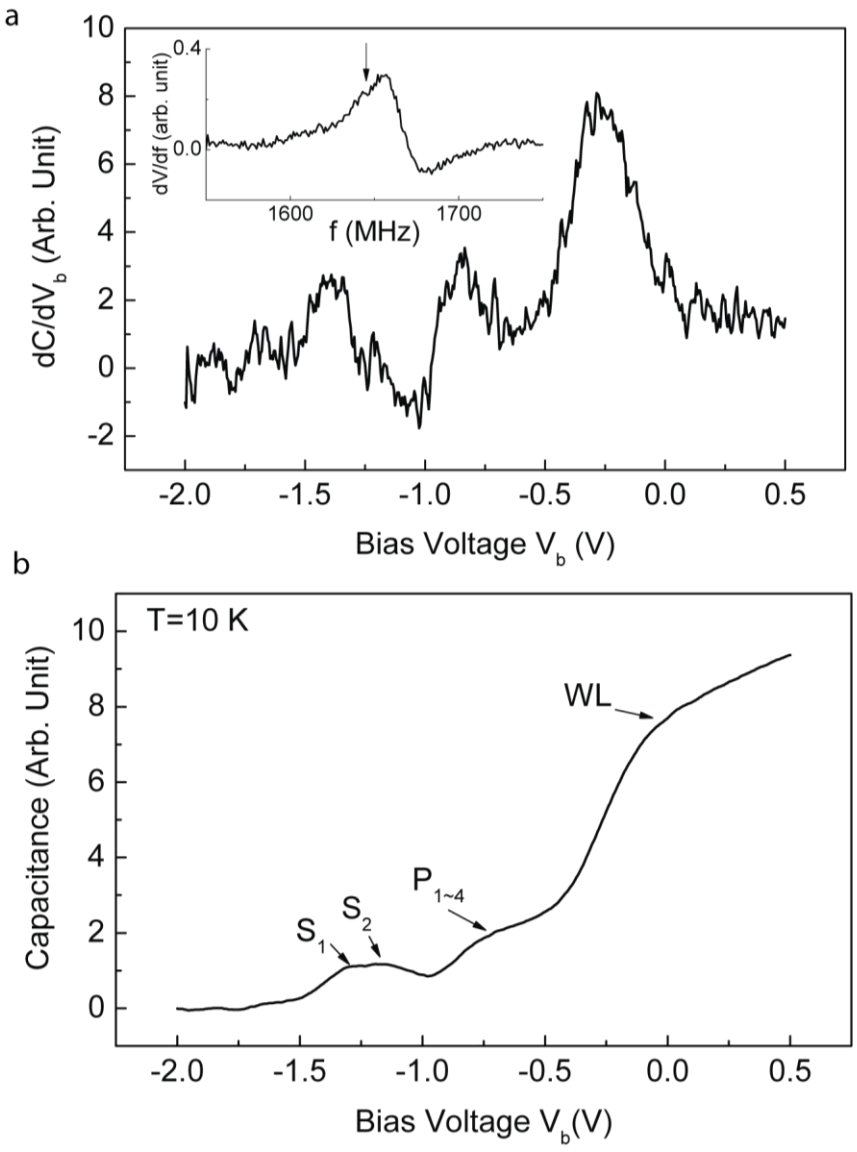

Figure 5.4 Microwave C-V spectroscopy. (a) Differential dC/dV_b curve obtained by lock-in detecting the ac modulation frequency. This curve shows the slope of conventional *C-V* curve. The inset shows the differential resonance curve of the resonator. The arrow indicates the working frequency 1650 MHz chosen in this experiment. (b) *C-V* curve recovered by integrating the dC/dV_b curve in (a).

5.2.5 Summary and future work

In summary, we utilize a microstrip resonator based capacitance sensor to measure SAQDs capacitance at microwave frequencies. By comparing with a low frequency *C-V* curve, we see that the spectra are frequency-independent owing to the very thin tunneling barrier of this SAQDs sample. The sensitivity of the microstrip capacitance sensor is in the order of 10^{-19} F/$\sqrt{\text{Hz}}$, which can be further improved by using the latest microwave power detectors, and is enough to probe the capacitance of a single quantum dot (~10^{-18} F). The sensitivity of this technique is also "tunable" by adjusting the series capacitance C_0, provided that the overall capacitance of the sample is not too large. This technique can be used in conjunction with a low temperature scanning force microscope(*107*) to obtain high-resolution images of the microwave response by connecting a cantilever or tuning fork force sensor (with a sharp tip) to the resonator, and can also be used to gate SAQD structures at these frequencies, with the ultimate goal of electrically sensing and controlling a single SAQD.

5.3 SCANNING CAPACITANCE IMAGING OF q-2DEG NANOSTRUCTURES AT $LaAlO_3/SrTiO_3$ INTERFACE

Utilizing conductive AFM lithography, we have been successful in creating on demand nanoscale devices at the 3 uc $LaAlO_3/SrTiO_3$ interface, as introduced in Chapter 3. However, these devices are made of a thin sheet of electrons and are virtually invisible from the mainstream microscopes including AFM, SEM and TEM. An imaging capability for these nanostructures is highly desirable for device characterization. Kelvin probe force microscope

(KPFM) images the surface potential using an AFM at non-contacting mode. The best resolution we can get is around 100 nm (unpublished), far beyond the size of nanostructures (<10 nm) created at the $LaAlO_3/SrTiO_3$ interface. Integrating the microwave capacitance sensor with an AFM, it is possible to observe the microwave response between AFM tip and nanostructures, thus leading a way to image the q-2DEG nanostructures.

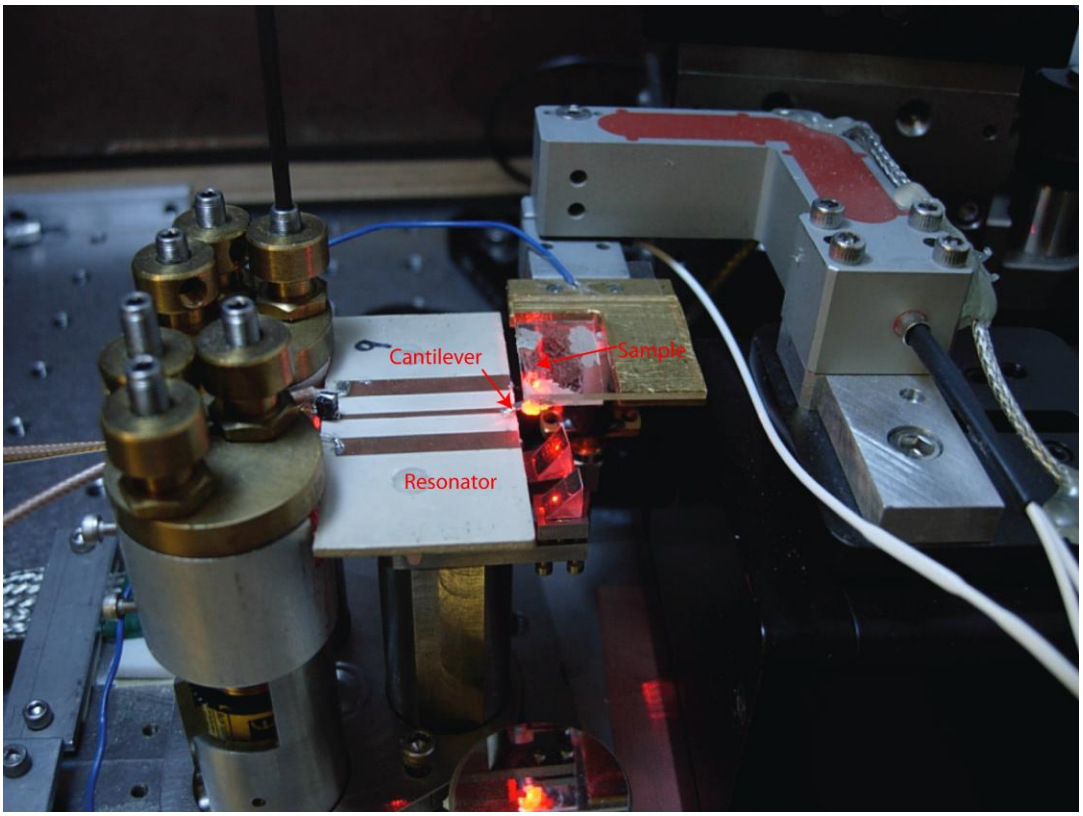

Figure 5.5 A home-made Scanning microwave microscope setup.

Here we used a similar design as Ref. (*108*) to integrate with the microwave capacitance sensor with a home made AFM. Full instrumentation detail can be found in Appendix. As shown in Fig. 5.5, an AFM cantilever is attached to the resonator to sense the capacitance between the tip and sample during the scan. Regular cantilever tip with thin metal coating (typically 20 nm platinum) will not couple microwave since the metal thickness is well below the skin depth. A full metal probe with high aspect ratio is desired to localize microwave at the tip

apex and minimize the stray capacitance between tip holder and sample surface. In our approach, we used a home made tungsten tip to conduct preliminary tests. However we do not have AFM feedback with this tip by lacking a flat and highly reflective surface to focus detection laser beam. Instead, we monitored the microwave signal (Fig. 5.6) to prevent the tip from crashing while approaching the surface.

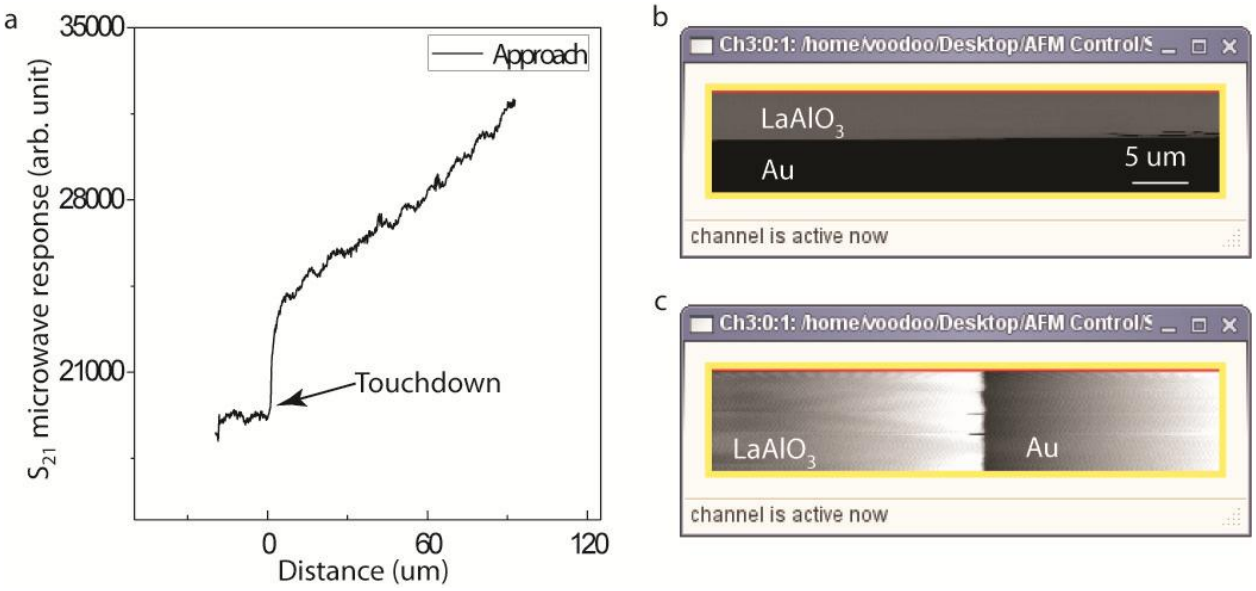

Figure 5.6 Microwave Imaging. (a). Microwave approach curve. (b) Microwave imaging of sample surface with gold and $LaAlO_3$. (c) Scan rotation is rotated by 90° with respect to (b), further confirms microwave contrast between electrode and dielectric.

During the operation, we set the working microwave frequency to the one with maximum slope on the resonant curve. Then an "L" shape tungsten tip is approached to the $LaAlO_3/SrTiO_3$ sample surface. The S_{21} microwave response is monitored in real time, and a big drop in the microwave signal is a signature of tip touchdown (Fig. 5.6). During the scan, any capacitance change between will cause a resonant frequency shift, which is mapped out by the voltage signal in the peak detector. Figure 5.6b,c shows the microwave imaging of sample surface with gold electrode and $LaAlO_3$ dielectric. The microwave contrast between the electrode and dielectric

provides a promising future for imaging q-2DEG nanostructures. However due to lack of a good force sensor and a mediocre performance of the peak detector (-50 db sensitivity), we have not achieved this goal yet.

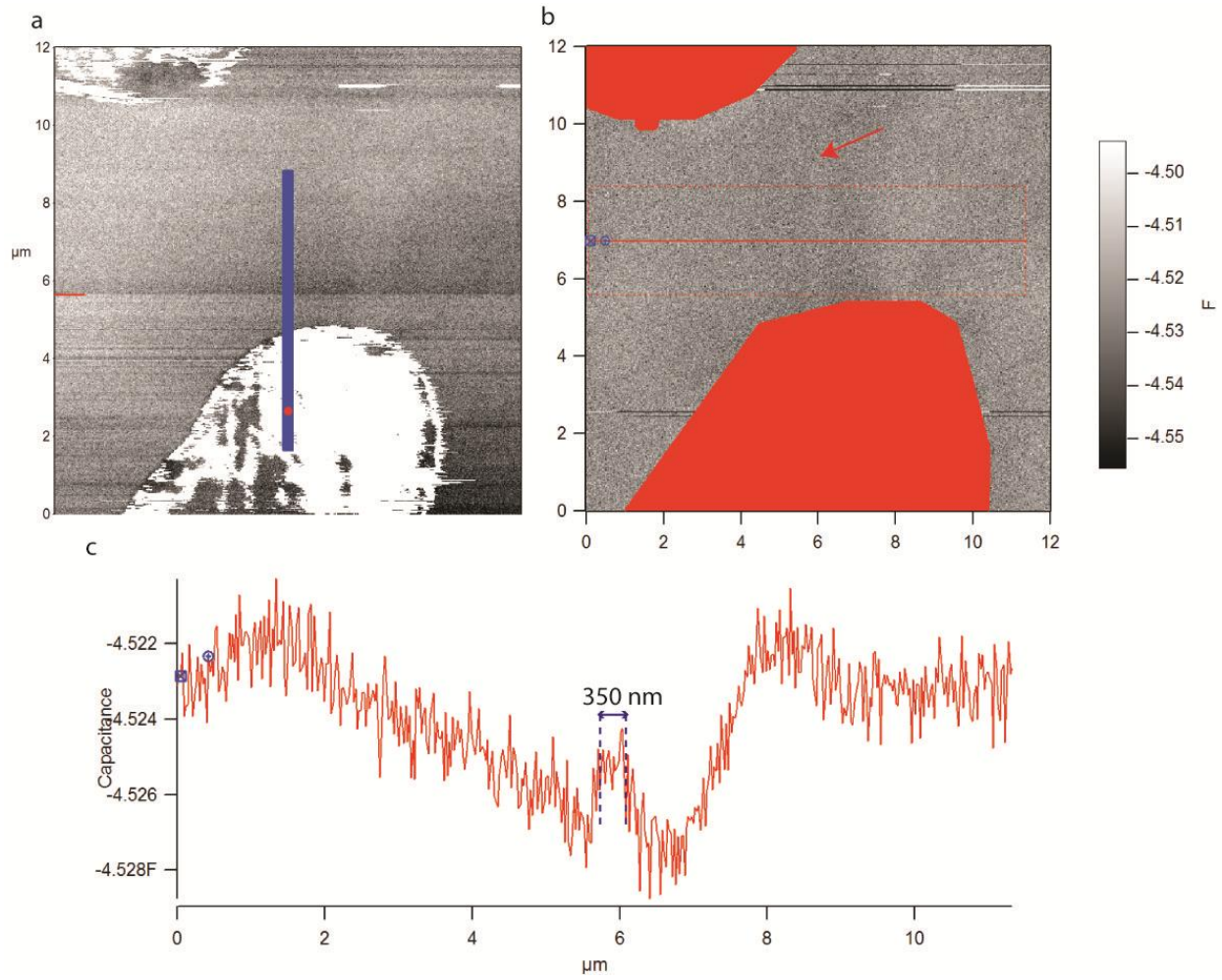

Figure 5.7 Microwave imaging of q-2DEG nanowires at the $LaAlO_3/SrTiO_3$ interface. (a) 60 nanowires were written in a 7 μm×250 nm area contacting the ground electrode. (b) Microwave image shows a faint box on $LaAlO_3$ surface as indicated with the red arrow. (c) Signal average in the red box in (b). A plateau with 350 nm width show up at the same location of nanowires. The size dispersion is probably due to the fact that the written area is not perpendicular to the red box.

Now commercial scanning microwave microscopes are in a development stage or become available recently. Asylum Research is developing a scanning microwave microscope very similar to our design. In this microscope, a network analyzer is used to detector microwave power with a much higher sensitivity than the peak detector we used. In the mean time, a full metal tip is commercialized for use (Rocky Mountain Technology). With these two advantages, we used this microscope to image the q-2DEG nanostructures at the $LaAlO_3/SrTiO_3$ interface. In this experiment, a series of nanowires were written in a 7 μm×250 nm area in contacting with the ground electrode (Fig. 5.7a). The microwave image reveals a faint box (Fig. 5.7b) in the area that the nanowires were written. Further imaging processing shows a plateau with 350 nm width when averaging the image. The size discrepancy is due to the fact that the written area is not perpendicular to the averaging area, which introduces errors. Further measurement was prohibited due to limit amount of access time to the instrument (2.5 days in Asylum Research).

The development of the scanning microwave microscope is still under way. Future direction includes better power detector (use of network analyzer), a full metal tip, and improve the quality factor of resonator

6.0 ELECTRIC CHARACTERIZATION OF MEMRISTIVE DEVICES AT MICROWAVE FREQUENCIES

The memristor, known for "memory resistor", provides a new prospect of view of nonlinear resistive switching devices by bridging the charge and magnetic flux(*109*). The non-volatile switching behavior, ultra-dense scaling and fast response make it a very promising candidate for next generation nanoelectronics applications including non-volatile memory, neuromorphic computing and stateful logic operation(*110*). Huge progress has been made to understand the physics, including the direct observation of filamentary conduction channels through high resolution transmission electron microscopy (HRTEM). In this chapter I will introduce the project I advanced at HP labs. In this project we integrate a Pt/TiO_2/Pt nano-crossbar memristor to a 15 GHz microwave resonator to probe the ultra-small capacitance change between ON/OFF states by using the resonance frequency perturbation method. The extracted capacitance change (4.6 aF) can be used as a state parameter to further understand the internal structural difference between ON/OFF states.

6.1 THE FOURTH ELEMENT

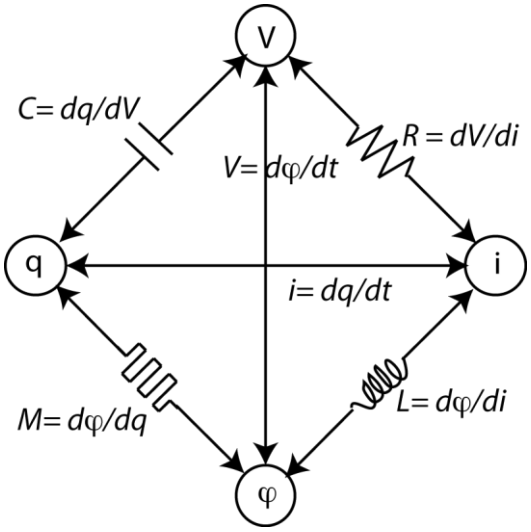

Figure 6.1 Symmetry in fundamental circuit elements indicates the existence of missing memristors.

If we write the basic circuit variables in a figure as Fig. 6.1, we will find out that among magnetic flux, charge, current and voltage, most of them can bridge each other with a simple mathematical relation by introducing the resistor, capacitor and inductor. However, there is a missing piece between magnetic flux and charge. In 1971, Leon Chua first perceived this broken symmetry and proposed a non-linear element memristor (short for memory resistor) such that

$$d\varphi = Mdq \tag{6.1}$$

where M is the memristance(*111*), φ and q are magnetic flux and charge respectively. Differentiate (6.1) versus time at both sides we will get

$$v = M(q)i \tag{6.2}$$

where *v* and *i* represent voltage and current respectively.

The memristance is a function of charge and the physical meaning can be understood from Stanley Williams (HP Labs) quote: "Memristance is a property of an electronic component. If charge flows in one direction through the circuit, the resistance of that component of the

circuit will increase, and if the charge flows in the opposite direction in the circuit, the resistance will decrease. If the flow of charge is stopped by turning off the applied voltage, the component will 'remember' the resistance that it had, and when the flow of charge starts again the resistance of the circuit will be what it was when it was last active"(*112*).

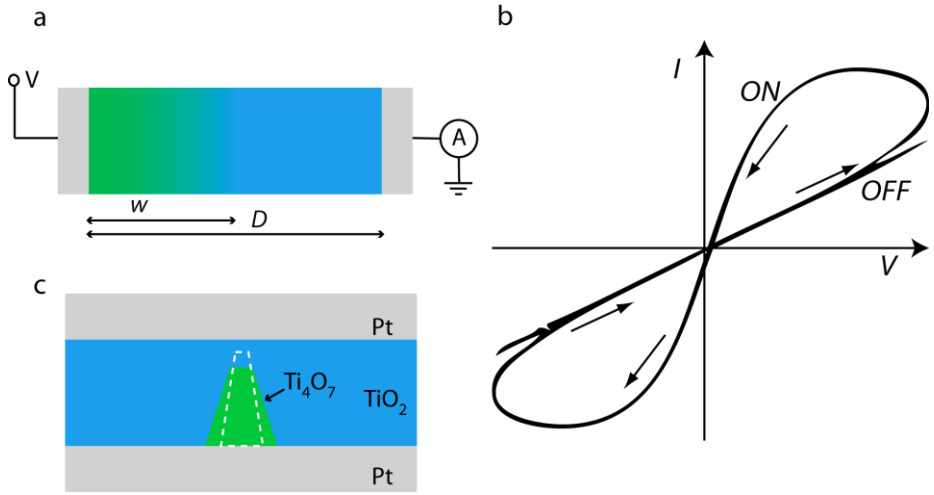

Figure 6.2 Memristor model and mesoscopic picture. (a) The "dopant drift" model for memristor. (b) The Lissajous curve like *I-V* curve showing two conductance states, "ON" and "OFF". (c) Mesoscopic picture of a filamentary conducting channel.

Despite self-completion in concepts, the memristor has long time been a missing piece by lacking a real physical application. Until recently Strukov et al. at HP labs proposed a physical "dopant drift" model by considering a semiconductor film sandwiched in two metal electrodes. As shown in Fig. 6.2a, the width of the film is D and the resistance of the device can be controlled by moving the dopants (e.g. oxygen vacancies) in a region $0<w<D$, where w is the doping region width. Assuming the minimum ($w=D$) and maximum resistance ($w=0$) are R_{ON} and R_{OFF} respectively, we have

$$v(t) = \left(R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) i(t) \tag{6.3}$$

The term in the parentheses has a form of memristance *M(q)*. Further assuming the mobility of film is μ_V, we have

$$\frac{dw(t)}{dt} = \frac{\mu_V R_{ON}}{D} i(t) \tag{6.4}$$

$$w(t) = \frac{\mu_V R_{ON}}{D} q \tag{6.5}$$

Plug (6.5) into (6.3) and neglect the second order of R_{ON} by assuming $R_{ON} << R_{OFF}$, we have the memristance

$$M(q) = R_{OFF}(1 - \frac{\mu_V R_{ON}}{D^2} q(t)) \tag{6.6}$$

The memristance has a linear dependence on charge and it has to be enforced by boundary conditions. Otherwise it will leads to an unrealistic value as time goes by. One reasonable boundary condition is that the value of *w* satisfies $0<w<D$, which requires oscillating external voltage and current. Such condition is known to result in a Lissajous curve like current-voltage (*I*-*V*) curve (Fig. 6.2b). In this curve, the conductance has two modes with one at higher conductance (ON) and the other one with lower conductance (OFF).

One physical memristor realization is the TiO_2 based resistive memory(*113-116*). Figure 6.2c shows a mesoscopic picture of Pt/TiO_2/Pt memristor, in which a thin TiO_2 film (~20 nm) is sandwiched between two platinum electrodes. Initially the film is not conducting. After an electroforming procedure by carefully applying a large voltage to the film, a filamentary conducting channel forms due to local dielectric breakdown(*117*). This filament is in crystalline Ti_4O_7 Magnéli phase, which is proved by high resolution transmission electron microscopy (HRTEM)(*118*) and scanning transmission x-ray microscopy (STXM)(*119*). The size of the filament can be controlled by external voltages by moving oxygen vacancies. The growth of the filament closes the tunnel gap between the filament and switching interface, resulting a large ON

state conductance. In the other hand, applying a voltage with an opposite sign will disrupt the filament and leads to a low conductance OFF state.

6.2 MOTIVATION

Despite the electronic characterization, numerous tools have been applied to unveil the operating mechanism of memristive devices, especially Pt/TiO_2/Pt system. Pressure modulated conductance microscopy locates the conduction channel and reveals the tunneling gap width(*120*). HRTEM visualizes the crystalline nanofilaments, finding the needle in the haystack(*118*). STXM also identifies the conduction channel and Ti_4O_7 Magnéli phase of the filament. All the above work greatly helps understand the device physics, however, they cannot reflect the device state in real time. Non-volatile memory application requires high stability and endurance of memristor operation. However, switching anomalies happen very often in real device operation. Another state parameter besides resistance, i.e. capacitance, is desirable since it contains additional information on the internal structure.

The capacitance change between ON/OFF states of a memristor is extremely small. A naïve estimate of a Pt/TiO_2/Pt system with a conducting filament of 1 nm radius, 1 nm tunneling gap and 1 nm tunneling gap change between ON/OFF states gives out ~ 2 aF (2×10^{-18} F) capacitance change. Such small change is beyond the measurement limit of any capacitance meters based on capacitance bridges and lumped *L*-*C* circuits. One way to lift this limit is to use microwave resonator perturbation method introduced in previous chapters.

6.3 RESONATOR DESIGN AND MEMRISTOR INTEGRATION

We utilized a microstrip transmission line resonator that was fabricated on a 3-inch low loss, high dielectric constant sapphire wafer (A-plane). The backside of the wafer was coated with 1.5 μm copper (or silver), three times of the skin depth at 15 GHz, as the ground plane. The thickness of metal is critical to localize the electric fields under the metal. Usually 3 times the skin depth will confine most of the field. The choice of metal is also based on this point, as the copper and silver have the smallest skin depth (~0.5 nm). The resonator uses a similar gap-coupled half-wave design as Ref. (*121*), in which the electric field is maximized at the resonator ends. Figure 6.3a and c show the metalized resonator structure (made of 1.5 um thick copper). The radial stubs serve as virtual ground for microwave and λ/4 narrow transmission lines block microwave to travel out of the resonator. Two 90° radial stubs with bias pads enables DC biasing for the memristor, while no microwave can leak to the biasing network.

The memristor was deposited at the end of the resonator, as shown in Fig. 6.3(b). To do this, we first deposited thin metal resonator structure (8 nm) to serve as a location mark. Then 3 nm Ti and 15 nm Pt bottom wire electrode (100 nm × 50 μm or 1 μm × 50 μm) was deposited in contacting with bottom λ/4 transmission line. After this 20 nm amorphous TiO_2 thin film was sputtered from a rutile source. Finally 33 nm Pt top electrode of the same size as bottom electrode was deposited in contacting with the resonator. The intersection of the electrodes formed the memristor. After memristor fabrication, 1.5 um copper and 100 nm Pt was deposited on top of previous thin resonator location mark to serve as the resonator.

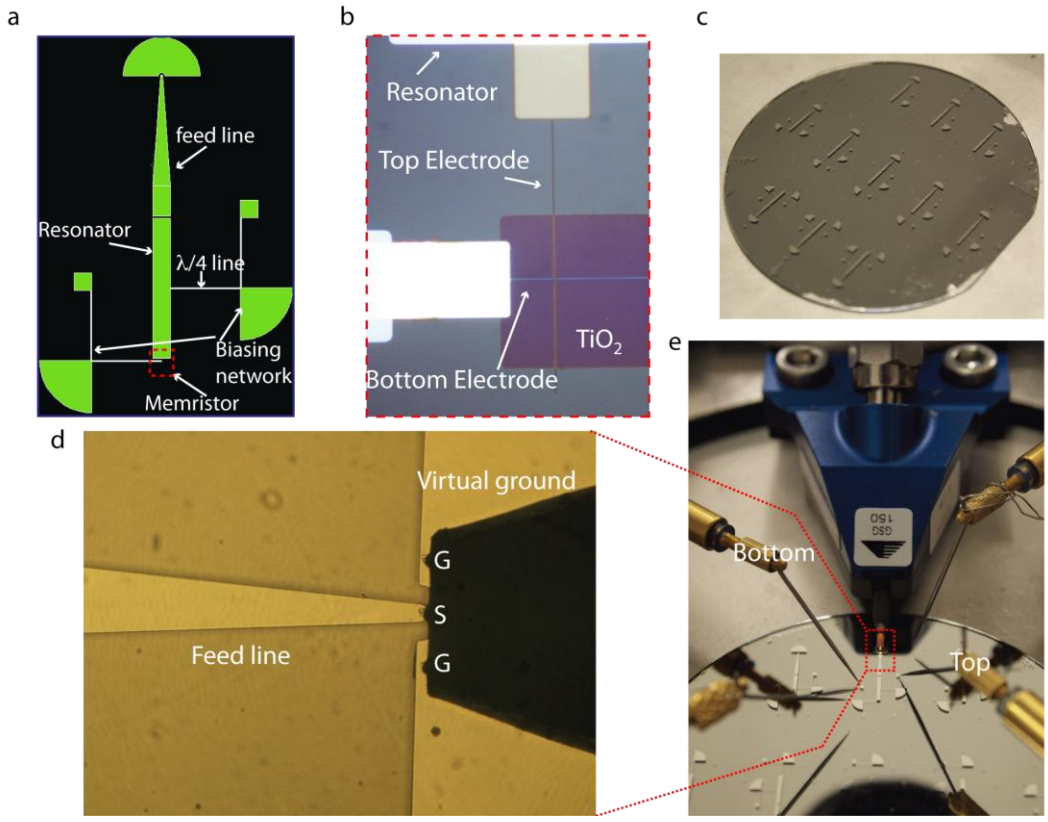

Figure 6.3 Resonator design and memristor integration. (a) Resonator design. The microwave is fed through the feed line and coupled to the microstrip resonator through a gap. The memristor is integrated at the resonator end, and the DC biasing network allows low frequency biasing for the memristor. (b) Optical view of a memristor (1 μm×1μm) in the red dashed box in (a). (c) Resonator fabricated on a 3-in sapphire wafer. (d) Optical graph of a 67 GHz microwave probe contacting the feed line. (e) Experiment set up in a probe station.

The measurement was carried out by landing a 67 GHz microwave probe to the feed line of the resonator in a probe station (Fig. 6.3e). The probe has a ground-signal-ground (GSG) pins configuration so that the ground pins contact the half-moon shape radial stub (virtual ground) and signal pin touches the feed line (Fig. 6.3d). The S_{11} parameter was measured by a 50 GHz network analyzer (HP 8364B), and the control of memristor states was done simultaneously through the DC biasing network.

We used finite element analysis (High Frequency Structure Simulator, HFSS) to characterize the resonator at resonance frequency. Figure 6.4a shows the S_{11} resonance curves of an unloaded resonator by HFSS simulation and experiment, which agree in 1% accuracy. Figure 6.4b shows the electric field distribution surrounding the resonator, showing that most of the microwave field is confined at the ends and only small field leaked to biasing network. Figure 6.4c is the *I-V* curve for a memristor fabricated, showing the non-volatile ON and OFF states.

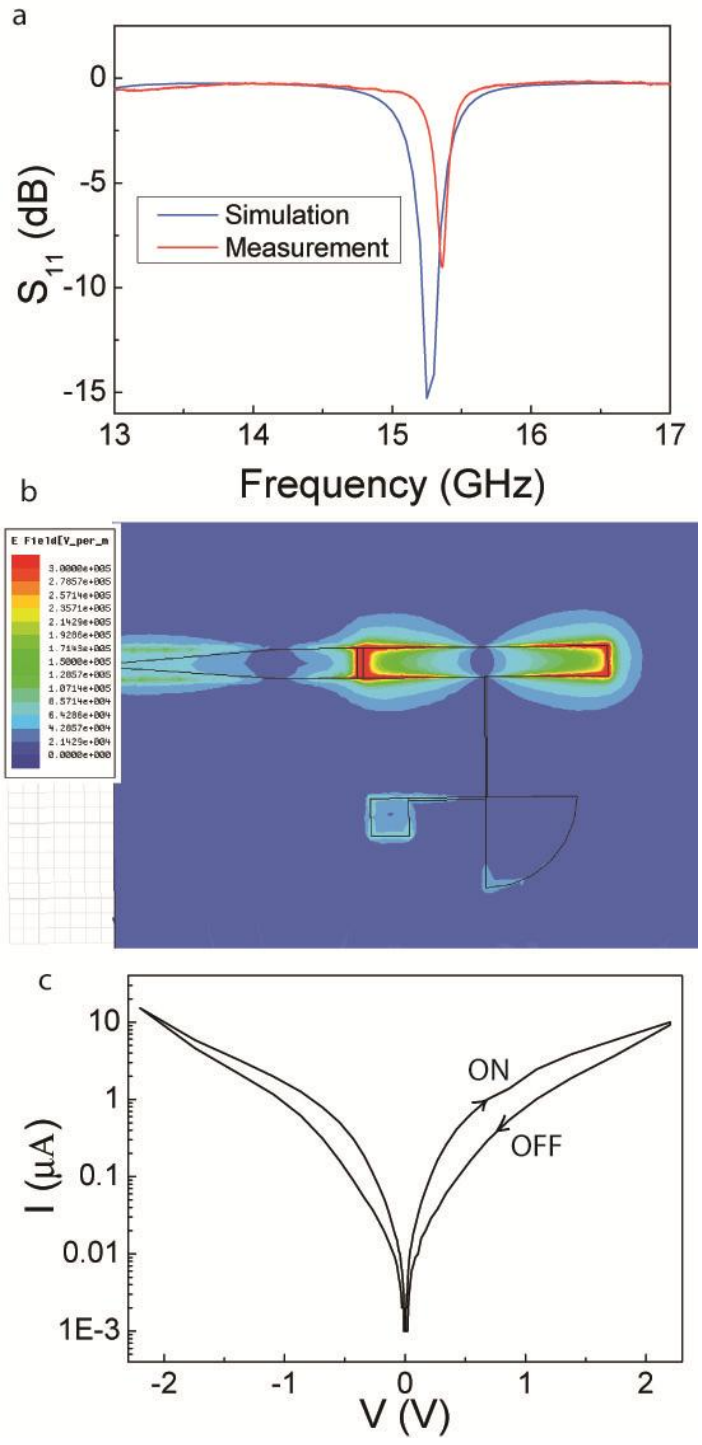

Figure 6.4 Resonator and memristor characteristics. (a) Resonator resonance frequencies by simulation and experiment. (b) Electric field distribution for an unloaded resonator. (c) *I-V* curve for a memristor showing two states non-volatile behavior.

6.4 RESONATOR FREQUENCY SENSITIVITY

Calibrating the frequency sensitivity is hard due to the lack of a capacitor standard and special resonator design. We took advantage of the small capacitor readily formed between λ/4 transmission line and the resonator. By varying the spacing between λ/4 transmission line to the resonator, the capacitance is also changed. Such change can be reliably determined by finite element analysis (COMSOL multiphysics simulator). Varying the spacing from 50 μm to 223 μm, the resonance frequency shifts 156 MHz and capacitance changes 1.5 fF. Owing to the low loss substrate and high resonance frequency, we conclude the frequency sensitivity as high as 104 MHz/fF (Fig. 6.5), which is two orders higher than low frequency resonators fabricated on pc board or coaxial transmission line.

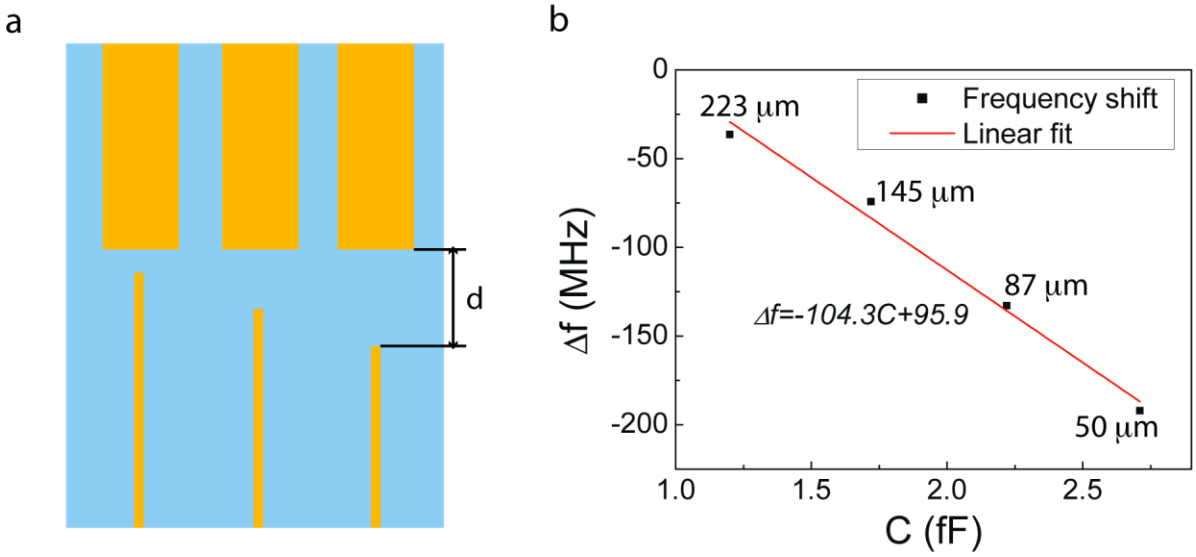

Figure 6.5 Resonator calibration. (a) The $\boldsymbol{\lambda/4}$ line and the resonator form a calibration capacitor whose capacitance can be determined by COMSOL finite element analysis. (b) By varying the spacing *d* (50 μm to 223 μm) between the $\boldsymbol{\lambda/4}$ line and the resonator, the capacitance of the capacitors is varied and the resonance frequencies are measured accordingly. The inferred frequency sensitivity is given by the slope of the fitted curve (red line).

6.5 EXPERIMENT RESULTS

The memristor was electrically formed to the OFF state by applying a large 9 V (amplitude) 1 μs (duration) pulse to locally breakdown TiO_2 film and form conducting filaments. After electroforming, a typical device operation requires 5 V 1 μs pulse to set device OFF and -4 V 1 μs pulse to turn ON, yielding ON/OFF ratios from 10 to 1000 for different devices and cycles. In the experiment, we applied a sequence of pulse cycles (combination of 5 V and 4 V 1 μs pulses) to switch the device ON and OFF, while simultaneously measuring the resistance and recording S_{11} microwave responses (spectra from 10 GHz to 38 GHz) by the network analyzer at a 1 KHz bandwidth. After each pulse cycle, we waited for 1 s to 20 minutes to take the spectrum to minimize the Joule heating related geometry changes.

Figure 6.6a shows the resistance changes between ON (200 KΩ) and OFF (200 MΩ) states. The resonance frequency f_r was extracted by fitting S_{11} to a Lorentzian function

$$S_{11} = \frac{A\gamma}{\gamma^2+(f-f_r)^2} \tag{6.7}$$

where γ is the half-width at half maximum, A is a normalizing factor and f_r is the resonance frequency. We find the frequency shifts about 478 KHz between the ON/OFF states (Fig. 6.6b), corresponding to a capacitance change of 4.6 aF. Moreover, the resonance frequency consistently follows the resistance changes, however, surprisingly the ON state has higher resonance frequency. The valence-change mechanism(*122*) states that the ionic movement of oxygen vacancies induces the growth and rupture of conducting crystalline TiO_x (x<2) filament. In the ON state, the tunneling gap between the filament and switching interface is smaller, resulting a larger capacitance (lower resonance frequency) by intuition.

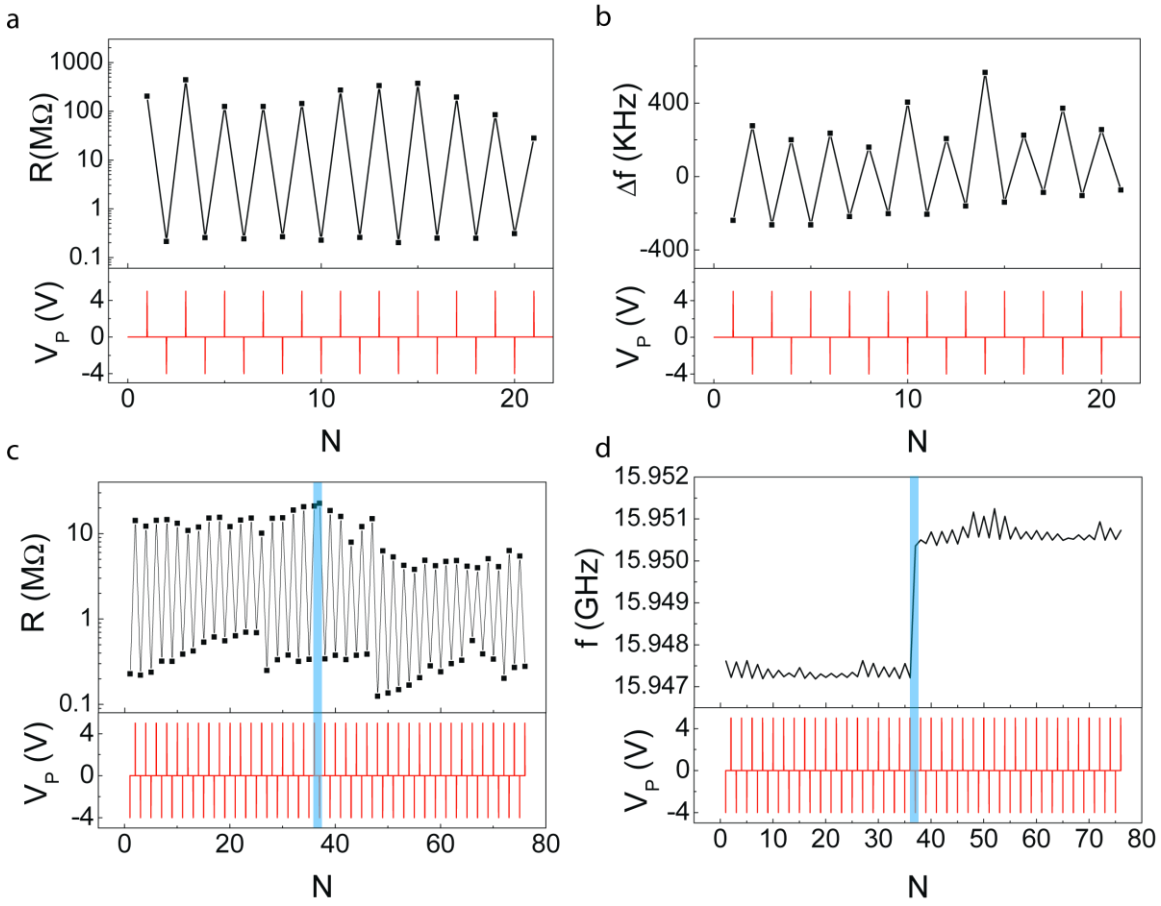

Figure 6.6 Memristor resistance and resonant frequency shift under ON/OFF cycles. (a) Resistance trace under external -4/5 V 1 μs pulse train through biasing network. (b) Resonance frequency trace under same pulse conditions as (a), the trace is shifted by 15.9524 GHz for clarity. (c) Different tryouts for the same device as (a). The switching interface is spontaneously reversed at cycle 35, while the resistance value are kept similar values. The blue shadow marks the transition cycles 35 and 36 where the resistance should switch to ON instead of staying in OFF state. (d) Corresponding resonance frequencies under same pulse condition as (c). The resonance frequency has a sudden jump between cycle 35 and 36, which indicates the destruction of a conducting filament.

In certain case, the device underwent a spontaneous change in switching interface. Positive pulses set the device to OFF state before cycle 35, but had a reverse effect after that cycle (Fig. 6.6c). The device state should be switched to ON state, however, it stayed in OFF state at cycle 36. The resistance values do not have obvious changes after this switch, however, the resonance frequency encountered a jump 10 times larger than the frequency difference between the ON and OFF states (Fig. 6.6d). This jump has been observed in different devices and experiment date. The inconsistency between the resistance and resonance excludes the argument that the resonance frequency shifts are caused by resistance changes. It also suggests that the capacitance information can provide additional information that is not revealed by the resistance, i.e. the internal structure of the memristor.

6.6 POSSIBLE MODELS

The contradiction between observation and expectation indicates the internal structure of the memristor is far more complicated than expected. HRTEM(*118*) images have proven multiple conical filamentary conduction channels. Under external pulses, oxygen vacancies redistribute through ionic transport, modulating the tunnel barrier gap and filament size. In the OFF state, it is very likely that the shape of filament turns from cone to conical frustum, increasing the top surface area but at a price of extended tunnel barrier gap (Fig. 6.7a,b). Assuming the tunnel barrier gap changes from 1 nm (ON state) to 2 nm (OFF state) according to pressure modulated conductance microscopy(*120*), COMSOL simulation shows that memristor geometry change can not fully account for higher OFF state resonance frequency. However, the dielectric constant of Ti_nO_{2n-1} ($n \geq 4$) within the tunnel barrier could be much larger than which of

surrounding TiO_2 in the OFF state. The modulation of tunnel gap results from metal-insulator transition from one conducting Magnéli phase to insulating rutile phase or a large n insulating Magnéli phase (Fig. 6a). In the OFF state, if some substantial amount of insulating material surrounding the filament is still in the Magnéli phase, then the dielectric constant is much larger than the rutile phase in the ON state. This non-volatile change of dielectric constant will lead to larger capacitance and lower resonance frequency.

We attribute the switching interface transition and sudden resonance frequency jump to the rupture of parallel filamentary conduction channels (Fig. 6.7c,d), whose existence are confirmed by HRTEM images. STXM(*123*) study also shows the emergence of new filaments as more pulse cycles are applied. In cycle 35, one filament that switches at the top interface dominates electron tunneling behavior. However in cycle 36, this filament is disrupted by some spontaneous process and a new filament that switches at the bottom interface take control. The sudden jump of the resonance frequency in Fig. 6.6d marks a signature for the rupture and creation of conducting filaments, which is can not be explained in the resistance values.

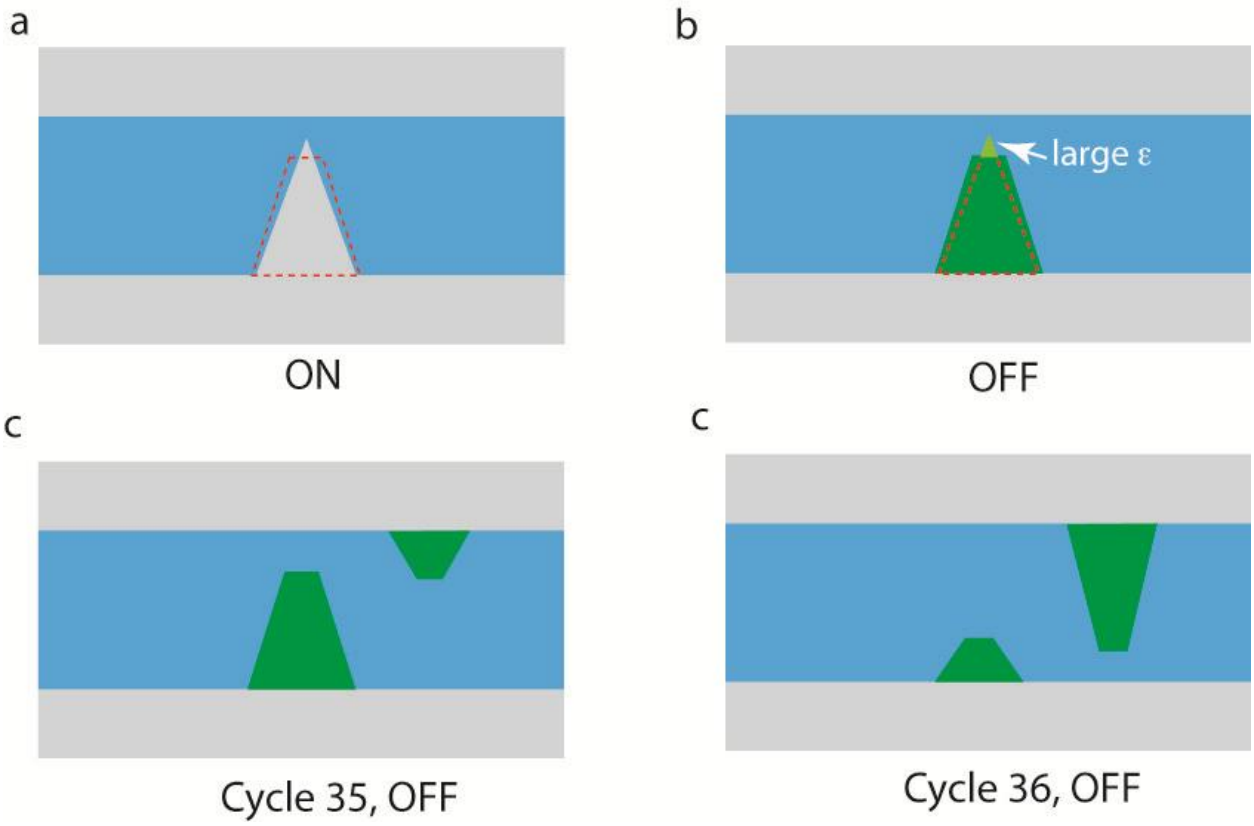

Figure 6.7 Possible models. (a) Device schematic for ON state, a cone shape filament is used. The red dashed shape indicates the filament in OFF state (b) Device schematic for ON state. The filament turns from cone shape conical frustum. The red dashed shape indicates the filament in ON state. The dielectric constant in the tunnel gap (indicated in light green) is much larger than the surrounding dielectrics, (c) In cycle 35, the tunneling behavior is dominated by one filament that switches at the top interface. (d) In cycle 36, the previous filament is disrupted, and new filament gains the control of tunneling behavior that switches at the bottom interface.

6.7 SUMMARY AND FUTURE WORK

To summarize, we fabricated a microwave resonator that has DC biasing capability. We also integrated memristors to the resonator and successfully observed the resonant frequency shifts with memristor ON/OFF states. The ability to measure the ultra-small capacitance change between ON/OFF states provides us an insight to the memristor operating mechanism. Such capacitance variation can be used as a state parameter together with resistance. Future work including resonator integration with devices fabricated using different materials and methods can shed light in full understanding of the electronic properties of memristive devices.

7.0 SUMMARY AND OUTLOOK

In this dissertation we have studied some novel devices including the SketchSET devices at the 3 uc $LaAlO_3/SrTiO_3$ interface, ferroelectric field transistors made directly on silicon using a strained SrTiO3 thin film that is commensurately grown silicon, and memristive devices fabricated on a sapphire wafer and integrated to a microwave resonator. These projects are relatively independent but they are well united under nanoelectronics in oxides and semiconductors. We also have developed novel tools to allow us probe the ultra-small capacitance of devices that could provide more information on the device states and shed light on better understanding the working principles. For examples, by knowing the capacitance information, we know how many electrons in the quantum dots and we know how the memristor devices switch. The integration of the microwave capacitance sensor to a home developed AFM also provides us to a versatile tool in studying nanoscale physics including sample dielectric properties and ferroelectric properties.

We have advanced and explored many in nanoelectronics. And the future is even more exciting, promising and challenging. For the SketchSET devices, exploring the spin effect will expand the capabilities of these devices to a next level. Quantum simulation is possible to carry out in SketchSET, in analogy to ions trapped in an ion trap. We can also combine the ferroelectricity and tunneling properties in SketchSET devices to sense ultra small forces, namely a piezoelectric mechanical sensor with charge read out.

The successful realization of silicon FeFET devices may leap over the long-term challenges in making a functional integration of FeFET with silicon. In the mean time, it provides further proof to the ferroelectric nature of strained $SrTiO_3$, which has been an academic debate since simple theoretical DFT calculation does not the ferroelectricity. In future, growing $SrTiO_3$ film on step-free silicon will improve the film quality. Also fabricating smaller devices will greatly improve the working frequency.

The successful observation of a capacitance change between ON and OFF states makes the capacitance another state parameter for understanding the operation of memristive devices. A commercial realization of non-volatile memory requires the memristors operating with high stability and endurance. The commercial product could emerge as early as 2012 owing to the hard work done by HP labs. The resonator provides a test bed for future memristors with new materials and new fabrication methods.

APPENDIX A

LOW TEMPERATURE SCANNING OPTICAL, FORCE AND MICROWAVE MICROSCOPY

In fundamental physics research at nanoscale, it is of great interests in knowing the information of sample surface topography, dielectric properties and optical properties at various temperatures. Any commercial product on microscopy does not provide all the capabilities in one. For this purpose, we developed a low temperature scanning optical, force and microwave microscope to study the novel properties of samples and devices at various temperatures. The development of this tool is spanned for many years and has 2 versions with similar design. The first version is made of macor and no microwave option is integrated(*107*). However, macor is fragile and subject to damages during the loading and unloading process in a cryostat. We made the second version of titanium, which is much sturdier and the thermal coefficients of titanium matches that of piezo driven motors to guarantee stable performance. In this appendix, I will introduce the design, fabrication and control of this versatile tool.

A.1 INSTRUMENTATION

Figure A.1 shows the photograph of the microscope. This titanium microscope consists of four major parts including two approach motors, an XY scanning stage, a feedback system and a microstrip resonator. The diameter of the microscope is about 1 inch, compact enough to fit in a helium flow cryostat. In the mean time, the limited space puts stringent requirements on the microscope design.

The top motor attaches the feedback piezo stack, microstrip resonator and force sensor. And the bottom motor holds an optical objective to focus light on the sample. The motors are driven by piezo stack actuators embedded in the microscope frame in a "stick-slip" mode. The XY stage has a custom made piezo stack from PI with a central hole allowing access of the optical objective. The scan size of the stage is 6 μm×6 μm and remains about 25% range at 4 K temperature. The coarse motion of the sample plate is done in a similar "stick-slip" motion.

Fig. A.1 Photograph of the microscope. The microscope consists of two approach motors. The top motor holds the AFM tip and microstrip resonator, and the bottom motor holds an optical objective. Each motor is driven by 6 piezo stack assemblies. The sample stage is a peizostack scanner with a range 6 μm×6 μm in X and Y directions. At low temperature, the range is reduced to about 1.5 μm×1.5 μm.

A.1.1 Approach motors

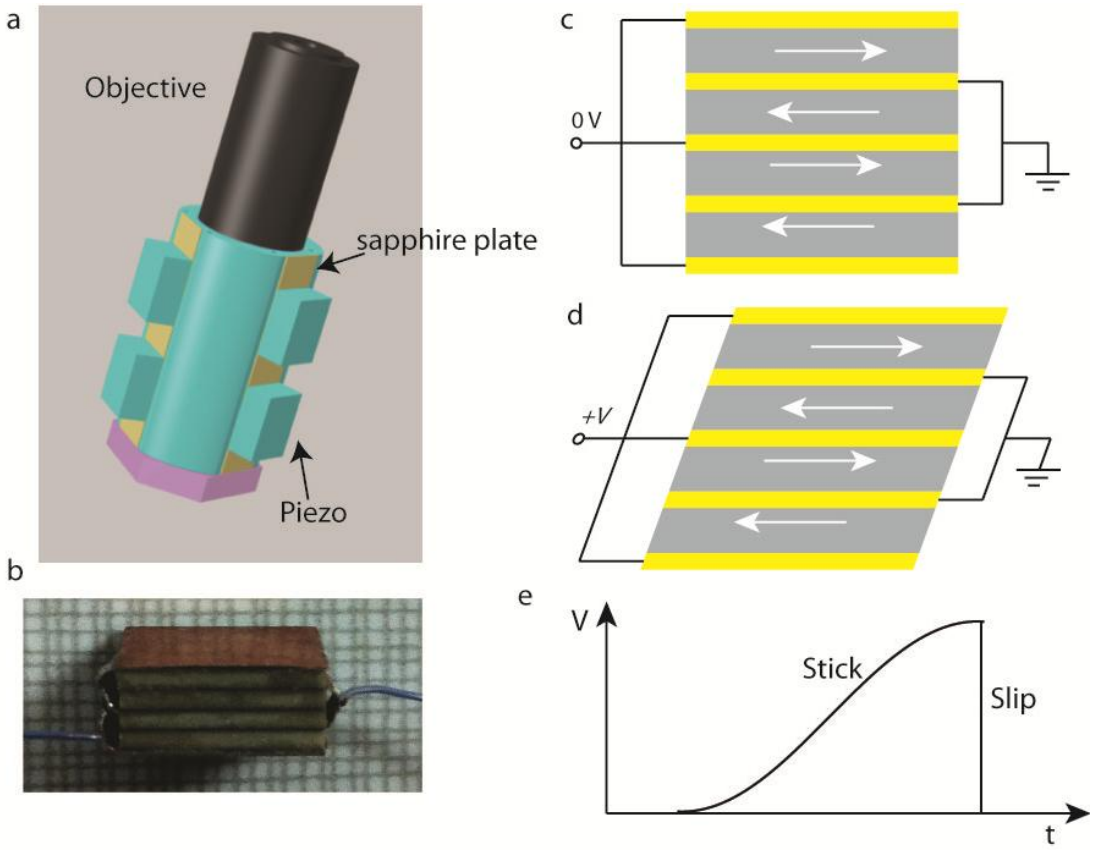

Fig. A.2 Approach motor (a) Schematic. (b) Photograph of a piezo stack assembly glued together by 4 shear piezo stacks and five thin copper electrodes. (c) Piezo stack assembly at 0 external voltage. (d) Piezo stack assembly under external voltage V, the piezo stacks are stretched. (e) External voltages applied to the piezo stacks. One step function of voltage will slip the piezo stacks on the sapphire plate glued on the approach shaft. Under a cosine shape voltage, the piezo stacks "stick" together with the approach shaft.

Each approach motor consists of 6 piezo stacks assembly (Fig. A.2a,b) embedded in the microscope frame, a shaft that holds the objective, and three sapphire plates between piezo stacks and the shaft to make smoother contacts. Each piezo stacks assembly is made from 4 shear piezo stacks. They are glued with thin copper electrodes in a way such that external positive voltages will stretch the piezo stacks (Fig. A.2c,d). More piezo stacks used, larger displacement can be

achieved. During the operation, 6 piezo stacks assembly slowly grab the shaft with static friction force under a gradually increased cosine shape external voltage (Fig. A.e). Then the voltage is suddenly reduced to zero in a step function and the piezo stacks "slip" to the original unstretched state. However the shaft remains in the same position since the friction force turns to kinetic. This is so called "stick-slip" motion to allow coarse movement of the motors. The force between the piezo stacks and the shaft is adjusted by a titanium sheet wrapped around the motor. Too large a force will increase the maximum static friction force and the "slip" part of motion will not happen. However if the force is too small, the piezo stacks can not hold the motor against the gravity.

A.1.2 Sample stage

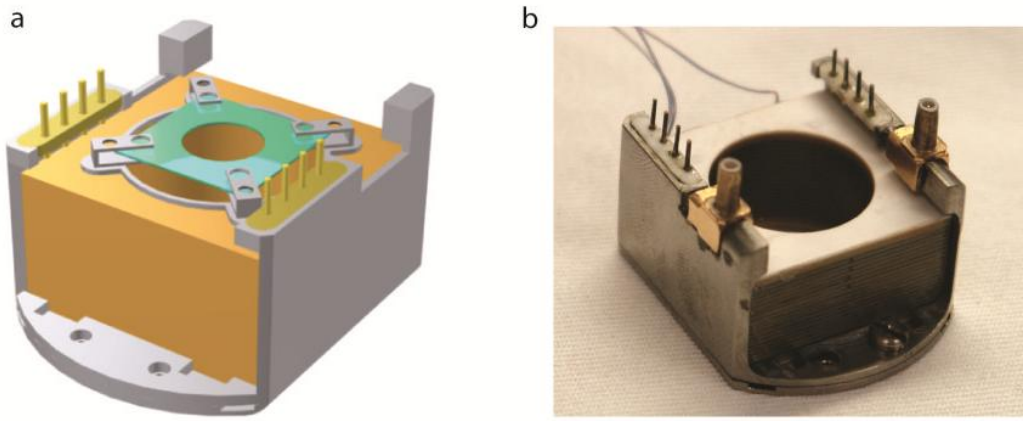

Fig. A.3 XY scanner

The XY sample piezo stack scanner is custom made by PI and held by a titanium frame. The dimensions are 24mm*24mm*15mm with a 17 mm hole in the center to allow optical access. The scan range is +/-3 um (+/-250 V) in both directions. The sample is hold by a

sapphire sample plate (green part in Fig.A.3a), which works in a "stick-slip" motion to coarsely move the sample. The sample plate is held by self-aligned sapphire hemispheres in 4 titanium clips.

A.1.3 Feedback piezo assembly and the resonator

The Z feedback piezo assembly and the microstrip resonator are held in the top approach motor (Fig.A.4). The Z feedback piezo (PI P-010.00H, 5 μm range) regulates the tip-sample separation during a scan, in the mean time it drives the force sensor at tuning fork resonance frequency 32 KHz. This vibration frequency is high enough that the feedback system will not react. As far as the feedback piezo stacks respond linearly to the external voltages, this vibration mode will decouple from the feedback system and won't cause imaging artifacts.

The resonator is glued to the feedback assembly, and the tuning fork force sensor is attached at the end of the resonator. Figure A.4b shows the resonance curve with the tuning fork sensor.

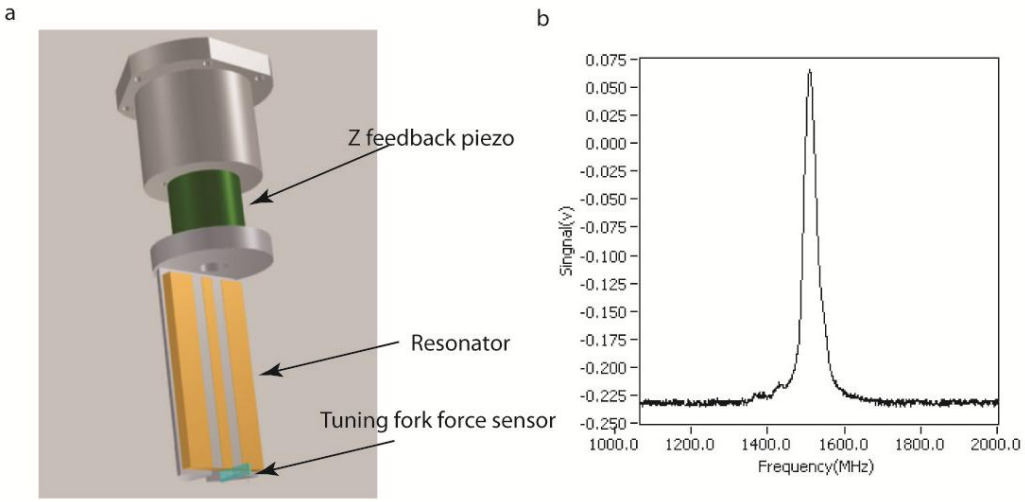

Fig. A.4 Feedback piezo assembly with the microstrip resonator

A.1.4 High voltage amplifiers

The driving voltages for the approach motors and feedback piezo stacks are in a range of -200 V to 200 V. And the output from the controller is smaller than 10 V. A high voltage amplifier is used to amplify the signal from the controller. Figure A.5 shows the circuit diagram for the home made power amplifier unit. It is based on a high voltage operation amplifier PA88 from Aptex Microtechnology. The basic circuit diagram is shown in Fig. A.5b, in which it amplifies the coarse signal with a gain -20 and a fine input signal with a gain close to 1. The out voltage V_o is

$$V_o = \frac{R_1}{R_0+R_1}\frac{R_c+R_f}{R_c}V_f - \frac{R_f}{R_c}V_c \tag{A.1}$$

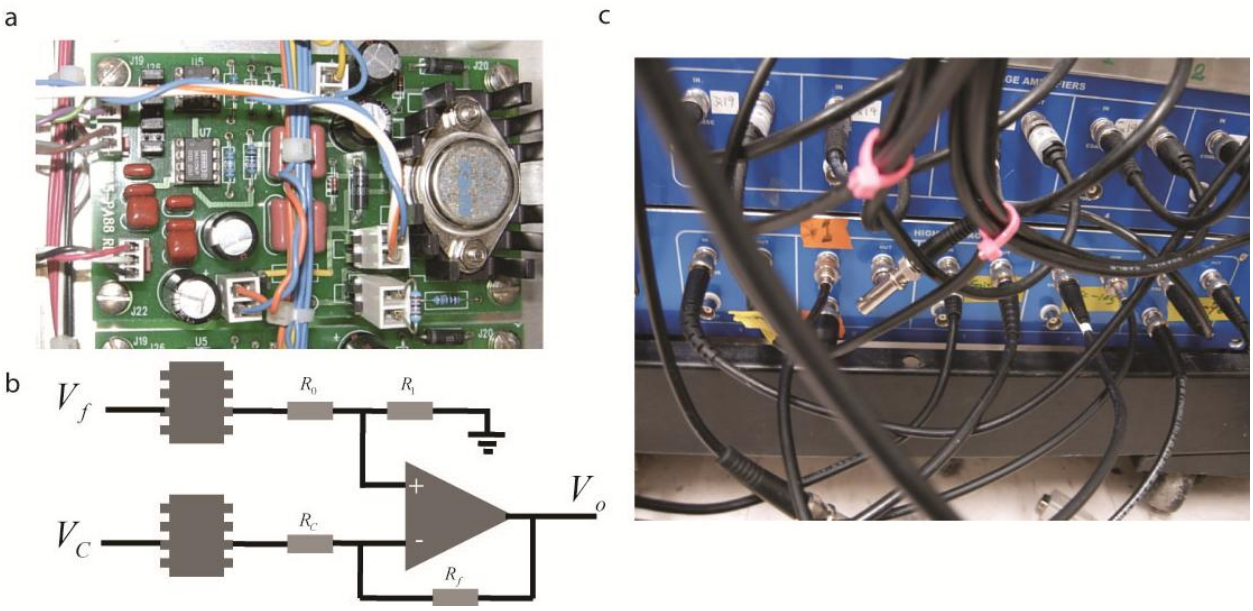

Fig. A.5 High voltage amplifier. (a) Circuit board. (b) Circuit diagram. (c) Amplifier boxes. Each box has 6 amplifier units.

A.2 WORKING PRINCIPLE

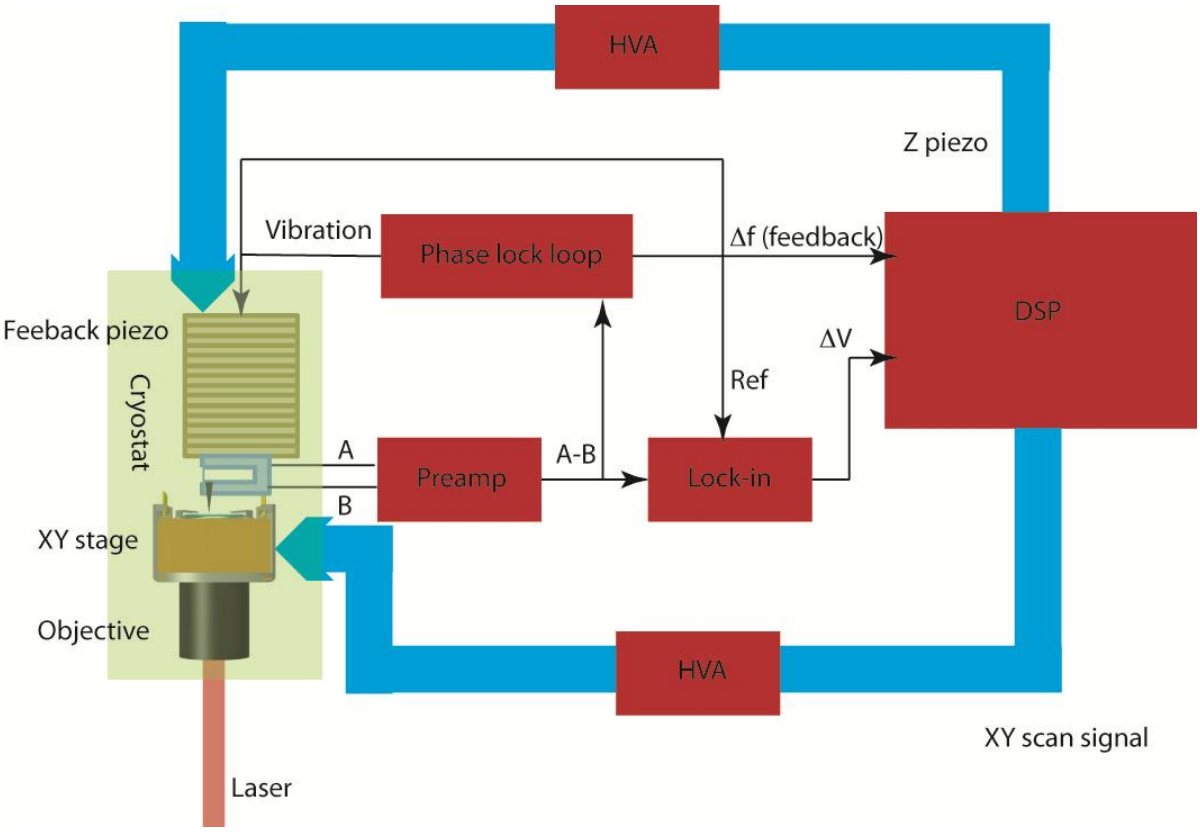

Fig. A.6 Working principle

This microscope works in a non-contact mode using a frequency modulated tuning fork sensor. Figure A.6 shows the AFM part working principle. While the microwave part is identical as shown in chapter 2 and 5. A phase lock loop (PLL) produces the driving signal at 32 KHz to vibrate the feedback piezo and in turn vibrates the tuning fork sensor. The tuning fork sensor is piezoelectric, so that it produces an AC electrical signal under external mechanical vibration. During the scan, change of the atomic forces between the tip and sample will shift the resonance frequency of tuning fork. This frequency shift is actively monitored by the PLL, effectively converts it to a voltage signal. This voltage signal is input to the DSP controller, which alters the control voltage of the feedback piezo to remain a constant tip-sample separation.

In the mean time the DSP controller outputs the scan signal and correlates this signal with the feedback to reconstruct sample tomographic image. Other information including the optical response and microwave response are input to the DSP too, so that the microscope can simultaneously produce optical and microwave images.

A.3 GXSM

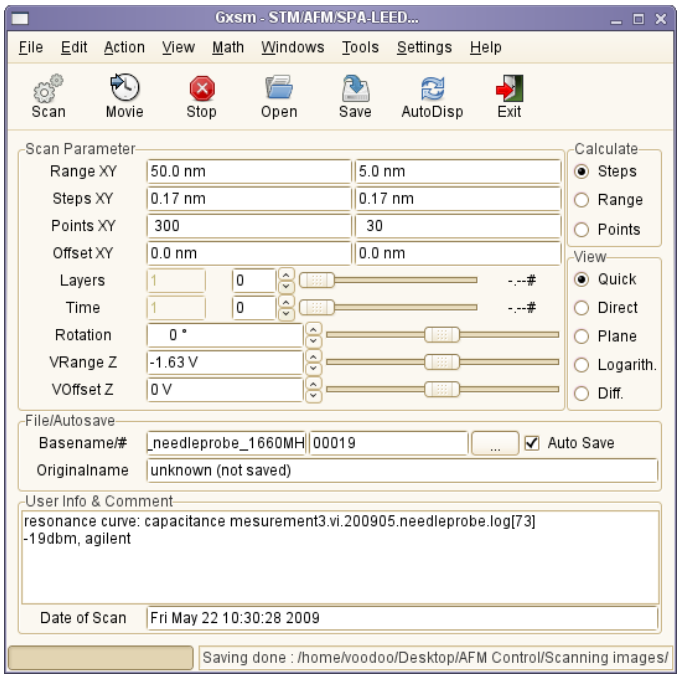

Fig. A.7 GXSM main window

The DSP controller is the heart of an AFM. A commercial controller usually costs much more than $20,000. We use an audio DSP board ($1000 value) with full hardware support by an open source microscopy software GXSM(*124*, *125*). GXSM, short for Gnome X Scanning Microscopy, is originated from University of Hannover in Germany and is currently maintained

by a team of developers. Figure A.7 shows the main window of GXSM running under Linux environment.

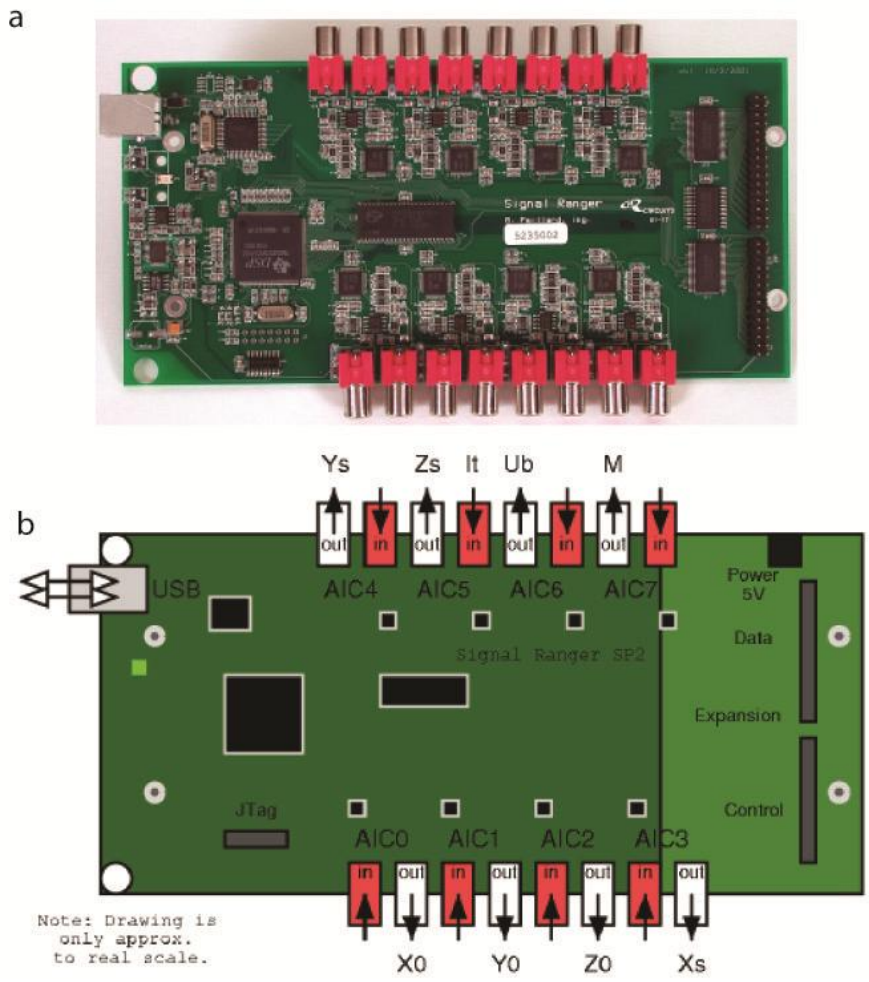

Fig. A.8 Signal ranger DSP board

The DSP board has (Signal Ranger SR-STD)100 MHz operation frequency and 8 inputs/ 8 outputs with 16 bit resolution. The scanning signal to the stage is output from channels 3 and 4, while the feedback I/O is channel 5. The output voltages range from -2 V to 2V,

BIBLIOGRAPHY

1. L. Kouwenhoven, C. Marcus, Quantum dots. *Physics World* **11**, 35 (Jun, 1998).
2. S. M. Reimann, M. Manninen, Electronic structure of quantum dots. *Reviews of Modern Physics* **74**, 1283 (Oct, 2002).
3. H. A. Wheeler, Transmission-line properties of parallel wide strips by a conformal-mapping approximation. *EEE Trans. Microwave Theory Tech.* **MTT-12**, 280 (1964).
4. G. Kompa, Practical Microstrip Design and Applications. *Artech House Inc.*, (2005).
5. A. Vonhippel, Ferroelectricity, Domain Structure, and Phase Transitions of Barium Titanate. *Reviews of Modern Physics* **22**, 221 (1950).
6. J. A. Andersen, *Reports to National Research Council*, (1918).
7. W. G. Cady, *Reports to National Research Council*, (1918).
8. G. Busch, P. Scherrer, *Naturwiss.* **23**, 737 (1935).
9. E. Wainer, A. N. Salomon, *Titanium Alloy Mfg. Company, Elec. Report* **8**, (1942).
10. E. Wainer, A. N. Salomon, *Titanium Alloy Mfg. Company, Elec. Report* **9 and 10**, (1943).
11. G. Shirane, S. Hoshino, *J. Phys. Soc. Japan* **6**, 265 (1951).
12. G. Shirane, R. Pepinsky, *J. Phys. Soc. Japan* **92**, 504 (1953).
13. R. E. Cohen, Origin of Ferroelectricity in Perovskite Oxides. *Nature* **358**, 136 (Jul 9, 1992).
14. J. H. Haeni *et al.*, Room-temperature ferroelectricity in strained SrTiO3. *Nature* **430**, 758 (Aug 12, 2004).
15. M. P. Warusawithana *et al.*, A Ferroelectric Oxide Made Directly on Silicon. *Science* **324**, 367 (Apr 17, 2009).
16. P. Zubko, G. Catalan, A. Buckley, P. R. L. Welche, J. F. Scott, Strain-gradient-induced polarization in SrTiO3 single crystals. *Physical Review Letters* **99**, (Oct 19, 2007).
17. J. F. Scott, Applications of modern ferroelectrics. *Science* **315**, 954 (Feb 16, 2007).
18. J. K. Clemens, Capacitive pickup and the buried subcarrier encoding system for the RCA VideoDisc. *RCA Rev.* **39**, 38 (1978).
19. R. C. Palmer, E. J. Denlinger, H. Kawamoto, Capacitive-pickup circuitry for VideoDiscs. *RCA Rev.* **43**, 194 (1982).
20. G. Binning, H. Rohrer, C. Gerber, E. Weibel, Surface Studies by Scanning Tunneling Microscopy. *Physical Review Letters* **49**, 57 (1982).
21. S. Alexander *et al.*, An Atomic-Resolution Atomic-Force Microscope Implemented Using an Optical-Lever. *Journal of Applied Physics* **65**, 164 (Jan 1, 1989).
22. A. Gruverman, O. Kolosov, J. Hatano, K. Takahashi, H. Tokumoto, Domain-Structure and Polarization Reversal in Ferroelectrics Studied by Atomic-Force Microscopy. *J Vac Sci Technol B* **13**, 1095 (May-Jun, 1995).

23. B. T. Rosner, D. W. van der Weide, High-frequency near-field microscopy. *Rev Sci Instrum* **73**, 2505 (Jul, 2002).
24. F. J. Giessibl, Advances in atomic force microscopy. *Reviews of Modern Physics* **75**, 949 (Jul, 2003).
25. G. Meyer, N. M. Amer, Novel Optical Approach to Atomic Force Microscopy. *Applied Physics Letters* **53**, 1045 (Sep 19, 1988).
26. V. Garcia *et al.*, Giant tunnel electroresistance for non-destructive readout of ferroelectric states. *Nature* **460**, 81 (Jul 2, 2009).
27. B. J. Rodriguez, C. Callahan, S. V. Kalinin, R. Proksch, Dual-frequency resonance-tracking atomic force microscopy. *Nanotechnology* **18**, (Nov 28, 2007).
28. S. V. Kalinin *et al.*, Towards local electromechanical probing of cellular and biomolecular systems in a liquid environment. *Nanotechnology* **18**, (Oct 24, 2007).
29. M. Golosovsky, D. Davidov, Novel millimeter-wave near-field resistivity microscope. *Applied Physics Letters* **68**, 1579 (Mar 11, 1996).
30. M. Tabibazar, N. S. Shoemaker, S. Harris, Nondestructive Characterization of Materials by Evanescent Microwaves. *Meas Sci Technol* **4**, 583 (May, 1993).
31. Y. S. Cho, A. Kirihara, T. Saeki, Scanning nonlinear dielectric microscope. *Rev Sci Instrum* **67**, 2297 (Jun, 1996).
32. M. A. Kastner, The Single-Electron Transistor. *Reviews of Modern Physics* **64**, 849 (Jul, 1992).
33. R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, L. M. K. Vandersypen, Spins in few-electron quantum dots. *Reviews of Modern Physics* **79**, 1217 (Oct-Dec, 2007).
34. D. L. Klein, R. Roth, A. K. L. Lim, A. P. Alivisatos, P. L. McEuen, A single-electron transistor made from a cadmium selenide nanocrystal. *Nature* **389**, 699 (Oct 16, 1997).
35. S. Kubatkin *et al.*, Single-electron transistor of a single organic molecule with access to several redox states. *Nature* **425**, 698 (Oct 16, 2003).
36. C. Stampfer *et al.*, Tunable graphene single electron transistor. *Nano Letters* **8**, 2378 (Aug, 2008).
37. A. Ohtomo, H. Y. Hwang, A high-mobility electron gas at the LaAlO3/SrTiO3 heterointerface. *Nature* **427**, 423 (Jan 29, 2004).
38. S. Thiel, G. Hammerl, A. Schmehl, C. W. Schneider, J. Mannhart, Tunable quasi-two-dimensional electron gases in oxide heterostructures. *Science* **313**, 1942 (Sep 29, 2006).
39. C. Cen *et al.*, Nanoscale control of an interfacial metal-insulator transition at room temperature. *Nature Materials* **7**, 298 (Mar, 2008).
40. C. Cen, S. Thiel, J. Mannhart, J. Levy, Oxide Nanoelectronics on Demand. *Science* **323**, 1026 (Feb 20, 2009).
41. D. F. Bogorin *et al.*, Nanoscale rectification at the LaAlO3/SrTiO3 interface. *Applied Physics Letters* **97**, (Jul 5, 2010).
42. P. Irvin *et al.*, Rewritable nanoscale oxide photodetector. *Nat Photonics* **4**, 849 (Dec, 2010).
43. N. Nakagawa, H. Y. Hwang, D. A. Muller, Why some interfaces cannot be sharp. *Nature Materials* **5**, 204 (Mar, 2006).
44. L. X. Zhang *et al.*, Origin of insulating behavior of the p-type LaAlO3/SrTiO3 interface: Polarization-induced asymmetric distribution of oxygen vacancies. *Physical Review B* **82**, (Sep 9, 2010).

45. F. Bi *et al.*, "Water-cycle" mechanism for writing and erasing nanostructures at the LaAlO3/SrTiO3 interface. *Applied Physics Letters* **97**, (Oct 25, 2010).
46. H. R. Zeller, I. Giaever, Tunneling, Zero-Bias Anomalies, and Small Superconductors. *Phys Rev* **181**, 789 (1969).
47. J. H. F. Scottthomas, S. B. Field, M. A. Kastner, H. I. Smith, D. A. Antoniadis, Conductance Oscillations Periodic in the Density of a One-Dimensional Electron-Gas. *Physical Review Letters* **62**, 583 (Jan 30, 1989).
48. M. Bockrath *et al.*, Single-electron transport in ropes of carbon nanotubes. *Science* **275**, 1922 (Mar 28, 1997).
49. L. J. Swenson, D. K. Wood, A. N. Cleland, Diffusion-based electron thermometry using a three-junction single-electron transistor. *Nano Letters* **7**, 1804 (Jun, 2007).
50. L. J. Guo, E. Leobandung, S. Y. Chou, A silicon single-electron transistor memory operating at room temperature. *Science* **275**, 649 (Jan 31, 1997).
51. A. Morello *et al.*, Single-shot readout of an electron spin in silicon. *Nature* **467**, 687 (Oct 7, 2010).
52. G. A. Steele *et al.*, Strong Coupling Between Single-Electron Tunneling and Nanomechanical Motion. *Science* **325**, 1103 (Aug 28, 2009).
53. H. T. A. Brenning *et al.*, A single electron transistor on an atomic force microscope probe. *Nano Letters* **6**, 937 (May, 2006).
54. H. vanHouten, C. W. J. Beenakker, A. A. M. Staring, Coulomb-BlockadeOscillationsinSemiconductor Nanostructures. *arXiv:cond-mat/0508454*.
55. L. P. Kouwenhoven, D. G. Austing, S. Tarucha, Few-electron quantum dots. *Rep Prog Phys* **64**, 701 (Jun, 2001).
56. H. W. Jang *et al.*, Ferroelectricity in Strain-Free SrTiO3 Thin Films. *Physical Review Letters* **104**, (May 14, 2010).
57. C. Cen, D. F. Bogorin, J. Levy, Thermal activation and quantum field emission in a sketch-based oxide nanotransistor. *Nanotechnology* **21**, (Nov 26, 2010).
58. G. Singh-Bhalla *et al.*, Built-in and induced polarization across LaAlO3/SrTiO3 heterojunctions. *Nature Physics* **7**, 80 (2010).
59. A. D. Caviglia *et al.*, Electric field control of the LaAlO3/SrTiO3 interface ground state. *Nature* **456**, 624 (Dec 4, 2008).
60. L. P. Kouwenhoven *et al.*, Excitation spectra of circular, few-electron quantum dots. *Science* **278**, 1788 (Dec 5, 1997).
61. S. Tarucha, D. G. Austing, T. Honda, R. J. vanderHage, L. P. Kouwenhoven, Shell filling and spin effects in a few electron quantum dot. *Physical Review Letters* **77**, 3613 (Oct 21, 1996).
62. M. Fricke, A. Lorke, J. P. Kotthaus, G. Medeiros Ribeiro, P. M. Petroff, Shell structure and electron-electron interaction in self-assembled InAs quantum dots. *Europhysics Letters* **36**, 197 (Oct 20, 1996).
63. K. A. Muller, H. Burkard, Srtio3 - Intrinsic Quantum Para-Electric Below 4-K. *Physical Review B* **19**, 3593 (1979).
64. D. Goldhaber-Gordon *et al.*, Kondo effect in a single-electron transistor. *Nature* **391**, 156 (Jan 8, 1998).
65. J. W. Park *et al.*, Creation of a two-dimensional electron gas at an oxide interface on silicon. *Nat Commun* **1**, (Oct, 2010).

66. R. G. Knobel, A. N. Cleland, Nanometre-scale displacement sensing using a single electron transistor. *Nature* **424**, 291 (Jul 17, 2003).
67. D. Loss, D. P. DiVincenzo, Quantum computation with quantum dots. *Physical Review A* **57**, 120 (Jan, 1998).
68. D. Jaksch, P. Zoller, The cold atom Hubbard toolbox. *Ann Phys-New York* **315**, 52 (Jan, 2005).
69. J. E. Lilienfeld, Device for controlling electric current. *US Patent* **No. 1900018**, (1928).
70. I. M. Ross, Semiconductive translating device. *U.S. Patent* **No. 2791760**, (1957).
71. T. P. Ma, J.-p. Han, Why is nonvolatile ferroelectric memory field-effect transistor still elusive? *Ieee Electron Device Letters* **23**, 386 (2002).
72. S. Salahuddin, S. Datta, Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano Letters* **8**, 405 (2008).
73. V. V. Zhirnov, R. K. Cavin, Nanoelectronics - Negative capacitance to the rescue? *Nature Nanotechnology* **3**, 77 (Feb, 2008).
74. H. Ishiwara, M. Okuyama, Y. Arimoto, Ferroelectric random access memories: fundamentals and applications. *Springer*, (2004).
75. S. L. Miller, P. J. Mcwhorter, Physics of the Ferroelectric Nonvolatile Memory Field-Effect Transistor. *Journal of Applied Physics* **72**, 5999 (Dec 15, 1992).
76. J. L. Moll, Y. Tarui, A new solid state memory resistor. *IEEE Trans. Electron Devices* **ED-10**, (1963).
77. P. M. Heyman, G. H. Heilmeier, A. f. f. e. d. P. I. (1966). A ferroelectric field effect device. *Proc. IEEE* **54**, 842 (1966).
78. C. H. Ahn *et al.*, Ferroelectric Field-Effect in Epitaxial Thin-Film Oxide Srcuo2/Pb(Zr0.52ti0.48)O-3 Heterostructures. *Science* **269**, 373 (Jul 21, 1995).
79. S. Mathews, R. Ramesh, T. Venkatesan, J. Benedetto, Ferroelectric field effect transistor based on epitaxial perovskite heterostructures. *Science* **276**, 238 (Apr 11, 1997).
80. W. Y. Fu, Z. Xu, X. D. Bai, C. Z. Gu, E. G. Wang, Intrinsic Memory Function of Carbon Nanotube-based Ferroelectric Field-Effect Transistor. *Nano Letters* **9**, 921 (Mar, 2009).
81. R. C. G. Naber, B. de Boer, P. W. M. Blom, D. M. de Leeuw, Low-voltage polymer field-effect transistors for nonvolatile memories. *Applied Physics Letters* **87**, (2005).
82. R. C. G. Naber *et al.*, High-performance solution-processed polymer ferroelectric field-effect transistors. *Nature Materials* **4**, 243 (Mar, 2005).
83. N. A. Basit, H. K. Kim, J. Blachere, Growth of highly oriented Pb(Zr,Ti)O-3 films on MgO-buffered oxidized Si substrates and its application to ferroelectric nonvolatile memory field-effect transistors. *Applied Physics Letters* **73**, 3941 (Dec 28, 1998).
84. S.-Y. Wu, A new ferroelectric memory device, metal-ferroelectric-semiconductor transistor. *IEEE Trans. Electron Devices* **21**, (1974).
85. J. Yu *et al.*, Formation and characteristics of Pb(Zr,Ti)O3 field-effect transistor with a SiO2 buffer layer. *Applied Physics Letters* **70**, 490 (1997).
86. M. Alexe, Measurement of interface trap states in metal-ferroelectric-silicon heterostructures. *Applied Physics Letters* **72**, 2283 (1998).
87. C. T. Black, C. Farrell, T. J. Licata, Suppression of ferroelectric polarization by an adjustable depolarization field. *Applied Physics Letters* **71**, 2041 (Oct 6, 1997).
88. M. Takahashi *et al.*, Analysis and improvement of retention time of memorized state of metal-ferroelectric-insulator-semiconductor structure for ferroelectric gate FET memory. *Jpn J Appl Phys 1* **40**, 2923 (Apr, 2001).

89. H. Ishiwar, Current status and prospects of FET-type ferreoelctric memories. *JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE* **1**, 1 (2001).
90. N. A. Pertsev, A. K. Tagantsev, N. Setter, Phase transitions and strain-induced ferroelectricity in SrTiO3 epitaxial thin films. *Physical Review B* **61**, R825 (Jan 1, 2000).
91. H. Li *et al.*, Two-dimensional growth of high-quality strontium titanate thin films on Si. *J. Appl. Phys.* **93**, (2003).
92. S. V. Kalinin, D. A. Bonnell, Imaging mechanism of piezoresponse force microscopy of ferroelectric surfaces. *Physical Review B* **65**, 125408 (Mar 15, 2002).
93. W. R. Thurber, R. L. Mattis, Y. M. Liu, J. J. Filliben, Resistivity-Dopant Density Relationship for Phosphorus-Doped Silicon. *J Electrochem Soc* **127**, 1807 (1980).
94. W. R. Thurber, R. L. Mattis, Y. M. Liu, J. J. Filliben, Resistivity-Dopant Density Relationship for Boron-Doped Silicon. *J Electrochem Soc* **127**, 2291 (1980).
95. E. Y. Tsymbal, H. Kohlstedt, Applied physics - Tunneling across a ferroelectric. *Science* **313**, 181 (Jul 14, 2006).
96. M. Gajek *et al.*, Tunnel junctions with multiferroic barriers. *Nature Materials* **6**, 296 (Apr, 2007).
97. G. Gerra, A. K. Tagantsev, N. Setter, K. Parlinski, Ionic polarizability of conductive metal oxides and critical thickness for ferroelectricity in BaTiO3. *Physical Review Letters* **96**, 107603 (Mar 17, 2006).
98. H. Kohlstedt, N. A. Pertsev, J. R. Contreras, R. Waser, Theoretical current-voltage characteristics of ferroelectric tunnel junctions. *Physical Review B* **72**, 125341 (Sep, 2005).
99. M. Y. Zhuravlev, R. F. Sabirianov, S. S. Jaswal, E. Y. Tsymbal, Giant electroresistance in ferroelectric tunnel junctions. *Physical Review Letters* **94**, 246802 (Jun 24, 2005).
100. J. Berezovsky *et al.*, Nondestructive optical measurements of a single electron spin in a quantum dot. *Science* **314**, 1916 (Dec 22, 2006).
101. J. Berezovsky, M. H. Mikkelsen, N. G. Stoltz, L. A. Coldren, D. D. Awschalom, Picosecond coherent optical manipulation of a single electron spin in a quantum dot. *Science* **320**, 349 (Apr 18, 2008).
102. M. Atature, J. Dreiser, A. Badolato, A. Imamoglu, Observation of Faraday rotation from a single confined spin. *Nature Physics* **3**, 101 (Feb, 2007).
103. A. J. Ramsay *et al.*, Fast optical preparation, control, and readout of a single quantum dot spin. *Physical Review Letters* **100**, (May 16, 2008).
104. G. Medeiros-Ribeiro, E. Ribeiro, H. Westfahl, g-factor engineering and control in self-assembled quantum dots. *Appl Phys a-Mater* **77**, 725 (Nov, 2003).
105. G. Medeiros-Ribeiro, J. M. Garcia, P. M. Petroff, Charging dynamics of InAs self-assembled quantum dots. *Physical Review B* **56**, 3609 (Aug 15, 1997).
106. P. Michler, Single Quantum Dots: Fundamentals, Applications, and New Concepts. *Springer*, (2003).
107. P. S. Fodor, H. Zhu, N. G. Patil, J. Jevy, Variable-temperature scanning optical and force microscope. *Rev Sci Instrum* **75**, 2971 (Sep, 2004).
108. T. Tran, D. R. Oliver, D. J. Thomson, G. E. Bridges, "Zeptofarad" (10(-21) F) resolution capacitance sensor for scanning capacitance microscopy. *Rev Sci Instrum* **72**, 2618 (Jun, 2001).
109. D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, The missing memristor found. *Nature* **453**, 80 (May 1, 2008).

110. J. Borghetti *et al.*, 'Memristive' switches enable 'stateful' logic operations via material implication. *Nature* **464**, 873 (Apr 8, 2010).
111. L. O. Chua, Memristor - Missing Circuit Element. *Ieee T Circuits Syst* **Ct18**, 507 (1971).
112. R. S. Williams, http://www.hpl.hp.com/news/2008/apr-jun/memristor_faq.html.
113. B. J. Choi *et al.*, Resistive switching mechanism of TiO2 thin films grown by atomic-layer deposition. *Journal of Applied Physics* **98**, (Aug 1, 2005).
114. K. M. Kim, B. J. Choi, Y. C. Shin, S. Choi, C. S. Hwang, Anode-interface localized filamentary mechanism in resistive switching of TiO2 thin films. *Applied Physics Letters* **91**, (Jul 2, 2007).
115. C. Rohde *et al.*, Identification of a determining parameter for resistive switching of TiO2 thin films. *Applied Physics Letters* **86**, (Jun 27, 2005).
116. D. S. Jeong, H. Schroeder, U. Breuer, R. Waser, Characteristic electroforming behavior in Pt/TiO2/Pt resistive switching cells depending on atmosphere. *Journal of Applied Physics* **104**, (Dec 15, 2008).
117. J. J. Yang *et al.*, Memristive switching mechanism for metal/oxide/metal nanodevices. *Nature Nanotechnology* **3**, 429 (Jul, 2008).
118. D. H. Kwon *et al.*, Atomic structure of conducting nanofilaments in TiO2 resistive switching memory. *Nature Nanotechnology* **5**, 148 (Feb, 2010).
119. J. P. Strachan *et al.*, Direct Identification of the Conducting Channels in a Functioning Memristive Device. *Advanced Materials* **22**, 3573 (Aug 24, 2010).
120. F. Miao *et al.*, Force modulation of tunnel gaps in metal oxide memristive nanoswitches. *Applied Physics Letters* **95**, (Sep 14, 2009).
121. A. C. Torrezan, T. P. M. Alegre, G. Medeiros-Ribeiro, Microstrip resonators for electron paramagnetic resonance experiments. *Rev Sci Instrum* **80**, (Jul, 2009).
122. R. Waser, M. Aono, Nanoionics-based resistive switching memories. *Nature Materials* **6**, 833 (Nov, 2007).
123. J. P. Strachan, *Unpublished*.
124. P. Zahl, M. Bierkandt, S. Schroder, A. Klust, The flexible and modern open source scanning probe microscopy software package GXSM. *Rev Sci Instrum* **74**, 1222 (Mar, 2003).
125. P. Zahl, T. Wagner, R. Moller, A. Klust, Open source scanning probe microscopy control software package GXSM. *J Vac Sci Technol B* **28**, (May, 2010).