PRELIMINARY FEASIBILITY STUDY OF SILICON ON INSULATOR (SOI) MICROPHONES

by

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ABSTRACT

PRELIMINARY FEASIBILITY STUDY OF SILICON ON INSULATOR (SOI) MICROPHONES

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This work discusses the feasibility of fabricating capacitive microphones from SOI wafers. Many current designs of capacitive microphones are fabricated by processing two individual wafers and then bonding them together afterwards. If successful, SOI wafers would offer the ability to make the microphones on one wafer and eliminate the possibility of alignment problems. The ultimate goal was to create functioning microphone membranes with different geometries and mechanically test their deflection under acoustic actuation.

Several microphone designs were examined and discussed. The fabrication process of creating the capacitive microphones from SOI wafers is discussed in full detail, and the four main process steps include fabrication, observation, modeling, and dynamic characterization. The fabrication process was altered between trials in order to produce better results, such as changing the etching time, etching acid, and drying process. Once the microphones were fabricated, they were observed with an SEM machine to examine the surfaces and cross-sections. Four membrane thicknesses were modeled in ANSYS and a nonlinear static analysis was performed to predict the deflection of the membrane and the natural frequencies were calculated. The microphones were also mechanically tested with two different methods, the Microvision system and a fotonic sensor, to measure the deflection of the fabricated membrane.

Overall, there were five square microphone sizes fabricated, which included 1/2", 1/4", 1/8", 1/16", and 1/32". They were fabricated on two different SOI wafers. The first wafer had a membrane thickness of 20 microns while the second wafer had a 4 micron thickness. The SEM images taken after each trial were used to determine the success of the fabrication process. The calculation of natural frequencies was used to indicate which membranes could be actuated. Some, mostly the smaller sizes, were proven to be too stiff to allow for recordable deflection. The ANSYS results were used as a comparison to the tested results and provided information for which geometries were better suited under different pressures. At higher pressures, the larger microphones are predicted to have a deflection larger than the gap between the membrane and the backplate, so those pressures would not be suitable for typical sound pressure levels experienced for testing. It also again proved that the smaller microphones were too stiff to get a measurable deflection. The microphones that had the most promise were the 1/2" 20 micron membrane and the 1/4" 4 micron membrane. There were many inconsistencies in the mechanical test data which suggest that stiction is a problem. However, the use of a profilometer showed thin cracks in the membranes.

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NOMENCLATURE

Chemical Symbols	Meaning
Au	Gold
$(CH_3)_4NOH$	Tetramethyl Ammonium Hydroxide
Cr	Chromium
H_2O_2	Hydrogen Peroxide
H_2SO_4	Sulfuric Acid
HF	Hydrofluoric Acid
NH_4F	Ammonium Fluoride
Pt	Platinum
Si	Silicon
Si_3N_4	Silicon Nitride
SF_6	Sulphur Hexafluoride
SiO_2	Silicon Dioxide
Ti	Titanium
ZnO	Zinc Oxide

Equation Symbols	Meaning
C	Capacitance
CC	Center to Center Hole Distance
d	Edge to Hole Center Distance
E	Modulus of Elasticity
f_{ij}	Natural Frequency
h	Material Thickness
L	Length
n	Number of Hole Spacings
Q	Charge
R	Etch Rate
t	Time
V	Voltage
γ	Mass per Unit Area
λ_{ij}	Frequency Parameter
μ	Density
ν	Poisson's Ratio

Acronyms	Meaning
BOE	Buffered Oxide Etch
CVD	Chemical Vapor Deposition
DRIE	Deep Reactive Ion Etching
EDP	Ethylene Diamine Pyrochatechol
FET	Field-effect Transistors
FRF	Frequency Response Function
HMDS	Hexamethyldisilazane
IC	Integrated Circuit
IPA	Isopropyl Alcohol
KOH	Potassium Hydroxide
LPCVD	Low Pressure Chemical Vapor Deposition
MEMS	Microelectromechanical Systems
MOS	Metal Oxide Semiconductor
MST	Microsystems Technology
PECVD	Plasma Enhanced Chemical Vapor Deposition
PZT	Lead Zirconate Titanate
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
SIMOX	Separated by Implanted Oxygen
SOI	Silicon on Insulator
TMAH	Tetramethyl Ammonium Hydroxide

1.0 INTRODUCTION

A largely growing field in engineering is that of micro-scaled systems. This field is known by various names throughout the world, such as microsystems technology (MST) in Europe, micromachines in Japan, and microelectromechanical systems (MEMS) in the United States. MEMS are microminiature systems that combine mechanical and electrical devices through utilizing microfabrication technology [7], and can range in size from micrometers to millimeters, and can be fabricated to function individually or in large arrays [12].

The fabrication process for MEMS has mostly been taken from the integrated circuit (IC) industry, which was developed in the 1980's. The IC micromachining process was initially used to create miniature electrical devices and was then extended to include the fabrication of microdevices [7, 17]. The use of IC micromachining provides the three main benefits of miniaturization, multiplicity, and microelectronics. Miniaturization is important to create devices that can handle smaller objects or to work in small spaces. Through many different fabrication techniques, the mass production of a single device is easy. The microdevice should be able to work individually, but it is also important that it can be made into an array to create a cooperative system that can achieve better results than a single device. Due to the similarity between MEMS and IC technology, the coordination and control of MEMS devices can be integrated with microelectronics [7, 12].

Due to the significant impact MEMS can have for both commercial and military applications, both industry and government have taken an interest in seeing the field grow. There are several different markets for MEMS but no single dominant application. Some examples of the MEMS application are in optics, transportation and aerospace, robotics,

medical, fluidics and chemical analysis, bio technology, and information technology. Some present commercial applications include automotive safety, braking, and suspension systems, compact computer display projectors, and telecommunication optical fiber components and switches. For the military, MEMS applications are used for security surveillance, miniature fluidic systems for propellant and combustion control, and for aerodynamic control of aircraft. It is expected that the MEMS field will continue to grow and flourish as can be seen from Table 1 that shows projected values for 2004 [17].

Table 1: Analysis and Forecast of US MEMS Markets (in millions of US dollars)

Year	Automotive	Medical	Information Tech. and Industrial	Military and Aerospace
1994	255.7	129.5	438.3	49.1
1996	355.0	164.4	492.8	62.2
1998	491.5	216.7	575.3	79.6
2000	645.7	291.3	733.3	110.7
2002	879.6	444.7	995.1	156.9
2004†	1172.0	716.0	1514.0	202.7

†Projected figures

One of the earliest and most successful MEMS applications was for inkjet printer cartridges. For this application, MEMS technology was used to make a head element that contained a large number of elements that form and shoot tiny droplets of ink at the paper. The MEMS design offered a faster high-resolution color printer. During its development, there was no available technology in use to help with the printer design. Through the use of research and several demonstrations, a new technology was developed that drastically changed the printing industry [25].

Another notable MEMS application is in the automotive industry. MEMS technology was used to create accelerometers to control airbag deployment. Before using MEMS ac-

celerometers, earlier airbags required several accelerometers to be mounted in the front of the vehicle with separate electronics closer to the airbag. Normally, two sensors would be placed closer to the front bumper and a third would be placed closer to the airbag. The sensors then had to be wired together. Through the use of MEMS, single-point sensing was made possible by integrating the accelerometer and electronic parts onto a single chip. The newer sensor reduces the number of sensors in the system and the associated wiring, lowers the cost, and provides a quicker response [16].

1.1 SILICON AS A MATERIAL

Silicon has been used in micromachining since the 1960's, when it was first used in integrated circuit technology. Research on silicon etching during the 1960's-1970's led to silicon's use in pressure transducers. By the end of the 1980's, micromechanisms and electrostatic micromotors were demonstrated with surface micromachining. It was not until the 1990's that MEMS were fabricated with silicon through the use of these technologies [5].

Silicon is a material that can be manufactured in single crystal substrates, the preferred material to make MEMS devices, which provides many electrical and mechanical advantages [8, 17]. Most researchers credit silicon's success for miniaturization to four main factors. It is an abundant inexpensive material that can be produced and processed to unparalleled standards of purity and perfection. The processing technique for silicon is based on thin deposited films, making the process agreeable to miniaturization. Photographic techniques can be used to define and reproduce the device shapes and patterns which is also useful in the miniature world. However, the most important feature of silicon is its ability to be batch-fabricated [20]. While silicon is the most common material for fabricating sensors, other materials used for microsystems include silicon oxides, nitrides, and carbides and metals such as aluminum, titanium, tungsten, gold, and copper.

1.1.1 Silicon as a Semiconductor

There are three main classifications of materials based on their ability to conduct electricity. In order of increasing conductivity, materials are classified as insulators, semiconductors, or conductors. In order for a material to conduct electricity, its electrons must have the energy to jump over the energy gap and move from the valence band into the conduction band. The energy gap is in units of electron volt (eV) and varies from material to material. In insulators, such as quartz and diamond, the gap is large and ranges from about 3 eV to 6 eV. Due to the large gap, very few electrons have the energy to move into the conduction band. Semiconductors have a gap range of 0.1 to 1 eV [6, 28], making it a possibility for free electrons to jump over the gap. In conductors, such as metals, the valence band and the conduction band overlap. This allows for the electrons to move freely into the conduction band. A representation of the band structures are shown below in Figure 1 [28].

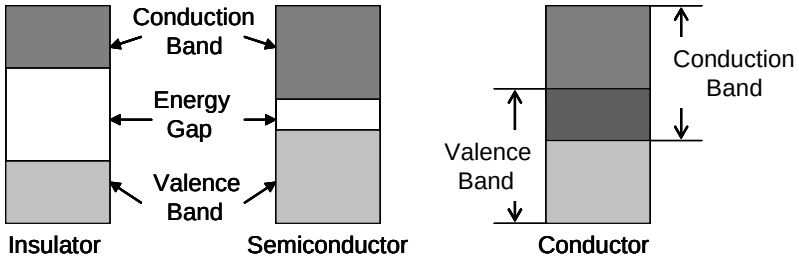

Figure 1: Models of the Three Band Structures

Silicon is classified as a semiconductor. Under normal conditions, semiconductors are poor conductors because there are no loosely held electrons. However, there are ways to alter the material's crystal structure in order to obtain free electrons and change the electrical conductivity of the material. This is done by using higher temperatures, applying strong electric fields, or by adding impurities to the material.

The addition of impurities or foreign atoms to a material is called doping. There are two types of doping, n and p. Using n-type doping, an excess of electrons is added to the

material while p-type doping adds holes in the material. Arsenic, antimony, and phosphorous are common n-type dopants for silicon and the most common dopant for p-type silicon is boron [17].

1.1.2 Single Silicon Wafers

Purchased silicon wafers are characterized by their orientation cut and by their doping level. The silicon is cut into thin wafers along specific crystal planes. The orientation cut then lies along the top surface of the wafer [17]. The most common orientations of wafers are (100)-oriented and (111)-oriented cuts. The wafers are also marked with "flats", which are used to show the orientation of specific planes within the wafer [13]. Typical configurations of four wafers are shown below in Figure 2 [25].

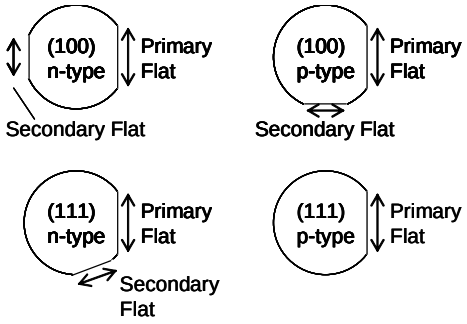

Figure 2: Orientation and Doping Type

1.1.3 SOI Wafers

Another type of silicon wafer available for purchase is the silicon on insulator (SOI) wafer. An SOI wafer has a layer of silicon dioxide sandwiched between two layers of single crystal silicon or polysilicon. This type of wafer is made by two main techniques: SIMOX (Separated by IMplanted OXygen) and bonded wafers. In the SIMOX process, the silicon wafer is implanted

with oxygen ions and the ions interact with silicon during an annealing process to form the buried oxide layer. The oxide layer can be controlled by changing the energy and dose of the implanted oxygen and the annealing temperature [17]. SOI wafers can also be made by bonding a base silicon wafer and a wafer with a grown oxide layer together. They are bonded through annealing [11]. After the annealing process, they can then be thinned through a polishing process. These two processes are shown below in Figure 3 [17].

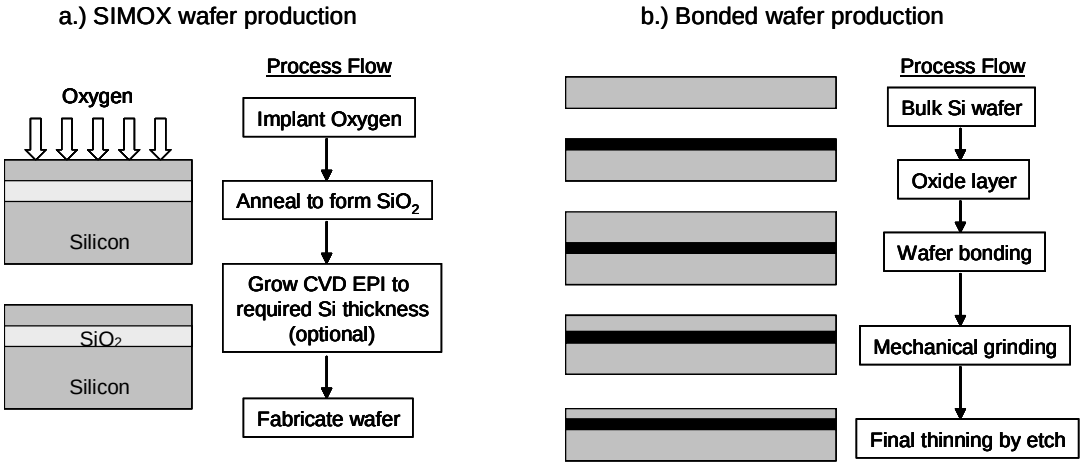

Figure 3: Comparison of a.)SIMOX and b.)Bonded SOI Wafers

The main purposes for using SOI wafers are for an etch stop, dielectric isolation, and sacrificial layer. The buried silicon dioxide layer can serve as an etch stop for many etchants that have a good selectivity of Si over SiO_2. The dielectric isolation of the wafer allows for the production of high temperature sensors, which can not be done when relying on p-n junction isolation. Dielectric isolation is also useful in fabricating components on a single chip. The third important application of SOI wafers is the use of the oxide as a sacrificial layer. With the oxide layer sandwiched in between the silicon layers, the release of the oxide can easily create cantilever beams and membranes.

1.2 MICROMACHINING, DEPOSITION, AND ETCHING

There are two main types of micromachining. Surface micromachining is an additive process that that uses a combination of sacrificial material layers and spacer material layers to create the mechanical parts above the silicon substrate's surface with deposited films. Bulk or substrate micromachining, which will be used in this project, is a subtractive process that creates the mechanical part by removing, or etching, the silicon substrate [5, 13]. The difference between the two processes can be seen in Figure 4 [13] below.

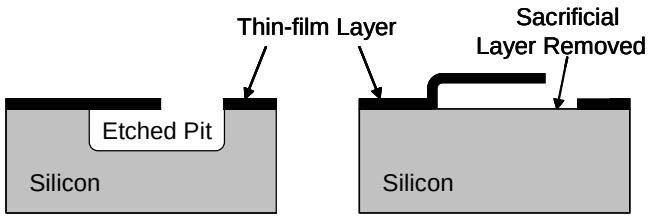

Figure 4: Bulk (left) and Surface (right) Micromachining of a Cantilever Beam

Surface micromachining relies heavily on adding layers of material to the substrate and removing sections of those layers through etching [25]. Many types of materials can be added onto the substrate, but the most popular are silicon dioxide, silicon nitride, polysilicon, organic compounds, and metallics. The thin layers can be placed onto the substrate by several methods. For example, silicon dioxide can be thermally grown through oxidation. Films can also be deposited by spin casting, sputtering, and evaporation methods. Spin casting uses a material that is dissolved in a suitable solvent. The solution is then applied to the wafer and spun at a high speed to allow the wafer to be uniformly covered. The wafer and solution are then baked to remove any excess solution. Sputtering requires the use of chemically inert atoms which are ionized in a plasma. These atoms are accelerated at a target and the atoms that are knocked out are allowed to reach the substrate. Evaporation, which is used mostly for metals, takes a heated metal sample and deposits the metal on the substrate through the flux of vapor atoms.

While the previous methods are all successful methods of depositing thin films, one of the most popular methods is by Chemical Vapor Deposition (CVD) [16]. The CVD process causes heated materials to come into contact with the substrate, allowing a chemical reaction to take place at the surface. This reaction causes the material's deposition onto the substrate. There are several different types of CVD processes, but the two referred to the most in this work will be LPCVD and PECVD. Low Pressure Chemical Vapor Deposition (LPCVD) is used at high temperatures between 550 and 600°C and offers good uniformity of the thin film layer. It is used primarily on doped and undoped high temperature oxides, silicon nitride, and polysilicon. The other CVD process that is used quite often in MEMS work, is Plasma-Enhanced Chemical Vapor Deposition (PECVD). This type of process provides very good adhesion, but is open to contamination by chemicals and particulates. PECVD operates at much lower temperatures, ranging from -300 to -400°C and is best used for low-temperature insulators over metals and passivation layers such as nitride.

Bulk micromachining is achieved by using etchants to remove the material and etch-stops to block the etchant from removing too much material. The etchants can either be isotropic or anisotropic. Isotropic etchants cause the material to be removed in a fairly equal rate in all directions and tends to create structures with rounded features. Sharply defined features, such as flat surfaces and sharp angles, are the result of an anisotropic etching process where the removal of material tends to progress in a preferred direction [13]. In some cases, both anistropic and isotropic etchants can be used to reduce the etch time and provide better selectivity and geometry control than using only one type of etching process. This type of process is known as combinational etching [29]. The etchants can also be classified into two different categories, wet or dry. Wet etchants rely on aqueous chemistries and have an advantage of offering inexpensive batch fabrication, while dry etchants use vapors and plasma along with equipment such as pipes and a vacuum chamber [17].

When using a silicon substrate, wet isotropic etching has several problems. It is difficult to mask with high precision while using a simple mask material such as SiO_2. The etch rate

is also very sensitive to agitation and temperature, making it hard to control the geometry during the etch process [16].

The rate of material removal for anisotropic etchants depends on the orientation of the crystal planes of the material. Crystallography uses a system known as Miller indices to specify planes in crystalline lattices. There are four notations of Miller indices to specify the difference between referring to a specific crystal plane or a family of planes, as is shown in Table 2 below.

Table 2: Notation for Miller Indices

Notation	Meaning
(ijk)	a specific crystal plane or face
{ijk}	a family of equivalent planes
[ijk]	a specific direction of a unit vector
<ijk>	a family of equivalent directions

Planes are designated by three numbers enclosed in parenthesis, one for each coordinate direction in the unit cell. For example, (011) indicates a plane that never intersects the x-axis, intersects the y-axis at a distance **b** from the origin, and intersects the z-axis at a distance **c** from the origin. Figure 5 shows the Miller indices in a cubic lattice.

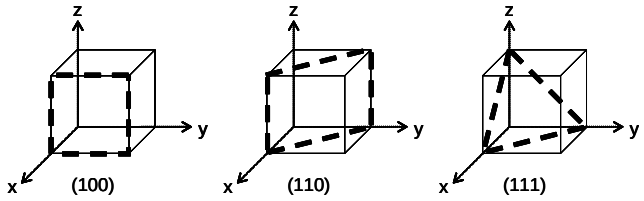

Figure 5: Miller Indices in a Cubic Lattice

The results of etching in the three planes are different, so the crystal orientation of the material must be specified before prescribing the exact etching process. The most common

etching planes have either (100) or (110) surface planes. Since the highest atom-packing density is found in the (111) plane, this plane is generally not attacked by the etchant and therefore not used as an etching plane [16]. The (111) plane will stop the etchant at 54.74° to the material's surface or perpendicular to the surface for the (100) and (110) planes respectively [14]. This is illustrated in Figure 6 below [13].

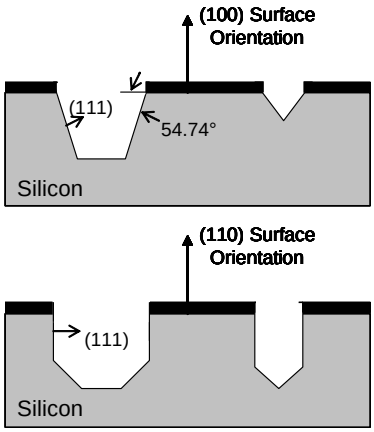

Figure 6: Anisotropic Wet Etching in the (100) and (110) Planes

1.2.1 Silicon Etchants

In order to choose the most appropriate etchant, the following issues must be considered: ease of handling, toxicity, etch rate, etch stop, etch selectivity over other materials, and mask material [16]. The three most widely used wet silicon anisotropic etchants are Ethylene diamine pyrochatechol (EDP), alkali hydroxides, and ammonium hydroxides, whose characteristics will be explained in depth below.

EDP was a popular etchant for many years. It has a selectivity to {111} planes and to p-doped silicon. This means that EDP will not etch the {111} planes or doped silicon as fast as the other planes. Due to this, heavy boron doping can be used as an etch stop. It can be masked by a variety of materials such as silicon oxides and nitrides, gold, chromium, and

copper [17]. The process is generally performed at temperatures between 110-120°C. The main advantage to using EDP is its smoothness of the etched surface and high selectivity between SiO_2 and silicon, making SiO_2 an ideal masking material [29]. Recently, EDP has not been used as frequently due to its hazardous nature. It is a highly dangerous nerve toxin and carcinogenic etchant and has recently been banned in most integrated circuit fabrication facilities. EDP must also be kept in a pure nitrogen environment since exposure to oxygen forms benzoquinone, which causes uncontrollable increases in the etch rate [4].

The second possibility for a silicon etchant includes the group of alkali hydroxides. Of the group, the most popular is KOH, potassium hydroxide. KOH is a simple system that is selective to the {111} plane and heavily doped p-type (p^{++}) silicon. Both boron and p^{++} doping can be used as etch stops [17]. Most KOH etches are performed around 80°C, where etching produces a uniform and bright surface. When performed above that temperature, the process can cause non-uniformity in the material. Hydrogen bubbles are formed along the silicon surface causing roughness, but can mostly be removed by agitating the etchant [16]. KOH is a skin irritant and is corrosive to the eyes and mucous membranes. The main disadvantages to KOH are that it is not compatible with the IC fabrication process and it etches SiO_2 at a rate too fast for it to be used as a mask, making Si_3N_4 the main masking material [4].

The last main type of etchant for silicon is in the ammonium hydroxide group, where tetramethyl ammonium hydroxide (TMAH or $(CH_3)_4NOH$) is the most popular etchant. TMAH is nontoxic, can be handled easily, does not decompose below 130°C, and shows good selectivity to silicon oxides and nitrides. If the etchant is prepared properly, TMAH can become selective to aluminum, making it fully IC-compatible [16, 18]. Both p-doped silicon and boron can be used as etch stops and TMAH is also selective to the {111} planes of silicon. This etchant is a strong base that is stable and colorless that can cause irritation to the skin, eyes, and mucous membranes [4]. The drawback to using TMAH is its slow etch rate and its tendency to cause rough surfaces. For most typical TMAH solutions, the etch rate and the surface roughness are decreased by increasing the TMAH concentration [14]

and at temperatures around 95°C, TMAH etching produces similar results to KOH etching [29]. Another way to produce smoother surfaces after etching is to include isopropyl alcohol, IPA, to the TMAH solution. At TMAH solutions of 25% wt, the addition of IPA improves the smoothness of the etched surface and decreases the appearance of micropyramids. While IPA-included solutions do not effect the etch rates of the masking layers, its presence reduces the undercutting ratios [18].

If vertical wall features are required, it is better to use a dry etching process called Reactive Ion Etching (RIE). RIE is a physically assisted chemical reaction that uses ion bombardment to etch away the material. The ions are directed straight downwards, causing the etch to be vertical. The six main steps in the RIE process include the following: (1)production of the reactive chemical species in the gas-phase, (2)diffusion of reactive species to the solid, (3)adsorption of reactive species into the solid, (4)diffusion over the surface and surface reaction, (5)reaction products leave through desorption, and (6)diffusion [16].

Finally, if a high-aspect-ratio is needed for vertical walls, Deep Reactive Ion Etching (DRIE) is used. This process allows for deeper etches by alternating between etching and deposition. DRIE etches the silicon for a specified period of time and then deposits a polymer layer on all exposed surfaces. This polymer layer acts as a guard to keep the lateral etching to a minimum. The polymer layer is quickly removed in the vertical direction when the etching continues. This process is highly selective to silicon dioxide and many photoresists, allowing either one to be used as a masking layer or an etch stop [13].

1.2.2 Silicon Dioxide Etchants

Some silicon etchants also etch silicon dioxide, such the wet etchants listed above. KOH will etch oxides at a faster rate than EDP or TMAH, but is still not considered the best etchant to use for oxides. Since oxide can be used as a good masking material and etch stop in the RIE process, it is not a suitable oxide etchant.

If oxide is used as a sacrificial layer along with a silicon substrate, it would be best to have an etchant that will not etch silicon. One of the most common oxide etchants is BOE,

which stands for buffered oxide etch. BOE is most commonly made of 6:1 40% NH_4F:49% HF. The HF causes the solution to attack oxides quickly. However, due to safety concerns and for better etching control, the HF is diluted before use [19]. However, if large portions of oxide must be removed, etching the oxide layer in a diluted 49% HF solution speeds up the etching rate by 5-10 times the rate of BOE.

Silicon dioxide etches equally in all directions so it is important to be able to control the etching. For example, if a vertical etch in oxide of 1 micron will result in a lateral etch to the right and left of 1 micron. This yields a hole of 1 micron high and 2 microns wide.

1.3 TRANSDUCERS

Transducers are devices that convert one form of energy into another. The two main types of transducers are actuators and sensors. Actuators convert thermal, electrical, and other forms of energy into mechanical energy and sensors convert different types of energy into electrical energy. Some typical examples of actuators include motors and pumps, while sensors typically measure parameters such as acceleration, temperature, and pressure. This project will ultimately focus on the fabrication and testing of silicon acoustic sensors used as microphones. The scope of the project will be limited however, to a study of the initial geometrical and mechanical feasibility of creating microphones from SOI wafers.

1.3.1 Acoustic Transducers

Microphones are a type of transducer that converts acoustical energy into electrical energy. In general, the main parts of the microphone are the diaphragm and the backplate. The diaphragm is a thin material section that vibrates due to the waves of acoustic pressure acting on its surface. The backplate, along with acoustic holes, allow the microphone's response to be tuned.

In general, microphones can be broken down into three types which include piezoelectric, piezoresistive, and capacitive. While most microphones work in a similar fashion, the different characteristics of each type of microphone will be explored further in Chapter 2.

1.4 THESIS TOPIC

This paper will focus on silicon acoustic sensors that will ultimately be used as microphones. The goal is to create acouso-mechanically functional microphones from SOI wafers, meaning that these microphones will not be electrically connected for this project. The final completed design would look similar to Figure 7, however this project focuses only on the upper two sections of the SOI wafer.

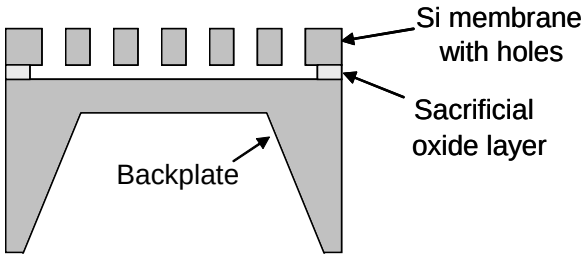

Figure 7: Completed Design of SOI Microphone

In this study, the functionality of the membranes from the SOI wafers will be examined. The capacitive microphones will be made from SOI wafers, allowing the oxide layer to be used as a sacrificial layer. The diaphragm will be made from the upper silicon layer and acoustic holes will be machined into the silicon. The acoustic holes will also act as etching holes for the buried oxide layer. Once the oxide is etched, the resulting microphone membranes can be tested.

In this project, five microphone sizes were studied, which included 1/2", 1/4", 1/8", 1/16", and 1/32" (in SI units of microns, the sizes are 0.0127, 0.00635, 0.003175, 0.001588,

and 0.0007938). The microphones are tested to see how the diaphragm responds as part of a mechanical study. By using different sized acoustic holes with different hole spacings, along with two membrane thicknesses, a geometrical study can be performed. Included in the geometrical study was a static analysis of four membrane thicknesses in motion under pressure. To observe the feasibility of the project, the cross-section of the microphones will be examined to see how the silicon holes are etched and if the oxide is etched uniformly. Although the microphones will not be electrically tested, mechanical measurements of the ensonified microphones will be made in order to evaluate their overall performance.

1.4.1 Thesis Organization

This work is organized into six main chapters. In order, the chapters are Introduction, Literature Review, Fabrication Process, Fabrication Results, Dynamic Characterization, and Conclusions and Future Work. The following Literature Review chapter discusses various microphone designs already completed and acts as an aid to better understand this work. The third chapter, Fabrication Process, discusses the process of making the microphones as well as some of the preliminary testing done to observe the membrane structures. Fabrication Results highlights the results of the microphones during the different stages of fabrication and discuss how they compared to expected results. The fifth chapter, Dynamic Characterization, discusses the dynamic testing of the microphone membranes and their results. Finally, the Conclusions and Future Work chapter discusses the overall work and findings of the project and also includes future directions.

2.0 LITERATURE REVIEW

There are three main types of microphones currently being used in MEMS devices. They include piezoelectric, piezoresistive, and capacitive (also known as condenser). This chapter will discuss the microphone designs already in the field and the differences between the various types of microphones. The first section will discuss piezoelectric microphones. The second and third sections will discuss piezoresistive microphones and capacitive microphones respectively. The final section will use a table to compare the differences of the individual microphone characteristics.

Overall, the main difference between the microphones is how they sense a change in the diaphragm. Piezoelectric microphones use piezoelectric material to generate an electric voltage in order to sense the movement of the membrane. Piezoresistors are used to sense the deflection of the membrane in piezoresistive microphones. Finally, capacitive microphones convert a change in capacitance into an electric signal.

2.1 PIEZOELECTRIC MICROPHONES

Piezoelectric microphones are single-chip transducers with no air-gap that use piezoelectric material to sense a change in the diaphragm. The piezoelectric material, mechanically coupled to the diaphragm, will sense any movement of the thin membrane. This movement causes stress in the piezoelectric material, which in turn generates an electric voltage [22]. Typically, these types of microphones have sensitivities ranging from 50 to 250 μV/Pa

along with frequency responses ranging from 10 Hz to 10 kHz. Their main disadvantage is considered to be their high noise level [13].

The first piezoelectric microphone was presented in 1983 by Royer et al [22]. This microphone had a 30 μm thick silicon diaphragm with a 3 mm diameter. Above the silicon, was a 3-5 μm ZnO layer sandwiched between two layers of silicon dioxide. The two oxide layers contained aluminum electrodes. A cross-sectional view of this microphone can be seen in Figure 8.

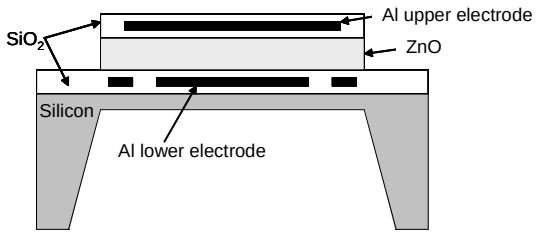

Figure 8: Cross-sectional View of Piezoelectric Microphone by Royer et al.

Another type of piezoelectric microphone was described by Bernstein et al. in 1997 [13], and was created as an underwater acoustic imager. This microphone used an array of sol-gel deposited lead zirconate titanate (PZT) as the piezoelectric layer. The microphone was made by oxidizing the silicon wafer, patterning the oxide, and then diffusing heavily doped boron into the silicon. The heavily doped regions were used as a masking material on the backside of the wafer and as an etch stop for the front side of the wafer. The wafer was oxidized again and then a Ti/Pt layer was deposited as a lower electrode. Next, a PZT layer was spun on, followed by an insulating layer of polyimide and another layer of Ti/Pt as the top electrode. The successful microphones had a final PZT thickness of 4 μm. The microphones were produced to emit and receive acoustic energy in water and had a frequency range from 0.3 to 2 MHz. Below, Figure 9 shows the cross-sectional view of the microphone.

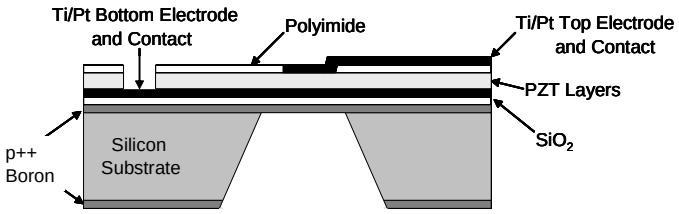

Figure 9: Cross-sectional View of Piezoelectric Microphone by Bernstein et al.

2.2 PIEZORESISTIVE MICROPHONES

The following section discusses piezoresistive microphones. These microphones can be made from a single chip, do not need an air-gap, and use four piezoresistors in a Wheatstone bridge configuration on top of the diaphragm. Two of the resistors are placed at the edge of the diaphragm while the other two are placed in the middle of the diaphragm. When the diaphragm deflects, the strains at the middle and the strains at the edge will have opposite signs, which causes an opposite resistance change in the piezoresistors [22]. Piezoresistive microphones generally have a sensitivity around 25 μV/Pa and have frequency responses that range from 100 Hz to 5 kHz [13].

In 1992, Schellin and Hess presented a piezoresistive microphone [24]. The microphone had a highly boron-doped silicon membrane. After doping the top side of the wafer, which was used as an etch stop, an insulating layer about 60 nm thick of silicon dioxide was grown onto both sides of the wafer. The next step was to use a atmospheric pressure chemical deposition to put down a 250 nm layer of polysilicon. This step was followed by boron implantation and an annealing process. The polysilicon was then patterned and plasma etched. Afterwards, a layer of silicon nitride was put down, patterned, and etched. the microphones could then be metallized with a 250 nm thick layer of aluminum. The silicon membrane had an area of 1 mm^2 and a thickness of 1 μm. The dimensions of the completed

microphone were 3 mm × 3 mm × 0.3 mm. The top view and cross-sectional view of the piezoresistive microphone is shown below in Figure 10.

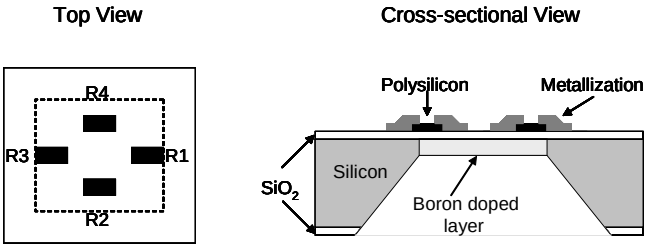

Figure 10: Top and Cross-sectional View of Piezoresistive Microphone by Schellin and Hess

2.3 CAPACITIVE MICROPHONES

The last major MEMS microphone type is the capacitive or condenser microphone. These microphones need to be biased with a DC voltage in order to operate. The exception to this are electret based microphones and field-effect transistors (FET) microphones.

Capacitive microphones operate on the principle of a variable capacitance. One electrode of the capacitor is on the diaphragm, which deflects inward or outward in response to an acoustic signal. The other electrode is on an adjacent stationary surface. Using the general equation for capacitance, as shown in Equation 2.1, a change in capacitance (C) results in a change in voltage (V) if the charge (Q) is held at a constant value.

$$V = \frac{Q}{C}. \tag{2.1}$$

The acoustic signal is converted into a capacitance change as the diaphragm deflects, which is then converted into an electric signal. When the diaphragm deflects into the microphone, decreasing the air gap size, the capacitance increases. If the diaphragm is deflected outward, then the potential increases. The output voltage is directly proportional to the diaphragm's displacement [6].

One drawback to the capacitive microphones is that the air gap causes damping, which decreases the sensitivity. However, there are three main ways to help reduce the damping problem. Thicker air gaps ranging between 5-20 μm in height reduce damping. Another method is to create grooves in the backplate in order to diminish the streaming losses. The third method to reduce damping is to incorporate a backplate with many holes [27]. Typical values for this type of microphone range from 0.2 to 25 mV/Pa in sensitivity, 1 to 20 pF for capacitance, and 10 Hz to 15 kHz for frequency response [13]. Overall, the bandwidth of the capacitive microphone is better than the other two types of microphones.

2.3.1 Electret Microphones

Electret microphones do not need external DC biasing due to their use of an electret material that stores a permanent charge. This material can be used in either the diaphragm or the backplate. The most common electret material is Teflon, followed by other polymers, aluminum-oxide, and silicon dioxide.

In 1984, Hohm and Gerhard-Multhaupt [9] presented the first electret silicon microphone that used silicon dioxide as the electret material. The silicon dioxide was 2 microns thick and liquid-contact charged to approximately -350 V. The oxide layer was the top layer of the p-type silicon backplate which had an area of 1 cm^2. The bottom electrode was made of 100 nm-thick vacuum-deposited aluminum. There was only one circular acoustic hole in this design, and it had a diameter of 1 mm. The hole was created in the center of the microphone by sand blasting through a mask. Mylar was used as a 30 micron spacer between the backplate and the diaphragm. The diaphragm was made of a 100 nm layer of aluminum coated with a 13 μm layer of Mylar. Below, Figure 11 shows the cross-sectional view.

2.3.2 FET Microphones

The other type of microphone that does not need an external DC bias is the FET microphone. These microphones use a biased membrane that forms a gate that moves relative to a fixed

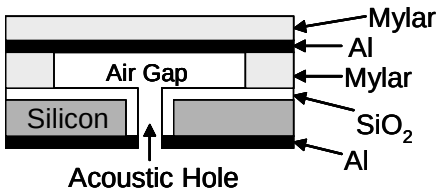

Figure 11: Cross-sectional View of Capacitive Electret Microphone by Hohm and Gerhard-Multhaupt

source and drain. The advantage of FET microphones is the low output impedance due to the preamplifier being integrated within the microphone. The disadvantage of this type of microphone is the absence of a bias element that defines a stable gate potential and its higher noise levels [13].

Kühnel [27] created a FET microphone in 1991. His design started with two silicon wafers with an oxide layer on the top side of each wafer. The backplate had a ridge that contained the highly n-doped source and drain regions along with a p-type channel of a Metal Oxide Semiconductor (MOS) transistor. The membrane chip had a silicon nitride diaphragm that was metalized with aluminum. The electrode acted as the moving gate. The air gap between the membrane and the gate oxide was 2 microns, and the source-drain ridge, only 110 microns thick, prevents large air-gap damping. The measured sensitivity for this microphone was between 0.1-1 mV and the frequency response was smooth up to 30 kHz. Figure 12 shows the cross-sectional view of the FET microphone [13].

2.3.3 Two Wafer Microphones

The majority of capacitive microphones are made by processing two individual wafers. One wafer is fabricated as the backplate while the other is fabricated as the diaphragm. Once the processes are completed, the wafers are bonded together to create the microphone. Most wafers are bonded together by using high temperature treatments or high electric

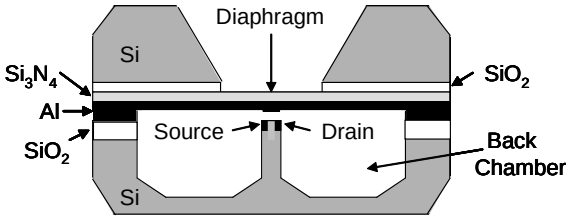

Figure 12: Cross-sectional View of FET Microphone by Kühnel

field strengths [22]. The disadvantage of using two wafers to create the microphone is in having to correctly align the wafers before the bonding step.

One of the earlier two-wafer designs was discussed by Hohm and Hess in 1986 [10]. The microphone was produced by fabricating two separate (100)-oriented p-type silicon wafers and then bonding the completed wafers together. The diaphragm was fabricated by covering the silicon on both sides in a 100 nm layer of oxide through thermal oxidation. This step was followed by depositing 150 nm layers of nitride on both sides through CVD at 800°C. The bottom side of the wafer was patterned to remove parts of the nitride and oxide layers and then the silicon and top oxide layer were etched with KOH to create a diaphragm membrane of 0.8×0.8 mm^2. The final step was the metallization of the diaphragm with a 100 nm layer of aluminum. The backplate was fabricated by creating an oxide layer of 2 microns through oxidation on both sides of the wafer. The bottom side of the wafer was patterned to create two rectangular slits that were 1 mm $\times$ 0.2 mm each after etching in EDP. The oxide layers were removed from both sides. A 2 micron oxide layer was deposited by CVD on the top outside edges to act as a spacer. Then another 2 micron layer of oxide was deposited by CVD, causing the top outside edges to have an oxide thickness of 4 microns. The final step to the backplate was to deposit a 0.5 micron aluminum layer. Figure 13 shows the completed device after bonding the two wafers together [10].

Higher sensitivity silicon microphones were shown in 1990 by Bergqvist and Rudolf [1]. These microphones had a sensitivity ranging from 1.4 to 13 mV/Pa and had a silicon di-

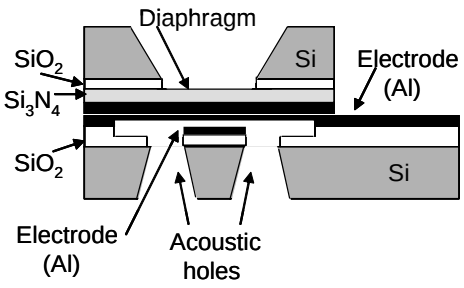

Figure 13: Cross-sectional View of Capacitive Microphone by Hohm and Hess

aphragm area of 2 mm^2 and thickness ranging from 5-8 μm. The lightly doped diaphragm was fabricated on one wafer by using a KOH anisotropic etch along with an electrochemical etch stop. The back wafer was made by the anodic bonding of glass and silicon wafers. The glass was thinned to 20 μm by mechanical polishing while the silicon had a thickness of 380 μm and was anisotropically etched in KOH. To create the holes in the glass layer, a silicon mask was used. The mask was then etched away afterwards. A thin film aluminum electrode was then formed on the glass wafer. Once all the fabrication steps were completed, the diaphragm wafer, the back wafer, and a bottom glass wafer were bonded together. The distance of the air gap was 4 μm. The combination of the four wafers created a condenser microphone as shown in Figure 14 [1].

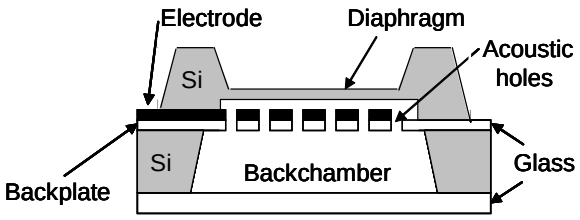

Figure 14: Cross-sectional View of Capacitive Microphone by Bergqvist and Rudolf

In 1992, Bourouina [3] presented a condenser microphone that did not require acoustic holes. In order to lower the air-streaming resistance, a thick air gap from 5 to 7.5 μm was used. The silicon wafer was double-side polished and square cavities were etched as the first step in the fabrication process. The etched depth was used to fix the air gap. The 1 μm thick diaphragm was made from heavily boron-doped (p^+) silicon. It was etched using the EDP boron etch-stop technique. The backplate was made of glass with an aluminum electrode layer. The diaphragm and the backplate were then bonded together using anodic bonding. The final device is shown in Figure 15 [3] below.

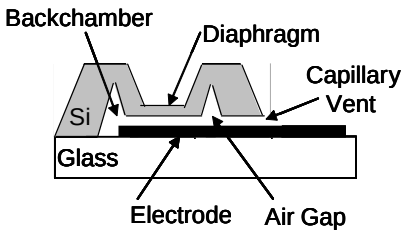

Figure 15: Cross-sectional View of Capacitive Microphone by Bourouina

A more recent example of a two-wafer designed microphone was presented by Scheeper et al. [23] in 2003. These microphones were fabricated using 350 micron thick double-sided polished p-type silicon wafers. The diaphragm wafer was thermally oxidized to have an oxide layer of 1.8 microns. After patterning the bottom side of the oxide, a 0.5 micron layer of LPCVD nitride was deposited to act as the diaphragm. The top side of the wafer was then patterned for etching. By using two different masks, chromium and gold layers were evaporated and patterned. The chromium layer was 100 Angstroms thick and the gold layer was 2000 Angstroms thick. The final step in the diaphragm wafer process was to etch the top side of the wafer in KOH. The backplate wafer started with the formation of a 1.2 micron thick oxide layer. The oxide was patterned and etched in KOH. After the removal of some of the remaining oxide layer, the wafer was etched again in KOH. This step was followed by an oxidization process to grow a 2000 Angstrom layer of oxide. Finally, the Cr/Au layers

were deposited and patterned. The wafers were bonded together by using gold-gold thermo-compression bonding. This type of bonding is done at low temperatures by making contact between the gold layers of the two wafers. By adding a slight pressure to the pair, the gold surfaces bond together in the heat. The final steps to this microphone include thinning the wafer by etching in TMAH and also releasing the nitride diaphragm, evaporating Cr/Au on the top side of the wafer, and the addition of an aluminum contact. The final device is shown in Figure 16 [23].

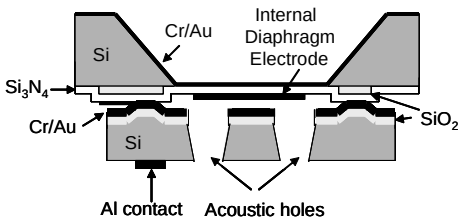

Figure 16: Cross-sectional View of Capacitive Microphone by Scheeper et al.

2.3.4 Single Wafer Microphones

While most capacitive microphones require separate wafer processing and then a bonding process, there are some microphones that are using a single wafer process. A single wafer microphone can be produced by using sacrificial layers. Some materials used as sacrificial layers are polysilicon, porous silicon, silicon dioxide, and aluminum. Single-chip capacitive microphones designs are rarer.

One of the earlier microphones was designed by Scheeper et al. [21] in 1991 and 1992. The design is based on using a single silicon wafer with a 1 μm-thick layer of LPCVD nitride grown on each side. The nitride was then patterned and etched in KOH. On the top side of the wafer, aluminum was evaporated as a sacrificial layer which was between 1 and 3 microns thick. Another micron-thick layer of nitride was grown on top of the aluminum layer using PECVD. Then an adhesion layer of 30 nm titanium was evaporated on the surface, followed

by the addition of the gold electrode. After patterning, the acoustic holes were etched in the Ti/Au layers and in the PECVD nitride. Using the acoustic holes, the aluminum sacrificial layer was etched. Finally, the last step of the fabrication was to evaporate 100 nm of aluminum on the bottom side of the wafer. Below, Figure 17 [21] shows the completed design.

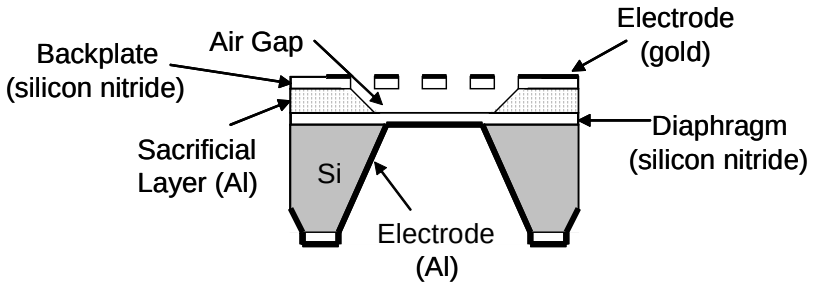

Figure 17: Cross-sectional View of Single Wafer Capacitive Microphone by Scheeper et al.

Another example of a single wafer capacitive microphone was presented in 1998 by Kronast et al [15]. This microphone was made from a double-sided polished p-doped silicon wafer. The first fabrication step was to p^+-dope both sides of the wafer. A thin nitride layer was deposited by LPCVD for use as a mask for the porous silicon formation. The porous silicon was created in a portion of the heavily p-doped silicon by etching in 25% HF and 50% ethanol in water. An electrical current was then sent through the porous silicon formation. The next step was to remove the masking layer and then sputter a 0.8 micron oxide layer onto the top side of the wafer. The oxide and the porous silicon would later be used as the sacrificial layer to create the air gap. Then a 300 nm layer of nitride was deposited with LPCVD on both sides. The nitride was used as a masking layer to create contact holes on the front side and windows on the back side of the wafer. After patterning the nitride by a mask, the holes and backside were etched in KOH. Aluminum was deposited on the front and back of the wafer to act as an RIE etch mask and a conductive layer. Acoustic holes were etched into the backplate to reach the porous silicon by RIE in SF_6 plasma. The porous

silicon was etched with KOH, and then the oxide layer was etched with HF. This last etching step releases the nitride diaphragm. Figure 18 [15] shows the final view of the single wafer microphone.

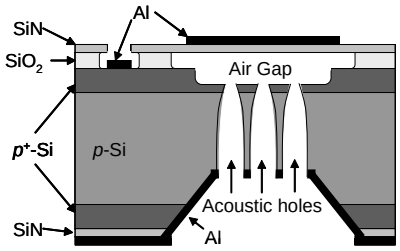

Figure 18: Cross-sectional View of Single Wafer Capacitive Microphone by Kronast et al.

2.4 DIRECT COMPARISON OF MICROPHONE TYPES

In order to better compare all of the microphones discussed in this chapter, the key features of each microphone design will be highlighted on the next page in Table 3.

Author, Year	Trans. Type	Diaphragm Material	Diaphragm (mm)	Gap Size (μm)	Sens. (mV/Pa)
Royer [22], 1983	Piezoelectric	30μm Si	diameter of 3	none	0.25
Hohm & Gerhard-Multhaupt [9], 1984	Electret	13μm Mylar	diameter of 8	30	3
Hohm & Hess [10], 1989	Capacitive	150nm Nitride	0.8 $\times$ 0.8	2	1
Bergqvist & Rudolf [1], 1990	Capacitive	5μm Si	2 $\times$ 2	4	10
Kühnel [27, 26], 1991	FET	150nm Nitride	1 $\times$ 1	2	0.1-1
Bourouina et al. [3], 1992	Capacitive	1μm doped Si	1 $\times$ 1	5	3.5
Schellin & Hess [24], 1992	Piezoresistive	1μm doped Si	1 $\times$ 1	none	0.025
Scheeper et al. [21], 1992	Capacitive	1μm Nitride	1.5 $\times$ 1.5	2.2	1
Bernstein et al. [26], 1997	Piezoelectric	doped Si & layers	0.8 $\times$ 0.8	none	NR†
Kronast et al. [15], 1998	Capacitive	300nm Nitride	2 $\times$ 2	1.3	3.2
Scheeper et al. [23], 2003	Capacitive	0.5μm Nitride	octagonal radius of 1.95	20	22

†not reported

Table 3: Silicon Microphone Designs

3.0 FABRICATION PROCESS

This chapter will detail how the microphone membranes were produced on the single-chip SOI wafer and cover some observations of the design. The three sections will explain the mask design, the process flow, and the testing procedure. The process flow section will be broken down into smaller sections to detail the different steps in the process. The testing procedures detailed here will only cover surface and cross-section observations.

3.1 MASK DESIGN

The fabrication process started with the design of the mask. The goal was to create a mask that allowed for different sizes of square microphones that included 1/2", 1/4", 1/8", 1/16", and 1/32". Acoustic holes of different diameters were also a requirement. The four diameters of acoustic holes were 5, 10, 15, and 20 microns. The acoustic holes also provided the means for etching the oxide layer of the SOI wafer.

The original mask design was divided into quarters to allow for dicing with a diamond scribe. Each quarter had a different acoustic hole size and its own etching time. To make the design easier, the microphones were placed in horizontal rows with a space of 100 microns between each membrane. A large gap through the center allowed for dicing the wafer without concerns of ruining a microphone. One quarter of the first mask is shown below in Figure 19.

However, while this design made the best use of the wafer area and allowed for the most microphones, it was not a practical design. A mask of this design could not be produced

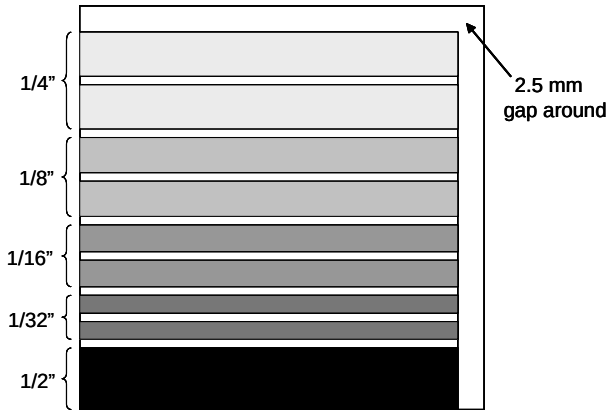

Figure 19: One Quarter of First Mask Layout

since there was no single die that was repeated. By using this first layout, the microphone shapes were easily changed into a repeated die structure allowing for mask production.

The new design resulted in one die that contained the following assortment of microphones: 1 1/2”, 4 1/4”, 4 1/8”, 8 1/16”, and 12 1/32”. The glass chrome mask was produced by JD Photo-Tools Ltd. in England. Since a 5 micron hole was a feature size beyond the capabilities of our mask maker, the intended 5 micron holes were changed to 10 microns to increase the chances of getting the 10 micron feature size to work. The holes were arranged so that the 1/2” microphone had 20 micron holes with 60 microns from hole center to center. The 1/4” and 1/8” microphones were arranged so that there were two microphones with 10 micron holes, one with 15 micron holes, and one with 20 micron holes. The hole centers were separated by a distance of 60 microns. Finally, the 1/16” and 1/32” microphones were arranged in rows containing four microphones with the acoustic hole diameters of 10, 10, 15, and 20 microns respectively. The first row of each type of microphone had a distance of 60 microns center to center and the second row had a distance of 80 microns center to center. For the last row of 1/32” microphones, there was a center to center distance of 100 microns. Due to the die layout, it was not possible to have more than one distance between the hole centers for the bigger microphones. If that was done, there would have been less

microphones overall. Therefore, only the smaller microphones have more options. In order to know where the microphones were located after etching, pits were formed along the outside of each microphone that had the same thickness as the acoustic hole diameter. These trenches could also be used to measure the depth of the silicon etching performed later in the fabrication process.

The final mask design called for the die to be repeated so there was a total of 20 dies on the mask arranged in 4 columns and 5 rows. The final design of a single die is shown below in Figure 20.

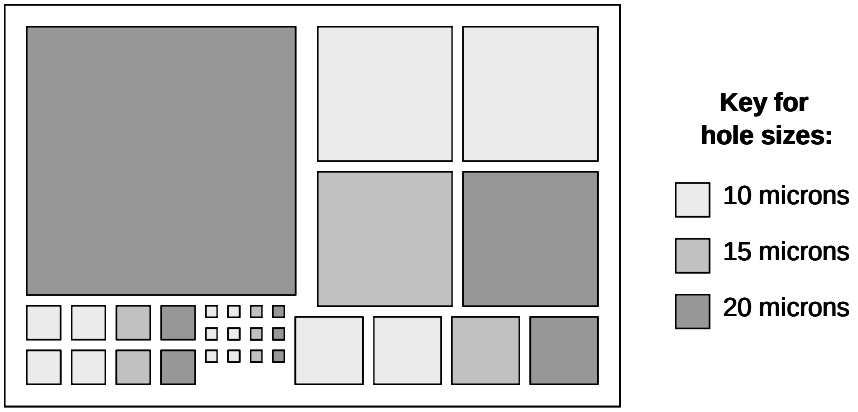

Figure 20: Final Design of Die for Mask Production

The dimensions for the hole locations were determined by designing for the minimal etch time in the BOE. The approximate etch rate for BOE in room temperature is 1200 Å/min. Due to the fact that silicon dioxide etches equally in all directions, to etch through the 2 micron thickness, the oxide will also be etched 2 microns to the left and to the right of the hole. The oxide etching time was determined by using Equation 3.1 below, where R is the etch rate, h is the material thickness, and t is the etching time. The equation yielded an etching time of 16.67 minutes to etch 2 microns of oxide.

$$t = \frac{h}{R}. \tag{3.1}$$

Once the oxide etching time was approximated, the number of holes per microphone had to be determined. This was done by converting the microphone size from inches to microns. Then a trial and error approach was taken to determine the optimal number of holes across the microphone. It was also important to leave room around the edge of the microphone to avoid collapsing the diaphragm during the sacrificial layer etching process. The equation uses two known values, the microphone size in microns (L) and the pre-determined hole distance from center to center (CC). The other value in the equation was the number of hole spacings (n), which was varied to change the output. The output of the equation was the distance (d) from the hole center to the edge of the microphone. The hole number was varied until this distance provided a safe value that would avoid over-etching and possibly releasing the entire membrane. The formula is shown below in Equation 3.2.

$$d = \frac{L - (n \times CC)}{2}. \tag{3.2}$$

The exact number of holes across the microphone was calculated by adding one to the number of hole spacings in the above equation. Once this number was obtained for each microphone size, the holes were added to the microphones in the mask design. Once the distances between the holes were determined, the total etching time for the microphones could be calculated using the distances between the holes and the etching values from Equation 3.1. Below, Table 4 shows the data calculated for the microphones. It includes the distance between hole centers, the microphone size, acoustic hole diameter, distance from the edge to the hole center, the number of holes across the membrane, and the approximate etching time.

Table 4: Complete Microphone Features

distance between hole centers CC, (μm)	mic size L, (in)	hole diameter (μm)	distance from edge to hole center d, (μm)	holes across	approx. etch time t, (min)
60	1/2”	20	50	211 × 211	250
	1/4”	10	55	105 × 105	250
		15	55	105 × 105	250
		20	55	105 × 105	250
	1/8”	10	57.5	52 × 52	250
		15	57.5	52 × 52	250
		20	57.5	52 × 52	250
	1/16”	10	43.75	26 × 26	250
		15	43.75	26 × 26	250
		20	43.75	26 × 26	250
	1/32”	10	36.875	13 × 13	250
		15	36.875	13 × 13	250
		20	36.875	13 × 13	250
80	1/16”	10	73.75	19 × 19	333
		15	73.75	19 × 19	333
		20	73.75	19 × 19	333
	1/32”	10	76.875	9 × 9	333
		15	76.875	9 × 9	333
		20	76.875	9 × 9	333
100	1/32”	10	96.75	7 × 7	417
		15	96.75	7 × 7	417
		20	96.75	7 × 7	417

3.2 PROCESS FLOW

The process flow for the fabrication is detailed in this section. The process was broken up into different phases since the work was done in different labs. The work completed in each lab had its own process flow, which is labelled here in phases. Phases 1 and 3 were completed at the University of Pittsburgh while Phase 2 was completed at Carnegie Mellon University. If necessary, the phase sections were broken down into smaller sections, called trials. These were used to highlight the differences in the fabrication process from the first time going through the process to the next. Each pair of SOI quarters went through all three phases before any etching processes were done on the next pair of SOI quarters. The first SOI wafer (used in the first and second trials) had a 20 micron-thick membrane and the second SOI wafer (used in the third trial) had a 4 micron-thick membrane. Both wafers had a 2 micron-thick oxide layer.

3.2.1 Phase 1

The first phase of the project was to perform the spinning functions, the photolithography process, dicing, and bonding. The process flow for the first phase of fabrication can be followed below in Figure 21.

This phase was started by pre-baking the wafer at 90°C for 10 minutes to remove any moisture in the wafer. This was followed by spinning on a layer of Hexamethyldisilazane (HMDS) to provide better adhesion between the silicon and photoresist. While the HMDS is used mostly to act as the adhesion layer between oxide layers and photoresist, it can be used between silicon and photoresist. After the HMDS was spun dry, the photoresist (AZ 4210) was spun on the wafer. The spinning recipe was the same for both layers. The starting cycle was set to 10 seconds, a speed of 500 rpm, and an acceleration of 200 rpm/sec. The middle cycle was set for 30 seconds, with speed and acceleration values of 3000 rpm and 500 rpm/sec respectively. The last cycle was 10 seconds at 1000 rpm and 500 rpm/sec. Once the spinning was completed, the wafer was baked in an oven for 30 minutes at 90°C.

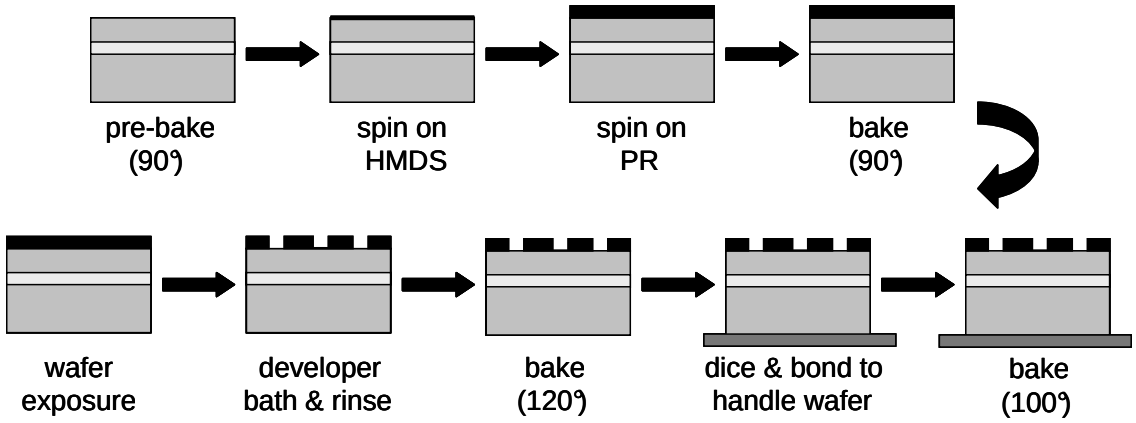

Figure 21: Process Flow for Phase 1

After the 30 minutes, the wafer was brought to the mask aligner for exposure. Since the exact exposure time was unknown, five test wafers were processed at different exposure times and different photoresists to determine the correct time before exposing the SOI wafer. The times used on the test wafers, in seconds, were 6, 10, 10, 7, and 13. The first two times were tested on AZ4110 photoresist while the remaining three were tested on AZ4210 photoresist. The best exposure time was determined to be 7 seconds. This step was then followed by the agitated immersion of the wafer in photoresist developer to show the image. The ratio of the developer to water was 1 AZ400k : 3 H_2O. After rinsing the wafer in DI water to stop the development process, the wafer was placed in the oven for 30 minutes at 120°C.

The final step for this part was to dice the wafer into quarters using a diamond scribe and then bond the sections onto handle wafers. The dicing was done easily by marking the edge with the diamond scribe, placing a needle under the mark, and then applying pressure on the sides of the wafer. This produced a clean-edged cut. Once the wafer was diced, each quarter was then bonded to a silicon wafer, which was used as the handle wafer.

The bonding was done by two different methods. The first two SOI quarters were bonded by using a thick layer of photoresist on the handle wafer as the bonding agent. In order to achieve a thicker layer of photoresist, the layer was spun on using a uniform speed of 800

rpm for 45 seconds, an acceleration rate of 1000 rpm/s, and a deceleration rate of 500 rpm/s. After the spinning recipe was completed, the SOI wafer section was placed on top of the handle wafer with some applied pressure. The two wafers were then heated in an oven for 20 minutes at 100°C.

The other two SOI quarters were bonded to the handle wafer by using double-coated thermal release tape, REVALPHA, from Nitto Denko. One side of the tape is easily removed by heating while the other side can be removed but is more permanent. The side that can be removed through heating was attached to the SOI quarter. The other side of the tape was attached to the handle wafer.

The bonding process is done because the etching time is different for the various acoustic holes and the RIE machine cannot etch just a portion of a wafer. Therefore, each quarter was etched according to the etching time needed for a particular group of acoustic holes. Also, due to the design, bonding the SOI quarter onto a whole silicon wafer makes the etching process safer because the wafer is held in place by clamping the handle wafer instead of the SOI wafer. Since the clamp never touched the SOI wafer, no microphone parts were damaged during the etching process.

3.2.2 Phase 2

The second phase of the fabrication process consisted of removing any native oxide on the wafer, silicon etching, removal of the handle wafer, and sacrificial oxide etching. The second phases's process flow can be followed below in Figure 22.

Due to heating the wafer, native oxide could have formed on the wafer's surface. Before etching with RIE, it is important to remove this layer. Since the native oxide growth is thin, approximately 80 to 100 Angstroms, the wafer can be dipped in BOE for about 5 seconds and then rinsed in water. BOE is used for this step because it will not attack the photoresist that is being used as a mask layer.

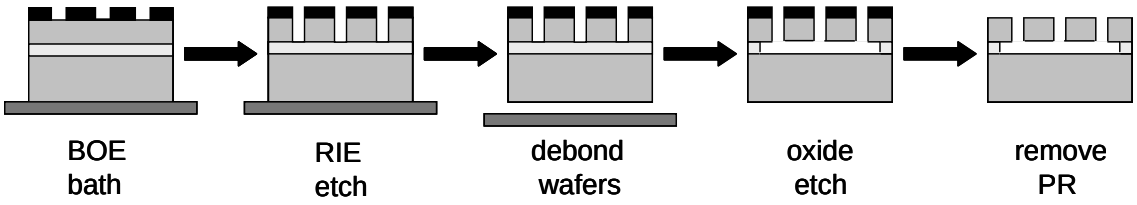

Figure 22: Process Flow for Phase 2

3.2.2.1 Trial 1 The wafer combination, bonded by photoresist, was then loaded into the RIE chamber. The wafers were etched for 60 cycles. Each cycle was etched for 20 seconds total, which included an 8 second passivation time followed by a 12 second etching time. The total time used for etching one wafer through 20 microns of silicon was 20 minutes. The SOI wafers were lifted from the handle wafer after the RIE process. The photoresist did not prove to be a good bonding agent because the wafers were no longer bonded after etching. The wafers were observed through a microscope to determine if the silicon had been completely removed by measuring the depth of the pits. One major problem was that one of the wafers got caught in the RIE chamber, which caused the photoresist layer to burn. The other quarter did not have this problem.

Next, the wafers were immersed in a BOE bath to remove the sacrificial layer of oxide. The wafers were placed directly onto the bottom of the bath's container and there was some agitation throughout the etching process. The wafers were taken out after 4 hours, and rinsed to remove the BOE. The final step was to remove the photoresist by immersing the wafers into a hot solvent alkaline bath.

3.2.2.2 Trial 2 Using the remaining two quarters of the SOI wafer that were bonded by tape, the etching process was done again. This trial used different times to provide better sidewalls during the silicon etching. After etching each of the quarters for 10 minutes, they were examined under a microscope. By examining the depth of the etch, it was determined

that the wafers would need more time in the chamber. The quarter for the 15 micron holes was etched for another minute while the quarter for the 20 micron holes was etched for another 2 minutes.

After the silicon etching was complete, the SOI wafers had to be removed from the handle wafer. This was done easily by heating the combined wafers on a hot plate at 150°C for approximately 5 minutes. The SOI wafer could then be lifted off of the tape's surface.

The SOI wafers were then immersed into a 49% HF bath to remove the sacrificial oxide layer. Since HF etches between 5 and 10 times faster than BOE, the times that had been calculated in Table 4 were divided by 10 to compensate for the fastest etching time in HF. The wafers were placed vertically into an agitated bath. The wafers were removed from the bath after 20 minutes when some of the membranes had been completely released. The wafers were rinsed in DI water and dried with the nitrogen gun.

3.2.2.3 Trial 3 For the third trial, the entire wafer was etched in the RIE chamber for 2 minutes and 20 seconds. Once the RIE etching was completed, the wafer was then diced into quarters to be etched in HF. Only two quarters were etched in 49% HF, and they were placed vertically into the acid with a slight agitation. The quarters were removed after 15 minutes. There were four membranes that had been completely released due to over-etching. The quarters were then placed directly into an agitated water bath to stop the etching.

The previous set of microphones did not have a clean surface after removing the photoresist, so the method of removing the photoresist was altered. For this trial, the wafers were placed into a bath of AZ KWIK Strip Remover. This container was then put onto a hot plate set to low. Once the photoresist was removed, the wafers were placed into an agitated water bath to rinse off any remaining remover. In order to dry the wafers, they were placed into an alcohol (2-propanol) bath for several minutes and then taken out and left to dry. Water guns and nitrogen guns were not used at all in order to keep the thin membrane from cracking.

3.2.3 Phase 3

After all of the processing on the wafers was completed, the last step was to determine if the fabrication process had been successful. It was important to observe the silicon membrane and check to ensure that the oxide layer was uniformly removed. All testing was performed by using a Philips XL-30 Scanning Electron Microscope (SEM) to capture images of the membrane surface and images of the cross-section. General observations of the silicon surface were also recorded.

3.2.3.1 Trial 1 The first test performed on the wafers was to observe the cross-section of some of the microphones. This was done to determine if the etching times were appropriate and if the structures had been released. Since it was a destructive test, it was only performed on one die per quarter SOI wafer. The SOI microphones were diced with a diamond scribe through the middle and each cross-section was examined through the microscope.

3.2.3.2 Trial 2 and Trial 3 For the second and third trials, only the membrane surfaces were examined using the SEM machine. For these cases, the membrane surfaces were examined to ensure that there were membranes left after etching in HF. After looking at the surfaces, it was determined that there were several membranes that could be used for further testing. The cross-sections were not examined since it would require the microphone areas to be diced and ruined for further testing.

3.3 CHAPTER SUMMARY

This chapter addressed the process steps performed on the SOI wafer. All of the results taken from these processes will be discussed in the following chapter. Chapter 4 will further explain the change in some of the process steps and also include any tables and figures needed to provide a more detailed explanation. The SEM images captured during the fabrication process will also be included.

4.0 FABRICATION RESULTS

The purpose of this chapter is to examine the results from the previous chapter in detail. The chapter will be broken into sections that address each result and its meaning to the project. The first section will explain any issues resulting from the mask design. The second and third sections will discuss the results from the three phases of fabrication. Since the SEM images captured in the third phase support the work done in the second phase of fabrication, these two parts will be condensed into one section.

4.1 MASK CONCERNS

Overall, the mask produced the holes and pits needed for the photolithography process. However, the mask had some complications. The main problem was that many of the 10 micron holes were not formed correctly. This resulted in the microphones for this hole size to not be available for use since the holes were not produced uniformly on the mask. This problem was expressed by the mask manufacturer, so it was not completely unexpected, but it did cause a loss of many microphones.

Another issue with the mask was with the resolution of the mask features. When observing the mask under a microscope, the curved and straight features did not have a smooth line. The lines were jagged, which produced images onto the wafer that were less then what was desired in terms of resolution. However, since this project was mainly focused on being a feasibility study, the mask was used for the fabrication anyway. In order to produce the microphones with a much clearer result, a better mask would be required. If the mask could

be made with better resolution, the 10 micron holes would also have a better chance of being produced.

4.2 PHASE 1

The two main parts of the first phase of fabrication consisted of finding the correct exposure time and in finding what type of bonding method works the best for this project.

4.2.1 Exposure Results

The first test that needed to be run was to determine the exposure time during the photolithography process. This was done by taking five single silicon wafers and subjecting them to varying exposure times and preparatory measures as shown below in Table 5. All of the wafers used the same HMDS and PR spinning recipes.

Table 5: Exposure Testing

Wafer No.	Pre-bake	HMDS Bake	PR	PR Bake	Exposure	Post-bake
1	10 min @ 90	None	AZ 4110	30 min @ 90	6 sec	30 min @ 120
2	10 min @ 90	None	AZ 4110	30 min @ 90	10 sec	30 min @ 120
3	10 min @ 90	None	AZ 4210	30 min @ 90	10 sec	30 min @ 120
4	10 min @ 90	10 min @ 90	AZ 4210	30 min @ 90	7 sec	30 min @ 120
5	10 min @ 90	10 min @ 90	AZ 4210	30 min @ 90	13 sec	30 min @ 120

After using the developer on the five test wafers, they were examined in a microscope. Some of the things that were specifically looked for were the smoothness of the lines, sharp corners, straight walls, and no silicon material at the bottom of the opening.

Upon examination, all the features that were exposed removed the photoresist. Due to the mask condition, the features did not have smooth edges. The wafer that was exposed for 10 seconds had fairly straight sidewalls, but the 7 second exposure had straighter sidewalls. The 7 second exposure also had smoother lines than the other wafers. Due to this, an exposure time of 7 seconds (Test Wafer #4 in Table 5) was chosen along with baking the wafer after spinning on the HMDS layer.

4.2.2 Bonding Results

In the first trial, the SOI wafer was attached to the handle wafer by using photoresist as the bonding agent. While it was an easy method to use, it created some problems after etching in the RIE chamber. The photoresist did not provide for good thermal properties, causing the handle wafer and the SOI wafer to be at two different temperatures. The photoresist was burned on one of the wafers. This could be due to the problem with the thermal properties or a problem with the machine. Also after etching for 20 minutes, the photoresist did not hold up as a bonding agent, causing the SOI wafer to come free from the handle wafer on its own.

The SOI wafer that was bonded to the handle wafer by thermal release tape for the second trial. There were no problems with the tape as a bonding agent. However, if not watched carefully, the photoresist could start to burn while heating the combined wafers to un-bond the SOI and handle wafers. Overall, the tape was easier to use and created fewer problems.

4.3 PHASES 2 AND 3

For the second phase, the etching methods for both the silicon and the oxide were examined. These results were used to make changes in the fabrication process to produce better microphones for each new trial. In order to visually see these results, the images captured

from the SEM machine in the third phase of fabrication were used. The general observations of the surface conditions are also noted here.

This section is divided into the three trials as in the previous chapter. Each trial will then discuss the general observations and etching processes along with SEM images to support the analysis.

4.3.1 Trial 1

As a reminder, the first trial was completed on the thicker SOI wafer (20 micron-thick membrane). The quarter wafers in this trial were bonded with photoresist, etched in the RIE chamber for 20 minutes, etched in BOE for 4 hours, and the photoresist was removed by a heated alkaline solvent bath.

4.3.1.1 General Observations By observation, the two quarters looked different since each quarter was processed separately in the RIE chamber. One quarter had been caught in the RIE chamber, causing the surface to have a hazy dark silver coloring to it. There were also sections of photoresist burnt onto the surface that could not be removed. The other quarter, not caught in the chamber, had a shiny bright silver surface and no markings as was expected.

4.3.1.2 Etching A microscope and the SEM machine were used to determine whether the silicon had been removed and how successfully the silicon was etched. The surface and cross-sections of the microphones were observed. Below, Figure 23 shows the surface of two 1/4" microphones with 15 and 20 micron holes.

After examining the cross-section, it was obvious that the silicon sidewalls were not smooth. The following picture, Figure 24, shows an example of the rough sidewalls from a 1/2" microphone. This is primarily due to the condition of the mask. While the rough surface can be tolerated for the beginning stages of testing, it would not be acceptable for the final design.

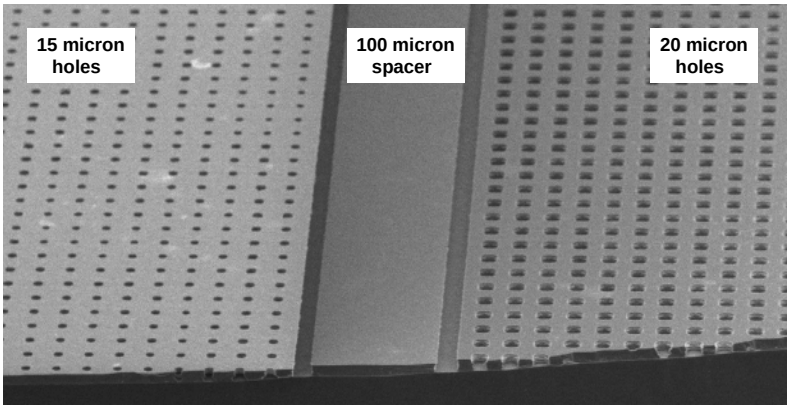

Figure 23: Surface of 1/4" microphones

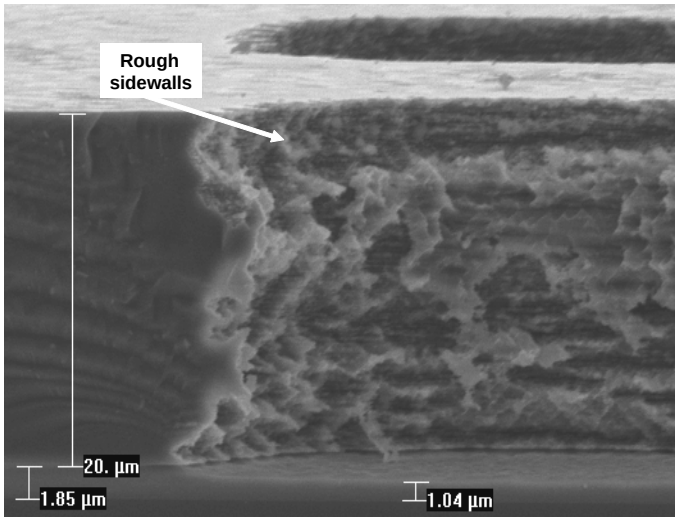

Figure 24: Silicon Sidewalls after RIE

The main problem that was observed in the first trial of RIE etching was that the wafers were over-etched. This can be seen from the "footing effect", shown in Figure 25, that was clearly visible when examining the 15 micron holes. When the etching process is continued after the silicon has been removed, the ions from the etching start attacking the bottom portion of silicon closest to the oxide. This creates a larger hole than intended at the bottom.

Another issue that arose was when the photoresist was burned during the silicon etching. This caused the surface of the wafer to have a different appearance and created several pockmarks throughout the surface. Below, Figure 25 shows an example of a 1/4" 15 micron-holed microphone with a burned photoresist layer on the surface along with the footing effect.

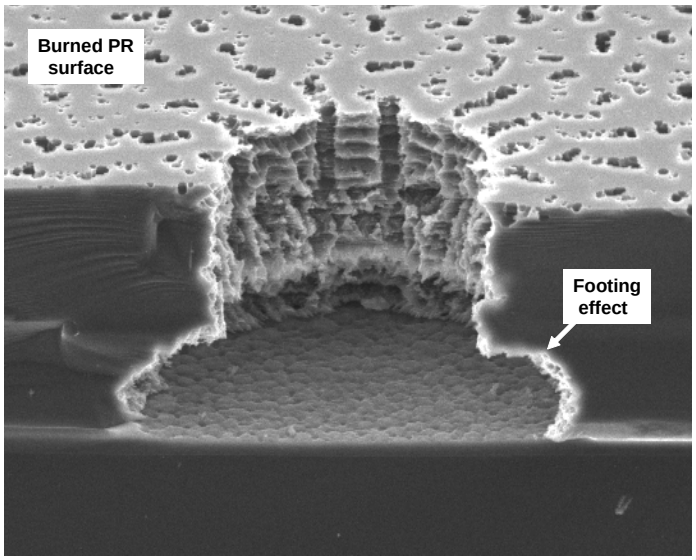

Figure 25: Burned PR surface and Footing Effect

When the wafers from the first trial were etched to remove the sacrificial oxide layer, they were placed into a bath containing BOE for 4 hours. By using BOE, which has a slow etching rate, there was a possibility of the oxide not etching in a uniform manner. Many

microphones were examined with the SEM machine as a check to determine if the oxide layer was uniformly removed from underneath the microphone membrane.

The first problem that was observed was that the oxide was not etched all the way through under a large majority of the silicon holes. There was a possibility that some of the passivation layer was left on the oxide surface, preventing it from etching at its typical rate. This is shown from the uneven oxide surface from a 1/2" microphone in Figure 26.

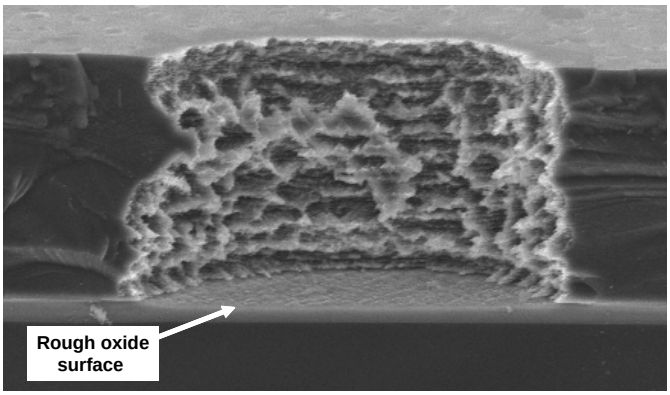

Figure 26: Rough Oxide Surface after Etching

There were many spots where the oxide layer did not etch. Since the wafer had to be diced in order to place it in the SEM machine, sections with remaining oxide were located. In a few instances, the membranes snapped off during dicing, leaving only the portion still connected to the oxide behind. One example of this is seen in Figure 27 from a 1/2" microphone.

An example of an unreleased and a released portion staying connected is seen in Figure 28. The 1/2" microphone was released on the right side, but not on the left. While it was expected that the 1/2" microphones might be a problem to get fully released structures, other microphone types had the same problem. This could be a result of placing the wafers into the BOE bath and letting them sit at the bottom of the bath with only a slight agitation. The BOE might not have been able to work its way into all of the holes.

The final product should look similar to Figure 29, where the oxide layer has been completely removed. This was taken from a portion of a different 1/2" microphone.

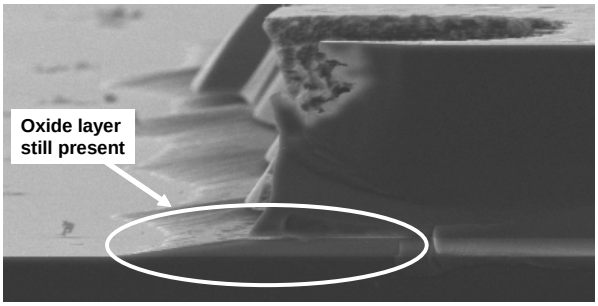

Figure 27: Remaining Oxide Layer with a Missing Membrane Section

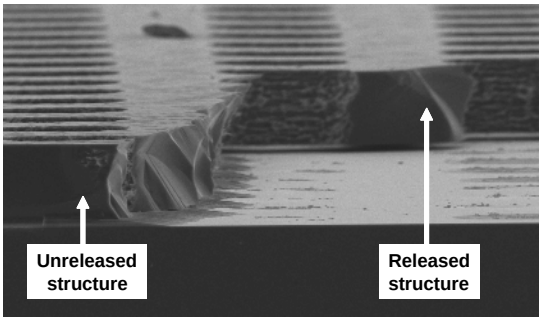

Figure 28: Membrane with Both Unreleased and Released Portions

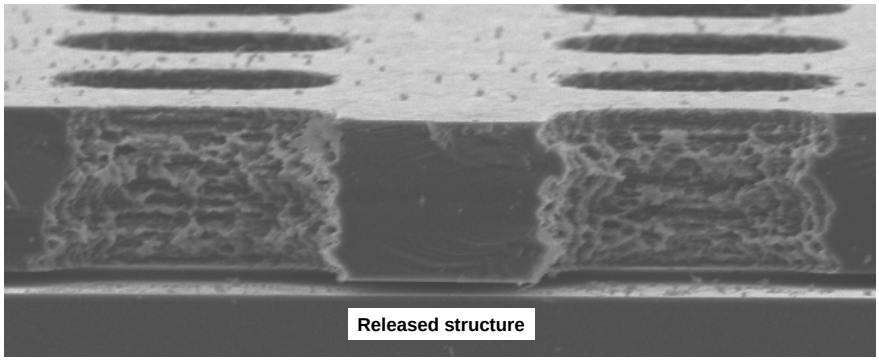

Figure 29: Released Membrane Structure

4.3.2 Trial 2

The second trial was also completed on the thicker SOI wafer. The two quarter wafers in this trial were bonded with tape, etched in the RIE chamber for 11 and 12 minutes, etched in HF for 20 minutes, and the photoresist was removed by a heated alkaline solvent bath.

4.3.2.1 General Observations In this trial, both quarters had the same surface conditions. They had a shiny silver coloring, but there were portions of the wafers that had a yellow or pink coating on them. Some parts also had what looked to be a sticky coating on them. While making observations using the SEM, these sections were looked at closely to determine what the surface problems were.

4.3.2.2 Etching The RIE etching time was changed in the second trial to reduce the footing effect seen in the previous trial. The SEM was again used to determine if the silicon etching was successful. Since there was a better success rate, the microphone cross-sections were not examined for the second trial. Only the surface conditions were observed.

For the second trial, the majority of the results were good. The microphones were checked to ensure that all of the holes had been etched and that the corners of the microphones were free from the trenches. Even though the corners need to be released from the trenches, the membranes are still attached to the rest of the wafer through the remaining oxide layer. Figure 30 shows a 1/16" microphone (20 micron holes, 80 CC) that was not fully released at its corner and a 1/32" microphone (15 micron holes, 60 CC) with fully released corners.

While the microphones that had the 10 micron holes could not be used, they were observed in this trial. In these types of microphones, a scaling effect can be observed in the trenches. The scaling effect happens when the RIE etching is not uniform and gets narrower at the top and bottom of the feature. This occurs since the smaller features have a lower etching rate. This is shown directly in Figure 31 below.

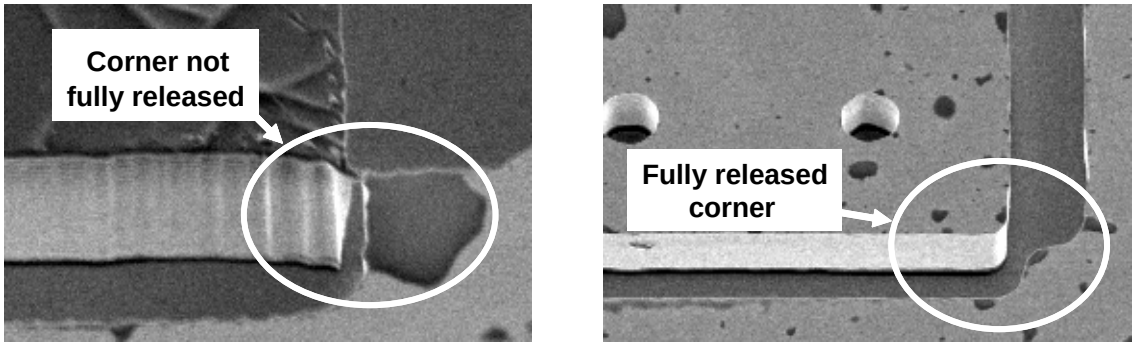

Figure 30: Unreleased (left) and Released (Right) Corners

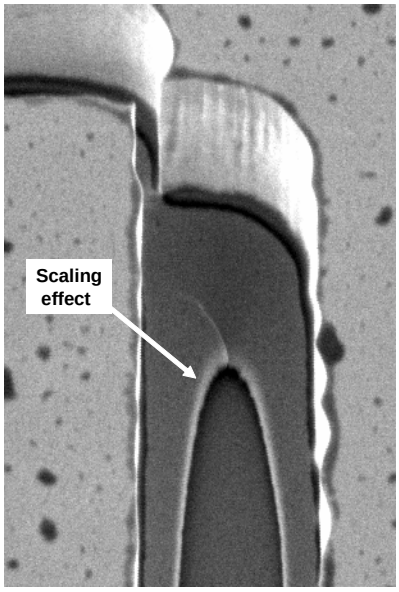

Figure 31: Scaling Effect in 10 micron Trench

The oxide etching in the second trial changed drastically. Instead of using BOE, HF was used in order to speed up the etching rate. The total process time was reduced to 20 minutes instead of over 4 hours. However, since the cross-sections were not able to be studied, it could not be observed if the oxide layer had been completely etched. The microphones were not diced to check the cross-sections since it is a destructive test. Therefore, a general study of the microphones was done from the surface.

This study supported the evidence that there was a coating on the surface of the wafer. Any film layer that stayed on top of the microphone surface caused the surface to look dark in the SEM machine images. The surface also looks as though there are cracks in the surface, but it is the thin film layer shifting. Upon closer inspection of the holes (magnifying the images to around 300%), the difference of the thin film holes and silicon holes can be seen due to the coloring change from film to silicon. The surface condition with a thin film layer can be seen in Figure 32.

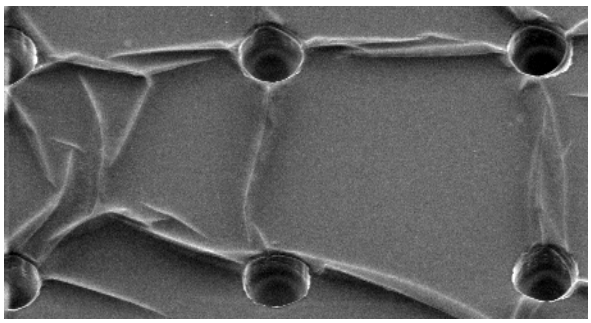

Figure 32: Thin Film Layer on Microphone Surface

The thin film layer can be seen more clearly when it is not directly on top of a microphone. The layer still appears as a darker layer on the silicon surface. Figure 33 shows a thin film that shifted across two microphones.

The thin film layer was determined to be a combination of HMDS and photoresist that was not removed with the stripper. In order to remove this layer, the wafers were placed into a hot sulfuric acid bath (3:1 H_2SO_4:H_2O_2). The combination of the two chemicals causes

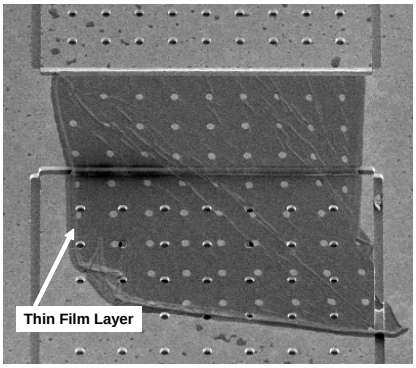

Figure 33: Thin Film Layer Between Two Microphones

the mixture to become heated. After keeping the wafers in the mixture for a few minutes, they were rinsed in water and dried in the oven at 90°C for 20 minutes.

A possible problem detected in this study was the poor adhesion between the three layers of the SOI wafer. One of the microphones broken during the fabrication process was examined. It was observed that the three layers had not broken together, but all three had broken separately. If there was a better bond, the three layers should have broken more uniformly across the combined wafer. These three distinct layers can be observed in Figure 34.

Finally, Figure 35 is an example of a properly released structure. The membrane has been released from the trenches and all of the holes have been etched. The spots on the surface are sections of photoresist that could not be removed. The following shows a 1/32" microphone with 15 micron holes and a 60 micron spacing between hole centers.

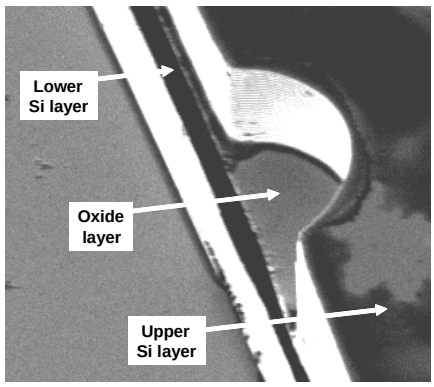

Figure 34: Three Layers of SOI Wafer

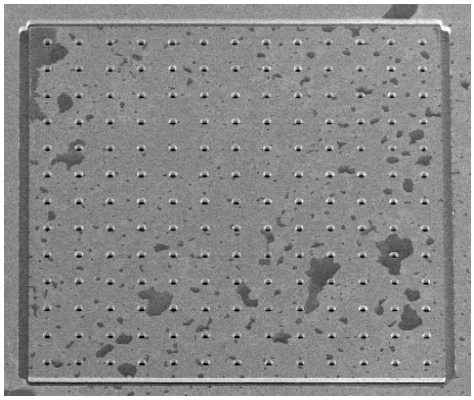

Figure 35: Possible Working Structure

4.3.3 Trial 3

The third trial was the first one to use the thinner SOI wafer. This wafer had a 4 micron-thick membrane. The two quarter wafers in this trial were etched in the RIE chamber for 2 minutes and 20 seconds, etched in HF for 15 minutes, and the photoresist was removed by a heated bath of AZ KWIK Strip Remover™.

4.3.3.1 General Observations The microphones for the third trial had better surface conditions than the ones for the second trial. The majority of the surface had a shiny silver coloring. There were only a few microphones that had a film covering. However, some of the membranes appeared to not have any tension and looked as though they were loose in some parts.

4.3.3.2 Etching Again, the SEM machine was used to capture images of the microphone surface. The surface images showed that there was a problem with the silicon etching. Some holes were not completely etched through, while others were. This can be better seen in Figure 36, where a 1/32" microphone is above the 1/2" microphone. The smaller microphone is etched completely, shown by the darker holes. The larger microphone's holes are still grey in color, and are no different than the surface coloring. The silicon etching problems could be due to non-uniform etching in the RIE chamber or if the photoresist was not fully developed and rinsed away.

Another problem with the silicon etching was that the etch did not produce clear holes, as shown in Figure 37. In many instances there were pieces of silicon still attached to the surface or the sidewalls of the holes. This was the case for the surfaces that were and were not completely etched. The following image shows an example of the etched (left) and not fully etched (right) 1/2" microphones.

The main concern of the third trial was that some of the membranes appeared to be loose, or not in tension. Several of the membranes were examined with the SEM. The surface conditions of these microphones were good. However, the holes along the edges did

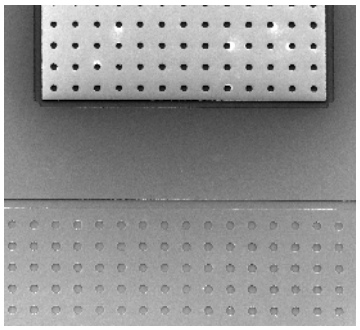

Figure 36: Etched (Above) and Not Etched (Below) Microphones

not fully etch while the middle part of the microphones did etch completely. This can be seen by observing in Figure 38 how the hole coloring goes from light at the edge to dark towards the center. The microphone shown below is 1/8" with 15 micron holes.

With the oxide etching, the only problem was that the HF etched too quickly to be controlled, similar to Trial 2. The fast etch rate caused at least one of the smallest microphones in each die to be over-etched, completely releasing the membrane from the rest of the wafer. Figure 39 shows a combination of 1/32" microphones. Two 60CC microphones are above two 80CC microphones. The 1/32" with 20 micron holes and 60CC (the upper right microphone) has been completely removed.

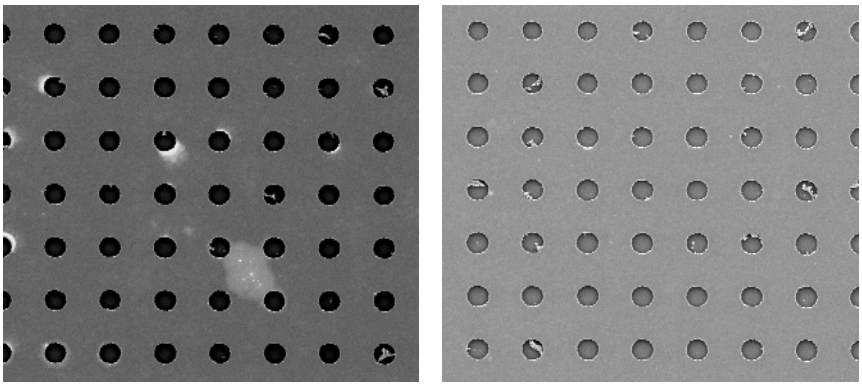

Figure 37: Remaining Silicon on Surface and Sidewalls after Etching

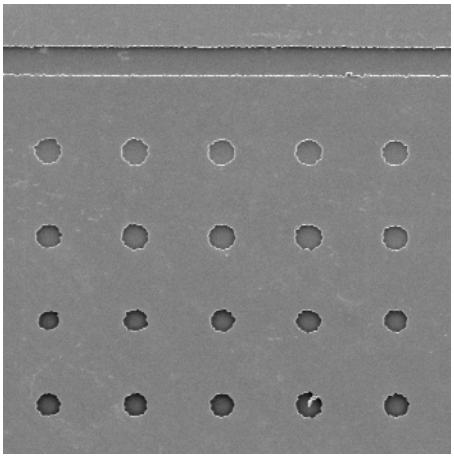

Figure 38: Membrane Without Tension

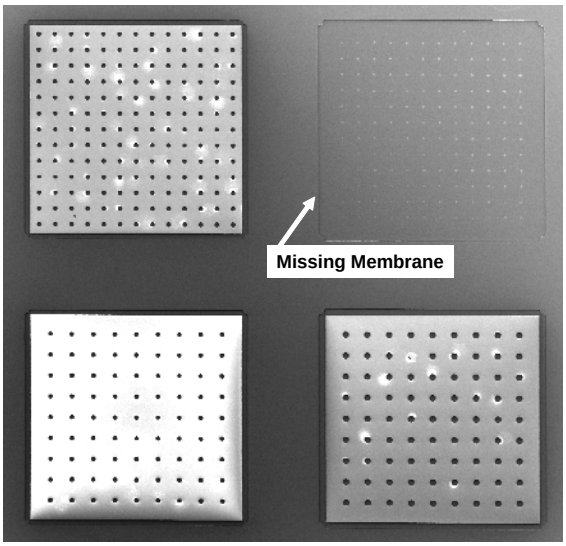

Figure 39: Group of 1/32" Microphones

4.4 CHAPTER SUMMARY

This chapter discussed the main microphone results from the fabrication process. Through the testing, several changes to the process were made to enhance the success of the microphones. A total of three trials were completed. After producing microphones that have a strong possibility of functioning, they were dynamically tested by exciting the membrane with acoustic noise. A static analysis was also done using ANSYS. These tests are discussed in the following chapter.

5.0 MODELING AND EXPERIMENTAL DYNAMIC CHARACTERIZATION

In this chapter, the dynamic testing results of the microphone membranes are discussed. The testing was done using the Microvision system (at Carnegie Mellon University) and a fotonic sensor (at University of Pittsburgh). Further testing was done through the use of a profilometer. The main sections of this chapter consist of background calculations, testing procedure, and testing results.

5.1 BACKGROUND CALCULATIONS

Before testing the membranes, it was important to have a better idea of what frequencies to test on the membrane and how the membrane was going to deflect. This section will contain the results for the natural frequency calculations and a static analysis in ANSYS. By using the data from ANSYS, the family of curves could also be plotted for better comparison between both the microphone sizes and the membrane thicknesses.

5.1.1 Natural Frequencies

The first calculations done were to determine the fundamental natural frequency of the microphone membranes. Natural frequencies are the frequencies at which a structure will tend to vibrate once it is in motion. By calculating the fundamental, or lowest, natural frequency of the microphones, the testing procedure could be done faster by concentrating on a range

of frequencies lower than the microphone's natural frequency. As with accelerometers, the transducer will be used well below the first natural frequency.

Since the microphone membranes were fixed along the sides, the membranes were modelled as clamped-clamped-clamped-clamped plates [2] with a length to width ratio of 1 for a square plate. The required values for this calculation included the following silicon material properties: width of plate (a), modulus of elasticity (E), Poisson's ratio (ν), thickness of plate (h), and mass per unit area (γ). The material constants for silicon as used in the equation are listed as follows:

- $E = 150$ GPa
- $\nu = 0.17$
- $\mu = 2{,}330$ kg/m^3
- $h = 20$ μm, 4 μm
- $\gamma = \mu \times h = 0.0466$ kg/m^2, 0.00932 kg/m^2

For this particular equation, λ is independent of ν. The natural frequency for this type of structure can be calculated as shown below in Equation 5.1 [2].

$$f_{ij} = \frac{\lambda_{ij}^2}{2\pi a^2}\left[\frac{Eh^3}{12\gamma(1-\nu^2)}\right]^{1/2}. \tag{5.1}$$

There were six given frequency parameters in the reference material for λ_{ij}^2, but only the first parameter (λ_{11}^2) was used for this calculation. The holes in the plate were not taken into account for the natural frequency calculations. They could be accounted for by changing the mass per unit area (γ) value to compensate for the loss in area. However, since the plate is only held fixed by a thin section of oxide, it is possible that the plate could act closer to a simply supported structure than a clamped structure. It is believed that these two changes would cancel each other out, leading to the decision to model the membranes as plates without holes that have clamped edges.

The fundamental natural frequency was calculated for the five different microphone sizes (1/2", 1/4", 1/8", 1/16", and 1/32") and four different membrane thicknesses (4 micron, 10 micron, 20 micron, and 30 micron). As a note, the 4 micron and 20 micron membrane

thicknesses correspond to the fabricated microphones. The results of this calculation are shown in Table 6.

Table 6: Fundamental Natural Frequency of Microphones

Membrane Size	1/2"	1/4"	1/8"	1/16"	1/32"
4 μm‡	12.02 kHz	48.07 kHz	192.27 kHz	769.55 kHz	3076.25 kHz
10 μm	30.04 kHz	120.17 kHz	480.66 kHz	1923.87 kHz	1690.62 kHz
20 μm‡	60.08 kHz	240.33 kHz	961.33 kHz	3847.73 kHz	15381.24 kHz
30 μm	90.12 kHz	360.50 kHz	1441.99 kHz	5771.60 kHz	23071.86 kHz

‡Fabricated Membrane Thicknesses

As seen from the results in Table 6, the majority of the fundamental natural frequencies are well above the audio range of 20 kHz. The exception is the 1/2" microphone with a 4 micron membrane. With the high natural frequencies, the microphone membranes are good candidates for further acoustic measurements. However, since some of the natural frequencies are extremely high and are in the MHz range, the stiffness in those membranes is too high to be actuated acoustically.

5.1.2 ANSYS Analysis

The other analysis performed before testing was to determine the deflection of the clamped plate through ANSYS. The plate was modelled as an 8-node elastic shell (SHELL93) with no holes. The material properties used for the analysis are the same as listed above for the fundamental natural frequencies calculation. All of the edges were held fixed in the z-direction, while the horizontal and vertical edges were held constrained in the x and y-directions respectively. After adding the displacement constraints, each membrane had a constant pressure applied to the square area. The pressures applied ranged from 20e-6 Pa to 20 kPa (0-180 dB Sound Pressure Level (SPL)) and they were increased by an order

of magnitude. The standard operating microphone pressures would be 20e-5 Pa to 20 Pa (20-120 dB). A total of 10 ANSYS results were collected for each microphone. To ensure that accurate solutions were provided, a nonlinear analysis was performed in ANSYS.

After plotting all of the results, the general nodal solution was similar between the microphones for the smaller pressures. The nodal solution for the 1/2" microphone with a 20 micron-thick membrane is shown below in Figure 40. For comparison, Figure 41 shows the same microphone membrane at a higher applied pressure of 200 Pa.

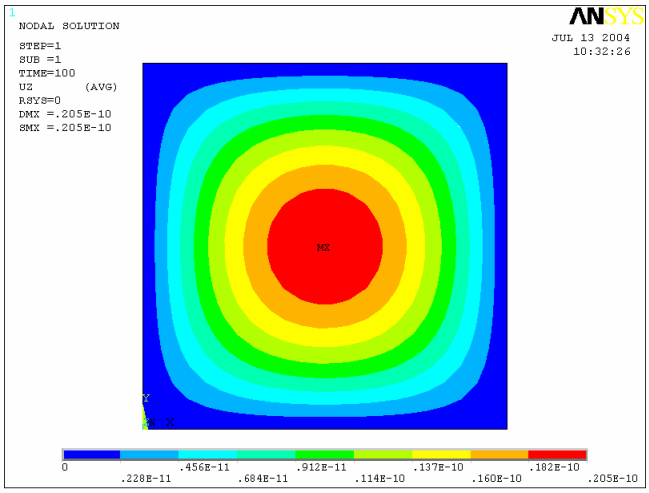

Figure 40: ANSYS Membrane Deflection for 1/2" 20μm-thick Membrane at 20e-6 Pa Applied Static Pressure

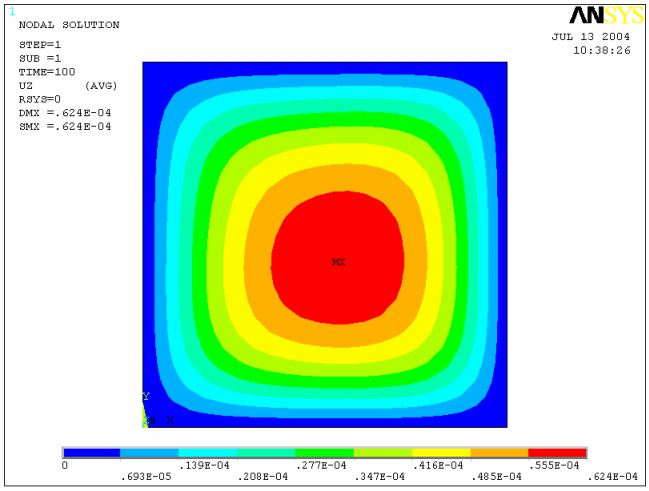

Figure 41: ANSYS Membrane Deflection for 1/2" 20μm-thick Membrane at 200 Pa Applied Static Pressure

Table 7 lists the maximum possible deflections that correspond to the fabricated microphones with 4 micron and 20 micron membrane thicknesses. Immediately following, Table 8 gives the maximum deflection for the membrane thicknesses that were not fabricated (10 micron and 30 micron). For some of the larger pressures, the solution did not converge in ANSYS and those results were not listed, as indicated by 'NL' in the Tables.

Also, since there is a 2 micron gap for this microphone study, the maximum deflection cannot be any larger than that. At the higher pressures, a much larger deflection is predicted through ANSYS. If the higher pressures are required, either the thickness of the membrane must be increased or the area of the microphone must be reduced in order to have a deflection less than the 2 micron gap. For the fabricated wafers, the predicted deflections less than 2 microns are highlighted in blue font in Table 7.

Table 7: Predicted Maximum Deflection Results Corresponding to Fabricated Wafers

	Pressure	1/2”	1/4”	1/8”	1/16”	1/32”
4 μm membrane	20e-6 Pa	2.56 nm	0.16 nm	0.01 nm	0.000627 nm	0.0000392 nm
	20e-5 Pa	25.6 nm	1.6 nm	0.1 nm	0.00627 nm	0.000392 nm
	20e-4 Pa	0.256 μm	0.016 μm	0.001 μm	0.0627 nm	0.00392 nm
	20e-3 Pa	2.34 μm	0.16 μm	0.01 μm	0.627 nm	0.0392 nm
	20e-2 Pa	10.1 μm	1.54 μm	0.1 μm	0.00627 μm	0.392 nm
	20e-1 Pa	27.6 μm	7.98 μm	0.985 μm	0.0627 μm	0.00392 μm
	20e 0 Pa	70.1 μm	22.7 μm	6.28 μm	0.623 μm	0.0392 μm
	20e 1 Pa	NL[†]	58.4 μm	18.5 μm	4.63 μm	0.391 μm
	20e 2 Pa	NL	146.0 μm	48.3 μm	15.1 μm	3.31 μm
	20e 3 Pa	NL	NL	121.0 μm	39.9 μm	12.2 μm
20 μm membrane	20e-6 Pa	0.0205 nm	0.00128 nm	0.0804 pm	0.00506 pm	0.00321 pm
	20e-5 Pa	0.205 nm	0.0128 nm	0.000804 nm	0.0506 pm	0.0321 pm
	20e-4 Pa	0.00205 μm	0.128 nm	0.00804 nm	0.506 pm	0.0321 pm
	20e-3 Pa	0.0205 μm	0.00128 μm	0.0804 nm	0.00506 nm	0.000321 nm
	20e-2 Pa	0.205 μm	0.0128 μm	0.804 nm	0.0506 nm	0.00321 nm
	20e-1 Pa	2.05 μm	0.128 μm	0.00804 μm	0.506 nm	0.0321 nm
	20e 0 Pa	17.1 μm	1.28 μm	0.0804 μm	0.00506 μm	0.321 nm
	20e 1 Pa	62.4 μm	11.7 μm	0.804 μm	0.0506 μm	3.21 nm
	20e 2 Pa	168.0 μm	50.3 μm	7.78 μm	0.506 μm	0.0321 μm
	20e 3 Pa	NL	138.0 μm	39.9 μm	4.98 μm	0.321 μm

[†]not listed

Table 8: Predicted Maximum Deflection Results Corresponding to Non-fabricated Wafers

	Pressure	1/2"	1/4"	1/8"	1/16"	1/32"
10 μm membrane	20e-6 Pa	0.164 nm	0.0103 nm	0.642 pm	0.0402 pm	0.00253 pm
	20e-5 Pa	1.64 nm	0.103 nm	0.00642 nm	0.000402 nm	0.0253 pm
	20e-4 Pa	0.0164 μm	0.00103 μm	0.0642 nm	0.00402 nm	0.253 pm
	20e-3 Pa	0.164 μm	0.0103 μm	0.642 nm	0.0402 nm	0.00253 nm
	20e-2 Pa	1.63 μm	0.103 μm	0.00642 μm	0.402 nm	0.0253 nm
	20e-1 Pa	11.9 μm	1.02 μm	0.0642 μm	0.00402 μm	0.253 nm
	20e 0 Pa	38.5 μm	8.56 μm	0.641 μm	0.0402 μm	0.00253 μm
	20e 1 Pa	102.0 μm	31.2 μm	6.04 μm	0.402 μm	0.0253 μm
	20e 2 Pa	NL[†]	83.9 μm	25.1 μm	3.89 μm	0.253 μm
	20e 3 Pa	NL	NL	68.9 μm	20.0 μm	2.49 μm
30 μm membrane	20e-6 Pa	0.00608 nm	0.381 pm	0.0239 pm	0.00151 pm	0.0000966 pm
	20e-5 Pa	0.0608 nm	0.00381 nm	0.239 pm	0.0151 pm	0.00966 pm
	20e-4 Pa	0.000608 μm	0.0381 nm	0.00239 nm	0.151 pm	0.00966 pm
	20e-3 Pa	0.00608 μm	0.381 nm	0.0239 nm	0.00151 nm	0.0966 pm
	20e-2 Pa	0.0608 μm	0.00381 μm	0.239 nm	0.0151 nm	0.000966 nm
	20e-1 Pa	0.608 μm	0.0381 μm	0.00239 μm	0.151 nm	0.00966 nm
	20e 0 Pa	6.02 μm	0.381 μm	0.0239 μm	0.00151 μm	0.0966 nm
	20e 1 Pa	40.8 μm	3.79 μm	0.239 μm	0.0151 μm	0.966 nm
	20e 2 Pa	127.0 μm	30.0 μm	2.38 μm	0.151 μm	9.66 nm
	20e 3 Pa	332.0 μm	103.0 μm	21.0 μm	1.51 μm	0.0966 μm

[†]not listed

Another useful tool is to calculate the predicted mechanical sensitivity of the microphones. Sensitivity is measured as the deflection per pressure with units of μm/Pa. For this case, the values at 2 Pa of pressure listed in the two tables above (Table 7 and Table 8) were divided by 2 Pa. The 2 Pa values were used since that was the approximate excitation for the tests will be presented later. These values are shown below in Table 9.

Table 9: Predicted Mechanical Sensitivity Values (μm/Pa)

	1/2"	1/4"	1/8"	1/16"	1/32"
4 μm	13.8	3.99	0.493	0.0314	0.00196
10 μm	5.95	0.51	0.0321	0.00201	0.000127
20 μm	1.03	0.064	0.00402	0.000253	0.0000161
30 μm	0.304	0.0191	0.0012	0.0000755	0.00000483

5.1.2.1 Family of Curves After completing the ANSYS solutions, the data was plotted in Excel using a log-log scale. This was done for two different types of comparisons. The first comparison created a family of curves that included the deflection data for each membrane thickness on one graph, making a total of four different graphs. The other comparison created a family of curves for each of the five microphone sizes. From any of the graphs, the expected deflection for a particular pressure can be determined.

The comparison for the membrane thicknesses produced the expected results, as shown in Figure 42 for a 4 micron family of curves. This illustrates how a 4 micron membrane deflects for various membrane sizes. The membrane with the highest deflection was 1/2" and the deflection decreased as the size decreased. It is also apparent that the smaller membranes have a more linear trend than the larger membranes, showing that they have a larger stiffness. The nonlinear region for deflection greater than 1 micron is a results of strain stiffening. Results for the other membrane thickness are similar and are attached in the Appendix.

Plotting the data for a specific microphone size, as shown in Figure 43 for 1/4" microphones, also produced the expected results. Again, the additional plots for the other sizes are included in the Appendix. The membrane with the most deflection was the thinnest membrane, and the deflection decreased with increasing membrane thickness. The plots also show that the thinner membranes fall out of the linear region more quickly than the thicker membranes. Also, at lower pressures, it will be extremely difficult to get any response from the smaller membranes, since the deflections can be less than the pico-meter range at low pressures (one example of this is the 1/32" at 20e-6 Pa).

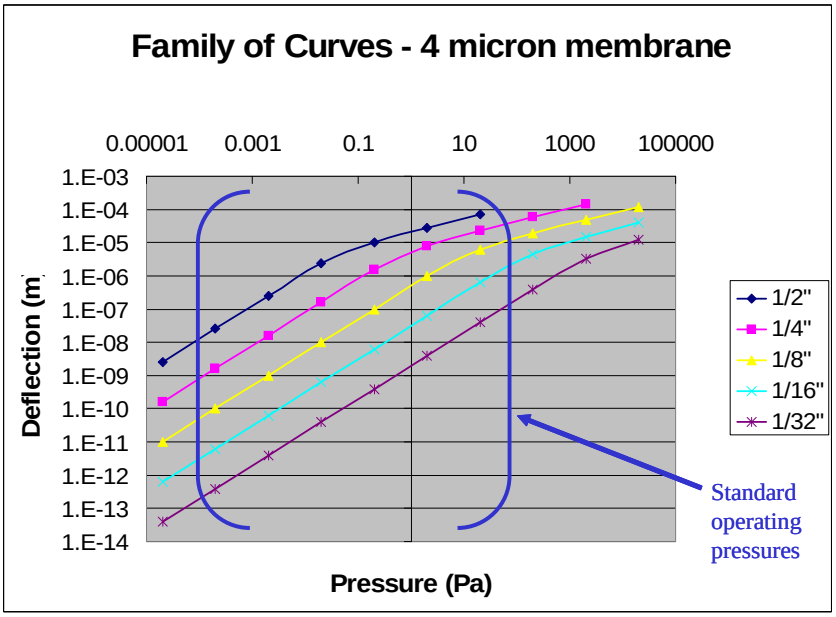

Figure 42: 4 μm Family of Curves

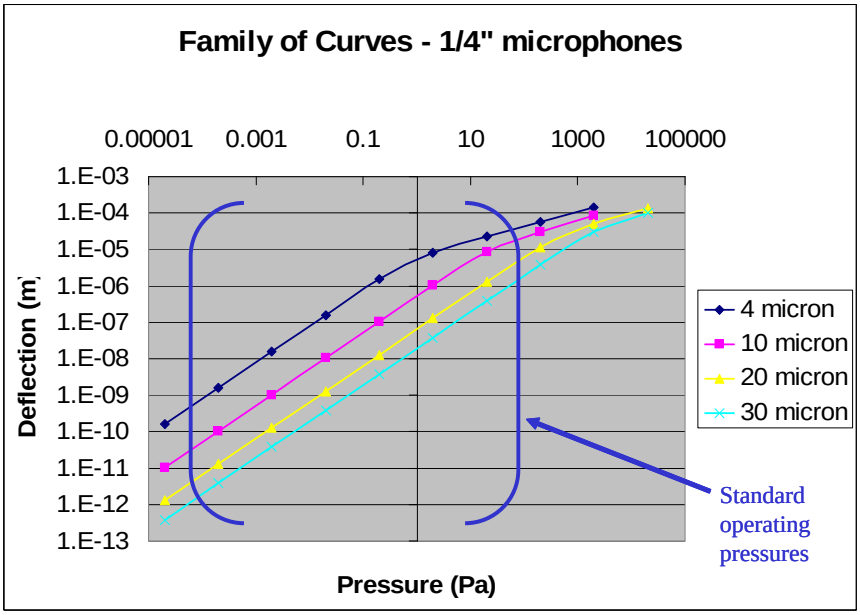

Figure 43: 1/4" Family of Curves

5.2 TESTING WITH MICROVISION

All of the existing microphones were tested by using the Microvision system at CMU. Microvision was used for its ability to measure the motion of a MEMS device in the x, y, and z directions. In this case, the movement in the z direction was the most important. However, the x and y movements were observed to ensure that the motion was not comprised solely of background noise.

To test the MEMS microphones, the Microvision system was set to sweep through a range of 10 linearly spaced frequencies from 100 Hz to 10 kHz, which was well below the calculated natural frequencies. This type of analysis is called a swept sine analysis. A small microphone (Kobitone microphone, Mouser product number 25LM032) was hooked up to the power amplifier and was used to project the pre-set frequencies at the MEMS microphones to get the membranes to vibrate. Any motion was then picked up by the Microvision microscope with the 50× lens and graphs were produced by the computer program. The plots could not be saved in Microvision, so the data was saved and later imported into Matlab to regenerate the plots. From this data, the movement of the membrane could be observed at the various frequencies. The data plotted displacement versus frequency. Each microphone was observed in two different locations.

5.2.1 Microvision Results

Upon analyzing the Microvision results regenerated in Matlab, it was determined that more testing would have to be performed. The Microvision results had too many inconsistencies to provide useful results. For example, deflections in the x and y directions that at times higher than the deflection in the z direction. Further, they also did not correspond well with the ANSYS results. Microvision was used a second time for the 4 micron membranes.

The following, Figure 44, contains two of the results from Microvision. This shows the deflection of the membrane in all directions for a 1/2" (20 micron holes, 60CC) microphone membrane and a 1/32" (20 micron holes, 80CC) microphone membrane. The larger microphones had results showing a slightly larger deflection along the z axis than the results for the smallest microphone. From the ANSYS results, it is clear that the deflection results should not be so close to one another. The 1/32" microphone was expected to have around 5 orders of magnitude smaller deflection when compared to the 1/2" microphone. It is estimated that the Kobitone microphone produced levels between 60-80 dB (20e-3 Pa to 20e-2 Pa), which gives a predicted deflection for the 1/2" 20 micron membrane between 0.2 μm and 0.32 nm. Another observation was that as the microphone size became smaller, the measured deflection results between the three directions became closer in magnitude. It is possible that Microvision was not able to pick up any deflection of the smaller microphone membranes due to the fact that their natural frequency was very high, indicating that they are too stiff to be an effective transducer. A main possibility for the poor results could have been from the speaker exciting the microscope stage and causing excitation in the x and y directions or from poor signal to noise ratio.

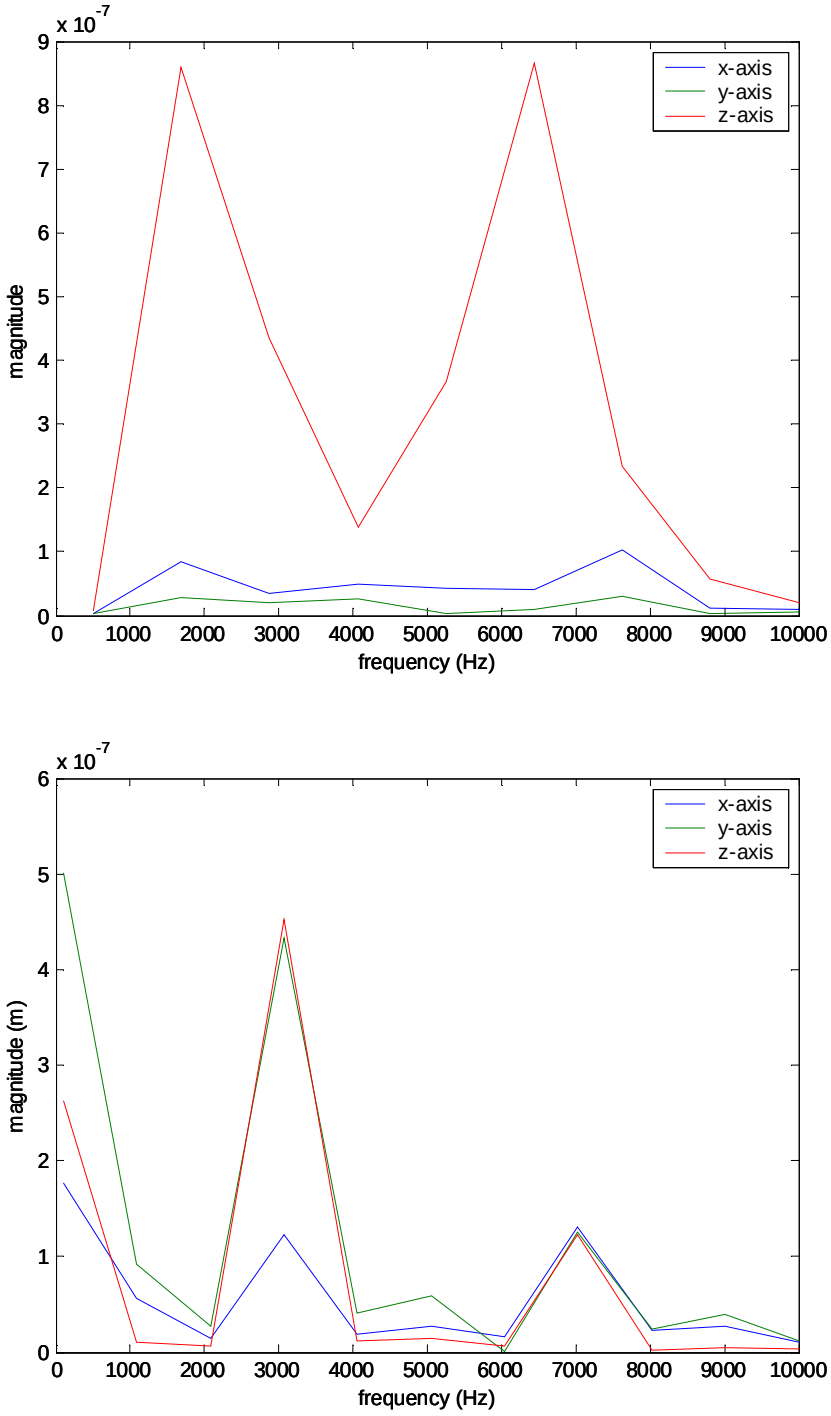

Figure 44: Microvision Results for 1/2" (top) and 1/32" (bottom) Microphone Membranes

5.3 TESTING WITH FOTONIC SENSOR

Another way to test the membrane deflection is with a fotonic sensor, which is focused on the SOI microphones. By connecting a power amplifier (Marchand Elctronics, PM24) and speaker (Peerless 832757), fotonic sensor (MTI 2000), and a microphone (1/2" B&K Type 4190) into SigLab (Model 20-42), the deflection can be measured. SigLab is used to generate white noise signals to excite the membranes and make all measurements. The measurements will show the transfer function and coherence for both the fabricated microphones (Channel 2 data) and the B&K microphone (Channel 3 data). The B&K microphone was used as a reference to compare to the collected data and to measure the actual sound pressure level at the membranes. The test set-up is depicted below in Figure 45.

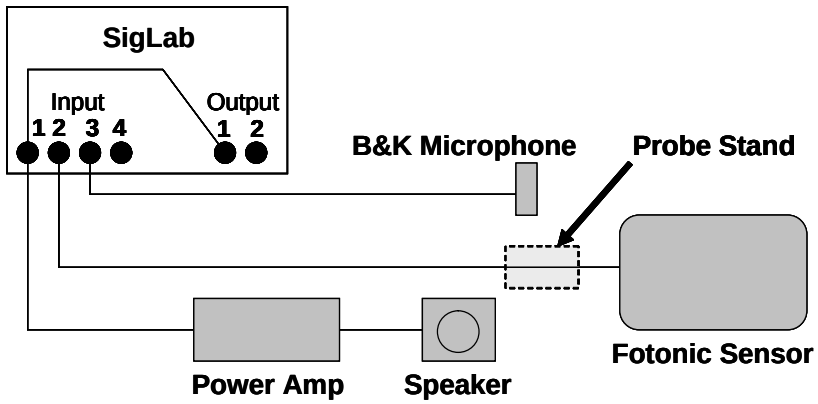

Figure 45: Fotonic Sensor Testing Set-up

Some general modifications were made from the Microvision test set-up since these measurements were performed in-house in the Sound, Systems, and Structures Laboratory. A bigger speaker was used to improve the signal to noise ratio and provide for louder noise since the fotonic sensor was not as sensitive as Microvision. It was found that levels of 2 Pa (100 dB) were required to produce appreciable deflections. However, this change also came

with the added risk of exciting the test stand. Driving the speaker hard also gave better coherence results.

In order to assure that the results in SigLab were not due to the vibration of the table, a plain silicon wafer was taped to the table and tested. Provided that the measurements were not recording motion, the SOI wafers would then be tested. Since this test performed with better results, the SOI microphones were excited by random acoustic noise and by a sine wave. The bandwidths tested included a range of 50 Hz, 100 Hz, 500 Hz, and 1000 Hz with a voltage of 0.6 V RMS. The power amplifier had a gain of 10. When taking the results, the coherence between the excitation signal and fotonic sensor was found to be poor above 500 Hz, so the bandwidth was limited to 1000 Hz, which is still much lower than the smallest microphone mode calculated for the natural frequencies.

5.3.1 Fotonic Sensor Results

After examining the results from this round of testing, it was clear that there was still motion being detected from the drive of the speaker. On average, the response for many of the microphones were almost identical. It is not understood why this occured. There were distinct modes around 80 Hz, 150 Hz, 210 Hz, and 810 Hz (shown in Figures 46 - 48). Given the low frequency and the fact that they do not change indicates these are the modes of the measurement stand. Foam padding was added under both the speaker and the probe stand, however the response from the 1/2" - 20 micron membrane, 1/4" - 4 micron membrane, and blank silicon wafer remained similar.

The following results collected from SigLab show the coherence (top plot), FRF (Frequency Response Function) magnitude (middle plot), and FRF phase for each test (bottom plot). Figure 46 gives the results for the blank silicon wafer. Figure 47 shows the 1/4" 4 micron membrane results while the 1/2" 20 micron membrane results are shown in Figure 48. The green and blue lines represent, respectively, the FRF between the white noise input signal and the B&K microphone and membrane. The red line shows the FRF between the membrane and the B&K microphone, therefore representing the broadband sensitivity of the

device, where the effects of the speaker dynamics have been removed. From the magnitude and phase results, it is shown that modes occur around 80 Hz, 150 Hz, 210 Hz, and 810 Hz. These modes are common to all of the results and also much lower than the expected natural frequency given in Table 6, which implies that they are likely from the test stand. The good coherence in Figures 46 - 48 occurs in the vicinity of the modes of the test stand (0-500 Hz at 500 Hz).

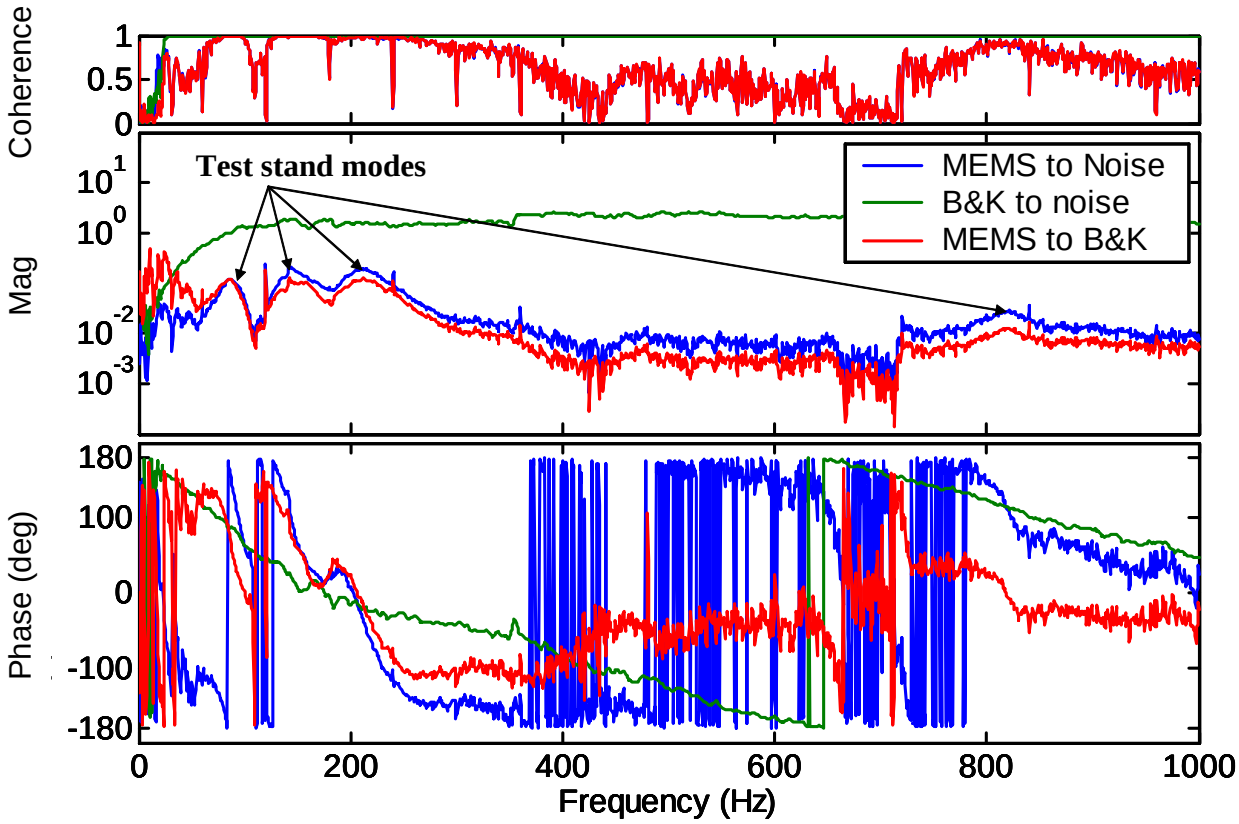

Figure 46: Blank Wafer Test

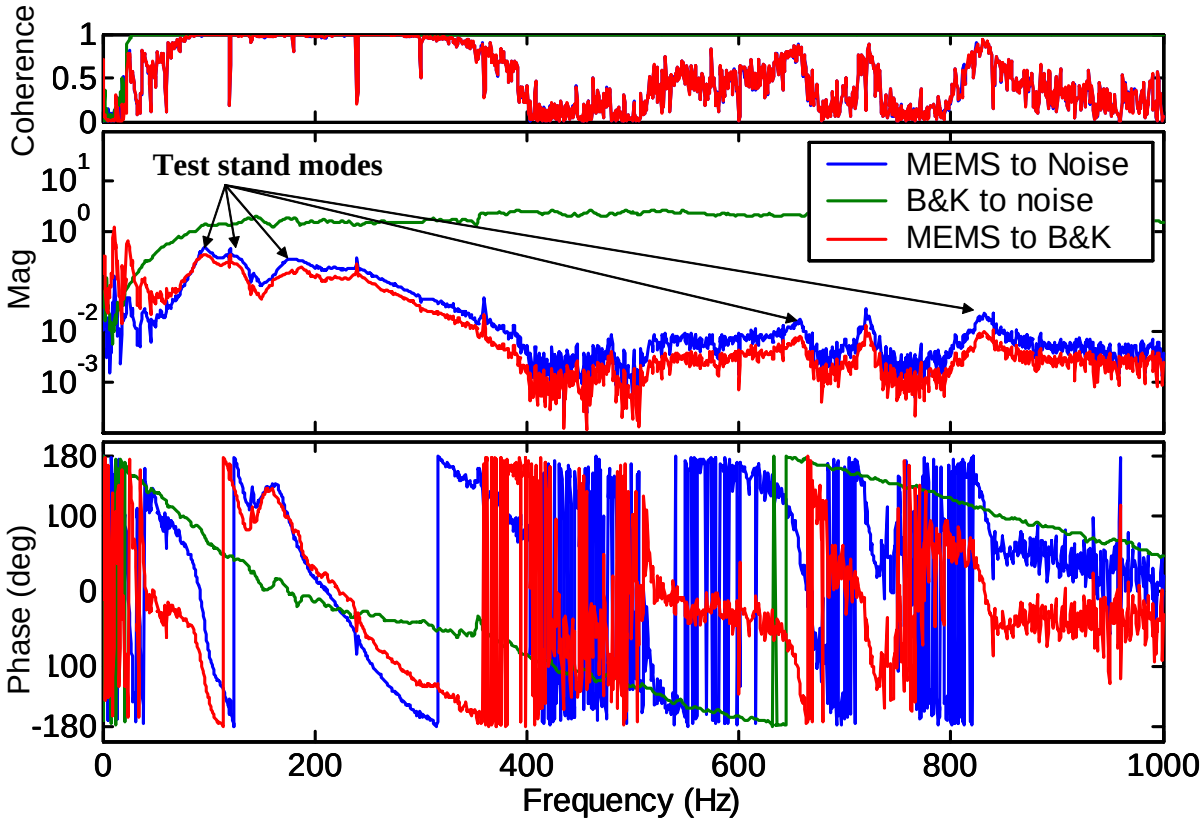

Figure 47: 1/4" 4 micron Membrane Test

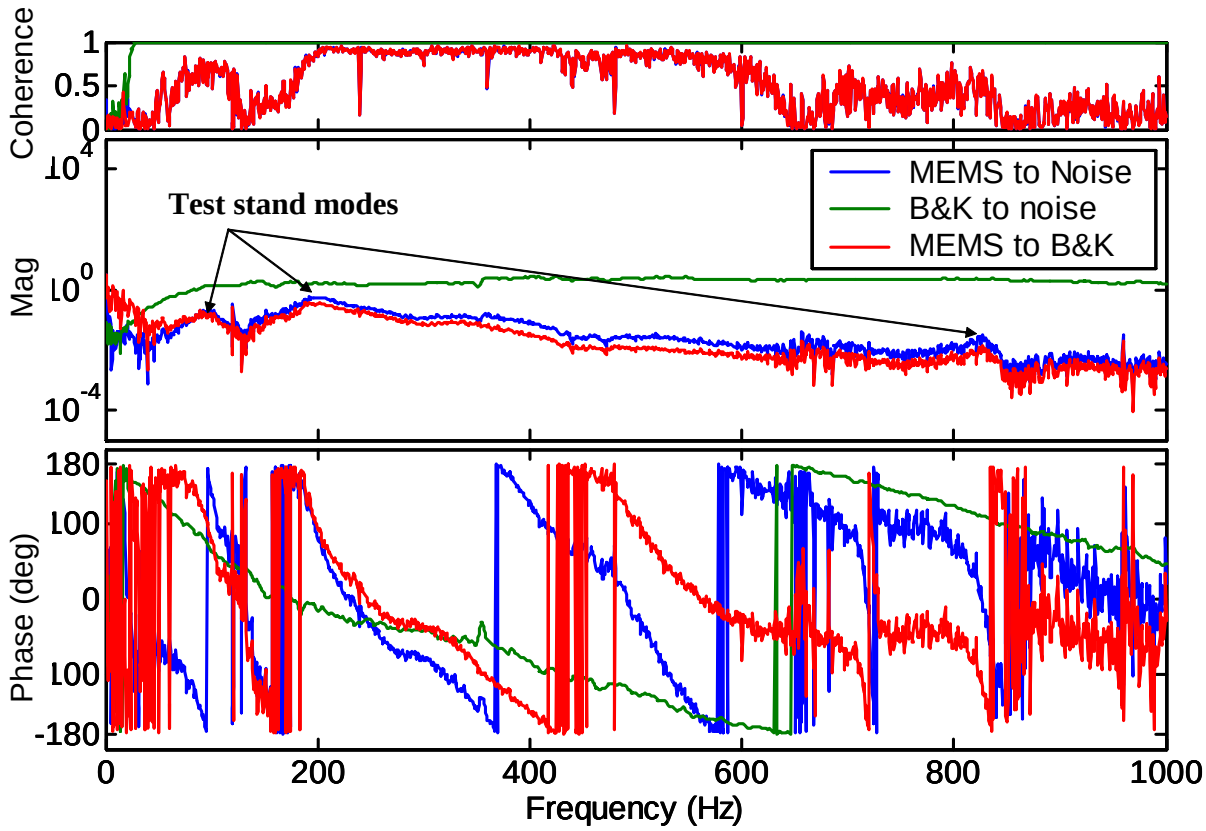

Figure 48: 1/2" 20 micron Membrane Test

5.4 PROFILOMETER TESTING

This test did not provide clear results that the microphone membranes were performing as expected. After two different types of testing methods were attempted without good results, it is possible that the membranes are not deflecting due to stiction. This would also explain why the blank silicon pieces gave similar results to the supposed membranes. Stiction is short for static friction and is name for the strong adhesion between contacting crystalline surfaces. It also includes sticking problems due to contamination. For the fabricated microphones, stiction could have occurred during the drying process after all of the etching was completed. Small water droplets could have remained afterwards causing the membrane to stick to the top silicon surface of the backplate.

In order to test the membranes for stiction, they were tested by a Dektak profilometer. This machine measures the level changes of a substrate. For this case, the membrane level was checked to determine if the height level dipped towards the middle due to stiction.

Several microphone membranes were examined in the profilometer. While the levels of the membranes were not completely even, there was no evidence of stiction. This was more noticeable on the thinner membranes, where the force of the profilometer caused the membrane to move. If the deflection problems of the membrane were due to stiction, the membranes would not have been able to be moved with the profilometer. On closer inspection through the machine, the silicon membranes contained thin cracks.

5.5 CHAPTER SUMMARY

This chapter discussed the testing results of the microphone membranes. It highlighted three background calculations performed on the microphones, such as natural frequency calculations, ANSYS static deflections, and also plotted out the ANSYS results for more clarification. The results of the two dynamic tests using Microvision and a Fotonic Sensor were discussed along with any corresponding data.

6.0 CONCLUSIONS AND FUTURE CONSIDERATIONS

In conclusion, microphone membranes were fabricated with SOI wafers of a 4 micron thickness and a 20 micron thickness. The fabrication process was documented and changes were made to previous trials in order to increase the fabrication success. The results of the fabrication process were noted through general observations and images gathered from the SEM machine.

Before mechanically testing the fabricated wafers, several calculations were made. First, the fundamental natural frequencies were calculated for the first frequency parameter for all five microphone sizes. These five sizes were 1/2", 1/4", 1/8", 1/16", and 1/32". Each size was then calculated for four different membrane thicknesses of 4 microns, 10 microns, 20 microns, and 30 microns. The natural frequencies were calculated in order to determine what frequencies would produce good results during acoustic testing. It also showed that some of the membranes with high frequencies would not be excited as easily as others.

All of the microphone sizes and membrane thicknesses were then run through a static nonlinear analysis in ANSYS to determine the maximum deflection of the membrane. The ANSYS model for each microphone required the membrane to be analyzed under pressures ranging from 20e-6 Pa to 20 kPa that increased by an order of magnitude. These results were used to determine the predicted deflection for the fabricated microphones. They were also used to create a family of curves for the different microphone membrane thicknesses and for the five sizes. These were used to look at the difference in the geometries in respect to the membrane deflection.

Once the calculations of the microphones were completed, they were tested mechanically. Two tests were run to determine the deflection. The first test, the Microvision system, used a swept sine analysis to measure the deflection at 10 linearly spaced frequencies. The second test was done with a fotonic sensor and used the aid of SigLab to change the incoming bandwidth and voltage to the test speaker. The results from both tests did not provide good enough results to determine if the membranes were deflecting as expected according to the ANSYS results. By using a profilometer to test for stiction, the membranes were observed to have thin cracks.

The suggestions for future work include four major topics. The first topic deals with the mask. The second change would be to the etching process. The third consideration is to the testing of the microphones. And finally, the last topic of change would be to add the electric connections and then more testing.

The mask should be redesigned to allow for only one set of hole center-to-center distances. Since the different distances change the required etching time, it would be more suitable to have only one distance on a wafer so that the oxide etching time was the same for the entire wafer. This would ensure that the entire wafer was released properly. To use more than one hole center distance, more masks would have to be produced.

A more important suggestion for the mask is to use a mask producer that can make smaller features with better resolution. The smaller holes might have come through if the mask could have been produced with a higher resolution. Also, with the better resolution, the photolithography process would have been clearer. This would result in more clearly defined features with smoother lines.

In order to be sure that the passivation layer from the RIE etching was removed, the wafer could be placed into the chamber for an oxygen plasma clean. This process would not etch the wafer, but simply remove any passivation layer that could possibly block the oxide etching by acting as a mask.

The oxide etching process was much better after switching to HF. However, the etching rate was too fast. By changing the concentration to 30-40% instead of 49%, the etching rate will be slower and easier to control.

Another etching process that could be added to this design was the backside etch for the backplate, which is common among other produced microphones. Most microphones do not have a solid block of material as the backplate. The backplate should be thinned through machining. This part of the design was left out due to time constraints.

A better testing apparatus would be another consideration. Microvision was helpful to determine if the microphones were moving, but it did not provide clear results. While the fotonic sensor gave slightly better results, there was still a problem with the stage moving due to the speaker vibration. A better analysis is needed to provide clear mechanical results and determine if the membranes were picking up sound. One possibility is the dynamic option of the Wyko NT1100 machine by Veeco. The Wyko DMEMS system can capture 3D measurement data as the device actuates and is capable of making both static and dynamic measurements.

Once the mechanical capabilities are verified, the last recommendation would be to create fully functioning microphones. This would include the process of heavily doping the membranes to make them more conductive, adding the electrical connections, and then testing the connections as in References [3], [10], [15], [21], and [23].

APPENDIX

FAMILY OF CURVES

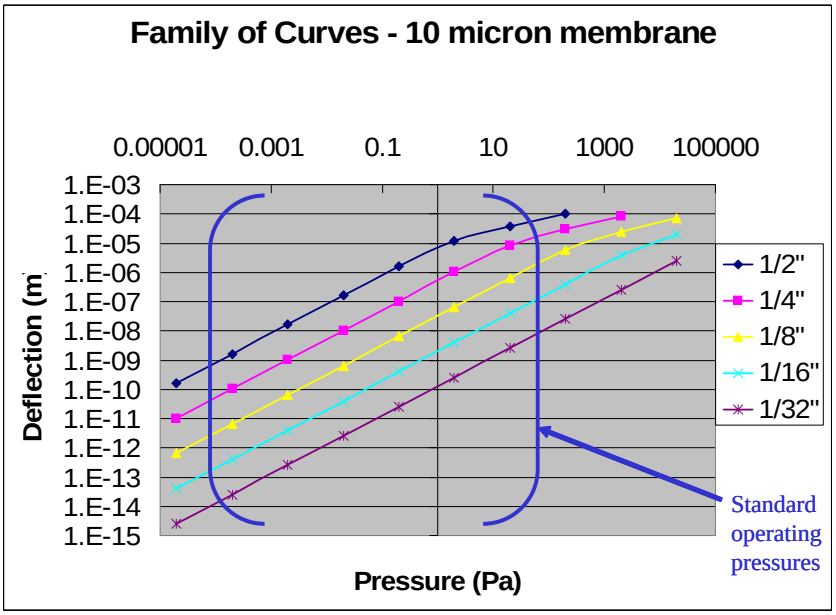

Figure 49: 10 μm Family of Curves

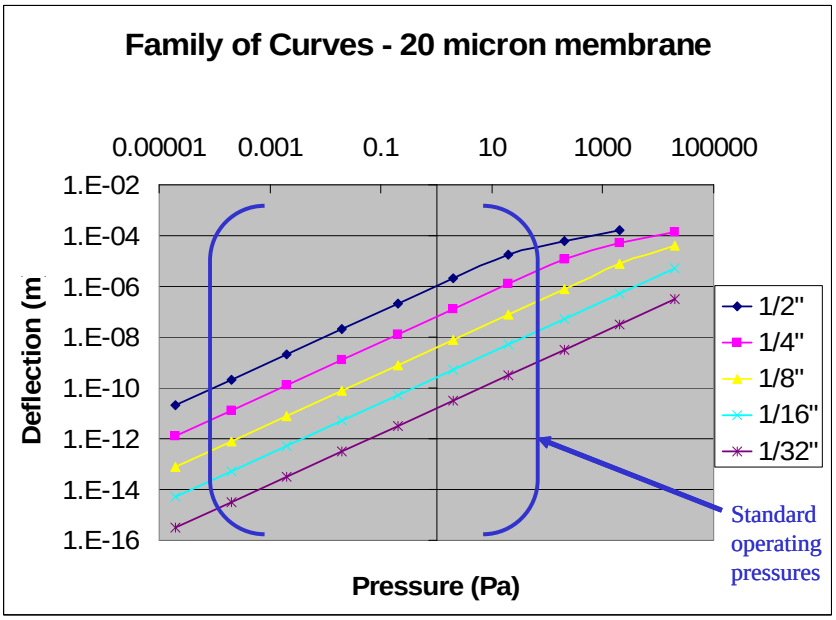

Figure 50: 20 μm Family of Curves

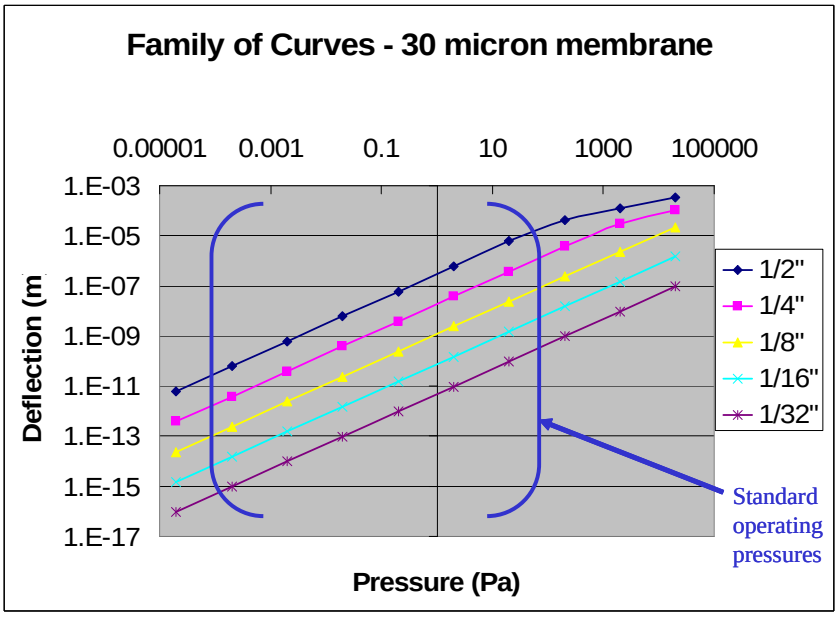

Figure 51: 30 μm Family of Curves

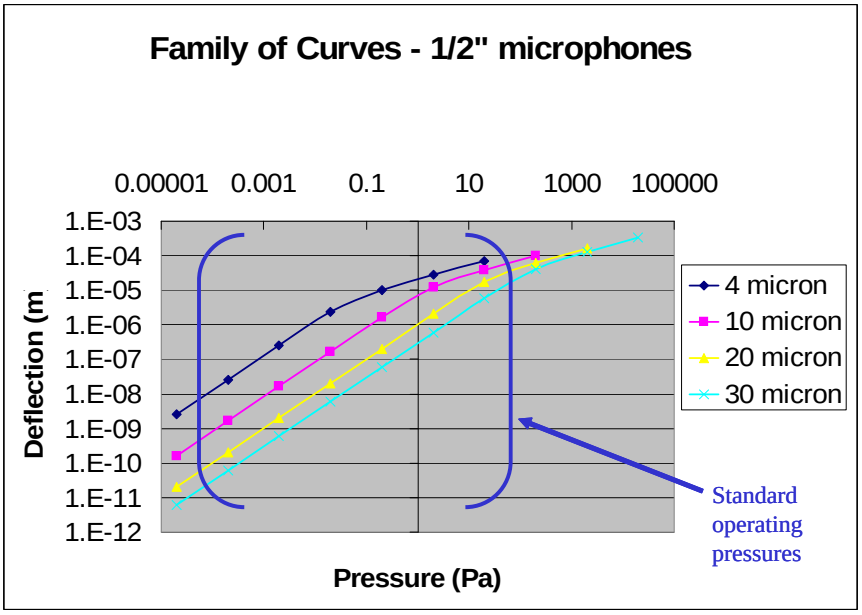

Figure 52: 1/2" Family of Curves

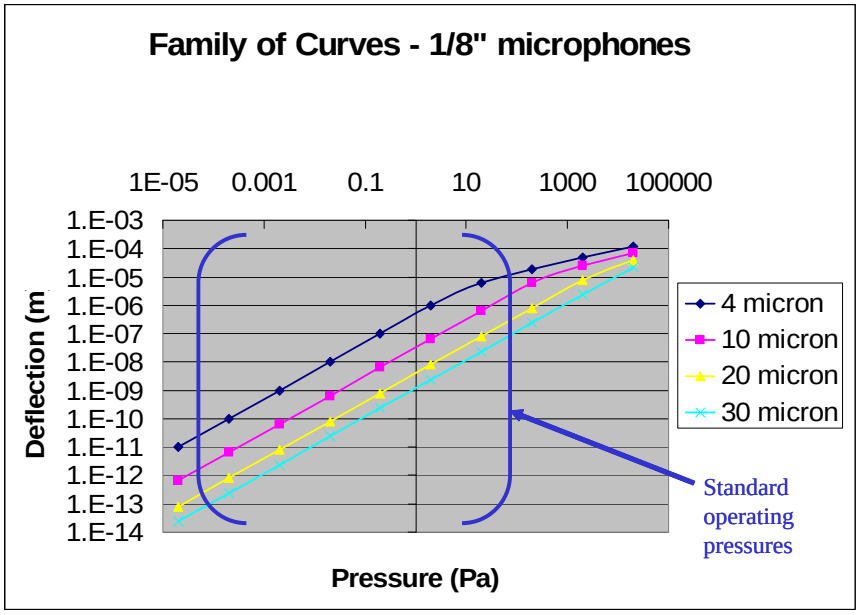

Figure 53: 1/8" Family of Curves

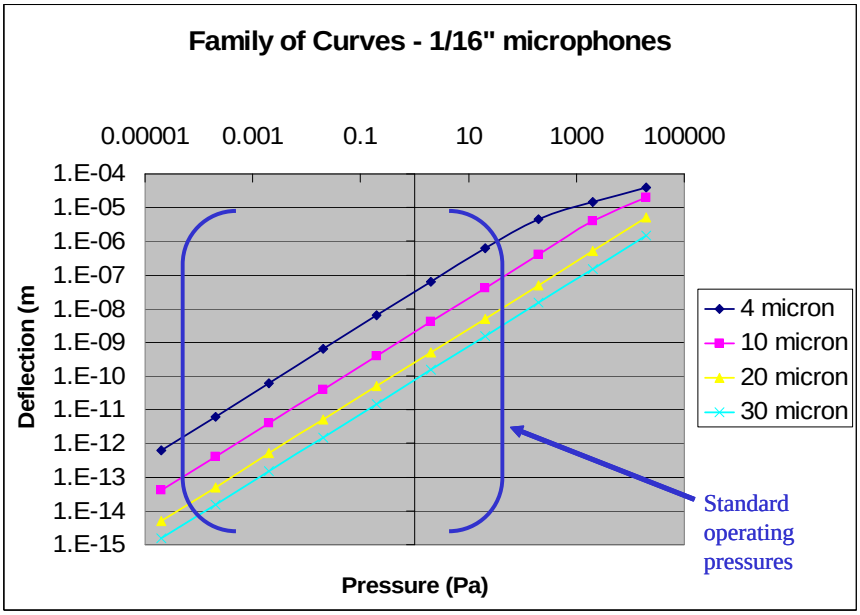

Figure 54: 1/16" Family of Curves

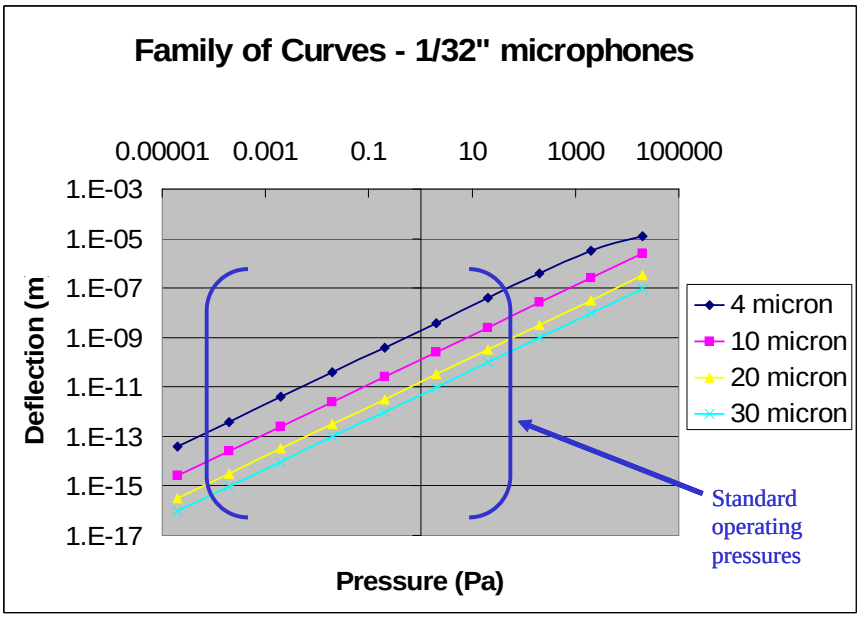

Figure 55: 1/32" Family of Curves

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