CONFORMANCE TEST SYSTEM DESIGN FOR ISO/IEC 18000-3 MODE 1 PASSIVE RFID

by

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The ISO/IEC 18000-3 standard deals with the Parameters for Air Interface Communications at 13.56 MHz. It defines three modes. This thesis focuses only on mode 1. Mode 1 is based on ISO/IEC 15693 that is adopted to define the way RFID "Contactless Integrated Vicinity Cards" communicate. It is commonly adopted by RFID manufacturers to be their guideline for high frequency (HF) RFID transponders.

As ISO/IEC 15693 has been widely adopted, the conformance test is important as it is the first step to evaluate the interoperability of the HF passive RFID products manufactured by different venders.

In this thesis, the development of a conformance test platform for ISO/IEC 18000-3 Mode 1 Passive RFID is described. This conformance test platform is implemented with National Instruments (NI) LabVIEW 8.5 and the LabVIEW FPGA module. It consists of two parts:

(1) An FPGA and host based ISO-18000 part 3 mode 1 conformed transceiver system (reader). This system is developed with the NI 5640R FPGA development board to realize the signal acquisition and processing in real-time. It supports all the mandatory and optional commands defined in ISO 18000-3 mode 1.

(2) A host based offline data measurement and testing platform. This platform is developed with LabVIEW 8.5 on the host PC to perform further measurement and test for the baseband waveform data acquired by the system in part (1).

This conformance test platform implemented is reusable, reconfigurable and can be customer defined within the parameters of the standard.

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PREFACE

I first express my gratitude and thanks to my advisor, Dr. Marlin H. Mickle, who offered me such a great opportunity for doing research and course work at RFID Center of Excellence. His enthusiasm in research and his personality deeply impressed me. His belief in me always encouraged me when I felt lost.

I would like to thank Dr. William Stanchina and Dr. Ronald G. Hoelzeman for serving on my thesis committee and giving me valuable suggestions on my thesis. I also appreciate Dr. Peter J. Hawrylak's support and guidance.

I want to thank my colleague and my friends, Dr. Yuan Sun, Dr. Ajay Ogirala and Michael Rothfuss for all their help.

I am also grateful to my family, who always support me and care about me.

1.0 INTRODUCTION

1.1 DESIGN MOTIVATION

RFID technology met a major milestone in 2001 by adopting international standardization. The market of the RFID products is becoming more and more mature. And the number of RFID product manufacturers has been increasing, and the importance of the international standards conformance and the interoperability correspondingly increases.

As an important part of passive RFID, the HF (13.56 MHz) RFID standard has been adopted for various applications. An automatic conformance test platform for HF passive RFID is therefore desirable.

There are some off-the-shelf conformance test platforms. However, most of them utilize a fixed core, and the parameters that can be customized are limited.

In these scenarios, a reconfigurable software defined conformance test platform can eliminate those shortcomings, and have its own features.

1.2 SCOPE OF WORK

In this thesis, an ISO 18000-3 mode 1/ ISO 15693 conformance test platform will be developed using NI LabVIEW 8.5 and LabVIEW FPGA module.

This conformance test platform will perform both real-time signal processing and offline data measurements and analysis.

Once the conformance test platform is implemented, commercial tags will be finally tested. The test results will be fully displayed on a GUI front panel using the host VIs and they will be easy to understand.

The contribution of this work will be in six areas:

(1) The designed conformance test platform is software-defined and is based on a reconfigurable FPGA board, so that the system is easy to be upgraded compared to those test platforms built on a fixed core.

(2) Each aspect of the standard will be analyzed and implemented in hardware and software.

(3) Means will be provided to adjust all of the parameters within the standard specifications.

(4) The data measurement and testing will be done automatically with the conformance test platform. For example, the characteristics of the signals, the timing of the reader requests and tag responses can all be measured automatically without requiring the user to manipulate the test devices.

(5) The waveform of signals can be saved. And the offline data measurement and analysis platform will be repeatable to test every device under test with the same data processing and testing methods.

(6) This conformance test platform will display the results in a format that is clear to read and easy to understand.

1.3 THESIS ORGANIZATION

The thesis is organized as follows:

First, in Chapter 2, the ISO 18000-3 protocol is introduced as it defines all the parameters for the communication between the interrogator and the tag.

Second, in Chapter 3, the development methods and procedure of the reconfigurable ISO 18000-3 mode 1/ ISO 15693 conformance test platform are described.

Third, in Chapter 4, the test results of the commercial RFID tags with the conformance test platform implemented are discussed.

Finally, the Conclusion of the thesis is presented in Chapter 5, and the Future research is discussed in Chapter 6.

2.0 ISO 18000-3 PROTOCOL BACKGROUND

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form a specialized system for worldwide standardization. ISO/IEC 18000 consists of a series of technical standards, under the general title Information technology — radio frequency identification for item management: and each for a unique frequency band.

ISO/IEC 18000-3 defines parameters for air interface communications at 13.56 MHz. It specifies three modes of operations in order to address different applications. The three modes are not interoperable. Either the interrogator/reader or the tags conformed with ISO/IEC 18000-3 shall support at least one of the modes or all of the modes as an option.

The conformance test platform developed in this thesis focuses on ISO/IEC 18000-3 mode 1. Mode 1 is compliant with ISO/IEC 15693, and describes a read/write system using a "reader talks first" technique. It specifies three main sections. (1) the “Physical Characteristics”, (2) the “Air interface and initialization” and (3) the “Anticollision and transmission protocol”.
A brief introduction of the standard is given in the following sections.

2.1 ISO 18000-3 MODE 1/ ISO 15693 AIR INTERFACE AND INITIALIZATION [1][2]

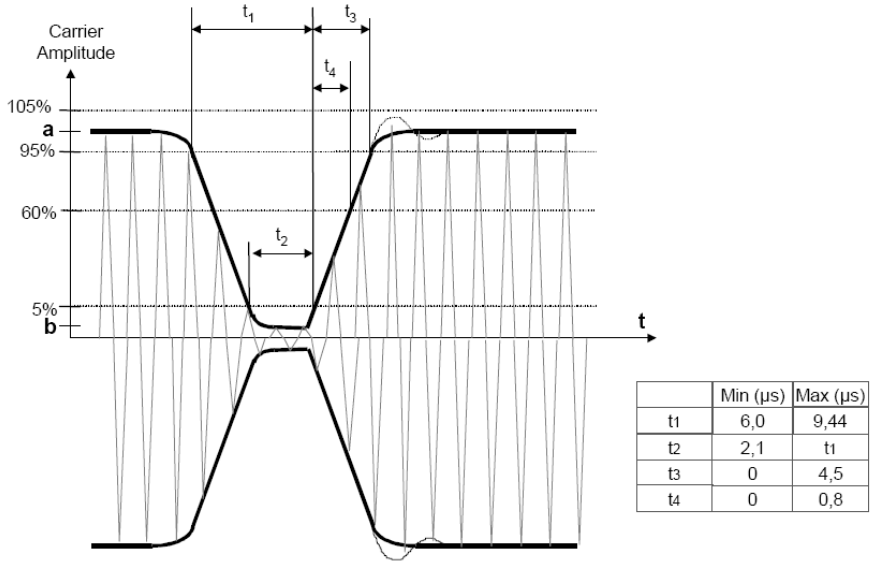
2.1.1 Communications signal interface interrogator/ reader to tag

Several parameters for the communication between interrogator/reader and tag are defined in ISO/IEC 15693-2 protocol.

2.1.1.1 Modulation

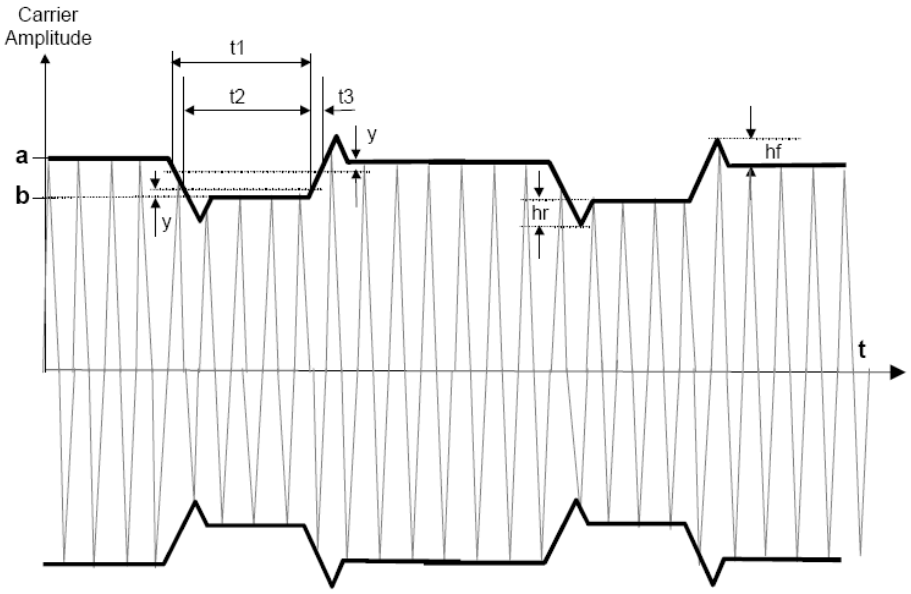
Interrogator/reader to tag communication uses the modulation principle of amplitude shift keying (ASK). Two modulation indices are used, 10% and 100%. The interrogator makes the choice of modulation indices. The tag shall be able to decode both.

Modulation of the carrier for 100% ASK, and modulation of carrier for 10% ASK are shown in Figure 1 and Figure 2.



	Min (µs)	Max (µs)
t1	6,0	9,44
t2	2,1	t1
t3	0	4,5
t4	0	0,8

Figure 1. modulation of 100% ASK



	Min	Max
t1	6,0 µs	9,44 µs
t2	3,0 µs	t1
t3	0	4,5 µs
Modulation Index	10%	30%

y	0,05 (a-b)
hf, hr	0,1 (a-b) max

Figure 2. modulation of 10% ASK

For either of the modes, the modulation index is defined by (a-b) / (a+b) as noted in the figures. And for 10% ASK, the tag shall be operational for any value between 10% and 30%.

2.1.1.2 Data coding and data rate

Data coding shall be implemented using pulse position modulation (PPM). Two modes of data coding shall be used. They are 1 out of 4 PPM and 1 out of 256 PPM. Both of the modes shall be supported by the tag. The interrogator makes the decision of the mode and indicates the tag within a start of frame (SOF).

(1) 1 out of 256 data coding mode

The 1 out of 256 pulse position modulation technique is as shown in Figure 3.

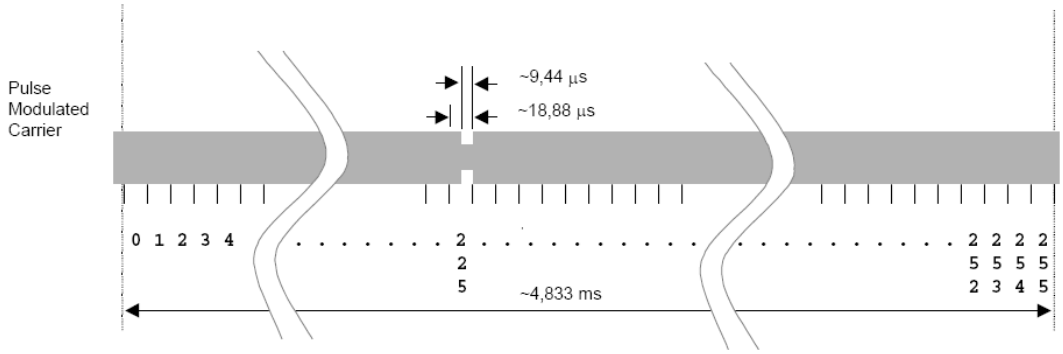


Figure 3. 1 out of 256 data coding mode (data = (11100001)b =225)

In this mode, the value of one byte of the transmitted data is represented by the position of one pulse and is ranged from 0 to 255. The value of the byte is determined by the position of the pulse on 1 of the 256 successive time periods of $256/f_c$ (~18.88 us, where f_c is the frequency of the carrier wave). The pause shall occur at the second half of the position of the time period that indicates the value, as shown in Figure 4.

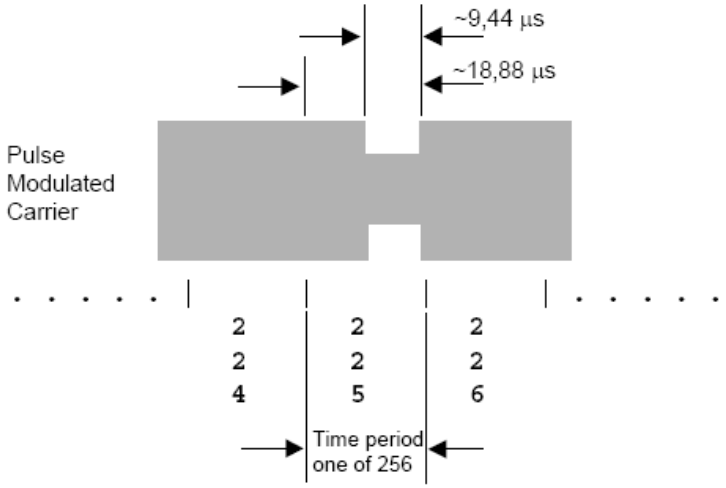


Figure 4. Detail of one time period

The transmission time of one byte is 4.833 ms, thus, the data rate is 1.66 kbits/s ($f_c/8192$). The last byte should be followed by an end of frame (EOF).

(2) 1 out of 4 data coding mode

The 1 out of 4 pulse position modulation technique is as shown in Figure 5.

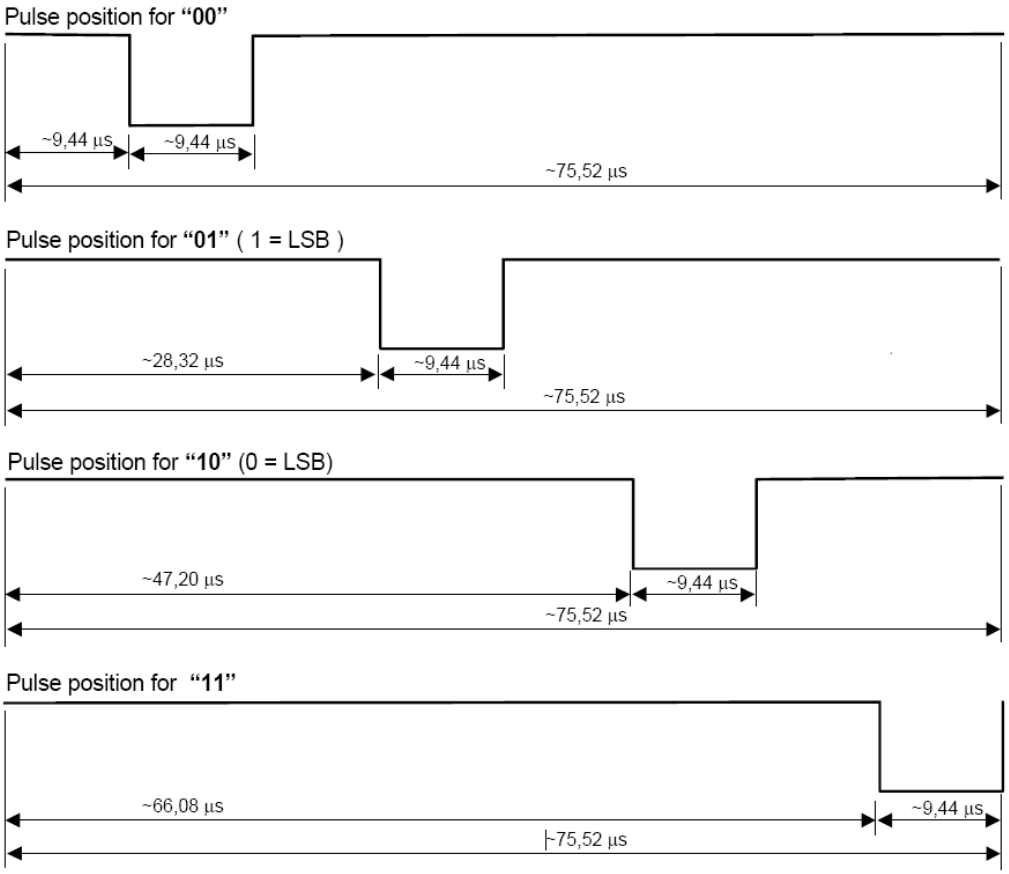


Figure 5. 1 out of 4 data coding mode

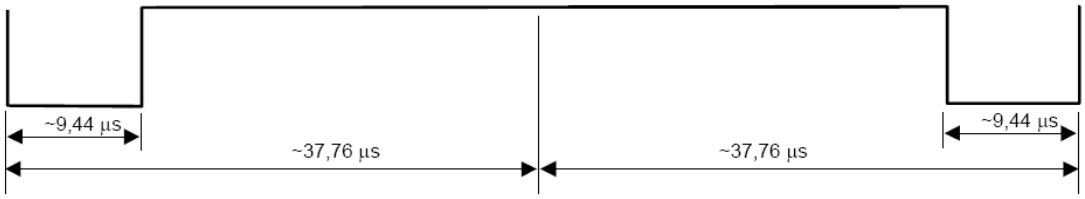
For this data coding mode, the position of one pulse determines two bits of the data to be transmitted at a time. Four successive pairs of bits form a byte where the least significant pair of bits is transmitted first. The data rate of 1 out of 4 mode is 26.48 kbits/s (f_c/512).

2.1.1.3 Start of frame (SOF) and End of frame (EOF)

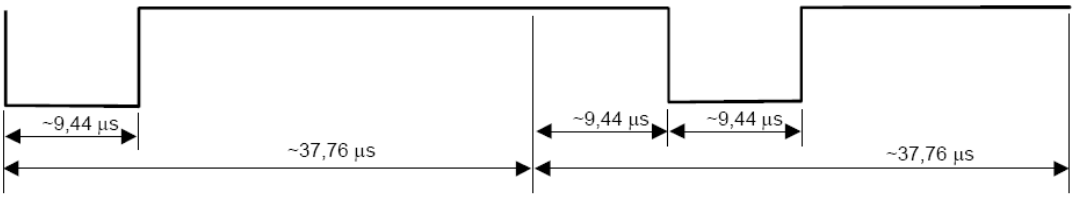
Framing is used for ease of synchronization and independence of protocol. Frames shall be delimited by a start of frame (SOF) and an end of frame (EOF).

The SOF has two modes, one is to indicate the selection of 1 out of 256 data coding mode, and the other is to indicate the selection of 1 out of 4 data coding mode.

The SOF sequences are as shown in Figure 6.



(a) 1 out of 256 data coding mode



(b) 1 out of 4 data coding mode

Figure 6. Start of frame

The EOF has a unique format that is applied to either of the data coding mode.

The EOF sequences are as shown in Figure 7.

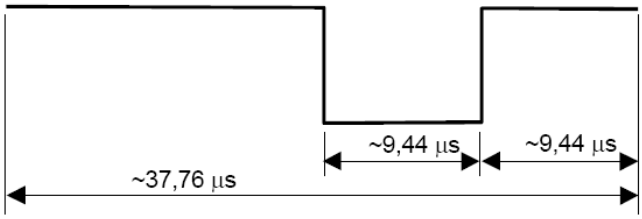


Figure 7. End of frame for either data coding mode

2.1.2 Communications signal interface tag to interrogator/reader

2.1.2.1 Subcarrier

The tag shall communicate to the interrogator, using load modulation, that a subcarrier with frequency f_s shall be generated by load the carrier f_c. One or two subcarriers may be used. This is selected by the interrogator using the first bit in the protocol header. The interrogator shall be capable of supporting both of the two subcarrier modes.

When one subcarrier is used, the frequency of the subcarrier shall be $f_{s1} = f_c/32$ = 423.75 kHz.

When two subcarriers are used, the frequency of the subcarriers shall be $f_{s1} = f_c/32$, $f_{s2} = f_c/28$ = 484.28 kHz.

2.1.2.2 Data rate

Two data rates may be used for each of the two subcarrier modes. The selection of the low data rate or high data rate is made by the interrogator using the second bit in the protocol header. The interrogator shall support the data rates as listed in Table 1.

Table 1. Tag to interrogator data rates

Data Rate	Single Subcarrier	Dual Subcarrier
Low	6,62 kbits/s (fc/2048)	6,67 kbits/s (fc/2032)
High	26,48 kbits/s(fc/512)	26,69 kbits/s (fc/508)

2.1.2.3 Bit representation and coding

The data bit shall be encoded using Manchester coding.

(1) Bit coding when using one subcarrier

Bit coding when using one subcarrier with high data rate is as shown in Figure 8. When low data rate is selected, the same subcarrier frequency shall be used, and in this case the number of pulses and the timing should be multiplied by 4.

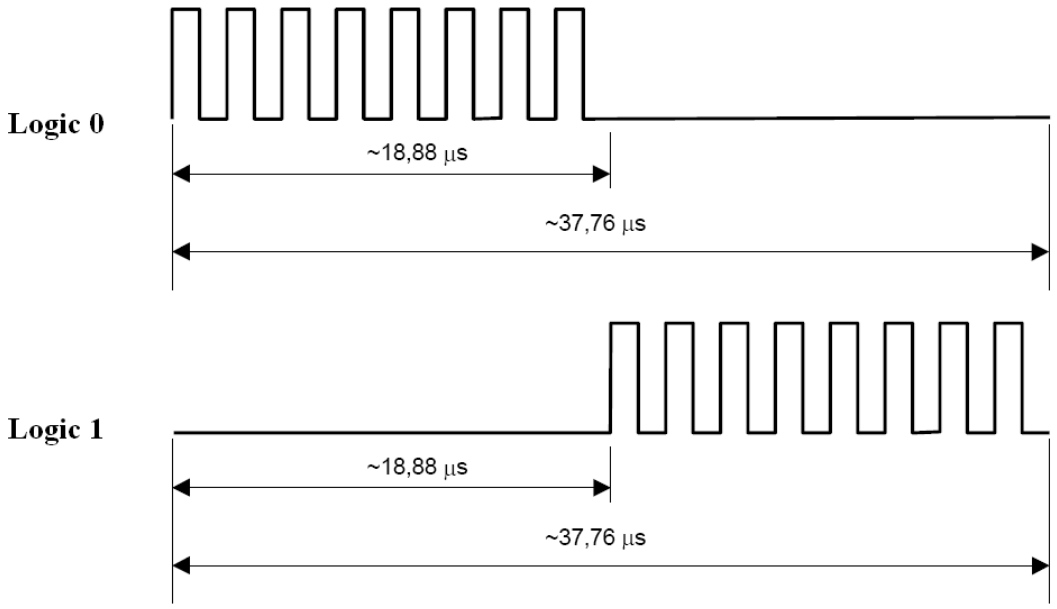


Figure 8. One subcarrier- high data rate bit coding logic 0 and logic 1

As shown in the figure, when the high data rate is used, a logic 0 starts with 8 pulses of $f_c/32$ (~423,75 kHz) followed by an unmodulated time of $256/f_c$ (~18,88 μs), and a logic 1 starts with an unmodulated time of $256/f_c$ (~18,88 μs) followed by 8 pulses of $f_c/32$ (~423,75 kHz).

(2) Bit coding when using two subcarriers

Bit coding when using two subcarriers with high data rate is as shown in Figure 9. When the low data rate is selected, the same subcarrier frequencies shall be used, and in this case the

number of pulses and the timing should be multiplied by 4. The phase transitions between the two subcarriers are continuous.

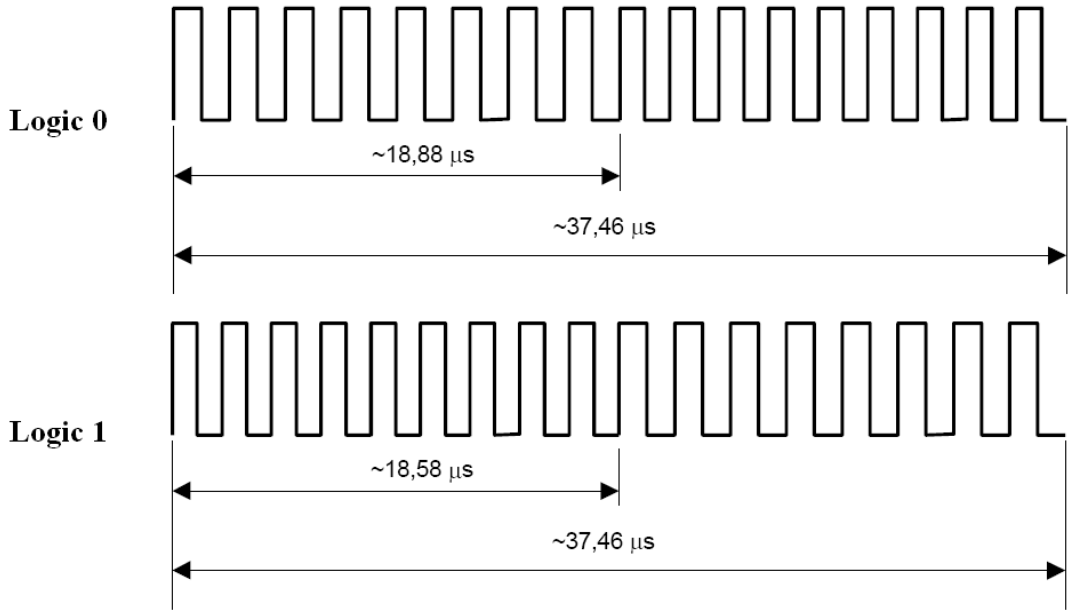


Figure 9. Two subcarriers- high data rate bit coding logic 0 and logic 1

As shown in the figure, when the high data rate is used, a logic 0 starts with 8 pulses of $f_c/32$ (~423,75 kHz) followed by 9 pulses of $f_c/28$ (~484.28 kHz), and a logic 1 starts with 9 pulses of $f_c/28$ (~484.28 kHz) followed by 8 pulses of $f_c/32$ (~423,75 kHz).

2.1.2.4 Tag to interrogator frames

Framing is used for ease of synchronization and independence of the protocol. Frames shall be delimited by a start of frame (SOF) and an end of frame (EOF).

2.1.2.4.1 Start of frame (SOF)

(1) SOF when using one subcarrier

The SOF for using one subcarrier with the high data rate is as illustrated in Figure 10. When the low data rate is selected, the same subcarrier frequency shall be used, and in this case the number of pulses and the timing should be multiplied by 4.

Figure 10. Start of frame when using one subcarrier high data rate

As shown in the figure, the SOF consists of three parts: an unmodulated time of $768/f_c$ (~56.64 µs), 24 pulses of $f_c/32$ (~423.75 kHz), a logic 1 which starts with an unmodulated time of $256/f_c$ (~18.88 us), followed by 8 pulses of $f_c/32$ (~423.75 kHz).

(2) SOF when using two subcarriers

The SOF for using two subcarriers with the high data rate is as illustrated in Figure 11. When the low data rate is selected, the same subcarrier frequency shall be used. In this case the number of pulses and the timing should be multiplied by 4.

Figure 11. Start of frame when using two subcarriers high data rate

As shown in the figure, the SOF consists of three parts: 27 pulses of $f_c/28$ (~484.28 kHz), 24 pulses of $f_c/32$ (~423.75 kHz), a logic 1 which starts with 9 pulses of $f_c/28$ (~484.28 kHz), followed by 8 pulses of $f_c/32$ (~423.75 kHz).

2.1.2.4.2 End of frame (EOF)

(1) EOF when using one subcarrier

The EOF for using one subcarrier with the high data rate is illustrated in Figure 12. When the low data rate is selected, the same subcarrier frequency shall be used. In this case the number of pulses and the timing should be multiplied by 4.

Figure 12. End of frame when using one subcarrier high data rate

As shown in the figure, the EOF consists of three parts: a logic 0 which starts with 8 pulses of $f_c/32$ (~423.75 kHz) followed by an unmodulated time of $256/f_c$ (~18.88 us), 24 pulses of $f_c/32$ (~423.75 kHz) and an unmodulated time of $768/f_c$ (~56.64 µs).

(2) EOF when using two subcarriers

The EOF for using two subcarriers with the high data rate is illustrated in Figure 13. When the low data rate is selected, the same subcarrier frequency shall be used, and in this case the number of pulses and the timing should be multiplied by 4.

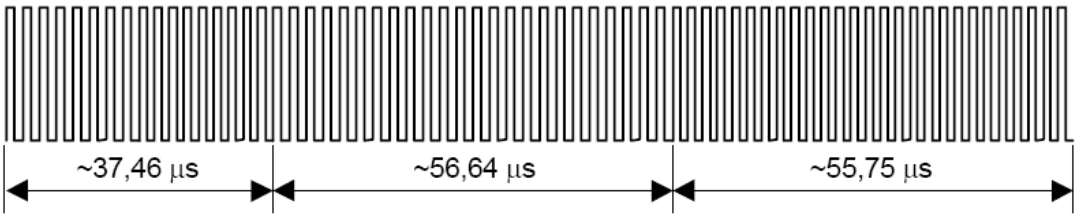


Figure 13. End of frame when using two subcarriers high data rate

As shown in the figure, the EOF consists of three parts: a logic 0 which starts with 8 pulses of $f_c/32$ (~423.75 kHz) followed by 9 pulses of $f_c/28$ (~484.28 kHz), 24 pulses of $f_c/32$ (~423.75 kHz), and 27 pulses of $f_c/28$ (~484.28 kHz).

2.2 ISO 18000-3 MODE 1/ ISO 15693 TRANSMISSION PROTOCOL

The mechanism to exchange instructions or data between the interrogator and the tag is based on the concept of “reader talks first”, which means the tag should only transmit signals to the interrogator after it receives a request from the interrogator and decodes it correctly.

2.2.1 Request format

The general format of the request sent from the interrogator is illustrated in Figure 14.

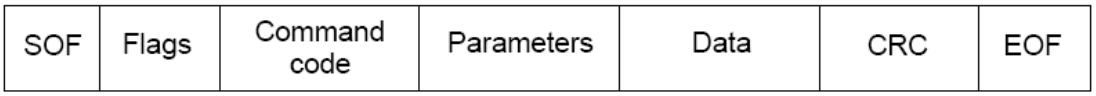


Figure 14. Interrogator request format

All the requests should be padded with a SOF and an EOF.

The 8-bit “Flags” specifies the tag behavior, e.g. single subcarrier or two subcarriers will be used, high data rate or low data rate will be used, any tags or only specific tags will execute the request. It also indicates whether corresponding fields are presented in the request or not, e.g., if the request is set to be in address mode, the unique identifier (UID) of the tag shall be included.

The 8-bit command code and the corresponding commands are as listed in Table 2.

Table 2. Command codes

Command code	Type	Function
‘01’	Mandatory	Inventory
‘02’	Mandatory	Stay quiet
‘03’-‘1F’	Mandatory	RFU
‘20’	Optional	Read single block
‘21’	Optional	Write single block
‘22’	Optional	Lock block
‘23’	Optional	Read multiple blocks
‘24’	Optional	Write multiple blocks
‘25’	Optional	Select
‘26’	Optional	Reset to ready
‘27’	Optional	Write AFI
‘28’	Optional	Lock AFI
‘29’	Optional	Write DSFID
‘2A’	Optional	Lock DSFID
‘2B’	Optional	Get system information
‘2C’	Optional	Get multiple block security status
‘2D’-‘9F’	Optional	RFU
‘A0’-‘DF’	Custom	IC Mfg dependent
‘E0’-‘FF’	Proprietary	IC Mfg dependent

2.2.2 Response format

The general format of the tag response is as illustrated in Figure 15.

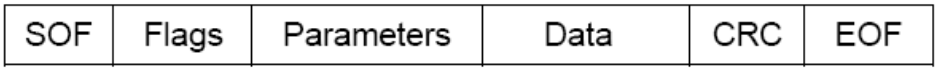


Figure 15. Tag response format

All the responses should be padded with a SOF and an EOF.

The 8-bit “Flags” indicates how the request has been proceeded, e.g., if an error occurs. It also indicates whether corresponding fields are presented in the response or not.

3.0 DEVELOPMENT OF ISO 18000-3 MODE 1 /ISO 15693 CONFORMANCE TEST SYSTEM

The ISO 18000-3 Mode 1/ISO 15693 conformance test platform is implemented with two parts to perform two-stage data acquisition and data analysis.

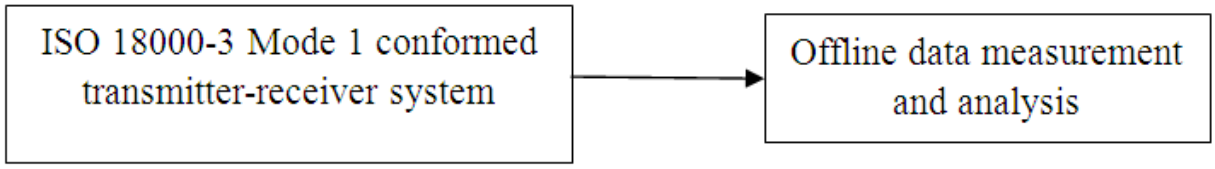


Figure 16. Architecture of the conformance test platform

3.1 STANDARD REALIZATION – THE DEVELOPMENT OF AN ISO 18000-3 MODE 1 CONFORMED READER

To implement the ISO/IEC 18000-3 Mode 1 conformance test platform, the first step is to develop an ISO/IEC 18000-3 Mode 1 conformed transmitter-receiver system. This system is also used to collect the data needed to be tested for conformance.

In this design, the ISO/IEC 18000-3 Mode 1 conformed reader is implemented with National Instruments LabVIEW 8.5 with LabVIEW FPGA module. It consists of an NI PCI-5640R IF Transceiver, RF front end (including NI 5610 upconverter and NI 5600 downconverter)

and host-based controlling and Graphic User Interface (GUI). The hardware structure of the system is as shown in Figure 17.

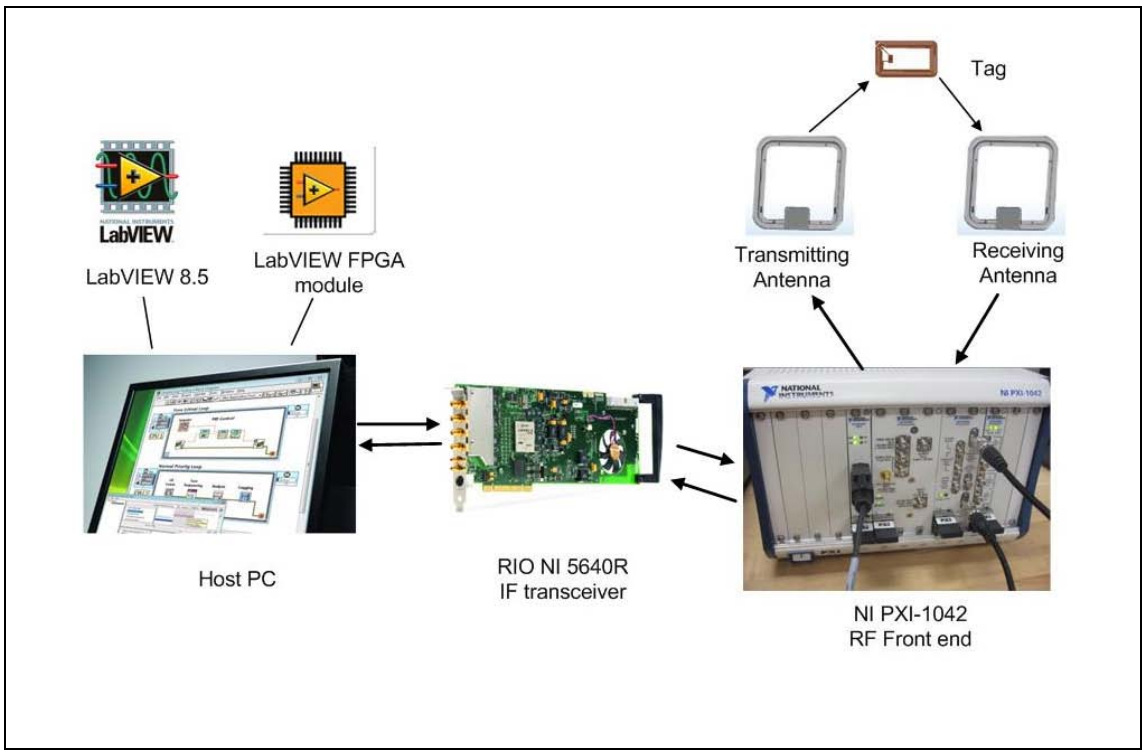


Figure 17. ISO 18000-3 Mode1 conformed transmitter-receiver system hardware structure

The development and configuration of each of the parts will be discussed in the following sections.

3.1.1 The RF Front End

The RF front end consists of two main parts. The NI PXI-5610 RF Upconverter and the NI PXI-5600 RF Downconverter. The NI PXI-5610 RF Upconverter is used to transfer the intermediate frequency(IF) to high frequency (HF (13.56MHz)), and the NI PXI-5600 RF Downconverter is used to transfer HF to the IF.

Both the RF upconverter and the RF downconverter are configured on the host VI. Virtual Instruments (VIs) are LabVIEW programs that imitate the physical instruments.

3.1.1.1 NI-5610 Upconverter

The block diagram of the RF upconverter is as shown in Figure 18.

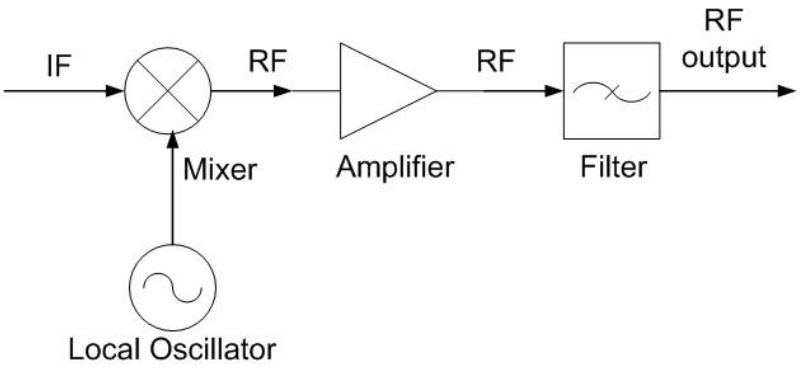


Figure 18. Upconverter architecture

The RF upconverter configuration block diagram is as shown in Figure 19.

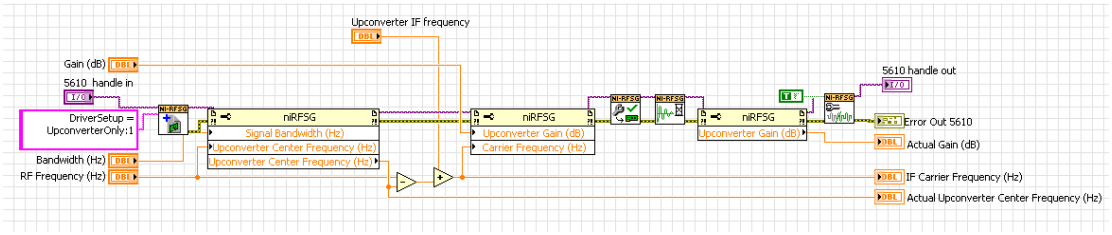


Figure 19. NI5610 upconverter only mode

The main modules are described as following:

(1) niRFSG Initialize With Options.vi

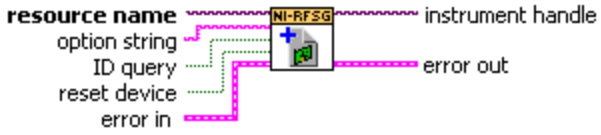


Figure 20. niRFSG Initialize With Options VI interface

This VI is used to open a session to NI 5610, and returns a value for the instrument handle parameter that is used to identify the instrument in all subsequent NI-RFSG VIs.

(2) Property nodes

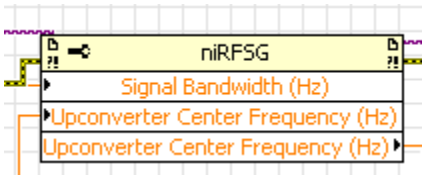


Figure 21. Property nodes

They are used to set the NI-RFSG properties. The desired frequency, the signal bandwidth, the IF frequency at which the arbitration must generate the input signal to the upconverter, and the gain of the upconverter are configured using property nodes.

(3) niRFSG Commit.vi

Figure 22. niRFSG Commit.vi interface

This VI is used to program the NI 5610 with the correct settings. The configured values are transferred to the hardware when calling this VI.

(4) niRFSG Wait Until Settled VI

Figure 23. niRFSG Wait Until Settled.vi interface

This VI is used to wait for the upconverter to settle at the configured values.

(5) niRFSG Configure Output Enabled VI

Figure 24. niRFSG Configure Output Enabled.vi interface

This VI is used to enable the signal output.

3.1.1.2 NI-5600 downconverter

The architecture of the downconverter is as shown in Figure 25.

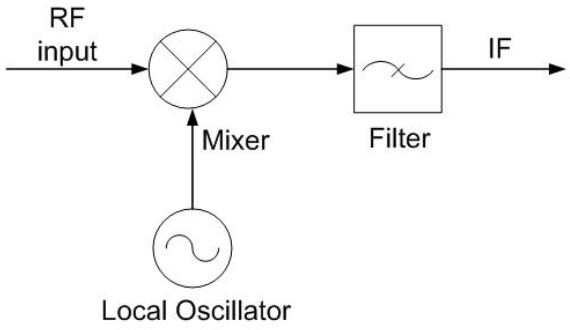


Figure 25. Downconverter Architecture

The RF downconverter configuration block diagram is as shown in Figure 26.

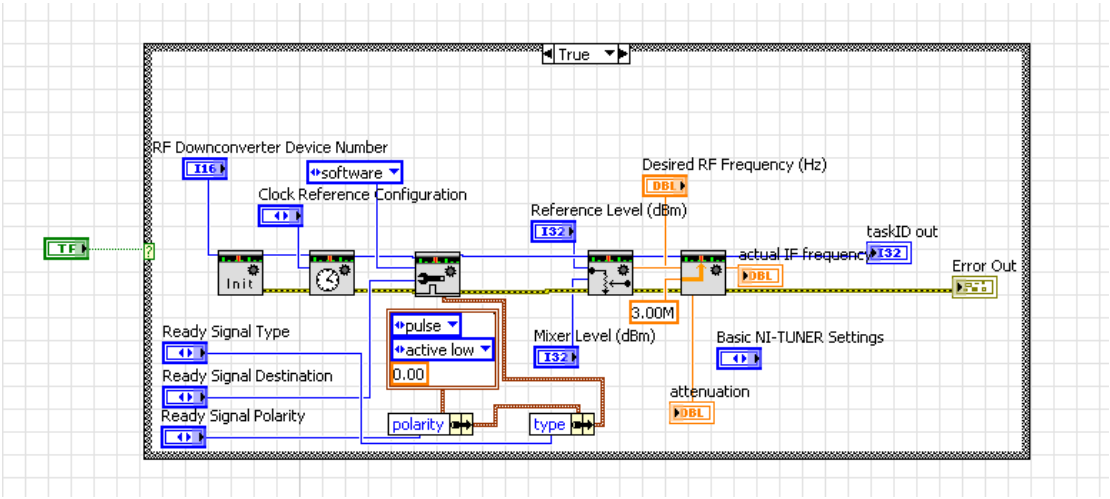


Figure 26. NI-5600 downconverter configuration block diagram

The main modules are described as follows:

(1) niTuner Initialize.vi

Figure 27. niTuner Initialize.vi interface

This VI is used to initialize the PXI-5600 downconverter by loading the calibration memory, clearing the internal registers, and setting the registers to the defaults.

(2) niTuner Config Reference Clock.vi

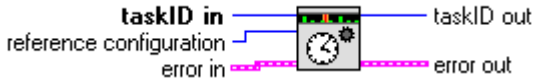


Figure 28. niTuner Config Reference Clock.vi interface

This VI is used to configure the reference clock source for the downconverter.

(3) niTuner Config Scan Advance.vi

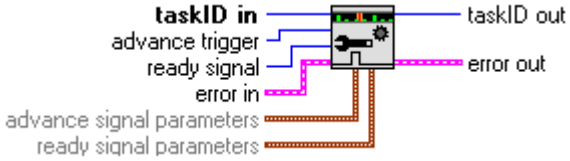


Figure 29. niTuner Config Scan Advance.vi interface

This VI is used to configure the scan advance trigger input and the ready signal output.

(3) niTuner Set Attenuation.vi

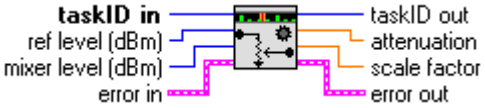


Figure 30. niTuner Set Attenuation.vi interface

This VI is used to set the PXI-5600 internal attenuators based on the reference level and mixer level settings.

(4) niTuner Set Freq(f).vi

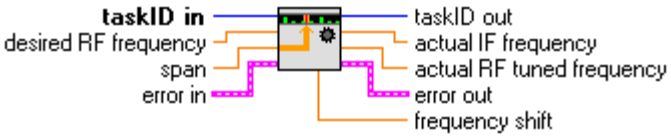


Figure 31. niTuner Set Freq(f).vi interface

This VI is used to set a single center frequency (13.56MHz) in the scan list and immediately begins to settle on this frequency.

3.1.2 IF Transceiver

3.1.2.1 Onboard Signal Processing (OSP) on NI 5640R

An IF transceiver is configured with LabVIEW FPGA National Instruments PCI-5640R taking advantage of the onboard signal processing and to provide the real-time communication between the reader and the tags.

The NI PCI-5640R is a cost-effective IF Transceiver with power and flexibility that makes it ideally suited for developing systems involving software defined radio and other communications applications. The PCI-bus board installs into a desktop PC and is fully programmable with intuitive LabVIEW graphical programming. It offers multiple options for preparing signals for transmission and processing received signals. An on-board Xilinx® Virtex-II Pro FPGA is utilized for in-line processing and use host-based processing by streaming signals to and from the host PC.

The key features [13] of the NI 5640R are

(1) 250 kHz to FM analog input and output frequency range

(2) Dual synchronized input channels, each has up to 20-MHz real-time bandwidth, 14-bit analog to digital converters, and built-in digital downconversion.

(3) Dual synchronized output channels, each has up to 20-MHz real-time bandwidth, 14-bits digital to analog converters, and built-in digital upconversion

(4) Inline and host-based options for processing using simplified graphical programming with LabVIEW

Hardware:

The analog front end of the PCI-5640R offers two IF inputs (AI0 and AI1 ports for receivers) and two IF outputs (AO0 and AO1 for transmitters). In the current design, two of the ports are used. The IF input AI0 is connected to the output of the NI 5600 downconverter to receive the IF signal from the RF front end, and the IF output AO0 is connected to the input of the NI 5610 upconverter to transmit the IF signal to the RF front end. A/D and D/A devices of PCI-5640R converters facilitate those channels and include built-in digital upconverter and downconverter that off-load computational requirements by allowing processing to occur at baseband. Signal samples are processed and prepared for transmission with the on-board Xilinx® Virtex-II Pro FPGA. The PCI-bus board also contains four DMA channels, and two of them are used to stream signal samples to and from the host memory for host-based processing.

Software:

The PCI-5640R offers different programming alternatives tailored for host-based or FPGA-based processing. In the current design, both kinds of processing are used. For host-based processing, the NI LabVIEW is used to configure and control the input and output channels to enable streaming data to and from host memory. For FPGA-based processing, the LabVIEW FPGA module is used to program the on-board FPGA for in-line processing with intuitive LabVIEW graphical programming languages.

The structure of the system is as shown in Figure 32.

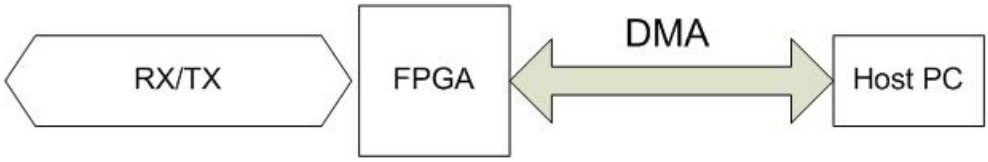


Figure 32. Software structure

The NI PCI-5640R is a reconfigurable Input/Output (RIO) device. Unlike the traditional IF digitizer/source devices which uses a fixed core with predetermined functionality, the NI PCI-5640R is based on a reconfigurable FPGA core surrounded by fixed resources. Figure 33 illustrates the architecture of the IF transceiver using the FPGA for this application.

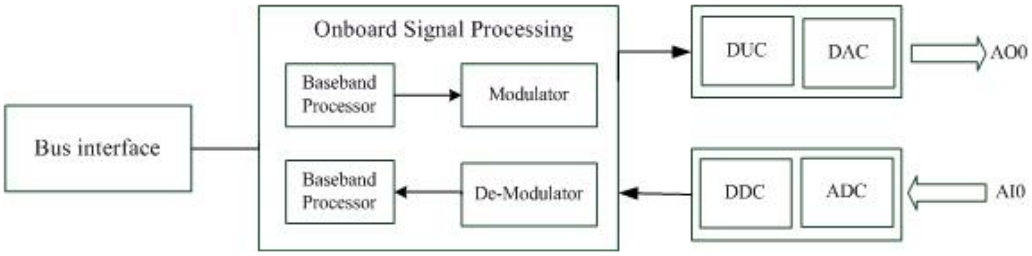


Figure 33. Architecture of IF transceiver

AO0 and AI0 are used for signal channel transmitting and receiving, respectively. The Xilinx Virtex II Pro FPGA is used on the NI PCI-5640R. The behavior of the FPGA core is configured by using the LabVIEW FPGA module to closely achieve the requirements of the system. The logic and digital signal processing (DSP) are embedded in the FPGA of the RIO device. For example, on the receiver side, the demodulation and the baseband signal decoding are done with the FPGA. The behavior of the module can be implemented as a VI and can be synthesized into a form that can be downloaded to the FPGA on the RIO device. The bus interface provides software access to the device. Each of the fixed I/O resources (including analog-to-digital converters (ADCs), digital-to-analog converters (DACs), digital I/O (DIO)

lines, and other input/output resources) and the bus interface consume only a small portion of the FPGA logic. The remaining FPGA logic can be used for high-level functional design.

The design of the transceiver includes two main components:

(1) An FPGA VI, which is implemented to determine the functionality of the hardware, and shall be downloaded to the FPGA target (NI PCI-5640R).

(2) A host VI, which runs on the host PC, and communicates with the FPGA VI using the FPGA Interface VIs. This host VI is used to control and monitor the behavior of the FPGA VI and also to display the captured waveforms and the computational results on the front panel.

3.1.2.2 Data Transmission

On the transmission side, the ISO/IEC 18000-3 mode 1 commands are assembled and sent out using 1 out of 4 or 1 out of 256 PPM data coding and ASK modulation.

The flow chart of the ISO/IEC 18000-3 mode 1 conformed transmitter is as shown in Figure 34.

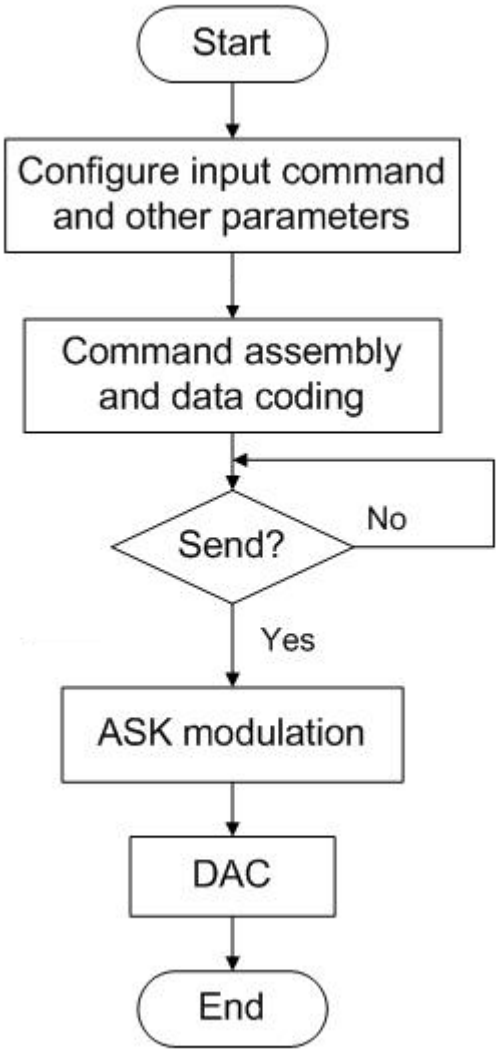


Figure 34. ISO/IEC 18000-3 mode 1 conformed transmitter flow chart

All of the commands defined in the standard (as listed in Table 2) are realized. The user can select one of the commands on the front panel of the host VI, the default pre-stored values of the parameters will be loaded to a editable table on the front panel (Figure 35). The values of the command parameters then can be edited and customized, and the command bit-stream will be generated according to the customized parameters when the host VI runs.

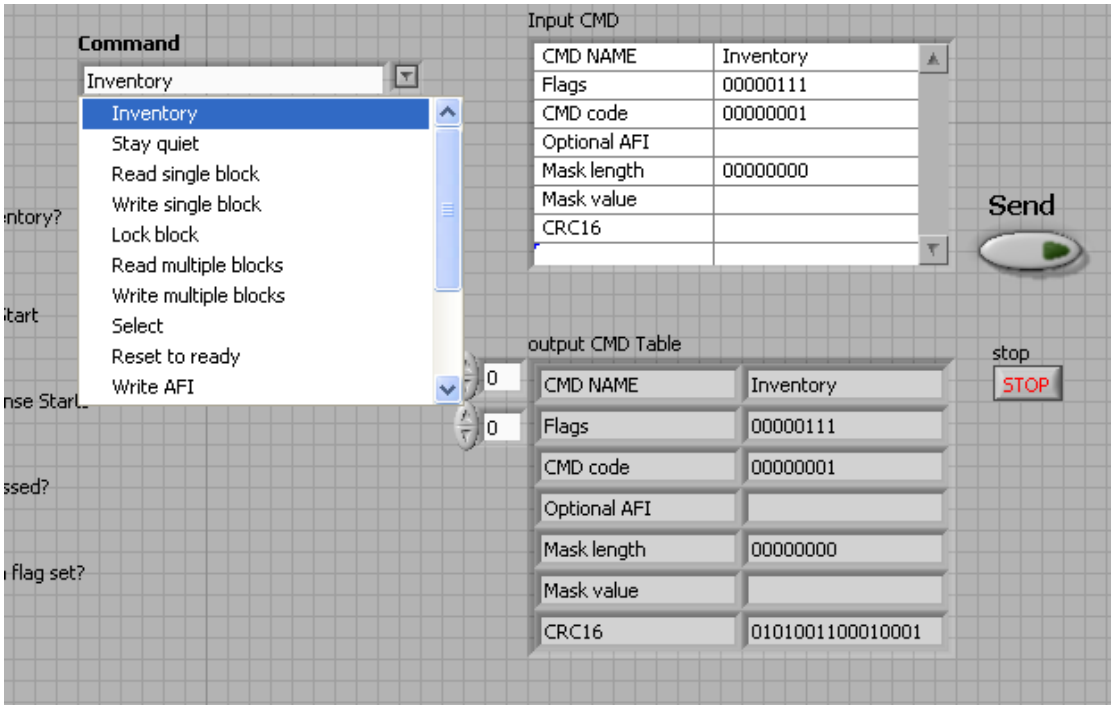


Figure 35. Command load and customize on the control panel of the host VI

3.1.2.2.1 Data coding

After the input command table is configured, the command bit-stream will be encoded using 1 out of 4 PPM or 1 out of 256 PPM by the data encoding VIs designed on the host PC. The user can determine which of the two data encoding modes is to be used by clicking the button on the front panel. Also, the generated raw bit-stream pattern will be assembled with the Start of Frame (SOF) and End of Frame (EOF) defined in the protocol using the same data encoding mode as the command bit-stream uses.

3.1.2.2.2 Direct memory access (DMA)

LabVIEW 8.5 and the later versions can support DMA.

A DMA FIFO “Bits from Host” is used on the FPGA. As the DMA FIFO on the FPGA is a 32-bit wide channel, to be more efficient, the bit-stream is packed per 32 bits on the host.

When the user presses the “send” button on the control panel, the assembled command bit-stream shall then be download to the FPGA via the DMA channels. The DMA transfer Loop, from host to FPGA, is as shown in Figure 36.

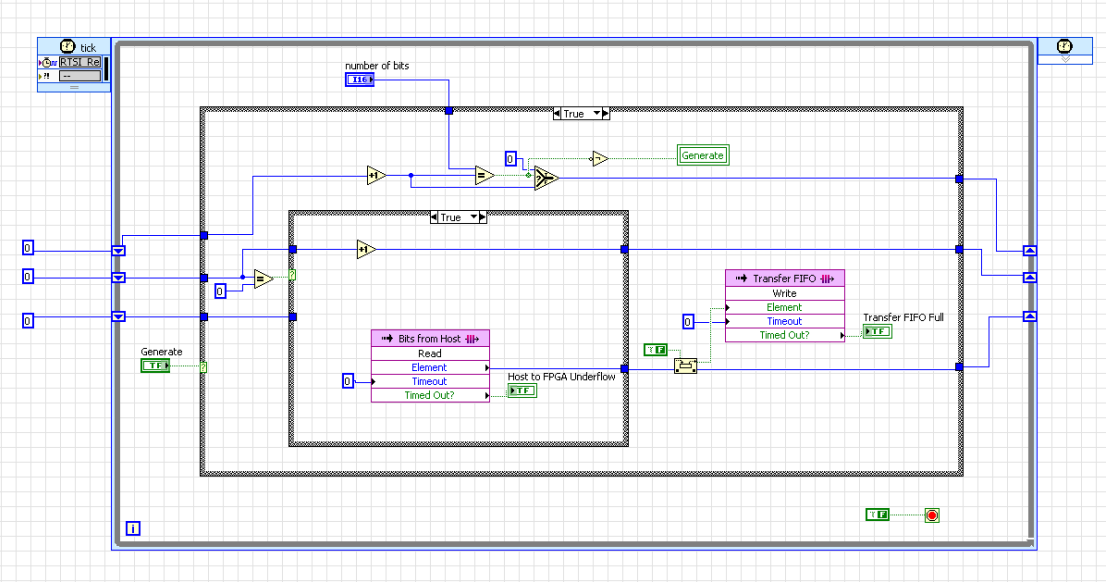


Figure 36. DMA transfer loop on FPGA VI

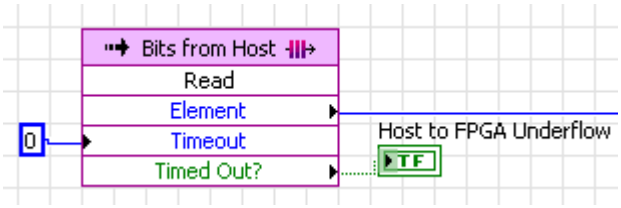


Figure 37. DMA FIFO Read

The “Bits from Host” Read method is used to read the packed input values from the DMA FIFO. The number of bits to be read is calculated on the host PC and is transferred to the FPGA through the FPGA interface “Read/ Write Control”. Thus, the number of samples that are read by the DMA FIFO Read shall be equal to the number of bits of the packed command message.

3.1.2.2.3 ASK modulation and DAC

The FPGA will perform the ASK modulation for the data stream in a generation loop for DAC (Figure 38).

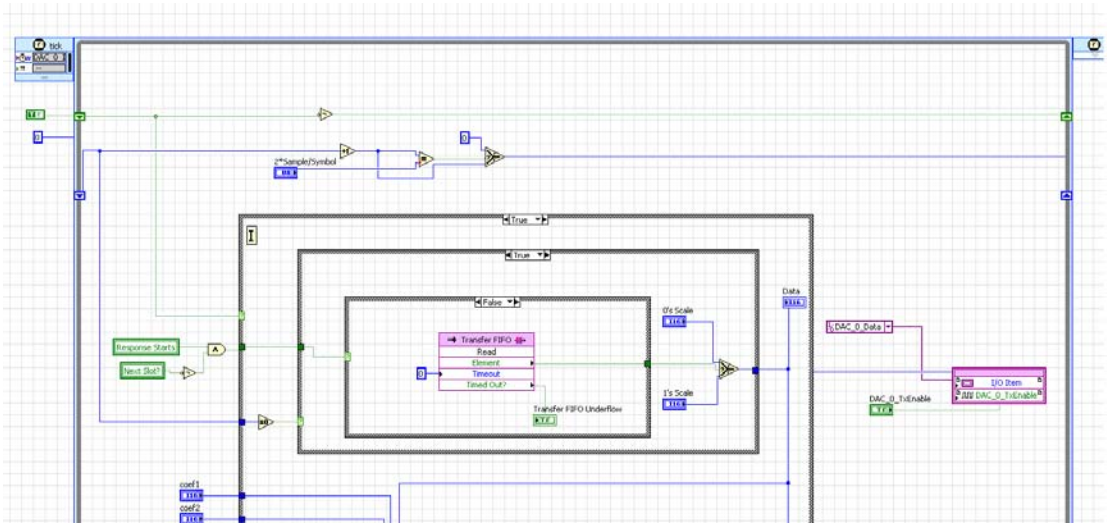


Figure 38. Generation loop for DAC on FPGA VI

In LabVIEW, I/Q data [12] are used to represent the signal. I/Q data are a translation of amplitude and phase data from a polar coordinate system to a cartesian (X,Y) coordinate system.

Assume the magnitude of a signal at time t is M(t), and the phase of the signal at time t is φ(t), then

$I(t) = M(t) \cos(\varphi(t))$, $Q(t) = M(t) \sin(\varphi(t))$.

The block diagram of ASK modulation onboard is as shown in Figure 39.

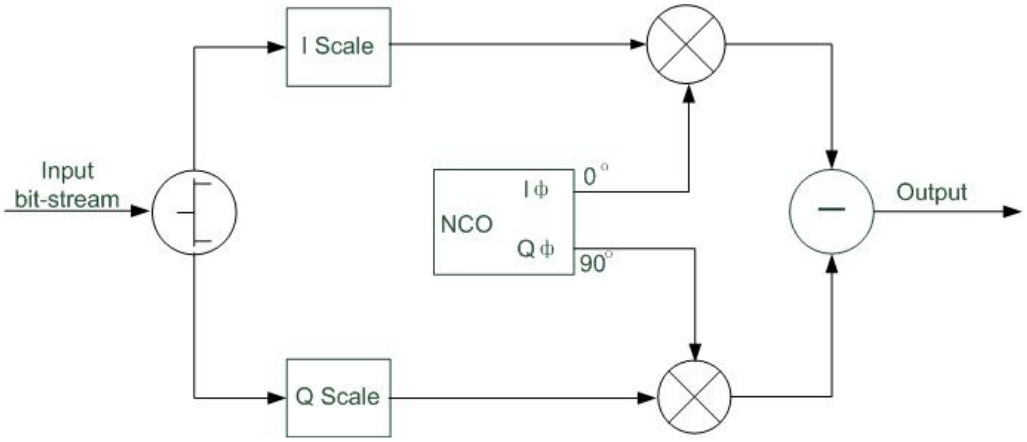


Figure 39. ASK modulation block diagram

When the binary symbol read out from the Transfer FIFO is logic ‘1’, then the magnitude of the multiplier is set to be the value of “1’s scale”, which can be considered as the Pre-Filter I Gain. When the binary symbol read out from the Transfer FIFO is logic ‘0’, then the magnitude of the multiplier is set to be the value of “0’s scale”, which is calculated according to the value of “1’s scale” and the modulation index, on the host PC.

The ASK modulated I/Q data shall then be sent to the DAC. In order to alternately write I and Q data to DAC_0, a Boolean variable is used to control which data are to be written. When the Boolean variable is true, the I value will be written to the DAC_0, and when the Boolean variable is false, the Q value will be written to the DAC_0. The Boolean variable is converted every clock cycle.

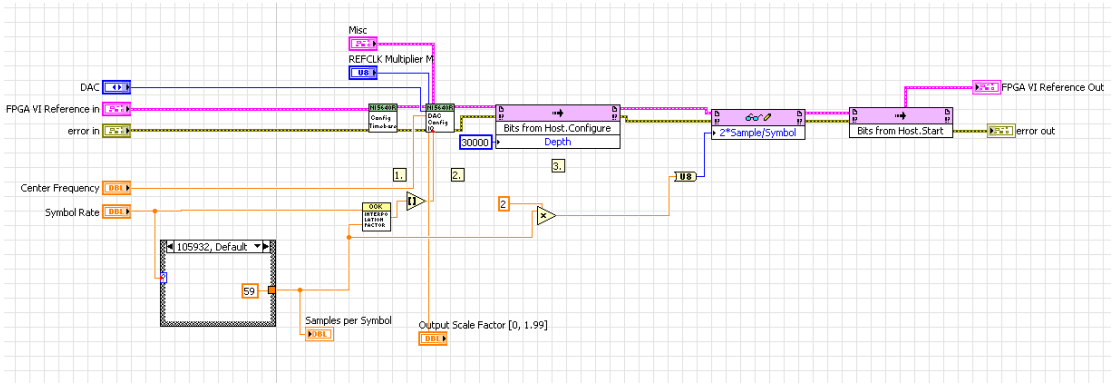
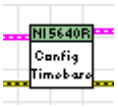


Figure 40. ASK Configuration

The IF RIO for transmission using ASK modulation and DAC is configured by two main VIs.

(1) ni5640R Configure Timebase.vi



This VI is used to configure the RTSI clock.

(2) Ni5640R DAC Configure for Quadrature Mode.vi

This VI is used to configure the DAC for Quadrature mode and also configures the interpolation factor for the given symbol rate.

3.1.2.2.4 Gibbs Phenomenon

The designed transmitter was complied and tested. However, from the waveform of the envelope of the signals captured by the receiver (the design of the receiver is discussed in the later section), the overshoots can always be observed at the rising edge or falling edge of the waveform (Figure 41). This is classic Gibbs phenomenon [8][9].

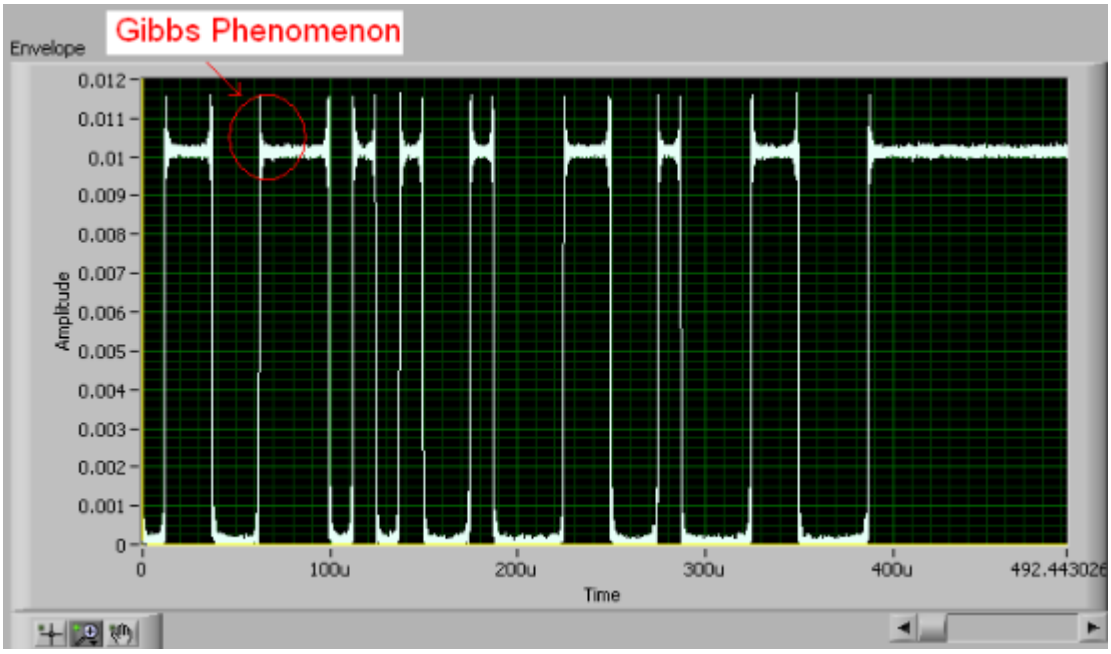


Figure 41. Gibbs phenomenon

The Gibbs phenomenon occurs here because of the 4x-interpolating Finite Impulse Response (FIR) filter in the AD9857 (the DAC). The FIR filter can be considered as an ideal filter, which passes the spectrum unchanged up to about 0.4 times the input sample rate (the I/Q data rate) and then the response rolls off abruptly. However, the signal that is fed into the DAC is the square wave, whose spectrum consists of an infinite sequence of harmonics, namely, a signal with theoretically unlimited bandwidth is fed into the DAC. However, the FIR filter in the DAC results in a spectrum with harmonics up to about 0.4 times the sample rate and then suddenly nothing above that. Whenever a signal has a spectrum with significant power at one frequency and an absence of power nearby, the time-domain waveform will have some sort of ringing.

The overshoot of the waveform cannot be ignored, because it would always exceed the tolerance of the maximum oscillation of the ASK modulated waveform as defined in the ISO/IEC 18000-3 mode 1 standard.

The solution is to limit the spectrum of the signal to 0.4 times the sample rate by filtering it before sending it to the DAC.

For this transmitter system, it is also important to achieve the filter with linear phase. Thus, an eighth-order FIR low-pass filter that has a symmetric impulse response

$$h[n] = h[8-n], \quad 0 \leq n \leq 8$$

is designed.

The design of the FIR filter utilized the NI Digital Filter Design (DFD) toolkit. The magnitude and the phase of the FIR filter are shown in Figure 42.

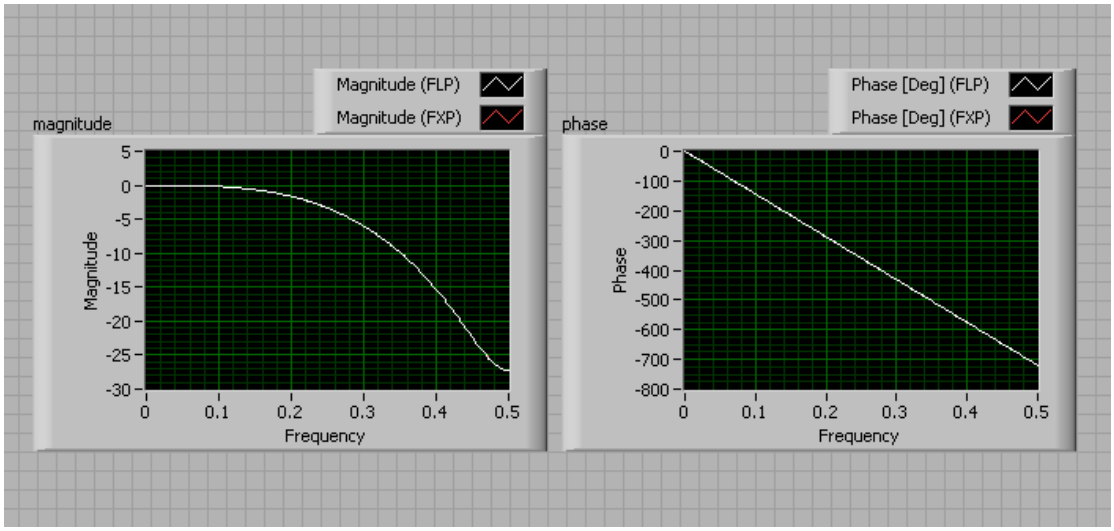


Figure 42. FIR low-pass filter characteristics

The structure of the nine-tap FIR filter [3] is as shown in Figure 43. The designed FIR filter on LabVIEW FPGA is as shown in Figure 44.

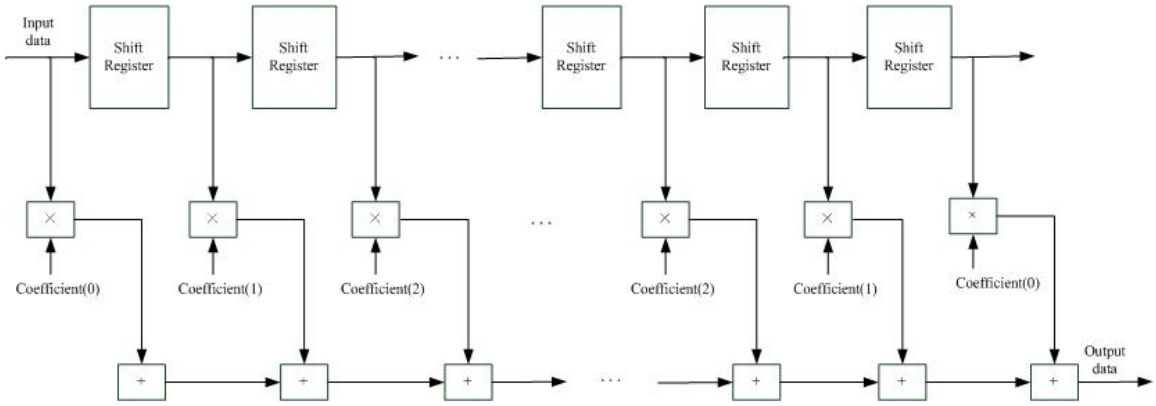


Figure 43. 9-tap FIR filter block diagram

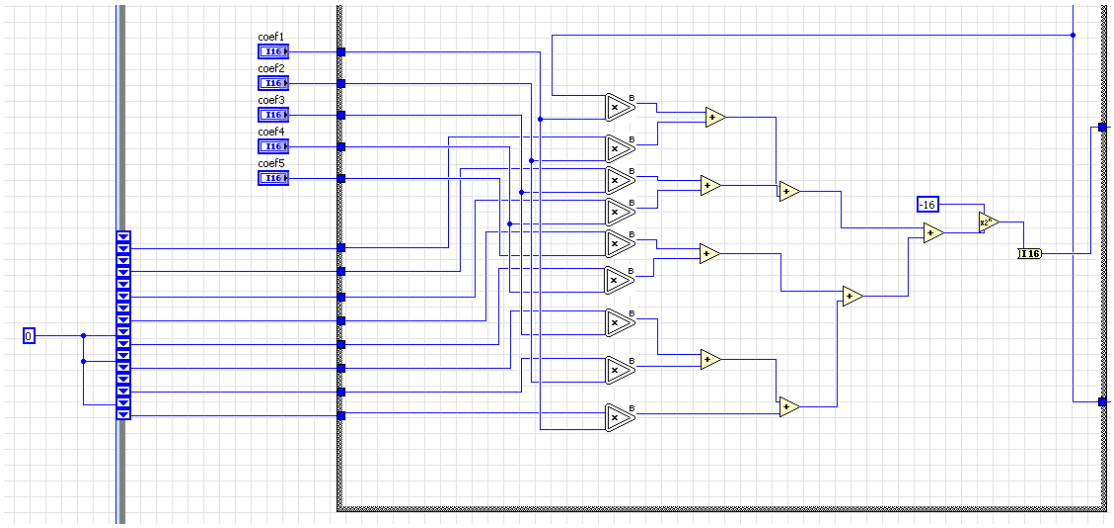


Figure 44. FIR filter on FPGA VI to avoid Gibbs Phenomenon

As shown in the previous figures, the structure of the FIR filter includes a set of shift registers. In each tap of the filter, the shift register is multiplied by a corresponding coefficient. The results of all the multipliers should then be summed up to get the output data. In order to achieve linear phase of the filter, the coefficients must be symmetric about the center tap.

After using the eighth-order FIR filter, the waveform of the transmitted signal is smoothed, and a typical waveform is as shown in Figure 45.

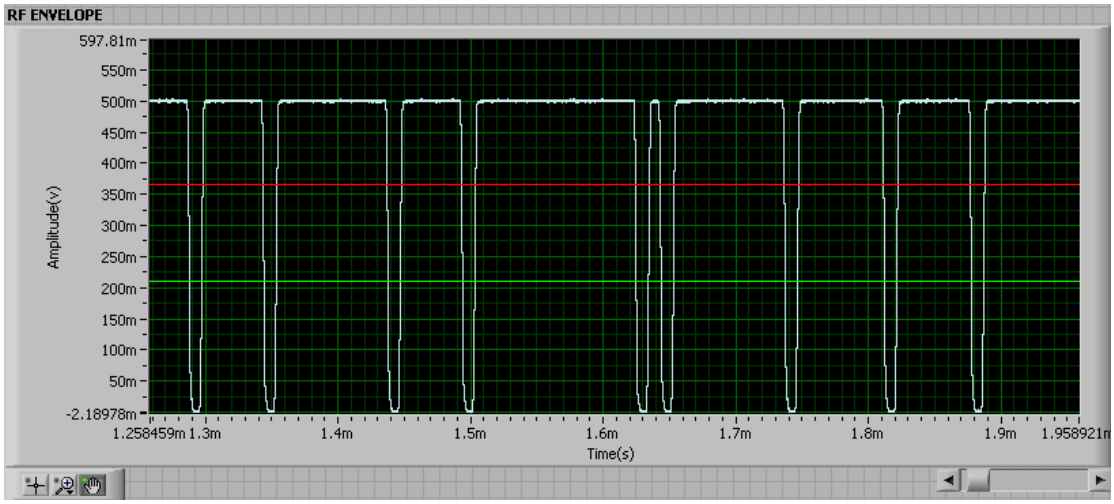


Figure 45. Smoothed waveform after using the FIR low-pass filter

3.1.2.3 Data Acquisition

On the receiver side, when the "Acquire" signal is high, the data acquisition starts. The flow chart of the receiver is as shown in Figure 46.

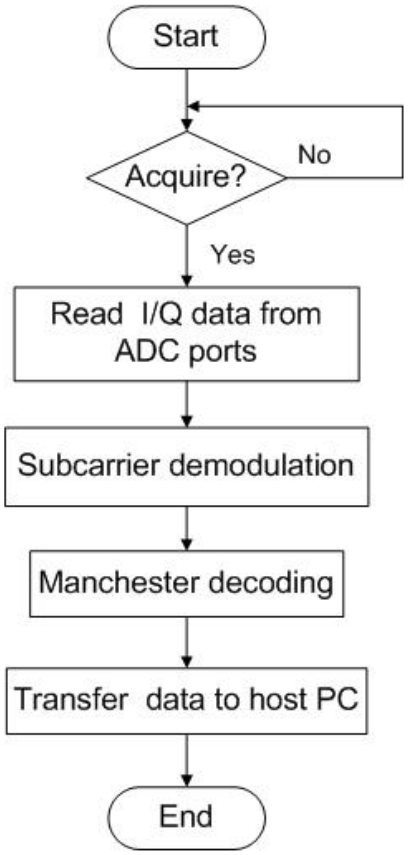


Figure 46. ISO/IEC 18000-3 mode 1 conformed receiver flow chart

The I and Q samples are read using the FPGA I/O node (Figure 47).

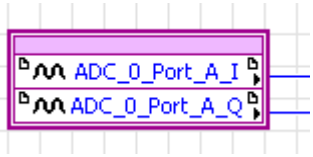


Figure 47. FPGA I/Q node

The two 16-bit values are then joined into an unsigned 32-bit value, and the value is written to a DMA FIFO " to host". The acquired I and Q samples are also processed by cross edge detection and decoding. When processing the inventory command, if the number of slots

flag is set to 16, sending the pulse to switch to the next slot should wait until the End of Frame (EOF) of the current tag response is detected.

The decoded array will transfer to the host VI, and the decoded tag response is displayed on the host VI front panel according to the corresponding tag response format to the command that was sent. An example for the decoded tag response display to the inventory command is as shown in Figure 48.

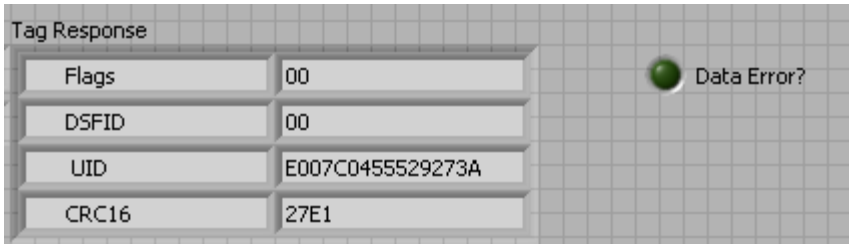


Figure 48. Decoded tag response to inventory command

The power spectrum and the constellation as well as the I/Q waveform are also displayed on the front panel of the host VI by virtual oscilloscopes.

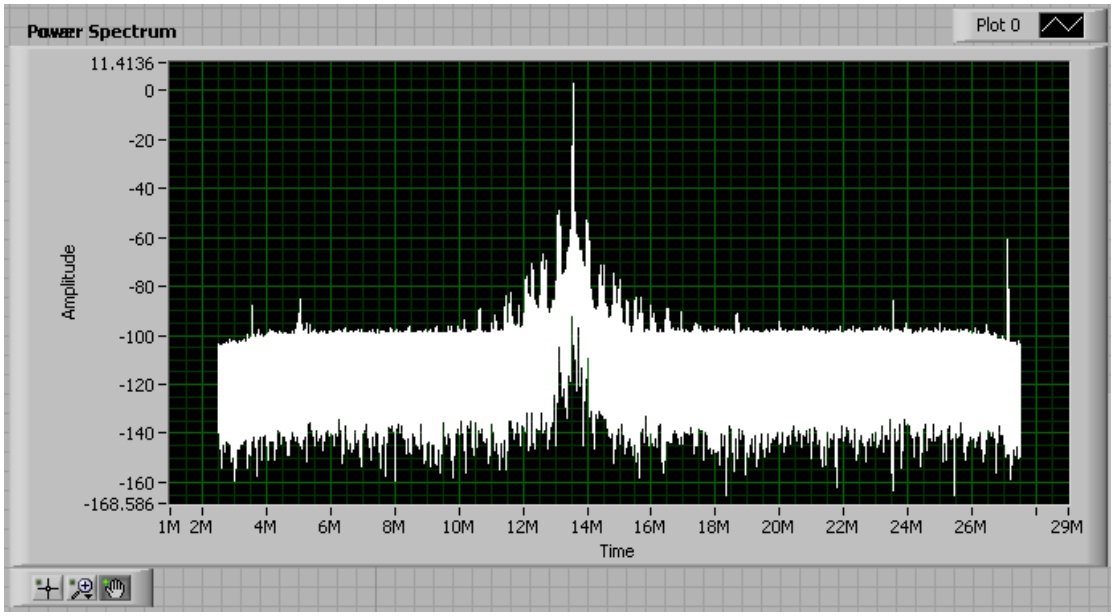


Figure 49. power spectrum

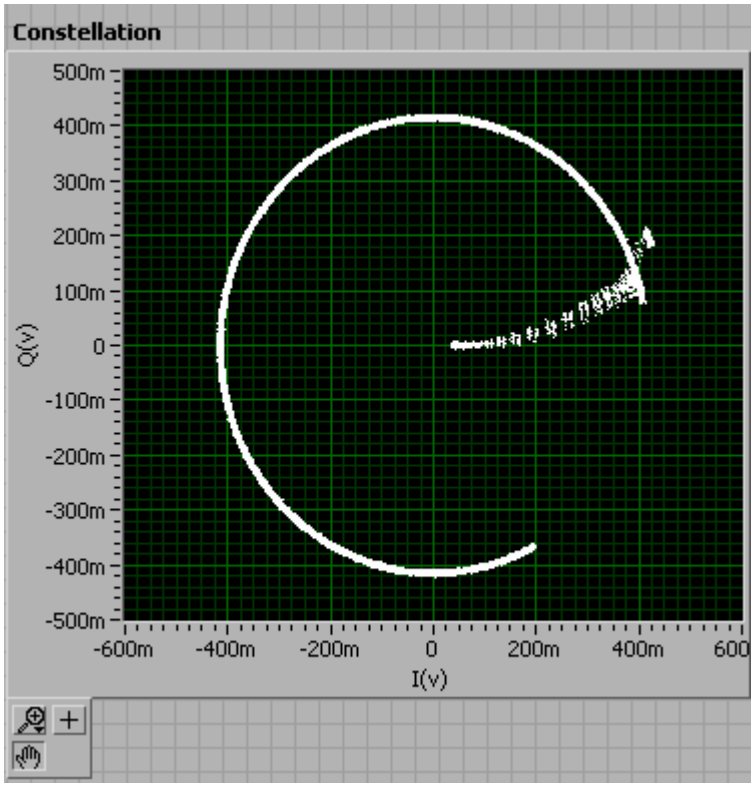


Figure 50. Constellation

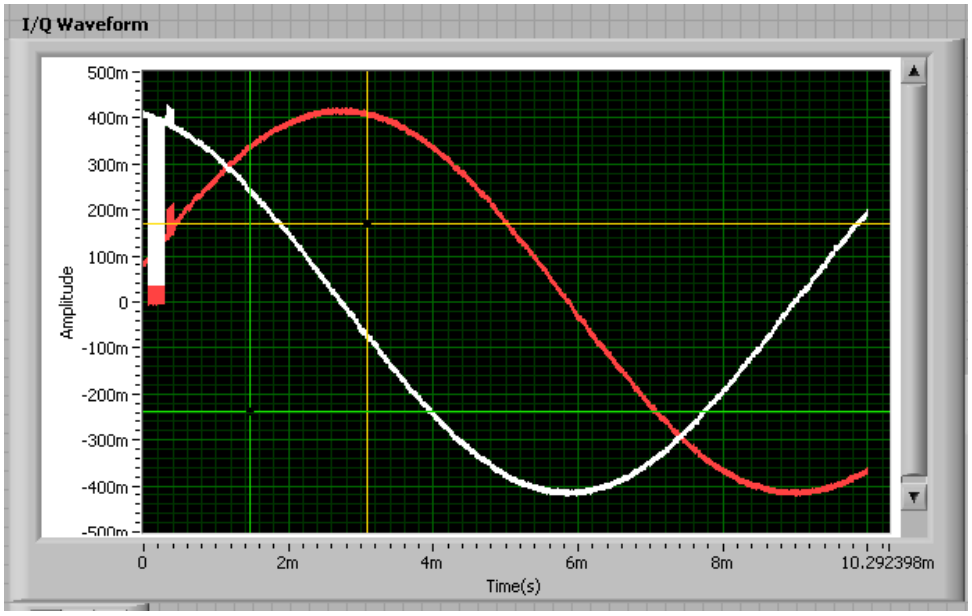


Figure 51. I/Q waveform

Also, for further testing, the waveform data that are captured can be saved to a LabVIEW waveform file to the disk, and this file can be loaded from the disk to perform off-line data measurement and testing.

The FPGA resources utilization of the entire system is summarized in Table 3.

Table 3. Device utilization summary

	Used	Available	Utilization
Number of BUFGMUXs	7	16	43%
Number of External IOBs	403	556	72%
Number of LOCed IOBs	403	403	100%
Number of MULT18X18s	11	136	8%
Number of RAMB16s	49	136	36%
Number of SLICEs	9271	13696	67%

3.2 OFFLINE DATA MEASUREMENT AND CONFORMANCE TESTING

Another part of the conformance test platform is the so-called offline data measurement and conformance test VI. This VI works on the host PC, and the input waveform data that is to tested should be loaded from the disk, which is captured and save by the transceiver system discussed in the previous section.

3.2.1 Goal and Methodology

The goal of this off-line conformance test VI is to measure the envelope waveform of the command sent by the reader and the envelope waveform of the tag response. In addition, it is necessary to check if they are compliant with the parameters defined in the ISO/IEC 15693-2, the communication interface between the reader and the tag, the timing specifications, and the data validation. The tolerance of some parameters can also be set to perform a customized testing.

3.2.1.1 Reader conformance test

For the reader testing part, the pulse widths of each of the pulses of the command envelope waveform are measured, stored and displayed on the front panel. The format of the Start of Frame (SOF) and End of Frame (EOF) are also checked and displayed by pass/fail on the front panel. Both the 1 out of 4 PPM data encoded waveform and the 1 out of 256 PPM data encoded waveform can be checked.

3.2.1.1.1 Edge detection

Because the commands sent from the reader use ASK modulation, the pulse width can be measured by detecting the rising and fall edges of the envelope waveforms.

The block diagram of the edge detection VI is as shown in Figure 52.

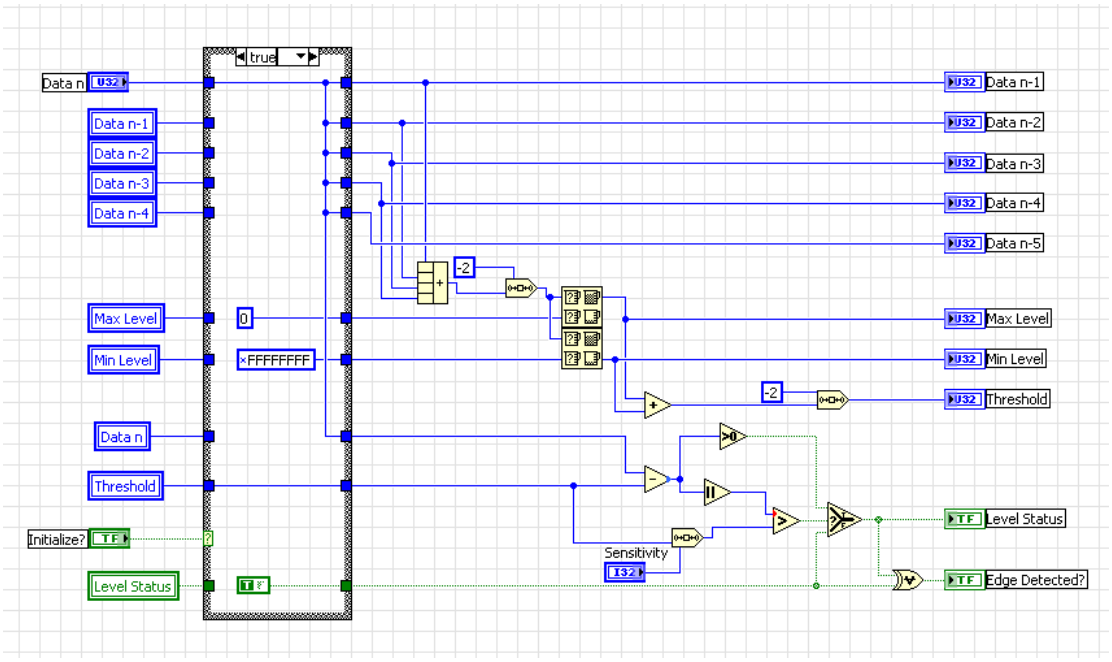


Figure 52. Edge detection block diagram

The method used here to detect the rising and falling edge of the waveform is as follows: In every iteration, the amplitudes of five continuous samples are considered for the calculation. A threshold is chosen to be the approximate average value of the maximum amplitude and the minimum amplitude. The difference between the amplitude of the sample and the threshold is calculated, and if the absolute value of the difference is large enough, then whether the difference (amplitude of the sample – threshold) is negative or positive should be updated as the level status. Once the level status changes, it indicates that an edge is detected.

3.2.1.2 Tag conformance test

For the tag testing part, the SOF, EOF and the data parts are checked with the protocol. As the tag response uses Manchester encoding with single subcarrier modulation or two subcarriers modulation, first, the tag response should be processed by subcarrier demodulation. After the demodulation, the Manchester encoded baseband signal can be recovered, and the demodulated

waveform is displayed by the virtual oscilloscope on the front panel. The Manchester encoded waveform is then checked using a counter with the edge detector module as described above to measure the pulse width and a decoder to decode the data sending by the tag. The decoded array is also be checked by a CRC-16 checker to validate the correctness of the data.

3.2.1.2.1 Subcarrier demodulation

Subcarrier demodulation is required to recover the baseband signal from the subcarrier modulated signal that is obtained after the carrier demodulation in the interrogator.

Methods for subcarrier demodulation [4]:

As the tag single subcarrier modulation is ASK modulation, the demodulation can be realized by either correlation demodulation or non-correlation demodulation.

(1) Correlation demodulation

The block diagram of the correlation demodulation is as shown in Figure 53.

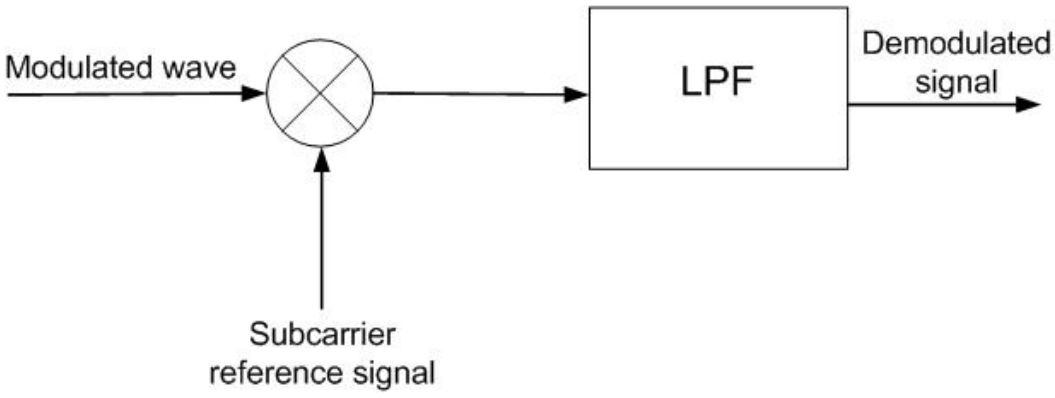


Figure 53. Block diagram of correlation demodulation

When using this method to demodulate, there must be a reference signal in the interrogator, and it must have the same frequency and the same phase as the subcarrier signal of the tag.

In the interrogator, the subcarrier frequencies can be easily generated by dividing the carrier (13.56 MHz) by 28 or 32. However, it is complex to realize the same phase.

(2) Non-correlation demodulation

When ASK modulation is applied, the envelope of the signal is proportional to the baseband signal. Thus, the baseband signals can be recovered by using envelope detection. In this way, it does not require a subcarrier reference signal with the same frequency and the same phase.

The non-correlation demodulation can be implemented by an envelope detector circuit. Another method is to use a retriggerable monostable circuit.

The retriggerable monostable circuit means in a time period, tw, of transient steady-state, the flip-flop can be re-triggered, if a new trigger pulse has been received.

As illustrated in Figure 54, when the flip-flop is triggered by pulse A, the circuit enters a transient state. During the time period tw of transient steady-state, if the flip-flop is triggered again by pulse B in $T_{\triangle}$ ($T_{\triangle} < t_w$), then the transient state timer will be reset from it is triggered by pulse B. So the pulse width of the output signal will become $T_{\triangle} + t_{w.}$

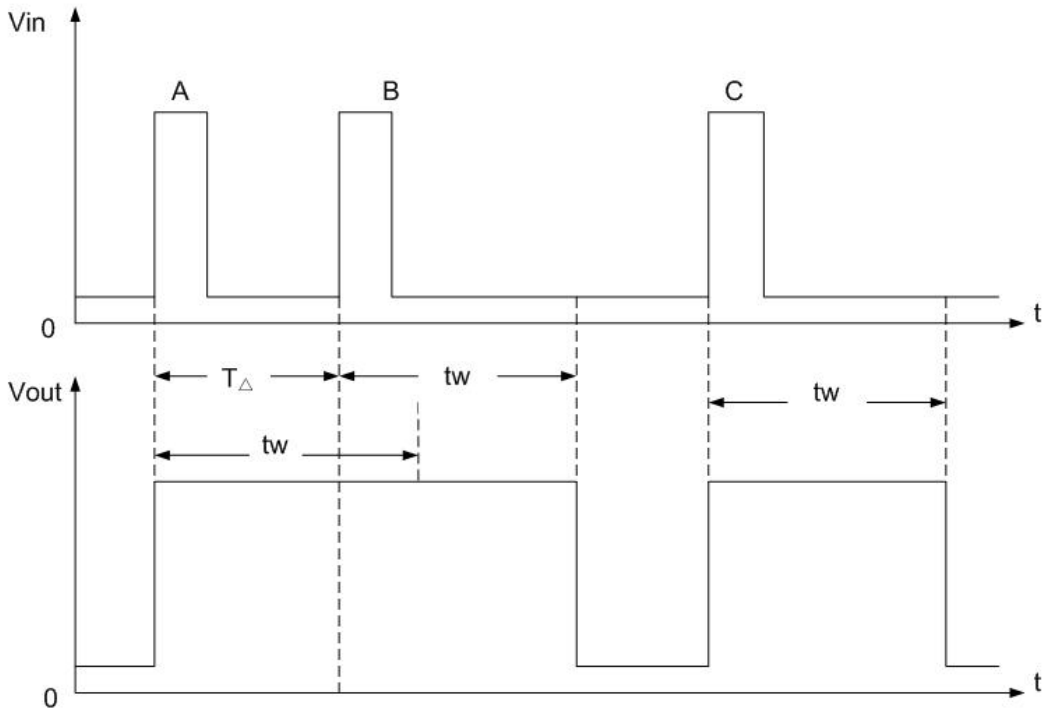


Figure 54. Waveform of retriggerable monostable circuit

In the conformance test platform, the methodology used for the subcarrier demodulation is non-correlation checking. The principle is similar to the description of the retriggerable monostable circuit above. The trigger signal is generated by the edge detection module as described in section 3.2.1.1.1.

For single subcarrier demodulation, set t_w to be somewhat larger than 2.36 us ($32/f_c$). Then the Manchester encoded baseband signal can be recovered.

For two subcarrier demodulation, set t_w to be a value between 2.07 us($28/f_c$) and 2.36 us ($32/f_c$), then the Manchester encoded baseband signal can be recovered.

3.2.1.2.2 Manchester decoding

The NRZ coded data signal can be recovered from the Manchester encoded signal by doing an XOR operation with the Manchester encoded data signal and the data clock signal. In the

platform designed, the Manchester encoded signal is center sampled at 1/4 and 3/4 of a single symbol, then compared the samples to the sampled data clock, and the data can be decoded.

3.3 SOFTWARE SETUP

All the parameters can be setup on the front panel of the host VIs.

3.3.1 ISO 18000-3 mode 1 conformed transmitter receiver system software setup

The software setup for the ISO 18000-3 mode 1 conformed transmitter receiver can be divided into three parts, (1) to setup the RF front end, (2) the IF transmitter, and (3) the IF receiver, respectively.

The RF front end setup on the front panel is as shown in Figure 55.

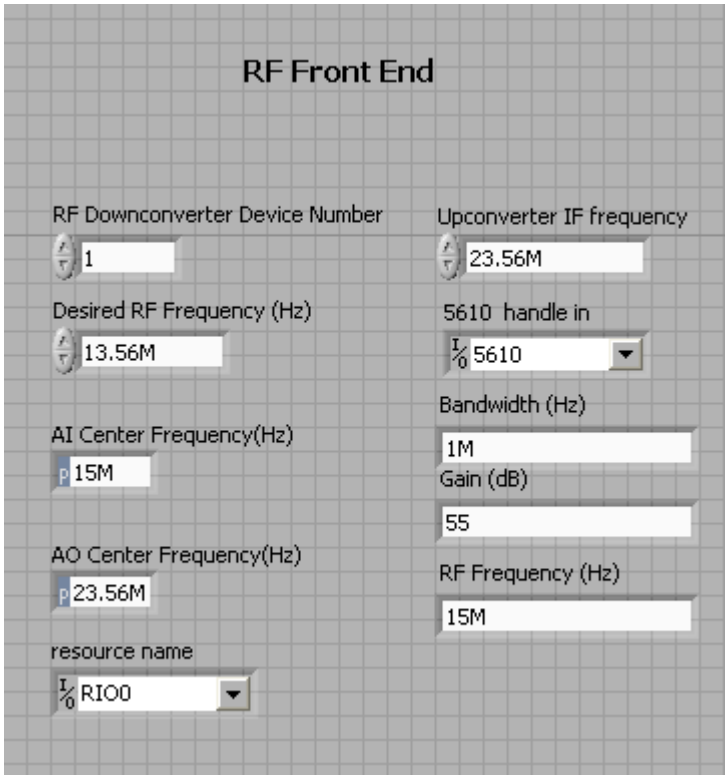


Figure 55. RF front end setups

The RF frequency should be setup for both the upconverter and the down converter. Also the bandwidth and the gain should be set for the upconverter.

The IF transmitter setups on the front panel is as shown in Figure 56.

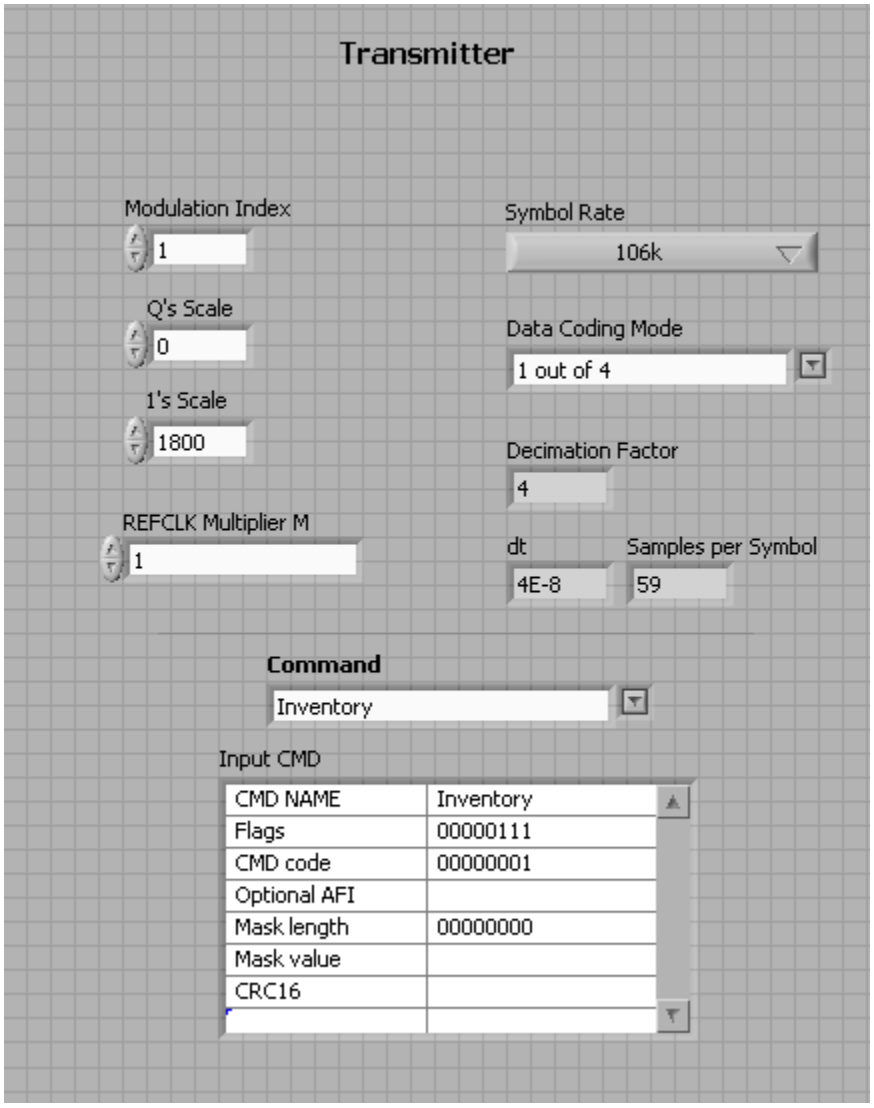


Figure 56. IF transmitter setups

The 1's Scale and the modulation index can be set to perform a customized transmission. Also, 1 out of 4 PPM mode or 1 out of 256 PPM mode can be selected from the Combo box "Data Coding Mode", and the command to be sent can be selected and edited.

The IF receiver setup on the front panel is as shown in Figure 57.

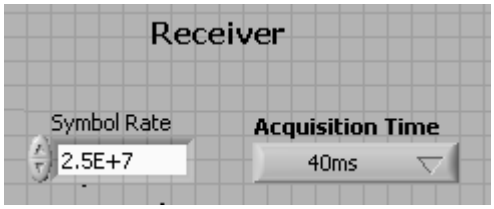


Figure 57. IF receiver setups

For the IF receiver part, only the sampling rate and the acquisition length need to be set.

3.3.2 Offline conformance test VI software setup

The front panel of the offline conformance test VI is as shown in Figure 58.

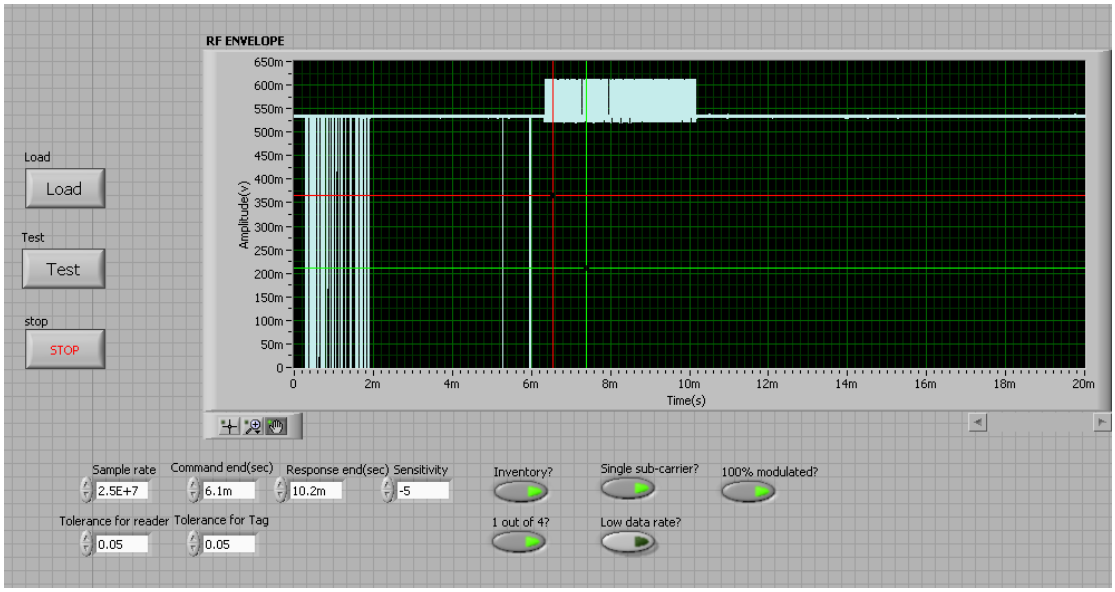


Figure 58. the front panel of the offline conformance test VI

To perform the off-line data measurement and analysis, first run this VI, click the “Load” button to select the waveform file to be tested, and the file will be loaded from the disk. Set the sample rate, the command period, the response period, the data coding mode used, and the tolerances for the reader test and for the tag test.

After setting up all the parameters, press the “Test” button, and the test will be performed automatically.

When the data measurements are done, this will be indicated by the “Done” signal as shown in Figure 59. Press “Stop” to stop running the test.

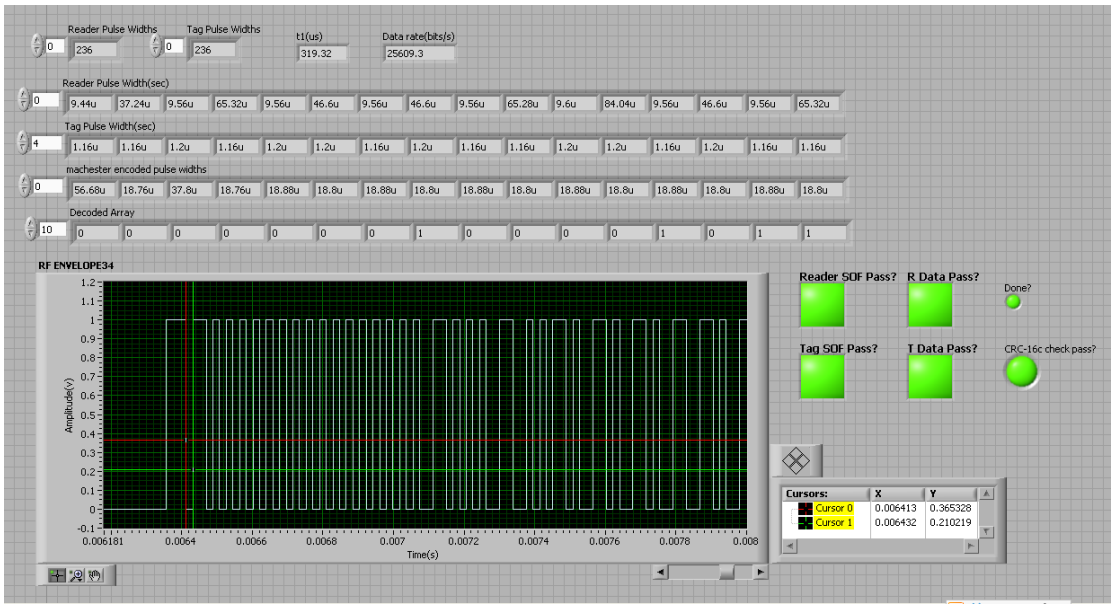


Figure 59. results display on the front panel of the offline conformance test VI

As can be seen in the figure, all the pulse widths of the request data and the response data are measured and shown on the front panel. The Manchester encoded tag response baseband signal is displayed by a virtual oscilloscope. The Manchester decoded tag response is shown, and checked by a CRC 16 checker. The frames of the request and the response, and the data field baseband waveforms of the request and the response are also checked. The results are displayed.

4.0 RESULTS AND DISCUSSION

4.1 TEST RESULT

The testing is focused on the tag conformance. Twelve ISO 18000-3 mode 1 conformed commercial tags were used as the device under tests (DUTs). All tests were successful.

The developed conformance test platform can also be applied for commercial reader tests as long as the request waveform from the reader is captured by the receiver of the test platform.

Tags were tested with all the commands. All the tags could support all the mandatory commands. Corresponding error codes are received, when the optional command is not supported by the tag.

Both the data coding modes (1 out of 4 PPM mode and 1 out of 256 PPM mode) are supported by the tags. And both the low data rate and high data rate are supported.

The tags can support 100% ASK modulation and are also operational for 10% to 30% ASK modulation.

For the offline data measurement part, the tag responses stored can pass the test with a tolerance of 1% when the sample rate of the receiver is 25 MHz.

5.0 CONCLUSION

In this thesis, a reconfigurable software defined ISO 18000-3 mode 1/ ISO 15693 conformance test platform has been developed using LabVIEW 8.5 with LabVIEW FPGA modules.

This conformance test platform includes an online real-time transmitter-receiver system and an offline data measurement and analysis VI.

The online real-time transmitter-receiver system is the complete ISO 18000-3 mode 1/ISO 15693 conformance specification. All the modulation indices, both of the data coding modes, both of the data rates, and all of the commands defined in ISO 15693-2 and ISO 15693-3 are implemented. The user can select and custom all those parameters. Typical interrogator to tag communication sequences are realized.

The key features of the system are:

(1) Software controllable RF front end

(2) Reconfigurable onboard baseband processing with time resolution of 4 us

(3) A host based GUI front panel for parameter control and results display.

The host based offline data measurement and analysis VI is developed for data measurements, and a pass/fail check for the waveforms captured by the real-time transceiver is provided.

This VI is an automatic test VI. The test results can be clearly reviewed on the front panel. Both the reader request and the tag response can be checked by this VI. Request and

response edge detections are realized, the subcarrier demodulation and Manchester decoding are also implemented to check the transmitted data field of the tag response.

Commercial tags have been tested using the conformance test platform developed. The tests were successful.

6.0 FUTURE WORK

First, in this thesis, for the off-line reader test part, the input waveforms that have been tested are obtained from the developed transmitter. Also, this off-line data measurement platform can be applied to ISO 18000-3 mode 1 supported commercial readers. In future work, different commercial readers can be used as device under tests (DUTs), and the validation results can be compared.

Second, as defined in ISO 18000-3 mode 1, when the inventory is without mask and the number of slots is selected to be 16, the capacity of tag responses without collision is only 16. The collision waveform is captured by the receiver developed in this thesis as shown in Figure 60.

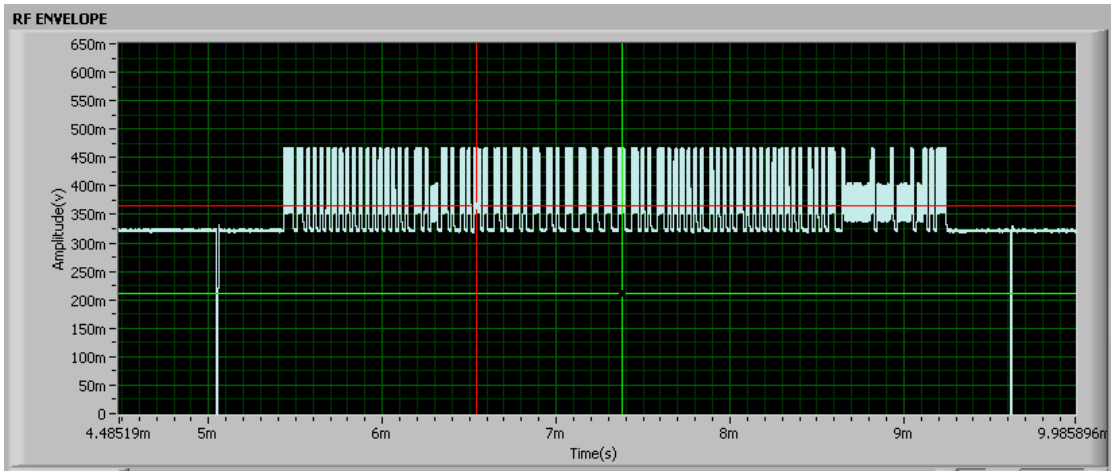


Figure 60. tag response collision waveform

Collision resolution is now possible and can be realized in future work [14].

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