INVESTIGATION OF HIGH-SPEED OPTOELECTRONIC RECEIVERS IN SILICON-GERMANIUM ($Si_{1-x}Ge_x$)

by

Amit Gupta

BE, Nagpur University, 2000

Submitted to the Graduate Faculty of

School of Engineering in partial fulfillment

of the requirements for the degree of

Master of Science

University of Pittsburgh

2003

UNIVERSITY OF PITTSBURGH

SCHOOL OF ENGINEERING

This thesis was presented

by

Amit Gupta

It was defended on

December 3rd, 2003

and approved by

Hong Koo Kim, Professor, Electrical Engineering Department

Raymond R. Hoare, Assistant Professor, Electrical Engineering Department

Donald M. Chiarulli, Professor, Computer Science Department

Thesis Advisor: Steven P. Levitan, John A. Jurenko Professor, Electrical Engineering Department

INVESTIGATION OF HIGH-SPEED OPTOELECTRONIC RECEIVERS IN SILICON-GERMANIUM ($Si_{1-x}Ge_x$)

Amit Gupta, MS

University of Pittsburgh, 2003

Silicon Germanium ($Si_{1-x}Ge_x$) is considered the choice for analog/mixed-signal RF and optoelectronic systems due to its high speed, low noise and compatibility with standard CMOS processes. The goal of this thesis is to investigate photo-detection in SiGe and optical receiver circuits in the commercially available IBM 5HP SiGe BiCMOS process. The study of photodetectors based on SiGe is of interest because of its high absorption capability at wavelengths between 1.1-1.5um. In this thesis several designs of receiver circuits and front-end transimpedance amplifiers (TIA) were designed and fabricated in the IBM 5HP (0.5µm) SiGe technology exhibiting high transit (f_T) and maximum oscillation frequency (f_{MAX}). Spectre simulations for both the transimpedance amplifiers and the complete receiver circuits are conducted at the single supply voltage of 3.3V in the Cadence Analog Affirma design environment. The analog mixed signal design tools NeoCircuit/NeoCell from Neolinear Inc. and Analog Affirma from Cadence Inc. are used for the optimization of the complete receiver circuits consisting of a transimpedance amplifier, a cascaded multi-stage differential amplifier and a decision circuit.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ACKNOWLEDGEMENT

I would like to express my deep appreciation to my research and faculty advisor Dr. Steven P. Levitan for trusting me to work on this project. I would like to thank him for his encouragement and guidance throughout the research for the last 2 years. His incredible advice and patience were important in the completion of my thesis. I also thank Dr. Donald M. Chiarulli, Dr. Hong Koo Kim and Dr. Raymond R. Hoare for serving on my master's thesis committee.

I also like to thank Chuck Brandt at the Pittsburgh Digital Greenhouse for their financial support and the valuable advice of Charles Buenzil at Benchmark Photonics Inc. and David Novosel at Intelligent Micro Design Inc. in this project.

A special thanks to Dr. Anthony Gadient, Mike Kelly and Jeremiah Cessna at Neolinear Inc. for always supporting me in trying to understand NeoCircuit/NeoCell.

I gratefully acknowledge the assistance and guidance of Dr. Donald M. Chiarulli in providing the facilities and lab equipment to test the optoelectronics chip in the Department of Computer Science, University of Pittsburgh.

Thanks to Dr. Mark Kahrs and Dr. Majd F. Sakr for their discussion and helpful points in my thesis. Without them, my thesis would not have been possible.

I would like to thank Jason Boles for his valuable help in installing the analog mixed signal design tools from Cadence Inc. and Neolinear Inc. and in many other aspects. I am also grateful to my past and current group, friends and others: Dr. Timothy P. Kurzweg now at Drexel University, Jose A. Martinez, Ibrahim Chamas, Michael M. Bails, Craig Windish, and Dave Reed for their support and suggestions.

I wish to thank my father, mother and brother for their support and understanding.

Last but not least, I would like to thank my graduate program administrator, Sandy Weisberg and others for their support.

1.0 INTRODUCTION

Fiber-optic technology plays a vital role in present telecommunication systems due to the low cost, small size, low transmission loss and high bandwidth compared to conventional electrical communication based on Copper (Cu). A fiber optic system consists of a transmitter, a channel and a receiver as shown in Figure 1.

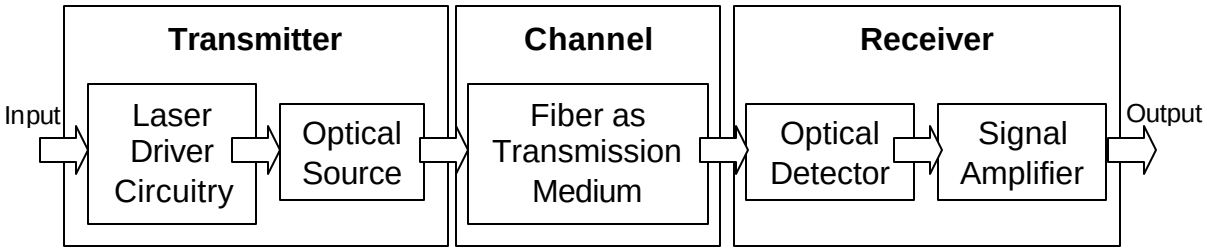


Figure 1 Key components of a fiber optic system

At the transmitter, the laser driver circuitry drives a laser source and the output is coupled into an optical fiber channel through which it propagates to the receiver. The laser source is connected by an optical fiber contained in a cable. The light leaving the optical fiber is absorbed by a photodetector that generates an electrical signal. The generated signal from the detector is weak, typically in the range of nano or micro-amps for a 1mWatt incident optical power depending on the design structure, size, efficiency and the technology used to build the photodetector. This generated signal must be amplified and thresholded before forwarding it to the digital signal processing circuitry.

There is an increasing demand for fiber optic systems in many emerging telecommunication and mobile communication systems and there are competing technologies

like Silicon (Si), Silicon-on-Insulator (SOI) and Gallium Arsenide (GaAs) to design such receivers. But, there are two main design constraints that need to be considered when designing such optical receivers. First, the technologies in which these receivers are designed should have high absorption capability at the wavelengths range of 1.3-1.5µm. Second, the technologies in which these transmitters and receivers are designed and fabricated should have low cost, high yield and high reliability.

The longer wavelengths are very important for long-haul fiber communication due to low insertion and dispersion loss. For silica based fibers, the three operating transmission windows are 850nm, 1310nm and 1550nm. For these transmission windows the attenuation in an optical fiber is typically 2.8dB/km, 0.52dB/km and 0.3dB/km respectively as shown in Figure 2. Since the attenuation is significantly lower at the two higher transmission windows, it is desirable to develop an efficient photodetector to function between the wavelengths of 1200-1300nm or 1150-1600nm range.

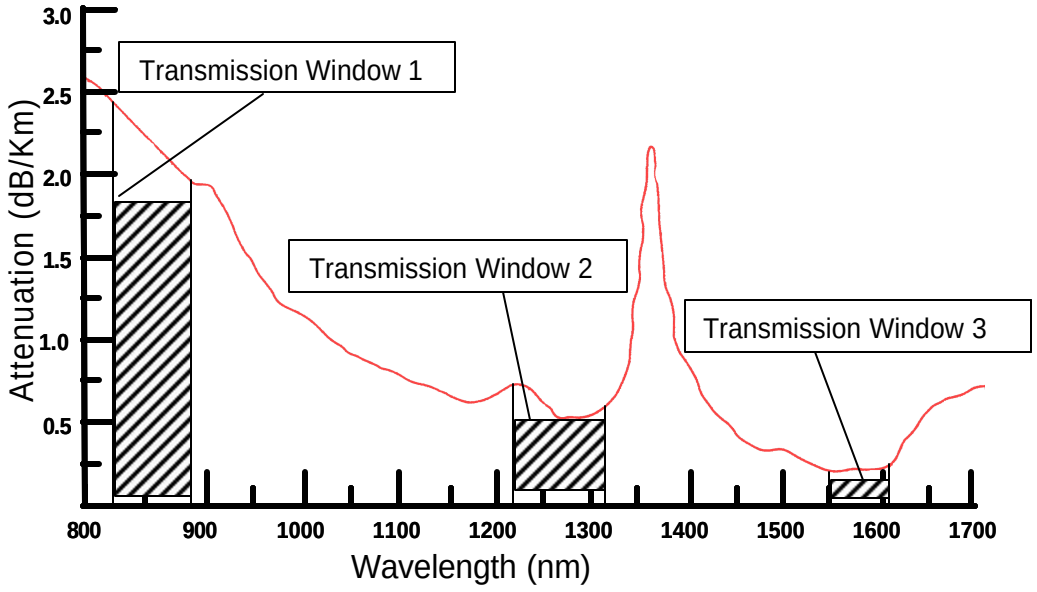


Figure 2 Optical fiber attenuation at different wavelengths [1]

Optical receivers based on III-V technology, like Gallium Arsenide (GaAs), can be used to make efficient optical detectors because of their direct band gap nature. But they have several drawbacks compared to Si technology. They are expensive to manufacture, have high defect densities, offer low reliability and most importantly are not compatible with the traditional CMOS processes. One of the ways to the reduce cost of receivers is to monolithically integrate optical detectors with electronic components. This integration also provides compactness, low parasitic losses, and reliability for Optoelectronic Integrated Circuits (OEIC).

On the other hand, Silicon (Si), an indirect gap semiconductor, has poor light absorption at wavelengths between 1.1 and 1.5um. It is also inferior to GaAs in terms of electron mobility and low noise. Many Si based photodetectors have been reported [2-5] but Si absorption capability is not efficient at the wavelengths between 1.1-1.5um. The photodiodes and phototransistors on Silicon-on-Insulator (SOI) were reported [6-7] to work at the wavelengths of 850nm. In spite the lower absorption coefficient of Si at longer wavelengths, it is the most widely used semiconductor in the semiconductor industry to build several analog and digital circuits due to its physical and chemical properties listed below:

- It is abundant in nature.
- It has virtually defect-free (single) crystals.
- It has excellent thermal and mechanical properties.
- It can be doped efficiently with both n-type and p-type impurities.
- It can be grown or deposited in different forms (crystalline, polycrystalline, amorphous).
- It can be etched easily.
- It crystallizes in the diamond lattice structure.
- It is non-toxic and highly stable at high temperatures.

- A high-quality perfect dielectric silicon oxide (SiO_2) can be grown by flowing oxygen across the wafer surface.

A new Si based technology, Silicon Germanium (SiGe), has been developed in the semiconductor industry to address the deficiency of low speed Si devices and high cost GaAs devices. SiGe was developed by the following companies, IBM [8], Hitachi [9], Conexant (Jazz) [10], Infineon [11], NEC [12], IHP [13], IMEC [14], TI [15], Philips [16], Lucent [17], ST Microelectronics [18], TEMIC [19], and CNET [20]. Several SiGe based photodetectors have been built [21-31] with high efficiency and an operating wavelength range of 1300-1500nm. These detectors were developed using custom SiGe processes. In this thesis, we investigate SiGe based photodetectors. These photodetectors are built using the only commercially available SiGe process, provided by IBM [8]. We believe, since this technology exhibits a maximum oscillation frequency (f_{MAX}) of 47GHz and transit frequency (f_T) of 65GHz, very high speed optoelectronic circuits can be designed in this process [32].

1.1 BACKGROUND AND MOTIVATION

The ability to integrate high-speed analog circuits based on SiGe HBT devices with optoelectronic systems provides a logical solution to the problems of next generation telecommunication and networking applications. Beyond the abilities of SiGe as a high-speed, CMOS compatible technology, there is additionally the possibility of using SiGe as the basis for monolithically integrated photodetectors.

The concept of a SiGe Hetero-junction Bipolar Transistor (HBT) is well understood and the detailed theory related to this device was first developed by Kromer in 1957 [33]. The first functional SiGe HBT was demonstrated in December of 1987 [34] and SiGe hetero-junction

growth techniques compatible with silicon technology were developed [35-36]. Since then there has been a tremendous advancement in the development of SiGe devices [37]. Due to the differences in the lattice constant and band gap energy of Si and Ge, the valence and the conduction band of a SiGe bipolar device changes giving rise to high electron mobility. This electron mobility varies with Ge composition and the doping profiles of impurities like phosphorous and arsenic in SiGe devices. Hence, circuits based on this SiGe technology have higher speed than conventional silicon. Thus, SiGe Hetero-junction Bipolar Transistor (HBT) devices are ideally suited for high-speed wireless communication systems. The need for high-speed circuits based on such devices is increasing and the market for SiGe BiCMOS based products has evolved to demonstrate a large number of digital, analog RF and microwave circuits for application to mobile communications, wide area networks, satellite communications, radar and optical fiber communications systems [32, 38-40].

A large number of commercial products using SiGe HBTs are currently on the market, and a foundry service for the IBM SiGe process is available through MOSIS [41]. The availability of this commercial process in the market has motivated us to build an optical receiver system for three reasons:

First, to the best of our knowledge no SiGe based photodetectors in the IBM 5HP technology have been reported.

Second, it is the only commercially SiGe process in the market available to us to carry out an investigation on SiGe based photodetectors.

Third, among all the SiGe processes available at he time this process offers highest level of transit (f_T) and maximum oscillation frequency (f_{MAX}) to design high-speed analog circuits.

1.2 STATEMENT OF WORK

In this thesis we utilize the IBM SiGe process in order to design and layout several designs of SiGe based photodetectors and receiver circuits for fiber optic systems. We carry out our work in five steps:

(i) Perform a quantitative analysis of the intrinsic photo-detection mechanism in IBM SiGe technology to build photodetectors. We also predicted the operating wavelength range in SiGe for high absorption coefficient, responsivity and high quantum efficiency.

(ii) Study the micro-fabrication steps for the IBM process to build photodetectors based on SiGe.

(iii) Investigate previous work on circuit topologies for transimpedance amplifiers and voltage amplifiers designed in SiGe processes.

(iv) Explore the capabilities of several analog design mixed signal tools from Cadence and Neolinear Inc.

(v) Design, simulate and layout several transimpedance amplifiers and a complete set of receiver circuits consisting of transimpedance amplifiers, differential amplifiers and a decision circuit in the IBM process.

1.3 THESIS ORGANIZATION

The goal of this thesis is to specifically investigate three areas. First, to examine the practicality of using photodiodes and phototransistors based on SiGe as photodetectors for longer wavelength light. Second, to test the abilities of Neolinear- NeoCircuit/NeoCell analog mixed signal design tools in optimizing receiver circuits designed using SiGe and CMOS devices.

Third, to design and fabricate several designs of complete receiver circuits consisting of transimpedance amplifiers, differential amplifiers and a decision circuit.

The thesis is organized as follows: Chapter 2 investigates the recent developments in SiGe based photodetectors. Chapter 3 discusses the optical properties, absorption coefficients of SiGe alloys and the efficiency of SiGe based photodetectors. Chapter 4 discusses the device physics of the SiGe Hetero-junction Bipolar Transistor (HBT). Chapter 5 discusses the micro-fabrication steps for the SiGe IBM 5HP process and the design of photodetectors. Chapter 6 presents the circuit selection, design, simulation results and layout of the front-end architecture-transimpedance amplifiers. Chapter 7 presents the configuration design of the receiver circuits with the test results of an optoelectronic receiver chip and Chapter 9 presents the summary and the conclusion.

2.0 INVESTIGATION ON $Si_{1-X}Ge_X$ PHOTODETECTORS

Several types of Si and $Si/Si_{1-x}Ge_x$ photodetectors including PINs, metal-semiconductor-metal (MSM) photodiodes, and avalanche photodiodes have been reported. Si retains its transparency at the longer wavelengths namely 1.1µm and above due to its indirect band gap nature. Ge offers a better absorption coefficient to incident light than Si at the wavelengths of 1.1 -1.5µm as shown in Figure 3. In order to address the absorption deficiency of Si at longer wavelengths, photodetectors with $Si_{1-x}Ge_x$ absorbing layer have been developed by other researchers [21-31]. No other researchers however, have investigated SiGe photodetectors in the IBM process.

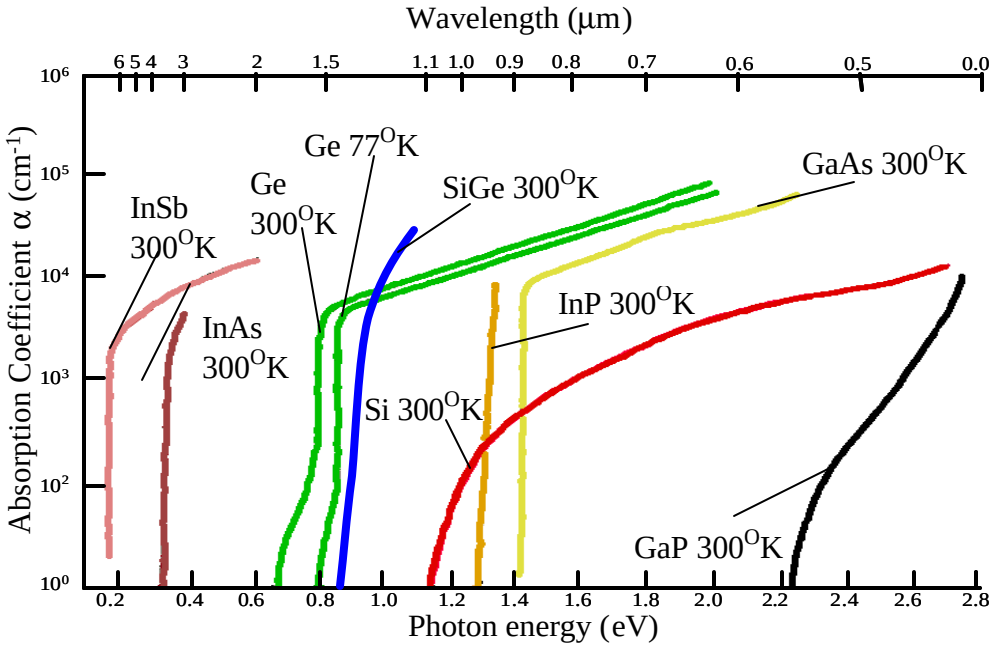


Figure 3 Optical properties of Si, SiGe and Ge alloys at wavelengths 1.1 -1.5mm [42-43]

2.1 DEVELOPMENT ON SiGe PHOTODETECTORS

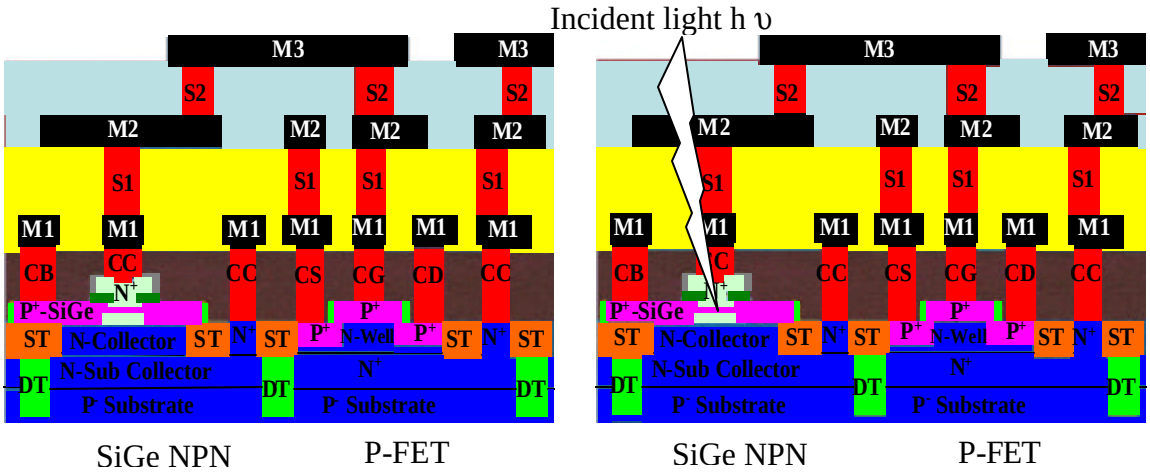
The possibility of using SiGe devices as high speed, low noise photodetectors in the near-IR spectrum from 850nm to 1550nm [21-31] has been explored. In theory, these detectors can cover the range of both free space and fiber optic communication wavelengths. Photo-detection has been implemented with SiGe Metal Semiconductor Metal (MSM), P-Insulator-N (PIN) [44], hetero-structure photodiodes [45-46] and phototransistors [47]. One example is a separated absorption multiplication avalanche photo diode (SAMAPD), which has been shown to work at 930nm with a bandwidth of 1.9GHz. This type of detector is optimized for short distance optical fiber communication systems [48]. A second technique is the use of SiGe in MSM photodiodes. These have been shown to have bandwidth in excess of 1GHz while being compatible with SiGe high electron mobility transistors (HEMT). These types of devices operate at much lower voltages than comparable bulk silicon photodiodes, with DC responsivity as high as 0.12A/W [49]. A third class of SiGe photodetectors is based on a vertical cavity multi-layer PIN diode. The quantum efficiency of one such device at 980nm was reported at 20% with a minimum receiver sensitivity of –10.4 dBm at 1 Gb/s [50]. Finally, investigations on different types of SiGe photodiodes for photo-detection in the 1.3μm - 1.55μm range [21-31] have been carried out. These photodetectors have quantum efficiency in the range of 1-25% at the wavelengths of 1300nm. It has been shown, that in order to achieve high responsivity at the 1.3μm wavelength region in SiGe/Si photodetectors, the percentage of Ge concentration should be in excess of 35-50 percent [51-52].

After investigating the development of several photodetector structures in other custom SiGe processes, the availability of the IBM process has prompted us to build photodetectors in this process. It was found that due to the fixed integration layers of the IBM SiGe process only

two kinds of photodetector structures are possible. Since Ge is graded only in the base of the NPN transistor the photodetectors based on NPN devices are of interest to us. Based on this idea, phototransistors and photodiodes based on SiGe NPN bipolar devices were designed and fabricated. A brief overview and a detailed description of the design and the fabrication of SiGe based photodetectors is discussed in sections 2.2 and 5.4 respectively

2.2 OVERVIEW OF THE IBM SiGe BASED PHOTODETECTOR STRUCTURES

In our study of SiGe based photodetectors in the IBM process we used the Blue Logic™ SiGe process. This is a BiCMOS process, which has NPN HBT SiGe bipolar transistors available. Several methods of light detection in SiGe photodetector were examined as well as multiple circuit configurations in SiGe BiCMOS built for amplification and thresholding. SiGe photodetectors were made by exposing the SiGe "base" layer of the HBT structure, as shown in Figure 4 and Figure 5.



Incident light h υ

Figure 4 Cross section of an IBM SiGe process **Figure 5 Exposed base for SiGe transistor** [40]

If the emitter is removed, the SiGe layer in the base can be exposed to external light, creating a photodiode. On the other hand, if the emitter contact is preserved and the base contact is removed then a phototransistor is created. In order to understand the detailed design SiGe photodetectors in the IBM process we must first discuss the optoelectronic properties of SiGe alloys in Chapter 3. The design and fabrication of photodetector structures based on IBM SiGe is discussed in detail in section 5.4.

3.0 OPTOELECTRONICS IN SiGe ALLOYS

The IBM SiGe process has encouraged us explore photodetectors and to study optical and electronic properties of SiGe alloys. Photodetectors, the first basic component of the fiber optic receiver system, as shown in Chapter 1, converts an incident optical signal into an electrical signal. For a weak input signal it is desirable to have a maximum amount of electric current generated. Therefore it is essential to consider the factors of responsivity and quantum efficiency of a photodetector with respect to the input signal. Responsivity of a photodetector is mainly related to the absorption coefficient and the thickness of the semiconductor material. A high absorption coefficient and thickness mean that more photons will get trapped in a photodetector device and higher current will be generated. The responsivity and the quantum efficiency in SiGe alloy is discussed in sections 3.7 and 3.8 respectively. The absorption coefficient depends on the intrinsic absorption mechanism in a semiconductor material and is discussed in section 3.6. For intrinsic absorption the photon energy of the incident optical light must be greater than or equal to the band gap energy and the phonon energy of the semiconductor material. The photon energy, phonon energy and the bandgap energy in SiGe alloys is presented in sections 3.1, 3.2, 3.3 and 3.4 respectively. Also it is estimated that the maximum percentage of Ge in the SiGe IBM process is 20% [36, 53] which is used for calculating band gap energy and dielectric constant in SiGe alloys.

3.1 PHOTON ENERGY

Photon energy is defined as the minimum amount of energy possessed by an incident photon to excite an electron from the valence band to the conduction band. The expression for photon energy is given as:

$$E = hu \tag{1}$$

Where h is Planck's constant = 6.6261×10^{-34} (Js); υ is the frequency of the incident light (Hertz) and E is the energy of the incident light in electron volts (eV).

Photons can be characterized by their frequency (υ) and wavelength (λ) as:

$$u = \frac{c}{l} \tag{2}$$

Where c is the velocity of light = 3×10^{8} (m/s); λ is wavelength of the incident light (m).

On substituting equation (2) in (1) the expression for photon energy is derived as:

$$E(eV) = \frac{hc}{l} = \left(\frac{6.6261x10^{-34}(Js)x3x10^{8}(m/s)}{lx1.6x10^{-19}(C)} \right) = \left(\frac{1241}{l(nm)} \right) \tag{3}$$

On using equation (3) the photon energy E (eV) of the incident light at different wavelengths is summarized in Table 1 as follows:

Table 1 Photon energy of the incident light at different wavelength

Wavelength (l) nm	Energy of the Incident Light E (eV)
900	1.3788
950	1.3063
1000	1.2410
1050	1.1819
1100	1.1281
1150	1.0791

Table 1 (continued)

1200	1.0341
1250	0.9928
1300	0.9546
1350	0.9192
1400	0.8864
1450	0.8558
1500	0.8273

As shown in Figure 6, as the wavelength increases, the light energy associated with the incident optical signal decreases. The significance of Table 1 is to find out the operating wavelength at which the intrinsic absorption in a SiGe semiconductor is possible. The mechanism of intrinsic absorption is discussed in detail in section 3.6.

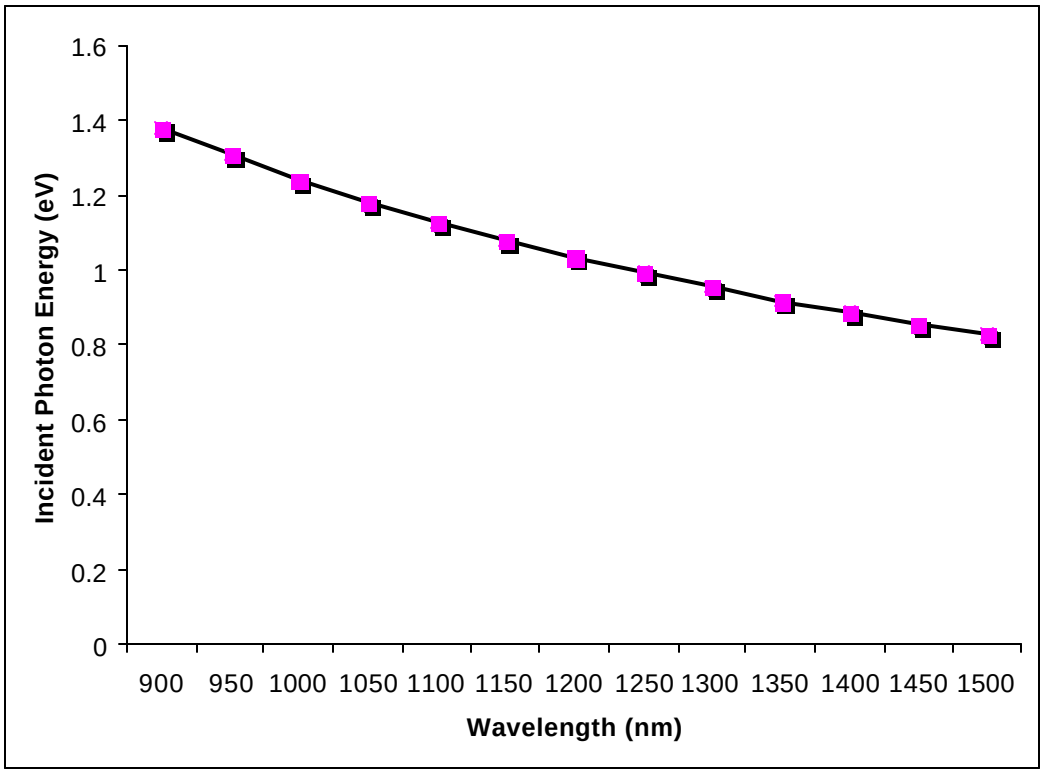


Figure 6 Incident light energy of photon for different wavelengths

3.2 ABSORPTION MECHANISM IN A SEMICONDUCTOR MATERIAL

The photo-electric effect based photodetectors are those that directly generate photocurrent from the interactions between the photons and atoms in the detector material. The probability of an atom absorbing a photon and generating carriers and forming photocurrent is small. However, since the number of atoms in a semiconductor is huge, the probability of an atom interacting with an incident photon to form photo-excited free carriers is quite high in a well designed detector.

Based on this idea, the concept of intrinsic band-to-band absorption, shown in Figure 7 is observed in a semiconductor material. In this mechanism the photon energy (E) of the incident light is greater than a material band gap energy E_g of a semiconductor material and a photon is able to excite an electron from the valence band up to the conduction band. The hole and the electron constitute a charge carrier and, on the application of an electric field, the hole and the electron can be transported through the material.

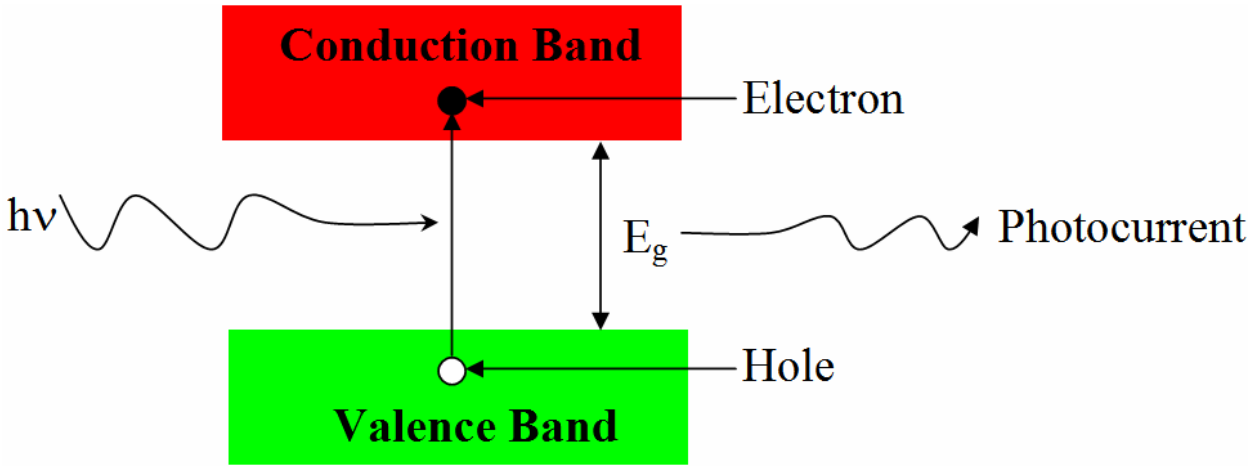


Figure 7 Intrinsic absorption phenomena in a semiconductor

The requirement for the sufficient photon energy (E) to create an electron-hole pair is expressed as:

$$h\upsilon \geq E_g$$

$$\frac{hc}{\lambda} \geq E_g \tag{4}$$

Where h is the Planck Constant = 6.63 x 10^{-34} (Js) and E_g is the band gap energy of the SiGe alloy (eV); c is the velocity of light = 3 x 10^8(m/s); λ is the wavelength of the incident light (m) and υ is frequency of the incident light (Hertz).

3.3 BAND GAP ENERGY IN SiGe ALLOYS

Band gap energy is defined as the amount of energy (in electron volts) required to free an outer most shell electron from its orbit, and promoting it from the valence to the conduction level. The expression for the band gap energy in SiGe alloys for different percentages of Ge [54, 55] is given as:

$$1.12 - 0.41\,x + 0.008x^2 \text{ for } (0<x<0.85) \tag{5}$$

$$1.86 - 1.2\,x \text{ for } (0.85<x<1)$$

Where x is the maximum percentage of Ge in the SiGe alloy.

The maximum percentage of Ge in the IBM process is 20% [36, 53] and therefore the first part of equation (5) is used for the calculation. The calculated value of band gap for $Si_{0.80}Ge_{0.20}$ is:

$$E_{gSi0.80Ge20} = 1.0383 \text{ eV}$$

This calculated value lies between the band gap energy of Si and Ge. See appendix for details.

3.4 PHONON ENERGY

A phonon is required for the conservation of momentum in order to enable the radiative transition of an electron from the minimum of the conduction band to the maximum of the valence band. In indirect semiconductors like Si a phonon is generated whenever photon energy is emitted. Therefore more photons will have energy E_g-E_p than E_g+E_p. Thus photon energy can be written as:

$$E(eV) = hu = \frac{hc}{l} = E_g + E_p$$

The phonon energy for the IBM $Si_{0.80}Ge_{0.20}$ is calculated as E_P ~ 50meV [55].

3.5 REFLECTIVITY IN SiGe ALLOYS

Reflection loss occurs due to differences in the index of refraction between the two materials. The Fresnel reflectivity ($\Re$) for an optical signal at normal incidence to an interface between two materials is expressed as follows:

$$\Re = \left[\frac{(h_1 - h_2)^2}{(h_1 + h_2)^2} \right] \quad (6)$$

Where η_1 is index of refraction of air =1 and η_2 is the index of refraction of the $Si_{1-x}Ge_x$ material.

The reflectivity depends on the index of refraction. The value of the index of refraction for SiGe alloys can be estimated from experimental results [51] shown in Figure 8. Since the percent of Ge is estimated to be 20% in the IBM SiGe process therefore, the index of refraction for the IBM $Si_{0.80}Ge_{0.20}$ is calculated as η_2=3.50 in Figure 8.

On substituting the values of η_1 and η_2 respectively in Equation (6) reflectivity can be calculated as:

$$\Re = \left[\frac{(1-3.5)^2}{(1+3.5)^2}\right] = 0.3086 \text{ or } 30.86\%$$

This value for the Fresnel reflectivity ($\Re$) is quite high.

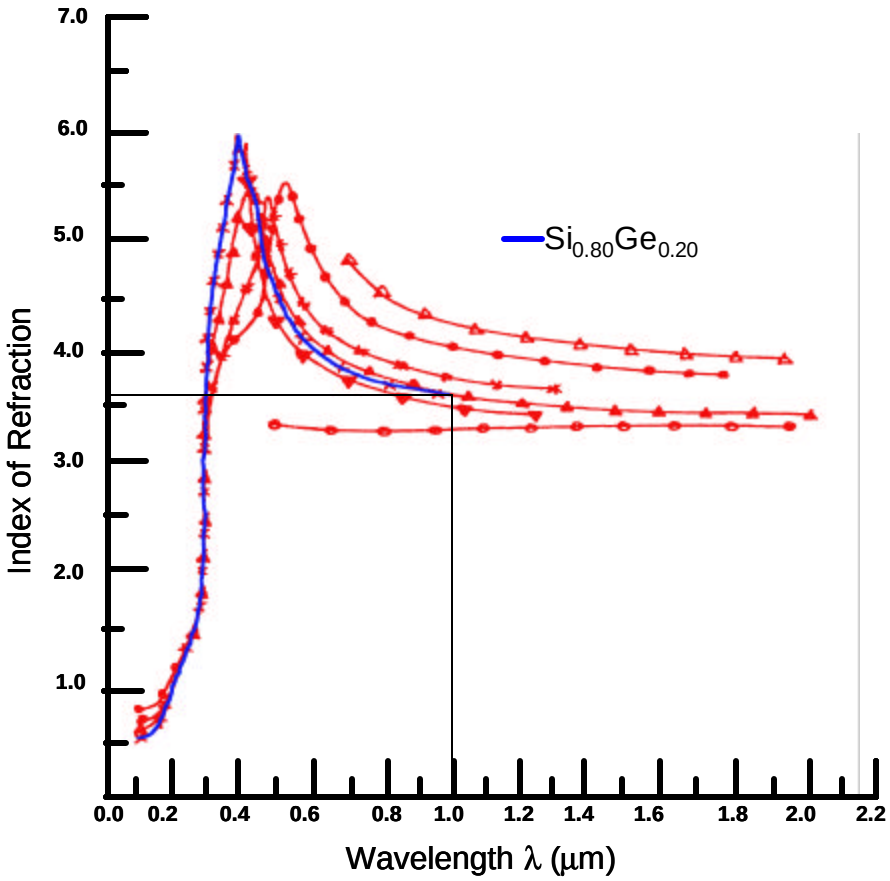


Figure 8 Refractive index of SiGe alloy versus wavelength [51]

So far we have calculated the values of photon energy, band gap energy, phonon energy and reflectivity for $Si_{0.80}Ge_{0.20}$ alloys in sections 3.1, 3.2, 3.3 respectively. These values are required to calculate the absorption coefficient in SiGe alloys at different wavelengths as shown in the next section.

3.6 ABSORPTION COEFFICIENT IN SiGe ALLOYS

The absorption coefficient (α) is the most important operating characteristic for photodetectors. In a detector, the photocurrent produced depends on the amount of photons absorbed and the absorption coefficient of a semiconductor. The quantum efficiency of the photodetector strongly depends on the absorption coefficient of the semiconductor material. Therefore an estimate of the absorption coefficient as a function of photon energy and Ge compositions in the SiGe alloy is necessary. In $Si_{1-x}Ge_x$ the indirect absorption process depends on the interaction of the electrons and the electromagnetic wave and, at the same time, depends on the interaction of the electrons and the semiconductor lattice structure. The penetration depth of the light in a semiconductor material can also be determined by calculating the absorption coefficient. Accordingly, it is very important to calculate the value of the absorption coefficient in SiGe at different wavelengths. The fundamental absorption coefficient (a) can be expressed as [56-58]:

$$a(E,T)=0 \text{ For } hu \le E_g + E_p$$

$$a(E,T)=\left[A_a\left\{\frac{\left(hu - E_g + E_p\right)^2}{e^{\left(\frac{kq}{kT}\right)}-1}\right\}\right] \text{ For } E_g - E_p < hu \le E_g + E_p$$

$$a(E,T)=\left[A_a\left\{\frac{\left(hu - E_g + E_p\right)^2}{e^{\left(\frac{kq}{kT}\right)}-1}\right\}+A_e\left\{\frac{\left(hu - E_g - E_p\right)^2}{1-e^{\left(\frac{-kq}{kT}\right)}}\right\}\right] \text{ For } hu \ge E_g + E_p \quad (7)$$

Where α is the absorption coefficient (cm^{-1}); A is the temperature-independent proportionality factor and A_a and A_e weigh phonon absorption and emissions contributions which are equal to 12000 and 3000 $cm^{-1}(eV)^{-1/2}$ respectively [61]; $h\upsilon$ is the photon energy (eV); E_g is the energy band gap for the IBM $Si_{0.80}Ge_{0.20}$ =1.0383 (eV); E_P is the phonon energy for the IBM $Si_{0.80}Ge_{0.20}$

= 0.05 (eV); T is absolute room temperature (300^{o}K) and k is Boltzmann's constant = 8.617 x 10^{-5} (eV/K).

Before calculating the absorption coefficient in SiGe alloys it is required to know the wavelength range between which the intrinsic absorption in SiGe semiconductor is possible. On substituting values of the band gap energy in IBM $Si_{0.80}Ge_{0.20}$ from section 3.3 and the photon energy of incident light from Table 1 in equation (1) we can summarize the operating wavelength range for intrinsic absorption in SiGe alloys as shown in Table 2:

Table 2 Operating wavelength for intrinsic absorption in $Si_{0.80}Ge_{0.20}$ alloys

Wavelength (λ) nm	$hu \geq E_g + E_p$ **(eV)**	**Intrinsic Absorption Condition**
900	$1.3788 \geq 1.0383 + 0.05$	(Satisfied)
1000	$1.2410 \geq 1.0383 + 0.05$	(Satisfied)
1100	$1.1281 \geq 1.0383 + 0.05$	(Satisfied)
1150	$1.0791 \geq 1.0383 + 0.05$	(Satisfied)
1200	$1.0341 \geq 1.0383 + 0.05$	(Not Satisfied)
1250	$0.9928 \geq 1.0383 + 0.05$	(Not Satisfied)
1300	$0.9546 \geq 1.0383 + 0.05$	(Not Satisfied)
1400	$0.9191 \geq 1.0383 + 0.05$	(Not Satisfied)
1500	$0.8273 \geq 1.0383 + 0.05$	(Not Satisfied)

One can conclude from Table 2 that if the photon energy of the incident light is greater than or equal to the band gap energy of IBM $Si_{0.80}Ge_{0.20}$ semiconductor material between the wavelength range of below 900 to 1150 nm. Therefore the intrinsic absorption is only possible between these wavelengths. On substituting the values of photon energy (E), band gap energy (Eg), phonon energy (Ep) and reflectivity ($\Re$) for SiGe alloys in equation (7) the absorption coefficient at wavelength of 1150nm is calculated as follows:

$$a(E,T)=\left[12000\left\{\frac{\left(1.0791(eV)-1.0383(eV)+0.05(eV)\right)^{2}}{e^{\left(\frac{0.05(eV)}{8.617x10^{-5}(\frac{eV}{^{0}K})x300(^{0}K)}\right)}-1}\right\}+3000\left\{\frac{\left(1.0791(eV)-1.0383(eV)-0.05(eV)\right)^{2}}{1-e^{\left(\frac{-0.05(eV)}{8.617x10^{-5}(\frac{eV}{^{0}K})x300(^{0}K)}\right)}}\right\}\right]$$

a (λ=1150, 300^{O}K) = 17.01/cm

Table 3 gives a summary of the absorption coefficient at different wavelengths of incident light. The absorption coefficient in $Si_{0.80}Ge_{0.20}$ alloys decreases at longer wavelengths. After λ=1200 nm the absorption coefficient starts increasing again, but it is irrelevant since intrinsic absorption beyond λ=1150 is not possible as already seen above.

Table 3 Absorption Coefficient in $Si_{0.80}Ge_{0.20}$ alloys at 300^{0}K for different wavelengths

Absorption Coefficient (a) at different wavelengths l (nm)	**Output Results (per cm)**
800	1387.195
900	605.157
1000	246.54
1100	45.1837
1150	17.01
1200	14.55
1300	64.99
1400	164.01
1500	291.46

The result obtained for the absorption coefficient in SiGe as shown in Table 3 is plotted in Figure 9. It can be observed in Figure 9 that the results obtained from our calculations for SiGe alloy is very close to the one obtained by experimental results [51].

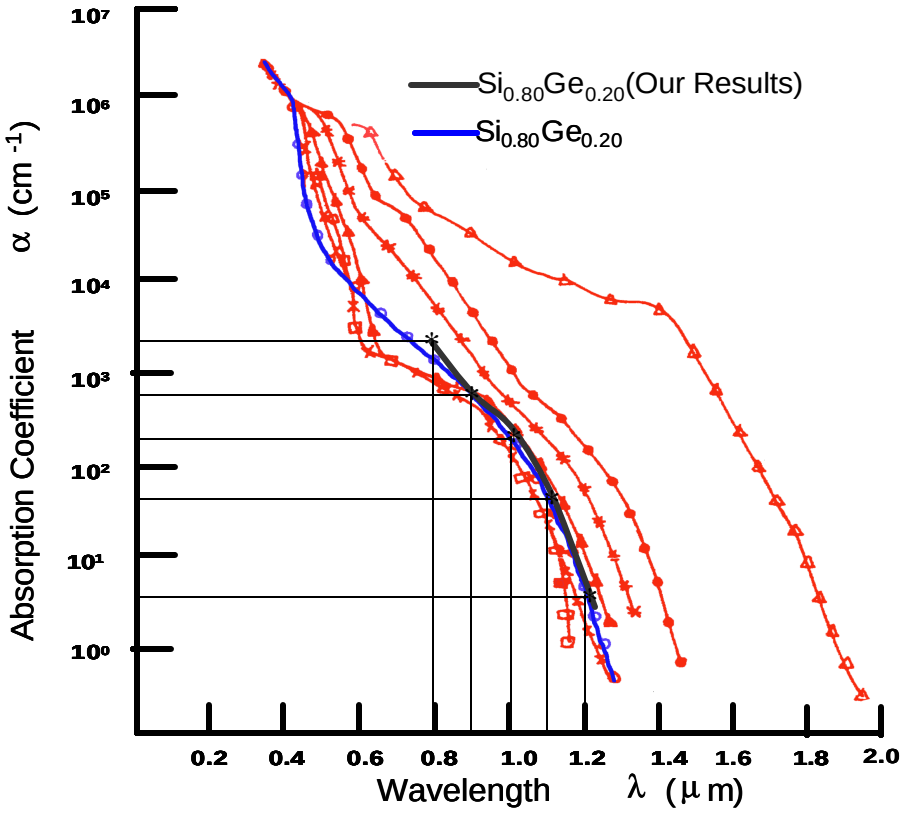


Figure 9 Optical absorption coefficients of SiGe alloys at different wavelengths [51]

3.7 PHOTODETECTOR QUANTUM EFFICIENCY

The light signal whose photon energy is sufficient to generate photo-carriers will continuously tend to lose energy within the crystal lattice as the optical field propagates through the semiconductor. Inside the semiconductor, the field decays exponentially as the energy is absorbed by a semiconductor. The material can be characterized by an absorption length and the penetration depth as shown in Figure 10. The power in the optical field decays with distance and

the amount of power absorbed in a semiconductor as a function of position within the material is given as:

$$P_{absorbed} = P_{incident}\left\{(1-\Re)(1-e^{-ax})\right\} \quad (8)$$

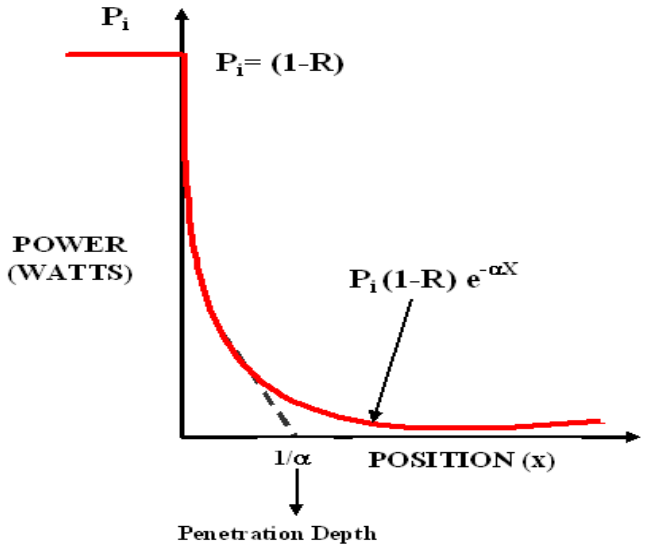


Figure 10 Optical light absorption in a semiconductor [59]

Where P_i is the power of the Incident light $=h\upsilon$; $P_{absorbed}$ is the power in watts for the number of photons absorbed (watts); α is absorption coefficient for $Si_{1-x}Ge_x$ and x is the depth or thickness of absorbing ($Si_{1-x}Ge_x$) layer.

Hence equation (8) can be rewritten as:

$$\frac{P_{absorbed}(x)}{P_{Incident}(x)} = \left[(1-\Re)(1-e^{-ax})\right]$$

Therefore photodetector quantum efficiency $\eta(x)$ can be defined as:

$$\eta(x) = \frac{\text{Number of photo-carriers absorbed}}{\text{Number of incident photons}} = \left[(1-\Re)(1-e^{-ax})\right]$$

On substituting the value of reflectivity ($\Re$) in equation (8) from section (3.5) and the width of the SiGe layer (50nm in the IBM process [40]) the value of the photodetector quantum efficiency at λ=1150 is calculated as:

$$h(x) = \left[(1-0.3086)\left(1-e^{-17.01(\frac{1}{cm})x50x10^{-9}x10^{2}(cm)}\right)\right] = 0.0058\%$$

Table 4 Quantum Efficiency of the IBM Photodetector at different Wavelengths

Quantum Efficiency h(x) at different wavelengths l (nm)	**Output Result (Percentage)**
800	0.47
900	0.20
1000	0.085
1100	0.01
1150	0.0058
1200	0.005

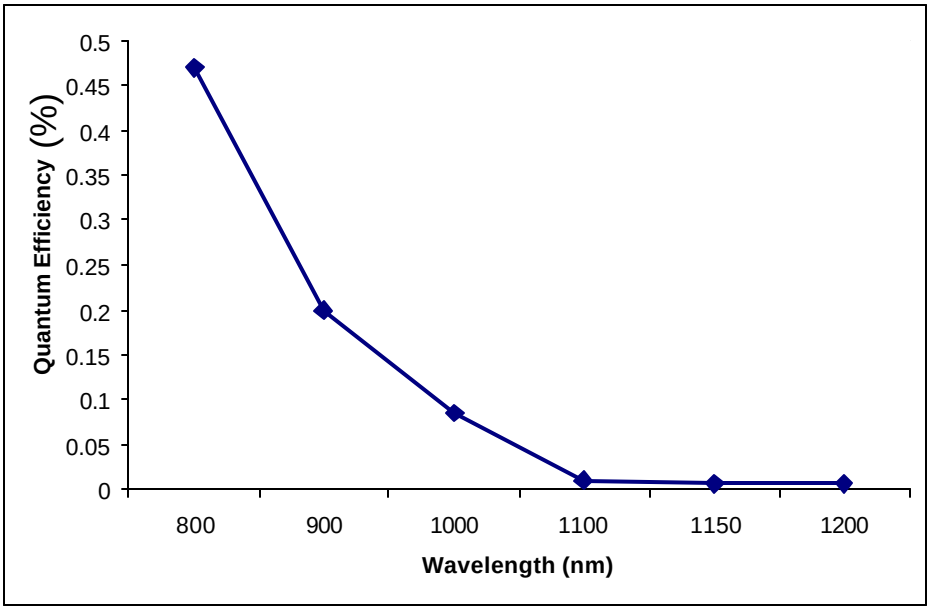


Figure 11 Quantum Efficiency versus Wavelength

In Table 4, a summary of the quantum efficiencies at different operating wavelengths is shown. The calculated result in Table 4 is plotted in Figure 11 which indicates that at longer wavelengths the external quantum efficiency in $Si_{0.80}Ge_{0.20}$ decreases.

3.8 RESPONSIVITY OF THE IBM SiGe PHOTOTRANSISTOR

The Responsivity (R) of the detector is defined as the ratio of the photocurrent produced to the incoming optical energy received. It depends critically on the absorption spectrum of the semiconductor material. For high responsivity, the absorbing material should have a band gap very near, but above the wavelength limit of the optical signal. The expression for responsivity is given as:

$$R = \left(\frac{h(x)q}{hu}\right) = \left(\frac{h(x)q\,l}{hC}\right) = \left(\frac{h(x)q\,l\,(nm)}{1241}\right) \tag{9}$$

Where η is the photodetector quantum efficiency $0 \leq \eta \leq 1$; q is electron charge equal to 1.6×10^{-19} (J); h is Planck's constant = 6.6261×10^{-34} (J s) and υ is the frequency of the optical signal (Hz)

On substituting the value of the photodetector quantum efficiency value from section (3.7) into equation (9) the responsivity of the IBM photodetector at λ=1150 nm can be calculated as:

$$R = \left(\frac{h(x)q}{hu}\right) = \left(\frac{5x10^{-5}x1150(nm)}{1241}\right) = 48.34\mu \text{ Amps/Watt}$$

Table 5 Responsivity in the IBM $Si_{0.80}Ge_{0.20}$ at different wavelengths

Responsivity (R) at different wavelengths l (nm)	Output Result (Amps/Watt)
800	3.029m
900	1.450m
1000	0.684m
1100	88.63µ
1150	43.34µ

Thus Table 5 shows at longer wavelengths the responsivity of the photodetector in $Si_{0.80}Ge_{0.20}$ alloys decreases. These values are plotted in Figure 12 as shown below:

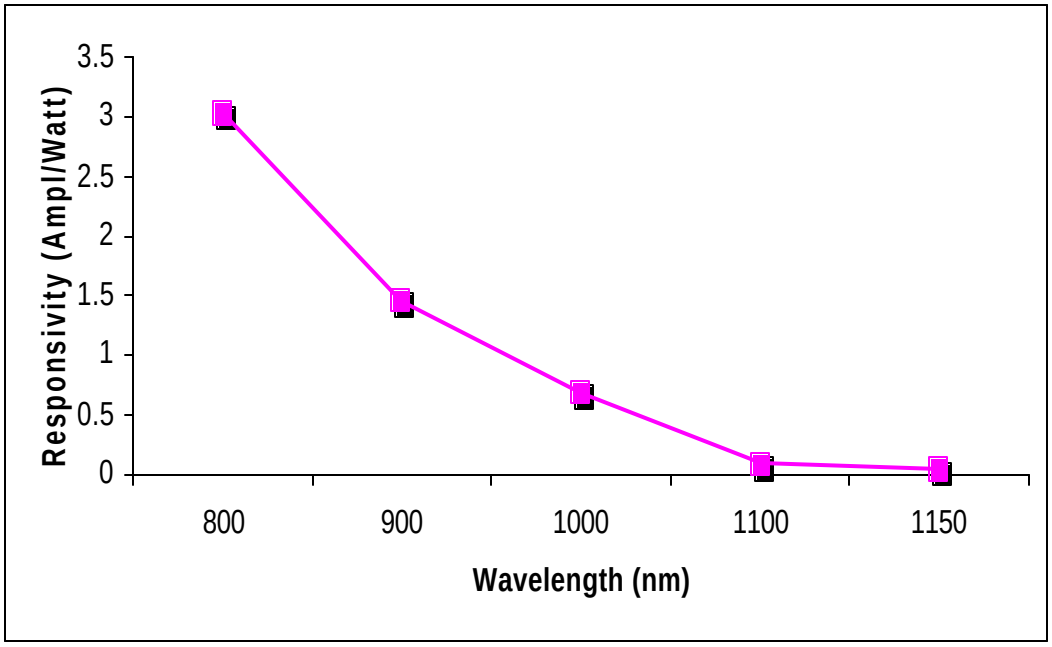


Figure 12 Responsivity of SiGe based photodetectors at different wavelengths

3.9 DEPLETION REGION IN THE IBM PHOTOTRANSISTOR

In the previous chapters it has been shown that Ge has higher absorption capability than Si at wavelengths between 1.1-1.5μm. Therefore for efficient absorption it is desirable to have a maximum percentage of Ge in the SiGe alloy. However the combination of materials and quantum mechanical considerations complicates matters. At Ge compositions of 30-50%, the strained layer thickness cannot exceed 10-50 nm before the onset of misfit dislocations. Such dislocations would affect the SiGe device performance.

To the best of our knowledge the maximum percentage of Ge is 20% in the IBM SiGe process [36, 53] and since the Ge percentage is less than 35-50% the thickness of the base could be more than 50nm. Also, the majority of the photons are absorbed in the depletion region of the base-collector and emitter-base junction. Therefore it is necessary to calculate the depletion region width of the base-collector and emitter-base junction of the SiGe NPN transistor. But, since Germanium is graded more on the collector side and the width of the depletion region is more on the base-collector side than the emitter-base side, due to reverse bias, it is desirable to calculate the depletion region of the base-collector. The data to calculate the width of the depletion region in the IBM NPN SiGe transistor is taken from [40], the SiGe IBM process as mentioned below:

(i) Thickness or width of the SiGe base = 50nm or 0.05μm

(ii) Doping of boron in the base (p-type or N_A) = 2×10^{18} B/cm^3

(iii) Doping of phosphorous in the collector (n-type or N_D) = 10^{16} P/cm^3

(iv) Doping of arsenic in the collector (n-type or N_D) = 2×10^{21} As/cm^3

The depletion region width of the base and the collector sides of the NPN transistor under reverse biased conditions can be expressed [60] as:

$$X_{p-SiGe} = \left[\left(\frac{2K_s e_0 (V_J + V_R)}{q} \right) \left(\frac{N_D}{N_A (N_A + N_D)} \right) \right]^{\frac{1}{2}} \quad (10)$$

$$X_{n-Si} = \left[\left(\frac{2K_s e_0 (V_J + V_R)}{q} \right) \left(\frac{N_A}{N_D (N_A + N_D)} \right) \right]^{\frac{1}{2}} \quad (11)$$

Where Xn-Si is the depletion region width on collector (N-side); Xp-SiGe is width of depletion region on base (P-SiGe side); V_R is the reverse bias voltage applied to the base-collector junction=5(V); K_S is the relative permittivity or dielectric constant of N and P-SiGe; ε_0 is the permittivity of space= 8.85418 x 10^{-12} (F/m); q is the electron charge=1.6 x 10^{-19} C; N_A is the number density of acceptor atoms in a semiconductor=2x10^{18} (B/cm^3); N_D is the number of density donor atoms in a semiconductor=10^{16} (P/cm^3) and V_J is the potential generated across the depletion region.

The potential (V_J) generated across the base-collector junction of the NPN transistor can be expressed as:

$$V_J = V_T \ln\left(\frac{N_A N_D}{n_i^2} \right)$$

Where V_T = K T=8.62 x 10^{-5} x 300^0 K = 0.02586 V or ~26 (mV); k is Boltzmann's constant = 8.62 x 10^{-5} (eV/^{0}K); T is room temperature = 300 (^{0}K) and n_i is the intrinsic concentration of Si = 1x10^{10} (cm^{-3}).

In general for NPN transistors, the emitter is doped higher than the base and collector, and the base is doped higher than the collector. Therefore $N_A >> N_D$ and equations (10) and (11) can be reduced to equations (12) and (13) as given below:

$$X_{p-SiGe} = \left[\left(\frac{2K_s e_0 (V_J + V_R)}{q}\right)\left(\frac{N_D}{qN_A^2}\right)\right]^{\frac{1}{2}} \quad (12)$$

$$X_{n-Si} = \left[\left(\frac{2K_s e_0 (V_J + V_R)}{q}\right)\left(\frac{1}{N_D}\right)\right]^{\frac{1}{2}} \quad (13)$$

To calculate the depletion region width ($X_{p\text{-}SiGe}$), the dielectric constant (K_S) of $Si_{0.80}Ge_{0.20}$ is required [55] and calculated as follows:

$$K_{S\text{-}p\text{-}SiGe} = 11.7 + 4.5x$$

Where x = Maximum percentage of Ge in the IBM SiGe process=20% [36, 53]

$$\text{Hence } K_{S\text{-}SiGe} = 12.6$$

On substituting the calculated value of the dielectric constant, absolute permittivity, built-in potential, electron charge, and doping profiles of SiGe and Si in equations (12) and (13) the values of the depletion width of the base-collector junction is calculated as:

$$X_{p-SiGe-Base} = \left[\left(\frac{2x12.6x8.854x10^{-12}(\frac{F}{m})(5+0.851)(V)}{100x1.6x10^{-19}(C)}\right)\left(\frac{1x10^{16}(cm^{-3})}{(2x10^{18}(cm^{-3}))^2}\right)\right]^{\frac{1}{2}} = 4.51\text{nm}$$

$$X_{n-Si-Collector} = \left[\left(\frac{2x11.7x8.854x10^{-12}(\frac{F}{m})(5+0.851)(V)}{100x1.6x10^{-19}(C)}\right)\left(\frac{1}{1x10^{16}(cm^{-3})}\right)\right]^{\frac{1}{2}} = 870\text{nm}$$

Thus from the calculated values of the depletion region width, the depletion region width at the base-collector junction of the SiGe NPN transistor is greater that the thickness of the SiGe base in the NPN transistor. The thickness of the SiGe base layer is estimated to be 50nm [40]. Since, Germanium is graded more on the base-collector side than the emitter-base side the

probability of intrinsic absorption is higher, due to the Ge high absorption coefficient than Si at longer wavelengths. Therefore it is desirable to shine incident light at the base-collector junction of the NPN SiGe transistor rather than the emitter-base junction to have high absorption of photons in SiGe semiconductor material.

In order to understand the operation of SiGe phototransistors a device physics of SiGe NPN transistor with the significance of adding Ge is discussed in the next chapter.

4.0 DEVICE PHYSICS OF A SiGe HBT TRANSISTOR

A bipolar transistor is a current controlled device with an internal gain. The base current is related to the emitter and the collector current of the NPN transistor by a current gain (β). This current gain provides amplification in the transistor and therefore it is important to study how various current components in SiGe heterojunction transistor affect its current gain. Due to this gain the design of phototransistors is preferred over photodiodes.

4.1 CURRENT COMPONENTS

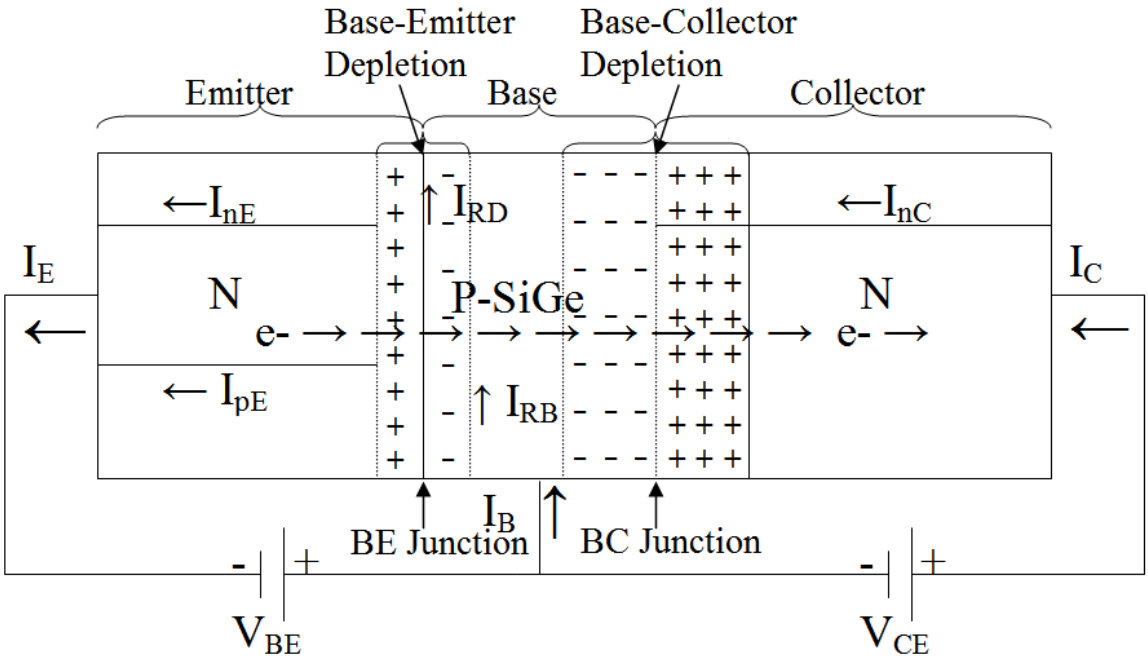


Figure 13 Current components of the IBM NPN SiGe transistor

Figure 13 shows the various current components which flow across the forward-biased emitter-base junction and the reverse biased base collector junction for an NPN transistor in forward active mode. As a result, electrons are injected from the emitter into the base and diffuse towards the collector due to a concentration gradient of electrons in the base. Furthermore, holes are injected into the emitter from the base. The emitter current (I_E) consists of the hole current I_{pE}- crossing from base into emitter and electron current I_{nE}-electron crossing from emitter into base. The ratio of the electrons to the holes crossing the emitter base junction is proportional to the ratio of the conductivity of the N and the P type materials and the conductivity is proportional to the doping concentration. This means, if the doping in a semiconductor is high then the conductivity is high and vice-versa. The electrons flowing from the emitter into the base tend to combine with the holes in the emitter-base depletion region producing current, called the I_{RB}- recombination current, in the base emitter depletion region. In the base, electrons are minority carriers and move only under the influence of diffusion. In the collector, only negligible recombination occurs. The hole current comes from the base and a small fraction recombines in the base region (I_{RB}) as well as in the base-emitter depletion region (I_{RD}). The remaining hole current which reaches the neutral emitter is defined as I_{nE}. This leads to the following components of the emitter, collector and base currents:

$$I_E = I_{nE} + I_{pE} + I_{RD}$$

$$I_B = I_{pE} + I_{RB} + I_{RD}$$

$$I_C = I_E - I_B = I_{nE} - I_{RB}$$

Currents I_{pE}, I_{RD}, I_{RB} should be minimized in order to enhance the collector current of the device. An important figure of merit is the current gain of the transistor (β) expressed as:

$$b = \frac{I_C}{I_B} = \frac{I_{nE} - I_{RB}}{I_{pE} + I_{RB} + I_{RD}} \approx \frac{I_{nE}}{I_{pE}}$$

Emitter Efficiency (γ) is the ratio of the injected carriers at the emitter base junction to the total emitter current as given below:

$$g = \frac{\text{Current of injected carriers at the emitter base junction}}{\text{Total emitter current}} = \frac{I_{nE}}{I_{nE} + I_{pE} + I_{RD}} \approx 1$$

Since the emitter is heavily doped $I_{nE} >> I_{pE}$ therefore, ϒ is nearly equal to 1.

Hence based on the above analysis, SiGe HBT has a high current gain (β) factor for NPN transistors due to high collector current density.

4.2 ROLE OF GERMANIUM IN HETERO-JUNCTION TRANSISTORS

Although the introduction of Ge in the base increases process integration complexity, it offers several advantages over Si based transistors as listed below:

(i) On the addition of Ge in the base of a NPN transistor the base transit time spent by electrons is decreased which results in a higher transit frequency (f_T) performance.

(ii) Ge increases the collector current density and hence current gain of the transistor due to high injection efficiency of the emitter in the NPN transistors. High emitter efficiency is due to high doping of the emitter and a reduction of the base doping.

(iii) The base of the SiGe HBT is doped significantly heavily, as compared to Si transistors, which offers low intrinsic base resistance. Due to this low intrinsic base resistance the maximum oscillation frequency (f_{MAX}) of SiGe HBT is higher than for Si transistors.

(iv) The Early voltage of a NPN transistor is a function of the collector current. Since the collector current is high for collector-emitter voltages due to the reduction of the base width for reverse bias the SiGe HBT has high Early voltage.

(vi) The mobility of electrons in Ge is typically 3900 (cm^2/V-s) which is two times faster than the mobility in Si. Therefore, it is desirable to have a maximum percentage of Ge in SiGe HBT to have high electron mobility and velocity overshoot.

(vii) SiGe has greater radiation hardness due to the use of Radiation and Thermal Processing (RTP). The effectiveness of the RTP depends on the Ge concentration in the source silicon wafers. On the application of the RTP, transistors made on SiGe alloys essentially increase their radiation stability.

(ix) Parasitic capacitance is reduced which increases the maximum oscillation frequency (f_{MAX}).

Thus, a SiGe device offers much higher frequencies and, therefore, very high-speed analog optical receiver circuits can be designed. Our designs and simulation analysis of optical receiver circuit are discussed in Chapters 6 and 7 of this thesis.

5.0 PHOTODETECTORS IN THE IBM SiGe PROCESS

In this chapter an overview of the micro-fabrication steps for the IBM SiGe process is presented. This understanding is necessary to find out the process steps for the formation of NPN SiGe bipolar transistors. Based on this, we can identify which mask layers form the emitter of the NPN SiGe transistor should be removed or changed to build photo-transistor and photo-diode structures.

5.1 OVERVIEW OF THE IBM SiGe PROCESS

IBM's 5HP process stands for "five metal layer high performance" process. This process integrates a SiGe HBT with a 0.5 micron CMOS process manufactured using conventional 200mm silicon wafer CMOS production tools. At present, IBM offers two versions of the SiGe HBT: a standard device targeting high-speed, small signal applications and a high-breakdown device designed for radio frequency (RF) power amplifiers and other analog circuit applications. The key feature of this process is the maximum Ge which is graded in the base of the NPN transistor, giving rise to a transit frequency (f_T) and a maximum oscillation frequency (f_{MAX}) of 47 and 60 GHz respectively. Depending on the application there are five different derivatives of the 5HP process available from the IBM [61]. They are listed as follows:

(i) **SiGe BiCMOS 5HP AM**: This is an analog metal option SiGe process with a thicker last layer of metal (LM) and dielectric, thereby enabling inductors with high quality factor (Q).

(ii) **SiGe BiCMOS 5DM**: This process comes with a dual metal option that offers high inductor and capacitor density by adding a copper metal level under the analog metal (AM) level.

(iii) **SiGe BiCMOS 5PA**: This process is suited for applications requiring high voltage capability and high linearity for use in power amplifiers.

(iv) **SiGe BiCMOS 5S**: This process is desirable for high performance solutions in storage, communications, and mixed-signal consumer applications.

(v) **SiGe BiCMOS 5HPE**: This integrates a high-speed, 43GHz SiGe HBT with a 0.35micron CMOS process for high performance transistors with low power consumption.

At the time of this investigation of photodetectors, the IBM 5HP high performance process was the only commercially available SiGe process through MOSIS for three metal layers only. The IBM SiGe Design Kit^{TM} is a set of files provided by MOSIS to design and layout circuits in the Cadence environment. It consists of the library of devices, models, Design Rule Checker (DRC), Layout Versus Extraction (LVS), and a full Spectre models for devices like gate lateral PNP transistors, polysilicon transistors, Metal-Insulator-Metal (MIM) capacitors, Schottky barrier diodes, varactor diodes, Electro-Static Discharge devices (ESD), resistors (NS, RN, and RI), and LM and wire bond-pads.

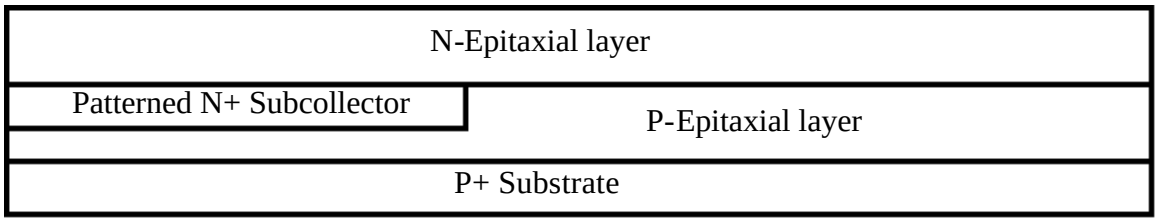
5.2 MICRO-FABRICATION STEPS FOR THE IBM SiGe 5HP PROCESS

The following steps are illustrative of the fabrication steps in IBM's SiGe process [36, 62]:

Step: 1 Formation of a starting stock

(i) The starting wafer is P+ substrate coated by a thin P-epitaxial layer.

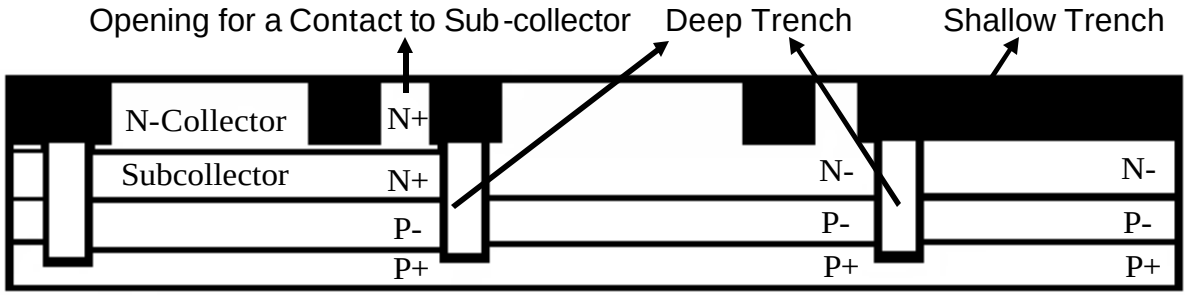
(ii) In the next step the P-epitaxial layer is patterned to grow the N+ sub-collector followed by a thin N- epitaxial layer which is grown everywhere.



Step: 2 Formations of shallow trench /deep trench isolation

(iii) After accomplishing step 1 a PolySilicon-filled Deep Trench (PST) and an oxide filled shallow trench is implemented for noise isolation.

(iv) Following deep trench isolation an opening for a contact to the sub-collector is created. Later, this contact is achieved by the process of deep phosphorous diffusion.

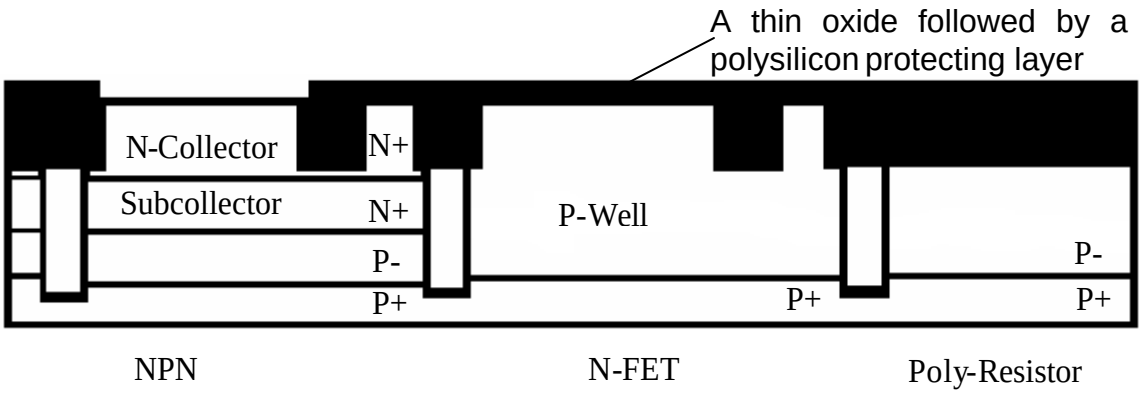


Step: 3 Formation of a N-P-N active area for SiGe HBT

(v) In this step implantation of the N-well and P-well takes place. The P-well and N-well is formed for FET and bipolar devices respectively followed by annealing.

(vi) A thin gate oxide of ~7nm is grown all over the surface followed by a thin deposition of a polysilicon layer. The polysilicon layer is deposited to protect the gate of the FET device.

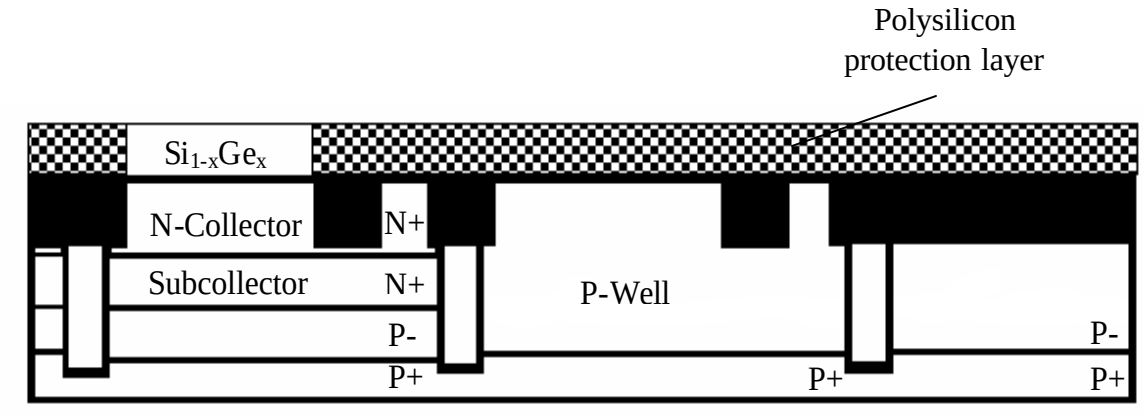
(vii) A gate protect polysilicon layer over the N-P-N active area region is patterned and removed by RIE, Reactive Ion Etching.



Step: 4 Formation of a SiGe layer by Ultra High Vacuum/Chemical Vapor Deposition

(viii) Exposed polysilicon and silicon surfaces are hydrogen passivated and SiGe is grown by the UHV/CVD process.

(ix) The deposition of SiH_4 in the UHV/CVD process naturally results in the deposition of polysilicon over the oxide field region and epitaxial silicon over the active device region. Note that the deposition of polysilicon over the oxide field region serves as a natural extrinsic base electrode.



Step: 5 Emitter pedestal formation for the emitter of SiGe HBT

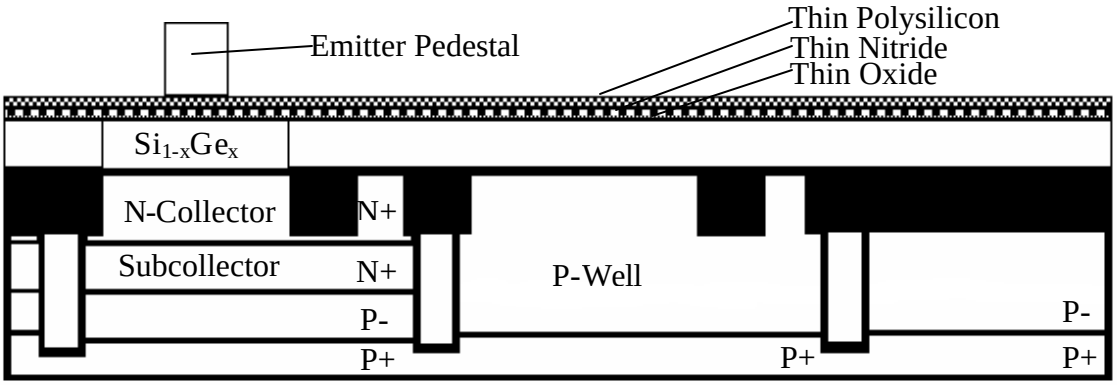
(x) Following base deposition a passivation oxide layer is grown using low temperature HIPOX

(xi) A thin layer of nitride is grown, followed by a thin layer of polysilicon.

(xii) An Emitter "Mandrel" is completed followed by PECVD nitride and PECVD oxide.

(xiii) The emitter window is defined as a lithographic pedestal and etched into an oxide/nitride stack stopping on the conversion layer polysilicon

(xiv) A highly conformal oxide spacer formed on the mandrel serves to space a high dose extrinsic base boron implant away from the emitter opening in a self aligned manner.

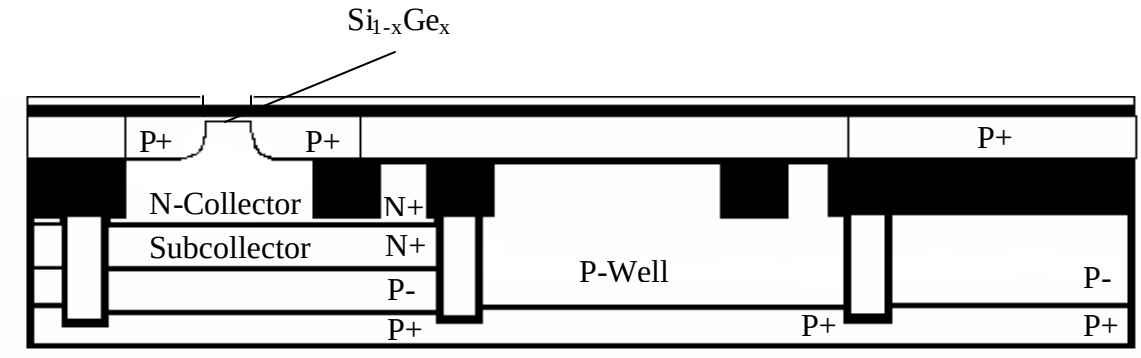


Step: 6 Opening for the emitter

(xv) After forming the emitter mandrel and leaving behind the nitride pad which defines the final emitter window, the emitter stack is removed.

(xvi) Using low temperature HIPOX oxidation and nitride emitter pedestal as a local mask for oxidation barrier, the polysilicon over the implanted extrinsic base and over the field oxide regions is converted completely to oxide.

(xvii) After converting polysilicon to oxide the nitride is removed exposing the unconverted polysilicon plug.

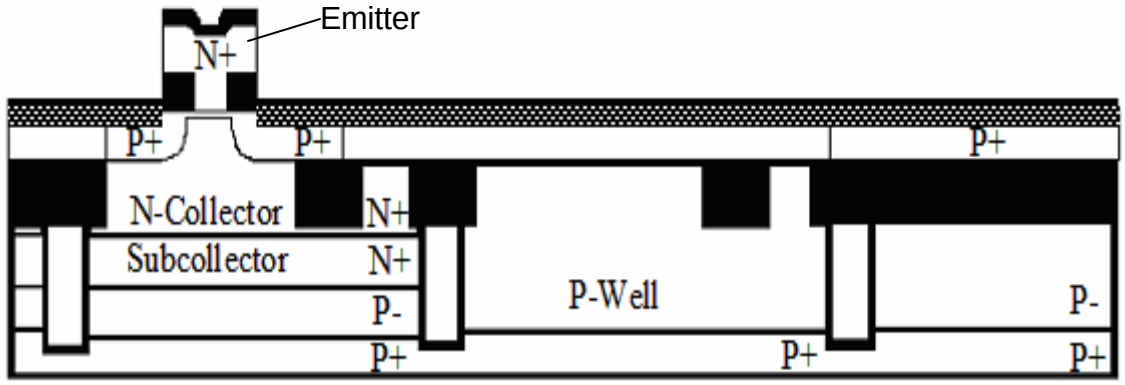


Step: 7 Emitter poly-deposition and ion implantation

(xviii) The final fabrication steps involve the deposition, implant and annealing of the emitter polysilicon layer.

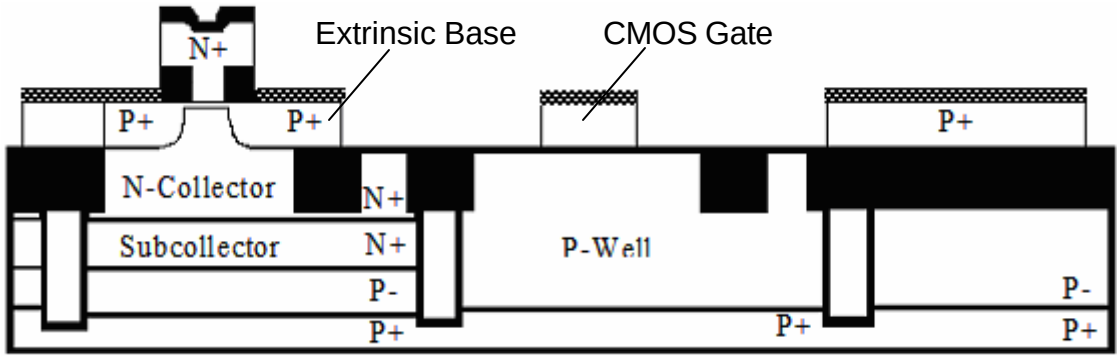
(xix) After a final HF dip, the emitter polysilicon is deposited and ion implanted with arsenic, capped with silicon nitride, and patterned with an etch that stops on the dielectrics over the base region

(xx) The emitter is doped with implanted arsenic



Step: 8 Formation of the extrinsic base and gate etch

(xxi) After emitter formation, the extrinsic base, CMOS gate and poly-resistors are all patterned and etched together.



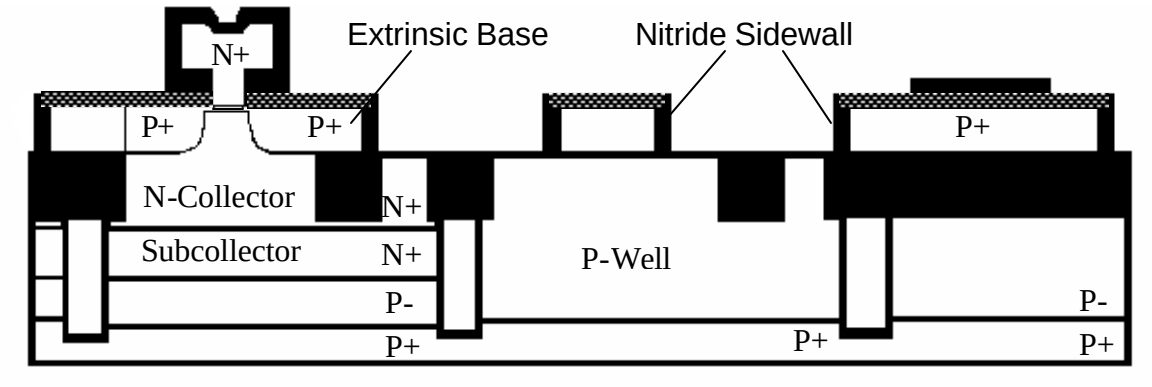
Step: 9 Poly-re-oxidation, nitride side wall

(xxii) At this stage the emitter is doped with implanted arsenic and the extrinsic base and polysilicon resistors are all doped with implanted boron.

(xxiii) The emitter remains capped with nitride to prevent dopant loss and prevent silicidation. Ambient oxygen is used for the emitter furnace anneal to re-oxidize the gate and extrinsic base side walls.

(xxiv) A nitride sidewall is formed on the FET gates and the extrinsic base using reactive ion etcher is used to etch back a deposited nitride layer.

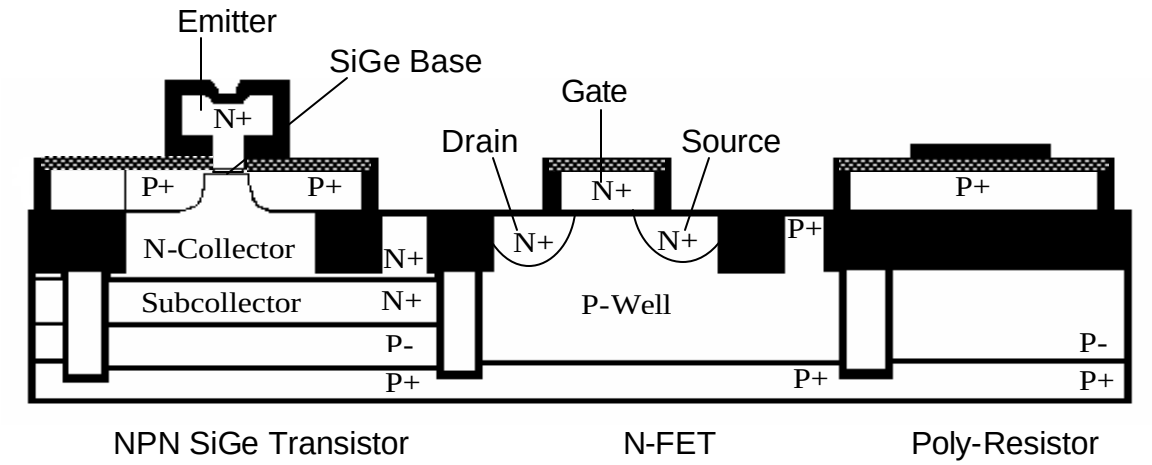
(xxv) The nitride sidewall is formed over the emitter, base, gate and resistors.



Step: 10 Formation of FET Source, Drain, Gate by ion implantation

(xxvi) A dual poly process that simultaneously dopes the Source, Drain, and Gate is used for FET devices.

(xxvii) In the last step, salicide is formed all over the surface as a protective coating.



5.3 CROSS SECTION OF AN IBM NPN PHOTOTRANSISTOR

An overview of building photodetector in the IBM SiGe process has already been discussed in section 2.2.

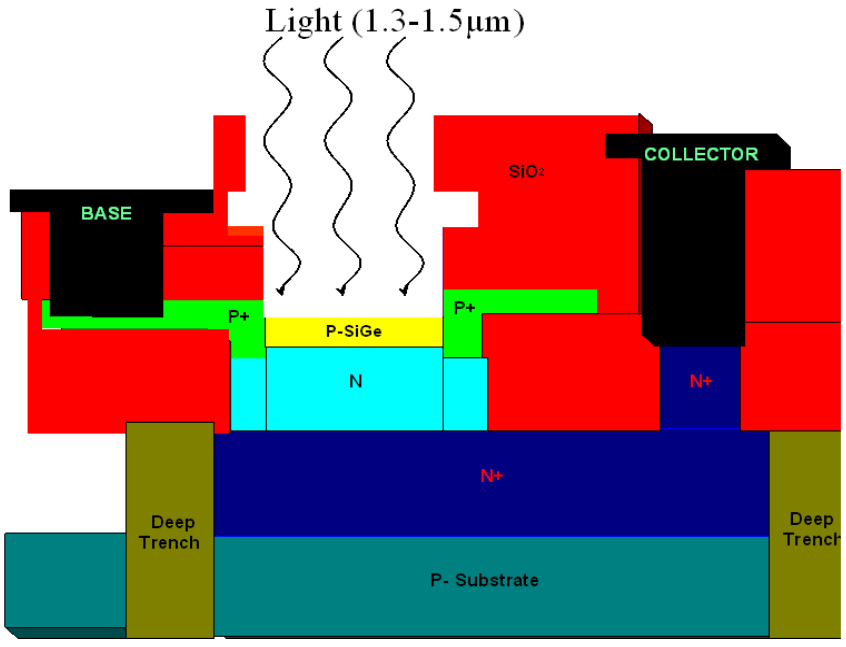


Figure 14 Cross section of the IBM NPN transistor with emitter removed

The basic idea of using IBM NPN SiGe transistor as a photodetector and photodiode is shown in the cross section of the IBM SiGe NPN transistor in Figure 14. Light falls on the base of the transistor which generates an electron hole pair in the depletion region on the base collector junction. In order for conduction to take place an electron from the valence band is made to jump to the conduction band where it starts conducting. Since the base-collector junction is reverse biased, those electrons are attracted towards the positive side of the supply voltage forming the collector current on the output side of the collector.

Figure 14 shows a cross section view of the NPN hetero phototransistor with the emitter removed and light is shinning directly on the base of the transistor. The photons are absorbed in the base and the collector region. For every one photon there is one electron-hole pair generated in the base, base-collector depletion region, and within the bulk collector. On the application of suitable reverse bias to this device, an electric field is generated which separates the photo-generated electron-hole pair. The electrons in the collector region are collected by the field of the base-collector junction, leading to the current flow in the external circuit. The holes that are generated in these regions are swept into the base, thereby increasing the base potential. This in turn increases the base-emitter forward bias. A large number of electrons that are injected from the emitter into the base are collected in the collector.

If the depletion region penetrates a distance W_1 in to the p-type region and W_2 in to the n-type region, then we require $W_1 N_{A\ (p\text{-}SiGe\text{-}type)} = W_2 N_{D\ (n\text{-}type)}$. This is because the total charge per unit area on either side of the junction must be equal in magnitude but opposite in sign. The depletion region will have a smaller area with high doping, therefore in the transistor shown in Figure 15 the width of the depletion region at the base collector junction is small on the base side and larger on the collector side.

Figure 15 also shows different profiles of Ge concentration in the base of the NPN transistor [63-68]. There are three possible doping profiles of Germanium in the base of the NPN transistor: uniform, trapezoidal and triangular. The triangular profile is important due to two reasons: First, it has the maximum percentage of Ge in the base of the NPN transistor. Second, for reverse bias, the depletion region width is greater on the base-collector junction than the base-emitter junction and Ge is graded more on the collector side than the emitter side. Therefore the probability of absorption of photons is greater on the base-collector junction than the emitter-base junction.

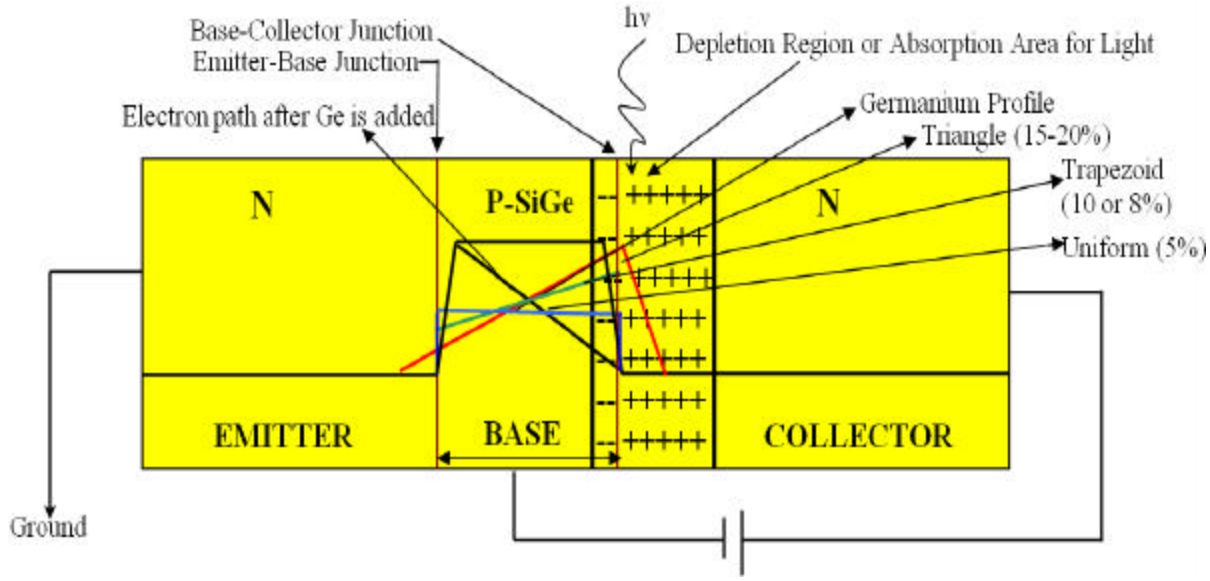


Figure 15 Planar view of NPN transistor showing different profiles of Germanium

5.4 DESIGN AND FABRICATION OF AN IBM SiGe PHOTODETECTOR

The photodetector designs were based on a SiGe NPN layout parameterized cell from the IBM design kit. After carefully studying the fabrication process it was determined that two mask layers were responsible for making the emitter of the NPN transistor. The first layer creates the base/emitter mandrel, which is removed later to create the access hole for the base in the

oxide/nitride/oxide insulation layer. Afterwards a second mask builds the emitter polysilicon above the base. It was seen in Figure 14 how the emitter cap above SiGe base is removed and the light is shined directly on the base of the NPN transistor. Based on this idea, several layout versions of photodetectors were created in which the emitter is partially or fully removed. The work on the layout of photodetectors was carried out by Leo Selavo, a graduate student of the Department of Computer Science at the University of Pittsburgh.

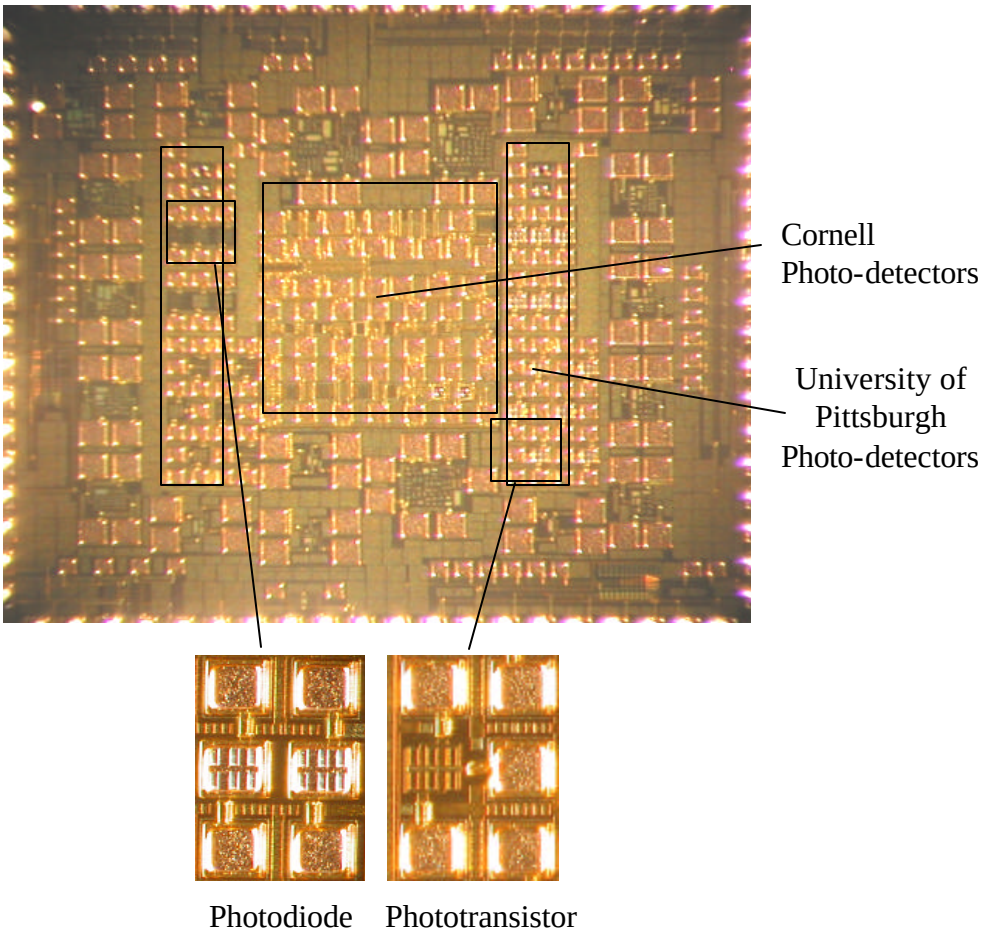


Figure 16 SiGe photo-receiver chip showing several SiGe based photodetector structures

(Photos Courtesy of Leo Selavo, Department of Computer Science)

Another set of photodetector test structures were designed and laid out at Cornell University. These researchers proposed to post-process the chip die by etching holes above the

photodetectors. Figure 16 shows a micro photograph of the designed and fabricated SiGe based photodetectors in the IBM process.

6.0 TRANSIMPEDANCE AMPLIFIERS

It has been already seen in section 3.8 that the responsivity or the output current of a $Si_{0.80}Ge_{0.20}$ photodetector is in the range of micro-amps for an input power of 1mW at the optical wavelength range between 900-1150 nm. Therefore, it is very essential to have a front-end circuit architecture with high conversion efficiency, high sensitivity, high bandwidth, and high gain. The transimpedance amplifiers (TIA) have such characteristics [69].

The transimpedance amplifier is a current to voltage converter. The key feature of the transimpedance amplifier design is that a feedback resistor (R_f) in the design controls the current to voltage conversion by affecting the gain and bandwidth of the transimpedance amplifier. Virtually all optical receiver designs are based on transimpedance amplifiers since optical detectors produce currents in response to incident light. In this chapter, fourteen transimpedance configurations based on different designs are simulated in the IBM SiGe process with an assumed minimum input current of 10μamps. The focus in this chapter is to study these transimpedance amplifier designs in terms of gain and bandwidth.

6.1 FRONT-END ARCHITECTURE OF RECEIVER CIRCUIT

The selection criteria used to build the front-end circuit architecture of an optoelectronic receiver is as follows:

First, we considered the possibility for the type of amplifier used to build optical receivers. We found that typically the front-end design can consist of one of three basic configurations a) Low impedance amplifier b) High impedance amplifier c) Transimpedance

amplifier, as shown in Figure 17. The three configurations have different characteristics which are best suited to a particular application. These configurations [69] are given as follows:

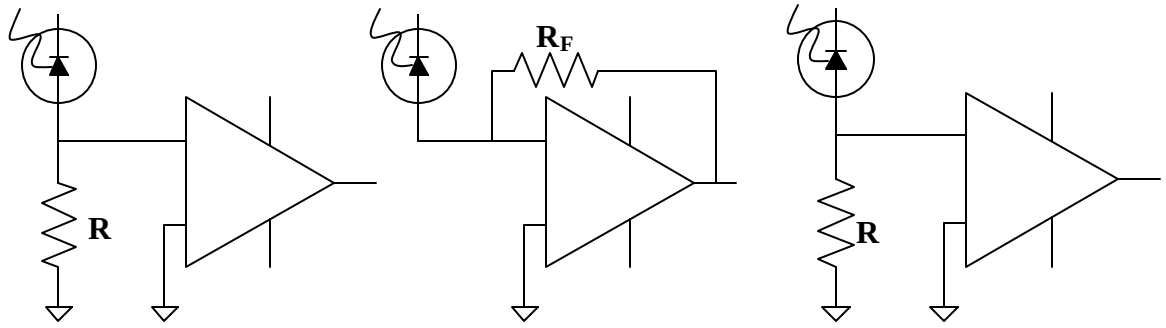


Figure 17 **Different front-end amplifier configurations for an optical receiver**

(i) The low impedance amplifier has a low value of the bias resistor (R). This low value of the resistor (R) ensures that the receiver has a wide bandwidth and a dynamic range of input resistance, but it also has a high noise level. This high noise level is due to the low value of the resistance.

(ii) The high impedance amplifier has a high value of the input bias resistor and produces significantly less noise, but the dynamic range of the receiver is relatively narrow and equalization is necessary after the amplifier to achieve a useful bandwidth.

(iii) The transimpedance amplifier, with the use of negative feedback, provides a useful compromise, giving a relatively broad bandwidth and dynamic range, as well as good noise performance.

Since transimpedance amplifiers have both the low-noise characteristics of high impedance amplifiers and the wide dynamic range of low impedance amplifiers, circuits based on this architecture were investigated.

Second, on selecting transimpedance the amplifier as the front-end circuit architecture for optical receiver transimpedance amplifiers, designs based on other custom SiGe processes like

MAXIM [70] were selected. The circuit topologies selected were re-designed and implemented in the IBM process to compare their individual respective performances.

Third, SiGe processes exhibiting the same transit frequency (f_T) and maximum oscillation frequency (f_{MAX}) as the IBM SiGe process were selected. The maximum oscillation frequency (f_{MAX}) is an imperative parameter of the SiGe process considered for the circuit environment. It is defined as the frequency at which the unilateral power gain becomes unity. It depends on the unity gain cut-off frequency (f_T) which is defined as the frequency at which the common emitter short circuit AC current gain becomes unity. These two frequencies determine the bandwidth of an amplifier. Therefore circuit topologies exhibiting almost the same transit frequency (f_T) and maximum oscillation frequency (f_{MAX}) as the IBM SiGe process were selected to compare their gain and bandwidth performance.

Fourth, in order to determine the utility and capability of the analog mixed signal CAD tools simple circuit topologies based on transimpedance amplifiers were designed. Analog tools from NeoCircuit/NeCell Neolinear Inc. and Spectre simulator from Cadence Inc. were provided to optimize and simulate these transimpedance amplifier designs.

6.2 CIRCUIT TOPOLOGIES OF TRANSIMPEDANCE AMPLIFIER

The transimpedance amplifier converts an input current from the photodetectors into a voltage typically in the range of millivolts. The key components which form the transimpedance amplifier is the use of a negative feedback between the output and input of the amplifier. This is employed for three main reasons [71]:

(i) It reduces distortion and makes the performance of the amplifier less dependent on transistor parameters.

(ii) It is used to extend the frequency response of the amplifier.

(iii) It is used to give the amplifier the desired values of the input and the output impedance and to provide DC stability over a range of operating conditions.

Based on the idea of negative feedback several transimpedance amplifier circuits were designed. These circuits were built and optimized using NeoCircuit/NeoCell analog mixed signal design synthesis tools and simulated using Spectre in the Cadence Affirma analog design environment. A pre-layout simulation of these TIAs will be discussed with respect to their feedback (R_f) values in this section. Later, post-layout simulation of the same TIAs is performed including parasitic resistances and capacitances after verifying the Design Rule Check (DRC) and Layout Versus Schematic (LVS) using DIVA. In this section, the focus is on the design aspect of the transimpedance amplifiers and how the use of negative feedback resistor (R_f) provides a useful compromise between gain and bandwidth.

Circuit topologies of transimpedance amplifier (TIA#1 – TIA#8) are based on a concept of using the first stage, a common emitter amplifier, as a current amplifier provided by an NPN SiGe transistor, followed by multiple cascaded stages of common emitter amplifiers with a feedback resistor (R_e). The other stage used is an emitter follower NPN transistor which acts as a buffer or voltage amplifier for the output stage. The comparison of common emitter, a common base, common collector amplifier stage is shown in Table 6. TIA#9-TIA#14 were selected and implemented in the SiGe IBM process to compare the performances of other custom SiGe and GaAs processes.

Table 6 Properties of different amplifier configuration for NPN transistor

Parameter	Common Emitter	Common Base	Common Collector
Input Resistance	Low (1KΩ)	Very Low (20Ω)	High
Output Resistance	High (40KΩ)	Very High (1MΩ)	Low
Input Current	I_B	I_E	I_B
Output Current	I_C	I_C	I_E
Current Amplification	ß= I_C/I_B	a=I_C/I_E	I_E/I_B
Current Gain	High	Less than unity≈0.99	High
Voltage Gain	Medium	Medium	Low

An AC analysis and transient analysis was performed for each simulated transimpedance amplifier as shown in section 6.2.1 to 6.2.14. The AC analysis provides the investigation for the small signal behavior of the transimpedance amplifier. The frequency response shows the gain and the bandwidth of the amplifier under DC bias stability conditions. The transient analysis most closely simulates the phenomena seen in the real circuit is preceded by DC analysis for the initial conditions.

Each of the modules of the optical receiver is fabricated individually and each TIA is simulated independently in order to detect their gain and the bandwidth with an assumed input current of 10µA. Since each test structure of TIA is simulated autonomously, no effect of capacitance from the photodetector on transimpedance amplifier is observed and therefore, the affect of the stray capacitance is neglected in the simulation. The gain peaking effect is observed in the transimpedance amplifiers. This is due to the intrinsic capacitance associated with the TIAs.The details of the circuit topology followed by AC analysis, transient analysis with layout of transimpedance amplifiers TIA#1-TIA #14 is discussed in this section. These transimpedance

amplifiers are simulated using Spectre in the Cadence environment and optimized using the analog synthesis tool NeoCircuit from Neolinear Inc.

6.2.1 Transimpedance Amplifier # 1

Figure 18 shows the circuit topology of the basic transimpedance amplifier. The TIA#1 circuit consists of a common emitter amplifier provided by NPN transistor Q1 as the input stage, which is used as a current amplifier. The feedback resistor (R_f) is applied between the base and the collector of the NPN transistor Q_1. This feedback has the effect of reducing the input resistance of the amplifier and is used as the input stage of the current amplifier. The feedback R_f decreases the output resistance of the amplifier [71]. In order to determine the small signal gain of the transimpedance amplifier, DC bias currents and voltages in all the branches of transistor Q1 need to be evaluated. The DC analysis of TIA#1 is illustrated in Figure 18 and calculated as follows:

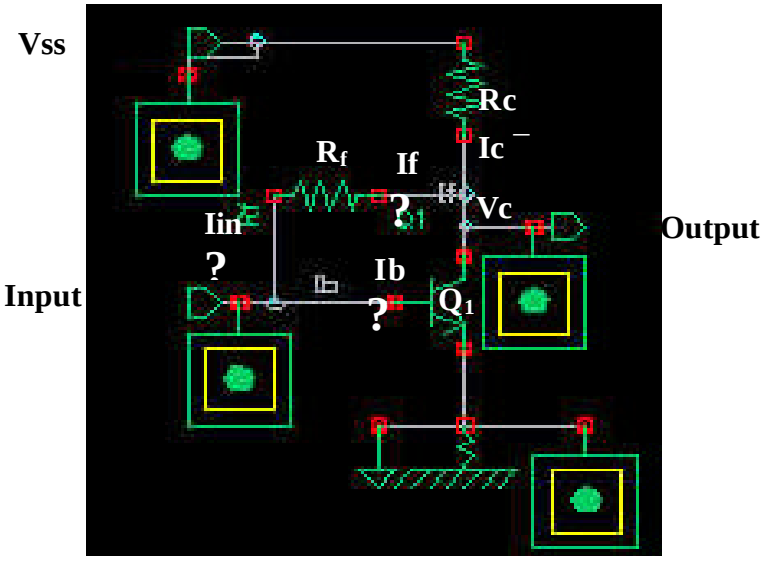


Figure 18 Tansimpedance amplifier #1- Circuit topology

Let the voltage and the currents at the emitter, base, and collector junction of NPN transistor Q1 be V_E, V_B, V_C and I_e, I_b, I_c respectively. Due to potential difference between the voltage at the collector and the base of transistor Q1 we can express:

$$V_C - V_B = I_f x R_f \tag{14}$$

Equation (14) can be rewritten as:

$$V_C = V_B + I_f x R_f \tag{15}$$

Also from the current relationship for a bipolar junction transistor [72], the current in a collector of a transistor Q1 can be expressed as $I_c = \alpha I_e$

$$I_c = \alpha \,.\, (1+\beta)\, I_b \tag{16}$$

Thus using equations (15) and (16) the transistor DC operating point can be found. On finding the DC operation points the AC analysis of TIA#1 can be summarized as follows.

Let the current flowing in the base of NPN transistor Q1 be I_b, then the current flowing in the collector is βI_b, thus the voltage at the collector with load resistance R_c is $V_c = \beta I_b R_c$. Therefore the current in the feedback R_f resistor is $I_f = \beta I_b Rc/R_f$. Also $I_{in} = I_b + I_f = I_b + \beta I_b R_c/R_f = I_b (1 + \beta R_c/R_f)$. If R_f is removed then the input current is simply I_b whereas if R_f exists then it has the effect of reducing the input resistance by the factor $1/ (1+\beta R_c/R_f)$ of its former value. If R_f is small as compared to βR_c then the input resistance is given as $R_b/\beta R_c$. Therefore the small signal AC gain of TIA#1 is given as the ratio of the output voltage to input current which is approximated as follows:

$$\frac{OutputVoltage}{InputCurrent} = \frac{bI_b R_c}{I_b\left(1 + b\,\frac{R_c}{R_f}\right)} \approx R_f$$

This shows that to a first approximation the amplifier gain is independent of the transistor parameters and depends on the feedback resistance (R_f) [71]. The -3dB frequency for an ideal transimpedance amplifier is given as [73]:

$$f_{3dB} = \frac{1}{(2pR_f C_f)} \tag{17}$$

Where R_f is the feedback resistance (Ω) and C_f is the stray capacitance associated with the negative feedback network.

Equation (17) is the expression for a cut-off frequency of an ideal operational amplifier, but practically, no amplifier is ideal and it has losses. The gain peaking which occurs in most of the frequency analysis of the transimpedance amplifiers occurs due to the capacitance associated with the photodetectors. This gain peaking can be reduced by increasing the value of the capacitance (C_f). But increasing the value of the capacitance decreases the bandwidth of the transimpedance amplifier for a fixed value of feedback resistance (R_f). Therefore for a fixed value of capacitance, the value of feedback resistor can be changed to get desirable bandwidth, gain, low noise and input and output impedance.

Figure 19 and Figure 20 show the transient and the AC analysis response of the pre-layout and post-layout simulation of TIA #1 at 10GHz with an input current of 10μamps. The post-layout simulation includes all the parasitic resistance and capacitance. Figure 21 shows the circuit layout of TIA#1 with input, output, ground and the power supply.

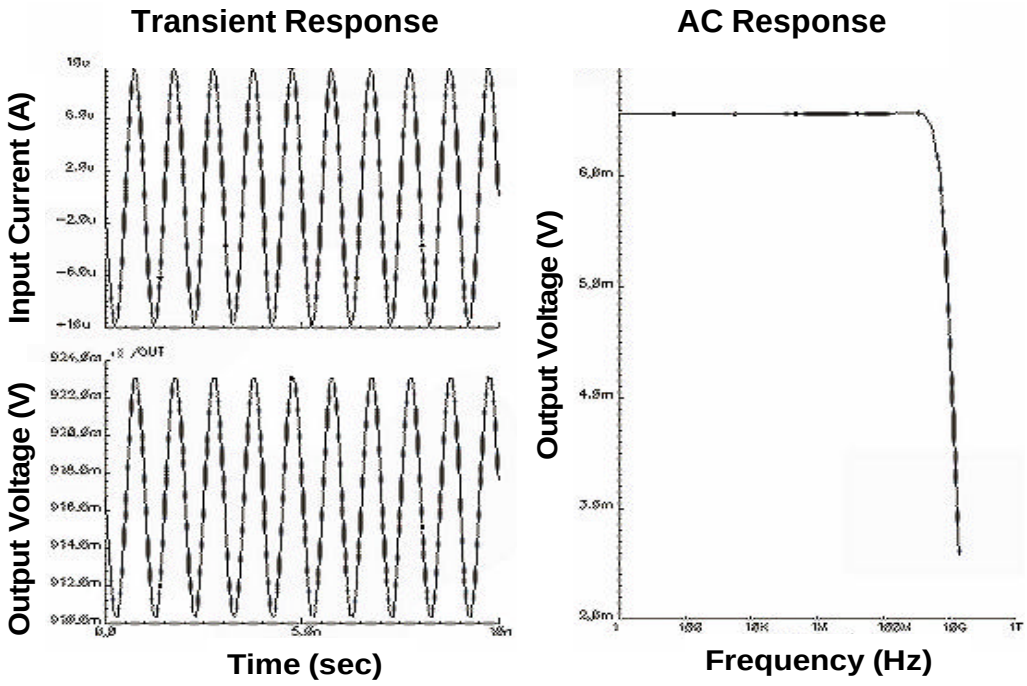


Figure 19 Pre-layout simulation result of TIA#1 at 10GHz

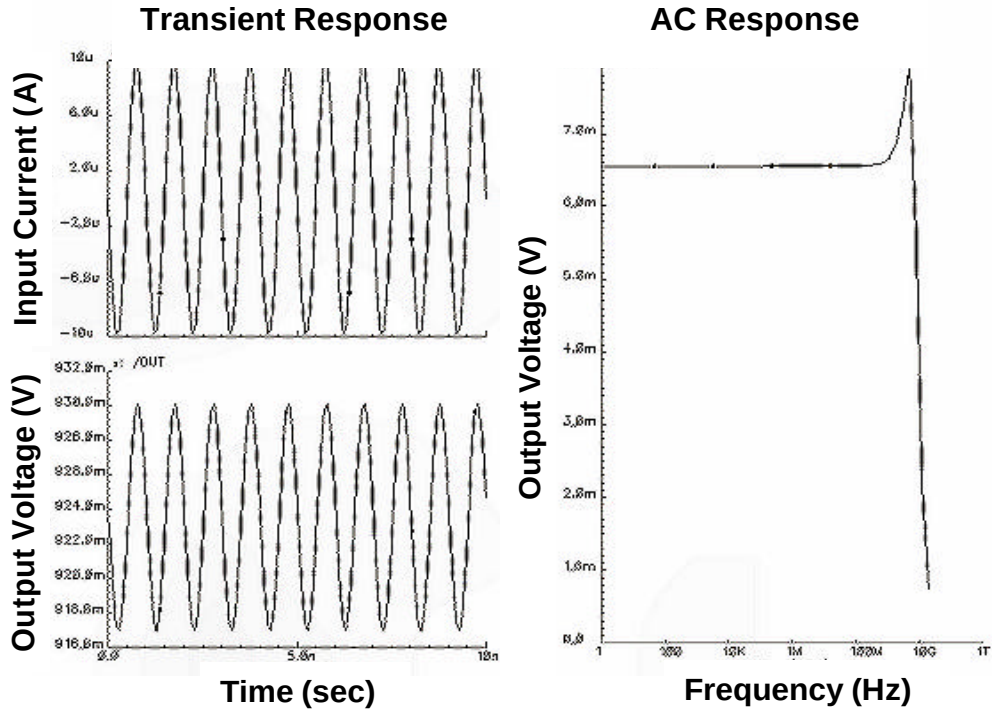


Figure 20 Post-layout simulation result of TIA#1 at 10GHz with I/O Pads

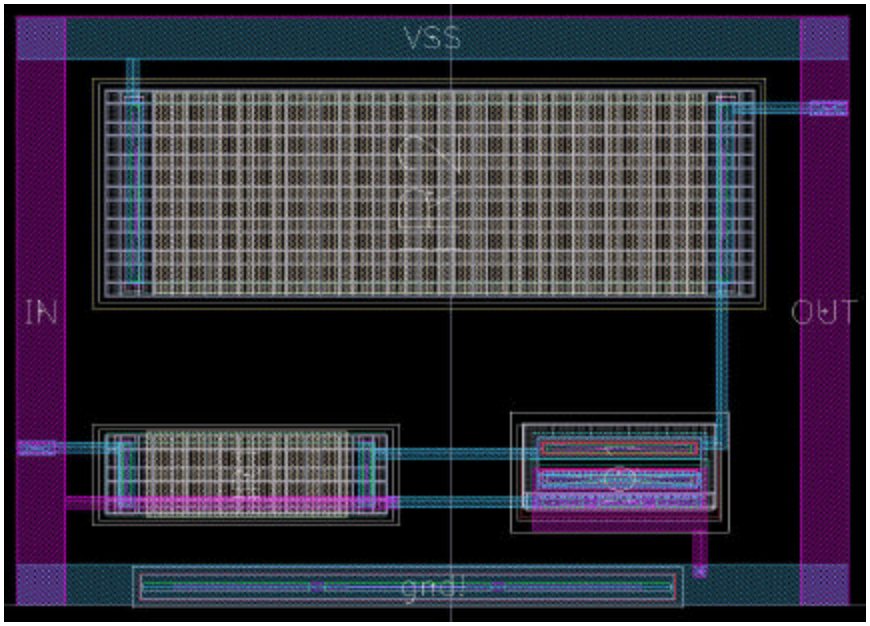


Figure 21 Circuit layout of TIA#1 with I/O Pads

6.2.2 Transimpedance Amplifier # 2

The circuit topology of a TIA#2, as shown in Figure 22, is composed of TIA#1 followed by an NPN transistor Q2 as a common emitter stage with a feedback resistor (R_e). This kind of feedback amplifier is known as series-series feedback amplifier [71]. With the addition of the second common emitter stage provided by NPN transistor Q2 the output gain and the bandwidth of the transimpedance amplifier increases due to the high input and the high output impedance of the second stage [71]. This high input and output impedance is desirable so that the output voltage of the first common emitter stage Q1 is amplified to give output current. There is not much gain achieved by the use of feedback resistance R_e but the addition of the feedback resistance Re increases the bandwidth of the transimpedance amplifier [71]. The final stage is a common collector stage provided by NPN transistor Q3 that acts by buffering the output to the next stage.

Figure 23 and Figure 24 show the pre-layout and post-layout simulation for TIA#2 demonstrating the increase in the output gain from 6mV in TIA#1 to 15mV in TIA#2. This output gain is due to the use of the second amplifying stage Q2. Figure 25 shows the circuit layout view of TIA#2 with input, output, power supply and the ground.

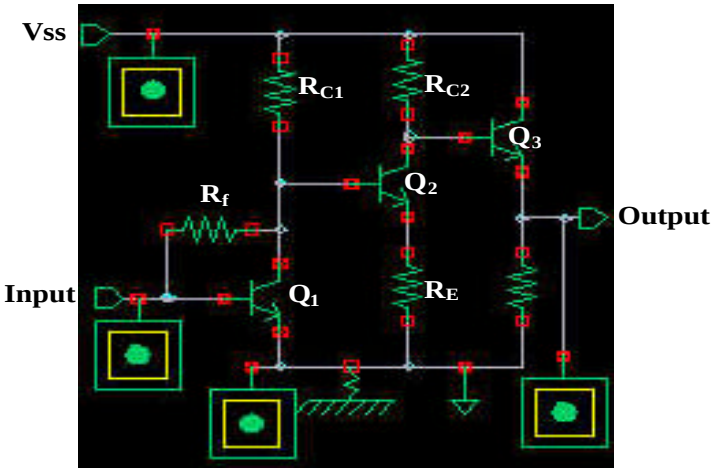


Figure 22 Tansimpedance amplifier #2- Circuit topology

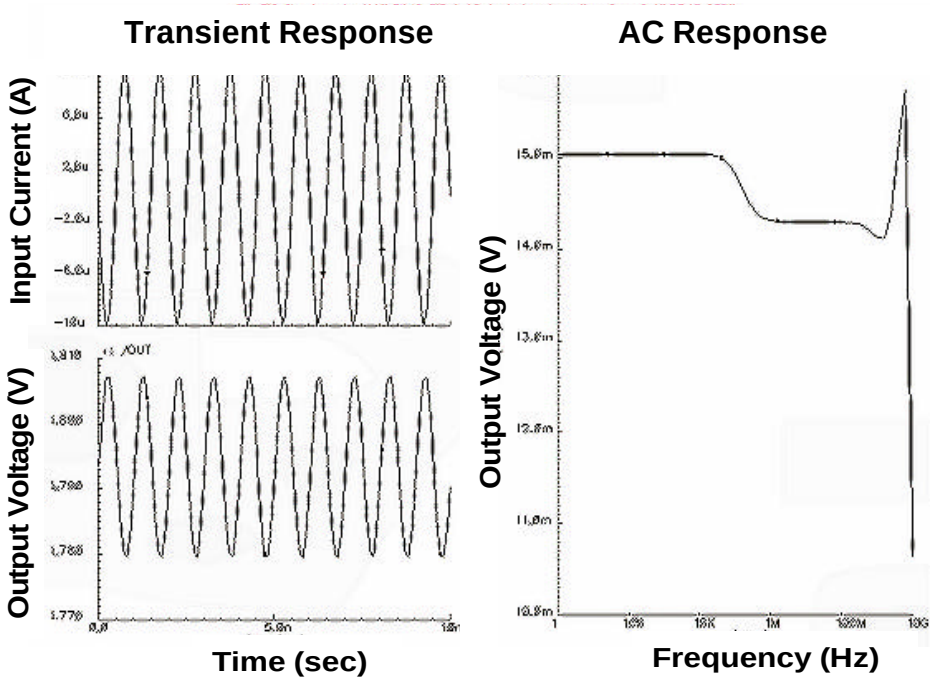


Figure 23 Pre-layout simulation result of TIA#2 at 10GHz

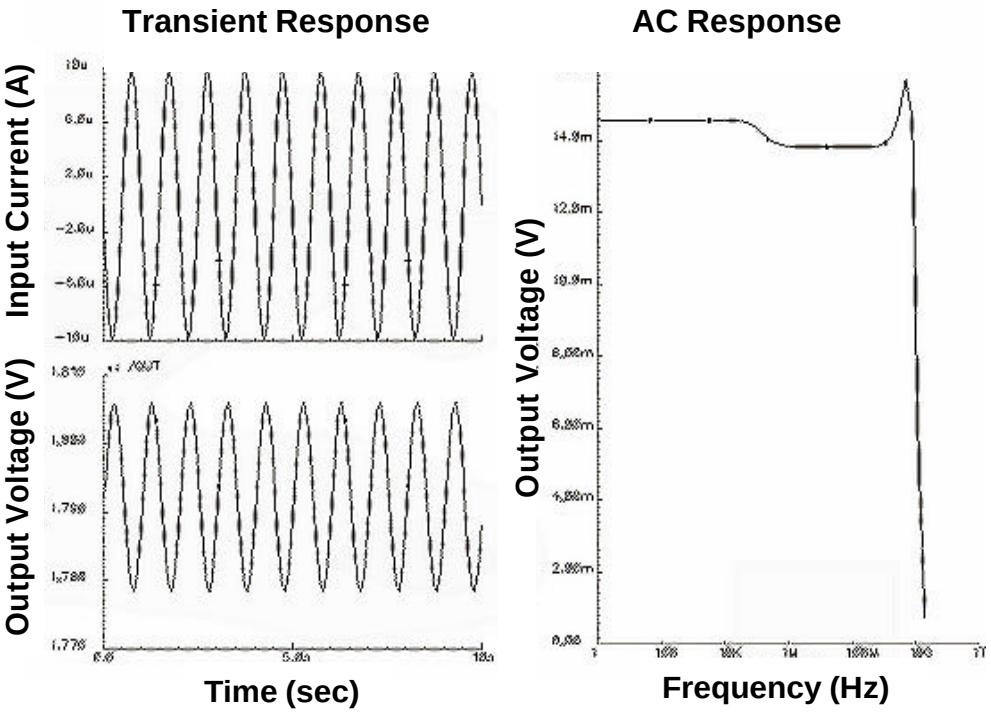


Figure 24 Post-layout simulation result of TIA#2 at 10GHz with I/O Pads

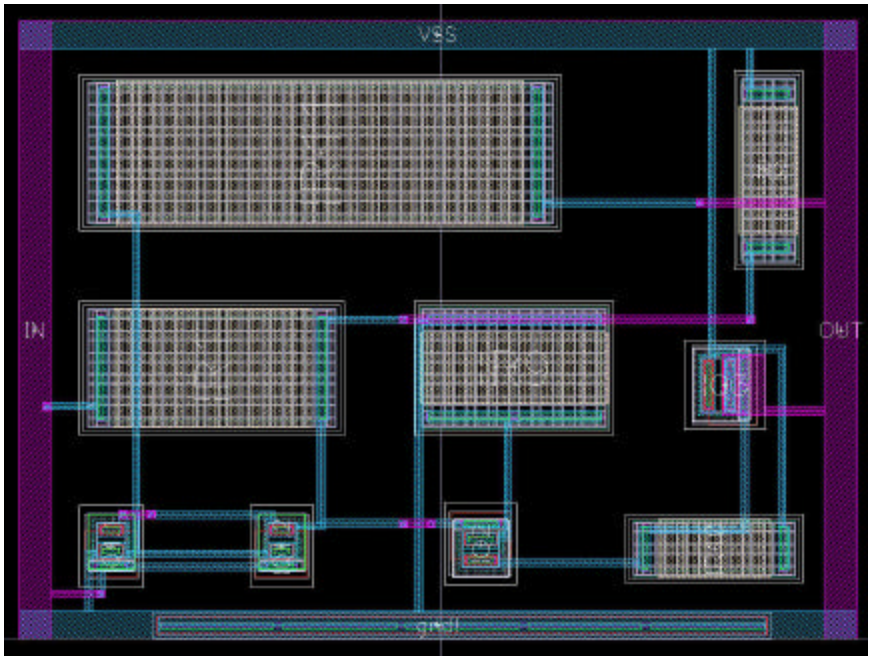


Figure 25 Circuit layout of TIA#2 with I/O Pads

6.2.3 Transimpedance Amplifier # 3

The Circuit topology for TIA#3 is shown in Figure 26. It consists of a two stage current amplifier in which the feedback resistor (R_f) is connected to the emitter of the second NPN transistor Q2 instead of connected to the collector of NPN transistor Q1 like TIA#1. The basis for this is due to the fact that voltage at the collector of Q1 is essentially the same as the voltage of emitter of the transistor Q2. This is shown as follows $V_{C1} - V_{BE2} = V_{B2}$ or $V_{C1} - V_{B2} + V_{E2} = V_{B2}$ or $V_{C1} + V_{E2} = 2V_{B2}$ and since the potential at the collector of Q1 is equal to the potential at the base of Q2 we can simply say that $V_{E2} = V_{C1}$. In fact, it is better to use the feedback from the emitter of the second stage Q2 since it reduces any distortion arising due to the inter-transistor DC coupling capacitor at high frequencies [74]. The approximated overall small signal gain for this TIA#3 stage is R_b/R_e which is also independent of the transistor parameters. This TIA is considered better than TIAs discussed since an output of 19mV is achieved for an input current of 10µA by taking the feedback from the second stage Q2. The pre-layout simulation, post-layout simulation and the circuit layout is shown in Figure 27, Figure 28 and Figure 29 respectively.

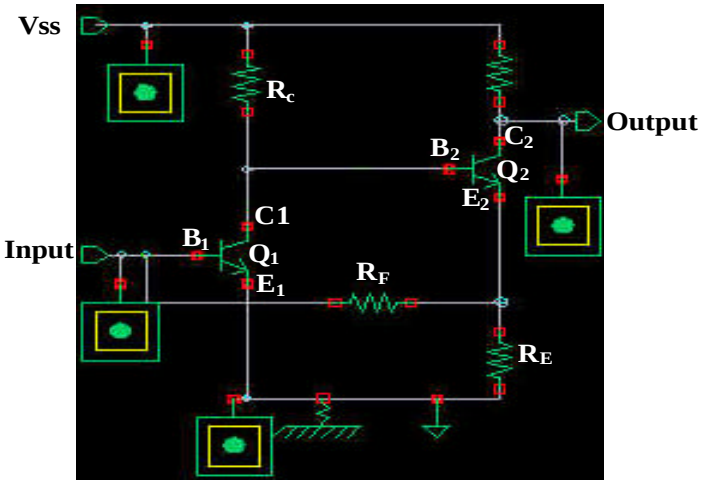


Figure 26 Tansimpedance amplifier #3- Circuit topology

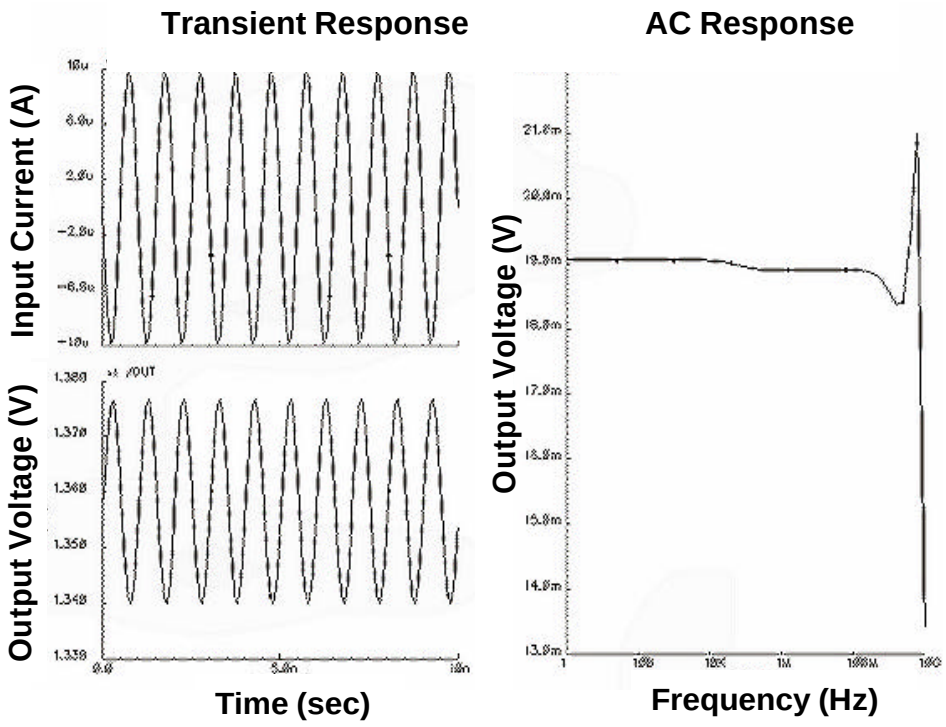


Figure 27 Pre-layout simulation result of TIA#3 at 10GHz

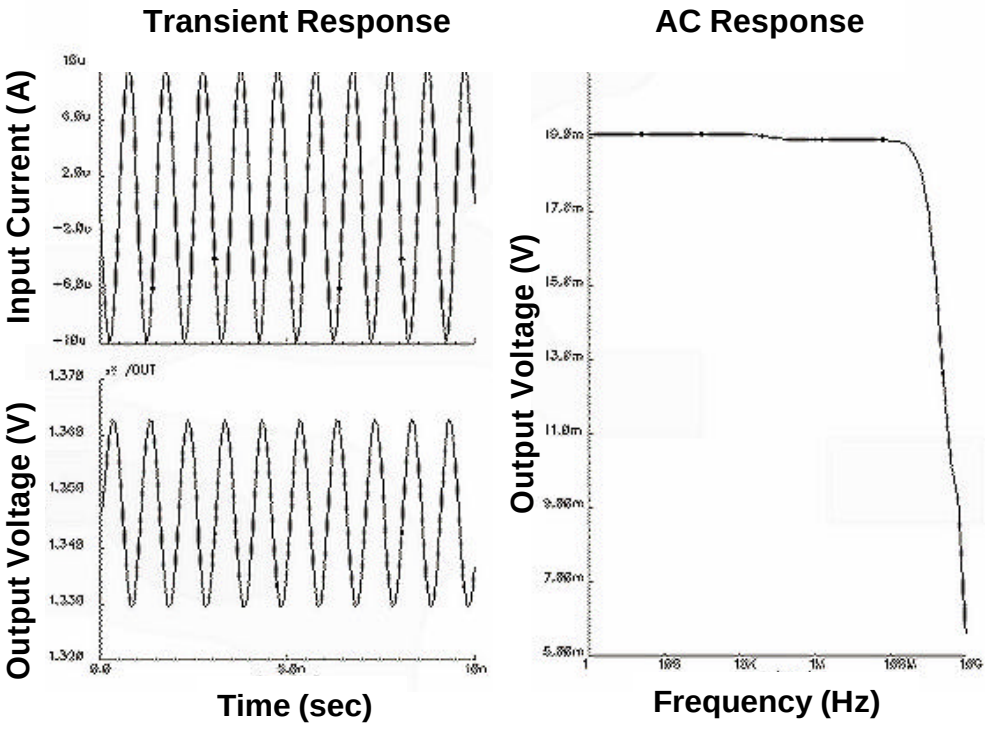


Figure 28 Post-layout simulation result of TIA#3 at 10GHz with I/O Pads

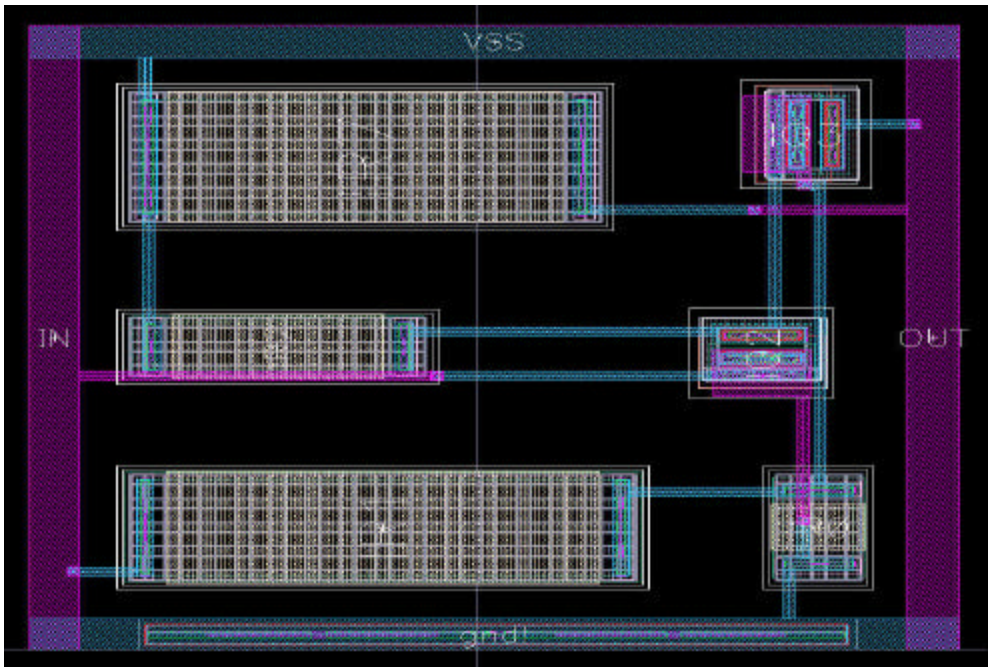


Figure 29 Circuit layout of TIA#3 with I/O Pads

6.2.4 Transimpedance Amplifier # 4

The Circuit design of TIA#4, as shown in Figure 30, is based on the same idea as TIA#3 except that transistor NPN Q2 is biased differently by removing the resistor connected between the collector of NPN transistor Q2 and the power supply Vss. On removing this resistor the second stage behaves like an emitter follower amplifier to buffer the output. The difference between the gains of the TIA#4 and TIA#3 are compared. TIA#4 uses only one amplifying stage that is Q1 as a common emitter amplifier to amplify the input current of 10µA. The output gain achieved by TIA#4 is approximately 6.5mV whereas the output gain achieved by TIA#3 is approximately 19mV. Since in TIA#3 an increase in the output is noticed due to the addition of common emitter stage with feedback resistor (Re).Therefore, for designs TIA#5 through TIA#8 more numbers of common emitter stages both with and without feedback resistors (Re) is used.

The pre-layout, post-layout simulation and the circuit layout is shown in Figures 31, 32 and 33 respectively.

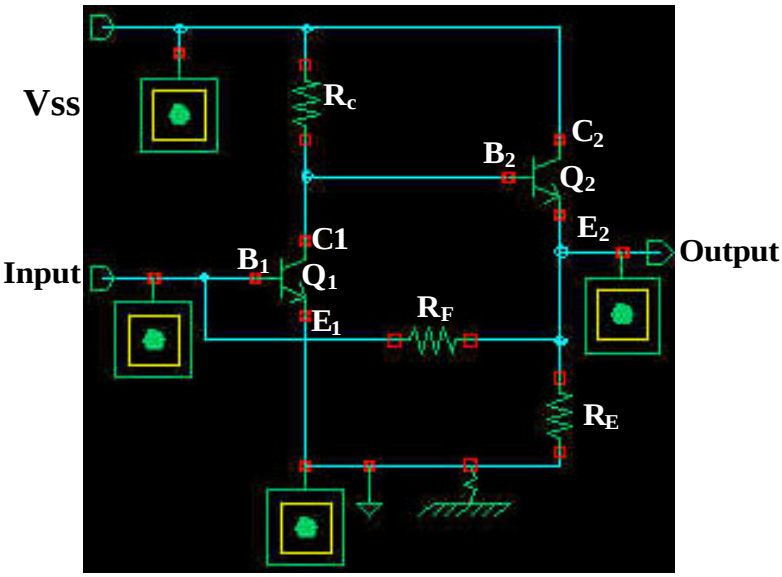


Figure 30 Tansimpedance amplifier #4- Circuit topology

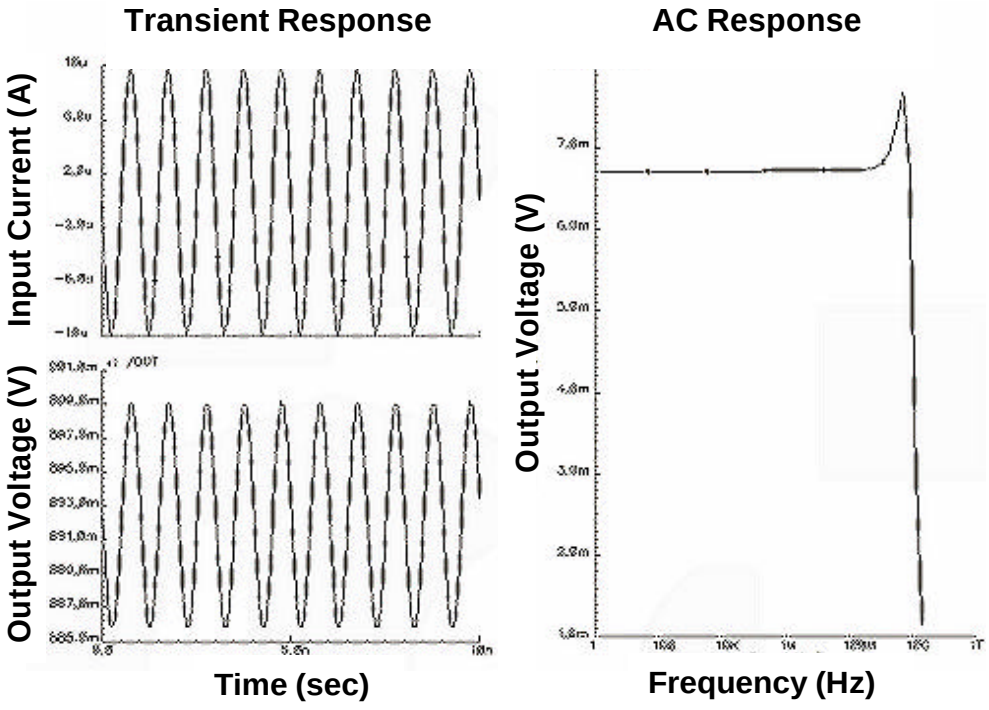


Figure 31 Pre-layout simulation result of TIA#4 at 10GHz

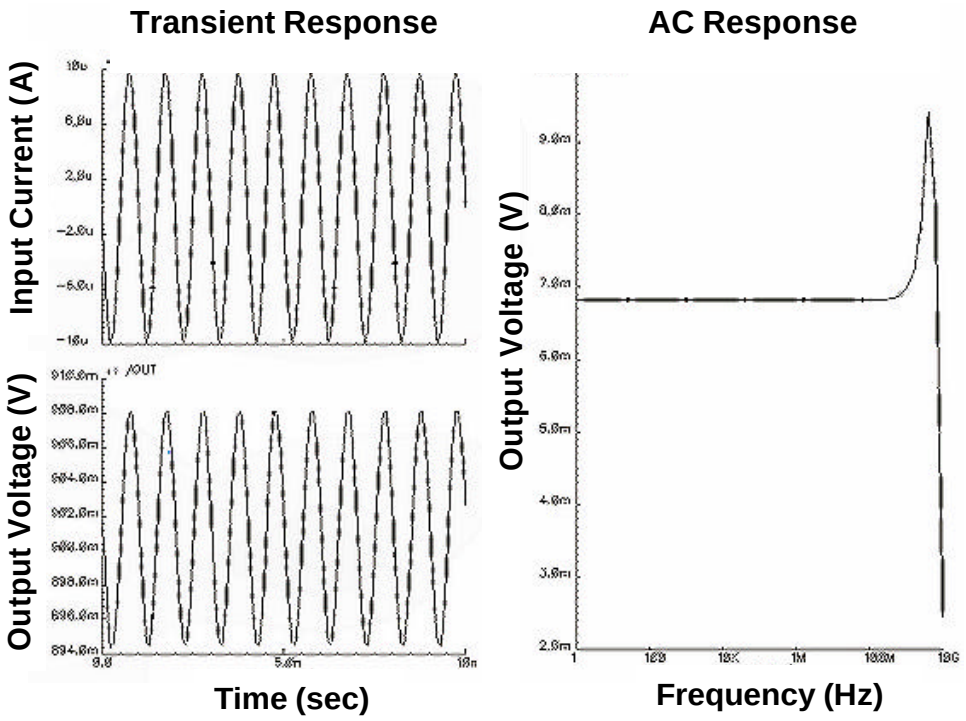


Figure 32 Post-layout simulation result of TIA#4 at 10GHz with I/O Pads

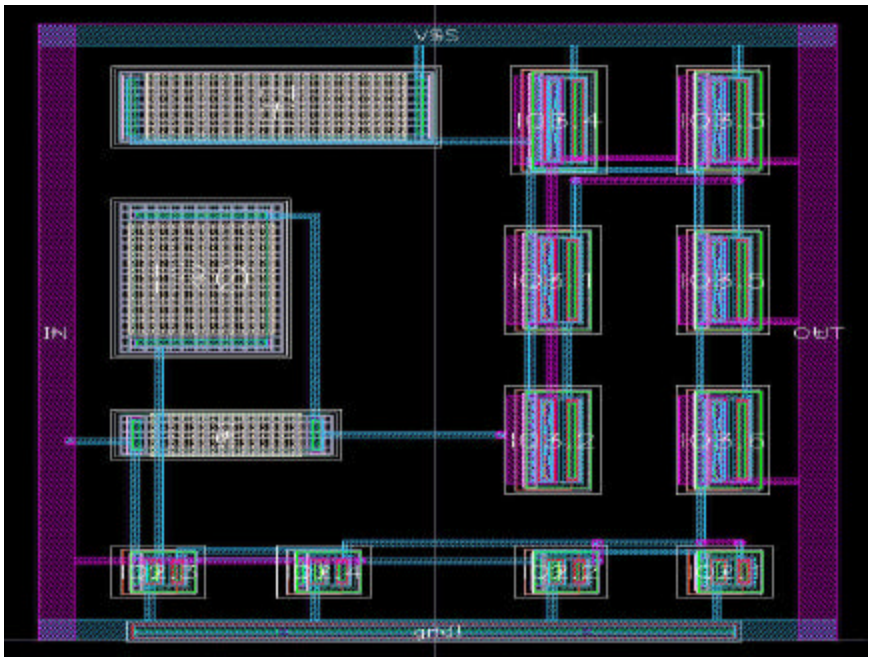


Figure 33 Circuit layout of TIA#4 with I/O Pads

6.2.5 Transimpedance Amplifier # 5

The front end of TIA#5, shown in Figure 34, consists of an NPN common emitter amplifier Q1 followed by a common collector stage Q2. The first two stages Q1 and Q2 are connected with the feedback resistor (R_f). The next stage is a common emitter amplifier provided by NPN transistor Q3 with a feedback resistor R_e for high gain and bandwidth. The output stage consists of the common collector stage which acts as an output buffer. TIA#5 offers an output of 25mV for an input current of 10µA at 10GHz which is better than the designs discussed so far. With the use of the Input and Output pads, the gain and the bandwidth of TIA#5 is not affected because NPN transistors Q2 and Q4 act as buffers. Figure 35, Figure 36, and Figure 37 show the pre-layout simulation, post-layout simulation and the circuit layout of TIA#5 respectively.

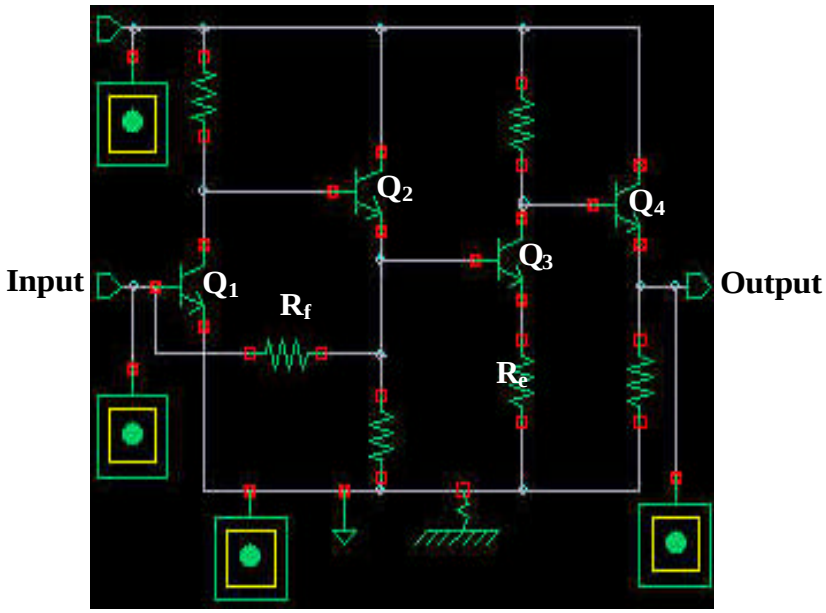


Figure 34 Tansimpedance amplifier #5- Circuit topology

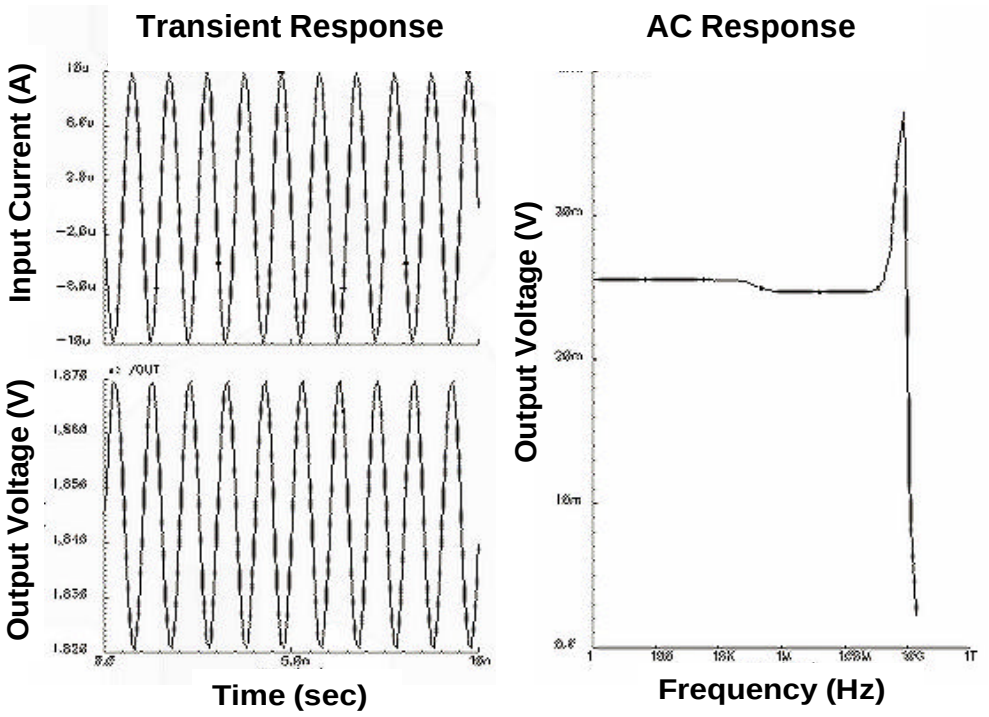


Figure 35 Pre-layout simulation result of TIA#5 at 10GHz

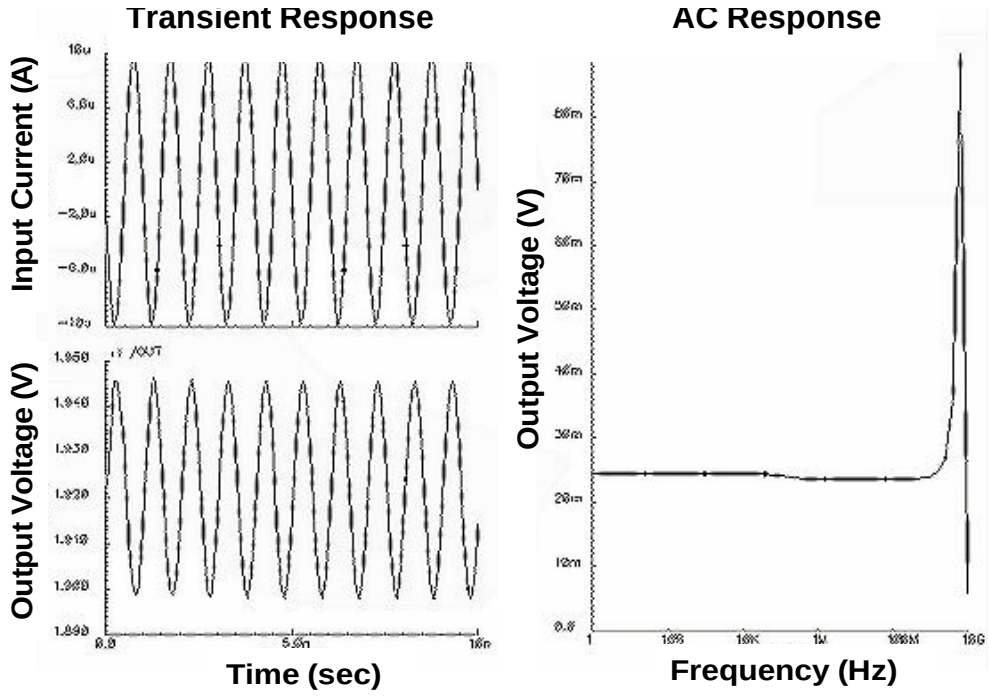


Figure 36 Post-layout simulation result of TIA#5 at 10GHz with I/O Pads

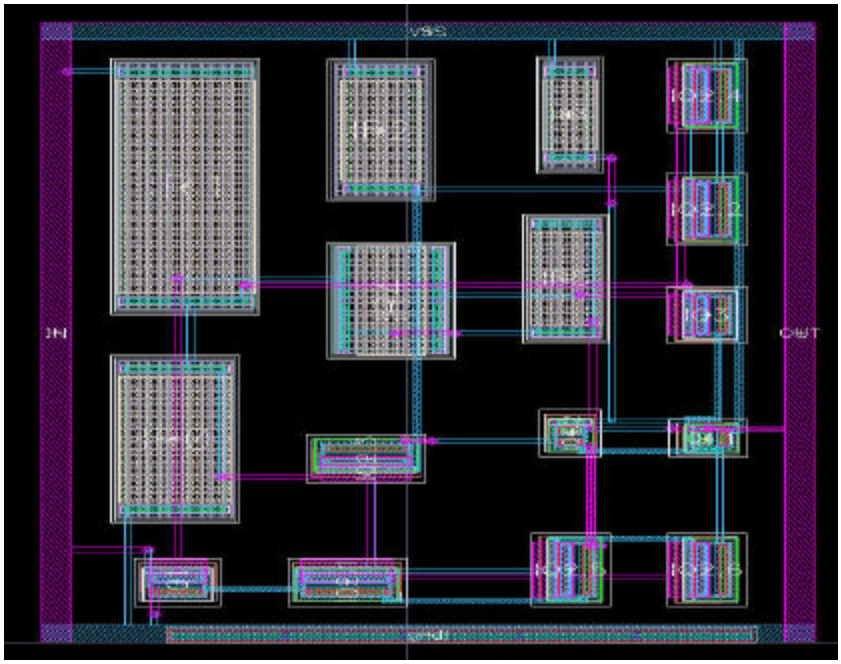


Figure 37 Circuit layout of TIA#5 with I/O Pads

6.2.6 Transimpedance Amplifier # 6

The circuit arrangement of TIA#6, shown in Figure 38, consists of four common emitter stages with NPN transistors Q1, Q2, Q3 and Q4. Transistors Q1, Q2, and Q3 are cascaded together. This kind of cascaded arrangement is used to obtain more output gain. An output of 30mV is achieved with this amplifier. The high gain is due to the increase of the feedback resistor value from 630Ω to 680Ω. By increasing the value of feedback resistor, bandwidth has been reduced to 6.5 GHz. This design is implemented to demonstrate, how the compromise between the gain and the bandwidth of an amplifier can be made by carefully selecting the value of the feedback resistor (R_f). Figure 39, Figure 40 and Figure 41 show the pre-layout simulation, post-layout simulation and circuit layout of TIA#6 respectively.

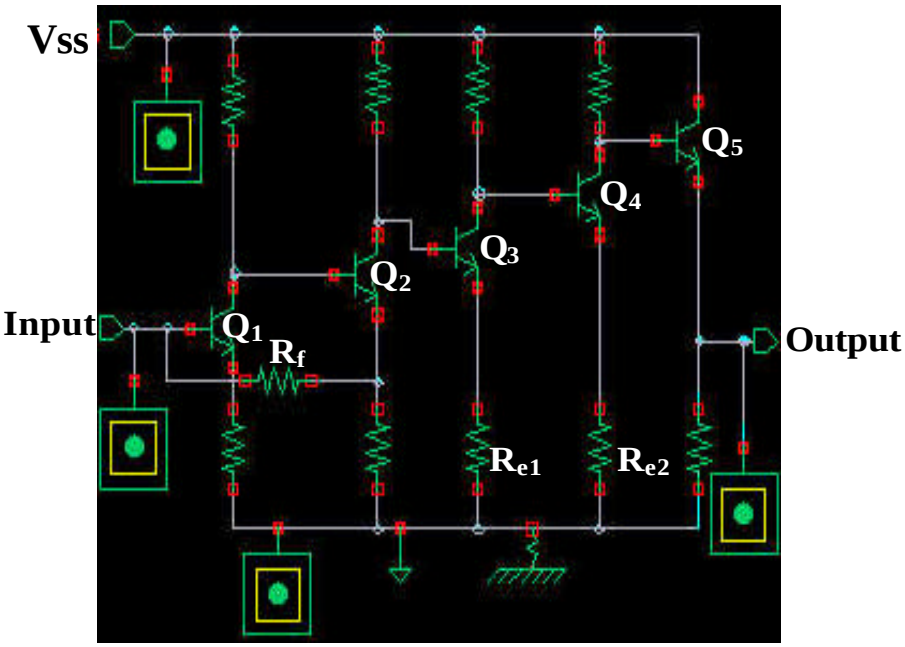


Figure 38 Tansimpedance amplifier #6- Circuit topology

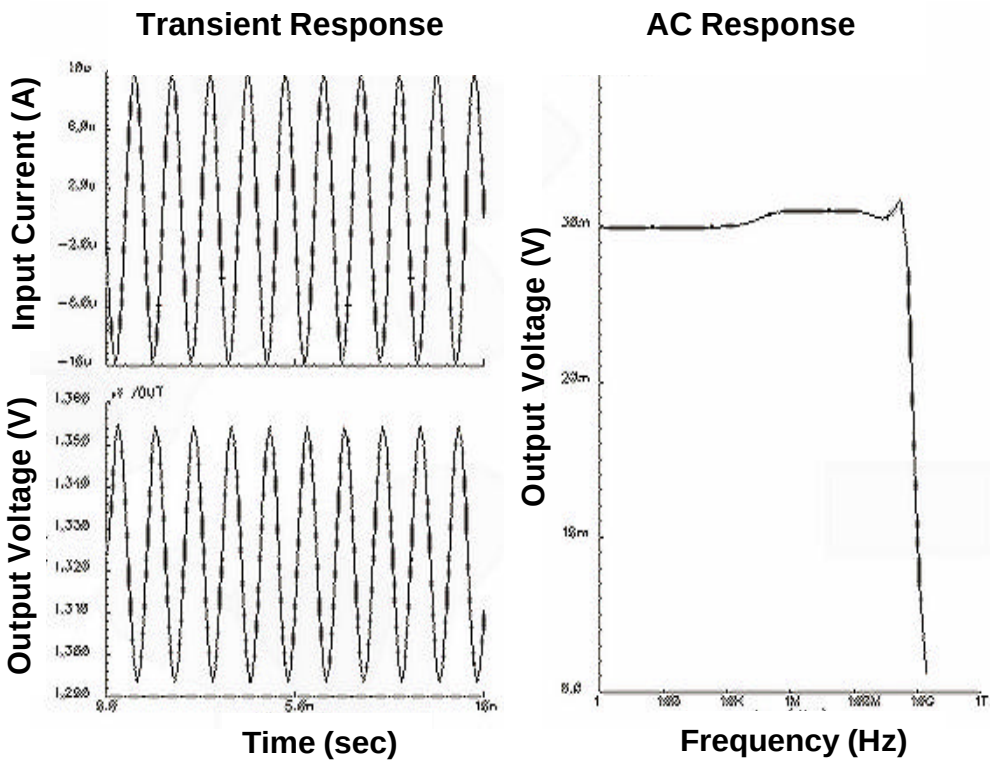


Figure 39 Pre-layout simulation result of TIA#6 at 10GHz

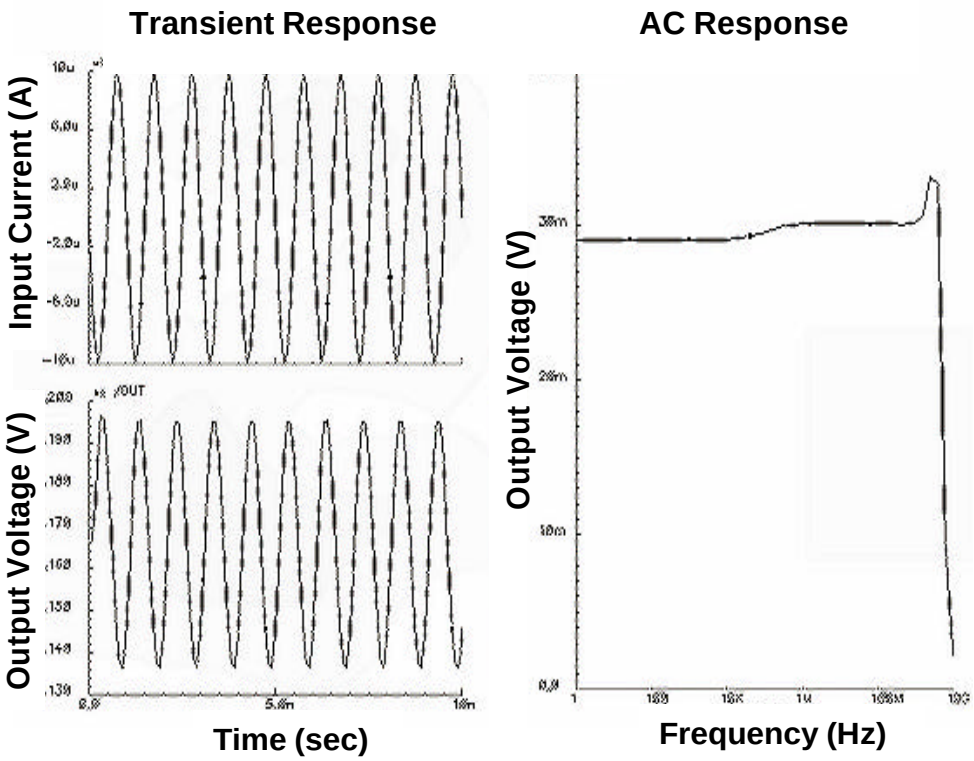


Figure 40 Post-layout simulation result of TIA#6 at 10GHz with I/O Pads

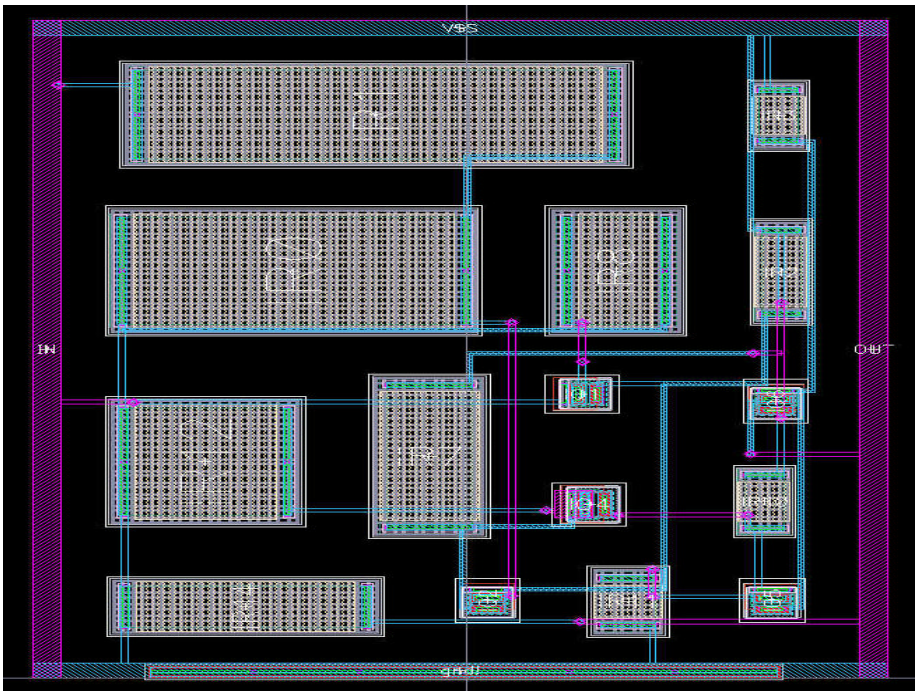


Figure 41 Circuit layout of TIA#6 with I/O Pads

6.2.7 Transimpedance Amplifier # 7

In the previously designed TIAs from TIA#1-TIA#6, the benefit of using a common emitter amplifying stage with and without feedback resistor (R_e), cascaded common emitter stages, buffer stages and feedback resistance from the second gain stage have been shown. The circuit design for TIA#7, shown in Figure 42, is designed on the basis of all these features. It consists of TIA#2 discussed in section 6.2.2 followed by an emitter follower stage NPN transistor Q3 which acts as a buffer for the output of the first stage NPN transistors Q1 and Q2. Following this is a two stage cascaded amplifier consisting of NPN transistors Q4 and Q5 employed in order to achieve maximum gain. The output is again buffered using NPN transistor Q6. This topology can achieve maximum output gain of 46.73mV. Figure 43, Figure 44 and Figure 45 show the pre and post-layout simulation with circuit layout of TIA#7 respectively.

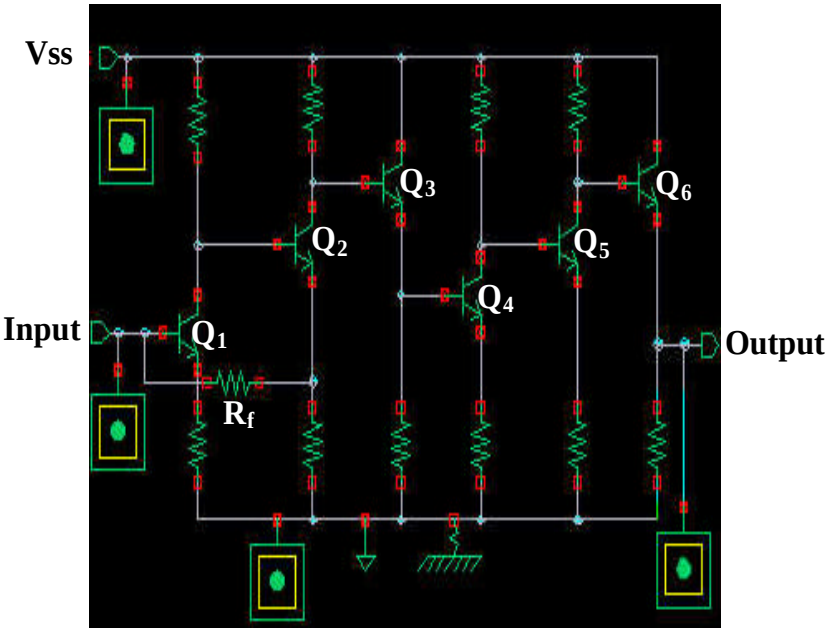


Figure 42 Tansimpedance amplifier #7- Circuit topology

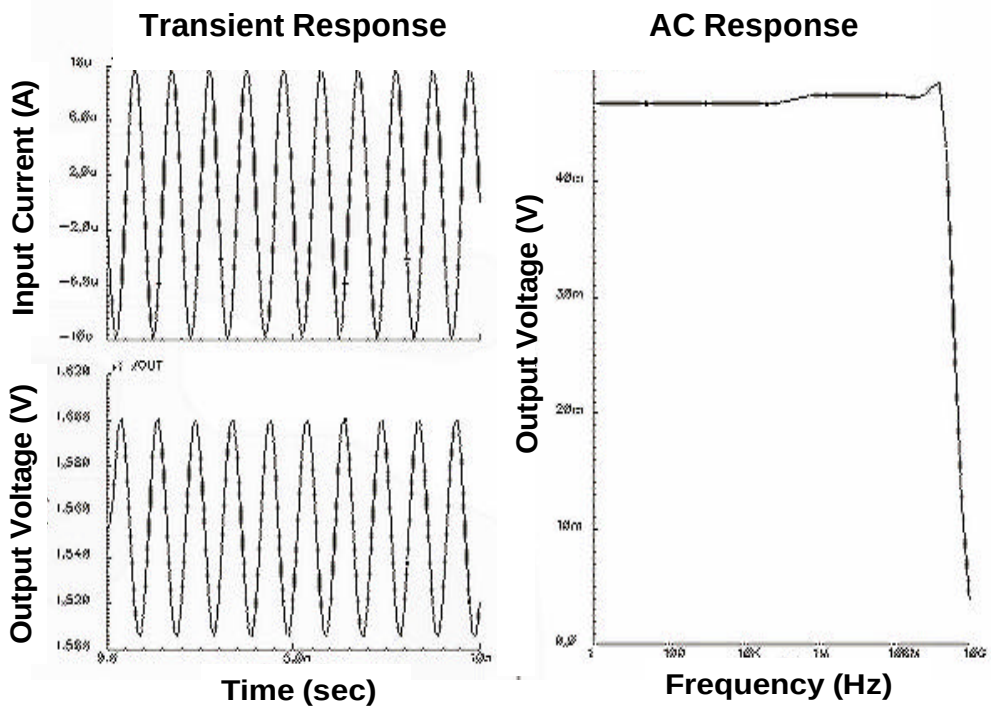


Figure 43 Pre-layout simulation result of TIA#7 at 10GHz

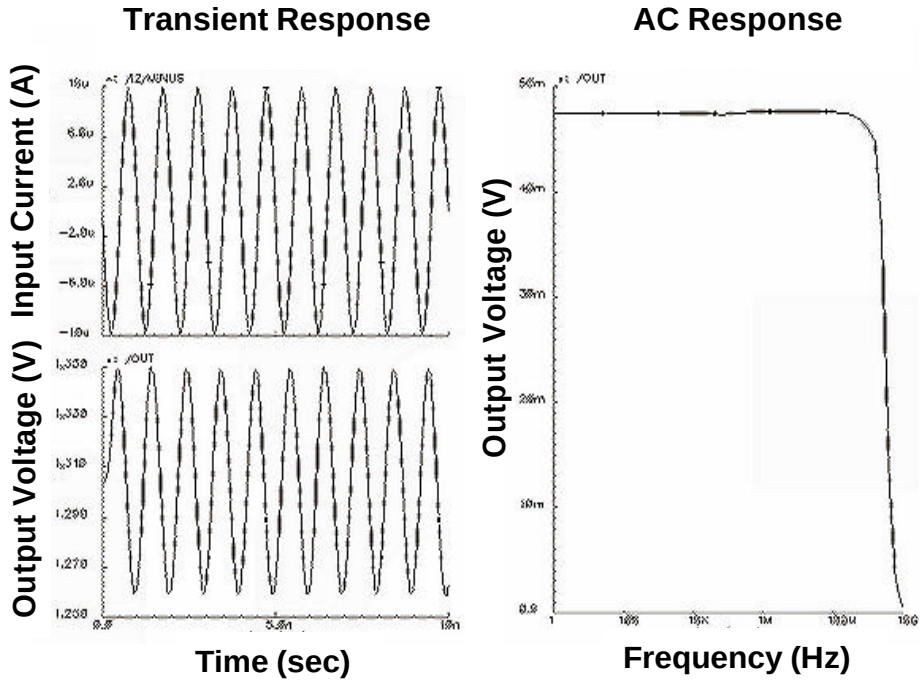


Figure 44 Post-layout simulation result of TIA#7 at 10GHz with I/O Pads

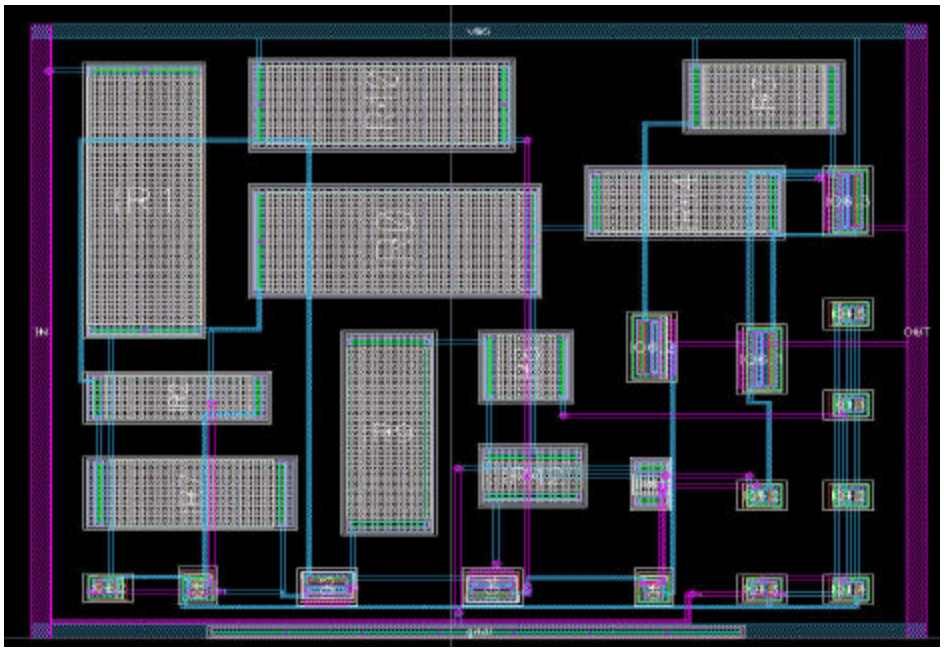


Figure 45 **Circuit layout of TIA#7 with I/O Pads**

6.2.8 Transimpedance Amplifier # 8

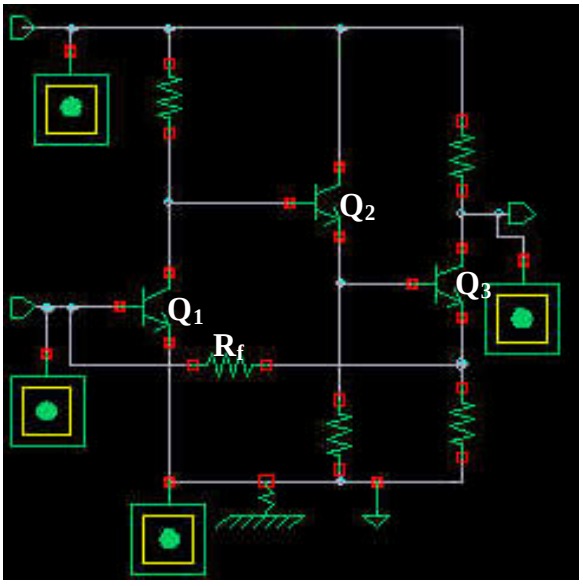


Figure 46 **Tansimpedance amplifier #8- Circuit topology**

The circuit plan of TIA#8 shown in Figure 46, consists of a NPN transistor Q1 acting as a common emitter stage for the input current followed by an emitter follower NPN transistor Q2 stage and NPN transistor Q3 as a common emitter stage. The feedback resistor (R_f) is taken from the output stage to avoid the inter-transistor DC coupling effect between intermediate stages. The intrinsic capacitances in the transistor device cause the output to fall off at higher frequencies [74]. Figure 47, Figure 48 and Figure 49 show the pre-layout simulation, post-layout simulation and circuit layout of TIA#8 respectively.

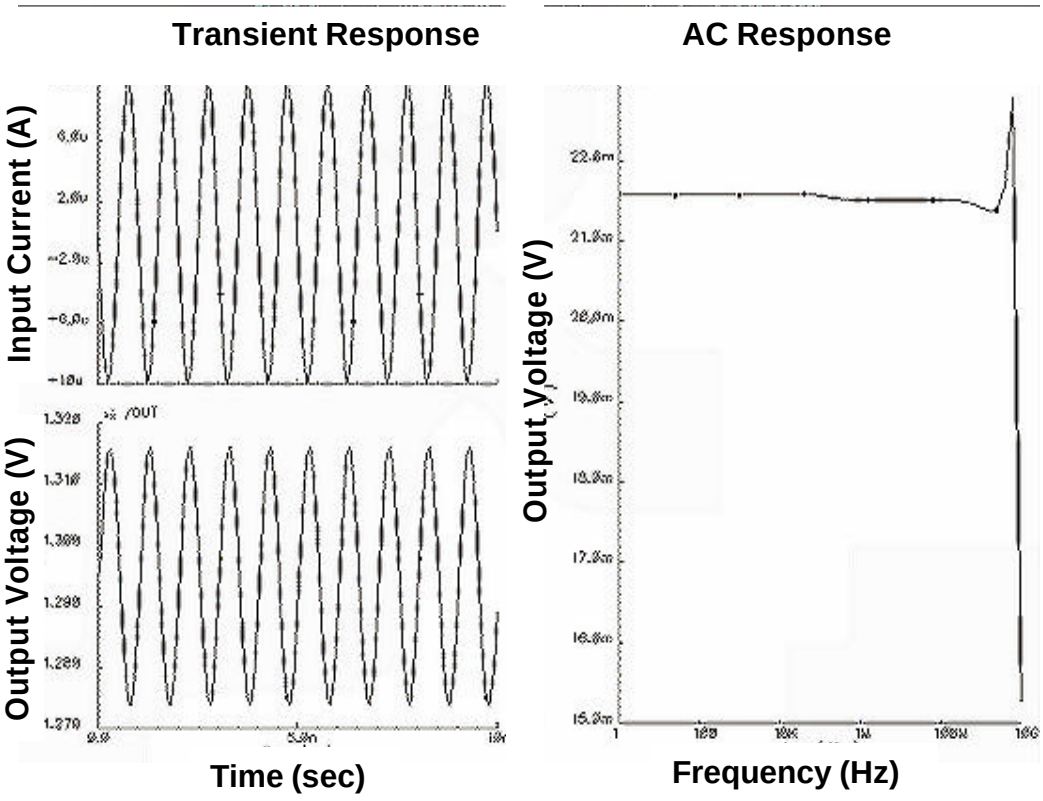


Figure 47 Pre-layout simulation result of TIA#8 at 10GHz

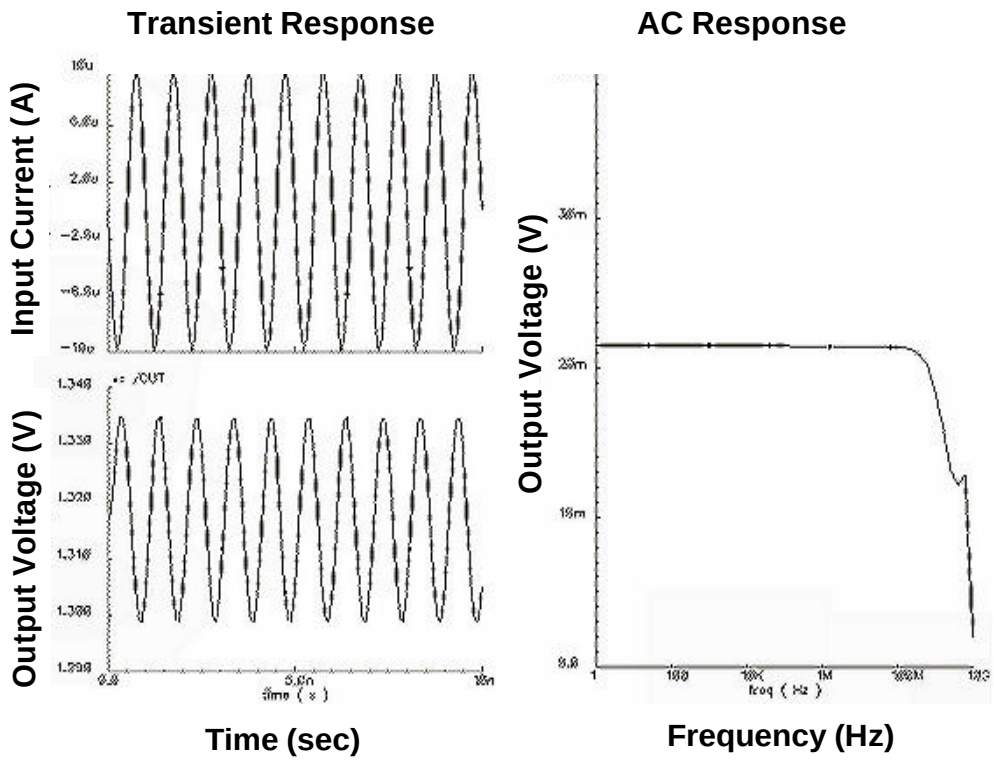


Figure 48 Post-layout simulation result of TIA#8 at 10GHz with I/O Pads

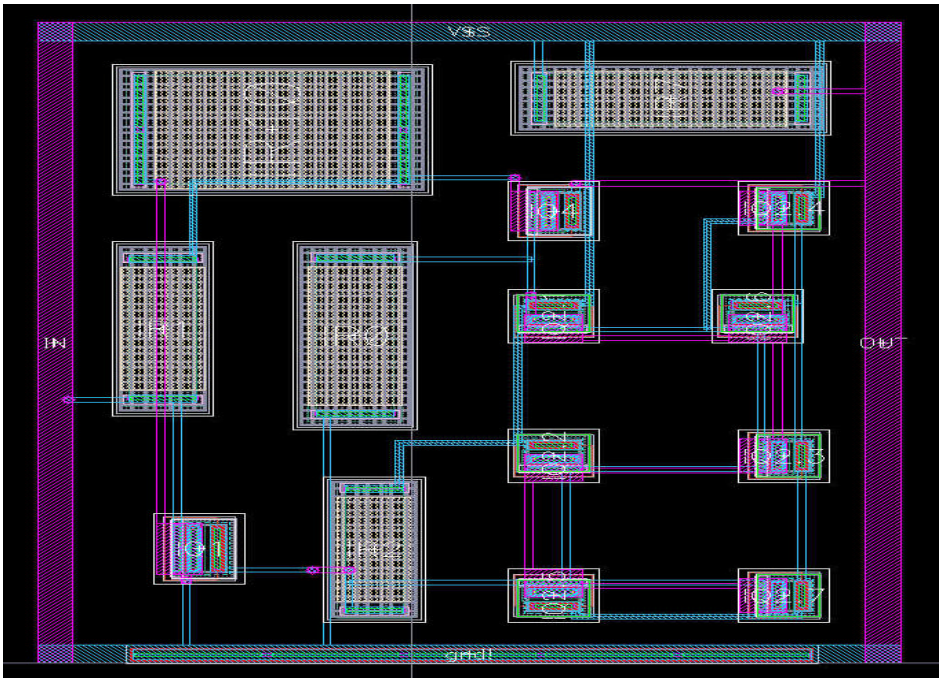


Figure 49 Circuit layout of TIA#8 with I/O Pads

6.2.9 Transimpedance Amplifier # 9

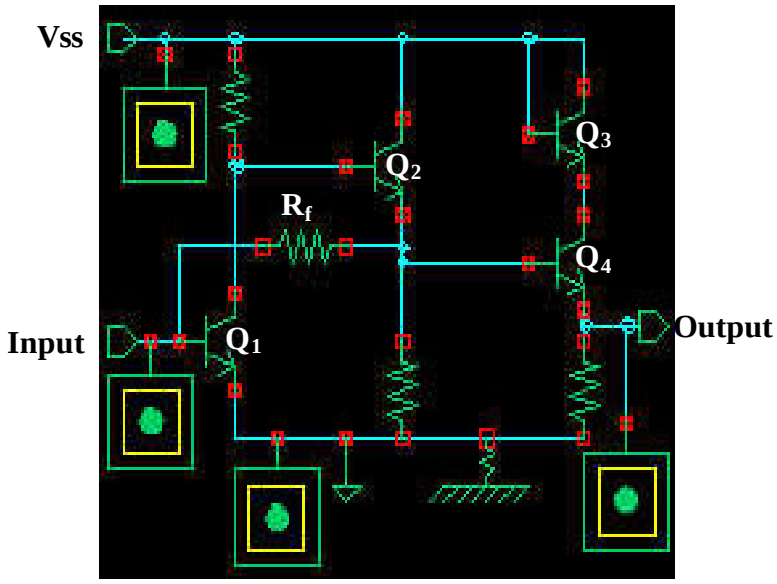


Figure 50 Transimpedance amplifier #9- Circuit topology

The front-end of TIA#9 [75], as shown in Figure 50, consists of a common emitter NPN transistor stage Q1 designed for a single channel optical receiver. This TIA is studied in terms of gain and bandwidth. The NPN transistor Q1 forms the common emitter stage followed by a NPN transistor Q2 that acts as an emitter follower. The final stage, a common emitter NPN transistor Q4 is biased with NPN transistor Q3 for stability. The simulation results in [75] show the output gain and bandwidth of 62dBΩ and 2.7GHz respectively in H-Spice for a custom SiGe process (0.8 micron) exhibiting transit frequency (f_T) of 45GHz whereas the Spectre simulation results of TIA#9 designed in the IBM SiGe process show gain and bandwidth of 55.22 dBΩ and 10GHz as shown in Figure 51 and Figure 52 respectively. A compromise has been made in the selection of the value of the feed back resistance (R_f) keeping the goal of 10GHz in consideration. Figure 53 shows the circuit layout of TIA#9 with I/O pads. Thus, the circuit designs of TIA#9 shows the enhancement of gain using the IBM SiGe process over other custom SiGe processes.

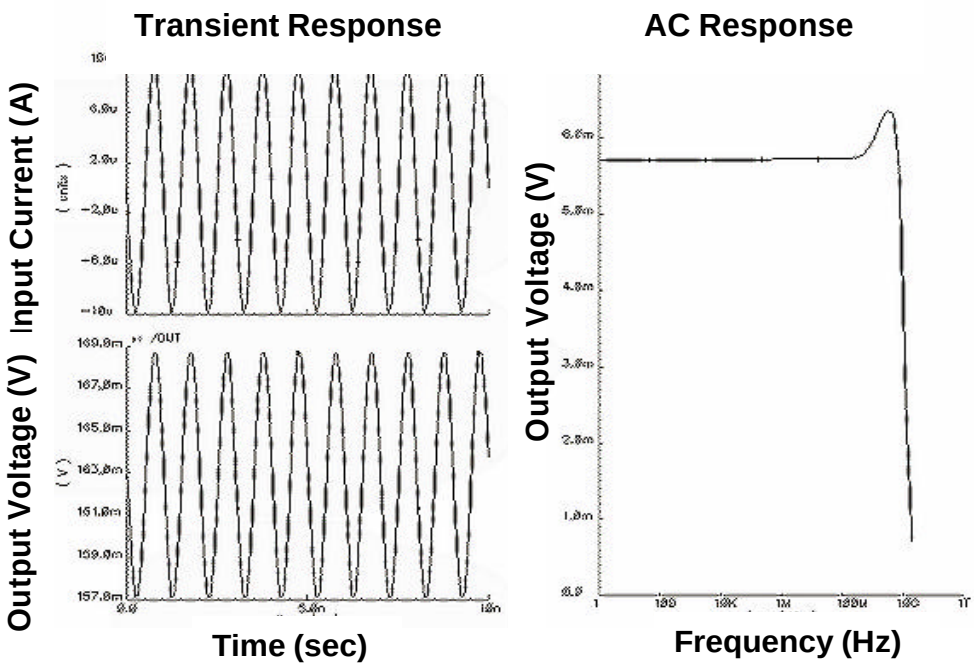


Figure 51 Pre-layout simulation result of TIA#9 at 10GHz

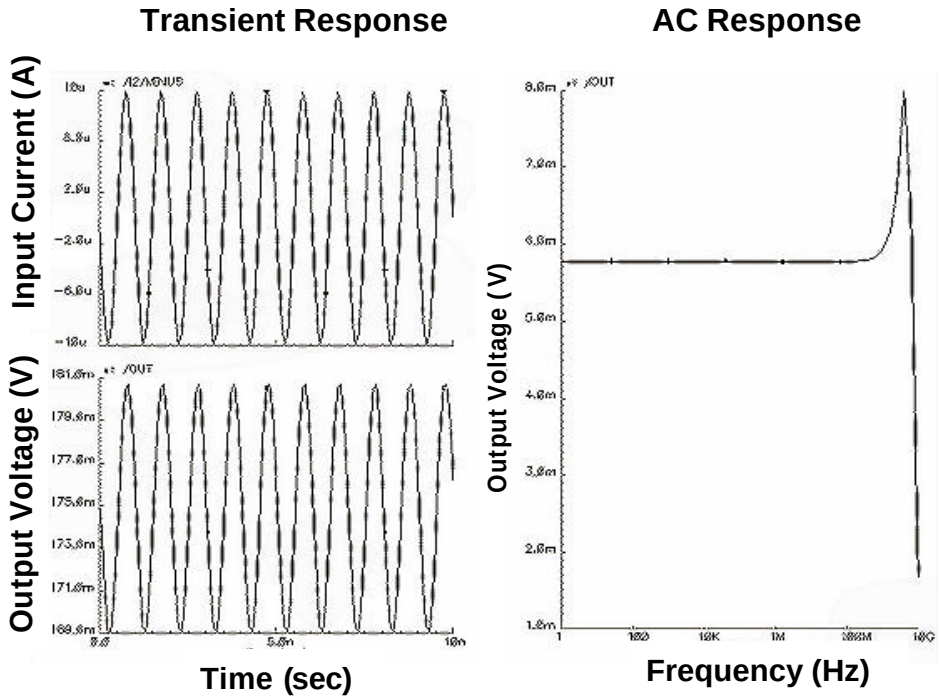


Figure 52 Post-layout simulation result of TIA#9 at 10GHz with I/O Pads

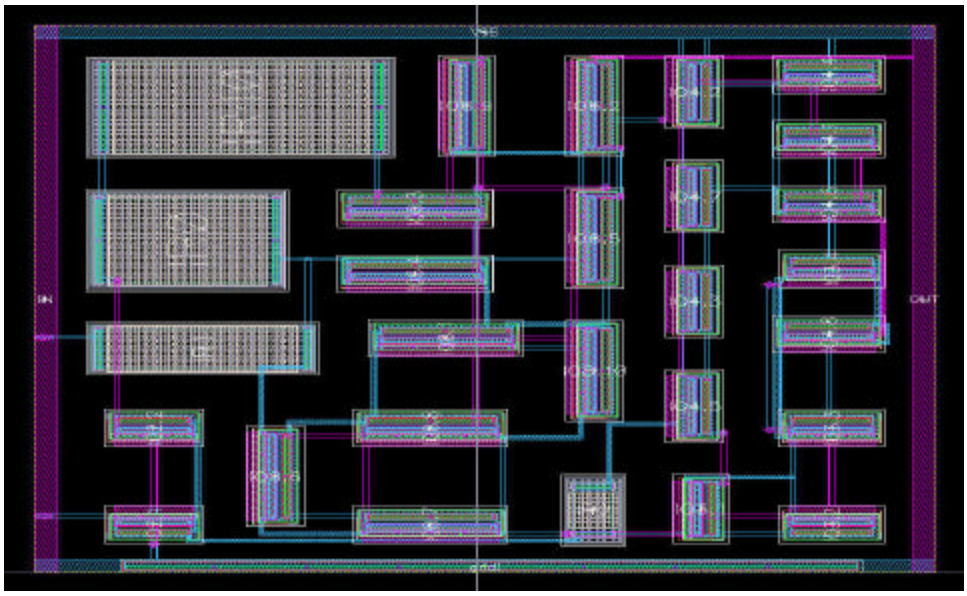


Figure 53 Circuit layout of TIA#9 with I/O Pads

6.2.10 Transimpedance Amplifier # 10

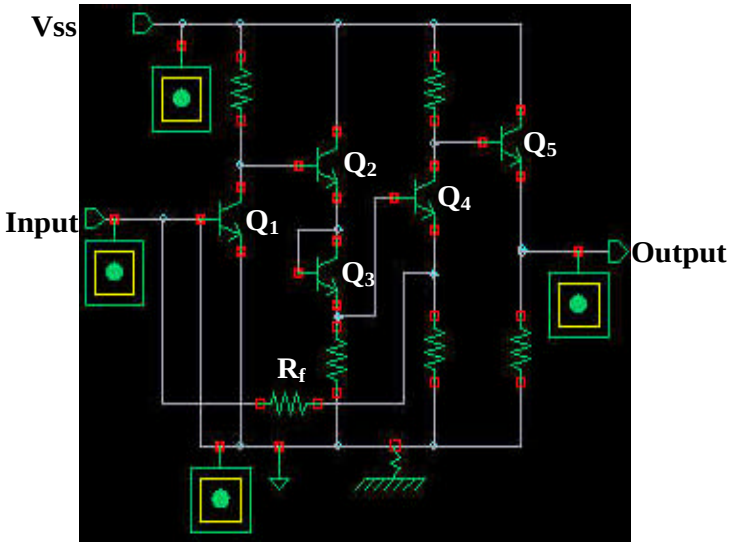


Figure 54 Transimpedance amplifier #10- Circuit topology

The circuit layout of TIA #10 [76] is a wideband transimpedance amplifier built for optical communication as shown in Figure 54. The topology consists of a front-end common

emitter NPN transistor Q1 amplifier stage for current amplification followed by NPN transistor Q2 which acts as an emitter follower or buffer. The emitter follower Q2 stage acts as a DC level shifter to keep the NPN transistor Q4 in the active region. The diode Q3 is added to keep transistor Q1 in the active region. The next two stages Q4 and Q5 are a common emitter with a feedback resistor (R_e) and an emitter follower used for high gain and bandwidth and for output buffering. The simulation results in [76] show an output gain and bandwidth of 60dBΩ at 0.96GHz. Whereas the Spectre simulations for TIA#10 implemented in the IBM SiGe process show a gain and bandwidth of 54.08dBΩ at 3GHz. Hence we show the benefit of using the IBM SiGe process. Figure 55, Figure 56 and Figure 57 show the pre-layout simulation, post-layout simulation and the circuit layout of TIA#10 respectively.

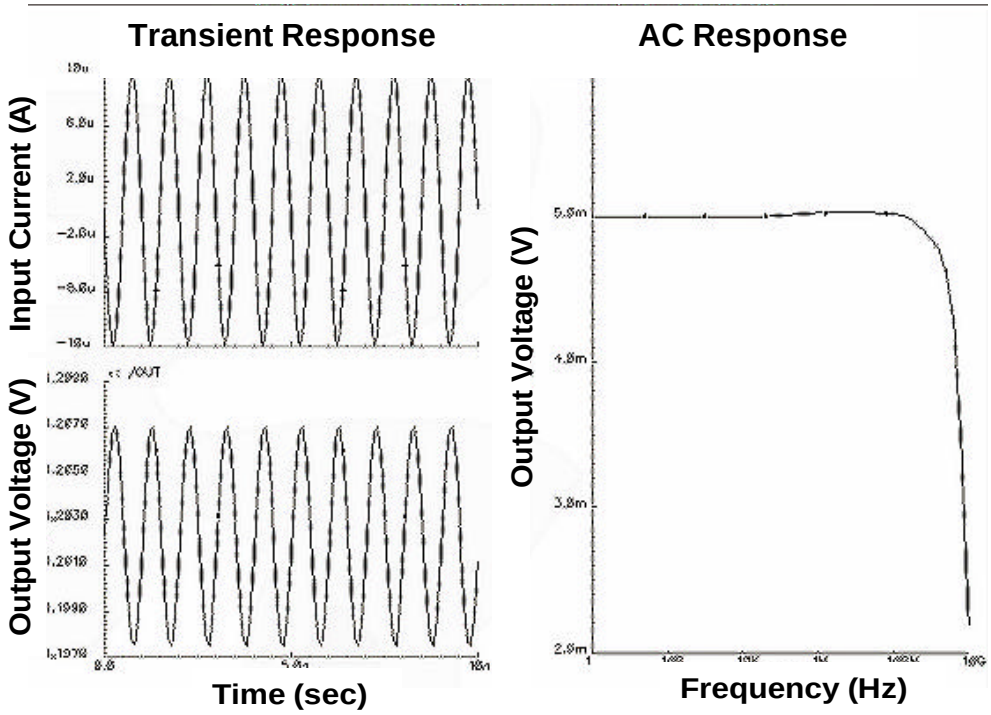


Figure 55 Pre-layout simulation result of TIA#10 at 10GHz

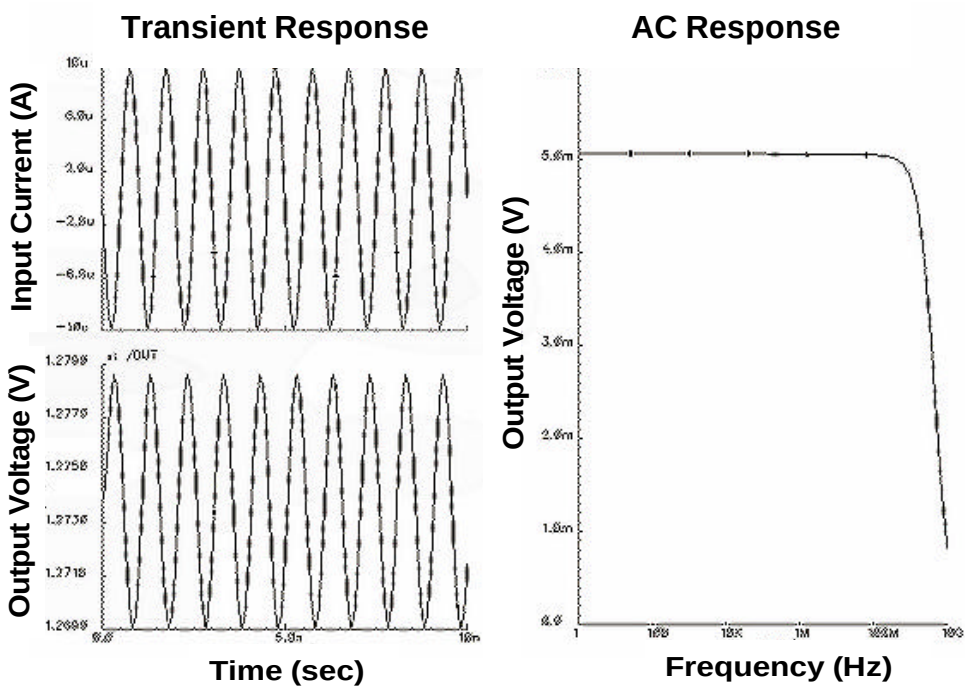


Figure 56 Post-layout simulation result of TIA#10 at 10GHz with I/O Pads

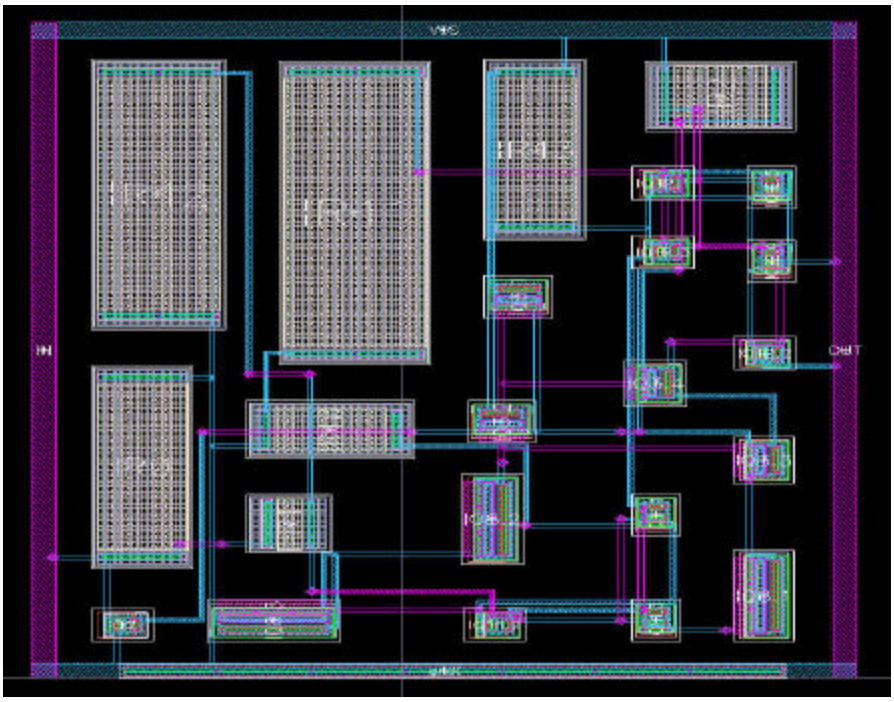


Figure 57 Circuit layout of TIA#10 with I/O Pads

6.2.11 Transimpedance Amplifier # 11

The circuit outline of TIA#11 [77], shown in Figure 58 consists of NPN transistor Q1 acting as a common emitter stage followed by two emitter follower NPN stages Q2 and Q3. The diodes Q4, Q5 and Q6 are used to optimize bias points. The SiGe process technology in which this topology was designed [77] offers f_T and f_{MAX} of 23GHz and 34GHz at the supply voltage of V_{cc}=3V. The simulation result in [77] offer an output gain of 45.2dBΩ at 3.2GHz and the Spectre simulation for TIA#11 realized with the IBM SiGe process shows a high gain of 60.03dBΩ at the bandwidth of 10GHz. A compromise between the gain and the bandwidth characteristics can be made by varying the value of feedback resistor (R_f). Figure 59, Figure 60 and Figure 61 show the pre-layout, post-layout simulation and circuit layout of TIA#11 respectively.

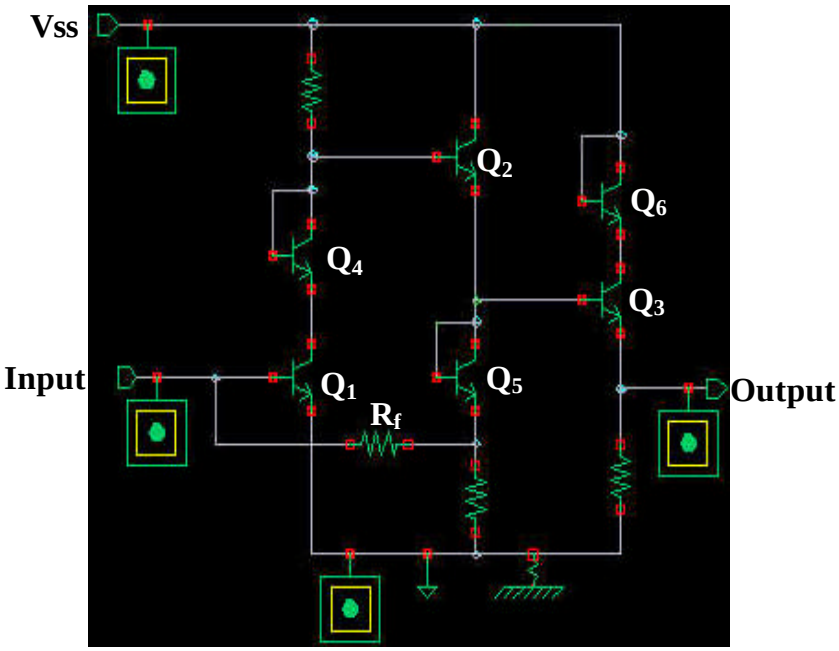


Figure 58 Tansimpedance amplifier #11- Circuit topology

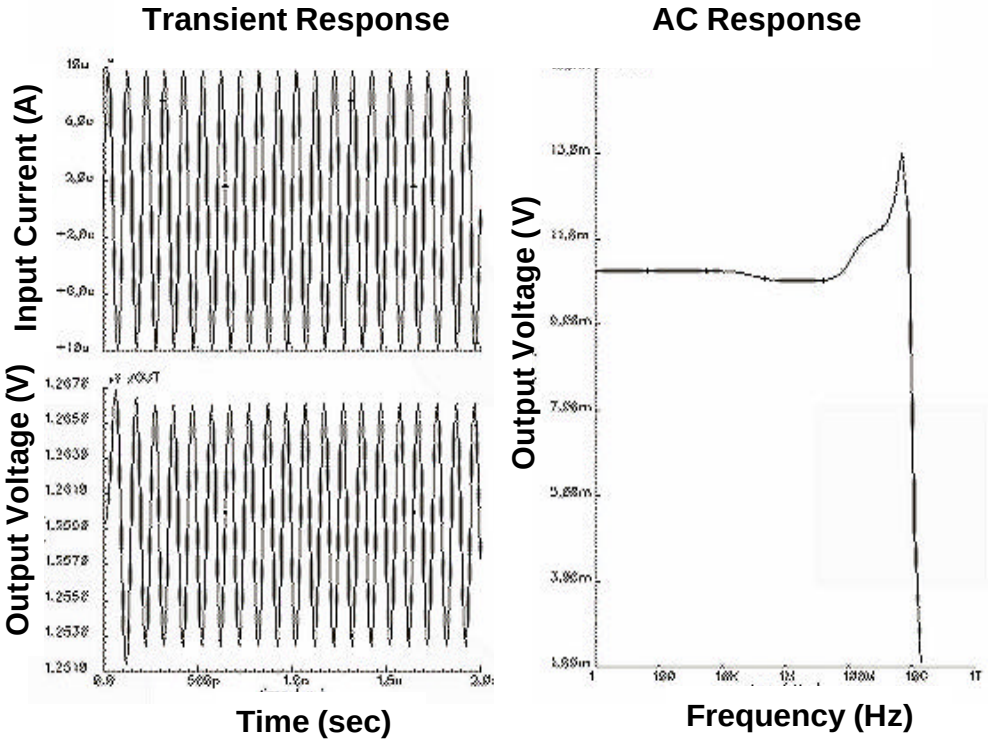


Figure 59 Pre-layout simulation result of TIA#11 at 10GHz

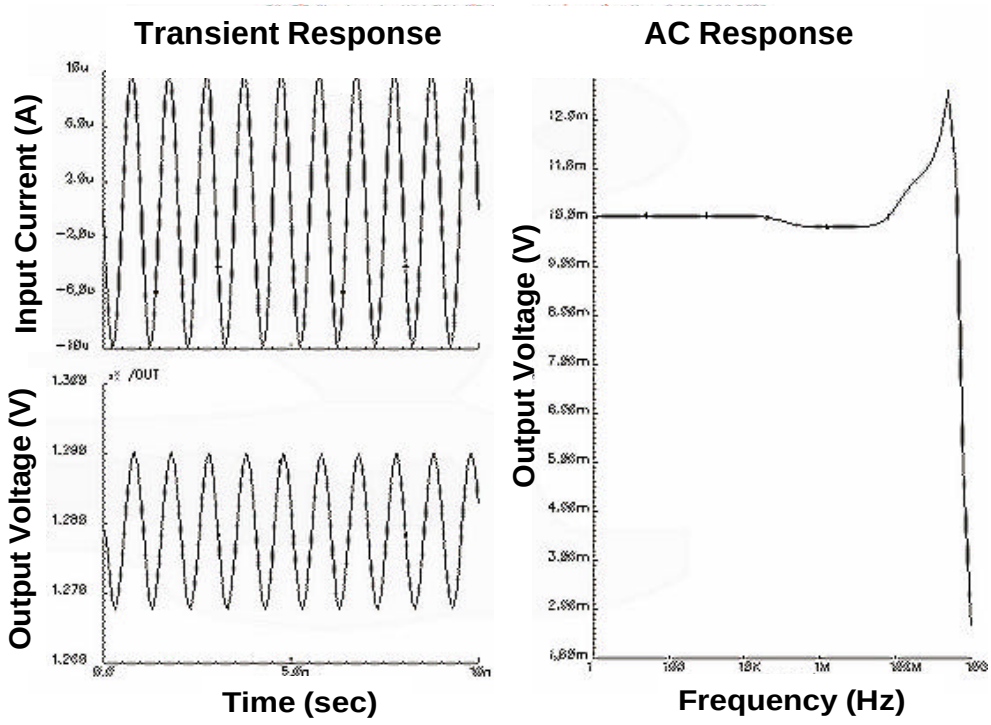


Figure 60 Post-layout simulation result of TIA#11 at 10GHz with I/O Pads

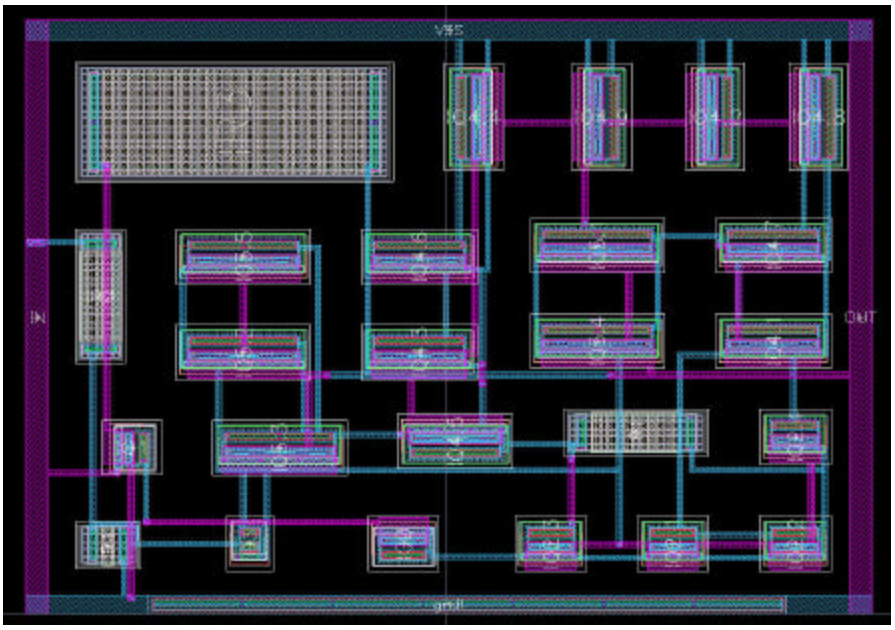


Figure 61 Circuit layout of TIA#11 with I/O Pads

6.2.12 Transimpedance Amplifier # 12

The circuit design for TIA#12 [78], shown in Figure 62, consists of NPN common emitter stage Q1 followed by an emitter follower stage Q2 and a common emitter NPN transistor stage Q3. The output of stage Q3 is buffered using NPN transistor Q4 which is a common collector stage. Figure 63, Figure 64, Figure 65 show the pre-layout simulation, post-layout simulation and the circuit layout of TIA#12 respectively. This circuit topology was designed [78] in a very fast GaAs-based HBT technology offering f_T and f_{Max} of 100GHz and 200GHz respectively. The simulation results in [78] show a peak to peak voltage of 400mV at the supply voltage of 5.3v where as the Spectre simulation for the same TIA#11 implemented in the SiGe IBM process shows a peak to peak voltage of 15mv at 10GHz. This circuit topology was selected to show that SiGe devices are comparable to GaAs devices in terms of high speed. Since the maximum

oscillation frequency of the GaAs process is very high as compared to the SiGe process the circuit topology designed in the IBM SiGe process does not offer equivalent speed.

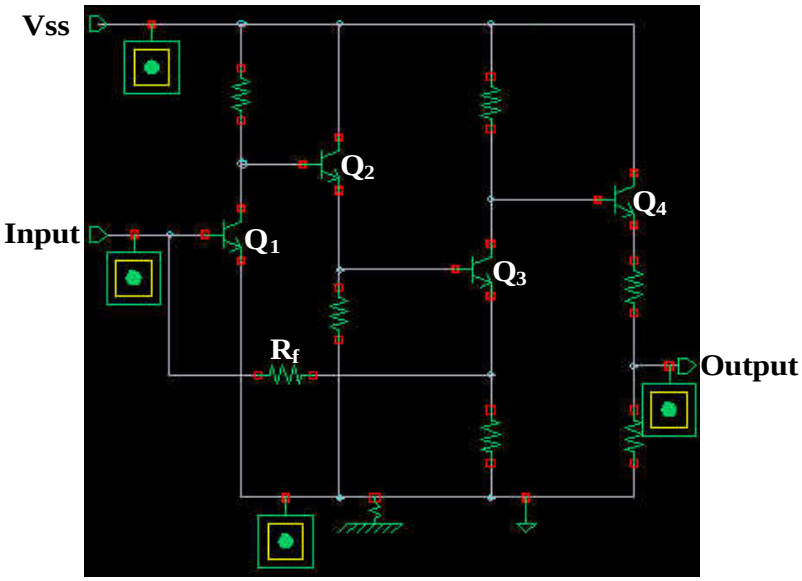


Figure 62 Tansimpedance amplifier #12- Circuit topology

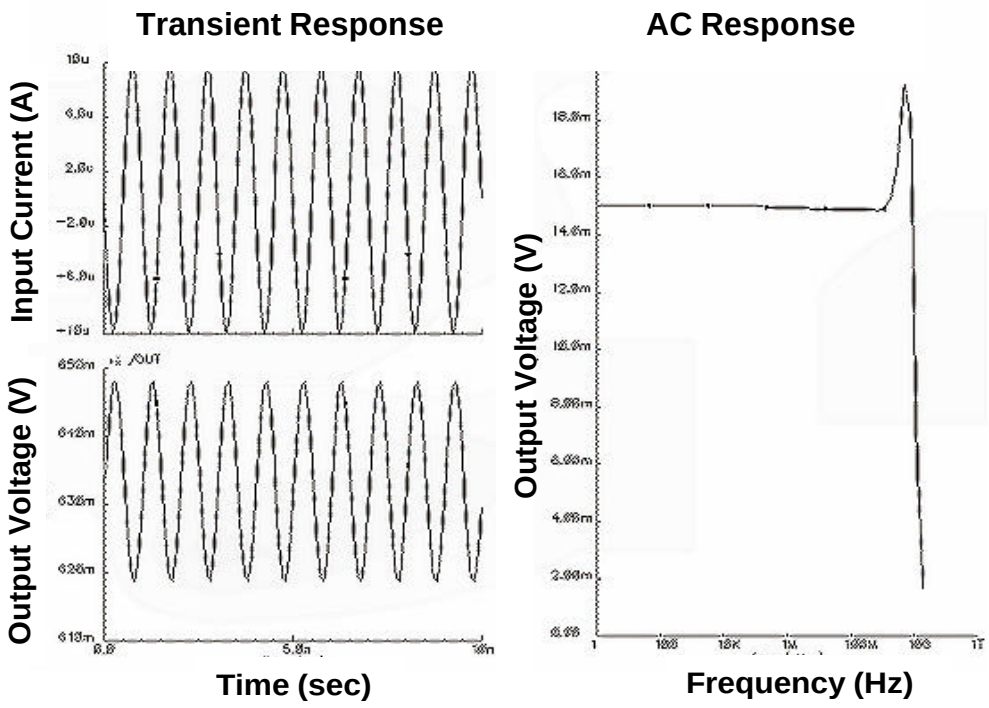


Figure 63 Pre-layout simulation result of TIA#12 at 10GHz

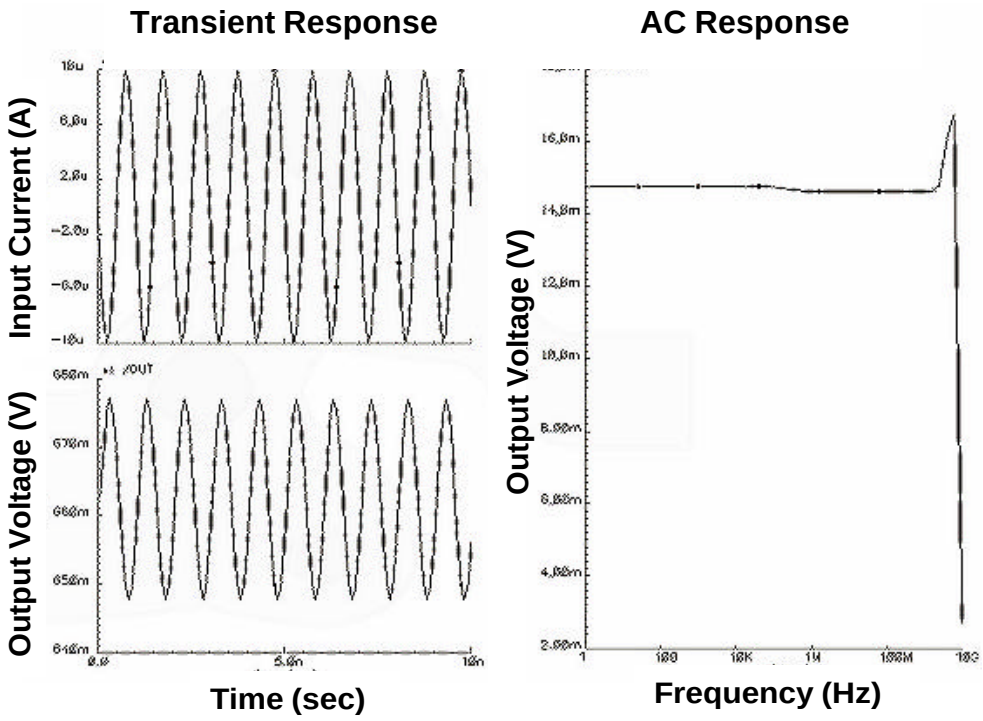


Figure 64 Post-layout simulation result of TIA#12 at 10GHz with I/O Pads

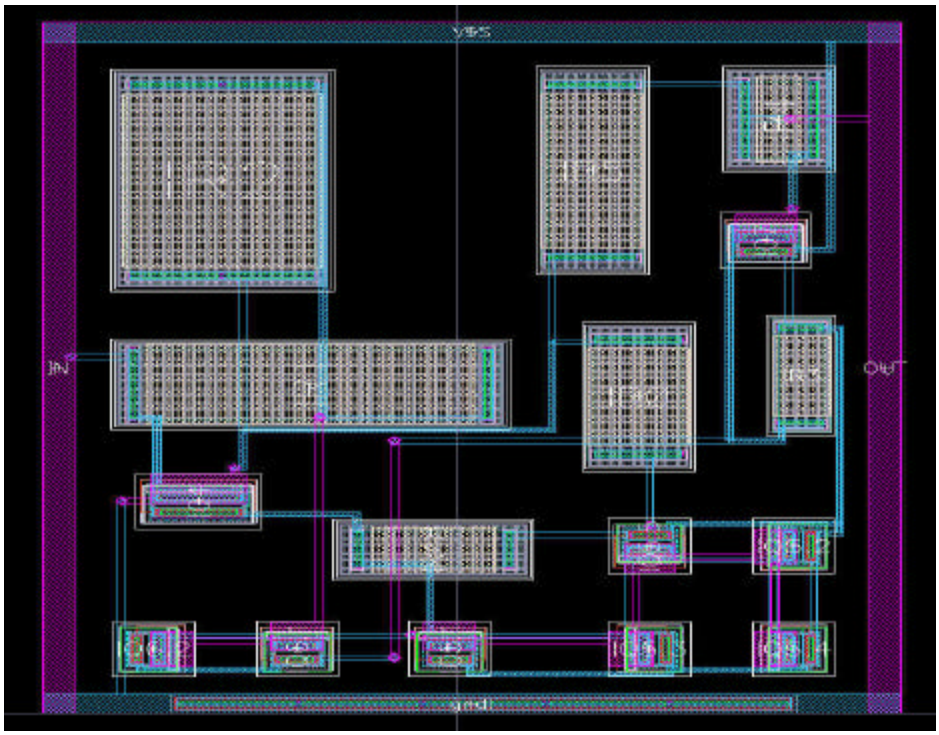


Figure 65 Circuit layout of TIA#12 with I/O Pads

6.2.13 Transimpedance Amplifier # 13

Circuit topology for TIA#13 [78], shown in Figure 66 is same as TIA#12 except that the performance of TIA#12 is increased by the addition of NPN transistors Q5, Q6, Q7, Q8 and Q9. TIA#13 consists of a common emitter stage Q1 followed by emitter follower stages Q2 and a common emitter NPN transistor stage Q3. The output of stage Q3 is buffered using NPN transistor Q4, which is a common collector stage. Due to the bias optimization using NPN transistors Q5, Q6, Q7, Q8, and Q9 there is significant increase in the output gain and the bandwidth in TIA#13. TIA#12 shows a gain and bandwidth of 15.03mV at 10.66 GHz whereas TIA#13 shows an output gain and bandwidth of 31.06mV at 11.44GHz. Figure 67, Figure 68 and Figure 69 show the pre-layout simulation, post-layout simulation and circuit layout of TIA#13 respectively.

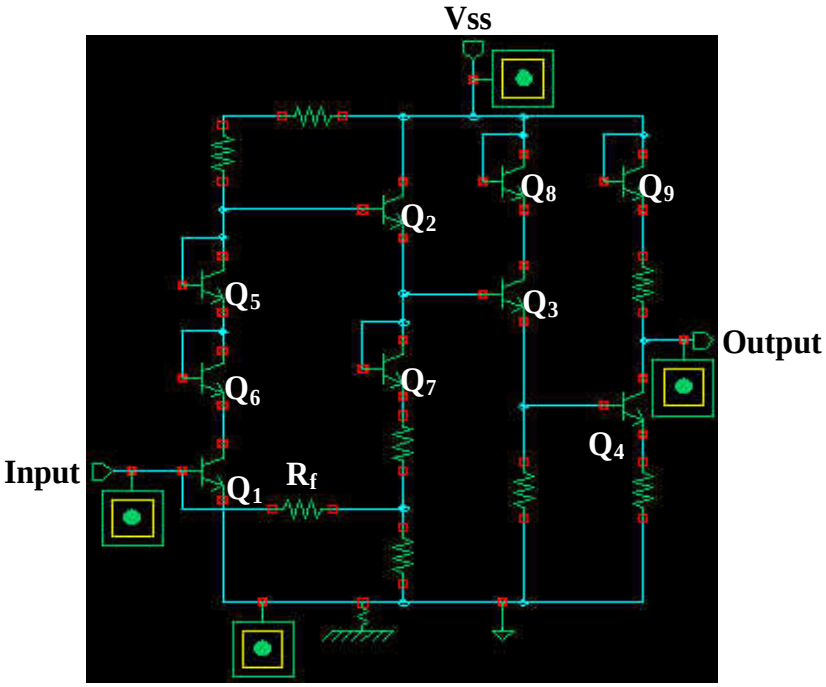


Figure 66 Tansimpedance amplifier #13- Circuit topology

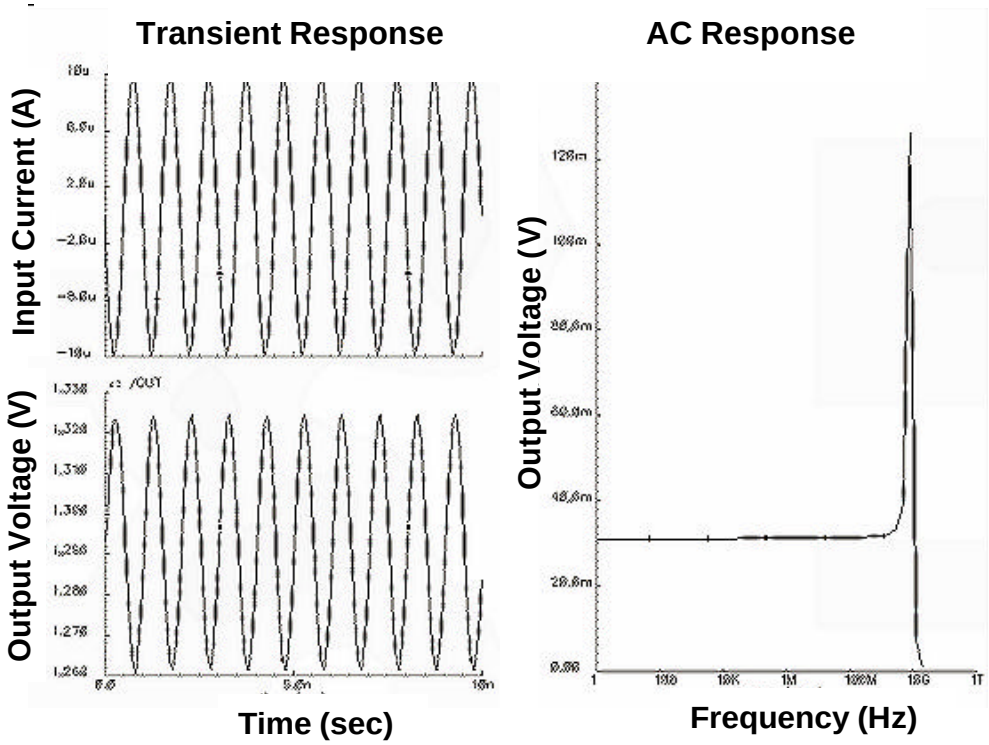


Figure 67 Pre-layout simulation result of TIA#13 at 10GHz

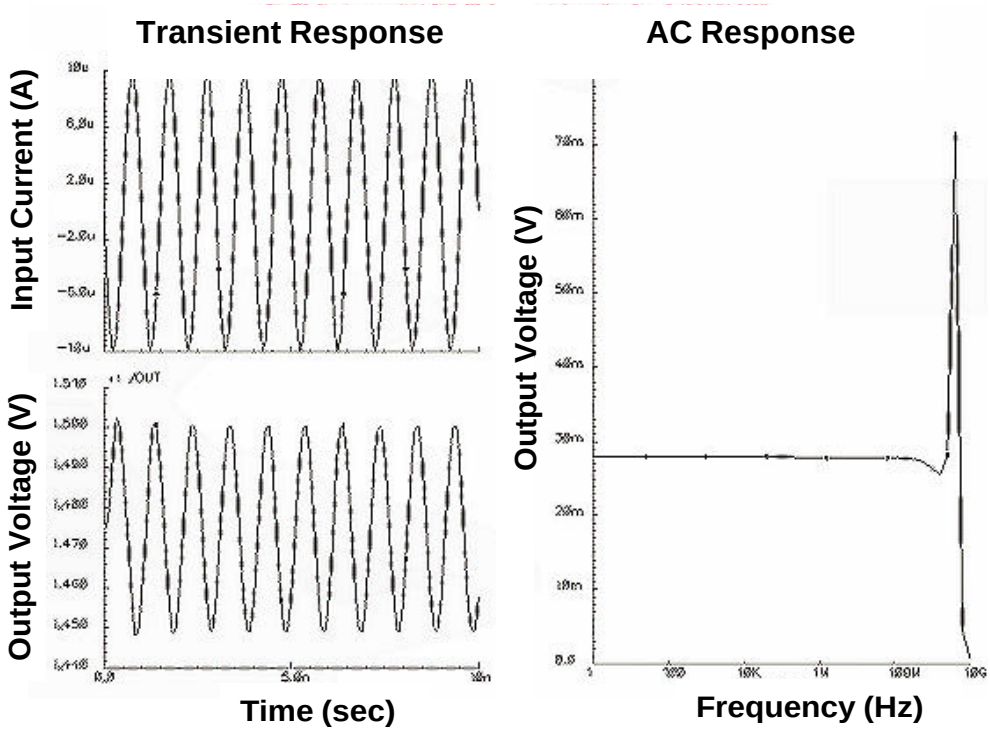


Figure 68 Post-layout simulation result of TIA#13 at 10GHz with I/O Pads

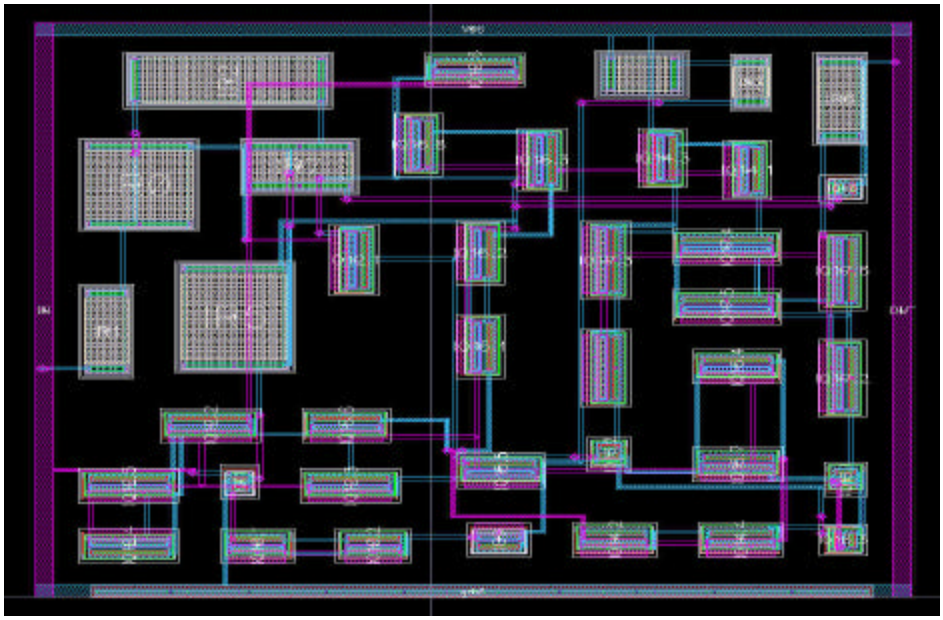


Figure 69 Circuit layout of TIA#13 with I/O Pads

6.2.14 Transimpedance Amplifier # 14

The front end of TIA#14 [79], shown in Figure 70 consists of NPN transistor Q1 as the common emitter amplifier stage followed by two NPN emitter follower stages Q2 and Q3. The bias points for the transistors are optimized using NPN transistors Q5 and Q6. The last stage Q4 is also used as a common emitter stage to give more gain. This circuit topology was designed in custom GaAs-HBT process exhibiting f_T of 40GHz. The Spice simulation result in [79] shows the bandwidth of 9 GHz whereas the Spectre simulation of TIA#14 realized in the IBM SiGe process possesses a bandwidth of 12.50 GHz. This shows the faster operation of IBM SiGe 5HP than GaAs-HBT transistors. Figure 71, Figure 72 and Figure 73 show the pre-layout simulation, post-layout simulation and circuit layout of TIA#14 respectively.

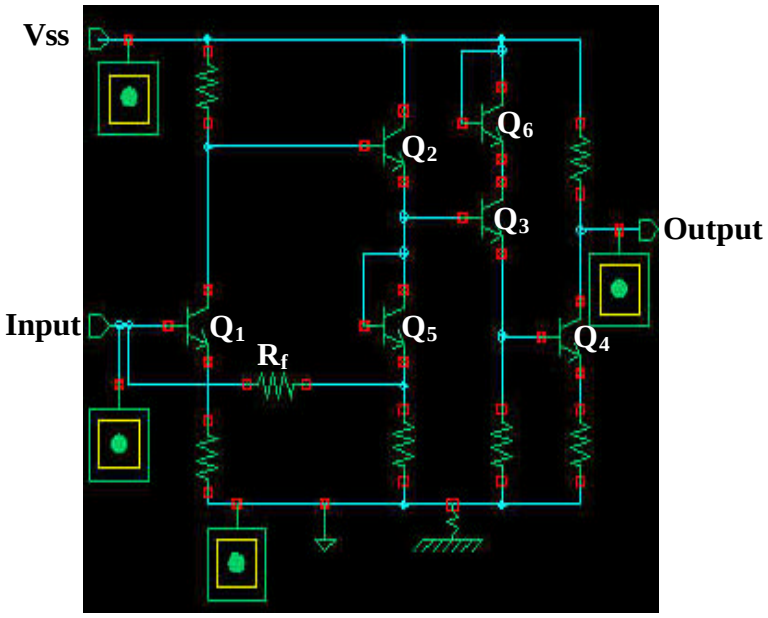


Figure 70 Tansimpedance amplifier #14- Circuit topology

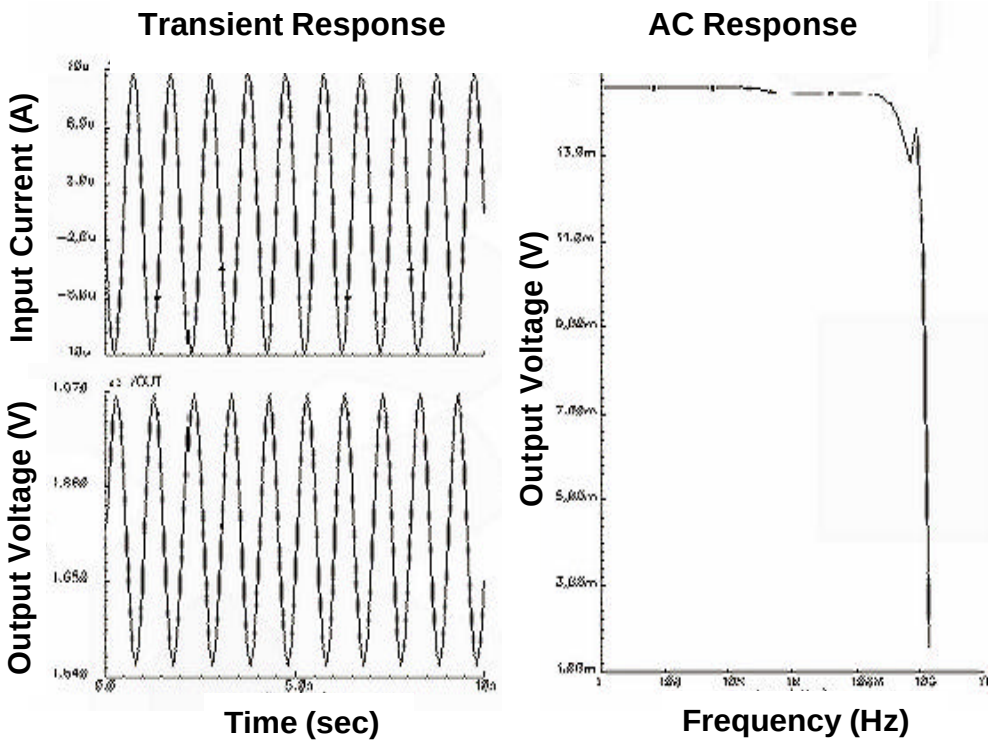


Figure 71 Pre-layout simulation result of TIA#14 at 10GHz

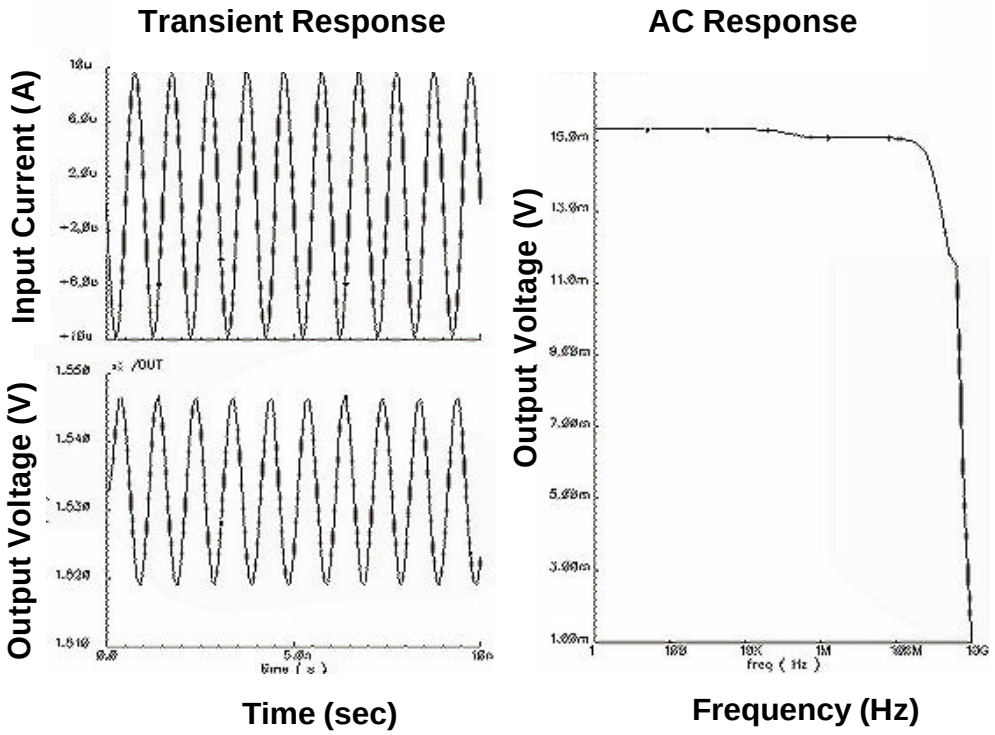


Figure 72 Post-layout simulation result of TIA#14 at 10GHz with I/O Pads

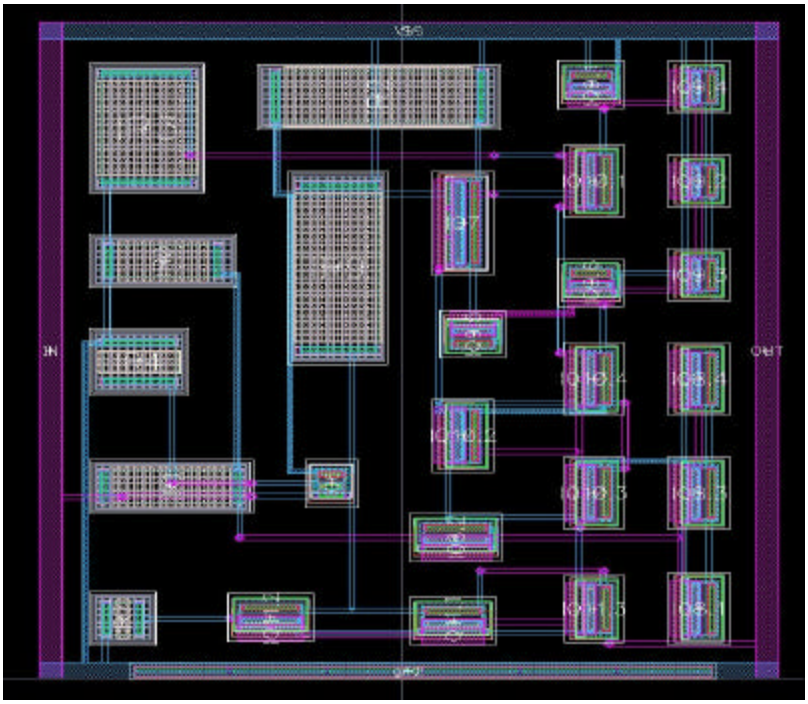


Figure 73 Circuit layout of TIA#14 with I/O Pads

To summarize, based on the requirement of converting photo-current from the SiGe based photodetectors to voltage, fourteen transimpedance amplifier circuits were designed. The transimpedance amplifier designs were based on series-series feedback and shunt-shunt feedback amplifiers. Most of the transimpedance amplifiers simulated using the Spectre simulator show a high gain and bandwidth of 10GHz as shown in Figure 7.

Table 7 Pre-layout and the post-layout simulation results of the transimpedance amplifiers

	Pre-Simulation			Post-Simulation (RCX)		Post-Simulation (RCX with I/O Pads)					
Circuit/ Topology	Output (mV)	Bandwidth (GHz)	Feedback Resistance $R_f(\Omega)$	Output (mV)	Bandwidth (GHz)	Output (mV)	Bandwidth (GHz)	Gain (dB Ω)	Physical Verification by DIVA DRC	EXT	LVS
TIA#1	6.56	10.11	700	6.55	10.18GHz	6.55	9.12GHz	56.32	✓	✓	✓
TIA#2	15.04	9.99	430	14.56	10.14GHz	14.56	9.86GHz	63.26	✓	✓	✓
TIA#3	19.60	9.96	700	19.11	9.84GHz	19.11	2.19GHz	65.62	✓	✓	✓
TIA#4	6.70	10.34	700	6.82	8.41GHz	6.82	8.45GHz	56.67	✓	✓	✓
TIA#5	25.52	10.93	630	24.41	9.54GHz	24.41	9.49GHz	67.75	✓	✓	✓
TIA#6	29.99	6.41	680	29.12	6.01GHz	29.12	5.21GHz	69.28	✓	✓	✓
TIA#7	46.73	3.33	680	47.50	2.97GHz	47.50	2.72GHz	73.53	✓	✓	✓
TIA#8	21.57	9.99	700	21.49	8.59GHz	21.49	1.84GHz	66.64	✓	✓	✓
TIA#9	5.70	10.06	700	5.77	8.33GHz	5.77	8.12GHz	55.22	✓	✓	✓
TIA#10	5.57	5.1	100	5.06	2.94GHz	5.06	2.97GHz	54.08	✓	✓	✓
TIA#11	10.25	10.48	700	10.04	7.96GHz	10.04	5.45GHz	60.03	✓	✓	✓
TIA#12	15.03	10.66	700	14.06	9.04GHZ	14.76	7.96GHZ	63.38	✓	✓	✓
TIA#13	31.06	11.44	580	28.01	7.70GHz	28.01	5.78GHz	68.94	✓	✓	✓
TIA#14	14.60	12.83	690	15.29	8.34GHz	15.29	4.22GHz	63.69	✓	✓	✓

These transimpedance amplifiers were optimized using the NeoCircuit analog synthesis tool. The output simulation result for pre-layout and post-layout simulation of the fourteen transimpedance amplifiers is summarized in Table 7. All the designed TIAs were laid out and verified by performing physical verification using DIVA. On verification, all the parasitic extracted in the layout were back annotated to the schematic to perform post-layout simulation. The output and the input signals of each transimpedance amplifier were connected to the input/output wire bond pads. The main objective for this is to test the practicality of transimpedance amplifiers independently. Due to the load by the pads there is a general decrease in the bandwidth of the transimpedance amplifiers observed in Table 7.

For comparison, the transimpedance amplifiers TIA9 to TIA#14 which were designed in other custom SiGe and GaAs processes and implemented in the IBM SiGe process demonstrate enhancement in gain, speed and bandwidth as summarized in Table 8.

Table 8 Comparison of TIAs design implemented in the IBM SiGe process

Output results of TIA implemented in the IBM SiGe process discussed above				**Output results of TIA implemented in other custom SiGe and GaAs technology**			
TIA	**Output (mV)**	**Bandwidth (GHz)**	**Gain (dBW)**	**Process Technology**	**Gain (dBW)**	**Bandwidth (GHz)**	**f_T and f_{MAX} (GHz)**
TIA#9	5.77	8.33	55.22	SiGe [75]	62	2.7	45
TIA#10	5.06	2.94	54.08	Si [76]	60	0.96	-
TIA#11	10.04	7.96	60.03	SiGe [77]	45.2	3.2	23 and 34
TIA#12	14.06	9.04	62.95	GaAs [78]	-	-	100 and 200
TIA#13	28.01	7.70	68.94	GaAs [78]	-	-	100 and 200
TIA#14	15.29	8.34	63.68	GaAs [79]	-	9.0	40

7.0 OPTICAL RECEIVERS BASED ON SiGe HBT TRANSISTOR

In the previous Chapter, it is seen how the output current from the photodetectors gets converted into a voltage using transimpedance amplifiers. The output voltage of the transimpedance amplifier is observed to be in the range of millivolts for a 10μamp input current. This output from the TIAs is not high enough for digital signal processing. Therefore, the output of the transimpedance amplifier is followed by multi-stage low noise differential amplifiers. These differential amplifiers convert the millivolt output of the TIAs in to suitable voltages to feed the last stage of an optical receiver know as decision circuit. The decision circuit compares the output of the circuit to a threshold level and determines whether the signal element is a binary '1' or a binary '0'. The digital signal can be processed further using this '1' and '0' pattern. Figure 74 shows a block diagram for a complete receiver circuit. We have already discussed the design of SiGe photodetectors in Chapter 5 and transimpedance amplifier circuit designs in Chapter 6. In this chapter, different ways of amplifying the TIA outputs with multistage cascaded low noise differential amplifiers, voltage amplifiers and low noise amplifiers to build complete optical receivers are presented. These complete receiver circuits are based on two transimpedance amplifiers selected from Table 7.

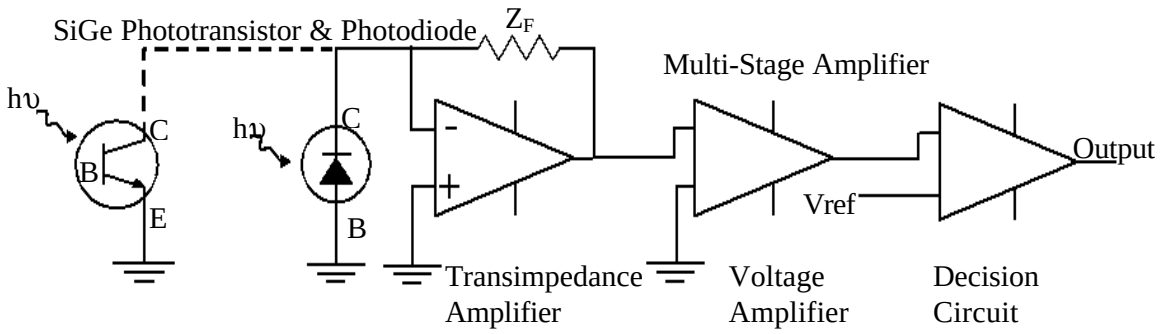


Figure 74 Block diagram for an optical receiver system

7.1 RECEIVER CIRCUIT # 1

The complete circuit schematic of receiver circuit #1 is shown in Figure 75, in which TIA#11 is used to build the front-end. The front-end of the receiver circuit consists of the transimpedance amplifier TIA#11 discussed above followed by three differential amplifier stages Q1-Q2, Q3-Q4 and Q5-Q6 biased differentially using NFET transistors N1, N2, N3 respectively. The output of the first differential stage is taken double ended in order to achieve a maximum gain [80] from the first stage. The output of the third differential amplifier is taken single ended followed by a Darlington pair buffer stage of Q7 and Q8 to buffer the output without distorting the amplified voltage signal from the previous differential stages. The last stage is the decision circuit stage which is a simple inverting stage formed with transistor P1 as a PMOS transistor and N5 as an NMOS transistor. This inverting stage compares the output of the buffer circuit to a threshold level, set by the gate thresholds (V_{th}) to determine if the signal element is a binary '1' or a binary '0'. Figure 76 shows the output results for all the intermediate stages of a receiver circuit for an input current of 10μamps.

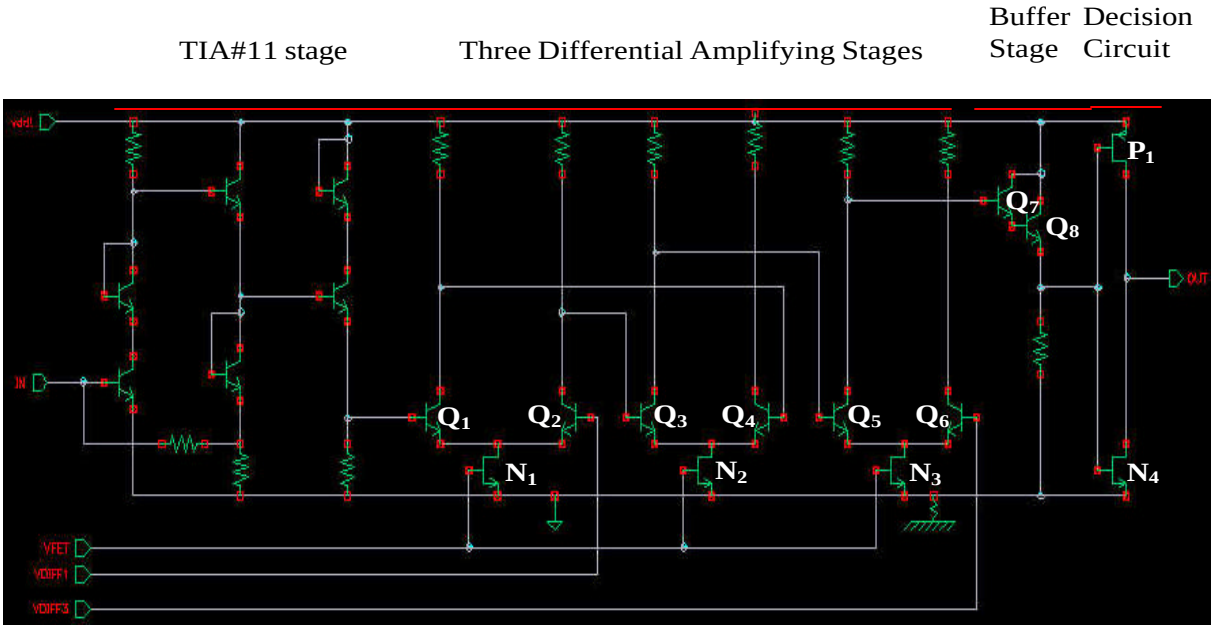


Figure 75 Receiver circuit #1- Circuit topology

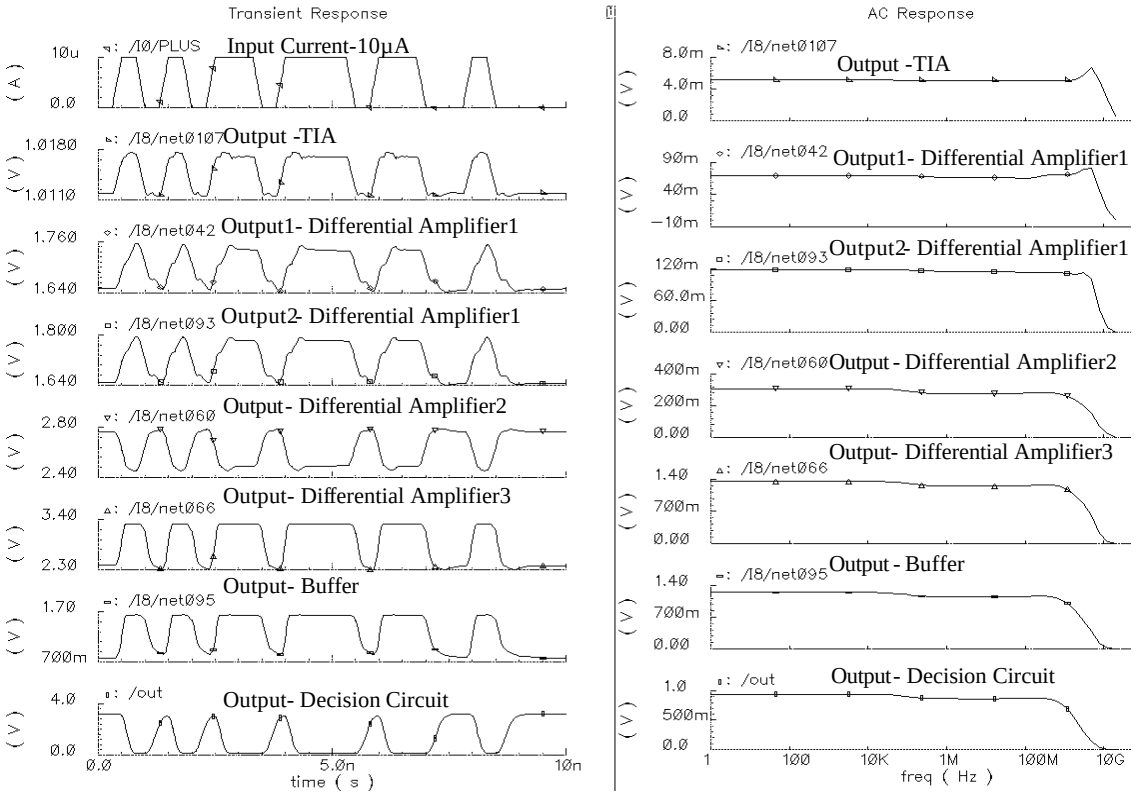


Figure 76 Output simulation results for receiver circuit#1

7.2 RECEIVER CIRCUIT # 2

The second complete receiver circuit is shown in Figure 77. The front end of the second receiver circuit consists of TIA#14 followed by a common emitter stage Q1 with a feedback resistance Re. This stage is used to enhance the output voltage of the pre-amplifying TIA stage and to have high bandwidth. The next stage consists of NPN transistor Q2 which acts as an emitter follower to buffer the output of the common emitter stage to the following differential stages [80]. In receiver circuit #2, the cascaded differential amplifier is different from the differential stages in receiver circuit #1 in terms of the way they are biased. In this circuit the two differential stages Q3, Q4 and Q5, Q6 are biased using a resistor and a common collector stage. The output of the first differential stage is taken double ended.

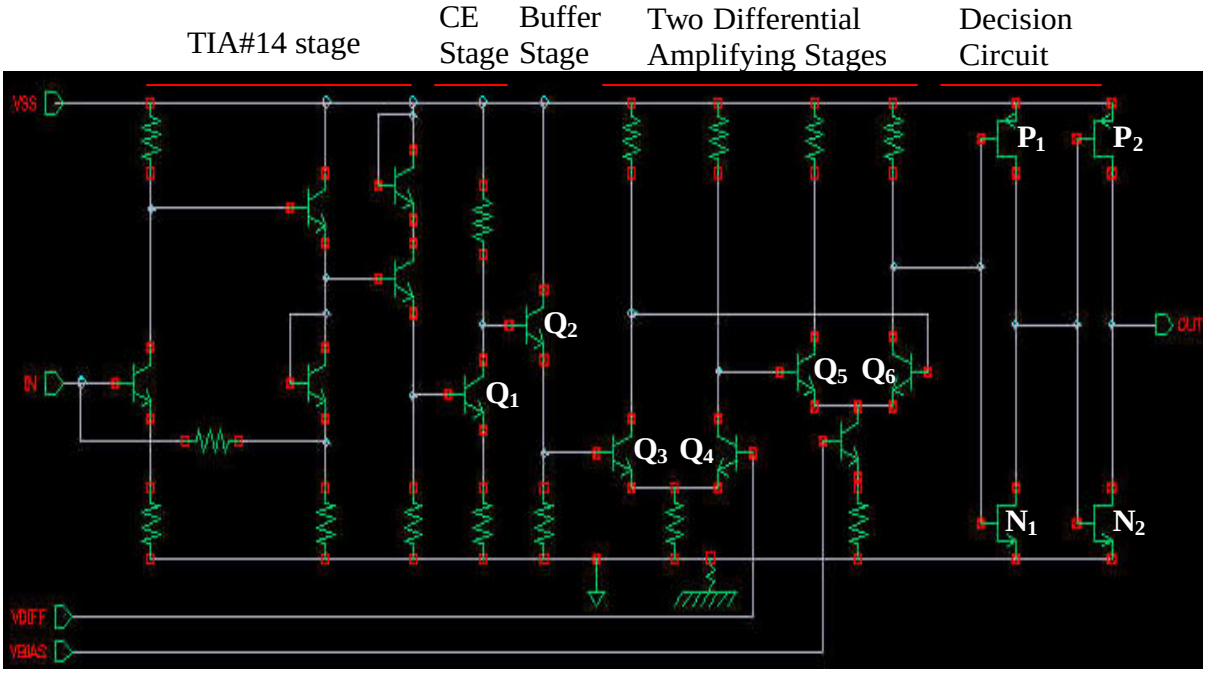


Figure 77 Receiver circuit #2- Circuit topology

The output of the second differential stage is single ended followed by two cascaded inverter stages P1 N1 and P2 N2 respectively. The two cascaded inverter stages are used in order to get a faster rise and fall time. The output waveform for all the intermediate stages is seen in Figure 78. Both receiver circuits have been simulated successfully with an input piecewise linear model at 2Gb/s.

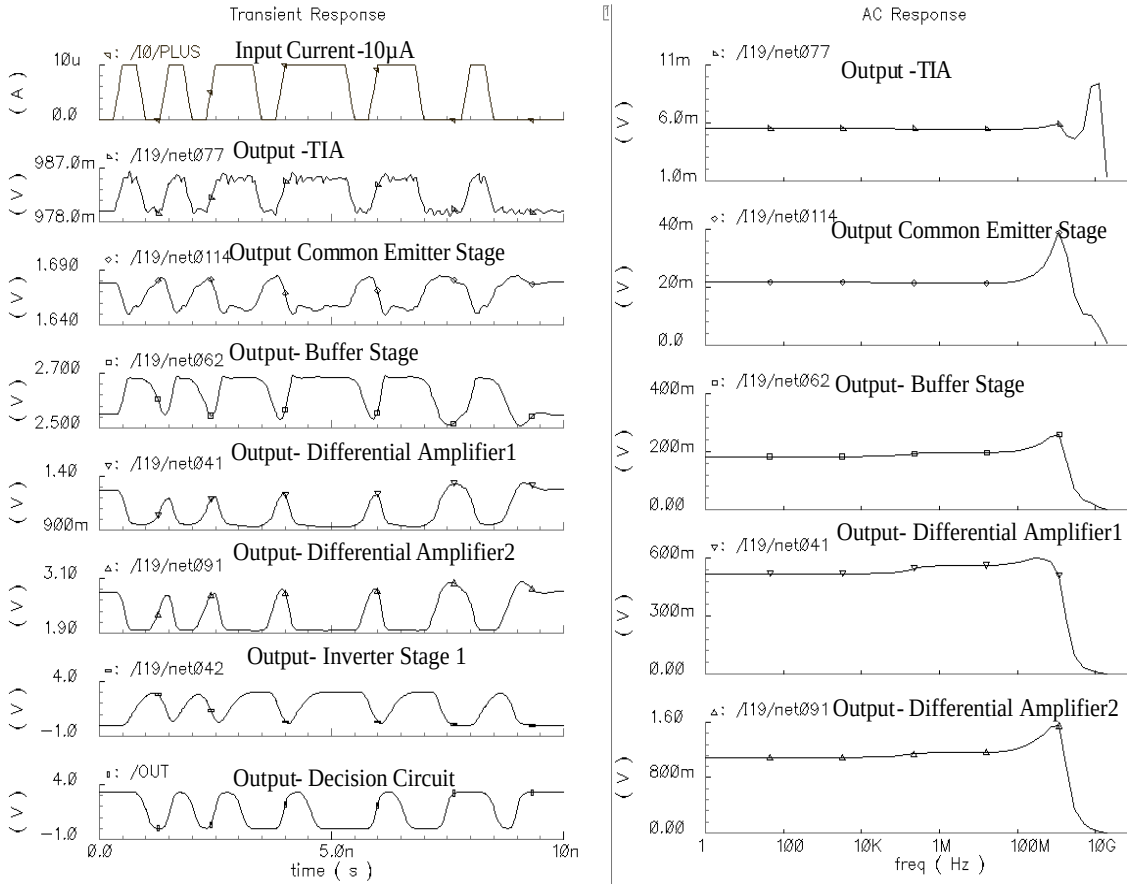


Figure 78 Output simulation results for receiver circuit#2

7.3 SiGe OPTOELECTRONICS RECEIVER CHIP LAYOUT

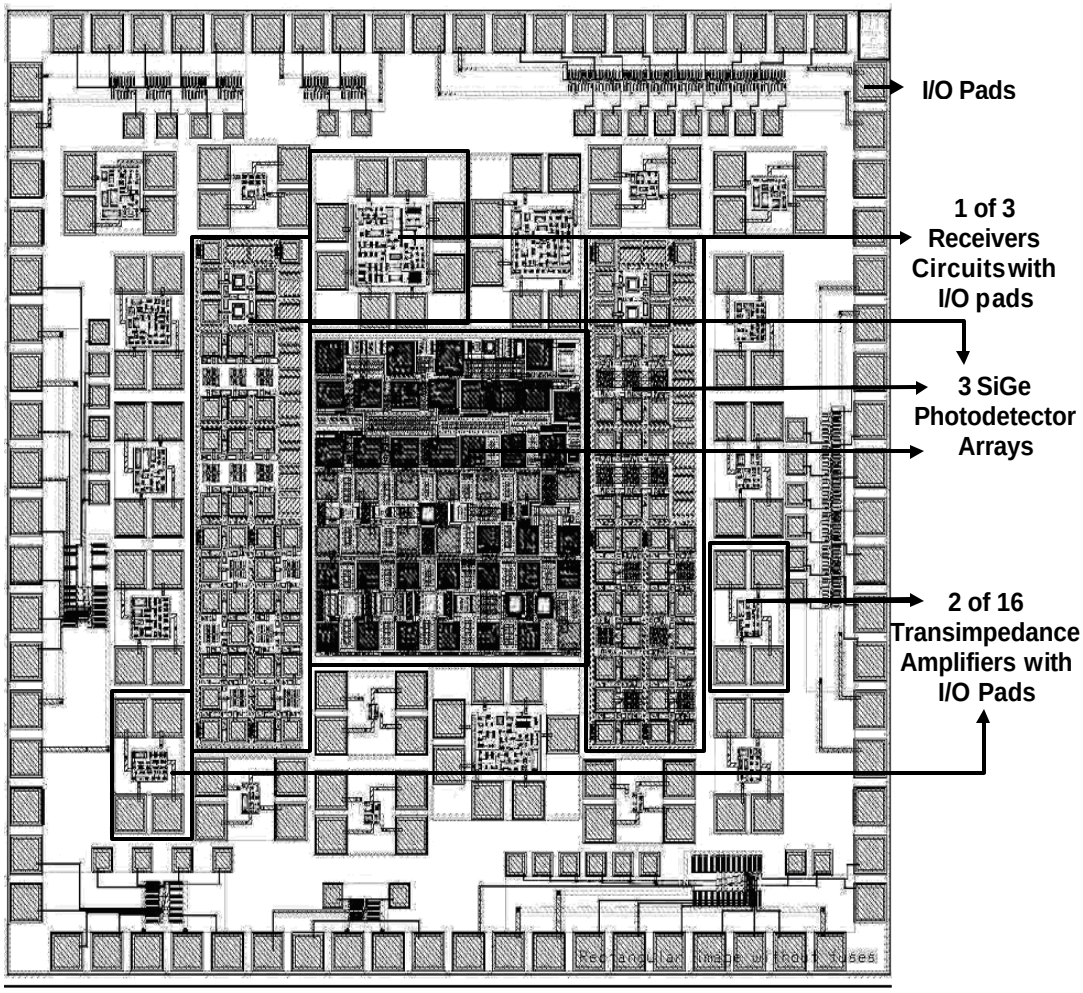


Figure 79 Test chip layout (3x3.3mm) showing the 16 transimpedance amplifiers, two receiver circuits and three different test structures for SiGe photodetectors arrays

7.4 TEST RESULTS

The SiGe photodetectors, transimpedance amplifiers and optical receiver circuits were designed and fabricated through MOSIS in the IBM SiGe (0.5 micron) process. Out of the fourteen transimpedance amplifiers fabricated, TIA#3, TIA#4, TIA#6, TIA#7 and TIA#14 were tested using the probing facilities in the Department of Computer Science at the University of

Pittsburgh. Figure 80 illustrates the test setup to measure the performance of these transimpedance amplifiers.

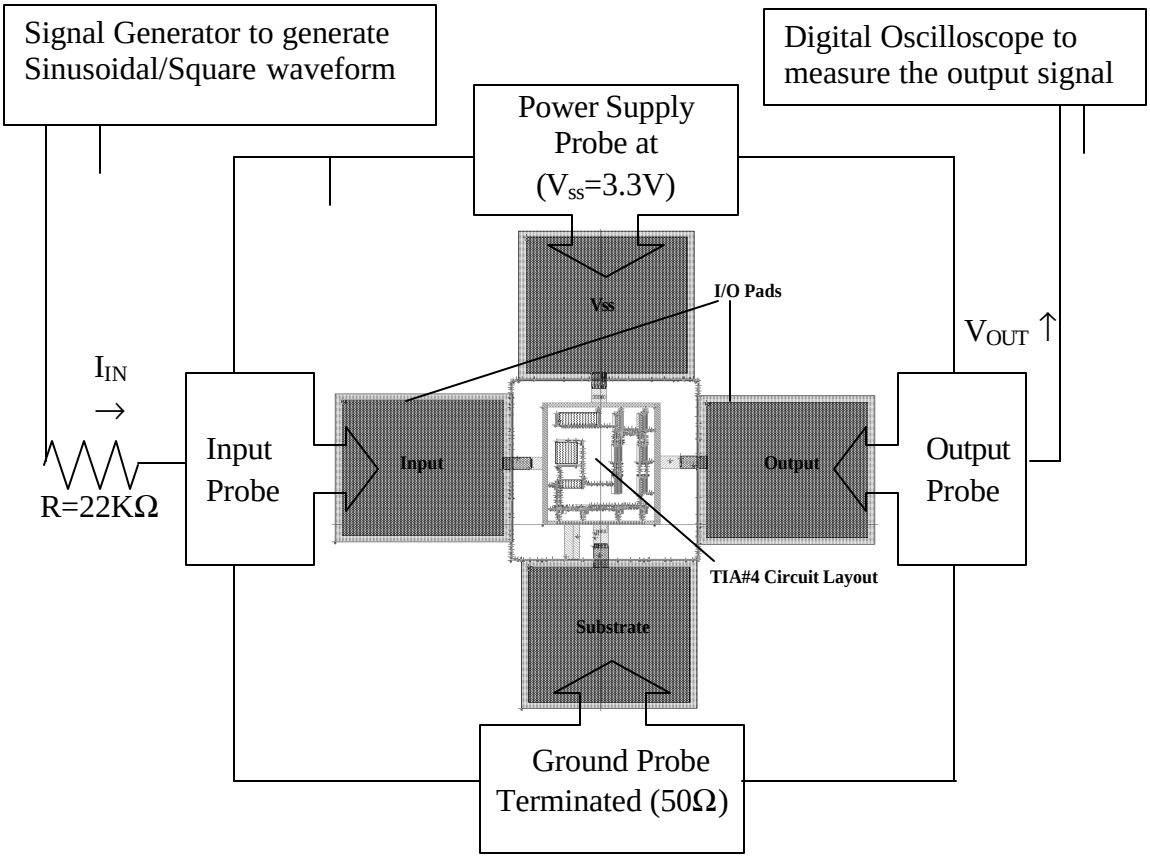


Figure 80 Block diagram of the test setup

As shown in Figure 80, the input signal is generated by a signal generator connected in series with a resistor to create an input current for the transimpedance amplifier. The output voltage converted by the transimpedance amplifier is sensed by a high precision probe which is connected to an oscilloscope to display the input and the output signal. The power supply probe and the ground probe are used to provide a supply voltage of 3.3 volts and common ground to the amplifier. The preliminary measurement results for transimpedance amplifier#4 at 200MHz are summarized in Figure 81.

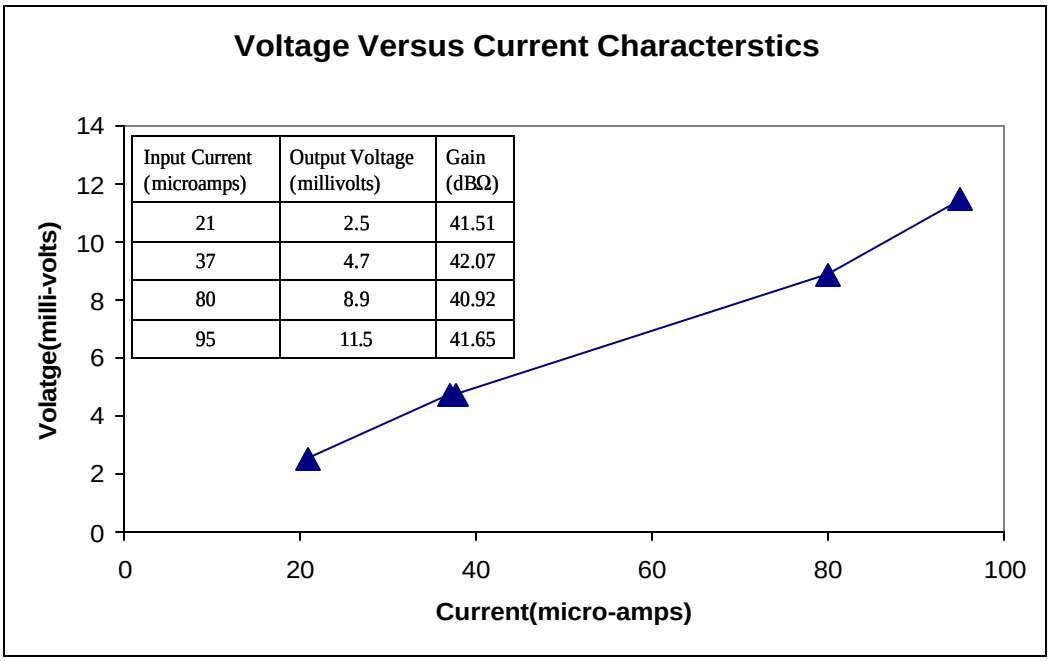


Figure 81 Voltage versus current characteristics of Transimpedance amplifier#4

Figure 81 should be compared to the simulation results of TIA#4 in Table 7 which shows an output gain of 56.67dBΩ at 8.45GHz in Table 7. We believe that much of the discrepancy comes from the limitation in the available testing facilities. The total power dissipation in TIA#4 is 19.8mW which agrees with the simulation results. The preliminary test result for transimpedance amplifier #7 is summarized in Figures 82 - 87. Figures 82 and 83 show the input and the output signal of transimpedance amplifier #7 at 1MHz. Figures 84 and 85 show the input and the output signal of TIA #7 at 10MHz. Figures 86 and 87 show the input and the output signal of TIA#7 at 100MHz.

The preliminary test results for TIA #3, TIA #6, and TIA #14 at different frequencies are shown in Figures 88 through 107. These preliminary results show that the transimpedance amplifiers are working, however they are not performing as well as predicted. This could be for

several reasons including the limited capabilities of the current test environment. Further testing will continue.

TIA#7

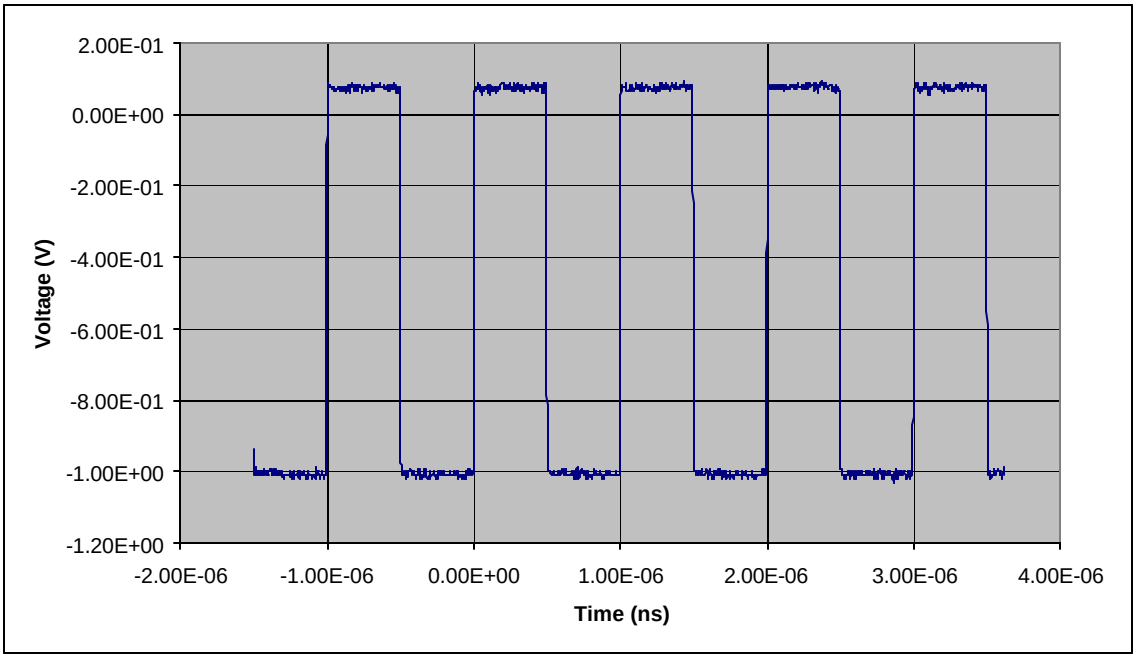


Figure 82 Input waveform of TIA#7 at 1MHz

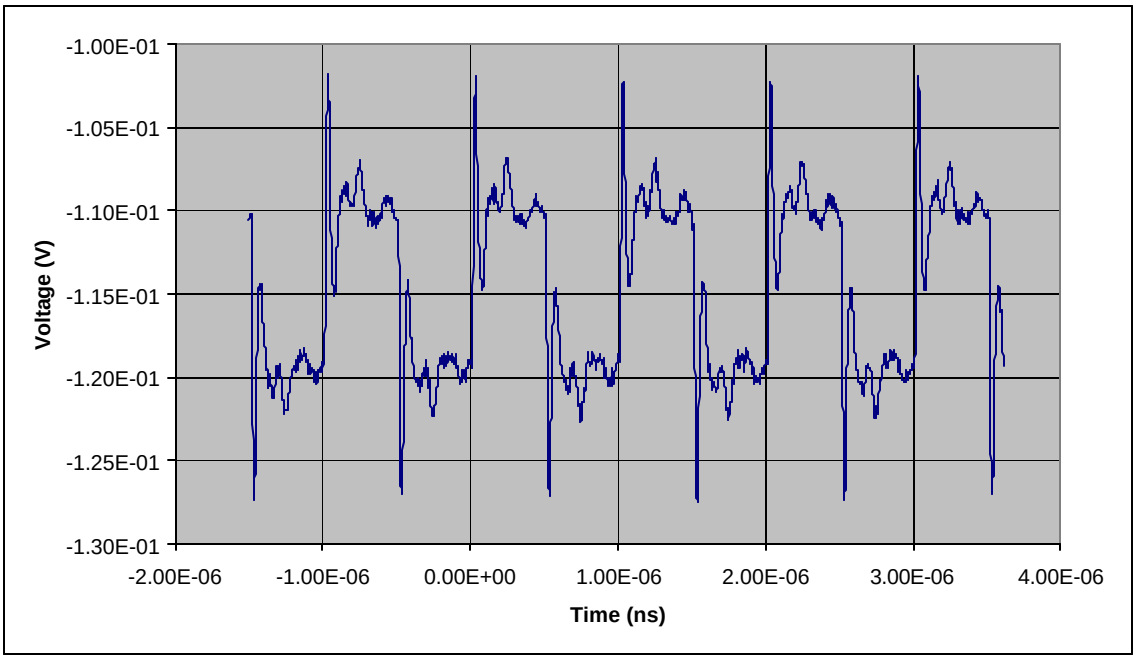


Figure 83 Output waveform of TIA#7 at 1MHz

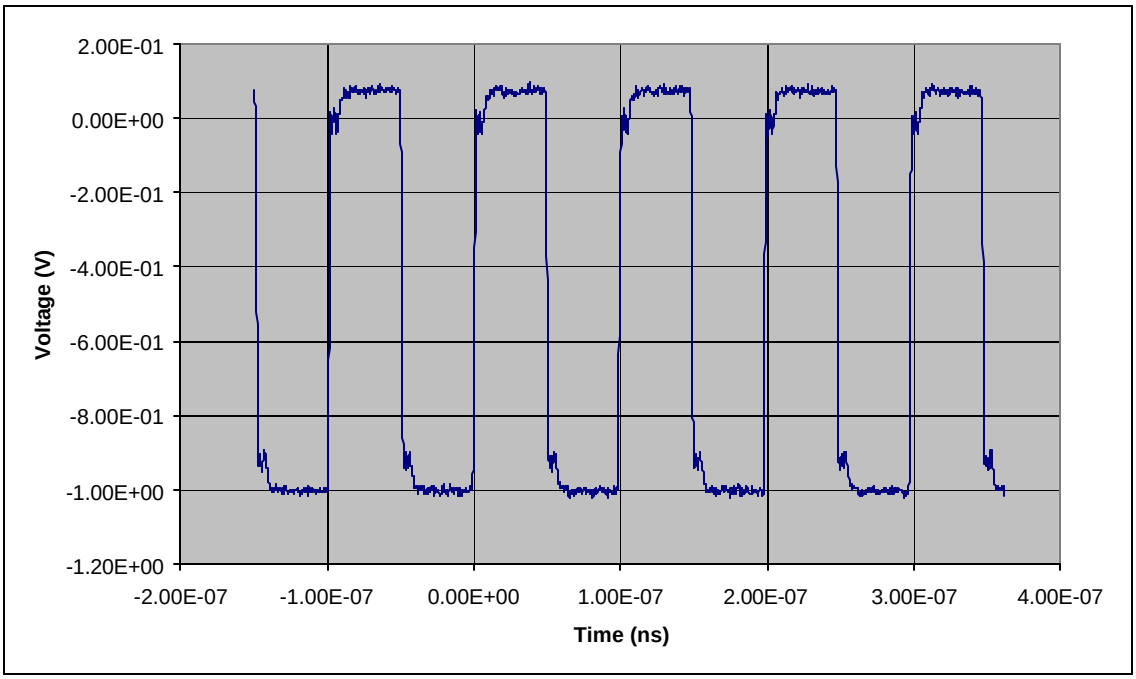


Figure 84 Input waveform of TIA#7 at 10MHz

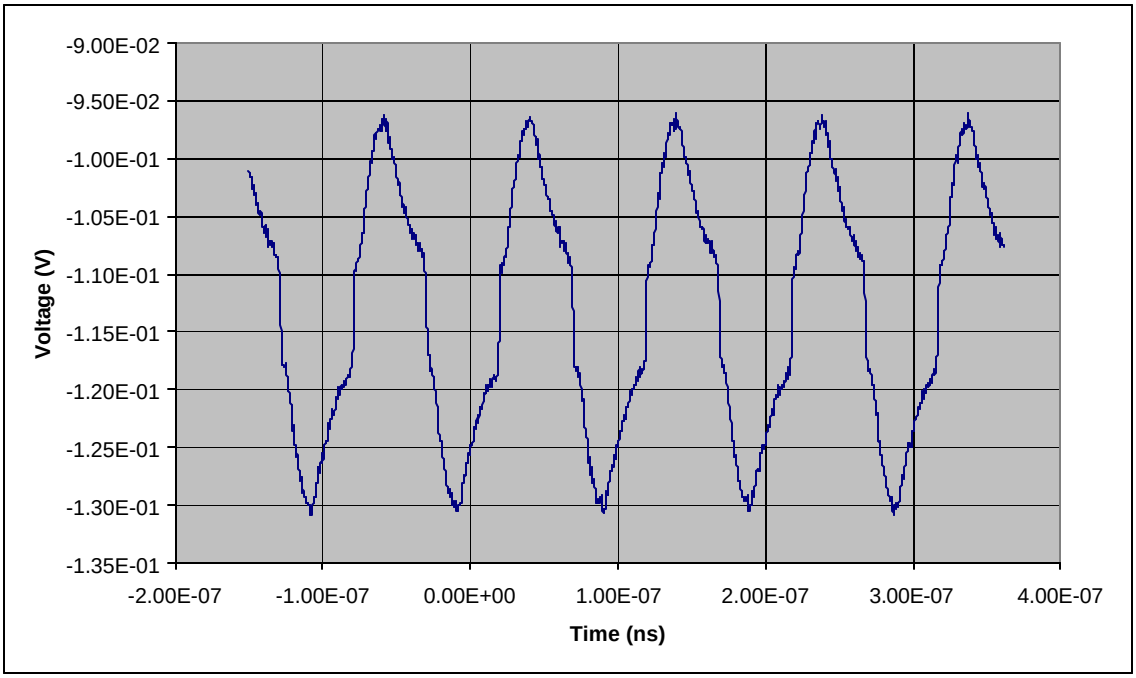


Figure 85 Output waveform of TIA#7 at 10MHz

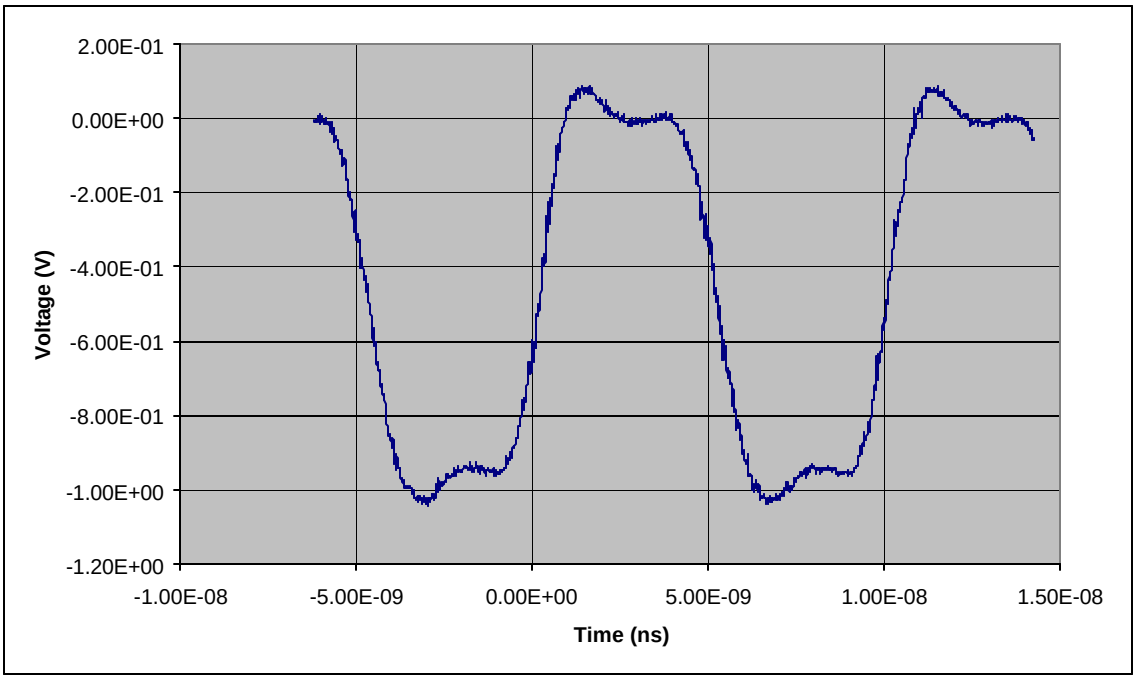


Figure 86 Input waveform of TIA#7at 100MHz

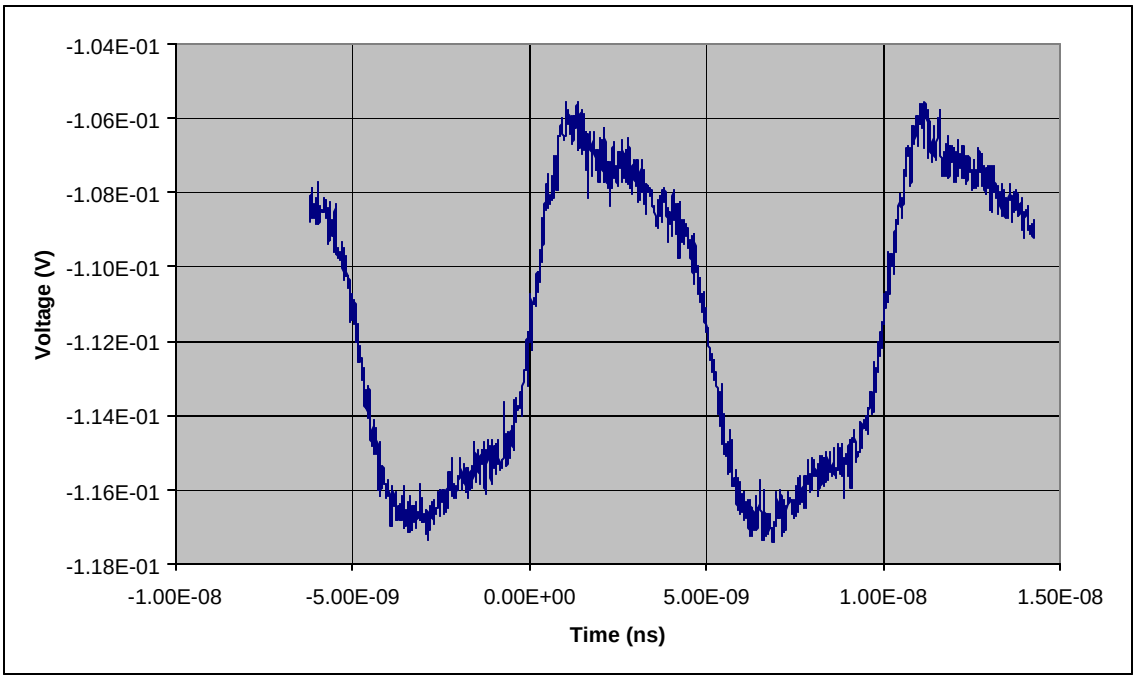


Figure 87 Output waveform of TIA#7 at 100MHz

TIA#3

Supply Current – 4mA

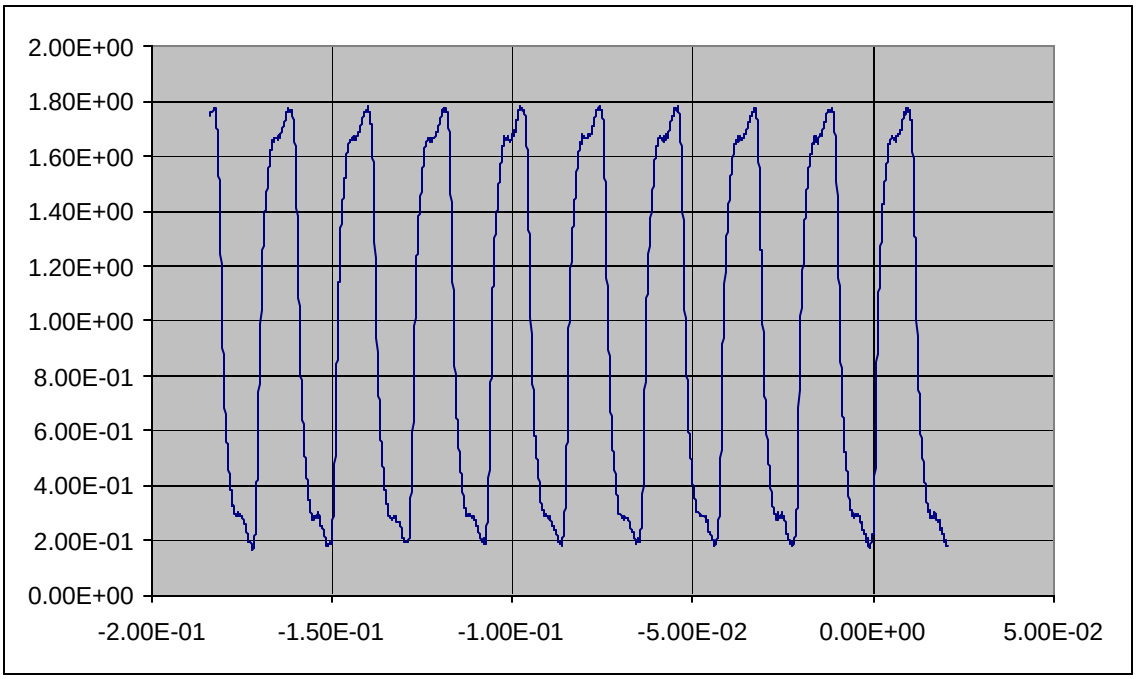


Figure 88 Input waveform of TIA#3 at 50MHz

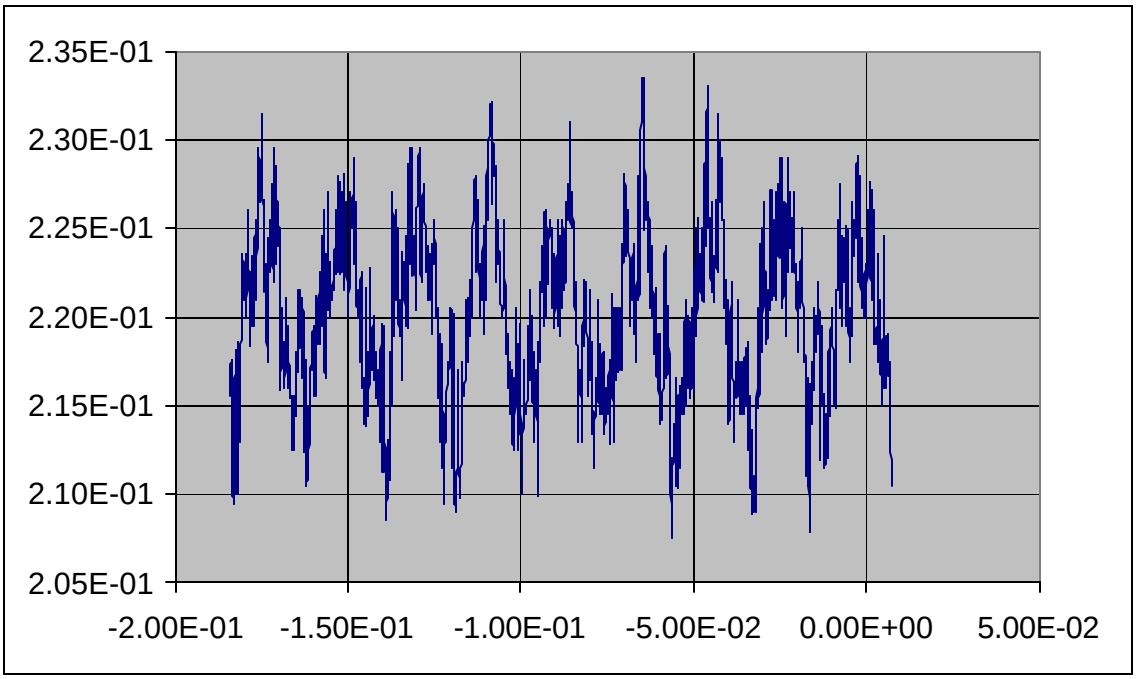


Figure 89 Output waveform of TIA#3 at 50MHz

TIA#6

Supply Current – 12mA

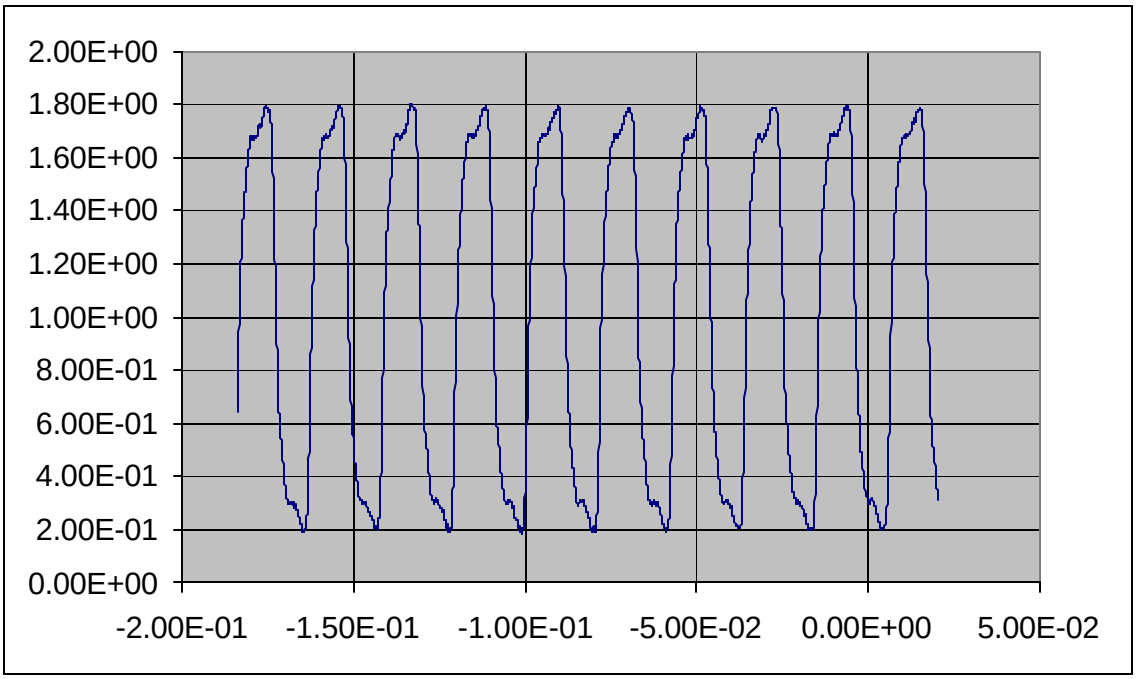


Figure 90 Input waveform of TIA#6 at 50MHz

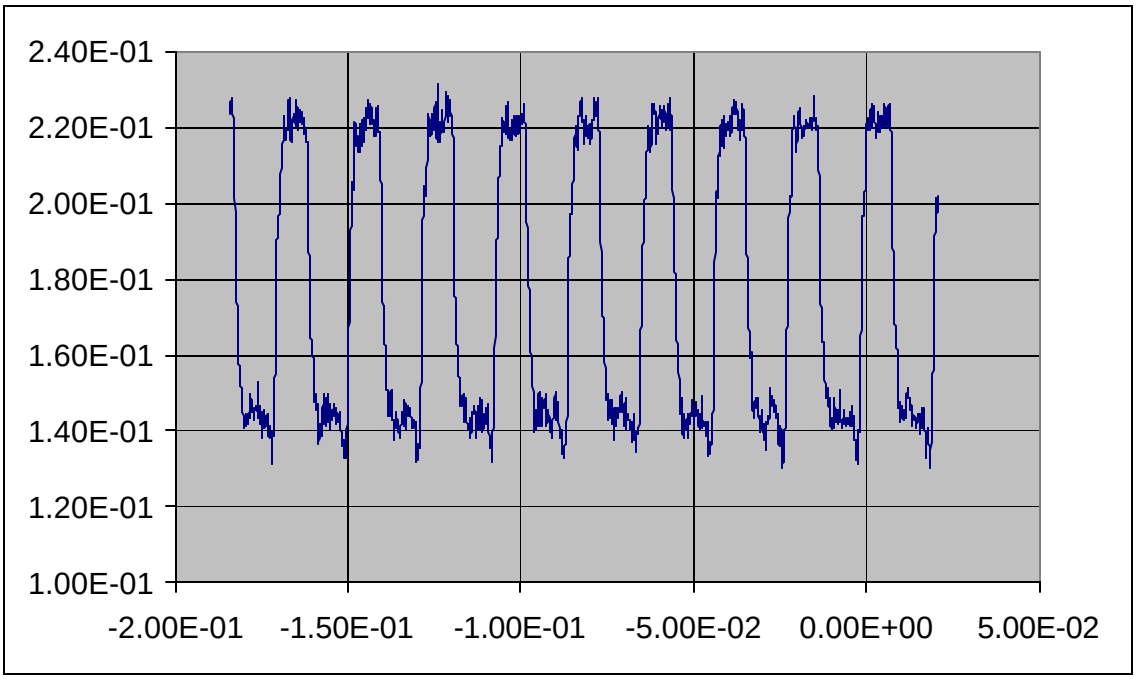


Figure 91 Output waveform of TIA#6 at 50MHz

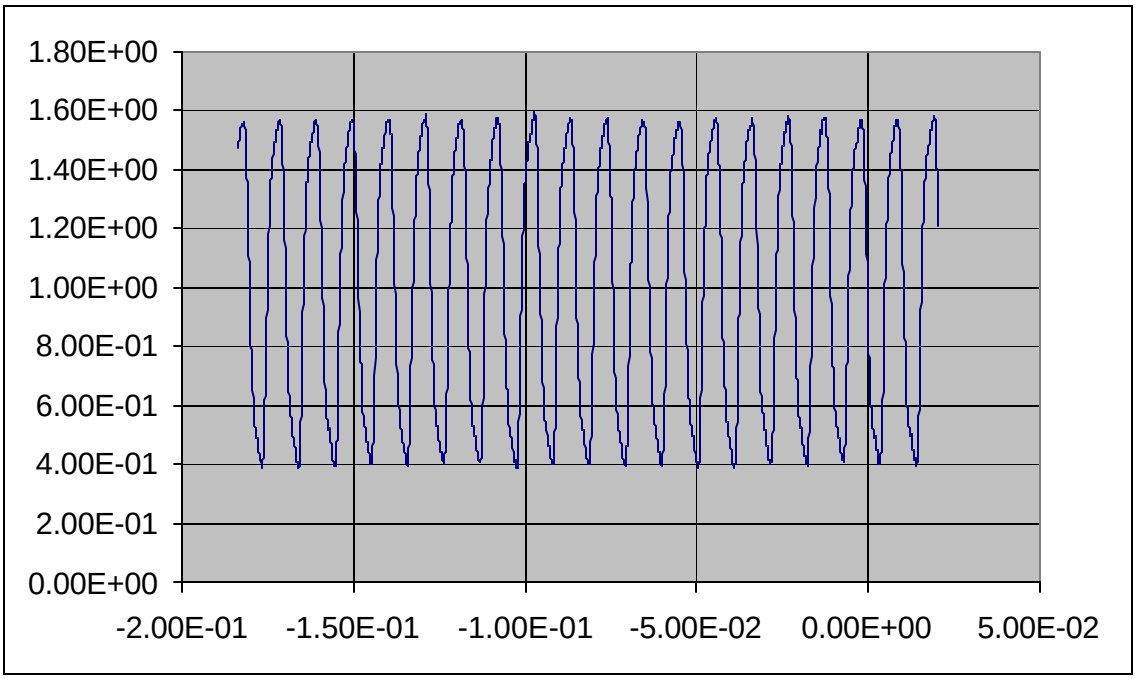


Figure 92 Input waveform of TIA#6 at 100MHz

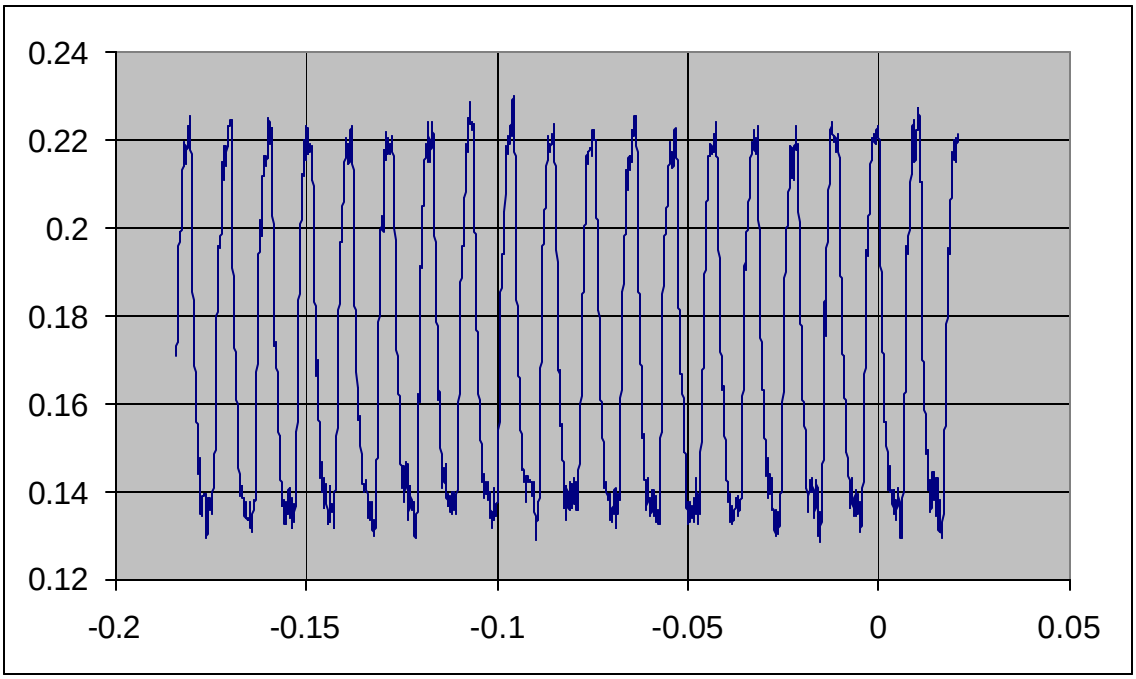


Figure 93 Output waveform of TIA#6 at 100MHz

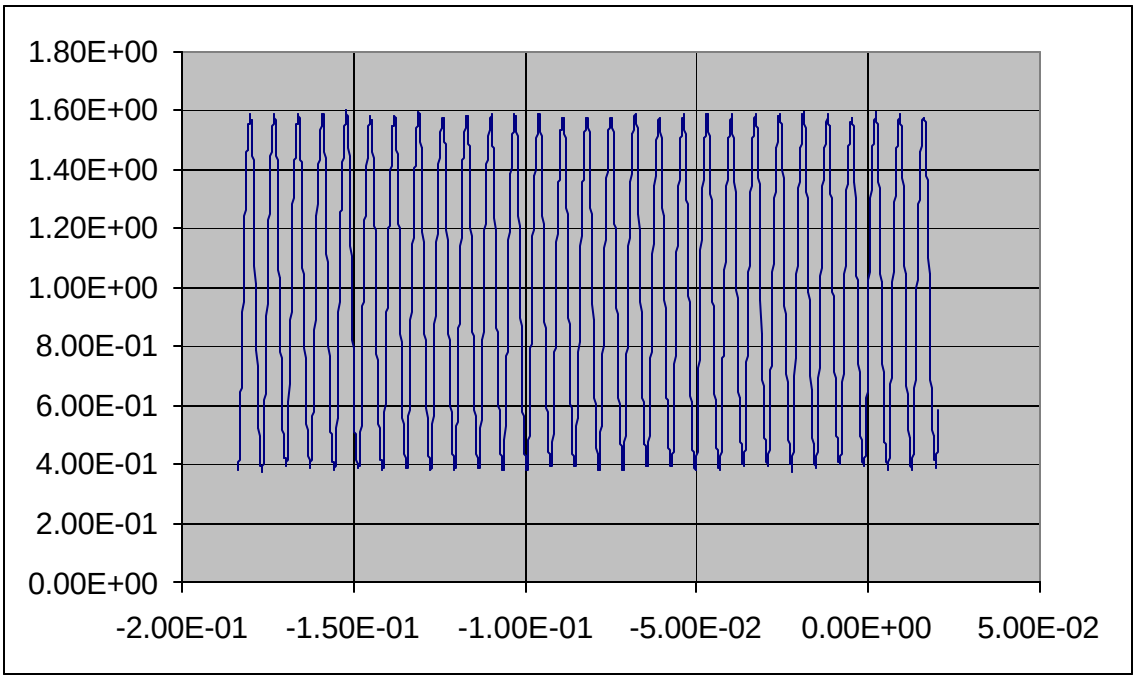


Figure 94 Input waveform of TIA#6 at 150MHz

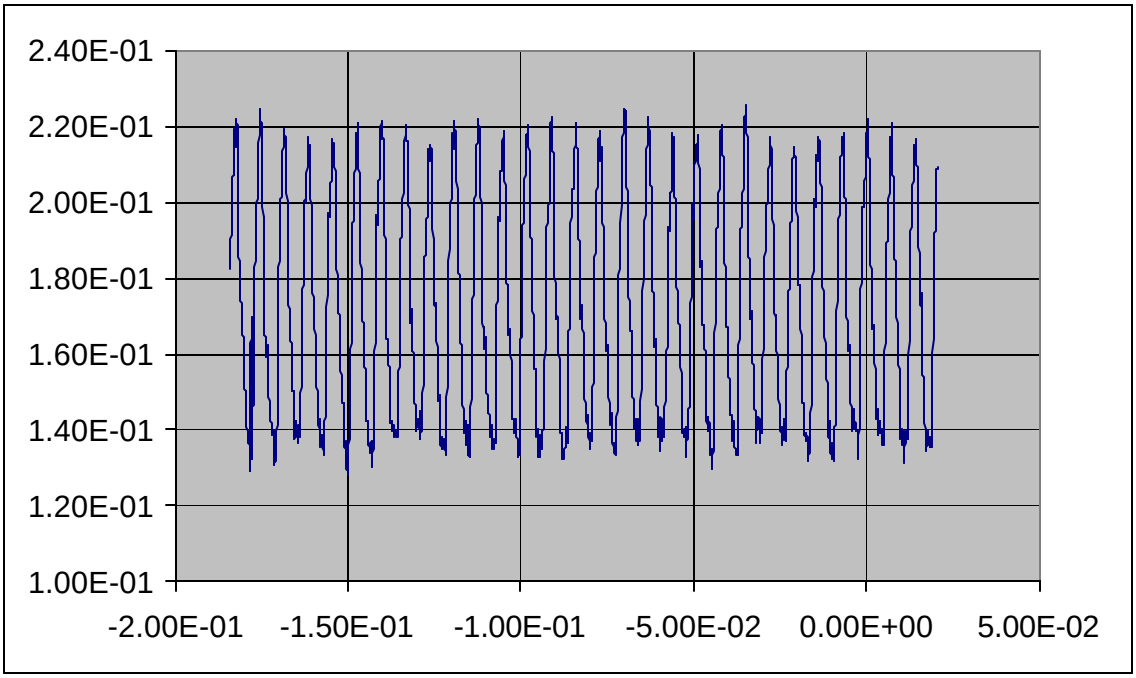


Figure 95 Output waveform of TIA#6 at 150MHz

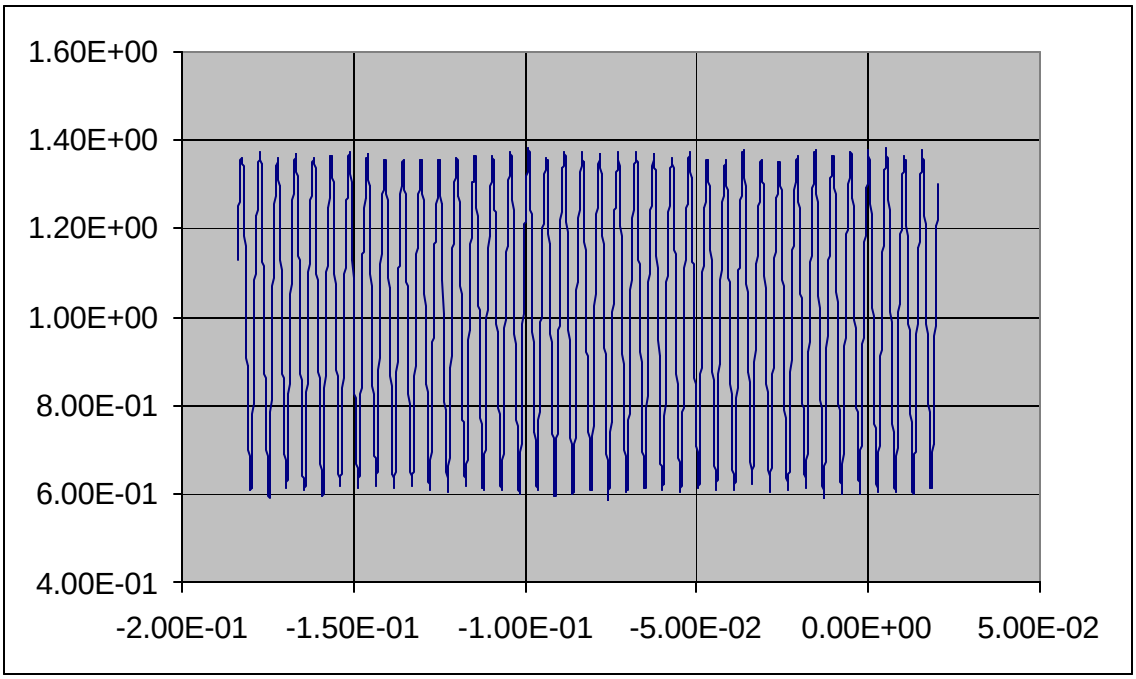


Figure 96 Input waveform of TIA#6 at 200MHz

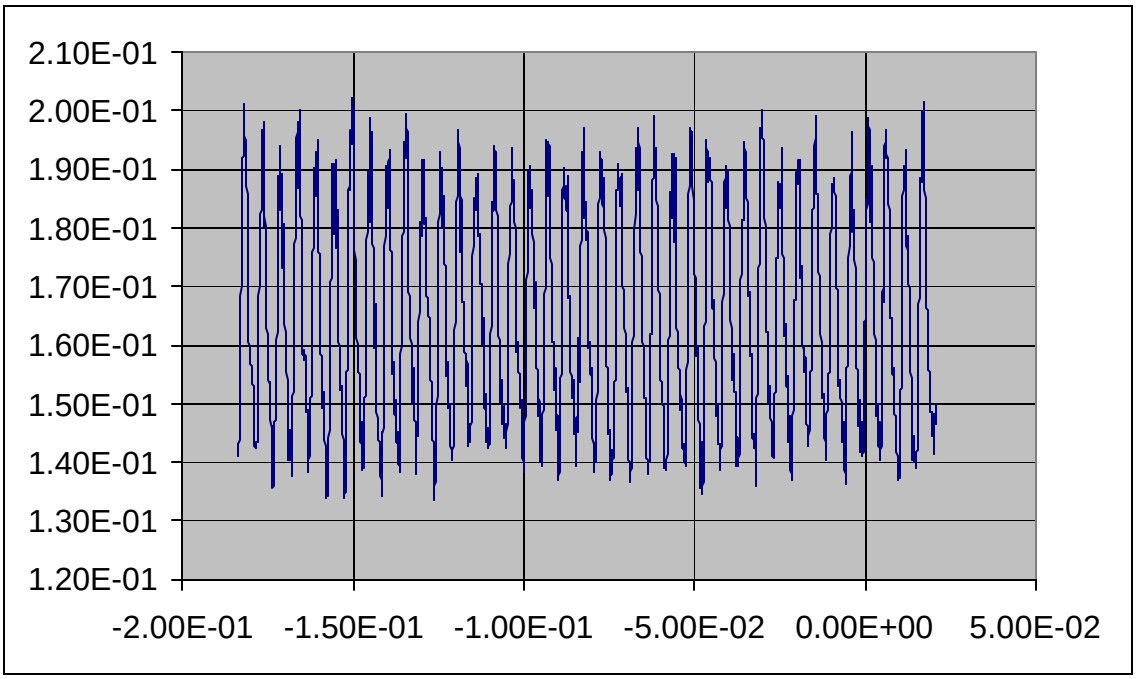


Figure 97 Output waveform of TIA#6 at 200MHz

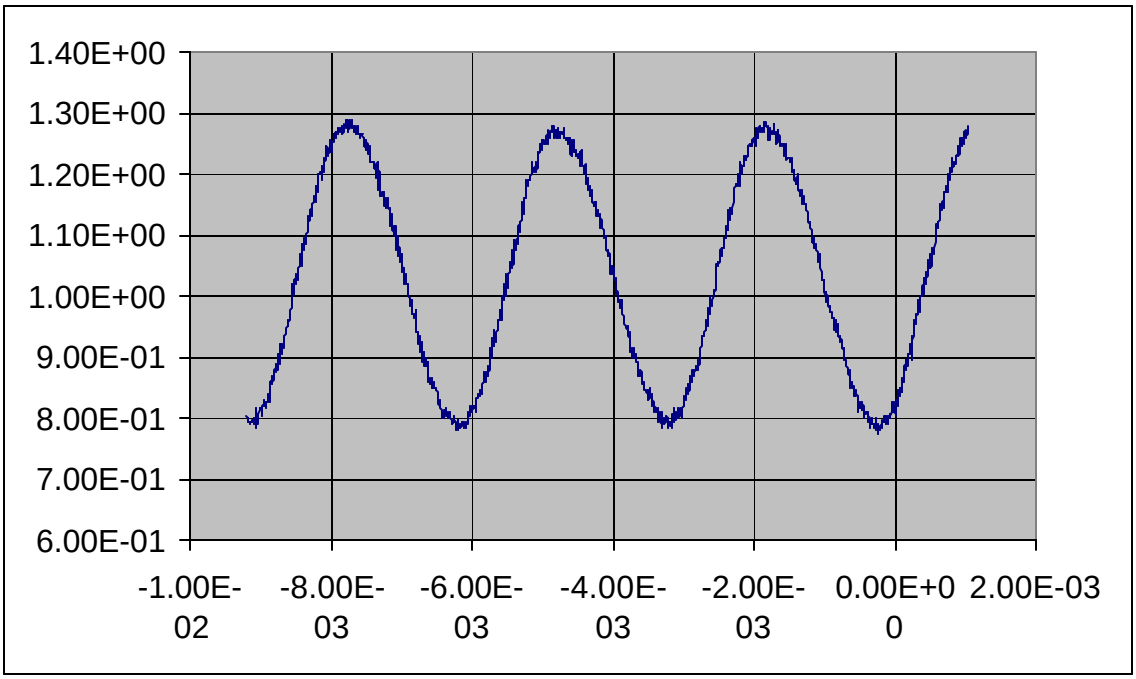


Figure 98 Input waveform of TIA#6 at 350MHz

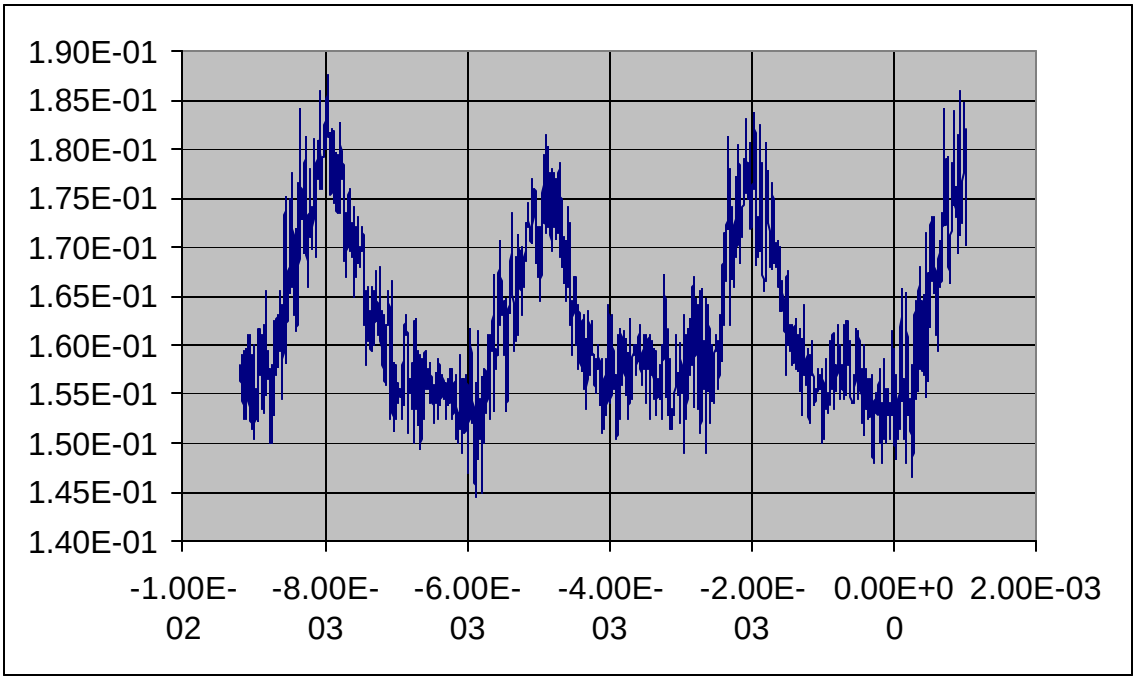


Figure 99 Output waveform of TIA#6 at 350MHz

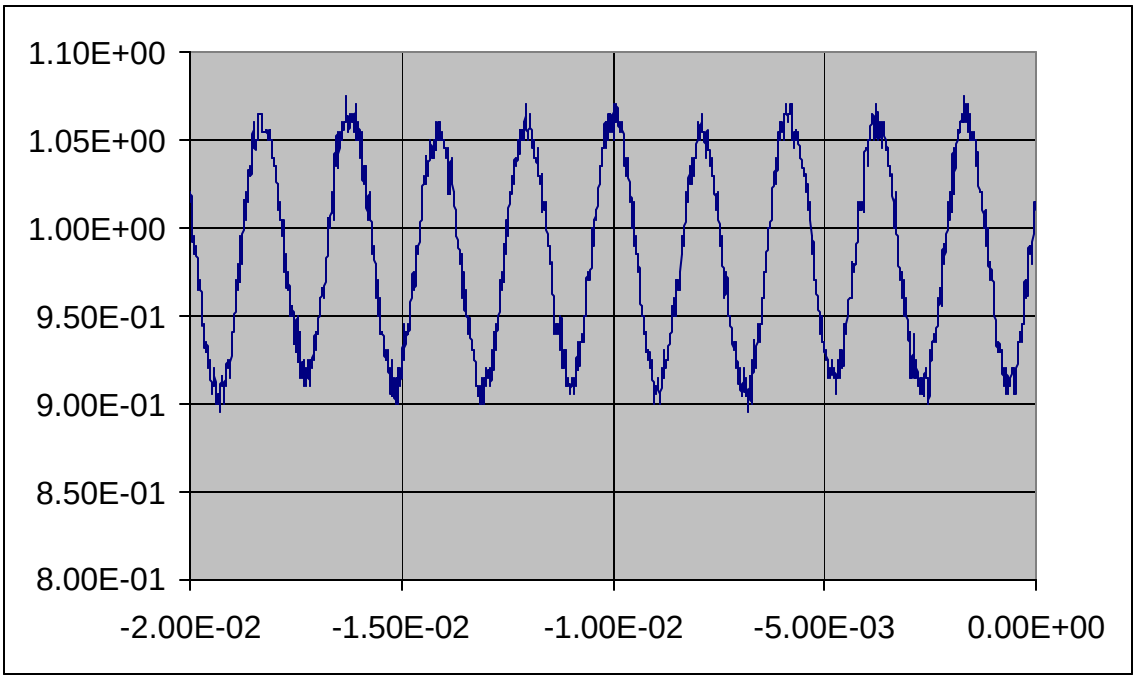


Figure 100 Input waveform of TIA#6 at 500MHz

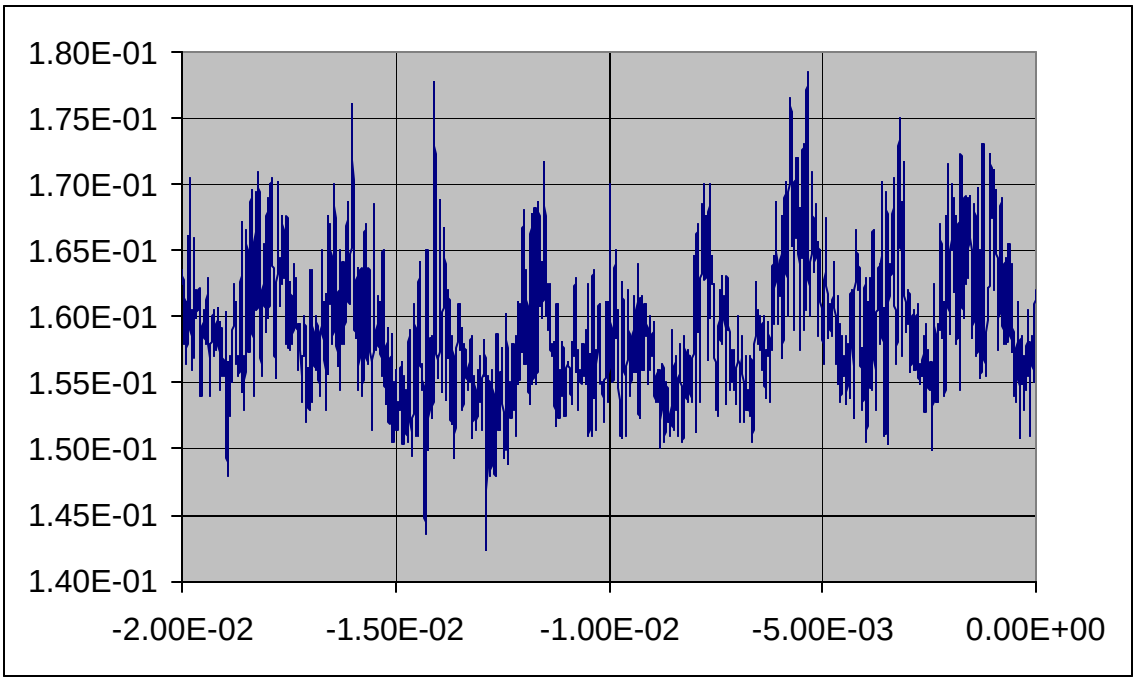


Figure 101 Output waveform of TIA#6 at 500MHz

TIA#14

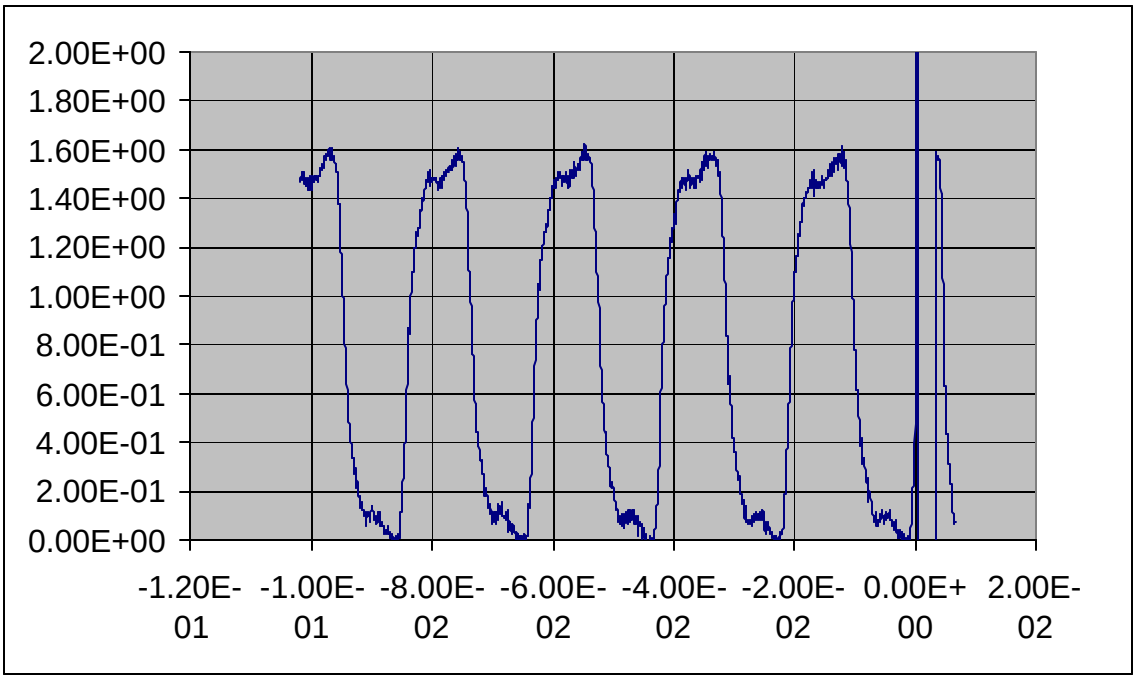


Figure 102 Input waveform of TIA#14 at 50MHz

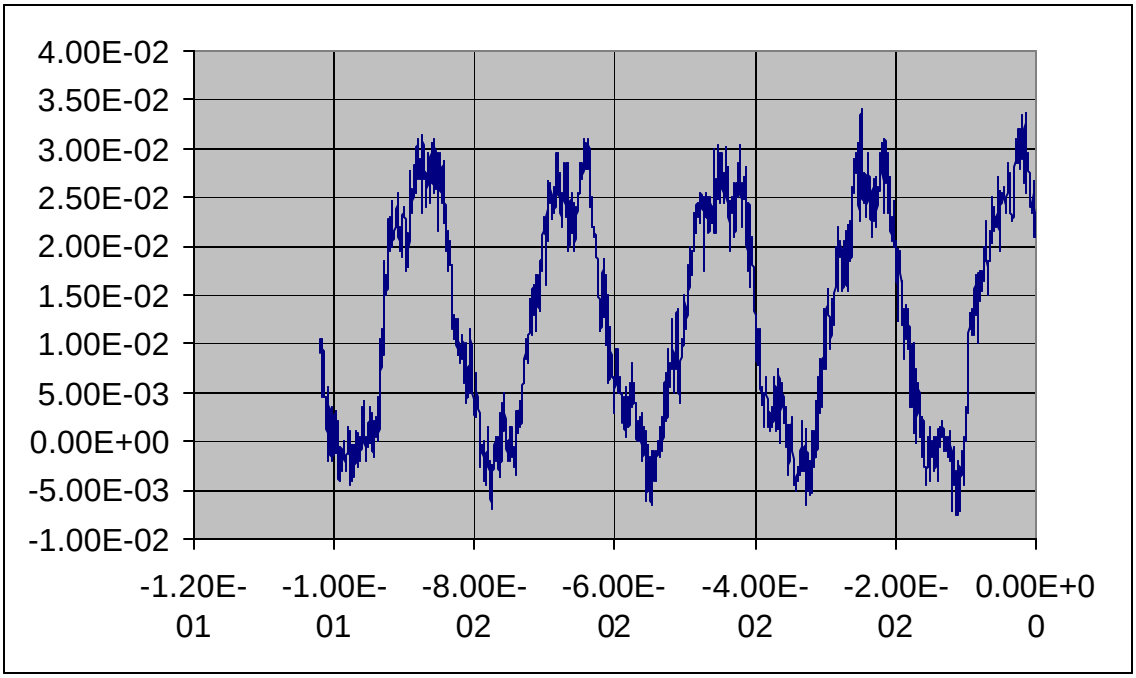


Figure 103 Output waveform of TIA#14 at 50MHz

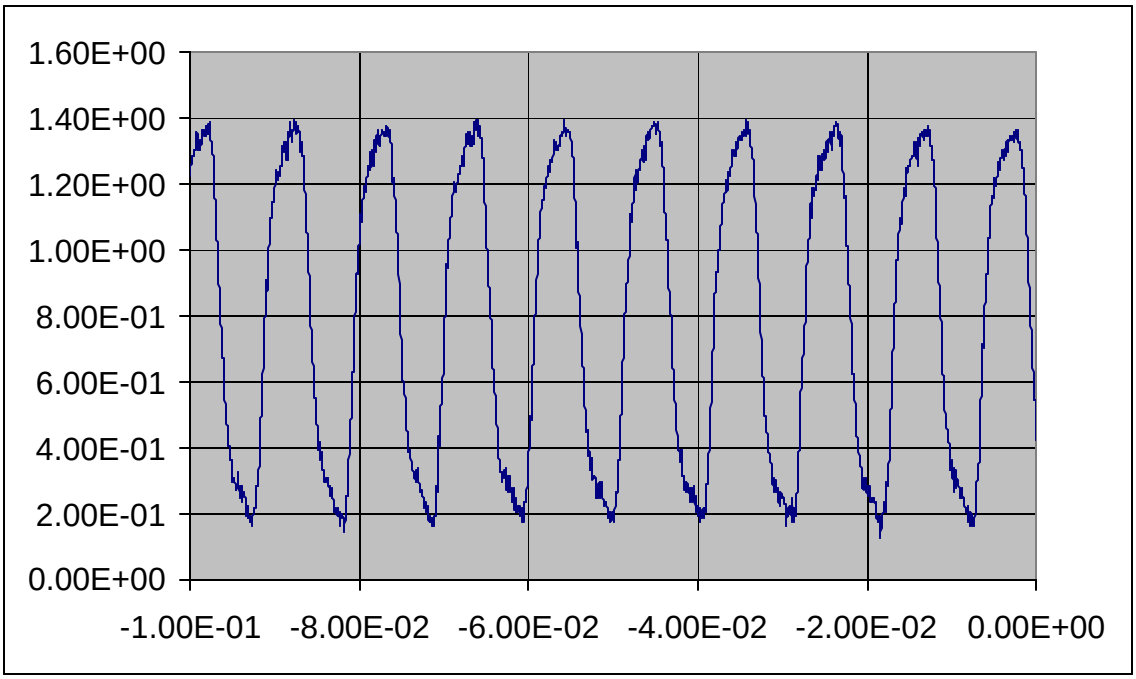


Figure 104 Input waveform of TIA#14 at 100MHz

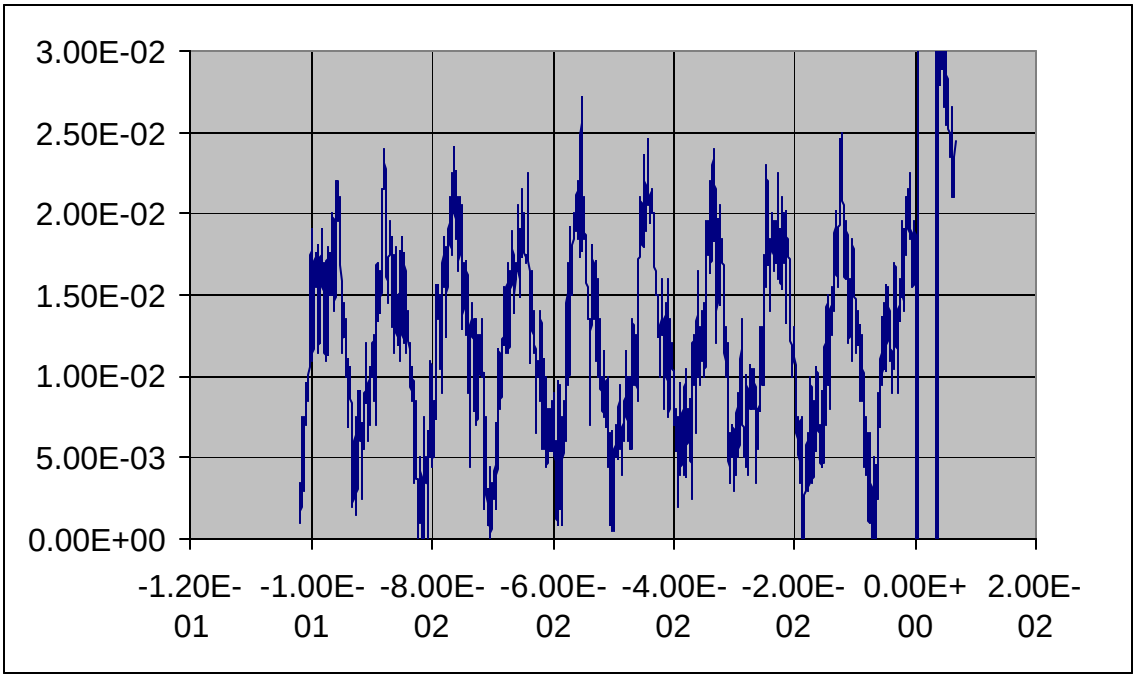


Figure 105 Output waveform a of TIA#14 at 100MHz

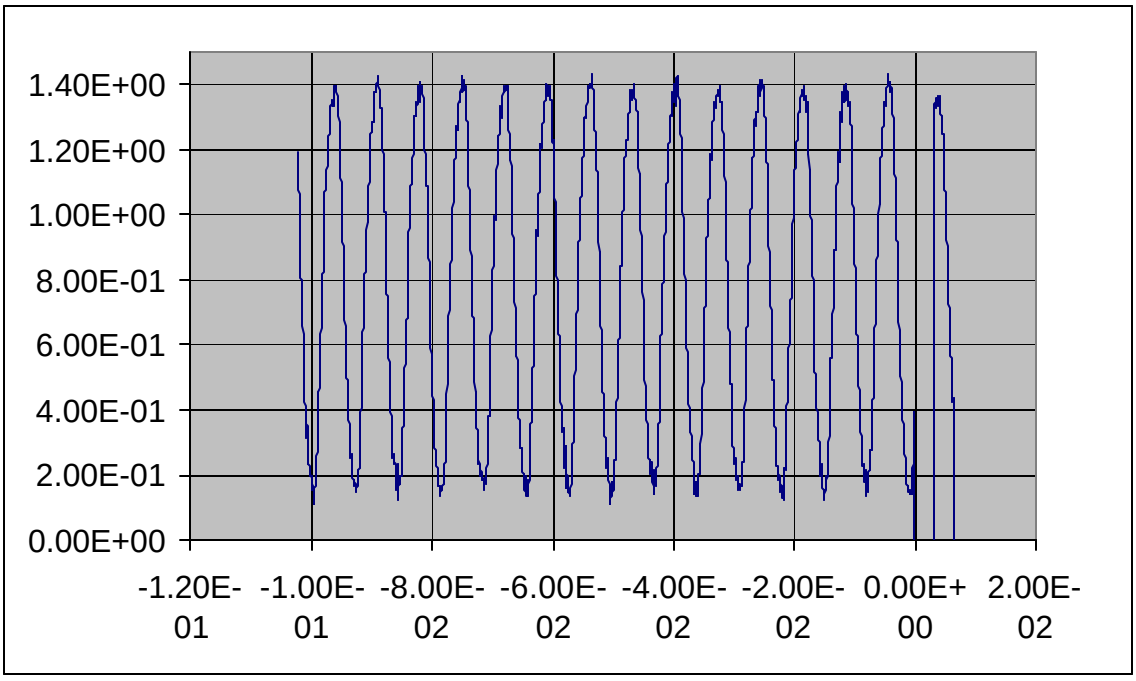


Figure 106 **Input waveform of TIA#14 at 150MHz**

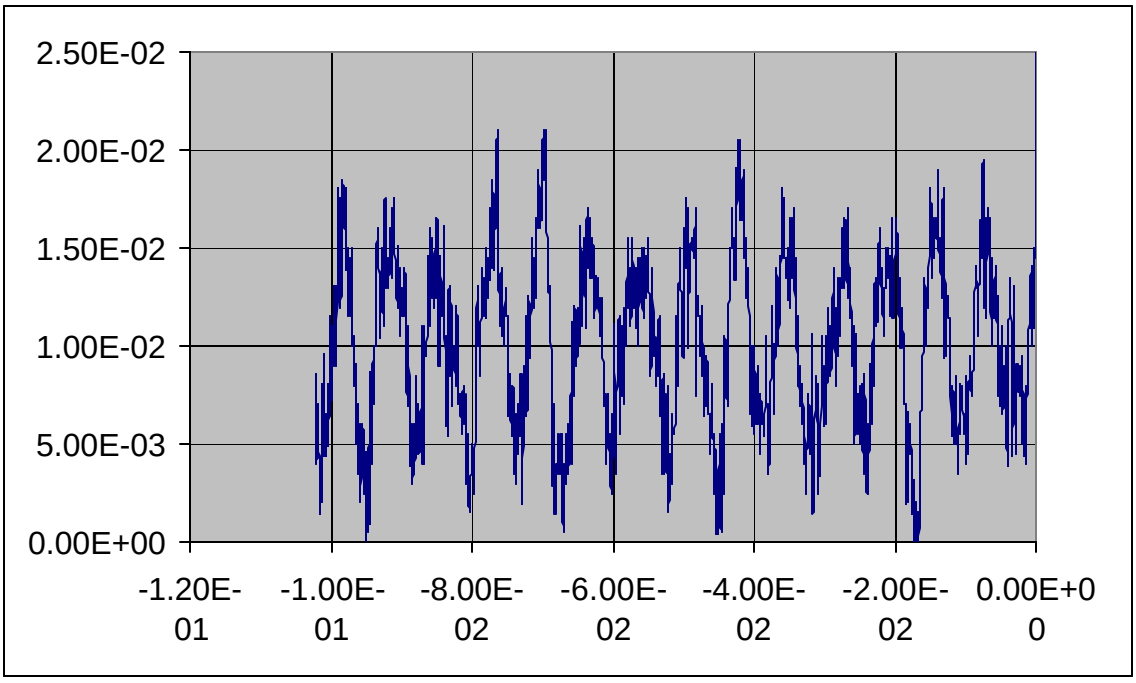


Figure 107 **Output waveform of TIA#14 at 150MHz**

8.0 SUMMARY AND CONCLUSIONS

8.1 SUMMARY

The goal of this research was to understand the Silicon-Germanium (SiGe) process for photodetectors and the design of high-speed analog optical receiver circuits. The availability of the commercial IBM process encouraged us to investigate SiGe photodetectors in this process. An overview of these photodetectors is presented in section 2.2. Our study of the optical and the electronic properties of SiGe alloys is discussed in Chapter 3. The work on SiGe based photodetectors is carried out by first understanding and analyzing the factors affecting the intrinsic absorption phenomenon in photodetectors. The analysis of factors like reflectivity, absorption coefficient, quantum efficiency and responsivity in the IBM NPN SiGe transistor is discussed in sections 3.5-3.8 respectively. SiGe photodetector designs using the NPN SiGe transistor were built based on the understanding developed of the micro-fabrication steps of the IBM SiGe 5HP process. These steps are presented in detail in section 5.1. In order to test the practicality of photodetectors at longer wavelengths range of 1100-1500nm, several SiGe photodetectors were designed and fabricated in this process as presented in section 5.4.

The generated output current from SiGe photodetectors depends on the size and the design of the detector. This current is typically low, in the microamps range for 1mWatt incident optical power. Since the generated current is low, a current to voltage converter is needed with high gain and efficiency. Transimpedance amplifiers are best suited for this purpose, rather than low or high impedance amplifiers due to their low noise, high gain and wide bandwidth as

discussed in section 6.1. Hence, fourteen different circuit topologies of transimpedance amplifier were designed in the IBM SiGe BiCMOS process, the details of which are discussed in section 6.2. These amplifiers were simulated and optimized using the Spectre simulator and the NeoCircuit analog synthesis tool respectively. Transimpedance amplifiers built in other custom SiGe and GaAs processes were chosen and implemented in the IBM SiGe BiCMOS process to compare their speed, gain and bandwidth performance.

The output signal generated from the transimpedance amplifier must have additional amplification before it is sent to digital signal circuitry. The range is typically in millivolts for an input current of microamps from optical detectors. The conversion efficiency for transimpedance amplifiers depends on the design and the technology used. In order to amplify the output signal of the transimpedance amplifiers, several multistage cascaded amplifiers stages, such as differential amplifiers and voltage amplifiers, were built in the IBM SiGe BiCMOS process as shown in section 7.1 and 7.2. These amplifying stages were designed and simulated individually to measure their performance.

The output of the transimpedance amplifier with multistage amplifying stages is fed to a decision circuit. The objective of the decision circuit is to sample and compare the output waveform signal of the amplifying stage to a threshold voltage. If the received output signal is below the threshold, the decision circuit produces zero at its output whereas one is produced if the output signal exceeds the threshold voltage. Thus, two complete receiver circuits composed of a transimpedance amplifier and a multistage cascaded differential amplifier with a decision circuit are designed, simulated and fabricated in the IBM SiGe process. The details and output results of the intermediate stages of a complete receiver circuit are discussed in Chapter 7 of this

thesis. Lastly, a complete layout of an optoelectronic chip built in IBM SiGe process is shown in section 7.3.

8.2 CONCLUSION

Based on the work performed in this thesis we can make the following conclusions.

First, the percentage of Ge in the IBM SiGe process is not high. Therefore intrinsic photo-detection at longer wavelengths is very low. The possibility of intrinsic absorption in the IBM NPN transistor is predicted to be between the wavelengths 800-1150nm. Hence, the responsivity of SiGe based photodetector for a 1mWatt input power in IBM $Si_{0.80}Ge_{0.20}$ process is summarized in Table 9.

Table 9 Responsivity of $Si_{0.80}Ge_{0.20}$ alloys at different wavelength

Responsivity (R) at different wavelength (nm)	Output Result (Amps/mWatt)
800	3.029µ
900	1.450µ
1000	0.684µ
1100	0.088µ
1150	0.043µ

Second, the circuits chosen from other custom Si, SiGe and GaAs processes and implemented in the IBM SiGe process show high speed, gain and high bandwidth. The simulation results of fourteen transimpedance amplifiers show the capability of working at 10GHz with the gain of 54-74dBΩ for an input current of 10µAmps and therefore, Silicon-Germanium devices can offer better speed performance than Si and GaAs devices for high-speed receiver circuits.

Finally, the decision circuits were built using CMOS devices and since the CMOS devices are slower than SiGe bipolar devices in the IBM SiGe BiCMOS process, it is predicted that the receiver circuits will work up to 2Gb/s.

APPENDIX

Table 10 **Basic properties of Si and Ge** [59]

Property	Silicon (Si)	Germanium (Ge)
Crystal Structure	Diamond	Diamond
Lattice constant (A^O)	5.4310	5.6575
Atoms/cm3	5.0×10^{22}	4.42×10^{22}
Atomic weight	28.09	72.60
Indirect energy band gap	1.12	0.66
Electron mobility	1500	3900
Hole mobility	450	1900

Table 11 **Optical properties of Si and Ge** [30-31]

Property	Silicon (Si)	Germanium (Ge)
Transparent regions (μm)	1.1-6.5	1.8-15
Dielectric constant	11.9	16.0
Refractive Index	3.455	4.001
Optical phonon energy	0.063	0.037

BIBLIOGRAPHY

[1] Roger L. Freeman, "Fiber-Optic Systems for telecommunication," A John Wiley & Sons, Inc., Publication, 2002.

[2] R.A. Soref, "Silicon-based optoelectronics," *42nd IEEE Int. ISSCC*, pp. 66 -67, 15-17 Feb. 1995.

[3] H. Hamano, Yamamoto, T., Nishizawa, Y., Oikawa, Y., Kuwatsuka, H., Tahara, A., Suzuki, K., Nishimura, A., "10 Gbit/s optical front end using Si-bipolar preamplifier IC, flip chip APD and slant-end fiber," *Elect. Letter*, vol. 27 (18), pp.1602-1605, 1991.

[4] M.Yamamoto, M. Kubo, and K. Nakao, "Si-OEIC with a built-in-photodiode," *IEEE Transaction Elect. Devices*, vol. 42, pp. 58-63, January1995.

[5] B. Jalali, l. Naval and A.F.J. Levi, "Si-based receivers for optical data links," *IEEE Journal of Lightwave Technology*, Vol. 12, No. 6, pp. 930-935, June 1994.

[6] J.-P. Colinge, "p-i-n photodiodes made in laser-recrystallized silicon-on-insulator," IEEE *Transaction on Electron Devices*, 33(2), pp. 203-205, 1986.

[7] W. Zang, M. Chan, S. K. H. Fung, and P. K. Fo, "Performance of a CMOS compatible lateral bipolar photodetector on SOI substrate," *IEEE Electron Device Letter* 19(11), pp. 435-437, 1998.

[8] A. J. Joseph, Coolbaugh, D. Harame, D., Freeman, G. Subbanna, S. Doherty, M., Dunn, J., Dickey, C., Greenberg, D., Groves, R., Meghelli, M., Rylyakov, A., Sorna, M., Schreiber, O., Herman, D., Tanji, T., "0.13 µm 210 GHz f_T SiGe HBTs-expanding the horizons of SiGe BiCMOS," *IEEE Int. Solid-State Circuit Conf*., pp. 180-2, 2002.

[9] K. Oda, Ohue, E., Suzumura, I., Hayami, R., Kodama, A., Shimamoto, H., Washio, K., "Self aligned selective-epitaxial-growth $Si_{1-x}Ge_xC_y$ HBT technology featuring 170-GHz f_{max}," *IEEE Int. Elect. Dev. Meeting*, pp. 332-335, 2001.

[10] Racanelli, M., Schuegraf, K., Kalburge, A., Kar-Roy, A., Shen, B., Hu, C., Chapek, D., Howard, D., Quon, D., Wang, F., U'ren, G., Lao, L., Tu, H., Zheng, J., Zhang, J., Bell, K., Yin, K., Joshi, P., Akhtar, S., Vo, S., Lee, T., Shi, W., Kempf, P., "Ultra high-speed SiGe npn for advanced BiCMOS technology," *IEEE Int. Elect. Dev. Meeting*, pp. 336-9, 2001.

[11] Bock, J., Schafer, H., Knapp, H., Zoschg, D., Aufinger, K., Wurzer, M., Boguth, S., Stengl, R., Schreiter, R., Meister, T.F., "High-speed SiGe:C bipolar technology," *IEEE Int. Elect. Dev. Meeting*, pp. 344-7, 2001.

[12] Hashimoto, T., Sato, F., Aoyama, T., Suzuki, H., Yoshida, H., Fujii, H., Yamazaki, T., "A 73 GHz f_T 0.18µm RF-SiGe BiCMOS technology considering thermal budget trade-off

and with reduced boron-spike effect on HBT characteristics," *IEEE Int. Elect. Dev. Meeting*, pp. 149-152, 2000.

[13] Heinemann, B., Knoll, D., Barth, R., Bolze, D., Blum, K., Drews, J., Ehwald, K.-E., Fischer, G.G., Kopke, K., Kruger, D., Kurps, R., Rucker, H., Schley, P., Winkler, W., Wulf, H.-E., "Cost-effective high performance high-voltage SiGe:C HBTs with 100GHz f_T and BVCEO x f_T products exceeding 220 V GHz," *IEEE Int. Elect. Dev. Meeting*, pp. 348-352, 2001.

[14] Decoutere, S., Vleugels, F., Kuhn, R., Loo, R., Caymax, M., Jenei, S., Croon, J., Van Huylenbroeck, S., Da Rold, M., Rosseel, E., Chevalier, P., Coppens, P., "A 0.35µm SiGe BiCMOS process featuring a 80GHz f_{max} HBT and integrated high-Q RF passive components," *Proc. IEEE Bipolar/BiCMOS Circ. Tech. Meeting*, pp. 106-9, 2000.

[15] Johnson, F.S., Ai, J., Dunn, S., El Kareh, B., Erdeljac, J., John, S., Benaissa, K., Bellaour, A., Benna, B., Hodgson, L., Hoffleisch, G., Hutter, L., Jaumann, M., Jumpertz, R., Mercer, M., Nair, M., Seitchik, J., Shen, C., Schiekofer, M., Scharnagl, T., "A highly manufacturable 0.25µm RF technology utilizing a unique SiGe integration," *Proc. IEEE Bipolar/BiCMOS Circ. Tech. Meeting*, pp. 56-9, 2001.

[16] Deixler, P., Huizing, H.G.A., Donkers, J.J.T.M., Klootwijk, J.H., Hartskeerl, D., de Boer, W.B., Havens, R.J., van der Toorn, R., Paasschens, J.C.J., Kloosterman, W.J., van Berkum, J.G.M., Terpstra, D., Slotboom, J.W., "Exploration for high performance SiGe-heterojunction bipolar transistor integration," *Proc. IEEE Bipolar/BiCMOS Circ. Tech. Meeting*, pp. 30-3, 2001.

[17] Carroll, M., Ivanov, T., Kuehne, S., Chu, J., King, C., Frei, M., Mastrapasqua, M., Johnson, R., Ng, K., Moinian, S., Martin, S., Huang, C., Hsu, T., Nguyen, D., Singh, R., Fritzinger, L., Esry, T., Moller, W., Kane, B., Abeln, G., Hwang, D., Orphee, D., "COM2 SiGe Modular BiCMOS technology for digital mixed-signal, and RF applications," *IEEE Int. Elect. Dev. Meeting*, pp. 145-8, 2000.

[18] Baudry, H., Martinet, B., Fellous, C., Kermarrec, O., Campidelli, Y., Laurens, M., Marty, M., Mourier, J., Troillard, G., Monroy, A., Dutartre, D., Bensahel, D., Vincent, G., Chantre, A., "High performance 0.25µm SiGe and SiGe:C HBTs using non-selective epitaxy," *Proc. IEEE Bipolar/BiCMOS Circ. Tech. Meeting*, pp. 52-5, 2001.

[19] Schuppen, A., Dietrich, H., Gerlach, S., Hohnemann, H., Arndt, J., Seller, U., Gotzfried, R., Erben, U., Schumacher, H., "SiGe-Technology and components for mobile communication systems," *Proc. IEEE Bipolar/BiCMOS Circ. Tech. Meeting*, pp. 130-3, 1996.

[20] Chantre, A., Marty, M., Regolini, J.L., Mouis, M., de Pontcharra, J., Dutartre, D., Morin, C., Gloria, D., Jouan, S., Pantel, R., Laurens, M., Monroy, A., "A high performance low complexity SiGe HBT for BiCMOS integration," *Proc. IEEE Bipolar/BiCMOS Circ. Tech. Meeting*, pp. 93-6, 1998.

[21] L. Naval, B. Jalali, L. Gomelsky, and J. M. Liu, "Optimization of Si1-xGex/Si waveguide photodetectors operating at λ=1.3μm," *IEEE Journal of Lightwave Technology*, Vol. 14, No. 5, pp. 787-797, May 1996.

[22] F. Y. Huang, Shawn G. Thomas, Michael Chu, Kang L. Wang "Epitaxial SiGeC/Si photodetectors with response in the 1.3μm - 1.55μm range", Electron Devices Meeting, 1996, International, pp. 665 -668, 8-11 Dec. 1996.

[23] F. Y. Huang, Kang L. Wang, "Normal-incidence epitaxial SiGeC photodetector near 1.3μm wavelength grown on Si substrate," F.Y Huang, Kang L. Wang, *App. Phys. Lett*., Vol. 69, No. 16, pp.2330-2, 14 Oct. 1996.

[24] H. Temkin, J. C. bean, T. P. Pearsall, N. A. Olsson, and D. V. Lang, "High photoconductive gain in GexSi1-x/Si strained-layer super-lattice detectors operating at λ=1.3μm," *Appl. Phys. Lett*., Vol. 49, No. 3, pp. 155-157, 21 July 1986.

[25] F. Y. Huang, K. Sakamoto, K. L. Wang, P. Trinh, B. Jalali, "Epitaxial SiGeC waveguide photodetector grown on Si substrate with response in the 1.3μm - 1.55μm wavelength range," *IEEE Photonics Technology Letters*, Vol. 9, No. 2, pp. 229-30, Feb. 1997.

[26] A Splett, A., Zinke, T., Petermann, K., Kasper, E., Kibbel, H., Herzog, H.-J., Presting, H., "Integration of waveguides and photodetectors in SiGe for 1.3μm," *IEEE Photonics Technology Letters*, 6(1), pp. 59-61, 1994.

[27] M. Sugiyama, T. Morikawa, T. Tatsumi, T. Hashimoto, and T. Tashiro, "A selective epitaxial SiGe/Si planar photodetectors for Si-based OEIC's," *Electron Devices Meeting*, pp. 583 -586, 10-13 Dec.1995.

[28] V. P. Kesan, P. G. May, E. Bassous, and S. S. Iyer, "Integrated waveguide-photodetectors using Si/SiGe multiple quantum wells for long wavelength applications," *Electron Devices Meeting*, 1990. Technical Digest, International, pp. 637-409-12 Dec.1990.

[29] Maurice H. Francombe, "Silicon Germanium alloy devices", Chapter 6, James Kolodzey, Handbook of thin film devices, vol. 1: Heterostructures for high performance devices, Published: San Diego : Academic Press, 2000.

[30] C. K. Maiti, G. A. Armstrong, "Application of Silicon-Germanium heterostructure devices," Chapter 9, SiGe Optoelectronic Devices, Published by: Institute of Physics Publishing 2001.

[31] C. K. Maiti, N. B. Chakrabarti, S. K. Ray, "Strained silicon heterostructures materials and devices," Chapter 10 Si/SiGe Optoelectronics, Published by: The institution of Electrical Engineers, 2001.

[32] D. J. Friedman, "SiGe BiCMOS integrated circuits for high-speed serial communication links," *IBM J. Res. & Dev*., vol. 47 No. 2/3, March/May 2003.

[33] H. Kromer, "Theory of wide-gap emitter for transistors," *Proc. IRE*, 45, pp.1535-7, 1957.

[34] S. S. Iyer, G. L. Patton, S. L. Delage, S. Tewari, and J. M. C. Stork, "Silicon-germanium base heterojunction bipolar transistors by molecular beam epitaxy," *IEDM Tech. Dig.*, 874, 1987.

[35] C. A/ King, J. L. Hoyt, J. F. Gibbons, "Bandgap and transport properties of $Si_{1-x}Ge_x$ by analysis of nearly ideal $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors," *IEEE Trans. Elect. Devices*, ED-36, 2093, 1989.

[36] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y.-C. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors: I. Material, physics, and circuits," *IEEE Trans. Devices*, ED-42, 455, 1995.

[37] Bill Schweber, "SiGe Gets Real," *EDN*, pp. 62-75, June 24, 1999(www.ednmag.com).

[38] H. Presting and U. Konig, "State and Applications of Si/SiGe High Frequency and Optoelectronic Devices," *Daimler-Chrysler Research Center Technical Report*, www.iaee.tuwein.ac.at/gme/hofg99/presting.htm.

[39] S. Voinigesu, P. Popescu, "Circuits and technologies for highly integrated optical networking IC's at 10 Gb/s to 40 Gb/s," *IEEE Custom Integrated Circuits Conference*, pp. 14-4-1-8, 2001.

[40] B.S. Meyerson, "Silicon: germanium-based mixed-signal technology for optimization of wired and wireless telecommunications", *IBM J. Res. Develop.*, Vol. 44, No. 3, pp. 391-407, May 2000 .

[41] MOSIS IC Foundry Service (www.mosis.org).

[42] T .K Woodward, Ashok V.Krishnamoorthy, "1Gb/s integrated Optical Detectors and Receivers in commercial CMOS technologies," *IEEE Journal on Selected Topics in Quantum Electronics*, Volume: 5 Issue: 2, pp.146 -156, March-April 1999.

[43] J.L Polleux and C.Rumelhard, "Optical Absorption Coefficient Determination and Physical Modeling of Strained SiGe/Si Photodetectors," *IEEE International Symposium on High Performance Electron Devices for Microwave and Optoelectronic Applications*, pp. 167 -172 CNAM, France, 13-14 Nov. 2000

[44] Jeremy D. Schaub, Daniel M. Kuchta, Dennis L. Rogers, Min Yang, Ken Rim, "Multi Gbit/s, high-sensitivity all silicon 3.3V optical receiver using PIN lateral trench photodetector," *Optical Fiber Communication Conference and Exhibit*, pp. PD19 -P1-3 vol. 4, 2001.

[45] F. Y. Huang, X. Zhu, M. O. Tanner, and K. L. Wang, "Normal-incidence strained-layer superlattice Ge0.5Si/Si photodiodes near 1.3μm," *Appl. Phys. Lett.*, Vol. 67(4), pp. 566-568, 24 July 1995.

[46] Adrian Vonsovici, Lili Vecan, R. Aptez, Alain Koster, and K. Schmidt, "Room temperature photocurrent spectroscopy of SiGe/Si p-i-n photodiodes grown by selective epitaxy," *IEEE Transactions on Electron Devices*, Vol. 45, No.2, pp. 538-542, Feb. 1998.

[47] Z. Pei, C. S. Liang, L. S. Lai, Y. T. Tseng, Y. M. Hsu, P. S. Chen, S. C. Lu, C. M. Liu, M. – J. Tsai and C. W. Liu, "High efficient 850nm and 1310nm multiple quantum well SiGe/Si heterojunction phototransistors with 1.25 plus GHz bandwidth (850 nm)," *Electron Devices Meeting, IEDM '02, Digest. International*, pp. 297 -300, 8-11 Dec. 2002.

[48] A. Torres-J. , E. A. Gutierrez-D., "A Planar Amorphous Si1-x-Gex Separated-Absorption-Multiplication Avalanche Photo Diode," *IEEE Electron Device Letters*, 18, (11), pp. 568-570, November 1997.

[49] Koester, S.J., Klepser, B.-U., Chu, J.O., Kuchta, D., Ismail, K., "1.1 GHz MSM Photodiodes on Relaxed Si1-x-Gex Grown by UHV-CVD," *Device Research Conference Digest*, pp. 60 -61, 22-24 June 1998.

[50] Soda, M.; Morikawa, T.; Shioiri, S.; Tezuka, H.; Sato, F.; Tatsumi, T.; Emura, K.; Tashiro, T., "A 1Gb/s 8 Channel Array OEIC with SiGe Photodetectors," *Proceedings of the 1997 International Solid State Circuits Conference*, pp. 120-121, 1997.

[51] C. K. Maiti, G. A. Armstrong, "Application of Silicon-Germanium heterostructure devices," Chapter 9, SiGe Optoelectronic Devices, Published by *Institute of Physics Publishing* 2001.

[52] A. Bandyopadhyay, M. Jamal Deen, "Photodetectors for optical fiber communication," Chapter 5, Photodetectors and Fiber Optics, edited by H. S. Nalwa.

[53] B. Jagannathan, M. Khater, F. Pagette, J.-S. Rieh, D. Angell, H. Chen, J., Florkey, F. Golan, D.R. Greenberg, R. Groves, S.J. Jeng, J. Johnson, E., Mengistu, K.T. Schonenberg, C.M. Schnabel, P. Smith, A. Stricker, D., Ahlgren, G. Freeman, "Self-aligned SiGe NPN Transistors with 285 GHz f_{MAX}, and 207 GHz f_T in a Manufacturable Technology," *IEEE Electron Device, Letters*, vol. 23 no.5 , pp. 258 -260, May 2002.

[54] John C. Bean, "Silicon – based semiconductors heterostructures column IV band gap engineering," *Proceedings of the IEEE*, Volume: 80 Issue: 4, pp. 571 -587, April 1992.

[55] Properties of advanced semiconductor materials GaN, AlN, InN, BN, SiC, SiGe edited by Michael E. Levinshtein, Sergey L. Rumyantsev, Michael S. Shur, Levinshtein.

[56] R. Braunstein, A. R. Moore, and F. Herman, "Intrinsic optical absorption in germanium-silicon alloy," *Phys. Rev.*, vol. 109(3), pp. 695–710, 1958.

[57] W.C. Dash, R.Newman, "Intrinsic optical absorption in single-crystal germanium and silicon at 77^0K and 300^0K," *Phys. Rev.*, vol. 99(4), pp. 695–710, 1955.

[58] Naval L., Jalali B., Gomelsky L., Liu J.M., "Optimization of Si/sub 1-x/Ge/sub x//Si waveguide photodetectors operating at /spl lambda/=1.3 /spl mu/m," *Lightwave Technology, Journal of*, vol. 14 Issue: 5, pp. 787 –797, May 1996.

[59] Jasprit Singh, "Semiconductor Optoelectronics Physics and Technology," McGraw-Hill Inc. publication, 1995.

[60] David A. Johns, Ken Martin, "Analog Integrated Circuit Design," published by John Wiley and Sons, Inc., 1997.

[61] www.ibm.com (http://www-306.ibm.com/chips/services/foundry/technologies/bicmos.html)

[62] Harame, D.L., Comfort, J.H., Cressler, J.D., Crabbe, E.F., Sun, J.Y.-C., Meyerson, B.S., Tice, T., "Si/SiGe epitaxial-base transistors - II. Materials, physics, and circuits," *IEEE Transactions on Electron Devices*, Volume: 42 Issue: 3, pp. 455 -468, March 1995.

[63] Joseph, A.J., Cressler, J.D., Richey, D.M., Harame, D.L., " Impact of profile scaling on high-injection barrier effects in advanced UHV/CVD SiGe HBTs," *International Meeting on Electron Devices* , pp. 253 –256, 1996.

[64] Joseph, A.J., Cressler, J.D., Richey, D.M., Niu, G., "Optimization of SiGe HBTs for operation at high current densities," *Electron Devices, IEEE Transactions on*, Volume: 46 Issue: 7, pp.1347 -1354, July 1999.

[65] Cressler, J.D., "Re-engineering silicon: Si-Ge heterojunction bipolar technology," *IEEE Spectrum*, Volume: 32 Issue: 3, pp. 49 -55, March 1995.

[66] Cressler, J.D., Comfort, J.H., Crabbe, E.F., Patton, G.L., Stork, J.M.C., Sun, L.Y.-C., Meyerson, B.S., " Profile Design Issues and Optimization of Epitaxial Si and SiGe-Base Bipolar Transistors and Circuits for 77K Applications," *Digest of Technical Papers, Symposium on VLSI Technology*, pp. 69 -70, 1991.

[67] Sun, J.Y.-C., Comfort, J.H., Warnock, J., Cressler, J.D., Patton, G., Stork, J.M.C., Burghartz, J., Harame, D., Crabbe, E., Lu, P.-F., Arienzo, M., Meyerson, B., "Advanced bipolar technology for the 1990s," *VLSI Technology, Systems, and Applications, Proceedings of Technical Papers*, pp. 269 –273, 1991.

[68] Harame, D., Joseph, A., "The emerging role of SiGe BiCMOS technology in wired and wireless communications", Devices, Circuits and Systems, 2002, Proceedings of the Fourth IEEE International Caracas Conference, pp. D052-1 -D052-17, 2002.

[69] David J. T. Heatley, "Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing," second edition, edited by Jose E. Franca, Yannis Tsividas, Chapter 5, 1994.

[70] MAXIM Inc. (http://www.maxim-ic.com/Fiber.cfm)

[71] Adel S. Sedra and Kenneth C. Smith, "Microelectronic Circuits," Fourth edition, published by the Oxford University Press, Chapter 8, Feedback Amplifier pp. 668-669, pp. 688-696, pp. 648, 1998.

[72] Adel S. Sedra and Kenneth C. Smith, "Microelectronic Circuits," Fourth edition, published by the Oxford University Press, Chapter 4, Bipolar Junction Transistors, 1998.

[73] H. Zimmermann, "Integrated Silicon Opto-electronics," published by Springer Series in Photonics, Chapter 11 Design of Integrated Circuits, pp. 239-247, 2000.

[74] Adel S. Sedra and Kenneth C. Smith, "Microelectronic Circuits," Fourth edition, published by the Oxford University Press, Chapter 7, Frequency Response, pp. 36-38, pp. 606-609, 1998.

[75] Sung Min Park, C. Toumazou, C. Papavassiliou, "A high-speed four-channel integrated optical receiver array using SiGe HBT technology," *IEEE International Symposium on Circuits and Systems*, May 28-31, 2000, Geneva, Switzerland, pp. v433-6.

[76] C. B. Yahya , "Design of wideband low noise transimpedance amplifiers for optical communications," *Proc. 43rd IEEE Midwest Symposium On Circuits and Systems*, Lansing MI, Aug 8-11, 2000, pp. 804-7.

[77] Rieh, J.-S., Qasaime, O., Klotzkin, D., Lu, L.-H., Yang, K., Katehi, L.P.B., Bhattacharya, P., Croke, E.T., "Monolithically integrated SiGe/Si PIN-HBT front-end transimpedance photoreceivers," *High Speed Semiconductor Devices and Circuits, Proceedings, IEEE/Cornell Conference on Advanced Concepts*, 4-6 Aug. 1997, pp. 322-31.

[78] Amamiya, Y., Suzuki, Y., Kawanaka, M., Hosoya, K., Yamazaki, Z., Mamada, M., Takahashi, H., Wada, S., Kato, T., Ikenaga, Y., Tanaka, S., Takeuchi, T., Hida, H., "40-Gb/s optical receiver IC chipset – including a transimpedance amplifier, a differential amplifier, and a decision circuit – using GaAs-based HBT technology," *Microwave Symposium Digest, 2002 IEEE MTT-S International*, vol. 1, 2-7 June 2002, pp. 87-90.

[79] Lee, W.S., Dawe, P.J.G., Sitch, J.E., Hadjifotiou, A., "Hybrid optical receivers with integrated electronics," *Optical Detectors and Receivers, IEE Colloquium*, 27 Oct 1993, pp. 6/1-4

[80] Adel S. Sedra and Kenneth C. Smith, "Microelectronic Circuits," Fourth edition, published by the Oxford University Press, Chapter 6, Differential and Multistage Amplifier pp. 487-501, 1998.