TUNING AND CONTROL OF AN ON-CHIP PIEZOELECTRIC RESONATOR

by

Matthew J. Volkar

BS Electrical Engineering, University of Pittsburgh, 2001
BS Computer Science, University of Pittsburgh, 2001

Submitted to the Graduate Faculty of

the School of Engineering in partial fulfillment

of the requirements for the degree of

Master of Science

University of Pittsburgh

2002

UNIVERSITY OF PITTSBURGH

SCHOOL OF ENGINEERING

This thesis was presented

by

Matthew J. Volkar

It was defended on

December 9, 2002

and approved by

William W. Clark, Associate Professor, Mechanical Engineering

Ronald G. Hoelzeman, Associate Professor, Electrical Engineering

Thesis Co-Advisor: James T. Cain, Professor, Electrical Engineering

Thesis Co-Advisor: Marlin H. Mickle, Nickolas A. DeCecco Professor, Electrical Engineering

ABSTRACT

TUNING AND CONTROL OF AN ON-CHIP PIEZOELECTRIC RESONATOR

Matthew J. Volkar, MS

University of Pittsburgh, 2002

From clock signals for digital circuits to frequency references and voltage controlled oscillators for communication systems, oscillators are a fundamental element in many electronic circuits. With the current trend toward smaller and more tightly integrated systems, many applications would benefit greatly from the ability to integrate an oscillator onto a chip.

In this thesis, we describe the design and development of a new oscillator technology which makes use of a piezoelectric resonator for frequency control. By using a specially constructed piezoelectric structure, the proposed design exhibits several significant advantages over other currently available technologies, including the ability to be manufactured on a silicon substrate. This document presents the design of the tuning and control circuitry for such a resonator as well as experimental results with a macro-scale prototype. Details of a truly single-chip oscillator solution, including the design of on-chip capacitors, switches and an amplifier, are also presented. Tuning of the prototype resonator structure is accomplished electrically, and the design has shown frequency tuning of up to 1.5% of the nominal value with a theoretical limit of 40% given the appropriate resonator design.

ACKNOWLEDGEMENTS

A special thanks Dr. J.T. Cain and Dr. Marlin Mickle of the Electrical Engineering department for their support and guidance throughout this project. I would also like to thank Dr. William Clark and Muturi Muriuki of the Mechanical Engineering department for their assistance with the mechanical aspects of the design. Without the efforts of all of these people, this research would never have been possible.

Additional thanks are extended to Dr. William Clark and Dr. Ronald Hoelzeman for their efforts in serving on this committee.

This project was sponsored in part by a contract with the Pittsburgh Digital Greenhouse titled "SOC Frequency Synthesis and Control for Radio Frequency Communication: Development of Novel Hardware and Design Flow".

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Page

1.0 INTRODUCTION AND MOTIVATION

The use of oscillators is fundamental to many areas of analog and digital circuit design. Oscillators are used to provide everything from frequency references for RF communication to clock signals for digital systems, and each type of application has a need for specific features and performance requirements. To meet these needs, oscillator designs have typically been divided into two categories: crystal controlled and non-crystal controlled. Crystal controlled oscillators make use of a crystal structure to govern the oscillation while non-crystal oscillators depend on more traditional electrical components such as inductors and capacitors or logic gates. In this thesis, we will present the design and development of a new oscillator technology that demonstrates a useful combination of the features and benefits of each of these two alternatives. The remainder of this chapter will provide additional information regarding these two oscillator types in order to provide a foundation upon which the new design will be built.

1.1 Crystal Oscillators

Crystal oscillators use the physical properties of a crystal structure to maintain the desired frequency of oscillation. The most common type of crystal oscillator uses a specially cut quartz crystal, and its frequency is determined by the physical dimensions and cut of the crystal. The cut of a quartz crystal refers to the angle at which it has been cut relative to the alignment of the crystal lattice. Since quartz crystals are anisotropic, meaning that their properties vary greatly with direction, this "cut" can have a large impact on the resulting oscillator characteristics such as frequency, quality factor[1], and temperature stability. Many different crystal cuts have been explored for their various properties, but nearly all high stability oscillators utilize the AT and SC cuts. Both of these cuts are temperature compensated, which means that their first order temperature coefficients are zero and only higher order effects contribute to their small frequency/temperature dependence. Crystal cuts can either be singly rotated or doubly rotated as depicted in Figure 1.1. The AT cut is a singly rotated cut with an angle θ of 35.25° with respect to the z-axis while SC-cut crystals are doubly rotated, with a θ of 34.11° and a ϕ of 21.93° [1].

[1] Also known as Q, oscillator quality factor is defined as the nominal frequency divided by the 3dB bandwidth and is used as a measure of the frequency stability of the oscillator

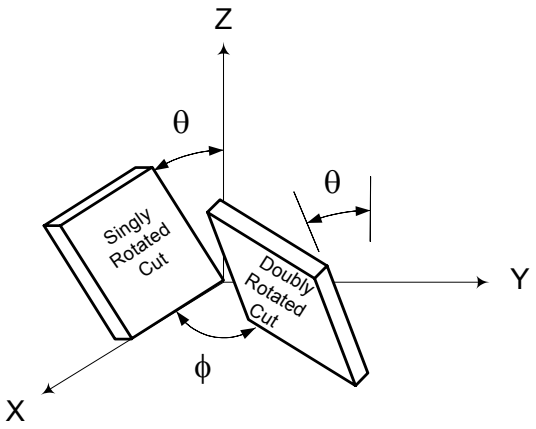

Figure 1.1: Methods of Cutting a Quartz Crystal

The major advantages of a crystal controlled oscillator are the extremely high quality factors that are attainable, on the order of 10^4-10^6 [2], as well as their excellent frequency/temperature stability. Oscillators with a high Q exhibit much better frequency stability, which allows them to be used in applications that require a high precision frequency reference. The frequency/temperature stability of an oscillator defines the ability of the oscillator to maintain its frequency in the face of changes in temperature. Crystal oscillators typically exhibit very small changes in frequency due to temperature variation, and these changes can be compensated for relatively easily. The simplest method of temperature compensation is shown in Figure 1.2 where a variable reactance, typically a varactor, is placed in series with the crystal.

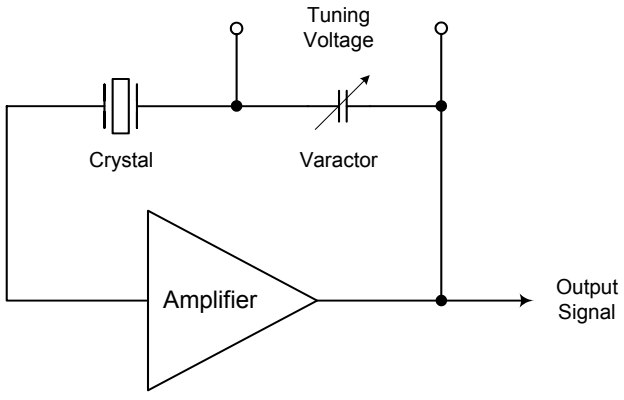

Figure 1.2: Basic Circuit for a Quartz Crystal Oscillator

This reactance can then be used to make small adjustments to the frequency of oscillation in response to temperature change. Other methods of temperature compensation include oven-controlled crystal oscillators where the crystal structure is maintained at a constant temperature by placing it in an oven. By maintaining the temperature of the crystal at a specific value, any variations in frequency due to temperature change are eliminated. Because this type of design is more complicated and requires more power, it is typically only used in cases where extreme stability is required. While the two characteristics of quality factor and temperature stability are important in many applications, there are also limitations to the use of crystal oscillators that make them undesirable for other applications.

Being based on a mechanical structure, there are restrictions on the size of the crystal that can be cut without sacrificing the manageability of the resulting structure. That is, if a high frequency oscillator is desired, the size of the structure becomes so small that it can be easily broken due to the brittleness of the quartz material. To alleviate this problem, crystal manufacturers have begun using an inverted mesa design where the edges of the crystal are thicker than the center. This design is shown in Figure 1.3 and is useful because it allows the center of the blank to be manufactured much thinner while still providing the structural support

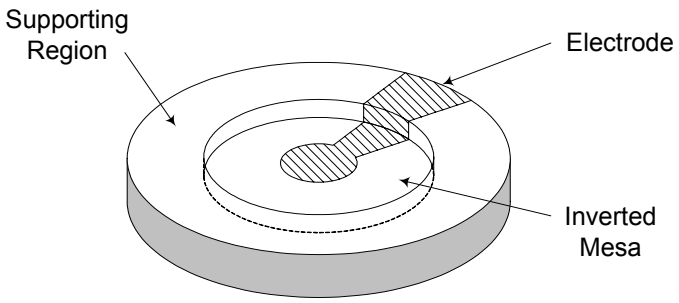

Figure 1.3: The Inverted Mesa Crystal Design

necessary for mounting the crystal. The use of this type of design increases the maximum frequency of a quartz oscillator, but this maximum is still in the range of 300MHz for fundamental mode crystals [3]. Frequencies above this limit are possible using 3rd or 5th overtone crystals, but these oscillators still exhibit many of the problems associated with

fundamental mode crystals, simply at a higher frequency. An overtone crystal is a crystal that has been manufactured so as to obtain oscillation at the odd harmonics of its fundamental frequency. So, while fundamental mode crystals reach a limit at around 300MHz, the maximum frequency of overtone crystals can reach into the gigahertz range. An additional implication of the dependence of frequency on size is that crystals are manufactured only in commonly used frequencies and, therefore, cannot be used in designs that require any arbitrary frequency. Compounding this fact is the limited tunability of a crystal oscillator, which is typically on the order of 50 parts-per-million (ppm) [4]. While this tuning range is sufficient for temperature compensation as was discussed previously, it is insufficient to make up for the lack of available crystal frequencies.

All of these considerations aside, however, the most significant drawback to the use of crystal controlled oscillators is the inability to fabricate these structures as part of an integrated circuit. The reasons for this inability are related to the manufacturing processes involved in building a quartz crystal. First, as discussed above, it is not possible to manufacture a quartz crystal that is comparable in size to that of an integrated circuit. This fact alone would prevent their integration, but even if it were possible to build such small crystals, it would be prohibitively expensive to integrate these crystals onto a chip. Because a quartz crystal must be carefully cut and sized, the crystal structure would have to be manufactured separately from the circuit and mechanically attached at a later time. This requirement of manufacturing the circuit and resonator separately and then combining them presents the biggest obstacle to constructing a single chip crystal oscillator. Due to their manufacturing characteristics, quartz crystals are typically packaged in a small metal can, as shown in Figure 1.4, and require relatively complex oscillator circuits. These circuits often involve a number of discrete components, which can result in a significant amount of space being required on a printed circuit board. Since many oscillators are used in applications where there is a severe space constraint, for example cellular telephones or handheld electronics, the ability to build the entire oscillator circuit on a single chip would be extremely beneficial. Historically, it has been this inability to manufacture fully integrated crystal oscillators that was the main driving force behind the development of alternative non-crystal oscillators.

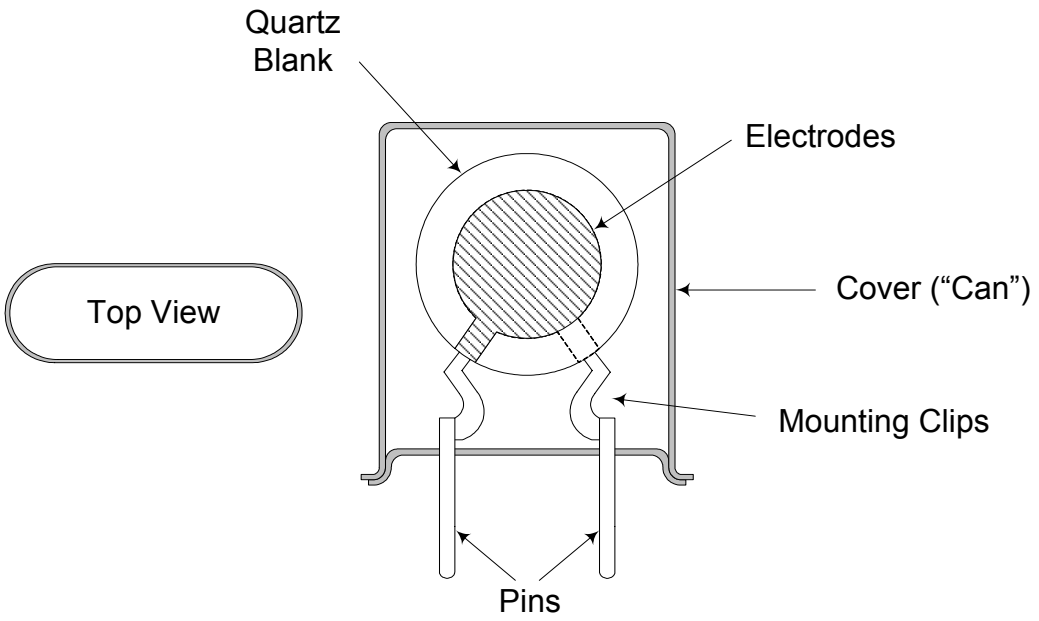

Figure 1.4: Typical Packaging of a Quartz Crystal

1.2 Non-Crystal Oscillators

To overcome some of the limitations of crystal controlled oscillators, most importantly that of the integrability of those designs, several types of non-crystal oscillator have been developed. Some examples of this type of oscillator include LC resonant tanks, ring oscillators, and voltage controlled oscillators. An LC tank circuit, such as shown in Figure 1.5, uses the natural resonance of an inductor-capacitor pair and can thus be designed to oscillate at virtually any desired frequency. The resonant frequency of a tank circuit is given by Equation (1.1).

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{1.1}$$

As can be seen from this expression, the frequency is directly dependent upon the values of the inductor and capacitor components and the tolerances of these components can then become a limitation. For example, on-chip inductors and capacitors have historically had tolerances of 20% [5], which means that it can be extremely difficult to obtain the desired frequency with any degree of accuracy using an LC tank. Assuming only a 5% variation in components, which is

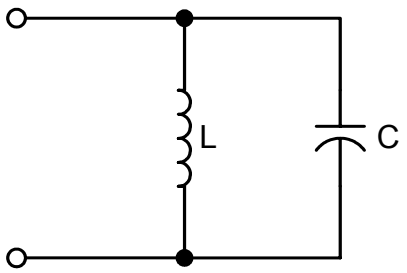

Figure 1.5: An LC Tank Circuit

often considered good for inductors and capacitors, the frequency of this type of oscillator would also vary by as much as 5%. This variability in the design not only means that the frequency will be off by as much as the specified amount, but that the resulting frequency will lack repeatability. For mass produced oscillators, repeatability is an important factor that can greatly impact the usability of the design. It is for this reason that LC oscillators are typically used in applications where an exact frequency is not a specific requirement. Another difficulty associated with the use of on-chip LC oscillators is the relatively large amount of area consumed by these designs. Integrated circuit designers typically try to limit the values of inductor and capacitor components used on-chip due to their large area requirement. Since the frequency of oscillation for an LC tank circuit is inversely proportional to the component values, this area limitation requires that the circuit operate at high frequencies. For this reason, typical on-chip LC oscillators operate in the gigahertz range. The quality factors of LC oscillators in this frequency range are extremely poor, however, with Q's on the order of 10 being common due to the poor quality of on-chip inductors [6]. While the use of an LC oscillator circuit eliminates some of the problems associated with crystal oscillators, their low quality factors and large area requirements, along with the difficulty in producing accurate frequencies, limit their usefulness.

Oscillator designs that make use of digital circuits, such as ring oscillators, can avoid some of the limitations of on-chip LC oscillators by utilizing CMOS transistors in the place of inductor and capacitor components. A ring oscillator circuit, shown in Figure 1.6, can be constructed entirely of CMOS transistors and is easily manufactured on an integrated circuit. As shown in the figure, this type of circuit consists of a series connection of inverters, which results in an oscillation because of the feedback path. Without this feedback, the circuit would simply operate

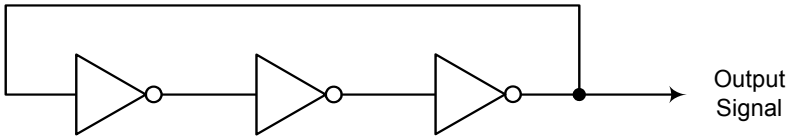

Figure 1.6: A Basic Three Stage Ring Oscillator

as a standard inverter that introduces a propagation delay proportional to the number of stages. By inserting the feedback path, the circuit exhibits oscillatory behavior due to the fact that the input and output are of opposite polarity but are connected together. As we will explain later, an oscillator design must exhibit a phase shift of 0° or 360° in order to function. Since the input and the output of the ring are of opposite polarity, they could be considered 180° out of phase. An additional phase shift is introduced due to the propagation delay through the stages of the ring, and the resulting oscillation will occur at the frequency at which the total delay accounts for an additional 180° of phase shift. The expression for determining this frequency is given by Equation (1.2).

$$f = \frac{1}{2Nt_{pd}} \tag{1.2}$$

Although they are easily integrable, there are also disadvantages to the use of ring oscillator circuits. Due to the fact that a ring oscillator is fundamentally a digital circuit, the output waveform is typically a square wave, which is undesirable for many oscillator applications as it can introduce unwanted signal harmonics. Further, the frequency of oscillation is determined by the parameters N and t_{pd} which correspond to the number of stages and propagation delay of a stage respectively. This formulation imposes limits on the frequencies that are possible using ring oscillator designs. For example, if the design uses minimum size inverters (which have the largest delay), increasing the number of stages is the only available method of slowing the oscillator. For this reason, low frequency oscillators are typically not feasible using a ring oscillator circuit due to the large number of stages and subsequent die area that would be required. Illustrating the relatively large number of stages that would be required, a ring oscillator circuit using 31 minimum size stages operates at a frequency of roughly 40MHz in the AMI ABN 1.5μm process [7]. The frequency of this same circuit would be significantly higher in today's advanced deep sub-micron fabrication technologies due to their significantly lower

propagation delays. In order to increase the frequency of a ring oscillator, we can reduce the number of stages to the minimum of three, but to further increase this frequency we must resort to lowering the propagation delay of each stage. This can be accomplished by increasing the sizes of the transistors used in the inverters but again increases the die area consumed by the design. Furthermore, there is a physical limit to the speed at which an inverter can switch, which will limit the maximum frequency possible in a given fabrication technology. Similar to crystal controlled oscillators, which have a very small tuning range, ring oscillator circuits are typically completely non-tunable, except in the case of specially designed voltage controlled configurations. By using what is known as a current starved ring oscillator, as shown in Figure 1.7, we can vary the oscillation frequency by varying a control voltage. In the design shown, lowering the control voltage limits the current available to the inverters in the ring and therefore increases their propagation delays. This increase in propagation delay results in a decrease in the

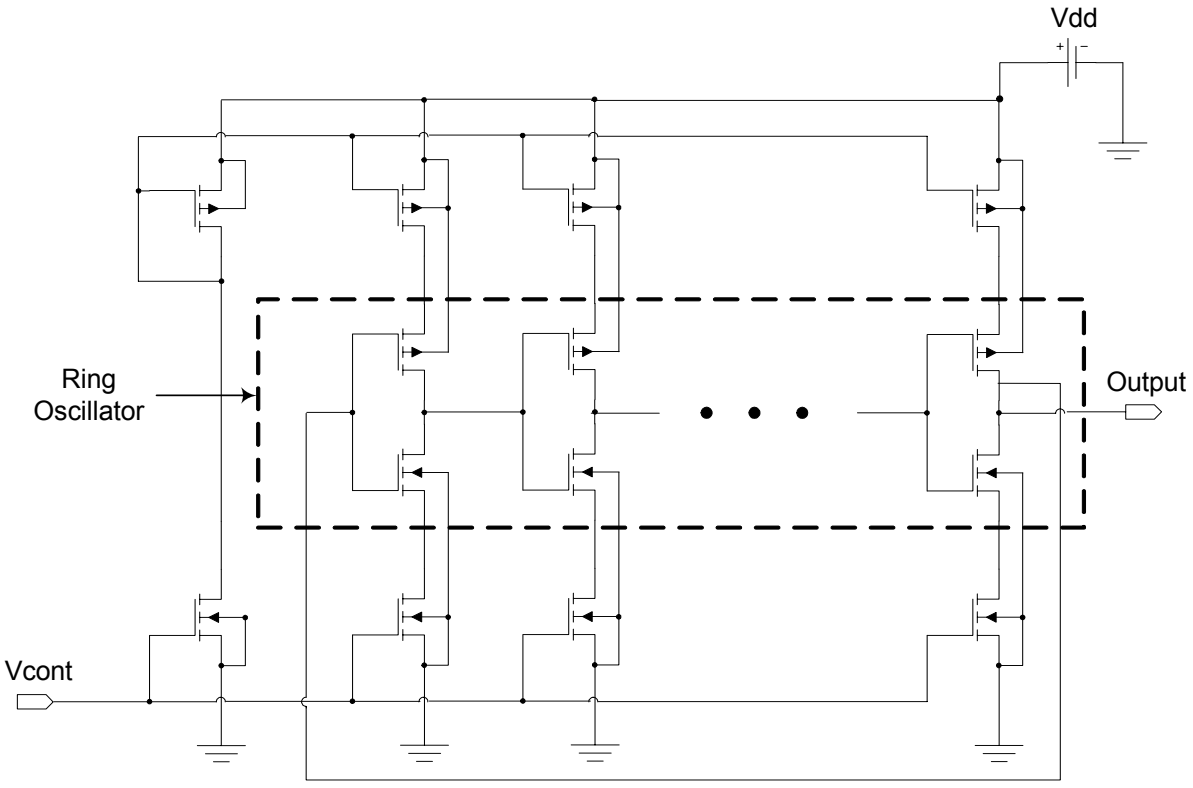

Figure 1.7: Current Starved Voltage Controlled Oscillator

frequency of oscillation for the circuit. These voltage controlled oscillators (VCOs) typically exhibit poor frequency stability, however, and are only used where their wide frequency range is required. As was the case with LC oscillators, we again see that these alternative types of circuits improve on some of the deficiencies of crystal designs, but do not offer a compelling alternative to those circuits.

2.0 PROBLEM STATEMENT

Given the limits of existing oscillator technology, it is desirable to develop a new type of oscillator that does not exhibit the same limitations. The most significant problem associated with current technology is the inability to construct precise, high quality oscillators as part of an integrated circuit. Today's high precision oscillator designs, such as quartz oscillators, cannot be built on-chip, while those that can be easily integrated exhibit relatively poor performance or other significant limitations. In this thesis, a new method of on-chip frequency synthesis is proposed that makes use of a micro-scale piezoelectric resonator. Using this resonator, we design and test an oscillator that exhibits good performance as well as the scalability required to make it a viable on-chip solution.

2.1 Oscillator Requirements

In order for an on-chip piezoelectric oscillator to become a practical alternative to the more traditional techniques, several issues must be considered. These factors include the possible frequency range, the size and complexity of the control circuit, the performance of the oscillator, and the ability to easily and inexpensively manufacture these devices. The requirements of the oscillator proposed in this thesis bridge the gap between those of the alternatives available in typical crystal and non-crystal designs. It is our intention to design, fabricate, and test a new oscillator technology that will exhibit many of the advantages of a crystal controlled oscillator while providing features not typically found in either of the two alternatives. Of considerable importance to this design is the ability to scale the resonator structure, along with necessary tuning and control circuitry, such that it can be constructed on a single integrated circuit. Since the most significant drawback to the use of standard crystal controlled oscillators is the inability to fabricate them on an integrated circuit, this scalability is one of the most important features of our proposed design. As was discussed briefly in Section 1.1, it is not strictly a size limitation that prevents crystals from being utilized on-chip. The ability to manufacture these devices as an integrated part of the design is also lacking. For this reason, it is not only necessary for the new design to be scalable, but it also must be easily constructed on-chip using CMOS compatible processing techniques.

Other features to be incorporated into the proposed design are the ability to switch and tune the frequency of operation dynamically using an electrical input. While the ability to build an oscillator of any arbitrary frequency, as is possible with an LC tank, is desirable, it is often not feasible when using a mechanical resonator. In the case of our oscillator design, the alternative is a single mechanical resonator that can operate at multiple frequencies and/or be tuned throughout a significant range. The increased tuning range of this design, along with its ability to switch nominal frequencies, makes its use possible in applications that do not typically utilize a crystal oscillator. A further concern of this new design is the frequency/temperature stability. As mentioned earlier, specific cuts of quartz, such as AT and SC, exhibit a very small frequency/temperature dependence that makes them ideal for many applications. In order to be competitive with these types of oscillators, the new design must exhibit good temperature stability or the ability to easily compensate for temperature changes. In the new design, temperature compensation can be implemented by making use of the large tuning range of the new oscillator. Table 1 summarizes some of the parameters of crystal and non-crystal oscillators as well as that of the design presented in this thesis. It is important to note that the parameters

Table 1: A Comparison of Parameters for Various Oscillators

	Crystal	LC	Ring	Prototype	Theoretical
Frequency	10^3-10^8 Hz	10^8-10^{10} Hz	10^6-10^8 Hz	10^2-10^4 Hz	10^3-10^8 Hz
Q	10^3-10^6	<20	N/A	>100	10^2-10^5
Tunability	<50ppm	Varies	None	~1.5%	40%
Size (mm)	8x8x2.5	On-chip	On-chip	16x57x0.3	On-chip

presented in this table are typical values and that those of the proposed design are included for both the prototype, which will be discussed later, as well as the theoretical performance limits of the design.

2.2 Scope of This Thesis

The focus of this thesis is the tuning, control, and electrical modeling of a piezoelectric resonator. Issues related to the mechanical properties of the resonator will be discussed only in cases where they directly influence the electrical control of the system or help to further illustrate the design of the oscillator. Modeling of the structure itself will be approached from the perspective of electrical/mechanical analogies with the end result being an equivalent circuit model that will be used in simulating the oscillator design. Design of the remainder of the oscillator circuit will be discussed in terms of off-the-shelf components, which are used in the prototype design, but will also include a description of the steps involved in integrating the design onto a chip. This description will highlight the design and implementation of a single integrated circuit that contains the tuning and control electronics necessary for the oscillator design. A demonstration of the abilities of this new design will be shown via electrical simulation as well as experimentally through the results of testing on a macro-scale prototype. A summary and conclusion will include a discussion of some of the applications for such an oscillator design as well as areas of future consideration.

3.0 BACKGROUND

In order to more fully understand the design presented in this thesis, it is necessary to have a fundamental understanding of several basic concepts that are important to oscillator design. The two most important concepts, which will be relied upon heavily in the remainder of this thesis, are the piezoelectric effect and the concept of mechanical resonance. Without either of these two properties, the design and construction of the proposed oscillator would be impossible. The remainder of this chapter will be devoted to a detailed discussion of these two concepts as well as the fundamentals of basic oscillator design.

3.1 Piezoelectric Effect

The piezoelectric effect describes the interaction between mechanical stress and electrical charge that occurs in certain materials. In these materials, a mechanical stress on the material generates an electrical charge in proportion to the magnitude of the stress. Conversely, an electric charge placed on the material will induce a mechanical stress. The piezoelectric effect, in both of its forms, is illustrated in Figure 3.1. In Figure 3.1(a), an applied stress in the form of a deflection has created an electrical charge on the surface of the material. The opposite effect is shown in Figure 3.1(b) where an applied voltage has caused a deflection in the material. Piezoelectric materials were first discovered in 1880 by Jacques and Pierre Curie who observed that, when a weight was placed on a quartz crystal, charges appeared on the crystal surface [4].

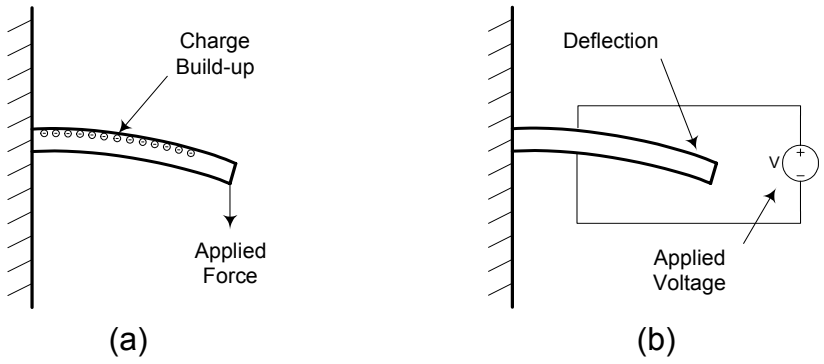

Figure 3.1: Basic Operation of the Piezoelectric Effect

This interaction between electrical and mechanical forces is known as electromechanical coupling and the value which relates charge and stress is known as the coupling factor. The coupling factor is a measure of the ability of a piezoelectric material to convert energy from its mechanical to electrical form and vice versa. A higher coupling factor implies that the material is more efficient in this energy conversion process, that is, that a given stress will generate more electrical charge. This electromechanical coupling is an extremely important part of the proposed oscillator design, where it provides both the interface between the electrical circuit and the mechanical structure, as well as the ability to tune the resonant frequency of the structure.

Since its discovery, the piezoelectric effect and materials which exhibit it have become widely used in many areas, including various types of electromechanical transducers such as pressure and flow sensors. More familiar applications of the piezoelectric effect include "click" lighters and common quartz wristwatches. In a so-called click lighter, pressing the ignition button places pressure on a piezoelectric material which, due to the piezoelectric effect, creates an electric charge. This charge is used to create a small spark that then ignites the lighter's fuel. The advantages of using a piezoelectric material in this application are the elimination of moving parts such as a flint sparker or expendable resources such as a battery. Under normal operation, the piezoelectric material will not wear out or need to be replaced or recharged as would alternative options. In a quartz wristwatch, a crystal controlled oscillator circuit, as was discussed above, is used as the frequency reference for the timekeeping function. In this case, the relatively good accuracy and temperature stability of the quartz design is ideal for the application, which does not require extreme precision. This application is probably the most common, yet little known, application of the piezoelectric effect. In each of these examples, the electromechanical coupling is used to provide a function that would not be available without the piezoelectric material. In the wristwatch oscillator, the electromechanical coupling provided by the quartz crystal is used to interact with an electrical control circuit. By converting the mechanical motion of the crystal into electrical energy, the resonance of the quartz crystal can be used to govern the frequency of oscillation of the circuit. This use of a mechanical structure in an oscillator circuit is discussed further in the following section.

3.2 Mechanical Resonators

Many oscillator designs, including the familiar quartz crystal oscillator discussed above, make use of a resonant mechanical structure. The basis for these designs is the fact that any given mechanical structure will demonstrate natural resonant frequencies that depend on the size, shape, and material properties of the structure. Through careful design of the structure, we can cause it to have a natural resonance at a specific frequency. Mechanical resonators can then be used in conjunction with, or in the place of, electrical components in an oscillator circuit. This is done by utilizing the electromechanical coupling of a piezoelectric material, such as a quartz crystal, to convert mechanical energy into electrical energy. The piezoelectric material can then be used as part of the structure or, in the case of most quartz oscillator designs, as the structure itself. The most common quartz crystal oscillators are mechanical resonators made of a single disc shaped piece of quartz crystal like that shown in Figure 3.2. This crystal structure is manufactured to a specific diameter and thickness based on the desired frequency, and designs of

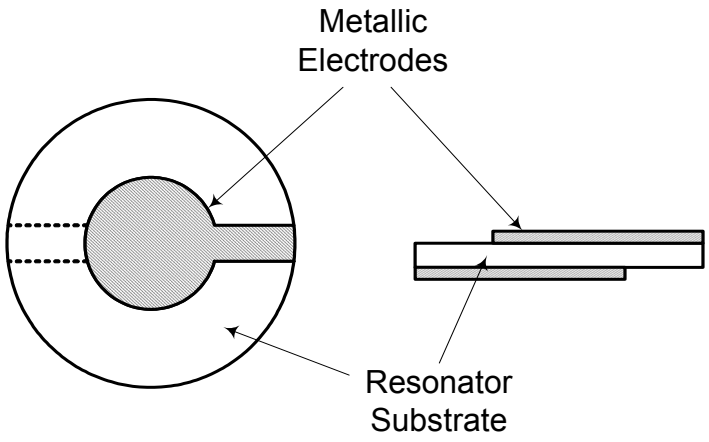

Figure 3.2: Example Quartz Crystal Blank

this type have been demonstrated operating at frequencies into the gigahertz range [4]. In this design, an alternating voltage applied to the electrodes causes the quartz disc to deform an amount that is determined by the natural response of the crystal structure. This deformation is maximum at the resonant frequency and ideally falls off quickly at frequencies above and below

resonance. Quartz crystals have a high quality factor which means that the range of frequencies for which the magnitude of this motion is high is limited to a very narrow band. It is this property of quartz crystals that makes them ideal for use in oscillator applications.

Since every mechanical structure can exhibit multiple types of motion (e.g. bending, twisting, stretching), each structure will also have multiple resonant frequencies. These different types of motion are referred to as modes, with some of the more common modes being illustrated in Figure 3.3. As a result of the effects of structure size and shape on these different modes of oscillation, each mode shown in the figure will oscillate at a different frequency. This allows the designer the freedom to specify the frequency of operation for an oscillator design by choosing

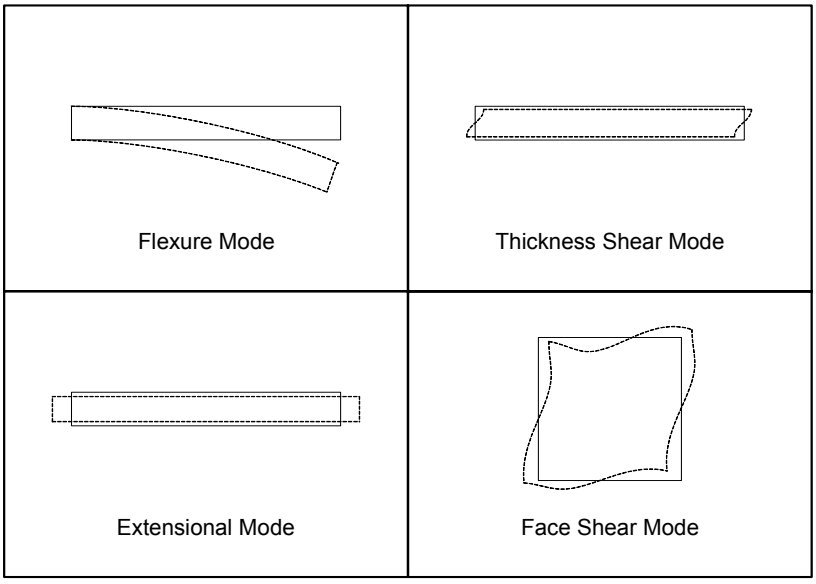

Figure 3.3: Modes of Motion for a Mechanical Structure

the oscillation mode that will be used. Typical high frequency quartz oscillator designs make use of thickness shear mode, while lower frequency designs, such as those in wristwatches, use flexure mode [4]. Adding further flexibility to the design is the fact that each mode also exhibits overtones, which can be used to produce oscillators at higher frequencies than are possible using the fundamental mode. A mechanical overtone is similar to a harmonic in an electrical signal, except that the frequencies of mechanical overtones are not necessarily integer multiples of the

fundamental. Examples of mechanical overtones for two common modes of oscillation are shown in Figure 3.4. Further discussion of these mechanical overtones will be presented in Chapter 4.0 where their use in the proposed design will be discussed.

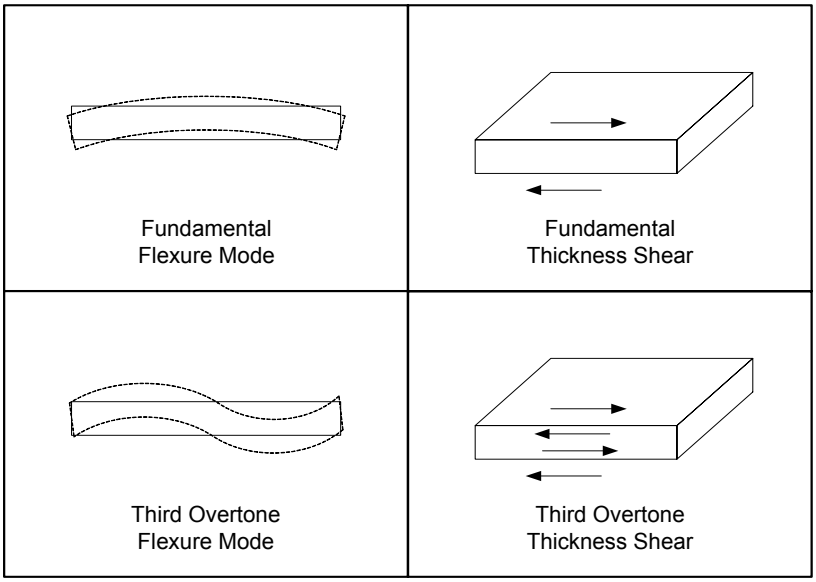

Figure 3.4: Overtones of Some Common Modes

3.3 Oscillator Design

At the most basic level, an oscillator is simply an amplifier with a frequency dependent feedback network, which is used to control the frequency of oscillation. The block diagram for this basic configuration is shown in Figure 3.5. Expanding upon this simple description, two important conditions must be met in order for oscillation to occur within the circuit. First, the gain/loss through the combined amplifier and feedback loop must be greater than unity in order for the system to be self sustaining. If this condition is exactly met (i.e. gain equal to 1), the oscillator will reach a steady state oscillation. If this condition is not met, the response of the system will vary depending on whether the gain is greater or less than one. In the case of a gain less than one, the magnitude of the oscillation will decay toward zero and the oscillator will not

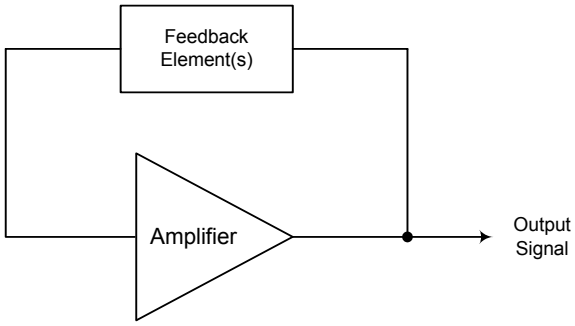

Figure 3.5: Basic Structure of an Oscillator Circuit

function. If the gain is greater than required, the magnitude of oscillation will increase until reaching the saturation voltage of the amplifier. The oscillation for each of these three conditions is shown in Figure 3.6. The first plot shows a loop gain less than one, the second a loop gain of exactly one, and the third a gain greater than one. Note that the signal begins to clip at the maximum amplifier voltage (+/- 2.5V) for a gain greater than one.

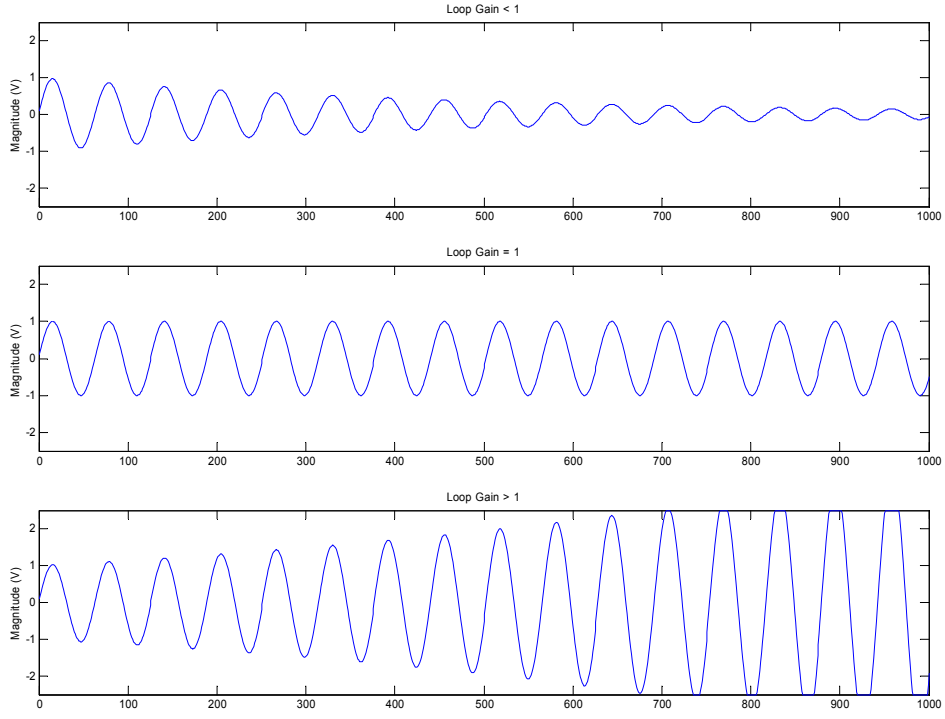

Figure 3.6: Effects of Differing Loop Gain

The second condition that must be met in an oscillator design involves the phase shift around the amplifier/feedback loop, which must be equal to 0° or 360°. This condition is important so that the energy fed back into the system adds to the total response. For example, if the loop phase was 180°, the energy that is fed back from the output to the input would interfere destructively therefore eliminating the oscillation. This effect is demonstrated in Figure 3.7. In this figure, the first plot represents the output signal from the amplifier while the second

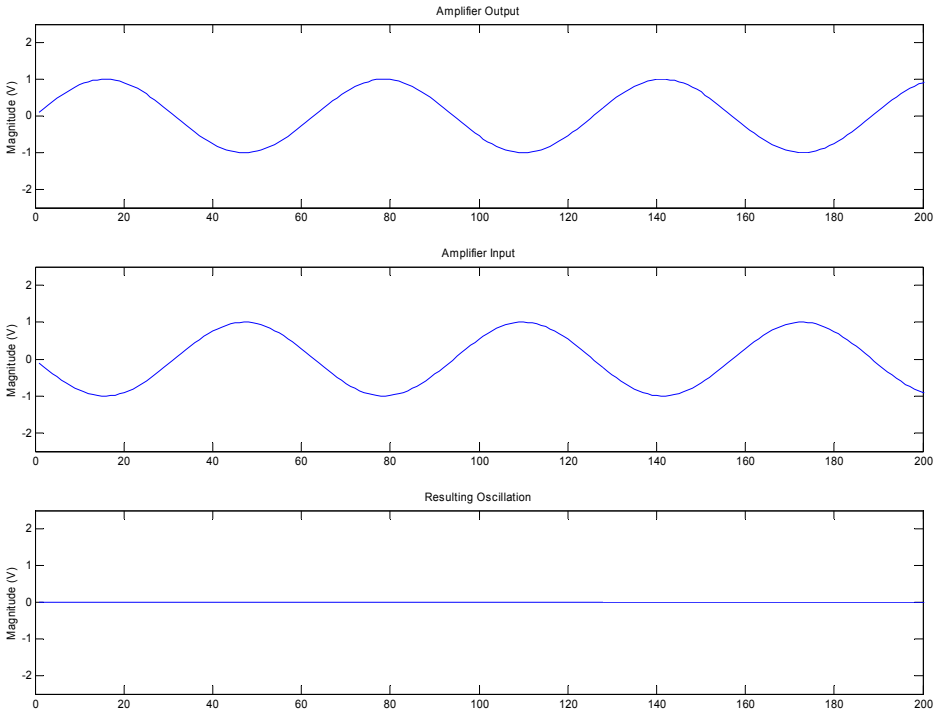

Figure 3.7: Effects of Incorrect Loop Phase

represents the input signal. Note the phase difference of 180° between these two signals. In the figure, the third plot shows how these two signals would combine in the oscillator. Since the loop phase is not equal to 0°, the two signals interfere with each other thus preventing oscillation from occurring within the circuit. Henceforward the two conditions discussed above will be referred to as the amplitude and phase conditions, respectively.

While both crystal and non-crystal oscillators can be thought of as using the same basic structure, these two types differ in the method of providing feedback. In the case of a non-crystal oscillator the natural resonance of an inductor-capacitor pair, also known as an LC tank, is often used as the feedback element. Using this configuration, the LC tank governs the amplitude condition by attenuating those signals that are far from the natural resonant frequency of the inductor-capacitor pair. The LC tank circuit also introduces a phase shift of 90° at its resonant frequency, which must be compensated for in the circuit design. Ring oscillator circuits, on the other hand, control the frequency of oscillation by governing the phase condition. As was discussed earlier, this type of circuit oscillates at the frequency at which the total propagation delay through the ring is equal to half of the period of oscillation. This essentially adds a 180° phase shift that is then compensated for by the 180° introduced by the inverting nature of the circuit. These two shifts add to satisfy the phase condition of the oscillator. In a crystal controlled oscillator, the amplitude condition is governed by the crystal, which takes the place of the tank circuit in an LC oscillator. In this type of oscillator, it is the mechanical properties of the crystal which are used to attenuate signals occurring at frequencies other than the resonant frequency of the structure. As was the case in an LC oscillator, the crystal structure also introduces a 90° phase shift that must be accounted for in the oscillator circuit. We will use a similar property of our piezoelectric resonator to introduce the ability to dynamically switch the frequency of operation.

4.0 SYSTEM SPECIFICATIONS

With a basic understanding of the principles of piezoelectricity, mechanical resonators, and oscillator design in hand, we can now develop the specifications of our new oscillator. These specifications will illustrate the details of the design as well as outline the functionality and performance of the resulting oscillator circuit. The fundamental architecture for this new design is illustrated in Figure 4.1. As discussed above, the most basic oscillator architecture consists of an amplifier with a feedback network. In order to meet the design requirements, the new

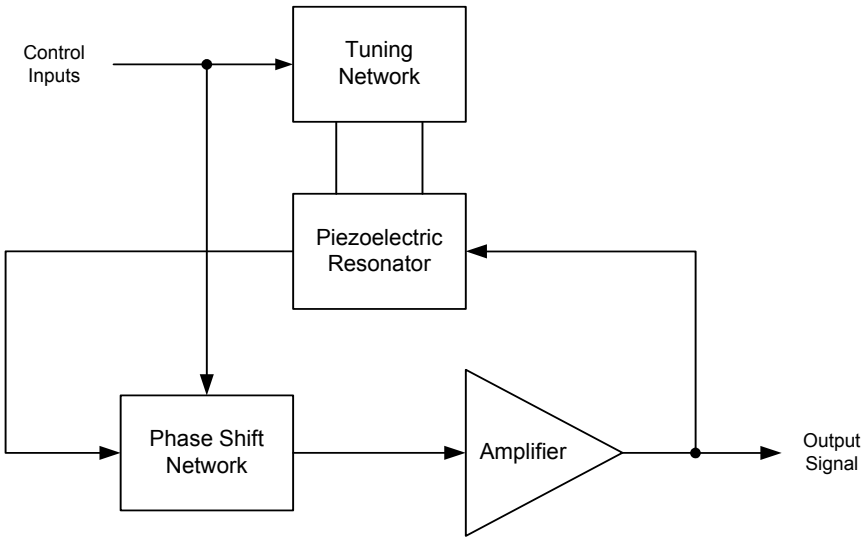

Figure 4.1: Proposed Oscillator Basic Architecture

oscillator maintains these portions, but it also expands upon this basic architecture to provide additional functionality. As can be seen in the above figure, there are two additional components in this new oscillator design: a phase shift network and a tuning network. It is these networks, in conjunction with the piezoelectric resonator, which provide this design with the additional features beyond those of a standard crystal controlled oscillator. This chapter will describe in greater detail the function of each of these components and the features that they enable. Further details regarding the implementation of this new architecture will be discussed in Chapter 6.0 where the prototype design is presented.

4.1 Piezoelectric Resonator

The main component of the feedback network for our new oscillator design is the piezoelectric resonator. This structure is designed to have a mechanical resonance at a specific frequency and consists of a multi-segment piezoelectric structure that is bonded to an elastic substrate. There are a several possible designs for this structure that will satisfy the requirements and the specific design chosen is not of particular importance to the techniques presented in this thesis. The design techniques used for the remainder of the tuning and control circuitry will remain the same regardless of the structure chosen, as long as this structure meets the specifications presented in this section. Two possible structure designs are shown in Figure 4.2, those of a cantilever beam and a stacked cylinder. Further, it is possible to design different size

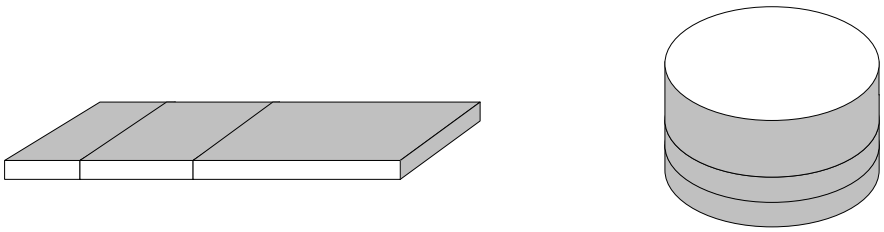

Figure 4.2: Possible Structures for the Piezoelectric Resonator

structures which will exhibit similar properties and can thus be utilized in this oscillator design. While the overall goal of this research is to design and implement a single chip piezoelectric oscillator, a multi-step approach to the issue of structure size has been taken. The prototype structure, presented in Chapter 6.0, is the first step and will be followed by at least one intermediate size structure before realizing the goal of an on-chip solution. The scaling of the design to an on-chip structure is possible due to the properties of the materials being used. Unlike a quartz oscillator, which must be specially cut from a single quartz crystal in order to have piezoelectric properties, the materials used for this structure can be deposited on a substrate in the desired shape and the piezoelectric properties can then be introduced.

The important specification for this structure is that it contains three independent piezoelectric portions that have been designed with specific functions in mind. In contrast to a

standard quartz crystal, which is a two terminal device, the structure used for this oscillator is of a unique design with four terminals. The added terminals are necessary to interface to the additional portions of piezoelectric material, which provide the flexibility of the new design. The first piezoelectric element is used to drive the structure and will be connected to the output of the amplifier. This element converts the electrical energy from the amplifier into mechanical energy, which is stored in the motion of the structure. A second element is used to provide feedback for the system and converts the motion of the beam back into an electrical signal, which can be processed by the amplifier. The final element is not directly utilized by the amplifier circuit, but instead provides the tuning ability for the design. This tuning function will be discussed in more detail in the next section. These three piezoelectric elements will henceforward be known as the actuator, sensor, and passive portions of the structure.

When power is applied to the oscillator control circuit, electrical noise in the amplifier circuitry is sent into the actuator which induces small oscillations of the structure. Oscillations of a frequency other than the resonant frequency are significantly damped and, therefore, filtered out by the mechanical response of the structure. These small oscillations then produce an electrical signal in the sensor piezoelectric element that is fed back into the amplifier circuit. This electrical signal, which has now been amplified, is applied back to the actuator electrode which, in turn, increases the amplitude of oscillation. If the amplitude and phase conditions of the oscillator have been properly met, the system will begin to oscillate at one of the resonant frequencies of the structure. Using only the actuator and sensor portions in this manner, we would have an oscillator design very similar to that of a typical quartz oscillator. It is the addition of the passive portion of the structure, which is used to provide an interface to the frequency tuning network, that makes this design unique. The details of this interaction between the passive piezoelectric element and the tuning network are presented in the following section.

4.2 Tuning Network

The tuning network, which interfaces with the passive piezoelectric element, makes it possible to tune the resonant frequency of the structure. This tuning is achieved by modifying the electromechanical coupling of the passive portion of the piezoelectric material. It has been found that by modifying the electrical circuit connected to a piezoelectric structure, the structure's mechanical properties can be modified [8]. In the case of our tuning network, this

modification is accomplished by capacitive shunting of the piezoelectric material. Figure 4.3 shows an example of how this might be implemented using a simple cantilever beam and a capacitor placed in parallel with the passive piezoelectric element. The mechanical oscillation of

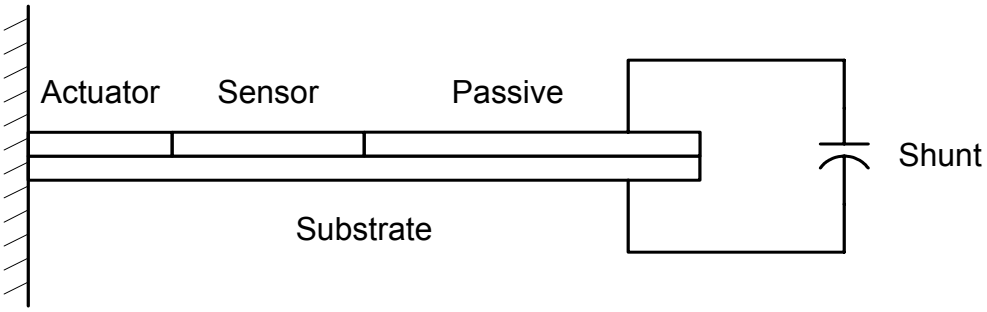

Figure 4.3: Capacitive Shunting of the Passive Segment

a piezoelectric material would normally cause a build-up of electrical charge on the electrodes of the material, but by shorting these two electrodes, this charge is dissipated and the piezoelectric effect is eliminated. Eliminating the piezoelectric effect for the material has the effect of removing the electromechanical coupling, which affects the mechanical properties of the material. This causes a change in the equivalent stiffness of the structure and varies its resonant frequency. In addition to simply shorting the material, we can actively change its properties by using a capacitive shunt as shown in the above figure. When a capacitor is placed across the piezoelectric material, the electromechanical coupling is reduced because the charge generated by the motion is shared between the capacitance of the piezoelectric element and that of the shunt capacitor. By shunting in this manner, the resonant frequency is shifted to some point between that of the open and short-circuit cases.

While the prototype system exhibits a much smaller range, this type of resonator can be constructed such that the frequency change between open and short circuit is theoretically up to 40% of the open circuit frequency. There are many factors that affect this maximum range, including the size of the passive portion and its location on the structure. A structure with a larger passive portion, or with a passive portion located such that its stiffness contribution is a dominant factor in determining the resonant frequency, will exhibit a larger difference between

the open and short circuit frequencies. Since the relationship between shunt capacitance and frequency is non-linear, a small change in capacitance has a large effect on the frequency near the open circuit frequency, but has a much smaller effect near short circuit. To allow frequency adjustments with the desired resolution, a network of shunt capacitors is connected in parallel using electrically controllable switches. By closing a specific subset of these switches, we are creating an electrically variable capacitor, which is then used as the shunt capacitance. For example, the simple configuration of two switched capacitors as shown in Figure 4.4 can provide a total of four distinct frequencies, those of open and short circuit and two intermediate values.

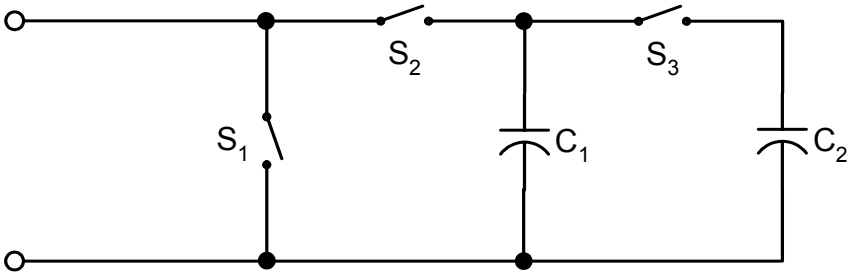

Figure 4.4: Simple Shunt Capacitor Configuration

By leaving all switches open, the circuit operates at the open circuit frequency, while closing switch S_1 will cause the circuit to operate at the short circuit frequency. Alternately, by closing only switch S_2 we can cause the circuit to operate at a third frequency somewhere between open and short circuit and determined by the value of capacitor C_1. If we close both switches S_2 and S_3, we get the fourth and final frequency which is determined by the parallel combination of capacitors C_1 and C_2, C_1+C_2. By increasing the number of capacitors and the complexity of their interconnection, we can produce an oscillator that is tunable to any accuracy required, limited only by the number of capacitors that can be feasibly integrated. Capacitors fabricated in a CMOS process, discussed in Section 6.4, are limited in size due to the die area consumed, which grows linearly with capacitor size.

4.3 Phase Shift Network

Recalling that one of the necessary conditions for an oscillator is the phase condition (i.e. loop phase equal to 0° or 360°), the phase shift network of this oscillator design is intended to meet this requirement. At the most basic level, the phase shift network is used to provide the phase shift required to satisfy the phase condition at the resonant frequency of the structure. For example, if the structure exhibits a resonant frequency of 10kHz with a phase shift of 90°, the phase shift network would need to provide a shift of 270° or -90° at that frequency in order to satisfy the phase condition of the oscillator. The phase shift network can be implemented in a variety of ways using passive components such as resistors and capacitors or using active circuits such as integrators and differentiators. Additionally, the amplifier itself can be used to provide phase shift by operating in the inverting configuration, which introduces a 180° shift. In the above manner, it can be relatively simple to sustain oscillation by introducing the phase required to satisfy the phase condition, however, by allowing the phase shift network to be variable, we introduce additional possibilities.

Recalling that a mechanical structure exhibits multiple resonant frequencies due to the various modes of motion, we can use the variable phase shift network to force the piezoelectric structure to oscillate in a specific mode. This network then makes it possible to quickly change the nominal frequency of oscillation for the system by changing the phase that is introduced and, therefore, the mode of oscillation. For example, consider a mechanical resonator that exhibits resonant frequencies of 5kHz and 15kHz and which introduces a phase shift of 90° at each frequency. By using a phase shift network that is frequency dependent, we can introduce a -90° shift at 5kHz, which will satisfy the phase condition and cause the oscillator to operate at that frequency. If we then modify the network to introduce a -90° shift at 15kHz instead, the system will begin to oscillate at the new frequency. Now, considering that any mechanical structure exhibits multiple resonances, we can use this phase shift network to produce a single oscillator design that can operate at multiple possible frequencies as required for this design.

5.0 SYSTEM MODELING

In order to perform electrical simulations of this new oscillator design using SPICE[2], it is necessary to have accurate electrical models of the components involved. While most components, such as the amplifier, tuning capacitors and phase shift network, are easily characterized, we must develop an equivalent circuit model for the piezoelectric resonator. This process involves examining the electrical/mechanical analogs for the system to determine the topology of the circuit and then extracting the equivalent circuit parameters. The steps used in developing this electrical model for our piezoelectric resonator are presented in this chapter.

5.1 Electrical/Mechanical Analog

In modeling the piezoelectric resonator, it is important to remember that it is a mechanical structure that is forced to oscillate at a specific set of frequencies and can be modeled mechanically as a simple vibrating structure. The basic model for a vibrating mechanical structure is that of the mass, spring and damper shown in Figure 5.1. For this model, there are

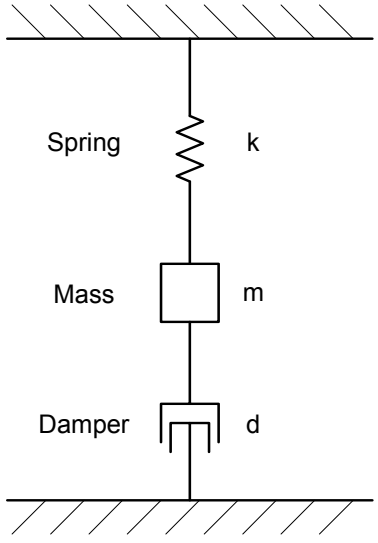

Figure 5.1: Basic Mechanical Model of the Resonator

[2] SPICE, or Simulation Program with Integrated Circuit Emphasis, is a general purpose circuit simulation program originally developed by the University of California at Berkeley

three fundamental parameters that determine the overall response: the mass of the system (*m*), the stiffness of the spring (*k*), and the damping of the damper (*d*)[3]. Writing the equation of motion for this system we obtain Equation (5.1).

$$m\frac{d^2x}{dt^2} = F(t) - d\frac{dx}{dt} - kx(t) \tag{5.1}$$

Assuming that we do not apply any external forces to the system, the *F(t)* term goes to zero, and the system oscillates at its natural resonant frequency as governed by Equation (5.2).

$$\omega = 2\pi f = \sqrt{\frac{k}{m}} \tag{5.2}$$

With no external forces applied to the system, the magnitude of oscillation will decay toward zero at a rate proportional to the damping coefficient, *d*. If we now assume that the structure is made of a piezoelectric material, the expression of Equation (5.1) must be modified. The presence of the piezoelectric effect introduces the conversion of mechanical energy into electrical, and it is proportional to the displacement of the system. The new force introduced into the system due to this effect is given by Equation (5.3), where *C* is the physical capacitance of the piezoelectric material and θ is its electromechanical coupling factor.

$$F(t) = \frac{\theta^2}{C}x(t) \tag{5.3}$$

Introducing this new term into the original equation of motion and setting the applied force equal to zero, we get an overall equation of motion that is given in Equation (5.4).

$$m\frac{d^2x}{dt^2} + d\frac{dx}{dt} + (k + \frac{\theta^2}{C})x(t) = 0 \tag{5.4}$$

By examining this expression, we can see that it is a standard second order differential equation. From a basic understanding of circuit analysis, we recognize that this equation is of the same general form as that of the series RLC electrical circuit shown in Figure 5.2. Using Kirchoff's

[3] The symbol typically used for damping is *c*, but to avoid confusion with capacitance *C*, we use *d* instead

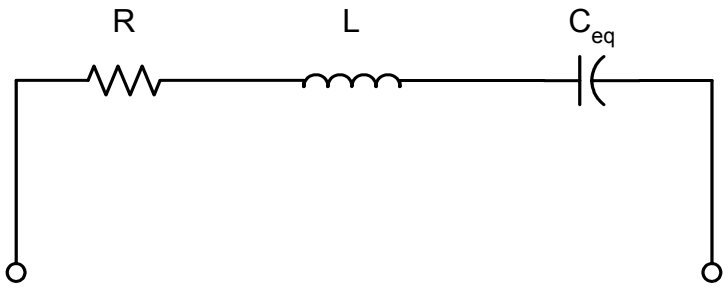

Figure 5.2: Basic Series RLC Circuit

voltage law around the loop gives the differential equation shown in Equation (5.5).

$$L\frac{d^2q}{dt^2} + R\frac{dq}{dt} + \frac{1}{C_{eq}}q(t) = 0 \tag{5.5}$$

By making an analog between charge and displacement, we can perform a mechanical to electrical conversion and thus develop an equivalent electrical circuit for our resonant mechanical structure.

While the above expressions are sufficient to develop an electrical model for a simple mechanical structure, the structure used in this oscillator design is more complicated. There are two important differences between our structure and that described above. First, our structure uses a piezoelectric layer bonded to an elastic substrate, which implies that there are two stiffness terms in the differential equation (or two springs in the mass/spring/damper model). Further, the piezoelectric layer is divided into three portions: actuator, sensor and passive, which requires that there be three coupling forces in the equation as well. However, due to the relatively small size of the actuator piezoelectric and its placement on the first prototype, we can neglect its electromechanically coupled contribution to the overall stiffness. Introducing these additional terms leaves us with the expression given in Equation (5.6) as the coefficient of the *x(t)* term.

$$k_{steel} + k_{piezo} + \frac{\theta_{sens}^{\ 2}}{C_{sens}} + \frac{\theta_{pass}^{\ 2}}{C_{pass}} \tag{5.6}$$

Recognizing the relationships between the coefficients of the mechanical and electrical differential equations discussed above, we can write three expressions relating the mechanical and electrical parameters. In our basic electrical circuit, which was shown in Figure 5.2, the three

electrical parameters are inductance (L), resistance (R) and capacitance (C). From a comparison of the coefficients of the mechanical and electrical equations, we develop the relationships given in Equations (5.7) through (5.9).

$$L = m \tag{5.7}$$

$$R = d \tag{5.8}$$

$$\frac{1}{C} = k_{steel} + k_{piezo} + \frac{\theta_{sens}^{\ 2}}{C_{sens}} + \frac{\theta_{pass}^{\ 2}}{C_{pass}} \tag{5.9}$$

We can break the capacitor value down further by noting that the equivalent capacitance of a series connection of capacitors is of the form shown in Equation (5.10).

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_n} \tag{5.10}$$

It follows that the expression of Equation (5.9) can be interpreted electrically as a series connection of four capacitors having the values given in Table 2. Having developed the relationships between the mechanical and electrical parameters, the following section will discuss the remainder of the electrical equivalent circuit.

Table 2: Capacitor Values for the Electrical Equivalent Circuit

Name	Description	Value
C_{ks}	Stiffness contribution of the steel substrate	$1/k_{steel}$
C_{kp}	Stiffness contribution of the piezoelectric	$1/k_{piezo}$
C_{cs}	Electromechanical coupling of the sensor	$C_{sens}/\theta_{sens}^{\ 2}$
C_{cp}	Electromechanical coupling of the passive	$C_{pass}/\theta_{pass}^{\ 2}$

5.2 Equivalent Circuit

Based on the discussion of the mechanical properties of the system presented in the previous section, the equivalent electrical circuit shown in Figure 5.3 has been developed. This circuit is

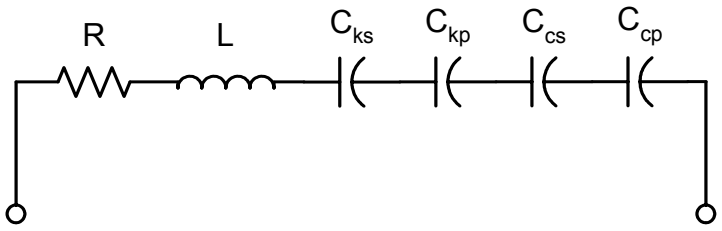

Figure 5.3: Motional Equivalent Circuit for the Resonator

not a completely accurate electrical representation of the structure, however, as it models only the mechanical behavior of the structure, not the electrical behavior. Furthermore, this circuit is only a single port model and it does not include the effects of the shunt capacitance. To correctly model the electrical behavior of the system, the equivalent circuit must also include the capacitance of the actuator electrode. This capacitance arises from the fact that the actuator piezoelectric element acts as a capacitor in the electrical circuit. In order to model this effect in our circuit, we simply add the actuator capacitance in parallel with the above RLC circuit. Since the output of the amplifier is connected to the actuator electrode, this capacitor also then serves as the input port of the equivalent circuit model. To determine the location of the output port, we recall that the input to the amplifier circuit is connected to the sensor electrode and, therefore, we take our output to be the voltage across this capacitance. Finally, to model the effects of tuning the structure, we place the shunt capacitor in parallel with the passive capacitance. The shunt is placed in this location because, as was discussed in the previous section, the shunting of the passive piezoelectric element varies its equivalent stiffness. The modified equivalent circuit model showing the input and output ports and the shunt capacitance is shown in Figure 5.4. This circuit now contains all of the necessary components to accurately model the frequency response of our resonator structure, but it falls short in two important aspects. First, this model represents only a single resonant frequency, while the structure itself exhibits multiple resonances. The second issue is that the response of this circuit does not accurately model the magnitude response of the system at the resonant frequency.

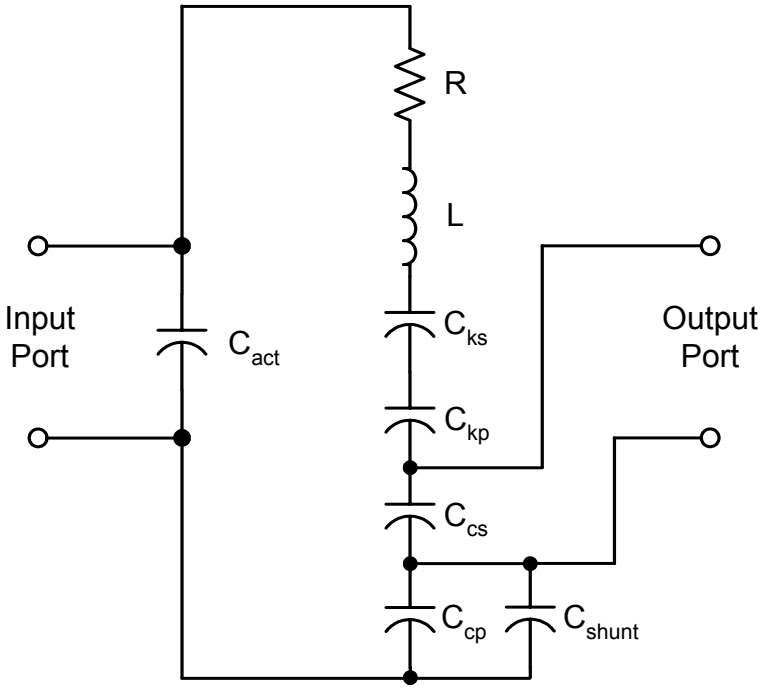

Figure 5.4: Equivalent Circuit with Input/Output Ports and Shunt

To include the multiple resonances of the structure, we can introduce additional RLC branches into the circuit. Each of these branches, known as motional branches, represents a specific mode of motion and, therefore, a specific resonant frequency. To account for the differences in the way the mechanical structure behaves at each of these frequencies, the circuit parameters must now be specified for each mode. For example, the inductor value is no longer specified as the mass of the system, but as the "modal mass", which is calculated for each mode from mechanical simulations of the system. Additional motional branches can be added in parallel with the branch shown above to account for as many mechanical modes as desired to accurately model the structure. For the prototype system, the mechanical simulations include the first five modes of motion and, therefore, the equivalent circuit includes five motional branches. If we were to simply connect these five branches in parallel with the actuator capacitor, the result would be a circuit model that accurately models the resonant frequencies of the system, but not their relative magnitudes. The reason for this is that each mode responds differently to excitation by the actuator piezoelectric, which is a result of the size and location of the actuator on the structure. Further, the location of the sensor with respect to the actuator causes some modes of

motion to introduce an inversion of the signal polarity. To compensate for these two effects, we are again forced to modify our equivalent circuit.

These final modifications include the introduction of several gain elements into the circuit and a decoupling of the motional branches. Since each mode responds differently to the voltage placed upon the actuator, we can no longer simply connect the motional branches in parallel. To correctly model this, we separate the motional branches and introduce a gain element at the input of each of branch as shown in Figure 5.5. This gain element is used to model the coupling of the actuator piezoelectric to the mechanical mode represented by the given motional branch. As

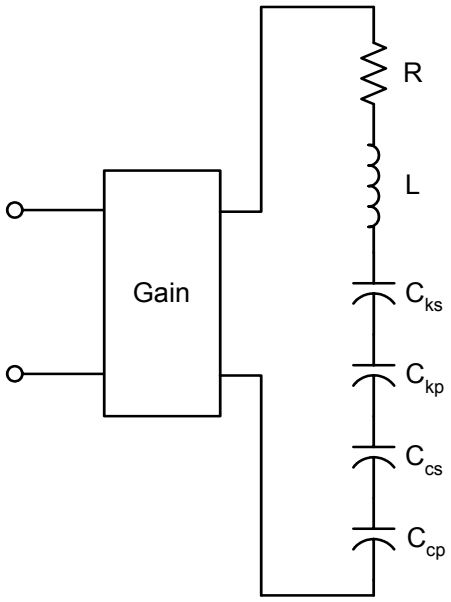

Figure 5.5: Introduction of Gain Block to Motional Branch

stated above, each mode responds differently to excitation by the actuator and it is this element which scales the magnitude of this response. A second element, which can have a gain of +/-1, is placed at the output of each motional branch to model the inversion of the signal for some modes. With the inclusion of this last element, we have an accurate model for the motion of the system. To model multiple modes, these motional branches are connected such that they receive their input from the actuator capacitor and their outputs are summed to make up the output

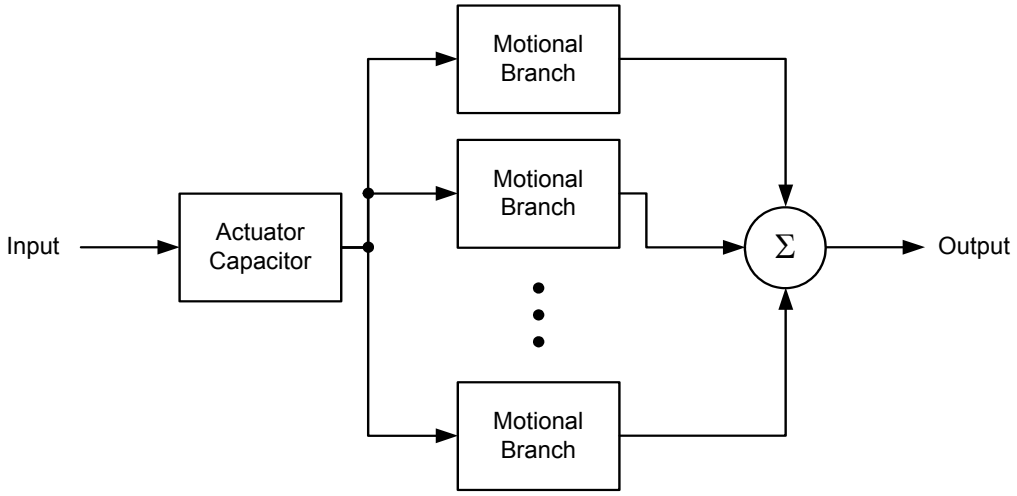

Figure 5.6: Block Diagram Representing the Overall Equivalent Circuit

signal. This configuration is shown in the block diagram in Figure 5.6. By constructing the equivalent circuit as presented in this section, we have a two port model which accurately represents each of the necessary aspects of the design. Results of the use of this model with the parameters of the prototype structure will be presented in Chapter 6.0.

6.0 PROTOTYPE IMPLEMENTATION

To demonstrate the basic operation of this new oscillator design, a prototype structure and corresponding oscillator circuit were designed and constructed. As stated earlier, a multi-step approach to the problem of constructing an on-chip oscillator has been taken. The prototype presented in this chapter represents the first step of this approach. The goal of this first prototype is simply to demonstrate the operation of the oscillator design including the frequency tuning and switching abilities. A second prototype structure of considerably smaller size is currently in development and will begin to demonstrate the scalability of the design. A final step will be to construct the resonator on-chip, along with the necessary oscillator electronics, and to demonstrate the operation of this single chip oscillator design. The mechanical design and construction of the first prototype resonator, as well as the frequency response data from this design are presented in the first part of this chapter. Also included are results of SPICE simulations using the equivalent circuit model developed in the previous chapter. The remainder of the chapter will provide details of the electrical circuit used to control and tune the prototype and will conclude with the results of these efforts.

6.1 Mechanical Design

In general, the mechanical resonator used for this design could be of any one of various different shapes or sizes as was discussed earlier. For the prototype design, a simple cantilever beam structure, which operates in flexure mode, was used. This particular structure was chosen for several reasons. The most important of these is its ease of manufacture at both the macro-scale, used for the prototype, and the micro-scale, which will be used in continuing this research. There are, however, disadvantages to this type of structure that impose limits on the performance of the oscillator. The two most significant disadvantages are that the quality factor of the piezoelectric material is poor for the flexure mode and that the frequencies for this mode are low compared to those of other modes. The piezoelectric material used in this design is Lead Zirconate Titanate which is more popularly known as PZT. This material was chosen due to its widespread availability and use in many sensor and actuator applications. Furthermore, PZT exhibits a relatively high electromechanical coupling, which allows us to demonstrate a larger tuning range than would be possible with other materials. The chosen design uses a cantilever

structure where a layer of PZT is bonded to an elastic substrate. This substrate, which is stainless steel in the prototype, is necessary because of the brittleness of the piezoelectric material. By bonding the piezoelectric to the steel, not only is the structure strengthened, but the steel layer increases the quality factor of the resonator. Ideally, the resonator would be constructed entirely of stainless steel, or some other high Q material, with only enough piezoelectric material as is required to excite and tune the structure.

In order to provide the required sensor, actuator, and passive portions, the piezoelectric layer is partitioned into three pieces by the creation of three separate electrodes. The basic structure of the beam and the layout of these three portions are shown in Figure 6.1. This

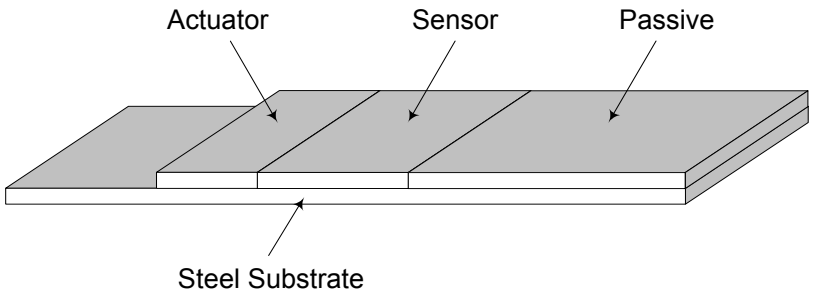

Figure 6.1: Basic Layout of the Cantilever Beam

structure is manufactured using several simple steps. The first step in the process is to cut the substrate materials (i.e. the PZT and stainless steel) to the appropriate size. The two layers are then bonded together and allowed to cure in a clamping mechanism. The next step involves creating the three separate electrodes required on the PZT material. This is accomplished by masking the three portions and etching away the electrode material. The final step involves making connections to each of the electrodes, which is accomplished by bonding a fine wire to the electrodes using conductive epoxy. The prototype structure measures 57mm long, by 16mm wide and 0.3mm thick. The actuator, sensor and passive piezoelectric portions are 10mm, 16mm and 28mm long respectively. Using this design, a tuning range of approximately 1% was expected from the resonator. Larger tuning ranges are possible, but for the first prototype, a

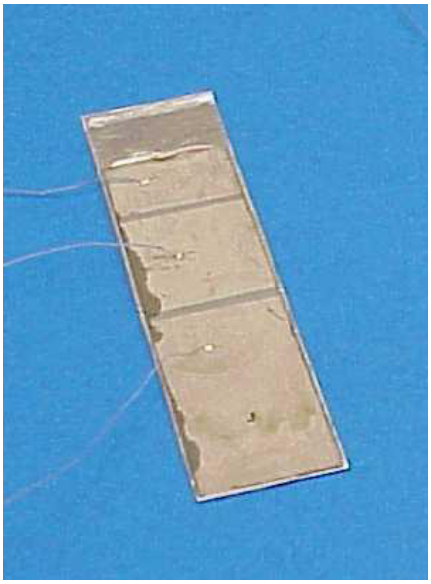

Figure 6.2: Picture of the Prototype Resonator

range of 1% was deemed sufficient to demonstrate the desired effects. For example, if we consider the frequency hopping scheme used for IEEE 802.11, the frequency range required is of approximately the same magnitude. 802.11b, which operates in the ISM band and offers up to 11Mb/s of data transfer, uses 80 communication frequencies with separations of 1MHz. Considering the base frequency of 2.4Ghz, this translates into an overall frequency range of roughly 3.3%. Comparing this result with our expected tuning range of 1%, we see that it is not unreasonable to expect to implement such a frequency hopping scheme using a single oscillator.

Figure 6.2 shows a picture of the completed beam structure. When operating in flexure mode, this beam exhibits a fundamental frequency of ~42Hz with multiple modes/overtones at higher frequencies. The frequency response of this structure from 0-10kHz is shown in Figure 6.3. Note the multiple resonant frequencies that are shown throughout even this small range. Using this frequency response data, simulations were performed with the equivalent circuit model discussed above to determine the validity of the model. The results of this simulation are presented in the following section.

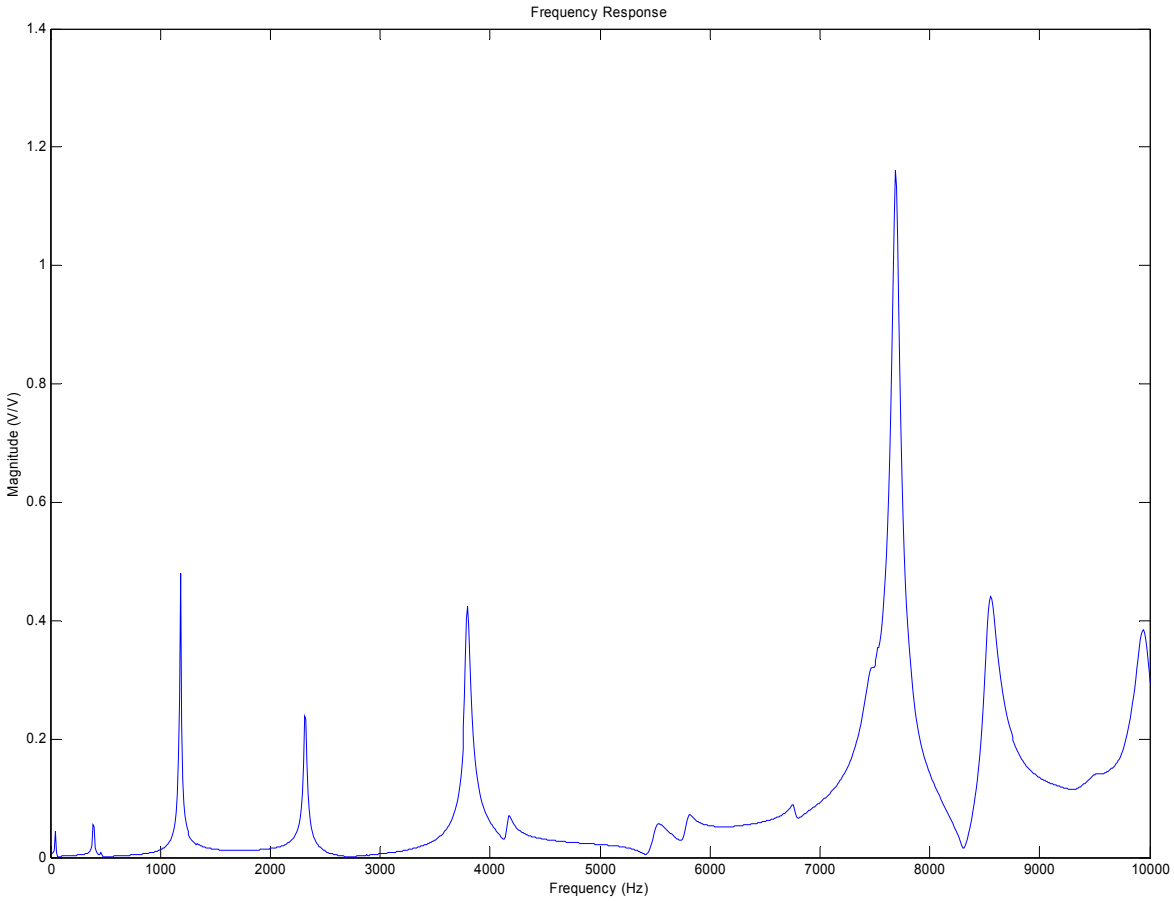

Figure 6.3: Frequency Response of Prototype Resonator to 10kHz

6.2 Equivalent Circuit Simulation

Using the electrical equivalent circuit developed in Section 5.2 and mechanical parameters developed from the mechanical design and simulation, a SPICE frequency sweep was performed to determine the accuracy of the model. The contents of the input file for this simulation are shown in Appendix A. The results of this simulation are shown in Figure 6.4 overlaying the experimental frequency response data. As can be seen from the figure, the results of this simulation very closely match those of the experimental data. Note that the mechanical modeling of the structure included only the first five modes of motion and so the equivalent

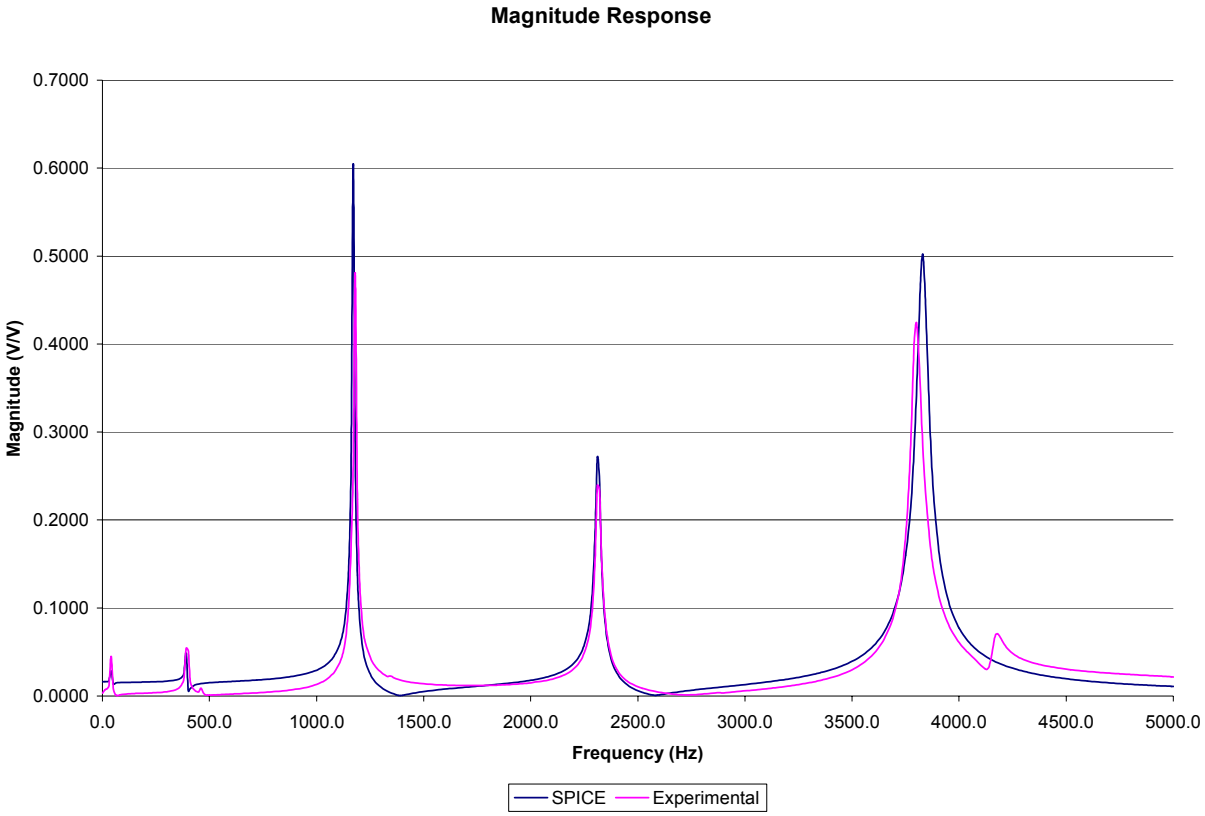

Figure 6.4: SPICE Equivalent Circuit Frequency Response

circuit only models the first five resonances. With the results of this simulation in agreement with the experimental frequency response data, the circuit that will make up the remainder of the oscillator design was developed. The development of this circuit is presented in the remainder of this chapter along with the relevant experimental results.

6.3 Electrical Design

As was discussed previously, the basic electrical circuit required for tuning and control of the mechanical resonator includes an amplifier, phase shift network and tuning capacitors. Due to the size of the prototype structure, it was not necessary to integrate these components onto a single chip and the design could be implemented using off-the-shelf components. The relatively low frequency of oscillation allowed for the use of a standard 741 operational amplifier as the basic amplifier component. The basic gain circuit, which is a simple non-inverting

configuration, is shown in Figure 6.5. The gain of this circuit is adjustable due to the use of potentiometer R_2 and is given in Equation (6.1).

$$A_v = 1 + \frac{R_2}{R_1} \tag{6.1}$$

Using a 100kΩ potentiometer for R_2 and a 2.2kΩ resistor for R_1, the circuit provides a gain in the range of 1-45V/V. This adjustable gain circuit allows the design to be adjusted so that it can satisfy the amplitude condition of the oscillator at the various resonant frequencies.

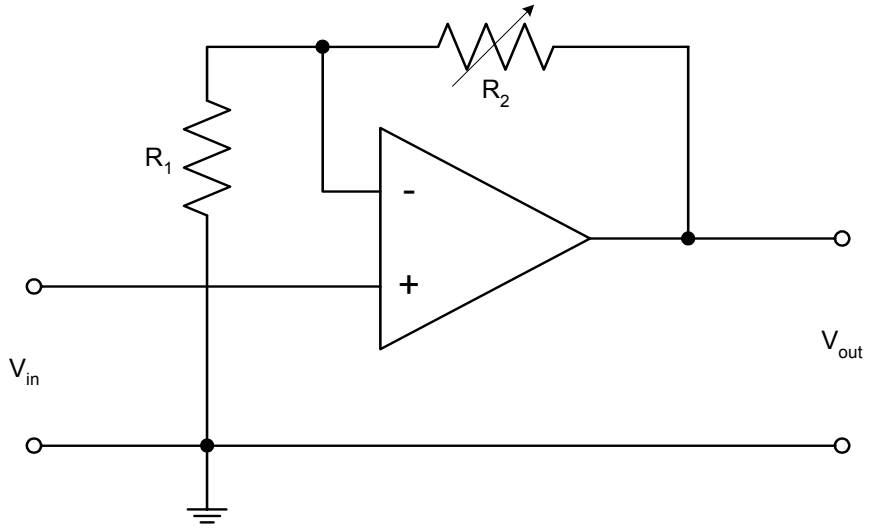

Figure 6.5: Basic Amplifier Circuit

During prototype testing it was also desirable to have an adjustable phase shift network in order to demonstrate the ability to select the mechanical mode of oscillation. This phase shift network is implemented as an all-pass filter, which can be adjusted to produce a variable phase shift by changing the value of a resistor The circuit used for this portion of the design is illustrated in Figure 6.6. By using a potentiometer in the place of resistor R_1, it is possible to vary the phase shift introduced at a specific frequency between 0° and 180°. The phase shift, ϕ,

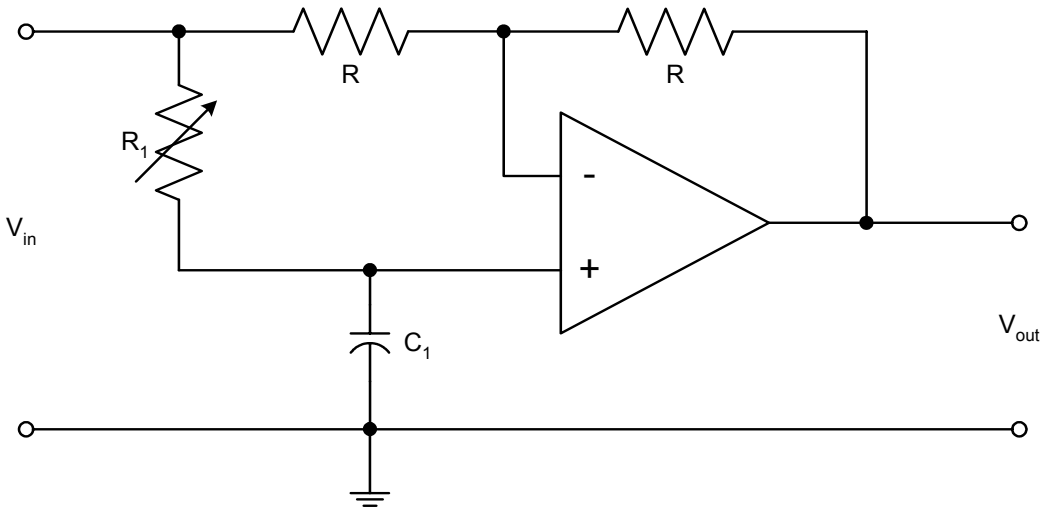

Figure 6.6: Variable Phase Shift Circuit

introduced by this circuit is dependent on R_1, C_1 and the frequency of interest, ω, and is given by Equation (6.2).

$$\phi = \tan^{-1}\left(\frac{\frac{2\omega}{R_1 C_1}}{\omega^2 - \left(\frac{1}{R_1 C_1}\right)^2}\right) \tag{6.2}$$

Rather than using potentiometer R_1 to adjust the phase shift between 0° and 180°, it is instead used to adjust the frequency at which the circuit provides a 90° phase shift. Recalling that, at each of the resonant points, the piezoelectric structure introduces a +/-90° phase shift, this allows the phase shift circuit to compensate for this shift at the various resonant frequencies. In order to simplify this process, the capacitor value C_1 is chosen such that a 5kΩ potentiometer can be used to adjust the frequency of this 90° shift throughout the range of interest. For the prototype design, the frequencies under consideration are between 1kHz and 10kHz and the resulting capacitor value is 47nF. The final portion of the prototype design is that of the tuning network. As discussed in Section 4.2, the tuning network is simply an interconnection of capacitors which allows for a variable shunt capacitance to be placed across the piezoelectric structure. For testing

purposes, a selection of different capacitors, whose values ranged from 1-47pF, was used to demonstrate the tuning ability of the design.

6.4 Experimental Results

Using the prototype oscillator and the circuit described above, experimental results were obtained for the various aspects of the design. Besides the obvious ability to oscillate the structure, the design should also possess the ability to tune the frequency using the tuning network and switch nominal frequencies using the phase shift network. The results of these experiments are presented in this section along with preliminary frequency/temperature characteristics of the oscillator.

6.4.1 Capacitive Tuning

Using the third bending mode of the resonator structure, which has a nominal frequency of 1172.4Hz, the results of capacitive tuning are presented in this section. To determine the maximum range available for this type of tuning, the frequency of oscillation is measured under the two boundary conditions. These conditions are that of having the electromechanical coupling of the passive portion either present or absent. As was discussed in Section 4.2, shorting the passive piezoelectric material will eliminate the electromechanical coupling that is normally present. For this reason, the boundary conditions will be noted as open circuit and short circuit, implying the presence or absence of this coupling factor. Any capacitive tuning that is performed will result in a frequency that is somewhere between these two values. For the mode under consideration, the open circuit frequency was measured at 1172.4Hz and the short circuit frequency was 1155.4Hz. This represents a tuning range of roughly 1.5%, which is slightly larger than the 1% that was designed for with this structure. It is also significantly larger than any tuning that can be accomplished using a quartz crystal. Again, it is important to remember that, using a different structure, we can theoretically demonstrate a tuning range of up to 40%.

Using a collection of shunt capacitors, a frequency versus capacitance curve was developed for the prototype and is shown in Figure 6.7. The frequency of the oscillator was measured at each value of shunt capacitance using a Goldstar FC-2130U 1.3GHz Universal Frequency Counter. The plot shown in the figure also includes the theoretical frequency versus

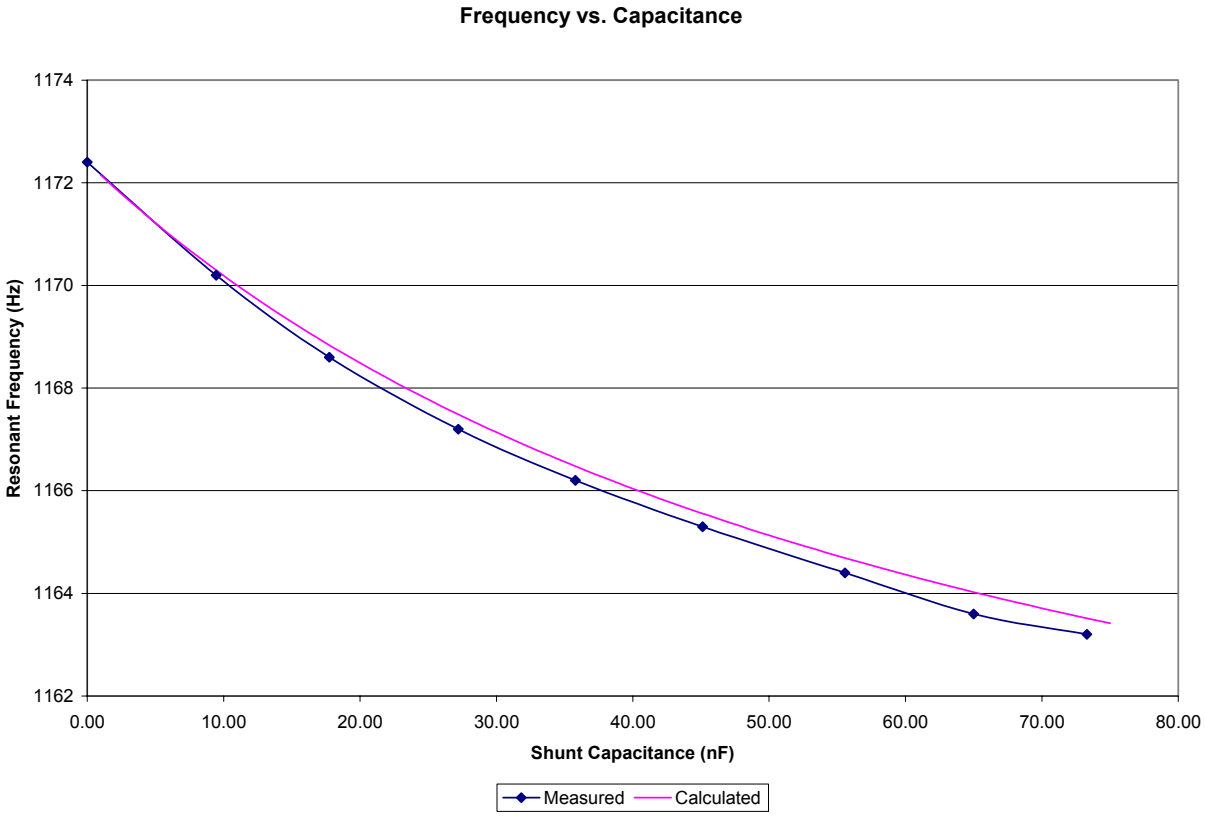

Figure 6.7: Frequency vs. Tuning Capacitance for Third Mode

capacitance curve, which was developed from the mechanical parameters of the system. Again we see that the theoretical values match very closely with the experimental results. The maximum difference between these two curves is less than 0.5Hz or an error of about 0.004%. This difference is likely due to error introduced in calculating the electromechanical coupling of the passive piezoelectric element. If this error is found to be consistent across multiple structures, it could likely be reduced or eliminated by making adjustments to the parameters of the electromechanical coupling calculation based on experimental results with these structures.

6.4.2 Modal Switching

The second type of frequency adjustment that is possible with this oscillator design is the ability to switch between mechanical modes through the use of the variable phase shift network. Tests were conducted to determine which of the resonant points of the structure could be excited using

this technique. As shown in the frequency response plot of Figure 6.3, the prototype system exhibits a total of nine resonant points up to a frequency of 10kHz. For the circuit configuration and component values discussed in Section 6.3, only five of the nine resonant frequencies of the structure could be excited. These frequencies are listed in Table 3 along with their quality factors and magnitude responses. There are several reasons why it might not be possible to

Table 3: Usable Resonant Frequencies to 10kHz

Frequency (Hz)	Q	Magnitude (V/V)
1172	120.8	0.611
2317	102.1	0.283
3802	72.2	0.502
7694	61.2	1.093
9942	47.9	0.226

excite each of the modes of the structure. First and most obvious is the inability of the amplifier or phase shift network to satisfy the amplitude and phase conditions. Inability to satisfy the amplitude condition could be due to a low gain amplifier or an extremely poor response by the resonator at that frequency. Secondly, since the phase introduced by the phase shift network is nonlinear with the resistance value, satisfying the phase condition can be difficult at frequencies either significantly above or significantly below the "sweet spot" for the phase shift network. This "sweet spot" depends on the value of capacitor that is chosen and the range of the potentiometer that is used. This is due to the relationship between the frequency at which the 90° shift occurs and the value of the potentiometer and is demonstrated in Figure 6.8. As can be seen from the figure, using the current circuit configuration, the phase shift network requires extremely large resistor values at low frequencies. Further, the resistor values required to differentiate modes at high frequency become very close to one another limiting the ability to select a mode. The sweet-spot for this example would be in the range of 1-5kHz.

Based on the experimental results, we have determined that the modes at the extremely low frequencies of ~40Hz and ~400Hz as well as the mode at ~5500Hz could not be excited due

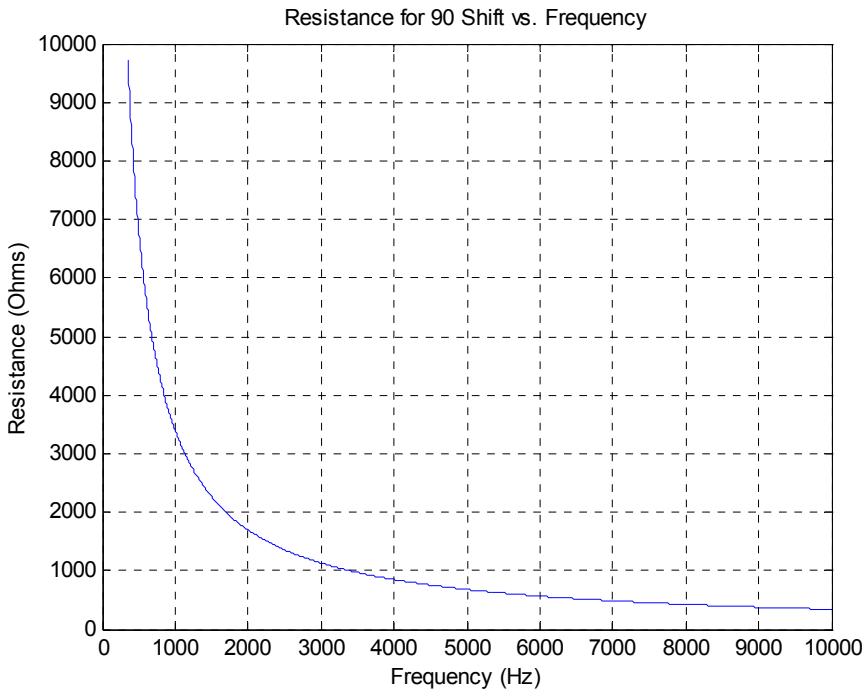

Figure 6.8: Resistance vs. Frequency for the Phase Shift Network

to the poor response of the structure at these frequencies. This poor response should be obvious from the frequency response plot where these peaks are of significantly smaller magnitude than the others. It was not possible to excite the resonance at ~8500Hz due to its proximity to the much stronger mode at ~7700Hz and the configuration of the circuit. As discussed above and in Section 6.3, the phase introduced by the shift network varies nonlinearly with resistance value and there exists a so-called sweet spot for the circuit. In the configuration discussed, using a 47nF capacitor, this sweet spot is roughly between the frequencies of 1kHz and 5kHz. To illustrate this difficulty, consider that the resistance value required to introduce 90° of phase at 7700Hz is roughly 340Ω while the same shift at 8600Hz requires a 300Ω resistor. Looking at it from another perspective, we see that using a 300Ω resistor, the difference in phase introduced at 8600Hz versus at 7700Hz is only 6°. Since the response of the structure at 7700Hz is significantly better and the phase difference at this frequency is very small, the structure oscillates at this frequency. The phase shift network could, of course, be modified so as to enable the excitation of both of these modes by thus increasing the phase difference between these two frequencies, but this could only be done by modifying the capacitor value. Changing

this capacitor value in order to enable greater control of the phase shift at high frequencies would result in the requirement of very large resistances at low frequencies and may prevent us from using the mode at ~1170Hz.

6.4.3 Temperature Stability

The final experiment that was performed was a test of the frequency/temperature stability of this oscillator design. Note that the results presented here are only preliminary as no design effort was spent attempting to design the structure for enhanced temperature stability. These tests were conducted by attaching a thermal probe to the resonator structure and placing it in an oven. The oscillator circuit was then connected to the structure and oscillation was induced, once again, using the third mode. Temperature and frequency measurements were taken at two minute intervals during the heating of the structure from an ambient temperature of 73.4°F up to a maximum of 120°F. Similar measurements were taken at one minute intervals during the cooling of the structure. The results from this experiment are presented in Figure 6.9. From the

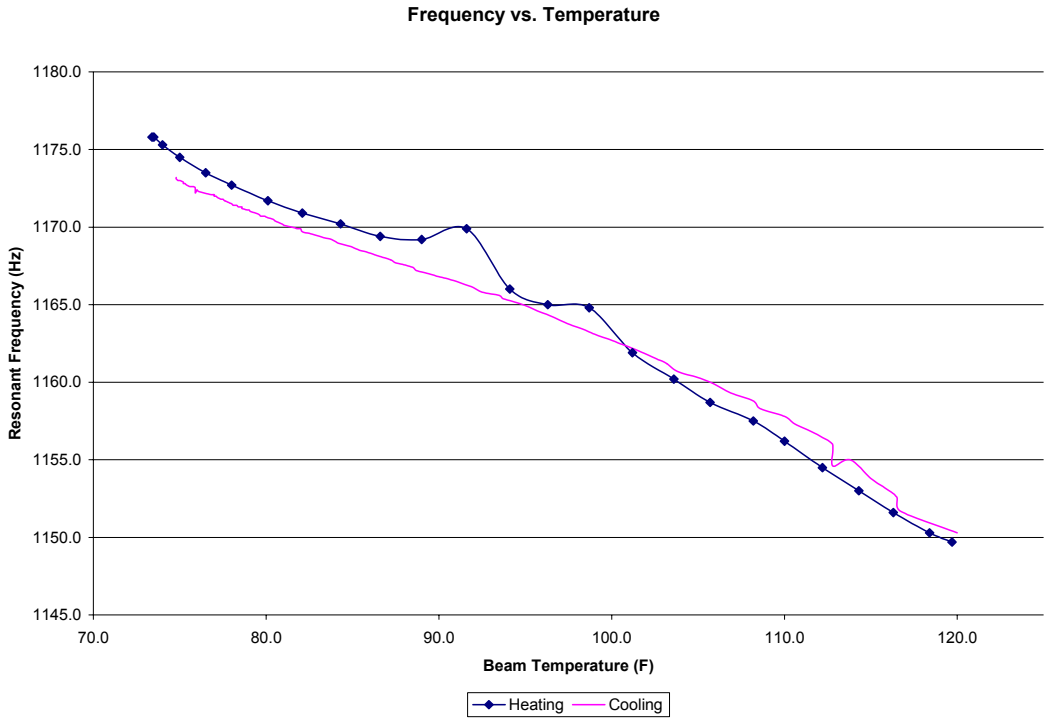

Figure 6.9: Frequency vs. Temperature for Third Mode

figure it can be seen that the frequency of the oscillator varied by roughly 26Hz during the heating cycle and 23Hz during the cooling cycle. This represents a change of approximately 2.2% which is of the same order as the tuning range of 1.5%. The temperature stability of this oscillator will need to be improved in order to make it a viable alternative to competing technologies, but this data represents a reasonable result for the first prototype as no design effort was expended to produce these results.

The frequency change exhibited by this design is the result of the combination of several factors. First, the coefficients of thermal expansion for the two layers of the structure are different. This results in the steel and PZT layers expanding at different rates, which causes an overall deflection of the beam. This induced deflection will cause a small change in the frequency of the oscillator. A second effect is due to the temperature dependence of some of the other parameters for the materials used, particularly Young's modulus, which affects the stiffness, and the electromechanical coupling factors. The sum of all of these effects results in the change in frequency that is seen at different temperatures. These temperature induced effects can be reduced by modifying the design of the structure. Possible modifications include the use of materials that have similar coefficients of expansion for the two layers, or using materials whose properties are not as greatly affected by temperature change. It may also be possible to limit these effects by designing the structure so that these effects are minimized or are offsetting in nature, but these possibilities will require further research. If none of these structure modifications can improve the frequency/temperature dependence to the desired level, it will be necessary to compensate for the temperature effects using the tuning abilities of the design.

7.0 INTEGRATED CIRCUIT DESIGN

As stated earlier, the prototype structure, whose results were presented in the last chapter, is only the first step toward producing a single-chip oscillator design. The next step on this path involves the construction of a smaller structure, which will be bonded to an integrated circuit. As covered in the discussion of quartz resonators, this is not a long term solution due to its high manufacturing cost, but is the next logical step in the design process. For this next step to be possible, it must be shown that the required electrical circuitry can be manufactured on a single integrated circuit. In order to demonstrate this, a prototype circuit was designed and fabricated using the AMI ABN 1.5μm BiCMOS process. Prototype runs for this process and several others are available through the MOSIS service[4]. The integrated circuit for this design includes each of the components of the prototype version discussed in the previous chapters. Careful design of several of these components is necessary and will be discussed in this chapter. Also covered in this chapter are the results, to date, from the fabrication of on-chip capacitors and switches.

7.1 Amplifier

The prototype design utilizes multiple 741 operational amplifiers to provide both gain and phase shift. In reality, an amplifier of this complexity is probably not required, nor even desired, for this design. Therefore, the integrated circuit version of the design employs a much simpler two-stage differential amplifier. This two stage amplifier makes use of a CMOS differential pair for the first stage followed by a common source second stage. Some of the difficulties that were encountered during the design of this element include the typical amplifier concerns of gain and bandwidth, but also included issues relating to the differential nature of the circuit. Since an on-chip resonator will be of considerably smaller size than the prototype structure, the frequency of operation will be significantly higher. Testing of this smaller structure has not yet been completed, but preliminary estimates place the frequency of operation in the range of tens to hundreds of kilohertz. Based on these requirements, it was decided that an amplifier with the highest gain possible, while still maintaining a bandwidth of several hundred kilohertz, should be

[4] MOSIS is a low-cost prototyping and small-volume production service for VLSI circuit development, more information is available online at www.mosis.org

sufficient. The gain and bandwidth requirements are contradictory in nature and the trade-offs that took place in the design of this amplifier will be discussed in the next section.

An additional complication of the amplifier design results from the need to produce both positive and negative voltages at the amplifier output. While many amplifier designs operate from a single supply voltage and thus produce a dc offset at the output, this would be undesirable for our design as it would produce a constant deflection of the beam structure. This constant deflection would result in a small shift in the frequency of the oscillator. While this change in frequency is small, we would like to avoid this issue, and thus the amplifier is designed to be operated with +/- 2.5V power supplies. In order for the circuit to operate using these supply voltages, however, the substrate of the CMOS circuit, which is typically grounded, must be connected to the negative supply voltage. This issue will become important in our discussion of the switches used for the interconnection of the tuning capacitors. The details of the design of the amplifier circuit, including simulation results, are given below.

7.1.1 Circuit Design

The basic topology of the amplifier is that of a CMOS differential pair as shown in Figure 7.1. The small signal gain of this circuit configuration is given by Equation (7.1).

$$A_v = \frac{v_o}{v_{id}} = g_m \frac{R_D}{2} \tag{7.1}$$

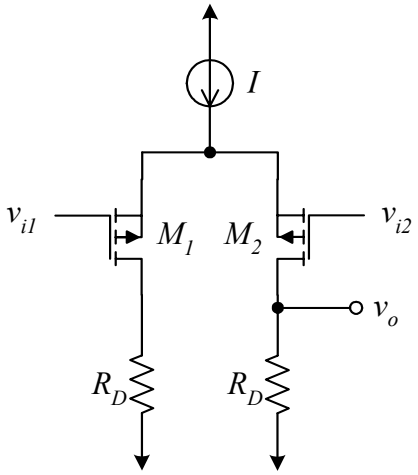

Figure 7.1: Basic CMOS Differential Pair

From this expression, we see that in order to get a high gain from this type of amplifier, we must have a high value for R_D. Further, if the two drain resistors are not matched exactly, the circuit will exhibit a dc offset at the output. Given that it is difficult to construct resistors in a CMOS process, especially large ones, we typically replace these resistors with an active load circuit. An active load, such as a current mirror, uses the properties of transistors to take the place of a load resistor. The basic current mirror, shown in Figure 7.2, uses the size ratio between two transistors to set the current ratio between them, as given in Equation (7.2).

$$\frac{I_O}{I_{REF}} = \frac{W_2 / L_2}{W_1 / L_1} \tag{7.2}$$

Using this circuit as an active load for the differential pair offers two significant advantages over the use of resistors. First, the output resistance of a CMOS transistor, on the order of 1MΩ, is

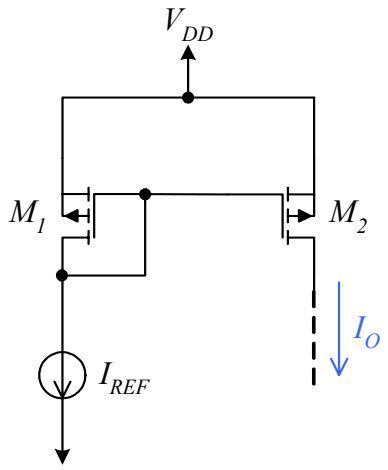

Figure 7.2: Basic CMOS Current Mirror

much higher than we would be able to attain using on-chip resistors. This means that we can get much higher gains from the differential pair using an active load than would be possible with integrated resistors. The second advantage is that it is much easier to match two transistors in a CMOS process than it is to match two resistors. Using resistors in the design would almost inevitably result in a dc offset on the output, which is undesirable for this amplifier design.

Referring back to the basic differential pair shown in Figure 7.1, we see that a current source is required to correctly bias the circuit. The CMOS implementation of this current source again makes use of a current mirror circuit, but instead of the standard mirror shown above, the chosen design makes use of a cascode current mirror. The benefit of using a cascode mirror is the increased output resistance of the current source, which is obtained at the expense of reduced voltage swing [9]. The basic structure of a cascode current mirror is shown in Figure 7.3.

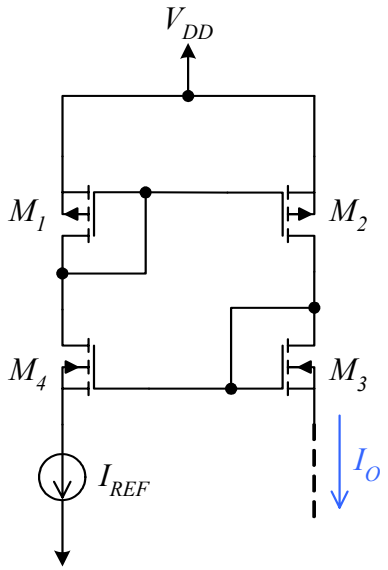

Figure 7.3: Cascode Current Mirror

Combining the differential pair with an active load and a cascode current source, we have a fully functional amplifier solution. The gain of this type of amplifier, however, is low at approximately 10V/V. To improve the gain of the amplifier, the sizes of the differential pair transistors could be increased, but this would adversely affect the bandwidth of the circuit. Instead, a second stage, which makes use of a simple common source amplifier, is added to the amplifier design. A common source amplifier, as shown in Figure 7.4, offers a relatively high gain while requiring a minimum of components. By combining this circuit with that of the differential pair discussed above, the resulting amplifier structure maintains the advantages of the

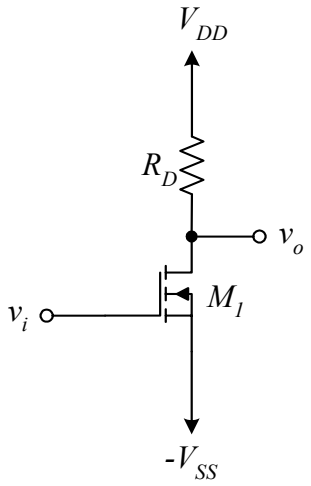

Figure 7.4: Basic Common Source Amplifier

differential pair but also exhibits higher gain due to the common source stage. The gain of the common source amplifier shown in the above figure is given by Equation (7.3).

$$A_v = \frac{v_o}{v_i} = g_m R_D \tag{7.3}$$

Again we see that a large resistor would be required to provide a high gain. As was the case with the differential pair, we can replace this resistor by an active load. In fact, when we cascade this amplifier circuit with the differential pair, the two active loads can be combined into a single current mirror circuit. The final amplifier design, showing the combined two-stage circuit, is shown in Figure 7.5. The performance of this circuit is presented in the following section.

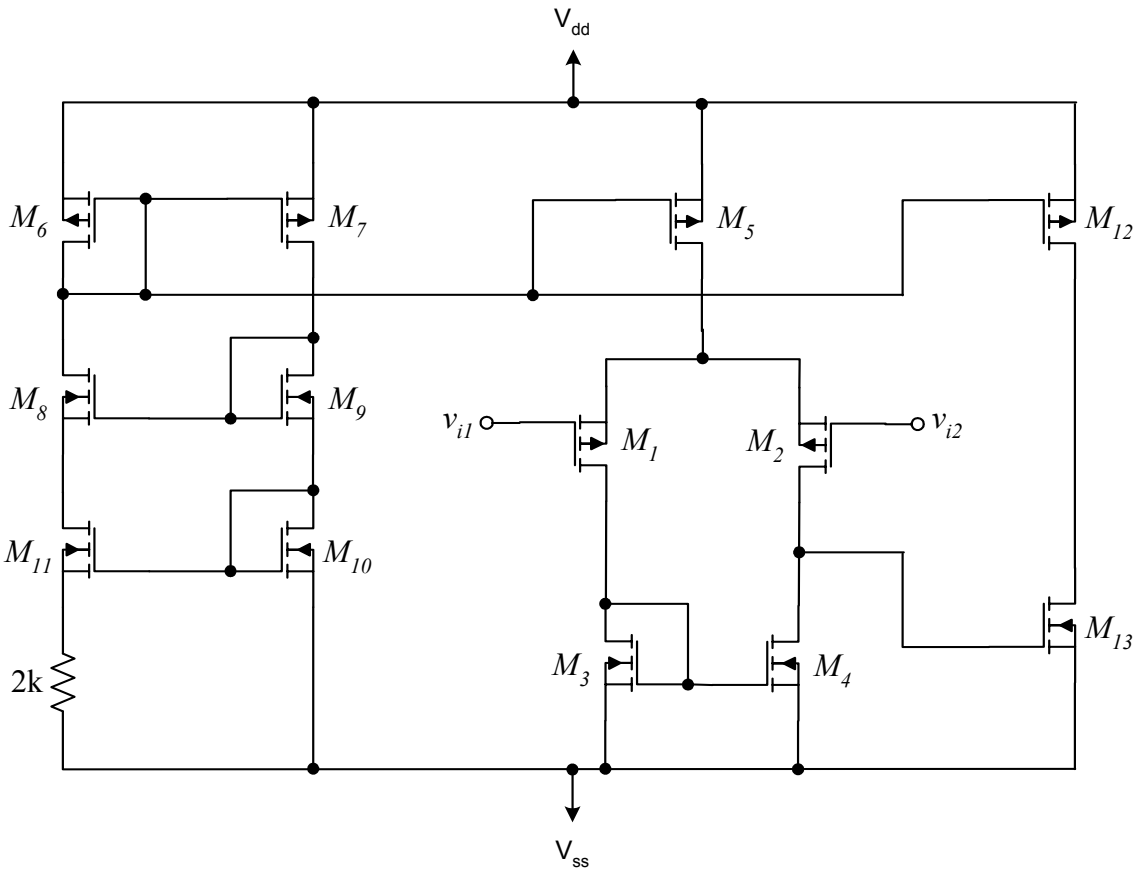

Figure 7.5: Complete Two Stage Amplifier Design

7.1.2 Simulation and Layout

Using the amplifier circuit shown above, SPICE simulations were performed to optimize the performance of the design. These simulations were performed using transistor parameter data provided by MOSIS for the AMI ABN 1.5μm BiCMOS process. Each transistor in the design was sized manually to provide the highest possible dc gain while maintaining the required bandwidth of the circuit. Given the design requirements, the transistor sizes that were used in the final design are presented in Table 4.

Table 4: Transistor Sizes for Integrated Circuit Amplifier

Transistor	Width (μm)	Length (μm)
M1	120	1.6
M2	120	1.6
M3	37.6	1.6
M4	37.6	1.6
M5-M10	25.2	1.6
M11	50.4	1.6
M12	25.2	1.6
M13	72.8	1.6

Using the above transistor sizes, the simulation results showed a dc gain of 599V/V and a 3dB bandwidth of 215kHz. The results of an ac sweep from 100Hz to 100MHz are shown in Figure 7.6. The SPICE code for this simulation is given in Appendix A. Based upon these results, a layout was created so that the design could be fabricated using the AMI ABN process. This layout is shown in Figure 7.7.

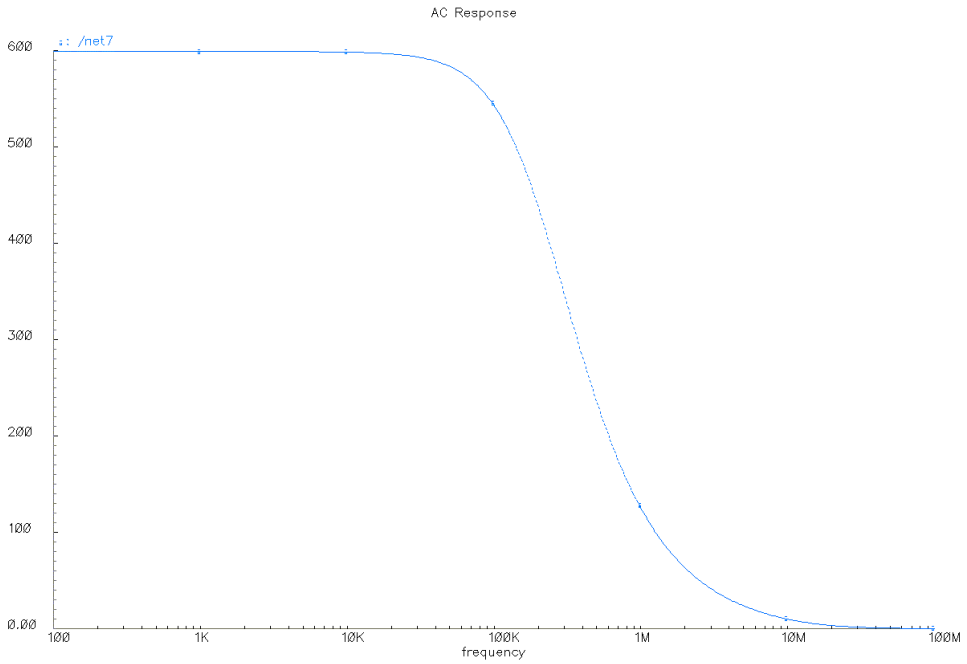

Figure 7.6: SPICE Simulation Results for Two Stage Amplifier

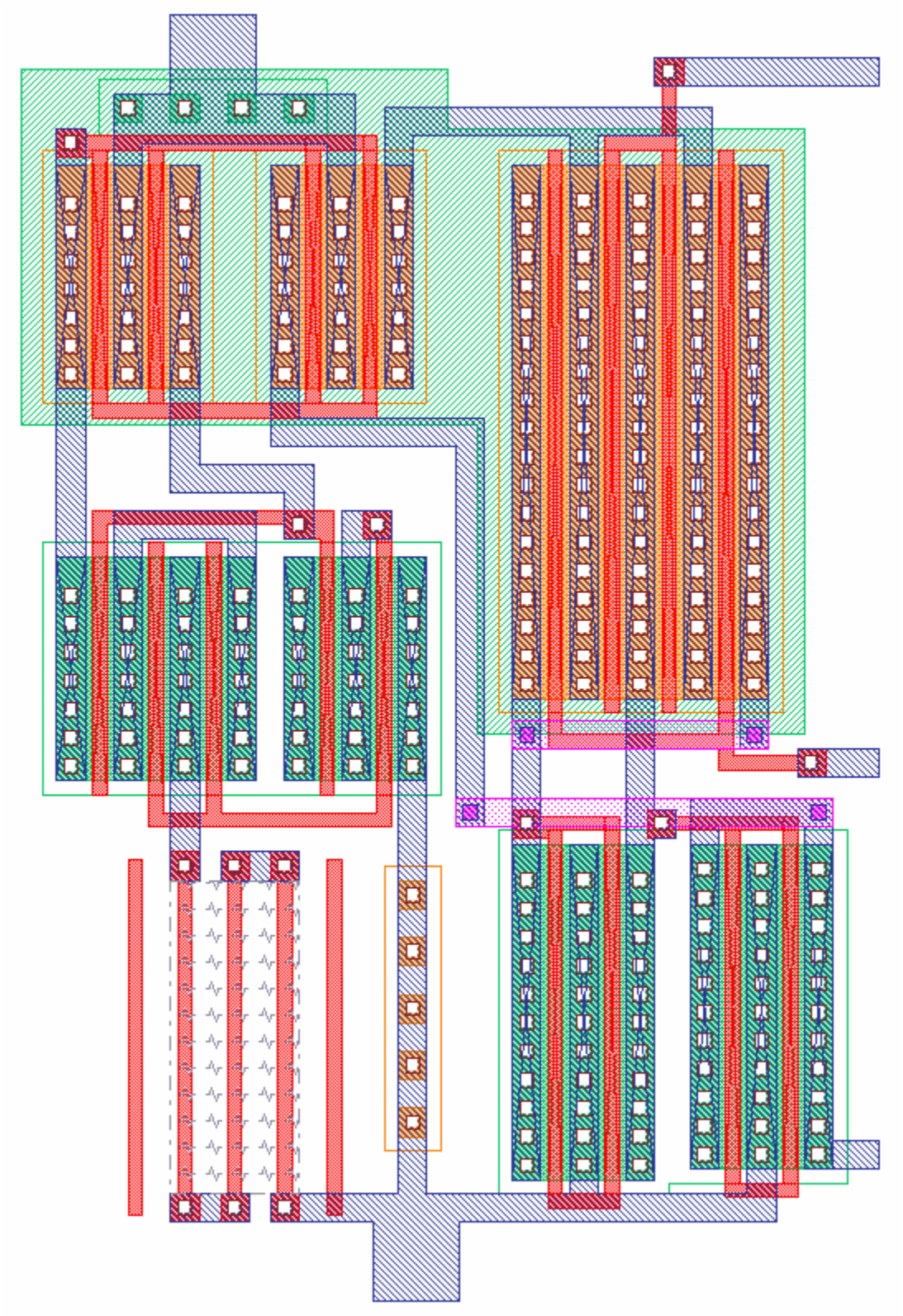

Figure 7.7: Two Stage Amplifier Layout

7.2 Tuning Capacitors

As discussed in Section 4.2, tuning of this oscillator design depends directly on the use of tuning capacitors whose values set the frequency of oscillation. To demonstrate the ability to tune our on-chip oscillator, multiple valued capacitors must be integrated onto the chip. In order to tune the oscillator with any degree of accuracy, it is important that these capacitors are accurately sized. Historically, on-chip capacitors have had poor tolerances, up to 20%, and it was our goal to design and fabricate capacitors with much better absolute accuracy. To accomplish this goal, we employed various design and layout techniques as discussed in the following section.

7.2.1 Capacitor Design

An integrated circuit capacitor is a relatively simple device that is constructed of two conducting layers separated by an insulating dielectric. These conducting layers can be any two of the layers provided by a CMOS process, such as poly and metal1 or metal1 and metal2. A graphical representation of the basic layout and construction of a simple CMOS capacitor is shown in Figure 7.8. The expression for the capacitance of an on-chip structure is given by

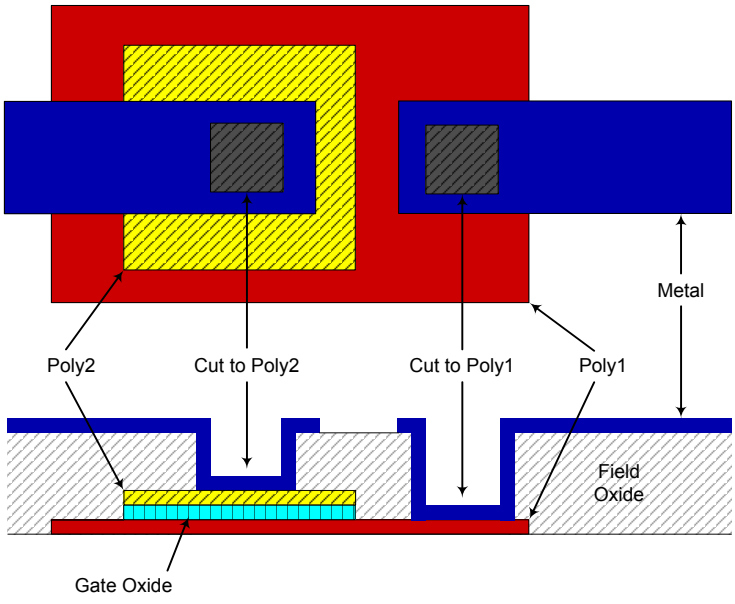

Figure 7.8: Poly-to-Poly Capacitor Construction

Equation (7.4), where C_{ox} is a process parameter which quantifies the interlayer capacitance for the two layers used.

$$C = \frac{\varepsilon A}{d} = C_{ox} A \tag{7.4}$$

For our design, we require relatively large valued capacitors which could not be implemented in a reasonable area using two metal layers. Instead, our capacitor designs make use of an additional layer of polysilicon which is provided by many analog processes specifically for this use. Poly-to-poly capacitors, as they are known, exhibit much higher capacitance per unit area compared to poly-to-metal or metal-to-metal capacitors. A comparison of the interlayer capacitance for the various layers of the AMI ABN process is given in Table 5 [7]. In this table, the layers on the left hand side represent the bottom plate of the capacitor whereas the layers

Table 5: Inter-Layer Capacitance Parameters for the AMI ABN Process

	N+Active	P+Active	Poly1	Poly2	Metal1	Metal2
Substrate	267	304	38		25	15
N+Active			1109	712	51	25
P+Active			1091	704		
Poly1				574	46	22
Poly2					46	
Metal1						36

across the top of the table represent the top plate. All capacitance values listed in the table are in units of attofarads[5] per square micron ($aF/\mu m^2$). As can be noted from the table, the capacitor structure which would have the highest capacitance per area would be poly over active, but this type of structure is not typically used. This is true because, using this structure, one plate of the capacitor would be constructed of an active area of the chip. This is undesirable due to the noise

[5] atto=10^{-18}

introduced into the substrate by this connection as well as the high series resistance of that plate. Therefore, the most desirable structure for an on-chip capacitor is built using poly1 and poly2, because it exhibits a much higher capacitance per unit area than metal-to-metal capacitors. Further, since the additional polysilicon layer is specifically intended for use in capacitor designs, the resulting structures do not exhibit the undesirable effects of the other types. It is for these reasons that our capacitor designs use poly-to-poly capacitors with a nominal capacitance of 600aF/μm^2.

There are two effects that can significantly reduce the absolute accuracy of integrated circuit capacitors. In order for our designs to exhibit high accuracy, we must carefully design our capacitors so as to minimize these effects. These two issues are over-etching and oxide gradients. Over-etching is the result of the fact that the wet etching commonly used in integrated circuit fabrication is completely isotropic, meaning that it etches in all directions at an equal rate [10]. Since the layer that is being etched has some finite thickness, the chemical etchant will begin to etch away some of the material under the edges of the photoresist before it has removed the entire layer. This effect is depicted in Figure 7.9 where we can see that the etching has proceeded slightly beneath the photoresist material. Over-etching results in fabricated structures

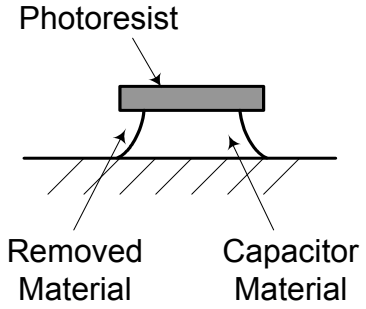

Figure 7.9: Example of the Effect of Over-Etching

that are smaller than designed and, for capacitor designs, this implies that the values of the capacitors are smaller than intended. Since the effect of over-etching is proportional to the perimeter to area ratio of the structure being etched, to minimize the over-etching effect we need to minimize this ratio [5]. The structure which exhibits the best perimeter to area ratio is a circle,

whose ratio is $2/\pi$, but round structures cannot be built in most processes. Using only 45° and 90° angles in the layout, which can be fabricated in the ABN process, the next best structure is that of an octagon, and it is this shape that has been used in our designs.

Besides minimizing the perimeter to area ratio for the layout, there are two additional steps that help to minimize over-etching effects. The first of these involves using unit size capacitor sections so that over-etching will affect all capacitors equally. By using unit sized sections and connecting a number of them in parallel to build a larger capacitor, different size capacitors will be over-etched in proportion to their values. This is true because each unit capacitor will be over-etched by the same amount, and thus the sum of the error will be proportional to the value of the capacitor. This result will maintain the ratio of actual value to expected value at a constant across designs. The second method involves using a bottom plate that is larger in area than the top plate so that only the over-etching effects of the top plate affect the overall capacitance value. A graphical representation of this concept is shown in Figure 7.10. As can be seen from the figure, if both plates are designed to be the same area, the value of the

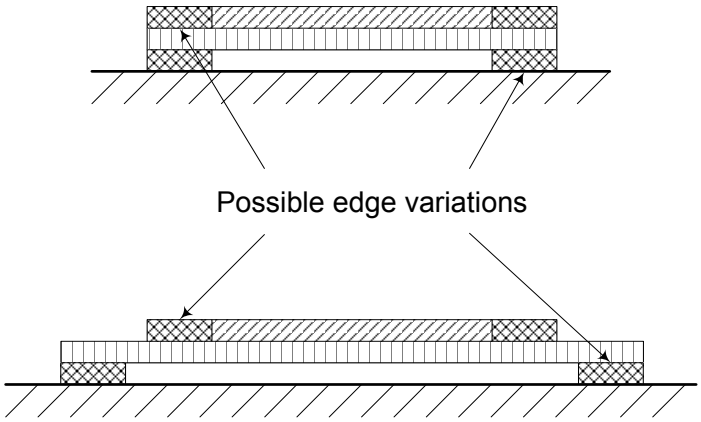

Figure 7.10: Design Using Larger Bottom Plate to Reduce the Effect of Over-Etching

capacitor will depend on the error introduced in etching both plates. If, however, we use a bottom plate that is larger than top plate, even when considering the worst case etching effect, the overall value depends only on the error introduced when etching the top plate. An additional source of error in capacitor designs is that introduced due to an oxide gradient across the chip.

Since the capacitance of a structure depends upon the separation between its plates, a gradient in the oxide layer which separates the two plates will cause a change in the capacitor value. Unfortunately there is no way to compensate for this to improve the absolute error of the designs. Common-centroid layout techniques are used to minimize this effect when designing ratioed capacitors, but the capacitors used for this design are required to be a specific value rather than a ratio.

7.2.2 Layout and Fabrication Results

Using the layout techniques discussed above, two different capacitor designs were constructed. One design uses unit size capacitors that are square and the other uses octagons. Both of these designs have been fabricated, with the results given in Table 6. These results are for a lot of five chips fabricated on a single run. Both capacitor designs were included on the

Table 6: 22.5pF Capacitor Fabrication Results

22.5pF Square Layout			22.5pF Octagon Layout		
Expected	**Measured**	**Error**	**Expected**	**Measured**	**Error**
22.47	22.29	0.80%	22.46	22.50	0.18%
22.47	22.33	0.62%	22.46	22.47	0.04%
22.47	22.15	1.42%	22.46	22.33	0.58%
22.47	22.36	0.49%	22.46	22.55	0.40%
22.47	22.04	1.91%	22.46	22.25	0.93%

same chip and the results were measured using an Agilent 4284A Precision LCR meter. Similar results were measured with a smaller sample from two other fabrication runs. The layout for a 22.5pF capacitor using octagonal sections is shown in Figure 7.11. The corresponding layout using square unit capacitors is shown in Figure 7.12.

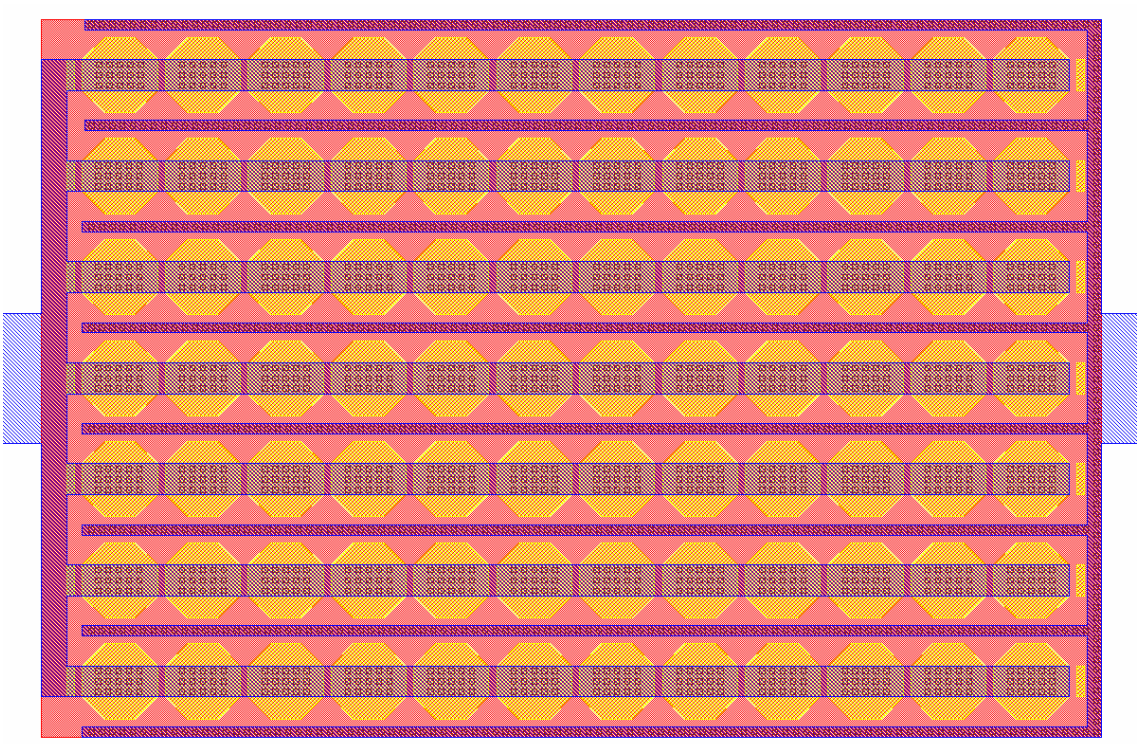

Figure 7.11: 22.5pF Capacitor Layout using Octagons

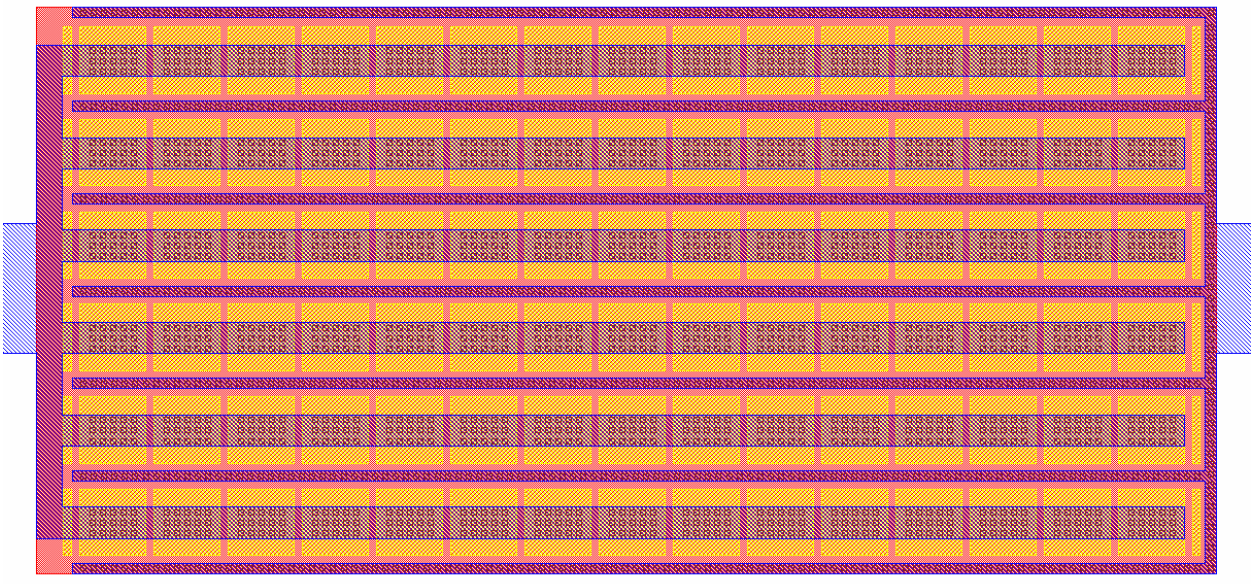

Figure 7.12: 22.5pF Capacitor Layout using Squares

Examining the results in Table 6, we can see that both types of layout produced results that were significantly better than the 20% tolerances that are typically quoted for poly-to-poly capacitors. Further, we can see that the octagonal layouts performed better than the square ones by producing consistently higher capacitances. This finding is in agreement with the reduction in over-etching that should occur using octagonal structures as opposed to square. While the error of the octagonal design is smaller than that of the square design, there is an additional area penalty for using octagonal sections. For example, the total area required for the capacitor in Figure 7.11 was roughly 72,600μm^2 while that of Figure 7.12 was only 63,000μm^2. We can see that the roughly 1% improvement in tolerances of the octagonal capacitors results in a 15% increase in total area. For this design, however, area is not a primary concern, while the improved tolerance directly relates to improved oscillator performance. Since the capacitors in this design are used to control the frequency of operation while tuning the oscillator, the accuracy of their values is extremely important. The fabrication results presented above are also significant because they show that, using careful layout techniques, capacitors with absolute tolerances of better than 5% can be built using a standard CMOS process.

7.3 Analog Switches

In order to tune the frequency of operation using the capacitors discussed above, it must be possible to add or remove these components from the tuning network. For the prototype system, this was accomplished using mechanical switches. For an integrated circuit version, however, these switches must be constructed on-chip using CMOS transistors. The design of these switches is discussed in the following section.

7.3.1 Pass Transistor Design

A mechanical switch, when placed into an electrical circuit, is nearly an ideal component, featuring an infinite off resistance and a very low on resistance. When trying to replace this type of element with a similar solution using CMOS transistors, some trade-offs must be made. For example, since a CMOS transistor does not physically break the connection between its source and drain when turned off, there will be a finite off resistance. Further, since the transistor uses a semiconductor substrate, the on resistance of the resulting switch will be significantly higher than a mechanical version. In our oscillator design, the infinite off resistance is not of significant

importance, but a large on resistance would adversely affect the quality factor of the entire oscillator circuit. To minimize this resistance the switch design utilizes a standard CMOS pass gate, which consists of one NMOS and one PMOS transistor connected as shown in Figure 7.13.

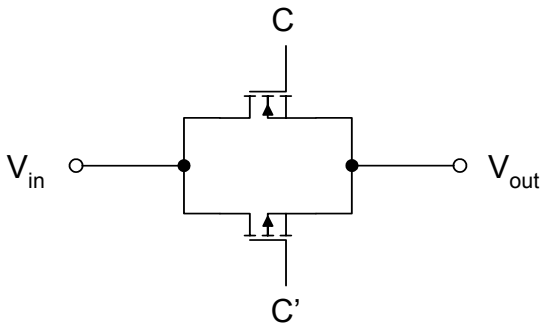

Figure 7.13: CMOS Pass Gate

A simple switch could be constructed using either one of these types of transistor, but the effective resistance of a transistor is dependent upon the drain to source voltage. The resistance versus input voltage curve varies for N and P type transistors and is shown in Figure 7.14 along with that of the complementary pass gate. This figure shows the resistance of the switch when

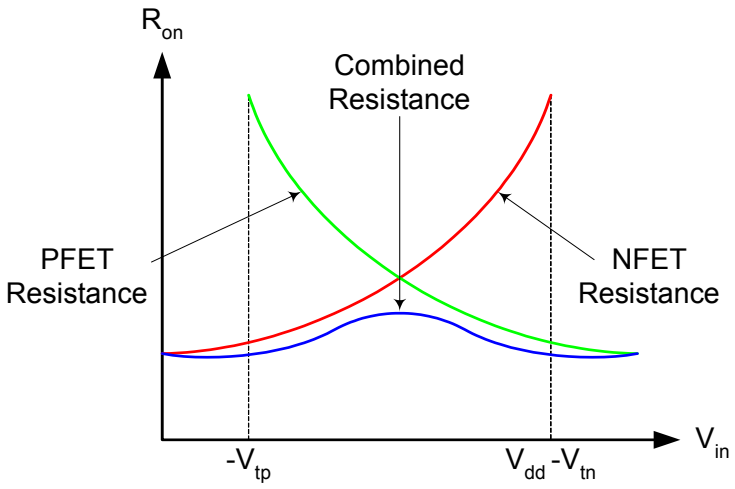

Figure 7.14: Resistance of PFET, NFET, and Complementary Type Switches

the inputs are connected such that the switch is operating in the "on" mode. Notice that, at input voltages below V_{tp}, the P transistor is off and exhibits a very high resistance. A similar statement can be made about the N transistor at input voltages above V_{dd}-V_{tn}. By placing the two types of transistor in parallel, the high resistance exhibited by the P transistor at low voltages is offset by the low resistance of the N transistor at that voltage and vice versa. In this way, the compound circuit exhibits a much lower average resistance, but more importantly this resistance is less dependent on the input voltage. These properties make the CMOS pass gate much more suitable for switch applications than a single N or P transistor.

Note, however that the compound circuit then requires a control signal and its complement in order to function properly. In order to minimize the interface pins required, an inverter has been integrated into the design to provide the complement of the control signal. It is here that the issue of having a non-grounded chip substrate becomes important. The pass gate and the inverter are controlled by digital signals which are normally +5V and 0V because the power supplies for the circuit typically have these values. By operating the amplifier circuit from a +/-2.5V supply, we are also requiring that the digital portion operate with these values. The primary implication of this is that a digital '1' is represented by +2.5V and a digital '0' is represented by -2.5V and that the external control signals must follow this format.

7.3.2 Layout and Fabrication Results

The layout for the above pass gate is shown in Figure 7.15. As mentioned above, this layout integrates the inverter necessary to produce the complement of the control signal rather than requiring two complementary control signals to be provided. The layout has been optimized in such a manner that it is possible to easily connect several of these switches in series as will be used in constructing the tuning network. Results of testing the fabricated switch show a high off resistance of several mega-ohms and an on resistance of approximately 60Ω. A lower on resistance may be possible by making the transistors larger, but there is a limit to the minimum resistance that can be obtained. Due to the relationship between transistor size and resistance for this circuit, we believe that this circuit approaches that minimum and a larger design would be beyond the point of diminishing returns.

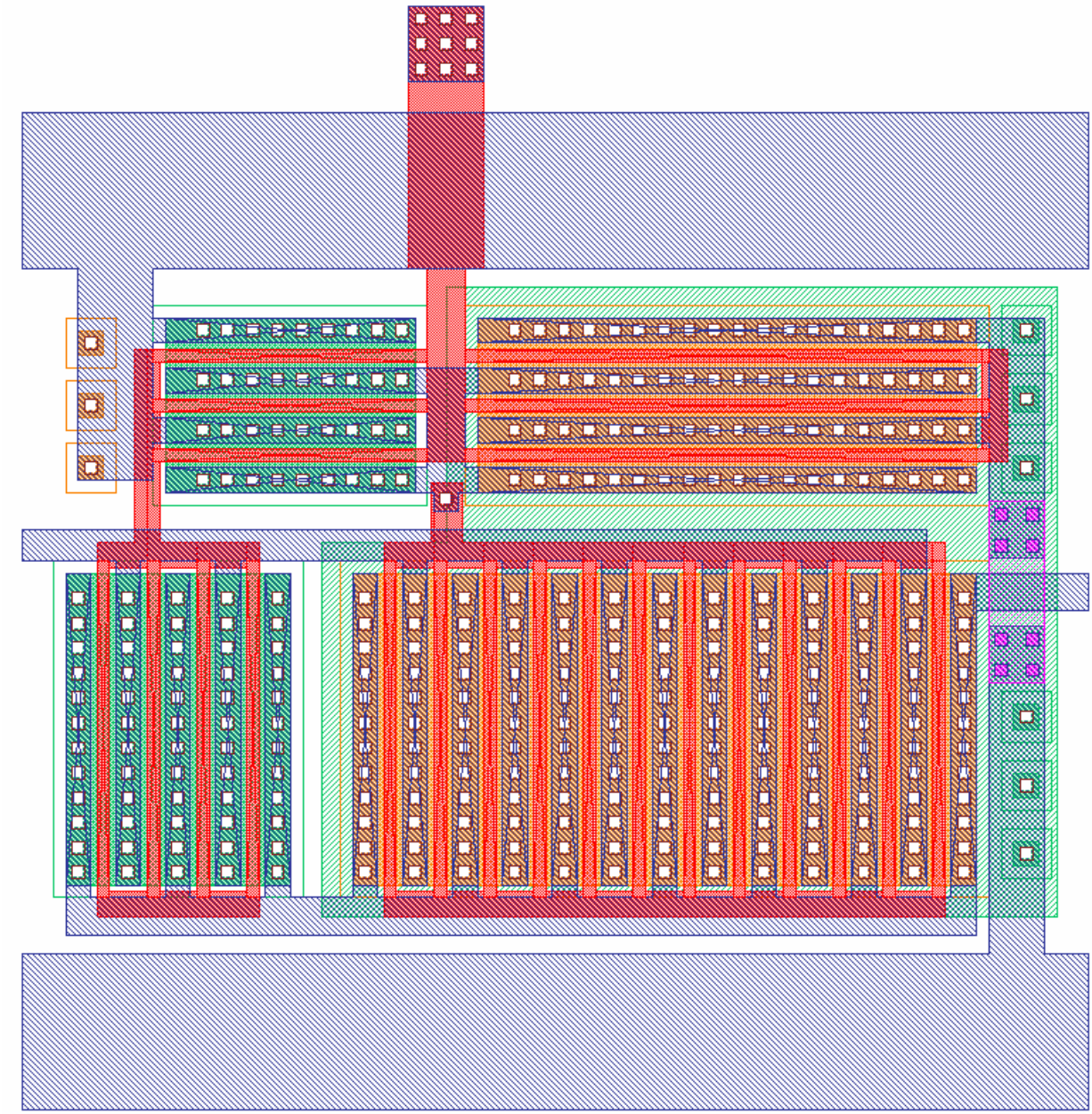

Figure 7.15: Layout of CMOS Pass Gate with Integrated Inverter

8.0 SUMMARY AND CONCLUSION

In this thesis, we have presented the design, development, simulation, and testing of a new oscillator technology which makes use of a piezoelectric resonator. Experimental results from a macro-scale prototype demonstrate the frequency tuning and switching ability of the design and simulation results show that an accurate electrical model can be developed for the structure. This first prototype was used to demonstrate the abilities of the design and the development of a second, smaller, prototype structure is nearing completion. This second prototype, which will be bonded to the integrated circuit, is the next step toward the goal of creating a single chip oscillator solution. To this end, a collection of the integrated circuit components that are required to control and tune this second prototype were designed and fabricated. The remainder of this chapter revisits the specific advancements made during this research as well as applications of the new oscillator design and ends with a discussion of areas of future consideration.

8.1 Summary of Advancements

There are several areas in which we feel that we have made significant advancements during this research. For example, the ability to accurately model the mechanical behavior of the resonator structure using an electrical equivalent circuit is of great importance to the design of future oscillators. This modeling allows for much simpler design and simulation of new designs without the costly and time consuming process of fabricating the structures. We feel that this modeling of the structure is one of the most important outcomes of this research. Further, the ability to switch between mechanical modes using the phase shift network is a novel solution that is important to the oscillator design. Several areas of the integrated circuit design are also noteworthy. The design of the integrated circuit amplifier and transistor based switches allows the design to proceed to the micro-scale that will be required in future research. While the design of these components is not necessarily superior, the results obtained with the integrated circuit capacitors represent a significant improvement over previous designs. The ability to fabricate CMOS capacitors with absolute tolerances of less than 1% allows for the design of circuits that require high precision absolute capacitances. In this design, these high precision capacitors can be used to tune the oscillator frequency with a high degree of accuracy.

8.2 Advantages and Applications

Now that we have presented the design and testing of this new oscillator, let us examine the benefits and possible applications of such a design. The first and most important benefit of this design is ability to integrate a high performance oscillator design onto an integrated circuit. This is made possible by the piezoelectric resonator, which, unlike a quartz crystal, possesses the scalability necessary to be constructed on-chip. The piezoelectric resonator in this design also provides the ability to switch and tune the frequency of oscillation. Switching of the frequency allows the oscillator to operate at any one of a set of frequencies and provides much greater flexibility than other oscillator solutions. Tuning in the design allows for adjustment of the frequency due to manufacturing variability or temperature changes, and the tuning range is significantly larger than that of a quartz crystal design. This increased range not only allows for compensation due to the above effects, but allows for the use of multiple frequencies within the tuning range, limited only by the resolution of the tuning network.

A very large number of applications could make use of the advantages of our new oscillator design. If the manufacturing costs of the new design are not prohibitive, it is obvious that any application that uses an alternative type of on-chip oscillator might make use of this design due to its higher quality factor and increased tuning range. The frequency switching and tuning abilities of the design open the door to a wide range of oscillator applications. One such example is that of the frequency hopping techniques used in many digital communication systems, such as cellular telephony. Currently, the number of communication channels is limited due to the bandwidth allocation and the required separation between channels. This separation must be maintained due to the poor quality of the oscillators used to generate the frequency reference. With a higher quality oscillator, such as described in this thesis, these channel separations could be reduced. This would be possible because the tuning range of the oscillator allows it to be used for every carrier frequency whereas, given a quartz oscillator, each frequency would require its own crystal. This is only one simple example and many additional new oscillator applications could, of course, be developed using this new oscillator design.

8.3 Future Work

Given that the oscillator prototype was constructed using off-the-shelf components and a macro-scale resonator, the most obvious area of future consideration is a second resonator

prototype, which will be bonded to the integrated circuit discussed in Chapter 7.0. This prototype will begin to demonstrate the scalability required to make a single-ship oscillator. The final step in this progression would be to construct the piezoelectric resonator on-chip with the tuning and control electronics. The fabrication techniques used for the two prototype structures are not well suited to an on-chip resonator, but appropriate fabrication procedures have been demonstrated elsewhere [11]. Other concerns with an on-chip prototype include the frequency of the structure and, therefore, the requirements of the on-chip amplifier. Since an on-chip structure would be of considerably smaller size than the prototype structure, the resonant frequencies will be significantly higher. This higher frequency may require an alternative amplifier design in order to provide the gain and bandwidth required for the oscillator design. Along with the integration of the current resonator design, alternative structure designs might be explored. Alternate designs to improve the frequency/temperature characteristics or increase the quality factor, have been considered, but no such structures have been built to date.

In addition to a single chip implementation of the design, there are several features which could be added or improved to produce a much more robust oscillator design. Since each mechanical mode has a different magnitude response, the gain of the amplifier currently must be adjusted each time the frequency is changed. Simplifying this process, by implementing some form of automatic gain control, would greatly enhance the usability of this design. Similarly a method of integrated temperature compensation would also be of particular use. This could be accomplished by integrating some form of temperature sensor that would be used to adjust the tuning capacitors so as to maintain frequency stability. As the tuning function of this new oscillator is of significant importance to the design, improving the resolution and accuracy of the tuning method might also be explored. To accomplish this, we could replace the smallest capacitor in the tuning network with a CMOS varactor, or voltage controlled capacitor, in order to allow very fine frequency adjustments. To simplify the use of the tuning network, a digital control circuit could be developed which would ease the tuning process. This circuit might, for example, accept an 8-bit word which would correspond to the desired frequency. The control circuit could then decode this word and apply the appropriate shunt capacitance to the structure to obtain this frequency. The above additions to the design represent only a small subset of the improvements that could be made during future research with this oscillator design.

APPENDICES

APPENDIX A

Equivalent Circuit Simulation

```
* SPICE input file for resonator equivalent circuit
*
*  November 5, 2002
*  Matthew Volkar
*

.OPTIONS LIST NODE POST
.temp 27


* AC analysis
.op
.ac lin 501 1 5.001k

* Log the output voltage
.print AC V(out)

* Measure the peak of each mode
.MEAS AC max1 MAX V(out1)
.MEAS AC max2 MAX V(out2)
.MEAS AC max3 MAX V(out3)
.MEAS AC max4 MAX V(out4)
.MEAS AC max5 MAX V(out5)

* Input sources
VIN input gnd AC 1

* RLC equivalent circuit
.SUBCKT rlc in+ in- out R=10 L=10m C=10u
R1 in+ t1  R
L1 t1  out L
C1 out in- C
Rt out in- 10X
.ENDS

* Test circuit
C0 input gnd 20n
```

```
E1 Vm1+ gnd input gnd 0.789m
X1 Vm1+ gnd out1 rlc R=15.7m  L=3.372m C=4.218m
E1out out temp1 out1 gnd 1

E2 Vm2+ gnd input gnd 0.677m
X2 Vm2+ gnd out2 rlc R=55.4m  L=1.753m C=93.20u
E2out temp1 temp2 out2 gnd 1

E3 Vm3+ gnd input gnd 5.057m
X3 Vm3+ gnd out3 rlc R=111.0m L=1.821m C=10.13u
E3out temp2 temp3 out3 gnd -1

E4 Vm4+ gnd input gnd 2.772m
X4 Vm4+ gnd out4 rlc R=259.2m L=1.818m C=2.600u
E4out temp3 temp4 out4 gnd 1

E5 Vm5+ gnd input gnd 6.952m
X5 Vm5+ gnd out5 rlc R=604.5m L=1.818m C=0.950u
E5out temp4 gnd out5 gnd 1

.END
```

APPENDIX B

Integrated Circuit Amplifier Simulation

```
* # FILE NAME: /AFS/EE.PITT.EDU/USR/GRAD/MATT/CADENCE/SIMULATION/OPAMPTEST/
* HSPICES/SCHEMATIC/NETLIST/OPAMPTEST.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON NOV 26 14:09:24 2002

* FILE NAME: CLARK04_OPAMPTEST_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: OPAMPTEST.
* GENERATED FOR: HSPICES.
* GENERATED ON NOV 26 14:09:25 2002.

R0 NET7  0    1E6 M=1.0
C0 NET7  0    13E-12 M=1.0
X1 NET12 NET3 0 NET7 NET1 OPAMP_G1
V2 NET3  0    AC 1.0 0.0 SIN 0.0 1E-3 10E3
V1 0     NET1 2.5
V0 NET12 0    2.5


* FILE NAME: CLARK04_OPAMP_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: OPAMP.
* GENERATED FOR: HSPICES.
* GENERATED ON NOV 26 14:09:24 2002.

* TERMINAL MAPPING: VDD = VDD
*                   VIN1 = VIN1
*                   VIN2 = VIN2
*                   VOUT = VOUT
*                   VSS = VSS
.SUBCKT OPAMP_G1 VDD VIN1 VIN2 VOUT VSS
R0 NET020 VSS 2E3 M=1.0
M12 VOUT NET041 VDD VDD AMI16P L=1.6E-6 W=25.2E-6 AD=100.8E-12 AS=100.8E-12
+PD=58.4E-6 PS=58.4E-6 M=1
M7 NET039 NET041 VDD VDD AMI16P L=1.6E-6 W=25.2E-6 AD=100.8E-12 AS=100.8E-12
+PD=58.4E-6 PS=58.4E-6 M=1
M5 NET034 NET041 VDD VDD AMI16P L=1.6E-6 W=25.2E-6 AD=100.8E-12
+AS=100.8E-12 PD=58.4E-6 PS=58.4E-6 M=1
M6 NET041 NET041 VDD VDD AMI16P L=1.6E-6 W=25.2E-6 AD=100.8E-12
+AS=100.8E-12 PD=58.4E-6 PS=58.4E-6 M=1
M2 NET0106 VIN1 NET034 VDD AMI16P L=1.6E-6 W=120E-6 AD=480E-12 AS=480E-12
+PD=248E-6 PS=248E-6 M=1
```

```
M1 NET069 VIN2 NET034 VDD AMI16P L=1.6E-6 W=120E-6 AD=480E-12 AS=480E-12
+PD=248E-6 PS=248E-6 M=1
M13 VOUT NET0106 VSS VSS AMI16N L=1.6E-6 W=72.8E-6 AD=291.2E-12 AS=291.2E-12
+PD=153.6E-6 PS=153.6E-6 M=1
M9 NET039 NET039 NET045 VSS AMI16N L=1.6E-6 W=25.2E-6 AD=100.8E-12
+AS=100.8E-12 PD=58.4E-6 PS=58.4E-6 M=1
M8 NET041 NET039 NET047 VSS AMI16N L=1.6E-6 W=25.2E-6 AD=100.8E-12
+AS=100.8E-12 PD=58.4E-6 PS=58.4E-6 M=1
M10 NET045 NET045 VSS VSS AMI16N L=1.6E-6 W=25.2E-6 AD=100.8E-12
+AS=100.8E-12 PD=58.4E-6 PS=58.4E-6 M=1
M11 NET047 NET045 NET020 VSS AMI16N L=1.6E-6 W=50.4E-6 AD=201.6E-12
+AS=201.6E-12 PD=108.8E-6 PS=108.8E-6 M=1
M3 NET069 NET069 VSS VSS AMI16N L=1.6E-6 W=37.6E-6 AD=150.4E-12 AS=150.4E-12
+PD=83.2E-6 PS=83.2E-6 M=1
M4 NET0106 NET069 VSS VSS AMI16N L=1.6E-6 W=37.6E-6 AD=150.4E-12
+AS=150.4E-12 PD=83.2E-6 PS=83.2E-6 M=1


* END OF SUBCIRCUIT DEFINITION.
.ENDS OPAMP_G1



* RUN T27G AUG-19-2002
.MODEL AMI16N NMOS ( LEVEL=49 VERSION=3.1 TNOM=27 TOX=3.03E-8 XJ=3E-7
+NCH=7.5E16 VTH0=0.5285518 K1=0.8983497 K2=-7.41330000E-02 K3=7.8351417
+K3B=-2.43597210E+00 W0=1.869568E-6 NLX=1E-8 DVT0W=0 DVT1W=0 DVT2W=0
+DVT0=1.0696066 DVT1=0.1454382 DVT2=0 U0=669.3622887 UA=1.562141E-9
+UB=1.45844E-18 UC=2.730079E-11 VSAT=1.066931E5 A0=0.5900469 AGS=0.1191453
+B0=2.585061E-6 B1=5E-6 KETA=-4.03904500E-03 A1=0 A2=1 RDSW=2.637669E3
+PRWG=-4.88367000E-02 PRWB=-1.24906500E-01 WR=1 WINT=6.997185E-7
+LINT=1.618422E-7 XL=0 XW=0 DWG=-1.64569200E-08 DWB=3.589272E-8 VOFF=0
+NFACTOR=1.0043295 CIT=0 CDSC=0 CDSCD=0 CDSCB=0 ETA0=-1.00000000E+00
+ETAB=0.132926 DSUB=1 PCLM=1.1620758 PDIBLC1=9.557769E-3 PDIBLC2=3.562906E-3
+PDIBLCB=-1.00000000E-01 DROUT=0.0654525 PSCBE1=2.49997E9 PSCBE2=5.729251E-10
+PVAG=4.731649E-6 DELTA=0.01 RSH=53.5 MOBMOD=1 PRT=0 UTE=-1.50000000E+00
+KT1=-1.100000E-01 KT1L=0 KT2=0.022 UA1=4.31E-9 UB1=-7.61000000E-18
+UC1=-5.600000E-11 AT=3.3E4 WL=0 WLN=1 WW=0 WWN=1 WWL=0 LL=0 LLN=1 LW=0 LWN=1
+LWL=0 CAPMOD=2 XPART=0.5 CGDO=1.84E-10 CGSO=1.84E-10 CGBO=1E-9 CJ=2.73834E-4
+PB=0.99 MJ=0.5554223 CJSW=1.466161E-10 PBSW=0.99 MJSW=0.1 CJSWG=6.4E-11
+PBSWG=0.99 MJSWG=0.1 CF=0 )


*RUN T27G   AUG-19-2002
.MODEL AMI16P PMOS( LEVEL=49 VERSION=3.1 TNOM=27 TOX=3.03E-8 XJ=3E-7
+NCH=2.4E16 VTH0=-8.47640400E-01 K1=0.4513608 K2=2.379699E-5 K3=13.3278347
+K3B=-2.22383320E+00 W0=9.577236E-7 NLX=1E-6 DVT0W=0 DVT1W=0 DVT2W=0
+DVT0=1.3845575 DVT1=0.3624043 DVT2=-5.25832000E-02 U0=236.8923827
+UA=3.833306E-9 UB=1.487688E-21 UC=-1.085620E-10 VSAT=1.809501E5 A0=0.6765573
+AGS=0.13997 B0=3.584033E-6 B1=5E-6 KETA=-2.97771800E-04 A1=0 A2=0.364
+RDSW=765.4044729 PRWG=0.3 PRWB=-3.00000000E-01 WR=1 WINT=7.565065E-7
+LINT=2.23361E-8 XL=0 XW=0 DWG=-2.13917000E-08 DWB=3.857544E-8
+VOFF=-8.77184000E-02 NFACTOR=0.2508342 CIT=0 CDSC=2.924806E-5
+CDSCD=1.497572E-4 CDSCB=1.091488E-4 ETA0=0.18903 ETAB=-1.40599000E-02
+DSUB=0.2873 PCLM=2.8739038 PDIBLC1=0 PDIBLC2=1E-3 PDIBLCB=-1.00000000E-03
+DROUT=0.021755 PSCBE1=3.34835E9 PSCBE2=5.01352E-10 PVAG=15 DELTA=0.01 RSH=75
+MOBMOD=1 PRT=0 UTE=-1.50000000E+00 KT1=-1.10000000E-01 KT1L=0 KT2=0.022
```

```
+UA1=4.31E-9 UB1=-7.61000000E-18 UC1=-5.60000000E-11 AT=3.3E4 WL=0 WLN=1 WW=0
+WWN=1 WWL=0 LL=0 LLN=1 LW=0 LWN=1 LWL=0 CAPMOD=2 XPART=0.5 CGDO=2.23E-10
+CGSO=2.23E-10 CGBO=1E-9 CJ=3.066249E-4 PB=0.7191052 MJ=0.4241436
+CJSW=1.679172E-10 PBSW=0.99 MJSW=0.1258493 CJSWG=3.9E-11 PBSWG=0.99
+MJSWG=0.1258493 CF=0 )

* END OF NETLIST


.AC DEC  101.000  100.000  1.000000E+08
.TEMP    25.0000
.OP
.save
.OPTION INGOLD=2 ARTIST=2 PSF=2 PROBE=0
.END
```

BIBLIOGRAPHY

BIBLIOGRAPHY

[1] Griffith, J. M. (1994). Development and Advancements in SC-Cut Crystals. Retrieved November 22, 2002 from Corning Frequency Control Inc. web site: http://www.corningfrequency.com/library/dasc.html

[2] Time and Frequency from A to Z. (n.d.). Retrieved October 28, 2002, from National Institute of Standards and Technology Boulder Laboratories web site: http://www.boulder.nist.gov/timefreq/general/glossary.htm

[3] Parzen, B. with Ballato, A. Design of Crystal and Other Harmonic Oscillators. John Wiley & Sons, 1983.

[4] Vig, J. R. (1992). Introduction to Quartz Frequency Standards. Retrieved November 11, 2002, from IEEE Ultrasonics, Ferroelectrics and Frequency Control Society web site: http://www.ieee-uffc.org/freqcontrol/quartz/vig/vigtoc.htm

[5] Hastings, A. The Art of Analog Layout. Prentice Hall, 2001.

[6] Nguyen, C. T.-C. and Howe, R.T. "An Integrated CMOS Micromechanical Resonator High-Q Oscillator," *IEEE Journal of Solid State Circuits, Vol. 34, No 4*. April 1999.

[7] MOSIS Parametric Test Results. (n.d.) Retrieved November 20, 2002, from MOSIS web site: http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-abn/t29v-params.txt

[8] Clark, W. W. "Vibration Control in State-Switched Piezoelectric Materials," *Journal of Intelligent Material Systems and Structures, Vol. 11, No 4*. April 2000.

[9] Sedra, A.S and Smith, K.C. Microelectronic Circuits. Oxford University Press, 1998.

[10] Cambell, S. A. The Science and Engineering of Microelectronic Fabrication. Oxford University Press, 2001.

[11] Lee, S.S and White, R.M. "Self-Excited Piezoelectric Cantilever Oscillators," *The 8th International Conference on Solid-State Sensors and Actuators and Eurosensors IX, Vol. 1*, June 1995.