AN ANALYSIS OF ANTENNAS AND THE EFFECT OF PROXIMATE ELEMENTS AND CONDUCTORS

by

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When designing and implementing energy harvesting devices, additional unanticipated energy may be harvested, dissipated or lost due to interference involving proximate elements on the Printed Circuit Board (PCB) or Integrated Circuit (IC). These components can be PCB or IC traces, planes or discrete circuit components. This alters a designer's expectations as to how much energy should be harvested. Empirical analysis can be used to quantify the energy added or subtracted by proximate elements. In this thesis, the Active Remote Sensor (ARS) PCB is modified a number of times to provide enough variations to compare each section's contribution to the overall energy harvested. The differences in harvested energy will provide future designers with a better sense of layout in order to reduce or harness, this effect. Additionally, the number and arrangement of antenna and voltage doublers are modified to see which configuration(s) work most effectively.

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1.0 INTRODUCTION

1.1 INTRODUCTION TO THE STATEMENT OF THE PROBLEM

The primary purpose of this thesis is to document an empirical investigation of the effects of proximate circuit conductors and devices on the performance of an energy harvesting circuit in Radio Frequency IDentification (RFID) systems. For background information on RFID and energy harvesting, refer to Appendix A.

Because of the extensive experience with the Active Remote Sensing (ARS) device, the investigation will be restricted to the ARS antennas and circuitry used in the thermal sensing device. However, from a practical standpoint, a single load resistor of 1 KΩ will replace the thermal function circuitry.

The intent here is to show the effect of the conductors for the antenna and the proximate circuitry. In order to compare and evaluate the alternative configurations, a single figure of merit will be used to rank performance and facilitate comparisons among alternatives.

The purpose here is to perform an empirical analysis based on a combinatorics approach to the proximate object effects as opposed to a strictly analytical analysis.

During the course of this research, it will be necessary to construct, test and evaluate each of the test devices. It will also be necessary to design a plan for conducting the research analysis in such manner as to further test and evaluate the individual devices.

1.2 STATEMENT OF THE PROBLEM

The purpose of the research is to:

1. Establish a method to measure the effects on reception by various proximate (near) elements of the whole circuit.
2. Use the method to determine which PCB and IC traces, in addition to soldered components, cause interference (either constructive or destructive).
3. Evaluate the results to observe performance deviations from standard theoretical expectations.
4. Develop design rules gained from this analysis to aid in future design.

1.3 TESTING STRATEGY

There are ten steps involved in the experiment. First the ARS and IR interface PCBs must be designed, fabricated and populated. Then, verification of populated components is conducted to test functionality. Next, several types of measurements are used to supplement initial energy harvesting results. One additional board, board 6, has an independent set of populating tests to see if soldered components are of any effect. Next, ground planes and circuit traces are scraped off to monitor effects on the circuit. Data analysis is done in two sets. The first set is plotted data analysis. The second set is a Boolean analysis of the plotted tables. The Boolean analysis can be compared to see which segments commonly influence each circuit. The summarized set of steps:

Step 1: Modify and Fabricate PCBs
Step 2: Populate PCBs
Step 3: Verify Components and Static Resistance
Step 4: Measure Energy Harvested with no Modifications
Step 5: Measure AC Swing at Charge Pump interface for Verification
Step 6: Measure DC Output of each Doubler for Verification

Step 7: Test Influence from Soldered Components (6 B_{COMP} Experiment)
Step 8: Remove Traces and Ground Planes to Measure Changes
Step 9: Analyze Data from Steps 4, 7 and 8
Step 10: Convert Data to Boolean Expressions to see What Works Best

2.0 PRINTED CIRCUIT BOARD SPECIFICATIONS

In order to characterize what circuit segments contribute to the interference, parts of the circuit need to be isolated and tested against a specifically differentiated device in order to quantify each area's influence. This section begins with an overview of the original PCBs and then goes on to describe the modifications to each PCB.

2.1 THE ORIGINAL ACTIVE REMOTE SENSING PRINTED CIRCUIT BOARD

This circuit illustrated in Figure 1 is easiest analyzed in sections. There are three main sections that will be discussed: the antennas, the thermal circuitry and the power measuring Light Emitting Diodes (LEDs). This device will sense and transmit a temperature measurement a distance of 6-8 feet with a 5.5-watt source and an antenna gain of about 6.

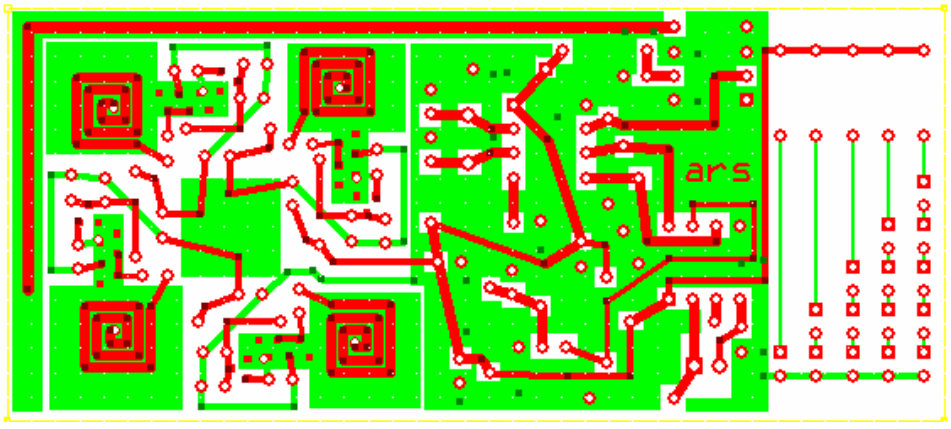

Figure 1: Original ARS board

2.1.1 Antennas and Voltage Doublers

There are four antennas and four voltage doublers in this part of the circuit. The output of each antenna feeds into the input of each voltage doubler, respectively. The positive and negative terminals of this system are identified in Figure 2.

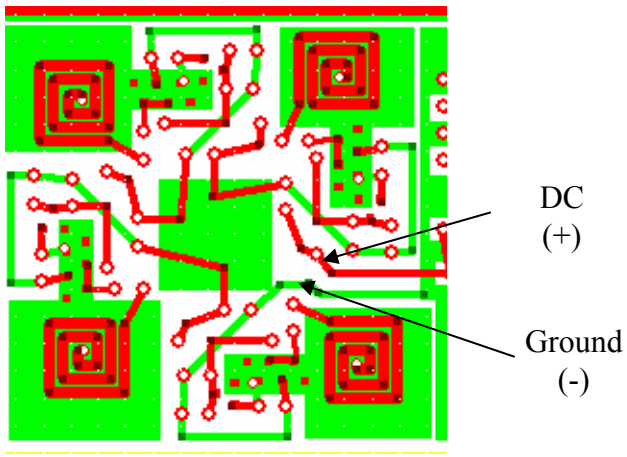

Figure 2: ARS board Antennas and Voltage Doublers

The schematic of the voltage doubler/antenna combination is shown in Figure 3. As can be seen, two forward biased diodes and one reverse biased diode are used as well as 4 capacitors, an inductor and a load resistor. The output capacitor on the right of the circuit is used to create a larger series voltage when combined with the other 3 voltage doublers as shown in Figure 4. This entire circuit can be simplified into a battery, where the positive terminal is the cathode of the right most capacitor, and the anode is ground, or the anode of the right most capacitor.

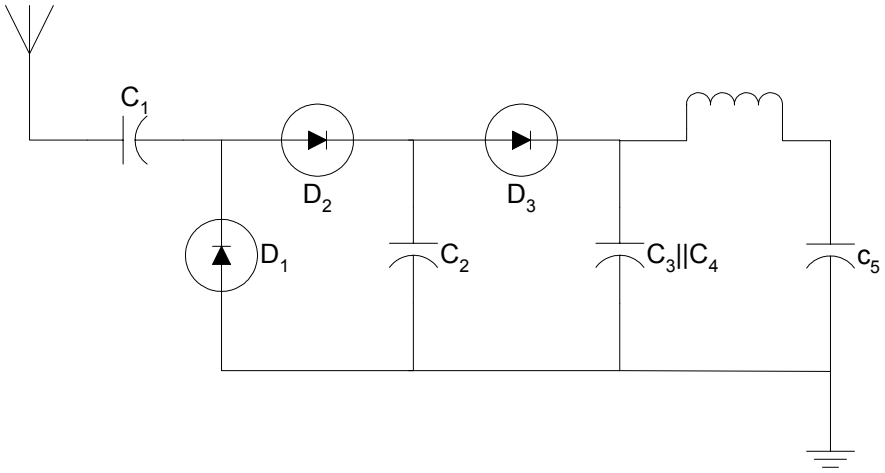

Figure 3: Antenna and Voltage Doubler Schematic

The individual output capacitors of each instance of the antenna/doubler combination are connected in series in the full implementation of a four-antenna system as shown in Figure 4.

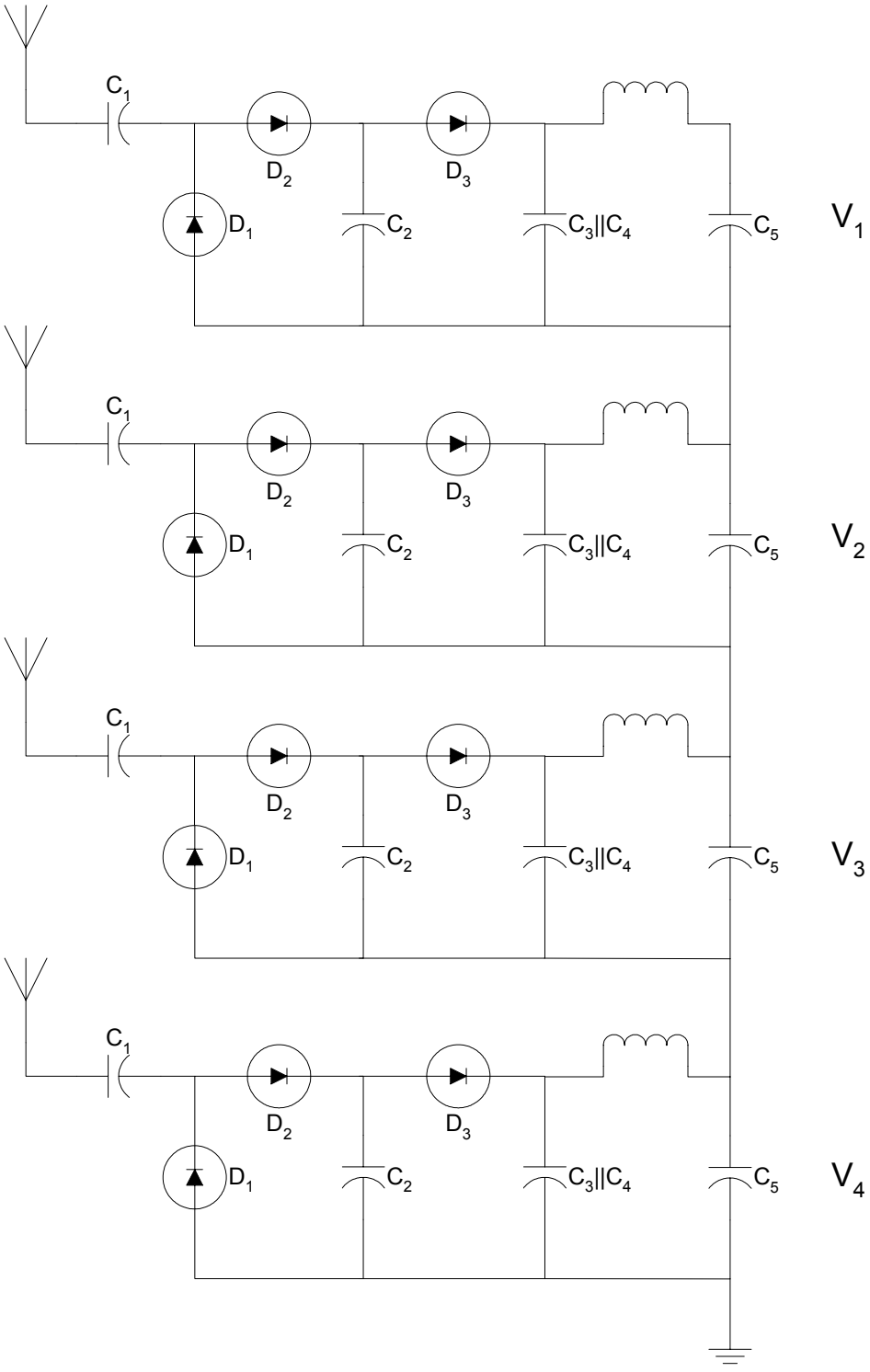

Figure 4: Four Series Connected Voltage Doublers

To show how the series connected voltage doublers and antennas behave, the analogous model of the battery greatly simplifies the analysis. As can be seen in Figure 5, when these four batteries are connected in series, the total voltage across these batteries is the sum of the four separate voltages. This of course is the ideal case, where smaller voltage drops across PCB traces are ignored, and assuming all four energy sources are operating properly.

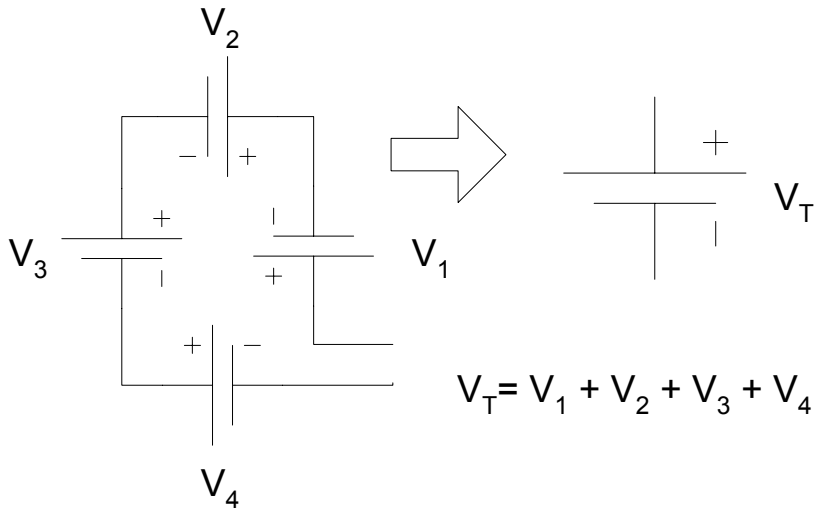

Figure 5: Equivalent Battery Model

2.1.2 Thermal Circuitry

The functional thermal sensing section of the original ARS PCB's schematic and layout are shown in Figure 6 and Figure 7, respectively. This circuit consists of several DIPS and passive circuit elements. This section is somewhat arbitrary in the current analysis due to the fact that it will not be used as intended in this experiment. The inclusion of this circuitry is to illustrate how the presence of the metal traces affects the energy harvesting process. In the fully implemented ARS, the components might also have an effect. However, the potential inconsistency in fully implemented test boards is likely to have more variations than the components.

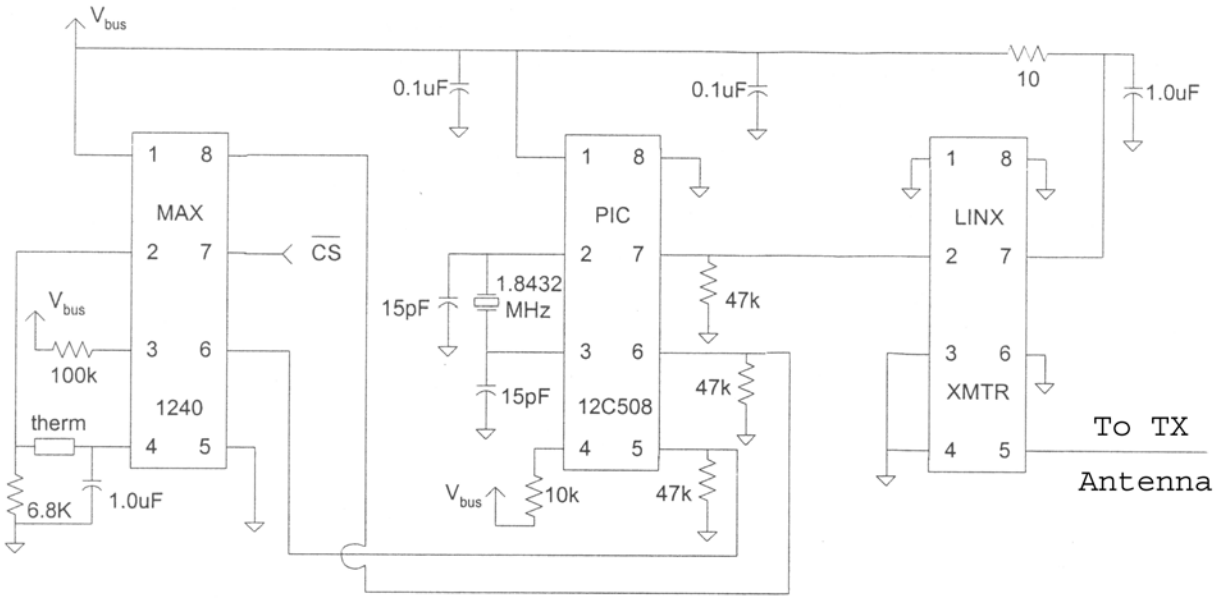

Figure 6: Thermal Circuit Schematic

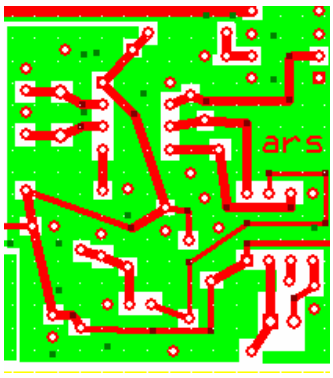

Figure 7: Thermal Circuit Layout

The output of the voltage doublers is what is referred to as V_{BUS} in this schematic. V_{BUS} powers the entire circuit, including the MAX A/D converter, PIC chip and the Linx Transmitter.

The MAX A/D converter maps a binary value to the analog signal detected from the thermistor. The PIC chip formats that result and adds in a device number and a checksum. The Linx Transmitter sends the data across another RF link. The transmitting antenna is connected to pin 5 of the Linx transmitter and is approximately a quarter wavelength of 433 MHz.

2.1.3 LED Power Meter

This section, shown in Figure 8, is also not being included in these experiments, but it is worth mentioning due to the fact that it is the former method of measuring energy harvested. The DC output of the voltage doublers feeds directly into this section, illuminating an increasing number of rows of LEDs when more energy is harvested. While this is a good idea of how to visualize the power received, there are no precise indications of power received, leading the viewer to potentially record an inaccurate power reading such as 'three rows are dimly illuminated' or 'two rows are brightly illuminated'. Table 1 lists power readings using this LED method. [4]

Table 1: Table of Energy Harvested vs. LED Illumination

Column	Voltage (V)	Power (mW)
1	1.8	0.09
2	3.5	4.03
3	5.3	18.23
4	7	46.4
5	8.8	97.42
All	12	252

Figure 8: LED Power Meter

2.2 ORIGINAL IR PCB

This circuit and PCB will be used instead of the power LEDs to measure energy harvested. There are two major sections of this circuit and PCB: the antenna/voltage doubler, and the infrared interface. Figure 9 shows the layout configuration of this board.

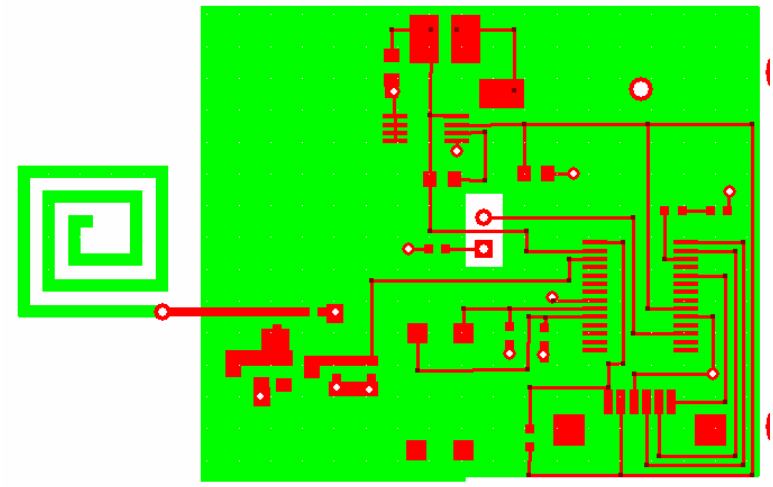

Figure 9: Original IR Interface PCB

2.2.1 Antenna and Voltage Doubler

These two familiar circuit elements function exactly like their counterparts on the original ARS PCB. The major difference here, shown in Figure 10, is that only one pair of antenna and voltage doubler is used, eliminating the need for the previously mentioned right-most capacitor to chain with other doublers. This circuit is included for completeness, but is not actually a part of the research in this thesis.

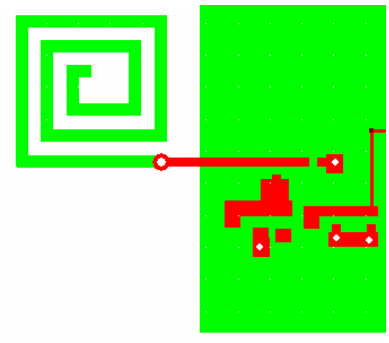

Figure 10: IR Interface Antenna and Voltage Doubler

2.2.2 IR Interface

The infrared interface contains a few items of interest. Figure 11 illustrates the DC input from the voltage doubler. The DC input is fed into an analog to digital converter (ADC) on a Programmable Interrupt Controller (PIC). This alone improves the accuracy over the guesswork involved in determining how many LEDs are illuminated and how bright they may be.

The other significant part of this section is the infrared interface. This takes the digital value in the PIC and adds a header before it transmits the information over an infrared link to another device, such as a PC, to decode the serial transmission and record the data. Figure 12 gives the schematic for the IR interface.

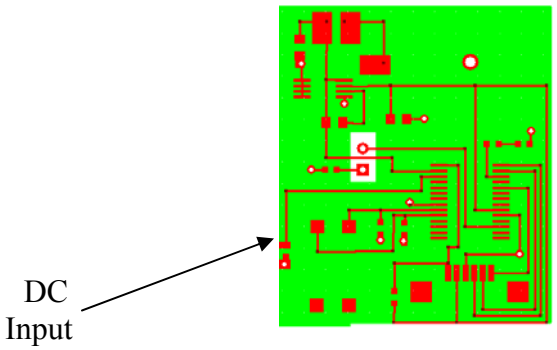

Figure 11: IR Interface Circuitry

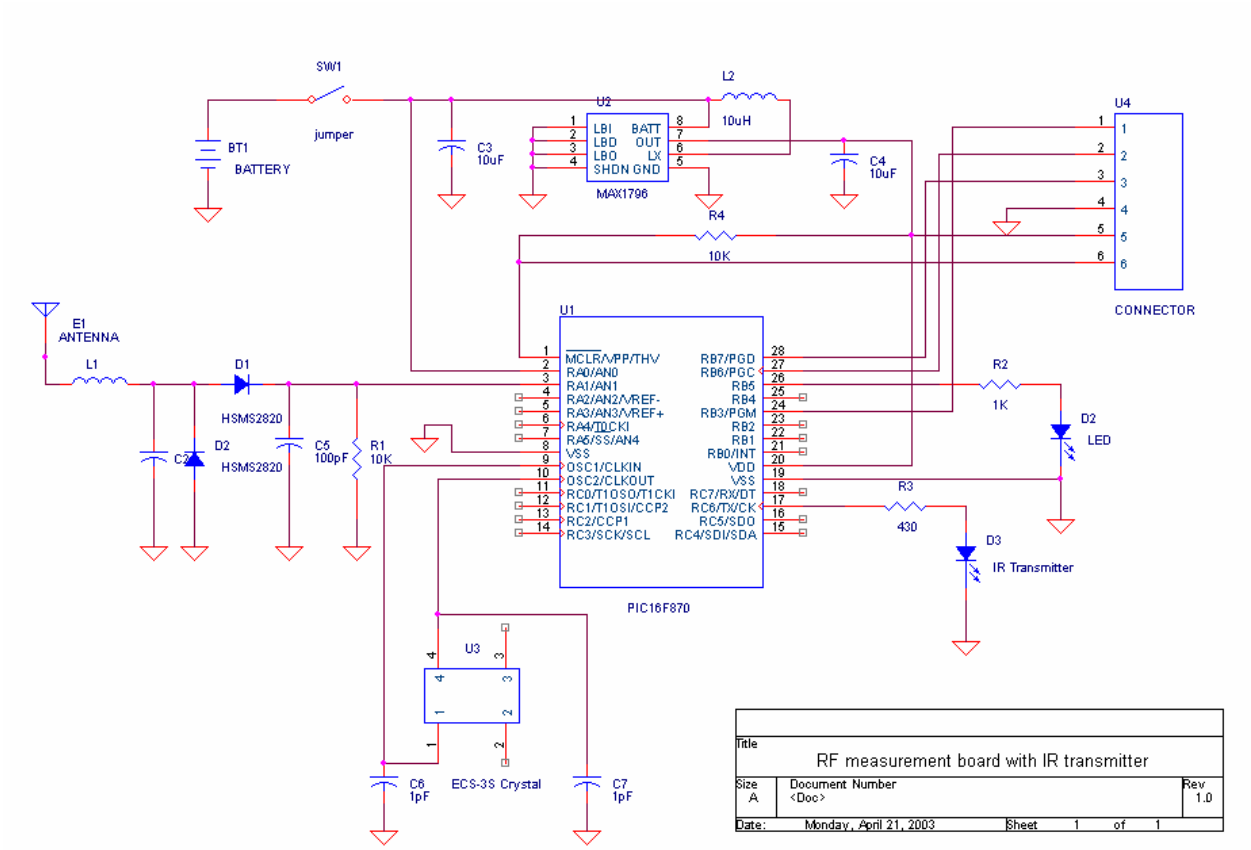

Figure 12: IR Interface Schematic

3.0 TEST STRATEGY AND MODIFICATIONS

As mentioned before, circuit modifications must be made in order to isolate each extraneous circuit element's contribution to the problem. Before the modification details are discussed, a few principles will need to be clarified in order to fully understand the circuit modifications.

3.1 ACTIVE REMOTE SENSOR

When altering four batteries in series, special attention must be paid to grounding and DC feeding issues. In Figure 13, batteries 1 and 4 are removed. As can be seen, the PCB layout now contains open circuits, leading to a non-grounded contact at the lowest non-negative potential of the circuit. This can be remedied by adding a trace to ground and to the DC output.

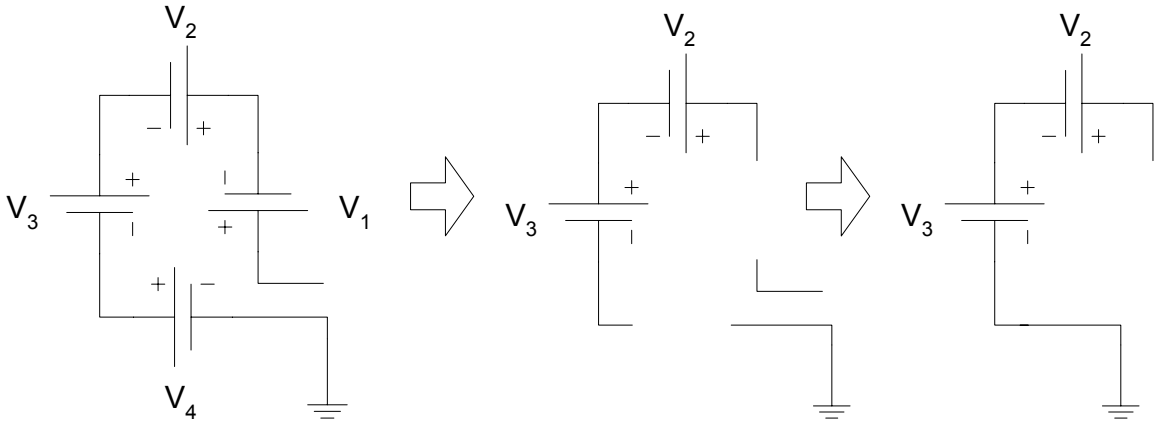

Figure 13: Illustration of Grounding and DC Feed modifications when altering the Circuit

The antennas and voltage doubler combinations are split up into four major sections: A, B, C and D. The thermal sensing circuit interconnections will be referred to as section E. Sections A and B are then split up in to A, A_{CKT}, B and B_{CKT}. The CKT subscript refers to the voltage doubler associated with said antenna. Table 2 maps the named circuit segment with its associate figure for visual clarification.

Table 2: Circuit Segment Identification

Circuit Segment	Figure #
A	14
A_{CKT}	15
B	16
B_{CKT}	17
C	18
D	19
E	20

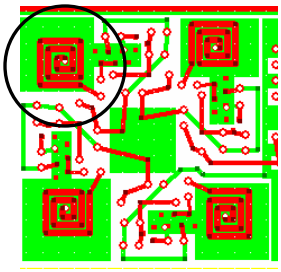

Figure 14: Circuit Subsection ‘A’

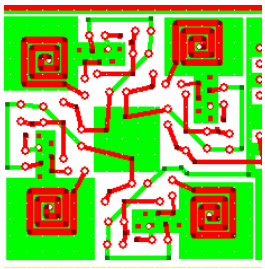

Figure 15: Circuit Subsection ‘A_{CKT}’

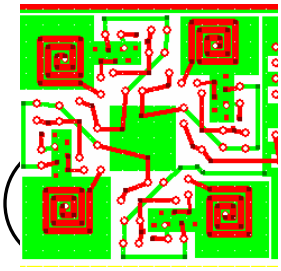

Figure 16: Circuit Subsection ‘B’

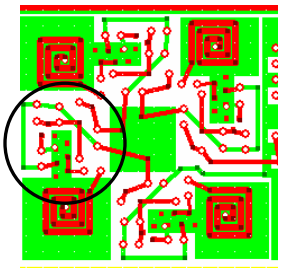

Figure 17: Circuit Subsection 'B_{CKT}'

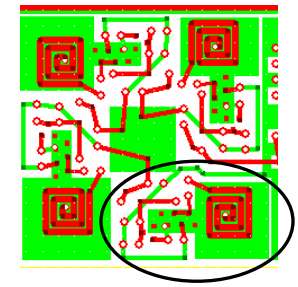

Figure 18: Circuit Subsection 'C'

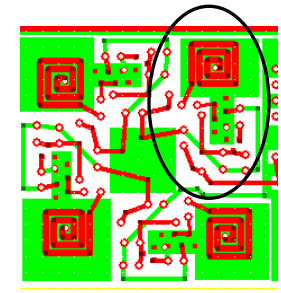

Figure 19: Circuit Subsection 'D'

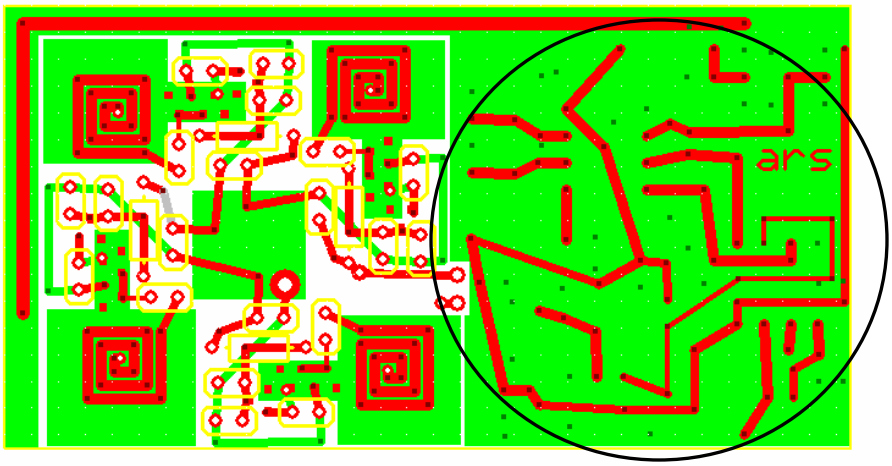

Figure 20: Circuit Subsection ‘E’

Now that the sections are identified, refer to Figure 21 to see the added contacts for a 2-pin ribbon header cable to connect to the wireless IR transmitter as well as new terminals for a load resistor to be placed between the DC output and ground. Those connections are necessary for the test measurement implementation. Based on the testing results, it appears this connection has little or no effect on the ARS energy harvesting performance.

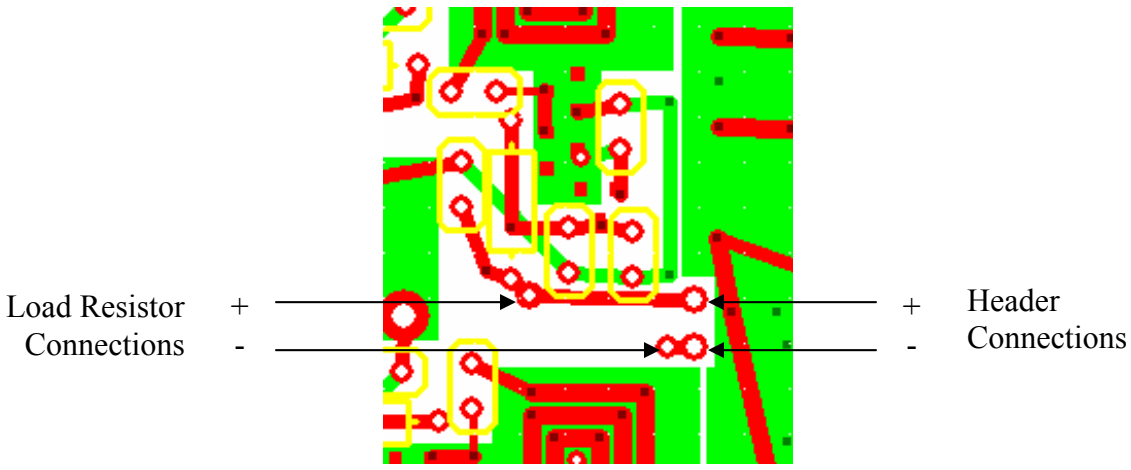

Figure 21: Header Modification for Ground and DC connections and new Load Resistor

Boolean expressions are used to designate what sections are omitted from or included in the circuit. These Boolean variables are listed in Table 3, and can be reviewed to see the variations and what figures to refer to for each variation. Appendix B contains actual photographs of the fabricated and populated PCBs.

Table 3: ARS PCB Modification Descriptor Table

ARS Variation	Boolean Representation	Figure #
1	A, A_{CKT}, B, B_{CKT}, C, D, E	20
2	A, A_{CKT}, B, B_{CKT}, C', D', E	22
3	A, A_{CKT}, B, B_{CKT}, C', D', E'	23
4	A, A_{CKT}, B', B'_{CKT}, C', D', E'	24
5	A, A_{CKT}, B, B'_{CKT}, C', D', E'	25
6	A, A^{*}_{CKT}, B', B_{CKT}, C', D', E'	26
7	A, A_{CKT}, B, B_{CKT}, C, D', E'	27
8	A, A_{CKT}, B, B_{CKT}, C', D, E'	28
9	A, A_{CKT}, B, B_{CKT}, C', D', E_{LEFT}	29

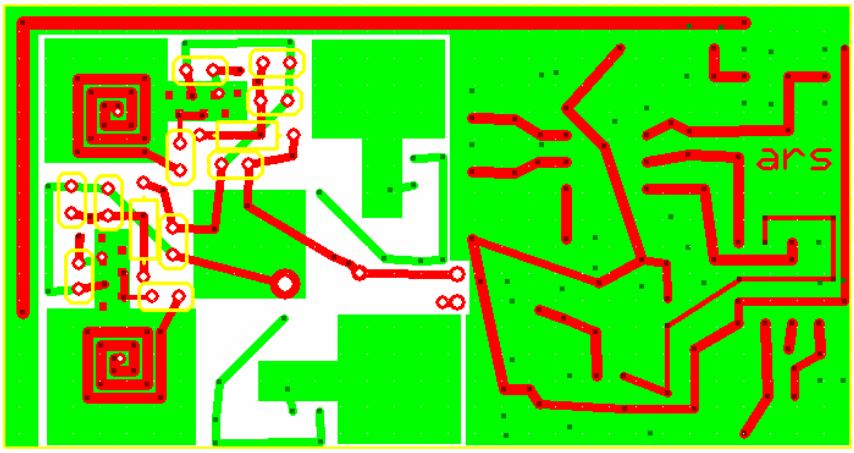

Figure 22: ARS Variation #2 - A, A_{CKT}, B, B_{CKT}, C', D', E

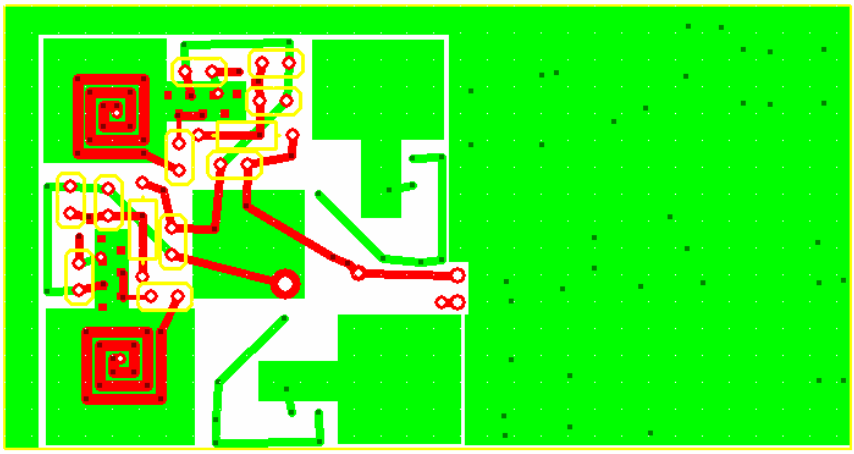

Figure 23: ARS Variation #3 - A, A_{CKT}, B, B_{CKT}, C', D', E'

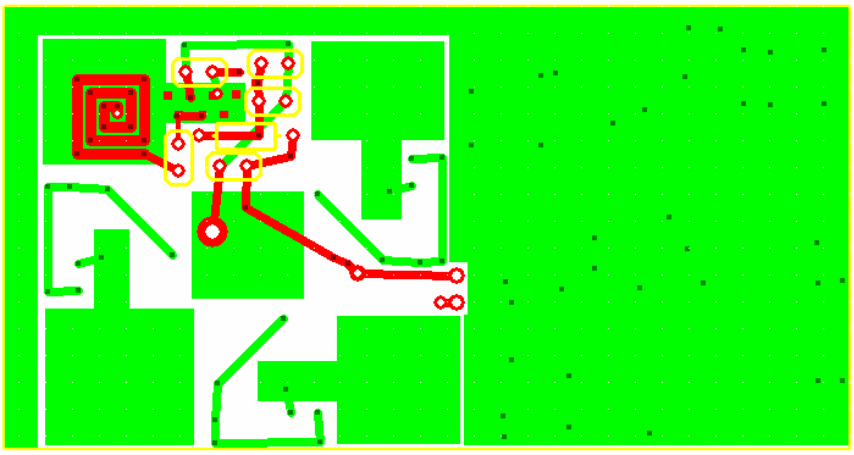

Figure 24: ARS Variation #4 - A', A'_{CKT}, B, B_{CKT}, C', D', E'

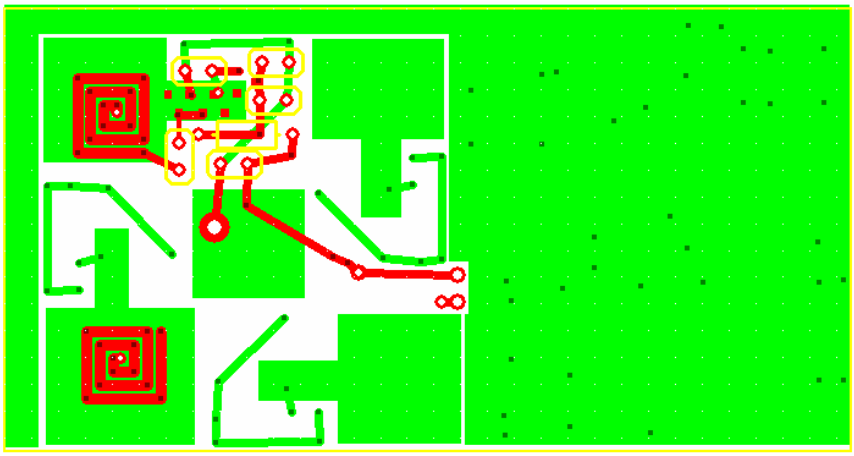

Figure 25: ARS Variation #5 - A, A'$_{CKT}$, B, B$_{CKT}$, C', D', E'

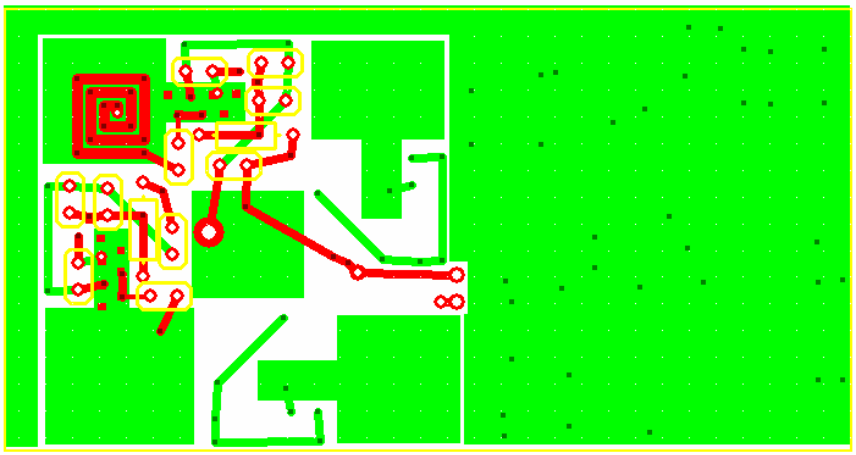

Figure 26: ARS Variation #6 - A', A$^{*}_{CKT}$, B, B$_{CKT}$, C', D', E'

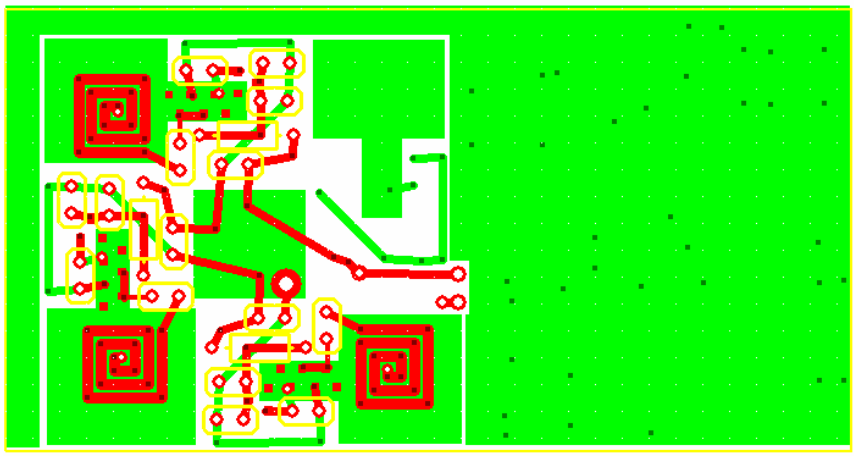

Figure 27: ARS Variation #7 - A, A_{CKT}, B, B_{CKT}, C, D', E'

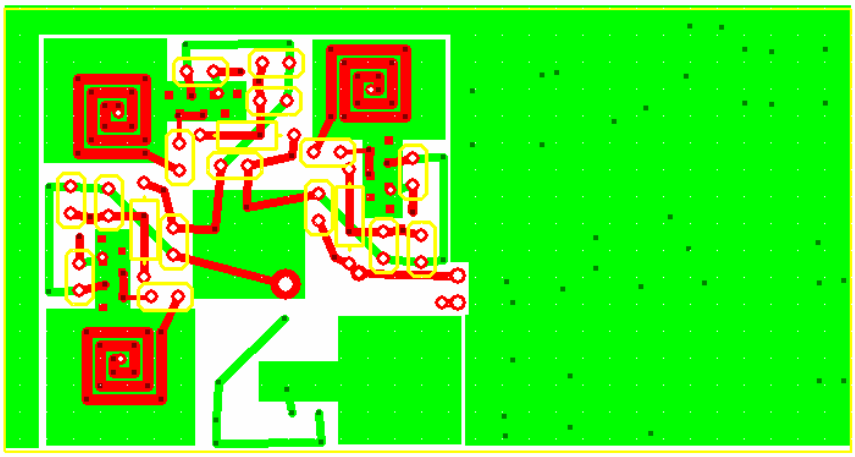

Figure 28: ARS Variation #8 - A, A_{CKT}, B, B_{CKT}, C', D, E'

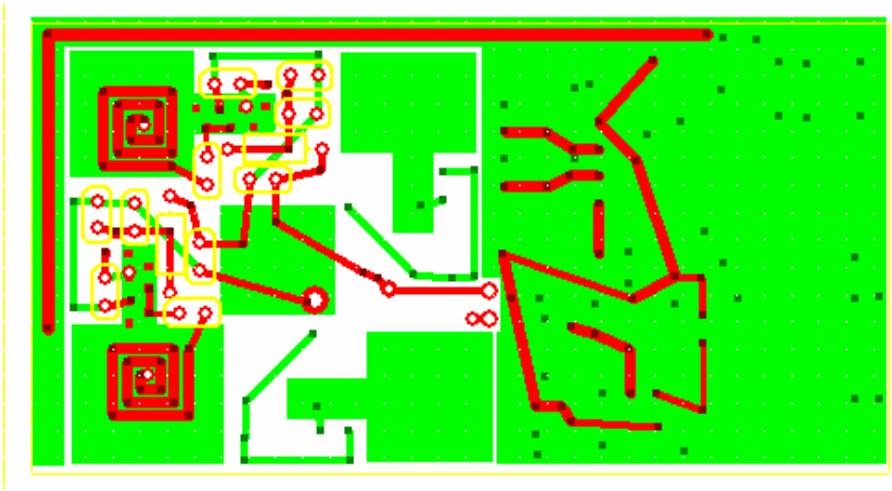

Figure 29: ARS Variation #9 - A, A_{CKT}, B, B_{CKT}, C', D', E_{LEFT}

3.2 INFRARED INTERFACE

On the infrared board, the DC feed from the included voltage doubler has been removed and replaced by the positive terminal of a 2-pin header. The negative terminal connects to the ground plane. This header is what makes the connection to the output of the modified ARS PCB. The whole modified board is shown in Figure 30 with a close up of the 2-pin ribbon header shown in Figure 31.

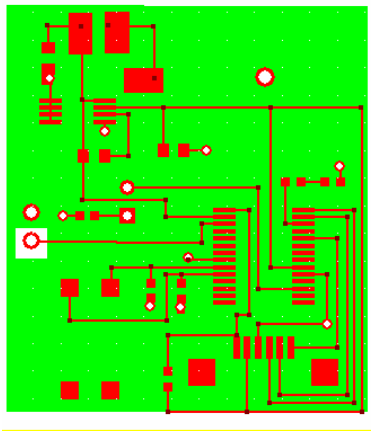

Figure 30: Modified IR Interface PCB

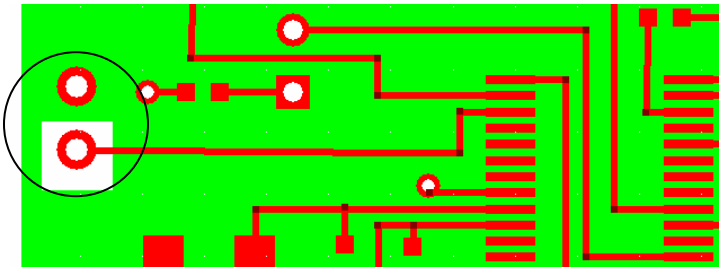

Figure 31: Close up of Header Modification for DC and Ground Connections

3.3 THE TEST CONFIGURATION

Figure 32 shows how the 2 PCB's connect together back to back and where they fit in the experimental setup, and Figure 33 shows the complete PCB submitted board for fabrication.

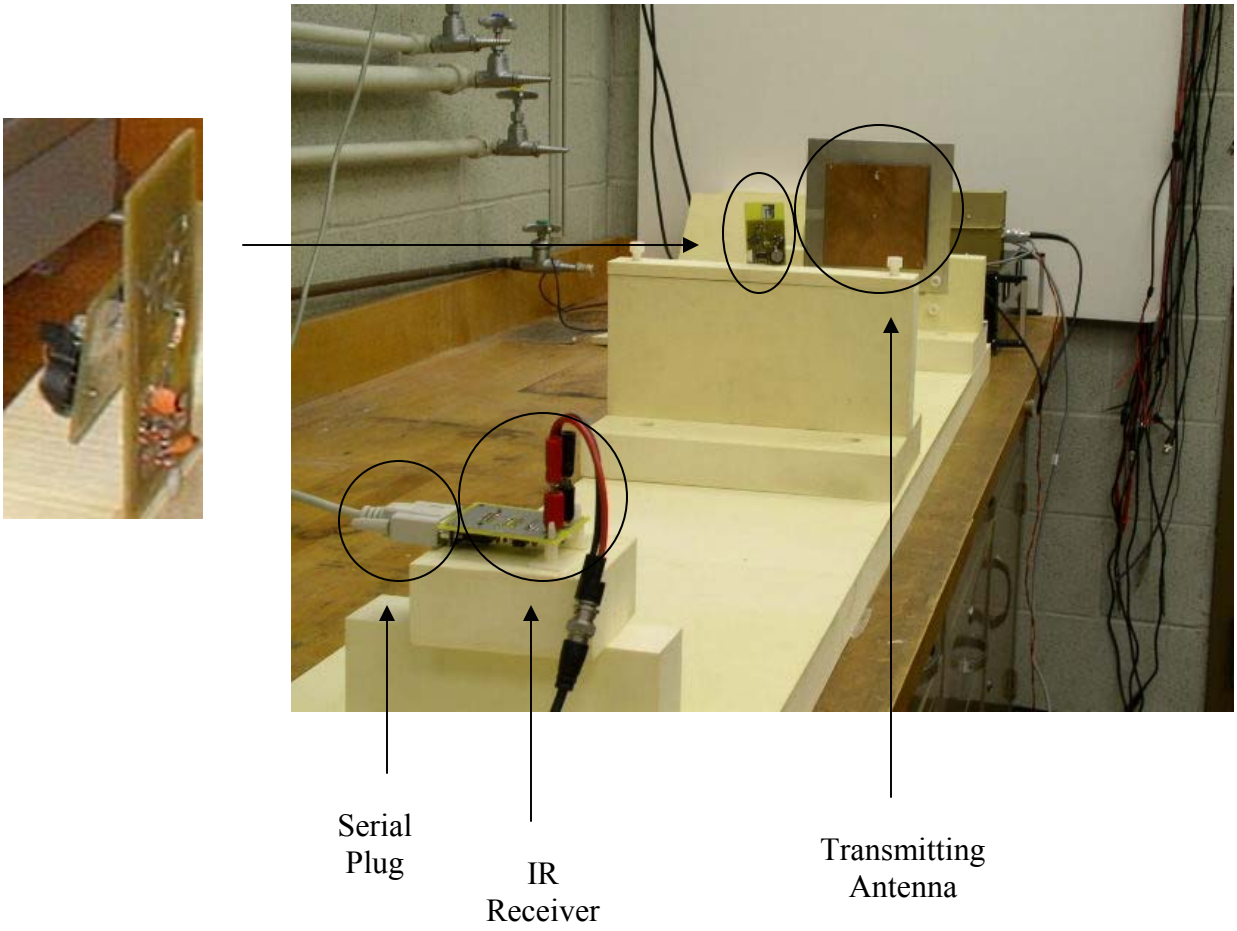

Figure 32: ARS and IR PCB's Physical Connection

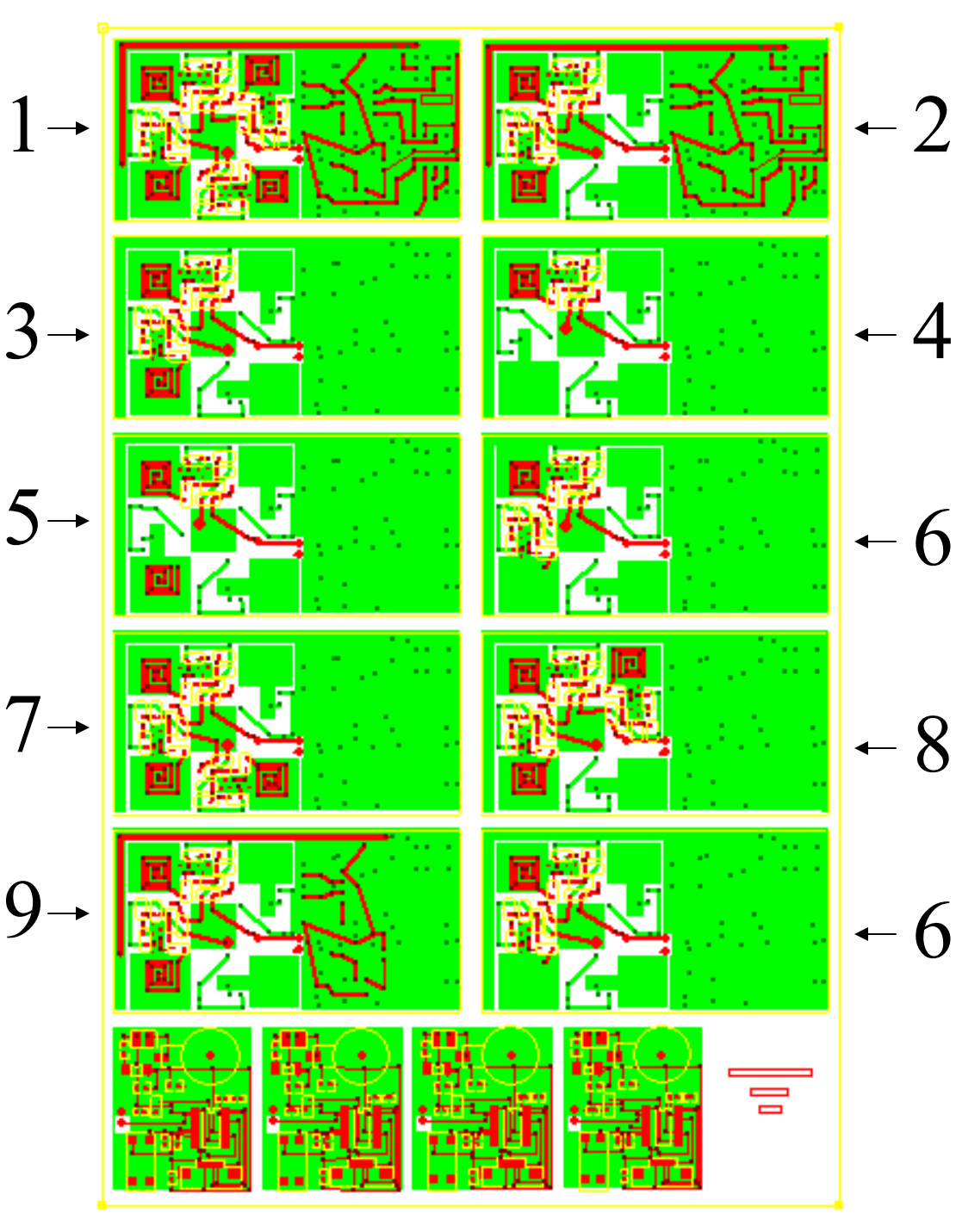

Figure 33: Entire set of PCB Test Modules

4.0 THE EXPERIMENTS

4.1 EXPERIMENTAL SETUP

For the actual experiments, three main components were used: the transmitter, the ARS/IR power sensing boards and the data acquisition unit. The transmitter is an RF signal generator. The RF signal is approximately 5.5 W at a frequency of 915 MHz that radiates from a linearly polarized patch antenna with directivity of around 6. The ARS board is connected to the IR interface board, which receives the harvested power and transmits the measurements, after doing a conversion to a digital quantity, via IR and adjusts on a sliding table as shown in Figure 34. The data acquisition unit receives the IR and transmits the measurements to a PC running a MATLAB program.

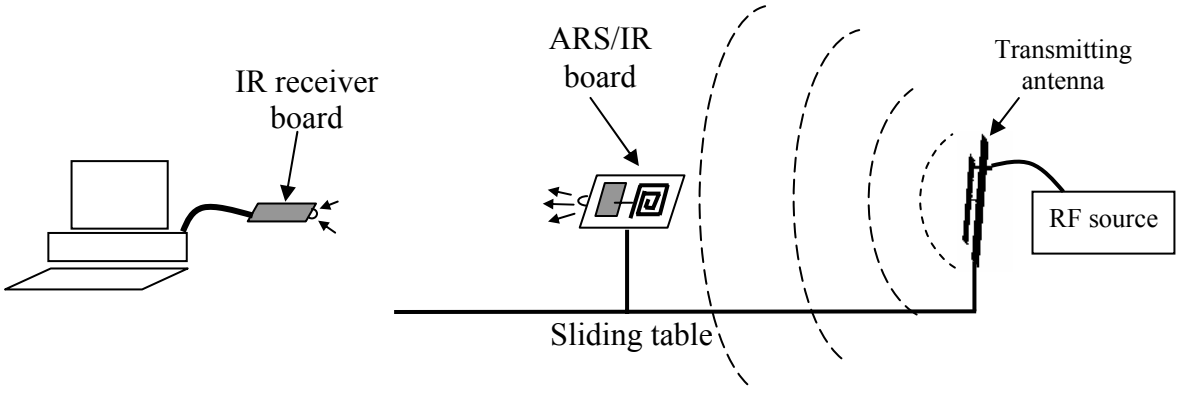

Figure 34: Illustration of Experiment Setup

The data acquisition on the PC is conducted with a MATLAB script called "Virtual Power Meter". This meter acquires data from the serial port and converts it into a milli-voltage (mV). Figure 35 shows the interface to the VPM while Figure 36 shows the graph that plots each sample.

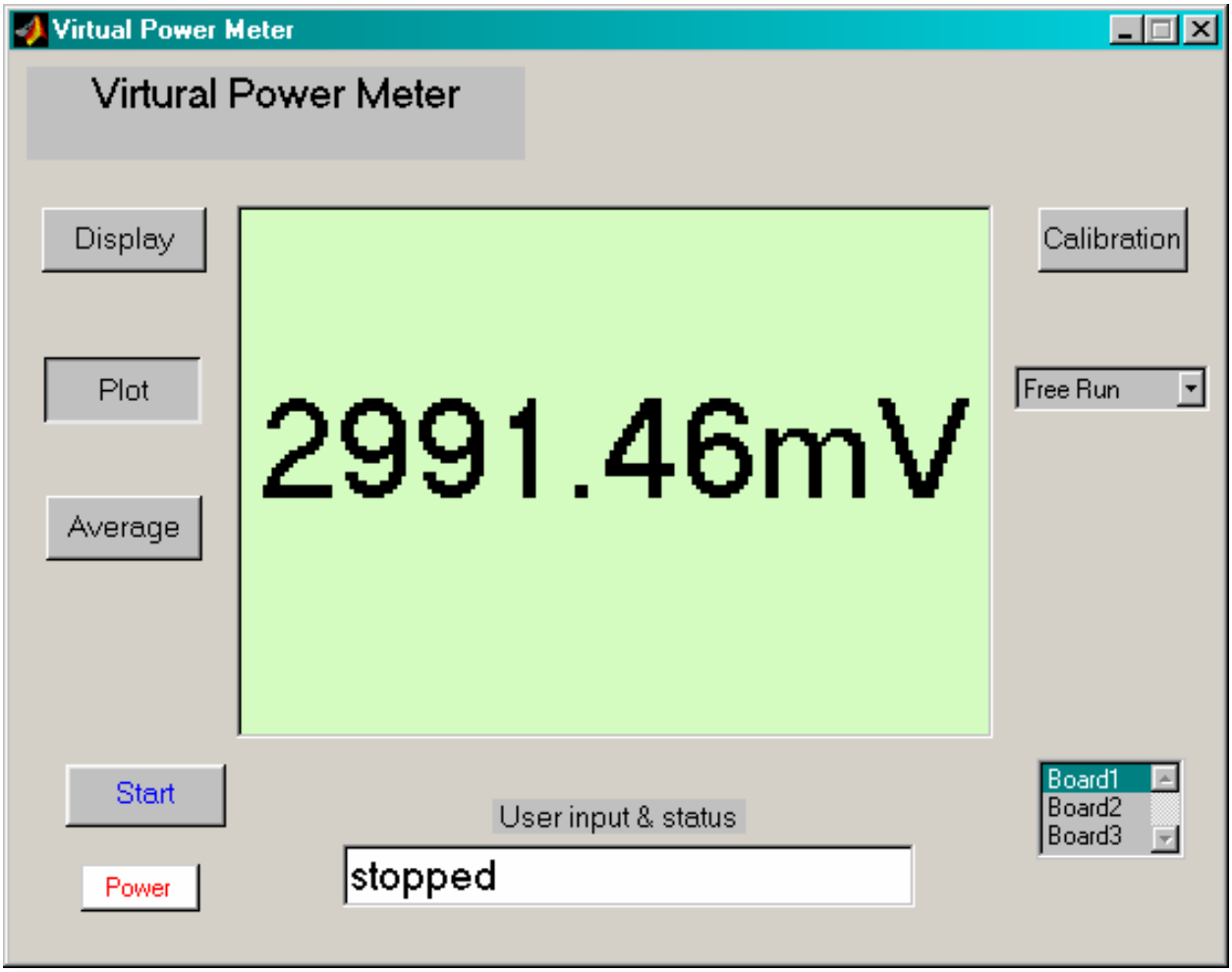

Figure 35: Virtual Power Meter Interface

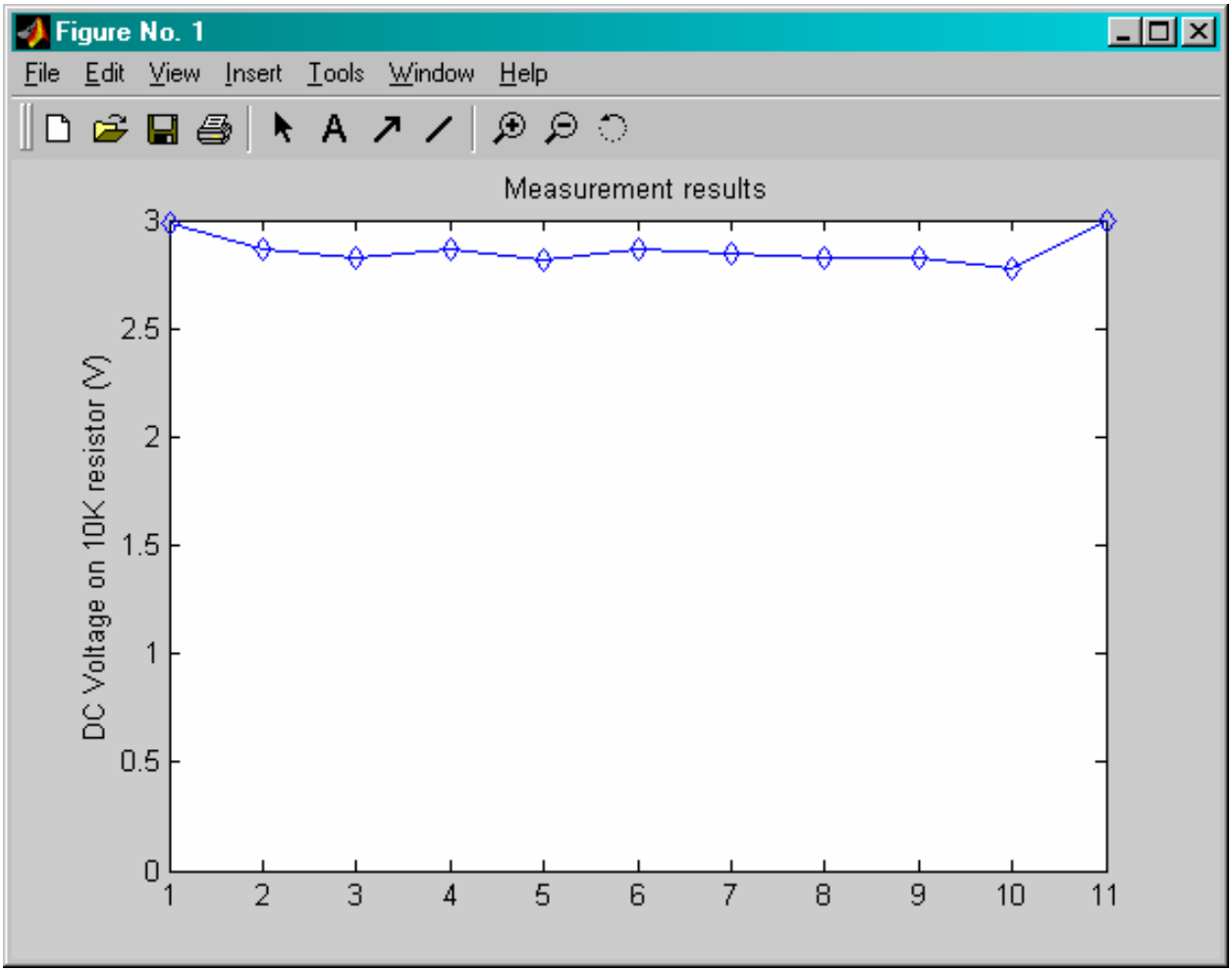

Figure 36: Sample Plotting on the VPM

The Virtual Power Meter script was written by Dr. Minhong Mi and was used in his dissertation. This uses the Graphical User Interface Development Environment (GUIDE) in MATLAB, which is not much different than other GUI development environments. This script was run on an HP Pavilion xf350, with a mobile AMD Athlon XP 1500 and 240 Megabytes of RAM. The serial link is an RS232 interface between the infrared receiver and the PC. This runs at a baud rate of 2400. The VPM collects all data in real time and not only plots the measurements, but also writes the values to a local file.

4.2 TESTING STRATEGIES

The nine populated ARS PCBs were each individually connected to the IR interface one at a time and initially tested at 3 distances - 70, 100, and 130cm. The purpose of doing this is to see how performance differs before any major modifications are made. This provided more insight as to how to modify the boards in the next phase of testing.

PCB variation #6 was involved in an additional experiment to measure influence from soldered components. The B_{CKT} subsection was populated one element at a time to illustrate any effects that soldered components had on the energy harvesting. The order for the populating is as follows: D1, D2, D3, C2, C3, C5, C1, L1, C4. The diodes were included first due to the low profile having little significant affect on the amounts of energy. The capacitors were next, excluding the output coupling capacitor that connects it to other voltage doublers. Finally, the inductor and the output capacitor were connected to see if it made any differences in measurements.

These experiments are also conducted without the ground plane behind the antennas.

> "A closely placed ground plane behind the antenna structure can lead to extraordinarily low radiation efficiency. Since the thickness of the PCB or the silicon wafer is usually fixed for a given process, it is very likely that the ground plane is not located at the proper position if we simply put it on the back of the board or the wafer. At the frequency of 915MHz, it is usually too close because the thickness of a normal PCB is on the order of 1mm to 2mm, which is less than $0.006\lambda_0$." [1]

The strategy for removing the traces and ground planes is illustrated in Table 4. The plan is to selectively remove sections one by one in order to obtain a differentiating result. The leading number in each equation represents the board number, and the other terms represent components removed. Other sequences of component removal may lead to different results. For example, if A_{GND} was removed first and the order of removal were reversed, results could vary. However, the total number of possible builds required and the potential variation in the fabrication would likely cause similar variations.

In each case, D_{GND} is removed first due to the assumption that since D_{ANT} is always a poor performer, removal of this specific ground plane can be expected to increase performance. C_{GND} is next, followed by B_{GND} and A_{GND}. The subsequent selection of ground removal after D_{GND} was chosen for reduced complexity in documentation and Boolean analysis. E_{LEFT} and E_{RIGHT} were saved for last due to the fact that board 9 retained all ground planes and was already missing E_{RIGHT}, and served as a reference for a 2-antenna system with intact ground planes. Board 1 and board 2 were evaluated with no antenna ground planes.

On board 1, the ground planes beneath the antennas were removed one at a time so that the cumulative effects of these ground planes could be seen piece by piece. Then the E_{RIGHT} section was removed to compare this 4-antenna setup with board 9, which has the same modified E region but with only 2 antennas. Board 2 had a similar strategy for ground plane removal, as well as the same modifications to the E region. Board 3 was left untouched because once the E region was removed from board 2 the two boards were identical. This provided a test of self-consistency. Board 4 again uses a similar ground plane removal. On board 5, B_{ANT} was removed to make it identical to board 4. Board 6 had a different series of tests to conduct so it was unmodified. Boards 7 and 8 had similar ground plane removal strategies. Board 9, which has always performed poorly up to this point, had the E region completely removed to measure this particular affect.

Table 4: Trace and Ground Removal Strategy

Board # - Traces Removed
1-D_{GND}
1-C_{GND}-D_{GND}
1-B_{GND}-C_{GND}-D_{GND}
1-A_{GND}-B_{GND}-C_{GND}-D_{GND}
1-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}
1-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}-E_{LEFT}
2-C_{GND}-D_{GND}
2-B_{GND}-C_{GND}-D_{GND}
2-A_{GND}-B_{GND}-C_{GND}-D_{GND}
2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}
2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}-E_{LEFT}
4-B_{GND}-C_{GND}-D_{GND}
4-A_{GND}-B_{GND}-C_{GND}-D_{GND}
5-B_{ANT}
7-A_{GND}-B_{GND}-D_{GND}
7-A_{GND}-B_{GND}-C_{GND}-D_{GND}
8-A_{GND}-B_{GND}-C_{GND}
8-A_{GND}-B_{GND}-C_{GND}-D_{GND}

On board 1, the ground planes beneath the antennas were removed one at a time so the cumulative effects of these ground planes could be seen one by one. Then the E_{RIGHT} section was removed to compare this 4-antenna setup with board 9, which has the same modified E region but with only two antennas. Board 2 had a similar strategy for ground plane removal, as well as the same modifications to the E region. Board 3 was left untouched because once the E region was removed from board 2, the two were identical. Board 4 again uses a similar ground plane removal strategy. On board 5, B_{ANT} was removed to make it identical to board 4. Board 6 had a different series of tests to conduct so it was unmodified. Boards 7 and 8 had similar ground plane removal strategies. Board 9, which has always performed poorly up to this point, had the E region completely removed to measure its affect.

These modifications were made in two separate sessions. The results do vary between sessions due to an imperfect setup of the testing facilities. Anything from an extra body in the room to a moved piece of equipment can affect the results. Due to the fact that anything can influence the measurement, multiple samples are gathered to improve accuracy. Because of this testing obstacle, all relevant measurements were repeated each time the experiments were conducted. Test results that appeared out of the ordinary were verified or dismissed by multiple measurements. Table 5 shows the first round of measurement scenarios and Table 6 shows the second.

Table 5: First Session of Measurements Scenarios

Board # - Traces Removed
4
4-B_{GND}-C_{GND}-D_{GND}
4-A_{GND}-B_{GND}-C_{GND}-D_{GND}
5
5-B_{ANT}
6
7
7-A_{GND}-C_{GND}-D_{GND}
10

Table 6: Second Session of Measurements Scenarios

Board # - Traces Removed
1
1-D_{GND}
1-C_{GND}-D_{GND}
1-B_{GND}-C_{GND}-D_{GND}
1-A_{GND}-B_{GND}-C_{GND}-D_{GND}
1-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}
1-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}-E_{LEFT}
2
2-C_{GND}-D_{GND}
2-B_{GND}-C_{GND}-D_{GND}
2-A_{GND}-B_{GND}-C_{GND}-D_{GND}
2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}
2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}-E_{LEFT}
7-A_{GND}-B_{GND}-D_{GND}
7-A_{GND}-B_{GND}-C_{GND}-D_{GND}
8
8-A_{GND}-B_{GND}-C_{GND}
8-A_{GND}-B_{GND}-C_{GND}-D_{GND}
9

5.0 RESULTS

5.1 VERIFICATION MEASUREMENTS

In order to accurately test these boards, a strategy was developed that involved different levels of verification. Components that were soldered to the board were measured and verified as shown in Table 7. This verification process is an integral part of determining whether or not the boards will work in the first place. Capacitors are measured in micro-Farads (μF) and diodes are measured by their turn-on voltage (V_{TO}) and are expressed in Volts (V). Since inductors are short circuits to DC voltages, it was not possible to measure them with the Radio Shack Digital Multi-meter that was used.

Table 7: Verification Measurements

		c1 (μF)	c2 (μF)	c3 || c5 (μF)	c4 (μF)	d1 (V)	d2 (V)	d3 (V)
1	**a**	1.033	1.069	2.769	2.768	0.275	0.275	0.275
	b	1.032	1.058	2.793	2.789	0.275	0.275	0.275
	c	1.027	1.005	2.81	2.812	0.275	0.275	0.275
	d	1.048	1.074	2.8	2.813	0.275	0.275	0.275
2	**a**	1.005	1.008	1.936	1.936	0.275	0.275	0.275
		0.972	0.958	1.979	1.979	0.275	0.275	0.275
3	**a**	1.021	0.991	1.982	1.982	0.275	0.275	0.275
	b	0.978	0.938	1.941	1.941	0.275	0.275	0.275
4	**a**	1.01	0.984	2.035	2.035	0.275	0.275	0.275
5	**a**	1.04	0.99	1.979	1.977	0.275	0.275	0.275
6	**a**	1.063	0.963	1.999	1.999	0.275	0.275	0.275
7	**a**	1.04	1.054	3.098	3.098	0.275	0.275	0.275
	b	0.983	1.059	3.126	3.13	0.275	0.275	0.275
	d	1.062	1.093	3.156	3.113	0.275	0.275	0.275
8	**a**	1.014	1.044	3.199	3.138	0.275	0.275	0.275
	b	1.026	1.074	3.102	3.102	0.275	0.275	0.275
	c	1.024	1.038	3.114	3.114	0.275	0.275	0.275
9	**a**	1.053	1.056	2.102	2.097	0.275	0.275	0.275
	b	1.044	1.032	2.108	2.108	0.275	0.275	0.275

When the ratio between the voltage across a circuit and current through a circuit is formed, the measurement is called static resistance and is used here to compare the DC impedance of each circuit. This is useful to see variations in soldered components between test modules. Static resistances were measured on the antenna/doubler circuits and are shown in Table 8 and plotted in Figure 37. These measurements were measured from the beginning of the antenna to the output capacitor of each voltage doubler.

Table 8: Static Resistance Measurement Results

ARS		R_S (kΩ)
1	**a**	50.4
	b	50.3
	c	50.1
	d	50.3
2	**a**	50.4
	b	49.6
3	**a**	50.4
	b	50.0
4	**a**	50.6
5	**a**	50.9
6	**a**	50.8
7	**a**	51.2
	b	50.7
	d	50.3
8	**a**	51.2
	b	50.9
	c	50.9
9	**a**	51.2
	b	51.1

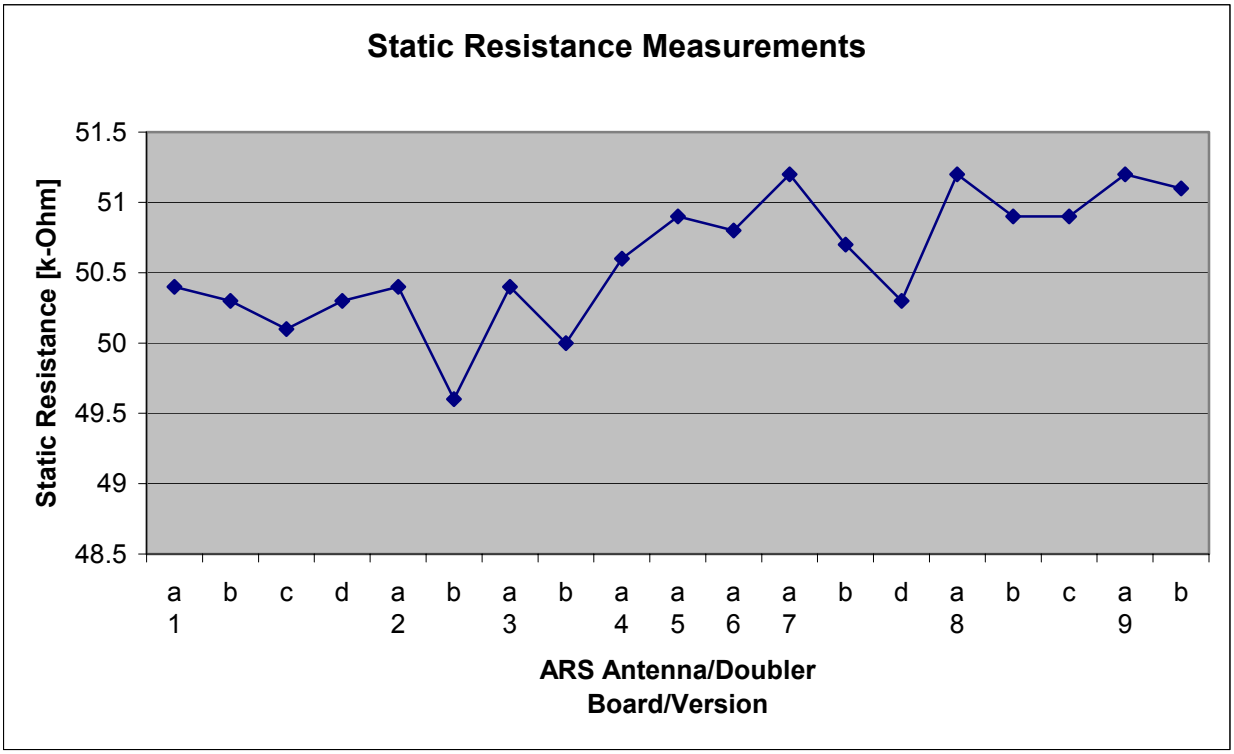

Figure 37: Plot of Static Resistance Measurements

5.2 POWER MEASUREMENTS

All measurements were conducted at three distances, 70, 100, and 130 cm. These distances are consistent with the distances set up by Dr. Mi in [1]. The difference here is that 70 cm was chosen as the closest distance due to the fact that the most efficient unmodified ARS variation barely reached 5 Volts at that distance. In a sense, this was a process of normalizing the performance to a 5 Volt margin.

5.2.1 Energy Harvesting Measurements with Virtual Power Meter

Board 1, despite having four antennas/doublers performs worse than most of the other variations that have fewer antennas. This was expected as described in Chad Emahizer's Master's thesis.

> "The single circuit was used only as a reference to compare with the other two circuits. The two-circuit series combination successfully produced more voltage than the single circuit. The placement of four tank circuits in series did not produce more voltage than the single circuit. This configuration produced negative voltage drops across some diodes due to the back biasing of those diodes. By placing four of these circuits in series and then shunting the first and fourth together by placing a load on the circuit combination caused the back biasing of the diodes. The four series circuit behaved as expected while unloaded, however I t did not perform well when loaded. Due to the negative voltages, the placement of four circuits in series was eliminated from further consideration." [2]

Board 1 was loaded in the case of the current thesis, so as expected; it did not function as designed. Board 9 was the worst performer, which was unexpected, due to the similar architecture of other boards that performed better. Board 8 performed worse than board 7, which was also unexpected. These results are listed in Table 9 and are plotted in Figure 38.

Table 9: Energy Harvesting Measurement Results

	0.7m [V]	1m [V]	1.3m [V]
1	4.33	0.757	0.3422
2	5	1.657	0.474
3	5	2.038	0.445
4	5	2.052	0.87
5	5	2.057	0.855
6	4.975	1.617	0.938
7	3.323	0.513	0.161
8	4.922	1.339	0.591
9	1.251	0.141	0.059

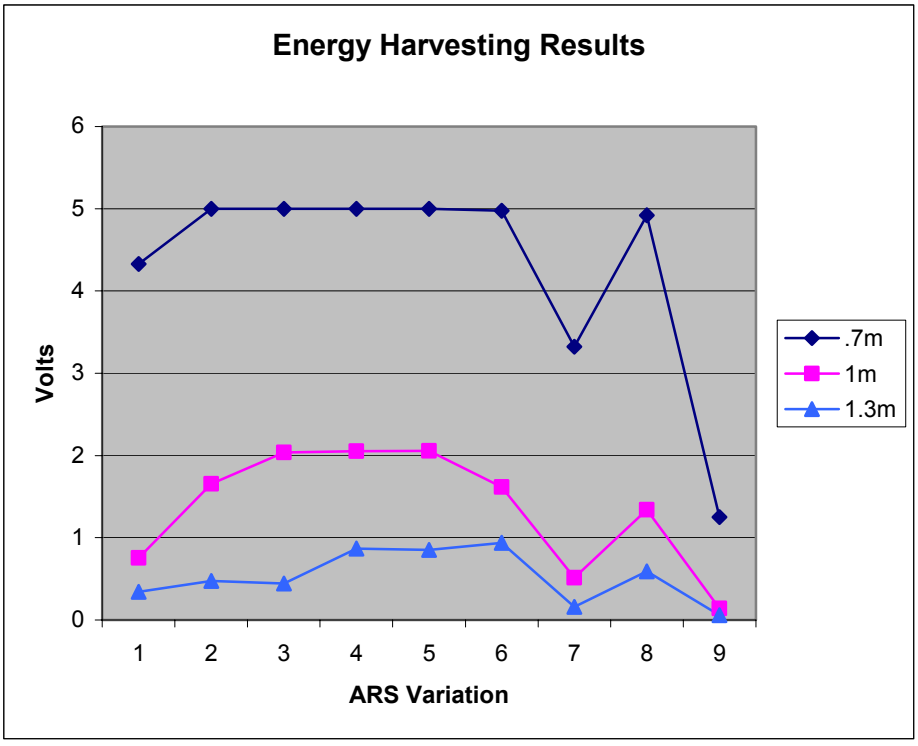

Figure 38: Plot of the Energy Harvesting Results

5.2.2 AC Swing at Charge Pump Interface

The next series of measurements involved taking the AC voltage at the output of the antenna and the input to the charge pumps. The measurements were done for every antenna/doubler combination by attaching a digital scope probe and using that signal for measurement. This connection is shown in Figure 39. The problem with this procedure is that the scope probes have different impedances than the impedance in the charge pump. So these results are strictly considered relative to other measurements of the same type. To measure these values, test points were soldered on the back of the boards. These measurements were very sensitive to movement (even at a few meters beyond the power sensing setup), so the results contain measurement variation at points. Duplicate measurements were taken to average out the variations. Three sets of measurements were taken at 1.3m and one set of measurements was taken at 0.7m. Table 10 shows these results and Figure 40 is a plot of them.

Figure 39: Close up of Scope Probe Connection

Table 10: Antenna/Charge Pump Interface Measurement Results

		0.7m [V]	1.3m Run 3 [V]	1.3m Run 2 [V]	1.3m Run 1 [V]
1	**a**	0.75	0.49	0.35	0.33
	b	1.05	0.44	0.28	0.405
	c	0.19	0.38	0.36	0.16
	d	0.6	0.3	0.29	0.125
2	**a**	0.975	0.62	0.36	0.205
	b	1.15	0.53	0.255	0.235
3	**a**	0.7	0.58	0.33	0.17
	b	1.15	0.66	0.23	0.25
4	**a**	0.74	0.5	0.265	0.305
5	**a**	0.9	0.63	0.315	0.305
6	**a**	0.85	0.51	0.295	0.305
7	**a**	0.53	0.37	0.335	0.295
	b	0.9	0.43	0.285	0.33
	d	0.45	0.29	0.29	0.11
8	**a**	0.69	0.43	0.305	0.355
	b	1.15	0.45	0.19	0.285
	c	0.19	0.31	0.37	0.145
9	**a**	0.2	0.42	0.365	0.165
	b	0.47	0.37	0.265	0.13

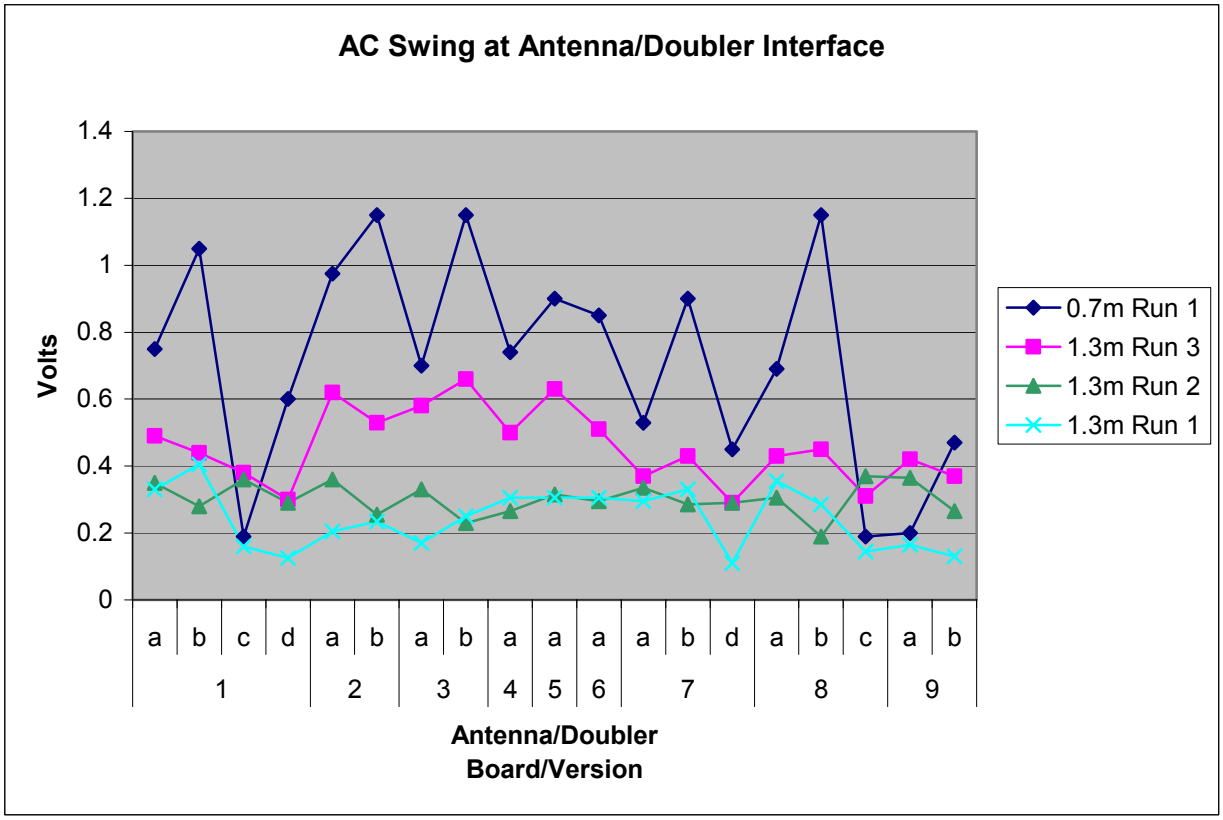

Figure 40: AC Measurement at Charge Pump Interface

This data supplements the measured values by illustrating the AC swing before any DC conversion is made. Keep in mind that the tests include board-to-board performance and section to section performance within each board. It can be seen that the worst performer, board 9 has a weak AC swing, verifying the poor performance. Board 8 outperformed board 7 in the post conversion measurements, and that can also be seen here. In general, antenna B has the most efficient reception at close range by tenths of a volt, but at long range, the differential is much smaller in the magnitude of hundredths of a volt. Antenna C performs extremely poorly at long ranges and slightly better at close ranges. Antenna D is slightly more efficient than antenna C, especially when both are present. The AC swing at the voltage doubler interface is a function of reception. If the reception is poor, the measurement of the AC swing will be small, leading to less potential energy to be harvested.

5.2.3 DC Measurements From Behind the Ground Plane

The next set of tests compares DC measurements taken manually with a scope from behind the ground plane using test points much like the ones used to measure the AC swing. Due to the difference in circuit impedance when a scope probe is connected, these values will not correspond to the measured values using the virtual power meter. Again, these measurements are going to be relative to each other as opposed to the VPM measurements.

According to the measurements in Table 11 that are plotted in Figure 41, similar trends can be observed that also occur in the AC measurements at the charge pump interface. Board 9 is still performing poorly. Board 8 is still performing more efficiently than board 7. Antenna D is still not very effective. All of these results also supplement the measurements taken from the VPM.

Table 11: DC Measurements from Behind the Ground Plane

		DC [V] @ 0.7 m
1	**a**	2.1
	b	1.95
	c	2.3
	d	0.44
2	**a**	0.81
	b	0.82
3	**a**	1.15
	b	1.13
4	**a**	1.85
5	**a**	1.9
6	**a**	1.45
7	**a**	0.95
	b	1.5
	d	0.3
8	**a**	1.67
	b	2.1
	c	2
9	**a**	0.1
	b	0

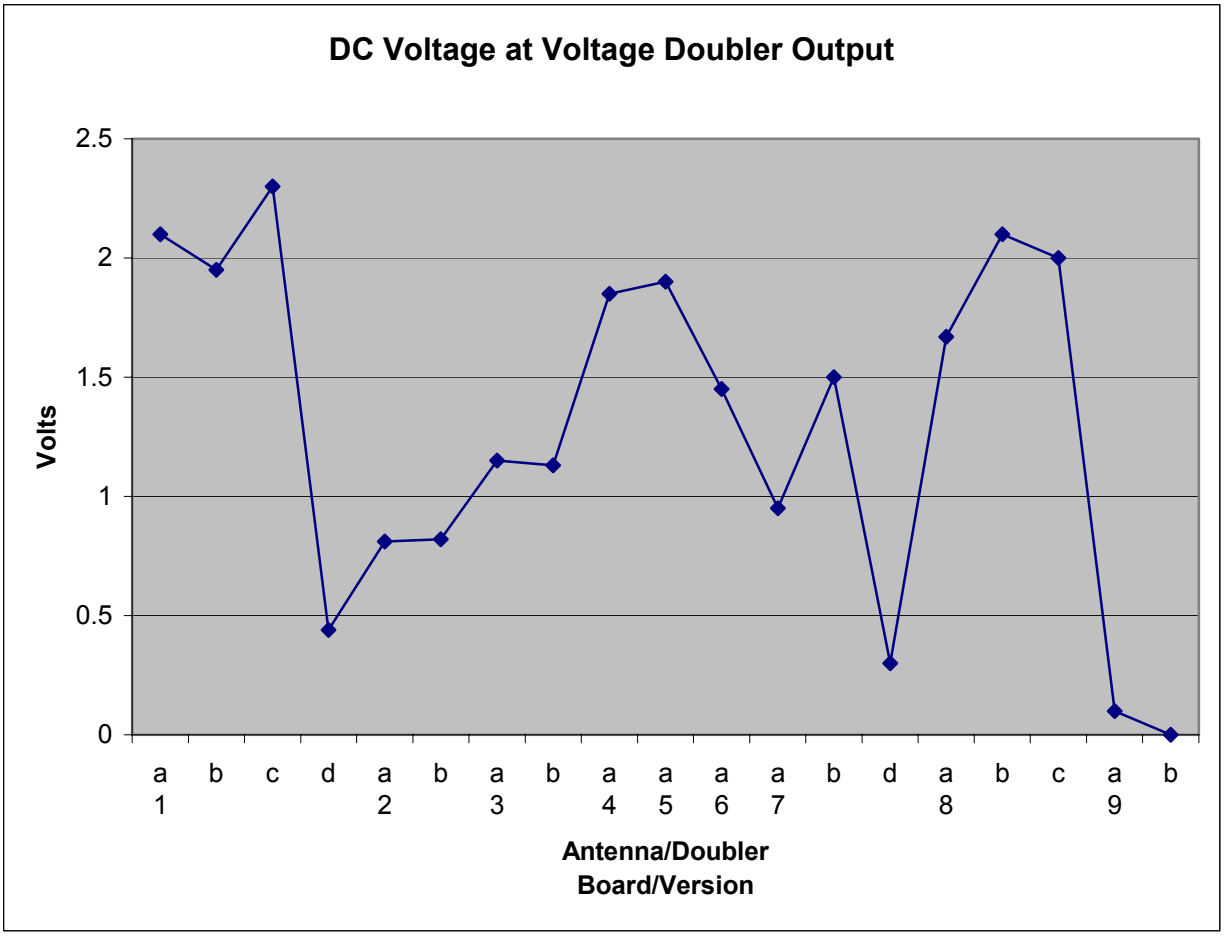

Figure 41: DC Measurement from behind the ground plane

5.2.4 Influence of Soldered Components

As mentioned before, board 6 underwent an independent series of tests to determine if actual soldered discrete components had any effect on the phenomenon being explored. At close range, none of these effects were manifested. At a mid range, it can be seen that the addition of D_3 reduced performance by a few tenths of a volt. The addition of the output capacitors C_3 and C_5 also reduced performance by nearly the same margin. At long range, there was a significant reduction in efficiency by an order of magnitude. So in general, as components were added, efficiency was reduced. Table 12 lists these results and Figure 42 is a plot of the results.

Table 12: Influence of Soldered Components

	0.7m [V]	1m [V]	1.3m [V]
D1	5	1.71	0.107
D2	5	1.64	0.107
D3	5	1.57	0.073
C1	5	1.78	0.029
C2	5	1.68	0.058
C3 || C5	5	1.43	0.005
C4	5	1.42	0.009
L1	5	1.45	0.009

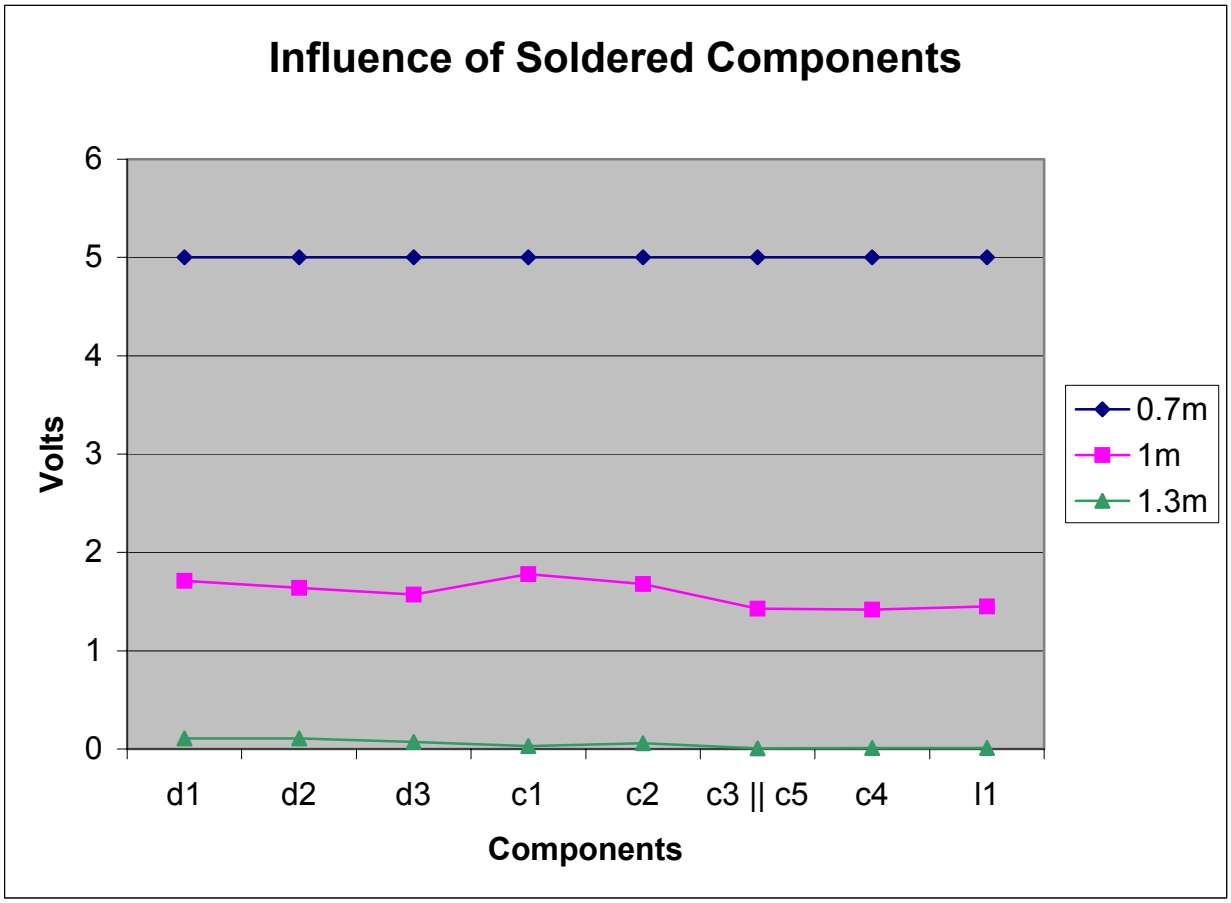

Figure 42: Influence of Soldered Components (Board 6)

5.2.5 Trace Removal Measurements

The next set of experiments involved removing metal traces and ground planes from the various PCBs. As mentioned before, this was done in 2 separate test sessions. The first session dealt with boards 4, 5, 7 and a duplicate of board 6 that will be referred to as board 10 from this point forward.

Table 13 lists the measurements and Figure 43 plots them. The first thing that can be noticed is that the performance of board 7 is drastically improved by removing the ground planes of all antennas in use. This test was performed at each distance. Board 5 exhibited a boost in performance with the removal of B_{ANT}, making it identical to Board 4 in appearance. Board 4 showed cumulative improvements with the removal of the consecutive ground planes. These experiments provided the initial results that are further illustrated in the next set of measurements.

Table 13: Second Round of Measurements

	0.7m [V]	1m [V]	1.3m [V]
4	5	1.749	0.107
4-B_{GND}-C_{GND}-D_{GND}	5	2.219	0.395
4--A_{GND}-B_{GND}-C_{GND}-D_{GND}	5	2.228	0.518
5	5	1.833	0.073
5-B_{ANT}	5	1.916	0.19
6	5	1.251	0.19
7	4.369	0.625	0.005
7-A_{GND}-C_{GND}-D_{GND}	5	1.525	0.073
10	5	1.515	0.083
10-B_{CKT}	5	1.974	0.317

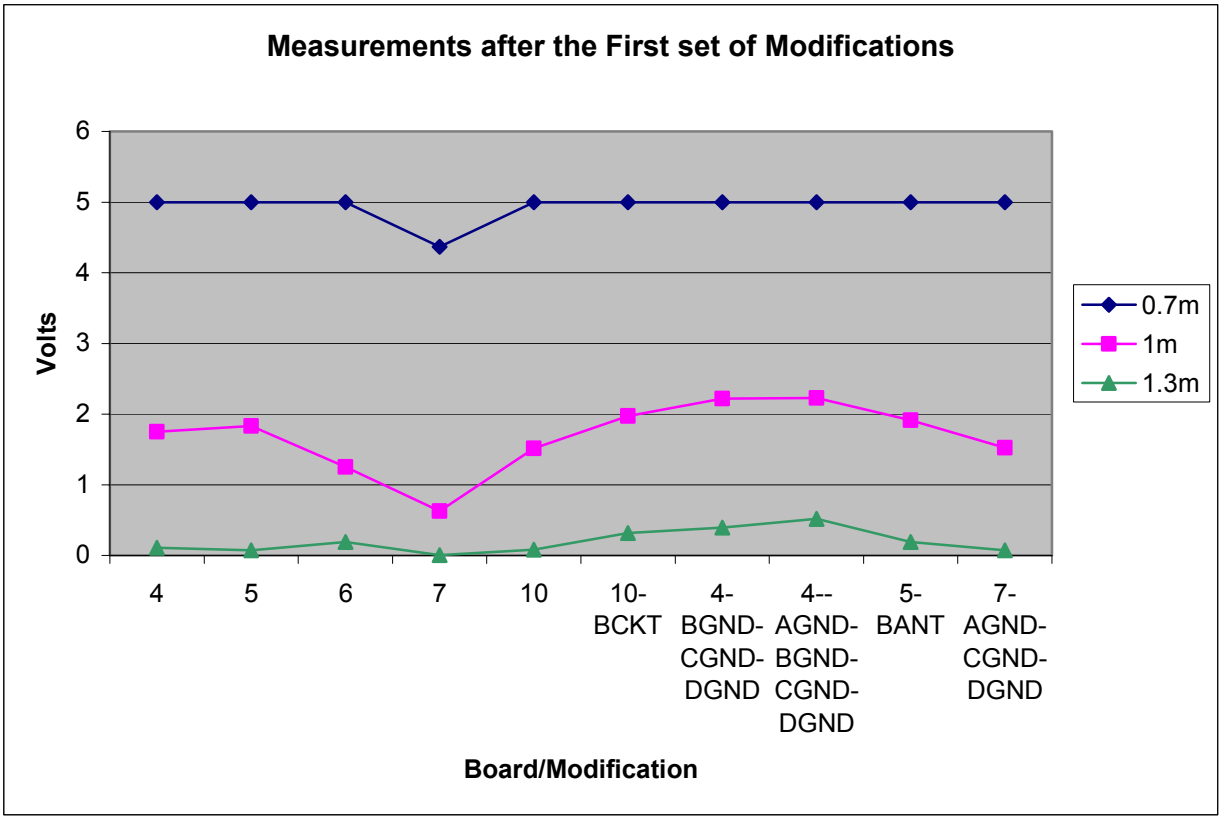

Figure 43: Results after the First Set of Modifications

The next sets of tests were all conducted in one session, but due to the relevance of each measurement, they are divided into 3 major sections. Since Board 1 was modified 6 times, and board 2 was modified 5 times, they each get separate tables and graphs. The remaining miscellaneous measurements are listed in Table 16. The three resulting sections are board 1, board 2 and the remaining board tests.

On board 1, as shown in Table 14 and plotted in Figure 44, removal of the antenna ground planes resulted in a gradual performance increase in the mid-distance range. When E_{RIGHT} was removed, the whole system suffered major losses. This configuration of the board resembles board 9 with four antenna/doublers instead of two. When E_{LEFT} was removed, performance of the system increased again, but did not reach the previous peaks of performance before the E region was modified. This signifies that there is a problem when E_{LEFT} is present without E_{RIGHT}.

Table 14: Board 1 Measurements

	0.7m [V]	1m [V]	1.3m [V]
1	4.65	0.78	0
1-D_{GND}	5	1.47	0.009
1-C_{GND}-D_{GND}	5	1.48	0.024
1-B_{GND}-C_{GND}-D_{GND}	5	1.5	0
1-A_{GND}-B_{GND}-C_{GND}-D_{GND}	5	1.64	0.004
1-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}	3.7	1.251	0
1-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}-E_{LEFT}	4.75	1.47	0.136

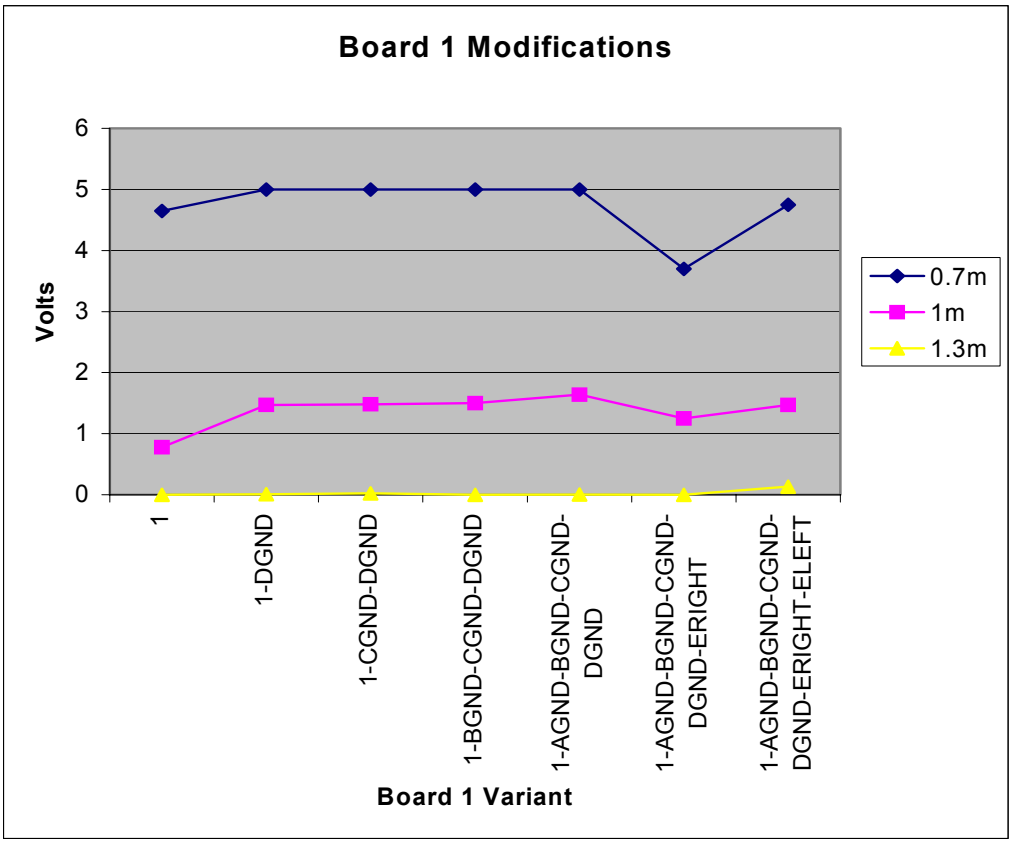

Figure 44: Board 1 Measurements

Board 2 underwent a similar series of trace removals as board 1 as listed in Table 15 and plotted in Figure 45. The only major difference here is that only two antennas are being used, so the first two steps for board 1 were combined into one step here. Removing C_{GND} and D_{GND} seemed to have little influence. However, when B_{GND} was removed, performance suffered drastically. This did not occur with board 1, in fact, this caused a small incremental improvement on board 1. Removing A_{GND} gave a small increase in operation at mid and long ranges, but the short range operation was still weak. As expected, removal of E_{RIGHT} made performance much worse, almost by an order of magnitude. When E_{LEFT} was removed, as expected, performance was restored to something comparable to the initial measurements.

Table 15: Board 2 Measurements

	0.7m [V]	**1m [V]**	**1.3m [V]**
2	5	1.52	0.474
2-C_{GND}-D_{GND}	5	1.749	0.459
2-B_{GND}-C_{GND}-D_{GND}	3.82	0.865	0.058
2-A_{GND}-B_{GND}-C_{GND}-D_{GND}	3.758	1.031	0.063
2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}	0.645	0.029	0
2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}-E_{LEFT}	5	1.657	0.234

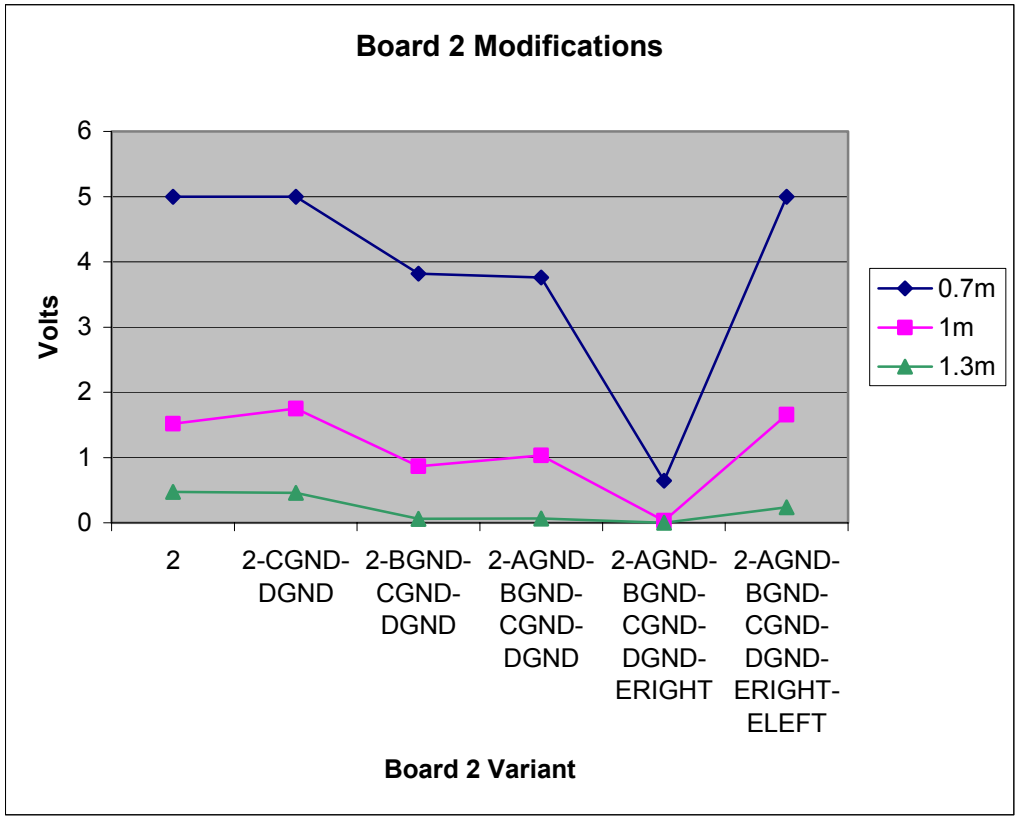

Figure 45: Board 2 Measurements

In this next set of measurements, board 7 underwent one more ground removal test with minimal change in functionality. Board 8 was tested similar to the test of board 7, also with minimal results. Board 9, which was thought to have been an anomaly despite component verification, was tested by removing the E_{LEFT} section, which hindered the performance of boards 1 and 2. This test proved that this section causes energy harvesting problems. Up to this point, after many rounds of testing, board 9 has never performed. Table 16 lists these results and Figure 46 plots them.

Table 16: Remaining Measurements

	0.7m [V]	1m [V]	1.3m [V]
7-A_{GND}-B_{GND}-D_{GND}	4.975	1.72	0.156
7-A_{GND}-B_{GND}-C_{GND}-D_{GND}	4.956	1.71	0.131
8	5	1.451	0.058
8-A_{GND}-B_{GND}-C_{GND}	4.99	1.613	0.102
8-A_{GND}-B_{GND}-C_{GND}-D_{GND}	4.922	1.564	0.97
9	1.065	0.156	0
9-E_{LEFT}	5	1.671	0.205

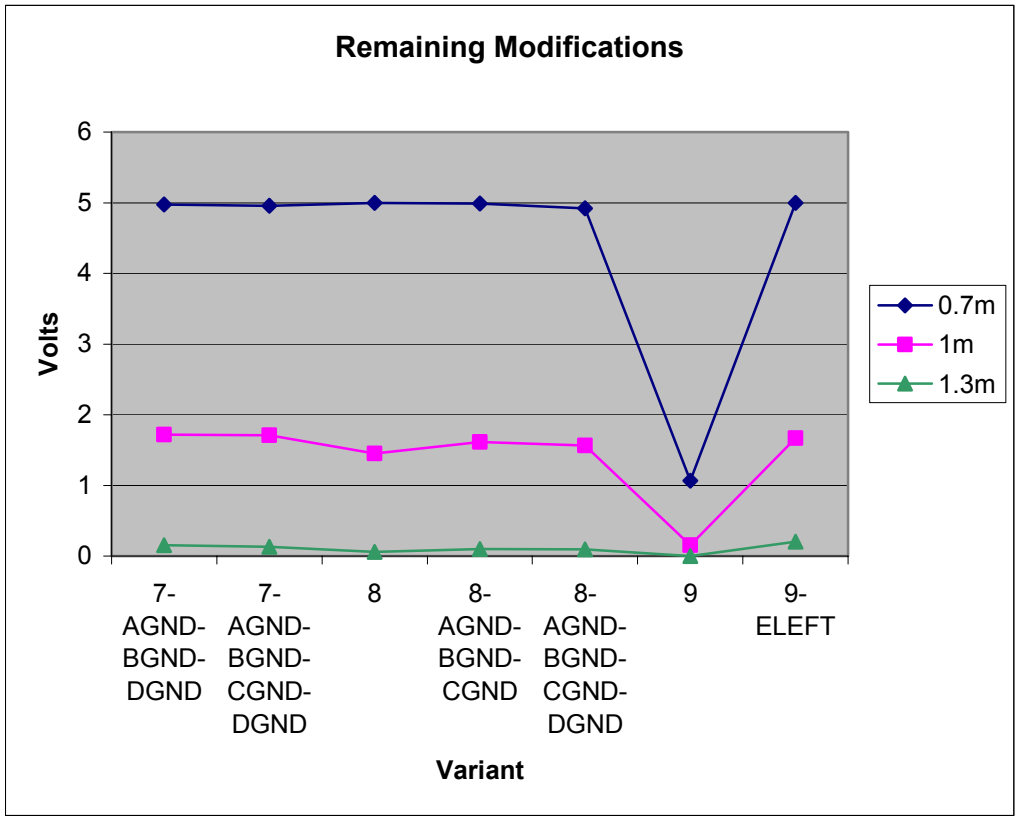

Figure 46: Remaining Measurements

6.0 BOOLEAN ANALYSIS

This section takes the data from section 4 and translates it all into Boolean expressions. There are two major parts to this analysis, before modifications (meaning trace and ground removal) and after modifications. Boolean variables differ between these two sub-sections because of the nature of the board modifications.

Each section of the unmodified boards has been previously defined in the Boolean expressions for ARS PCB modifications. Those expressions have been expanded into a larger vector or bitmap in the notation. Specifically, in addition to A and A_{CKT}, A_{COMP} designates soldered components; this only affects ARS variation 6. E is divided as E_{LEFT} and E_{RIGHT}. The bitmaps for each board are shown in Table 17. The usual "1/0" indicators are used to denote the sections of boards referenced by each situation. The intent is to define Boolean equations using these terms with additional Boolean criteria to describe performance.

Table 17: Bitmaps for each ARS Variation with no Modifications

ARS #	A_{ANT}	A_{COMP}	A_{CKT}	B_{ANT}	B_{COMP}	B_{CKT}	C_{ANT}	C_{COMP}	C_{CKT}	D_{ANT}	D_{COMP}	D_{CKT}	E_{LEFT}	E_{RIGHT}
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	1	0	0	0	0	0	0	1	1
3	1	1	1	1	1	1	0	0	0	0	0	0	0	0
4	1	1	1	0	0	0	0	0	0	0	0	0	0	0
5	1	1	1	1	0	0	0	0	0	0	0	0	0	0
6	1	1	1	1	0	1	0	0	0	0	0	0	0	0
7	1	1	1	1	1	1	0	0	0	1	1	1	0	0
8	1	1	1	1	1	1	1	1	1	0	0	0	0	0
9	1	1	1	1	1	1	0	0	0	0	0	0	1	0

Assuming all parts of subsection A are always present, and assuming all present CKT components are populated (except B_{COMP} on board 6), let B_A and B_C represent B_{ANT} and B_{CKT} (for more readable Boolean analysis) respectively and let C and D designate the circuit, antennas and components collectively. Figure 47 illustrates the new term grouping.

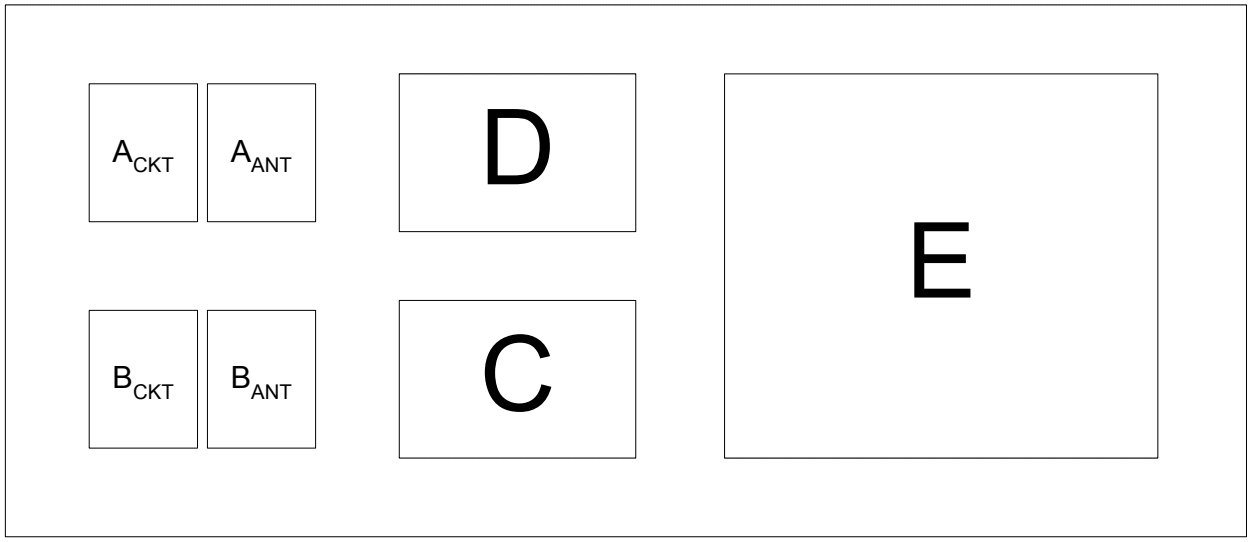

Figure 47: Illustration of New Variable Grouping

The low tolerance circuits provide a mechanism to use strict criteria with a minimal margin for error. The higher tolerance allows greater error, via inserting 'don't cares' (x), to allow more minterms in the Boolean expression. A minterm is a product term in which all variables appear exactly once, either complemented or uncomplemented. The data is divided between the low- and high tolerance circuits.

There are four tables in the next sections used to derive the Boolean algebra. The first table is the Boolean criteria. The criteria are applied to the measurements derived from this experiment. A threshold value is introduced to differentiate requirements for a 1 or 0. In the higher tolerance analysis, a second threshold is introduced to identify the criteria for a "don't care" (x). The truth table lists all relevant combinations of 1's and 0's (and x's), as well as the results. The table defines the minterms, simplifying the creation of a Karnaugh. The Karnaugh

map simplifies two-level Sum Of Products (SOP, or a sum of minterms) implementations [3]. The resulting Boolean expressions are simplified and compiled for comparison.

6.1 ENERGY HARVESTING MEASUREMENTS WITH NO MODIFICATIONS

6.1.1 Original 9 Boards: Low Tolerance

Table 18 defines criteria for a Boolean 1 or 0. There are four ones, on boards 2, 3, 4 and 5. Table 19 is the truth table. Table 20 is the K-map used to derive these values.

Table 18: Boolean Criteria

1	V = 5 V @ 70 cm
0	V < 5 V @ 70 cm

Table 19: Truth Table

Low Tolerance		0.7m	B_AB_CC	DE_LE_R
Boolean Value	**ARS #**	**[V]**		
0	**1**	4.33	111	111
1	**2**	5	110	011
1	**3**	5	110	000
1	**4**	5	000	000
1	**5**	5	100	000
0	**6**	4.975	010	000
0	**7**	3.323	110	100
0	**8**	4.922	111	000
0	**9**	1.251	110	010

Table 20: K-map

	B_AB_CC								
DE_LE_R									
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
	000	1	0	0	0	1	0	1	0
	001	0	0	0	0	0	0	0	0
	010	0	0	0	0	0	0	0	0
	011	0	0	0	0	0	0	1	0
	100	0	0	0	0	0	0	0	0
	101	0	0	0	0	0	0	0	0
	110	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0	0

A detailed explanation of 0-vectors will be explained in 6.1.3. Table 21 is a more readable K-map without the 0-vectors.

Table 21: Simplified Form of K-Map with Minterms Highlighted

	010	**110**	**100**	**000**
000	0	1	1	1
011	0	1	0	0

The Boolean expressions derived from these maps are given in (1)-(3):

$$\overline{B_C}\,\overline{C}\,\overline{D}\,\overline{E_L}\,\overline{E_R} + B_A B_C \overline{C}\,\overline{D}\,\overline{E_L}\,\overline{E_R} + B_A B_C \overline{C}\,\overline{D} E_L E_R \quad (1)$$

$$\overline{B_C}\,\overline{C}\,\overline{D}\,\overline{E_L}\,\overline{E_R} + B_A B_C \overline{C}\,\overline{D}(\overline{E_L}\,\overline{E_R} + E_L E_R) \quad (2)$$

$$\overline{B_C}\,\overline{C}\,\overline{D}\,\overline{E_L}\,\overline{E_R} + B_A B_C \overline{C}\,\overline{D}(\overline{E_L \oplus E_R}) \quad (3)$$

6.1.2 Original 9 Boards: Higher Tolerance

Table 22 defines the Boolean criteria for 0, 1, or don't care (x) in this segment.

Table 22: Boolean Criteria

1	V = 5 V @ 70 cm
0	V < 4.5 V @ 70 cm
x	4.5 V < V < 5 V @ 70 cm

The same assumptions are made, with the exception of included don't cares (x), representing marginal values. Table 23 is the truth table. Table 24 is the K-map.

Table 23: Truth Table

Higher Tolerance		0.7m	B_AB_CC	DE_LE_R
Boolean Value	**ARS #**	**[V]**		
0	**1**	4.33	111	111
1	**2**	5	110	011
1	**3**	5	110	000
1	**4**	5	000	000
1	**5**	5	100	000
x	**6**	4.975	010	000
0	**7**	3.323	110	100
x	**8**	4.922	111	000
0	**9**	1.251	110	010

Table 24: K-map

	B_AB_CC								
DE_LE_R									
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
	000	1	0	X	0	1	0	1	0
	001	0	0	0	0	0	0	0	0
	010	0	0	0	0	0	0	0	0
	011	0	0	0	0	0	0	1	0
	100	0	0	0	0	0	0	x	0
	101	0	0	0	0	0	0	0	0
	110	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0	0

Again, the highlighted minterms are illustrated in Table 25 on the reduced K-map.

Table 25: Simplified Form of K-Map with Minterms Highlighted

	000	**010**	**110**	**100**
000	1	x	1	1
011	0	0	1	0
100	0	0	x	0

The Boolean expressions derived from these maps are given in (4)-(6):

$$\overline{C}\overline{D}\overline{E_L}\overline{E_R} + B_A B_C \overline{C}\overline{D}\overline{E_L}\overline{E_R} + B_A B_C \overline{C}\overline{D} E_L E_R + B_A B_C \overline{C} D \overline{E_L}\overline{E_R} \quad (4)$$

$$\overline{C}\overline{D}\overline{E_L}\overline{E_R} + B_A B_C \overline{C}\overline{D}(\overline{E_L}\overline{E_R} + E_L E_R) + B_A B_C \overline{C} D \overline{E_L}\overline{E_R} \quad (5)$$

$$\overline{C}\overline{D}\overline{E_L}\overline{E_R} + B_A B_C \overline{C}\overline{D}(\overline{E_L \oplus E_R}) + B_A B_C \overline{C} D \overline{E_L}\overline{E_R} \quad (6)$$

6.1.3 Explanation of 0-vectors

To explain the 0-vectors, Table 26 lists the Boolean expression of the referred board segments and the ARS variations. The highlighted areas are non-zero vectors for lower tolerance circuits.

Table 26: Empty Vector Explanation

ARS Correspondence	B_AB_CC	
x	001	C is never present without B
6	010	When B_C is present and B_A is not, performance is less than 5V
x	011	C is never present without B_A
x	101	C is never present without B_C
1, 7	111	When C is present, performance is less than 5V
	DE_LE_R	
x	001	E_R is never present without E_L
9	010	When E_L is present and E_R is not, performance is less than 5V
1, 8	100	When D is present, performance is less than 5V
x	101	E_R is never present without E_L
x	110	D is never present without E_R
1	111	When D, E_L and E_R are present, performance is less than 5V

6.2 ENERGY HARVESTING MEASUREMENTS WITH MODIFICATIONS

The variables in this section differ from the variables in the previous section with the exception of E_L and E_R. This section focuses primarily more on ground plane removal. The derivation of the Boolean expressions is the same. The same tables are used to describe the process of derivation. To make the Boolean expressions more readable (A_{GND}, B_{GND}, C_{GND}, D_{GND}, E_{LEFT}, E_{RIGHT}) will be referred to as (A_G, B_G, C_G, D_G, E_L, E_R), respectively.

6.2.1 Board 1: Low Tolerance

Table 27 lists the Boolean criteria used for this segment of the experiment. Table 28 is the truth table, and Table 29 is the K-map. In this case, there are four 1's.

Table 27: Boolean Criteria

1	V = 5 V @ 70 cm
0	V < 5 V @ 70 cm

Table 28: Truth Table

Low Tolerance		**0.7m**		
Boolean Value		**[V]**	**$A_GB_GC_G$**	**$D_GE_LE_R$**
0	1	4.65	111	111
1	1-D_{GND}	5	111	011
1	1-C_{GND}-D_{GND}	5	110	011
1	1-B_{GND}-C_{GND}-D_{GND}	5	100	011
1	1-A_{GND}-B_{GND}-C_{GND}-D_{GND}	5	000	011
0	1-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}	3.7	000	010
0	1-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}-E_{LEFT}	4.75	000	000

Table 29: K-map

	$A_G B_G C_G$								
$D_G E_L E_G$									
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
	000	0	0	0	0	0	0	0	0
	001	0	0	0	0	0	0	0	0
	010	0	0	0	0	0	0	0	0
	011	1	0	0	0	1	0	1	1
	100	0	0	0	0	0	0	0	0
	101	0	0	0	0	0	0	0	0
	110	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0	0

Table 30 is a simplified form of this map with minterms highlighted.

Table 30: Simplified Form of K-Map with Minterms Highlighted

	000	**100**	**110**	**111**
000	1	1	1	1

The Boolean expressions derived from this set of maps are given in (7) and (8):

$$\overline{B_G}\,\overline{C_G}\,\overline{D_G}\,\overline{E_L}\,\overline{E_R} + A_G B_G \overline{D_G}\,\overline{E_L}\,\overline{E_R} \tag{7}$$

$$\overline{D_G}\,\overline{E_L}\,\overline{E_R}\,(\overline{B_G}\,\overline{C_G} + A_G B_G) \tag{8}$$

6.2.2 Board 1: Higher Tolerance

Table 31 lists the Boolean criteria for this segment of the experiment. Table 32 is the truth table and Table 33 is the K-map. The same assumptions are made here. Again, don't cares (x) represent marginal values.

Table 31: Boolean Criteria

1	V = 5 V @ 70 cm
0	V < 4.5 V @ 70 cm
x	4.5 V < V < 5 V @ 70 cm

Table 32: Truth Table

Higher Tolerance		**0.7m**		
Boolean Value		**[V]**	**$A_GB_GC_G$**	**$D_GE_LE_R$**
x	1	4.65	111	111
1	$1\text{-}D_{GND}$	5	111	011
1	$1\text{-}C_{GND}\text{-}D_{GND}$	5	110	011
1	$1\text{-}B_{GND}\text{-}C_{GND}\text{-}D_{GND}$	5	100	011
1	$1\text{-}A_{GND}\text{-}B_{GND}\text{-}C_{GND}\text{-}D_{GND}$	5	000	011
0	$1\text{-}A_{GND}\text{-}B_{GND}\text{-}C_{GND}\text{-}D_{GND}\text{-}E_{RIGHT}$	3.7	000	010
x	$1\text{-}A_{GND}\text{-}B_{GND}\text{-}C_{GND}\text{-}D_{GND}\text{-}E_{RIGHT}\text{-}E_{LEFT}$	4.75	000	000

Table 33: K-map

	$A_G B_G C_G$								
$D_G E_L E_G$									
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
	000	x	0	0	0	0	0	0	0
	001	0	0	0	0	0	0	0	0
	010	0	0	0	0	0	0	0	0
	011	1	0	0	0	1	0	1	1
	100	0	0	0	0	0	0	0	0
	101	0	0	0	0	0	0	0	0
	110	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0	x

Again, the highlighted minterms are shown in the reduced K-map in Table 34.

Table 34: Simplified Form of K-Map with Minterms Highlighted

	000	**100**	**110**	**111**
000	x	0	0	0
011	1	1	1	1
111	0	0	0	X

The logical expression based on the K-maps in this section is given in (9):

$$A_G B_G C_G D_G E_L E_R + \overline{A_G}\,\overline{B_G}\,\overline{C_G}\,\overline{D_G}\,\overline{E_L}\,\overline{E_R} + \overline{D_G} E_L E_R (\overline{B_G}\,\overline{C_G} + A_G B_G) \quad (9)$$

6.2.3 Board 2: Low Tolerance

Table 35 lists the Boolean criteria for this section. Table 36 is the truth table, and Table 37 is the K-map. There are 3 1's in this case.

Table 35: Boolean Criteria

1	V = 5 V @ 70 cm
0	V < 5 V @ 70 cm

Table 36: Truth Table

Low Tolerance		**0.7m**	**$A_GB_GC_G$**	**$D_GE_LE_R$**
Boolean Value		**[V]**		
1	2	5	111	111
1	2-C_{GND}-D_{GND}	5	110	011
0	2-B_{GND}-C_{GND}-D_{GND}	3.82	100	011
0	2-A_{GND}-B_{GND}-C_{GND}-D_{GND}	3.758	000	011
0	2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}	0.645	000	010
1	2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}-E_{LEFT}	5	000	000

Table 37: K-map

	$A_G B_G C_G$								
$D_G E_L E_G$									
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
	000	1	0	0	0	0	0	0	0
	001	0	0	0	0	0	0	0	0
	010	0	0	0	0	0	0	0	0
	011	0	0	0	0	0	0	1	0
	100	0	0	0	0	0	0	0	0
	101	0	0	0	0	0	0	0	0
	110	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0	1

Table 38 shows a simplified form of this map with minterms highlighted.

Table 38: Simplified Form of K-Map with Minterms Highlighted

	000	**110**	**111**
000	1	0	0
011	0	1	0
111	0	0	1

The logical expression derived from the K-maps in this section is given in (10):

$$A_G B_G C_G D_G E_L E_R + A_G B_G \overline{C_G D_G} E_L E_R + \overline{A_G B_G C_G D_G E_L E_R} \quad (10)$$

6.2.4 Board 2: Higher Tolerance

Table 39 lists the Boolean criteria used in this section of the experiment. In this case, there are three 1's and two don't cares (x's). Table 40 is the truth table, and Table 41 is the K-map.

Table 39: Boolean Criteria

1	V = 5 V @ 70 cm
0	V < 3.5 V @ 70 cm
x	3.5 V < V < 5 V @ 70 cm

Table 40: Truth Table

Higher Tolerance		**0.7m**	$A_GB_GC_G$	$D_GE_LE_R$
Boolean Value		**[V]**		
1	2	5	111	111
1	2-C_{GND}-D_{GND}	5	110	011
x	2-B_{GND}-C_{GND}-D_{GND}	3.82	100	011
x	2-A_{GND}-B_{GND}-C_{GND}-D_{GND}	3.758	000	011
0	2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}	0.645	000	010
1	2-A_{GND}-B_{GND}-C_{GND}-D_{GND}-E_{RIGHT}-E_{LEFT}	5	000	000

Table 41: K-map

	$A_G B_G C_G$								
$D_G E_L E_G$									
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
	000	1	0	0	0	0	0	0	0
	001	0	0	0	0	0	0	0	0
	010	0	0	0	0	0	0	0	0
	011	x	0	0	0	x	0	1	0
	100	0	0	0	0	0	0	0	0
	101	0	0	0	0	0	0	0	0
	110	0	0	0	0	0	0	0	0
	111	0	0	0	0	0	0	0	1

Table 42 is a simplified form of this map with minterms highlighted.

Table 42: Simplified Form of K-Map with Minterms Highlighted

	000	**100**	**110**	**111**
000	1	0	0	0
011	x	x	1	0
111	0	0	0	1

The logical expression derived from the K-maps in this section is given in (11):

$$A_G \overline{C_G} \overline{D_G} E_L E_R + \overline{A_G} B_G \overline{C_G} D_G \overline{(E_L \oplus E_R)} + A_G B_G C_G D_G E_L E_R \tag{11}$$

6.2.5 Other Boards

Some of these variations are redundant after removing certain components, and they will be discussed here. Measurement results were all comparable as expected when the PCB traces and proximate elements were the same. Board 3 is Board 2 without E_L and E_R. Board 5 is Board 4 without B_{ANT}. Board 6 and board 10 (which are identical) are Board 4 without B_{CKT}. Board 9 is board 3 without E_{LEFT}.

The measurement of Board 4 exceeded the limits of the testing equipment at 70cm range; measurements conducted at 1m show slight improvement, worth defining in Boolean terms. There are two 1's in this case, as shown in (12) and (13).

$$\overline{A_G B_G C_G D_G E_L E_R} + \overline{A_G B_G C_G D_G E_L E_R} \tag{12}$$

$$\overline{B_G C_G D_G E_L E_R} \tag{13}$$

Board 7 performed poorly until the active (in-use) antenna grounds were removed. There are also 2 1's in this case, as shown in (14) and (15).

$$\overline{A_G} B_G \overline{C_G D_G E_L E_R} + \overline{A_G B_G C_G D_G E_L E_R} \tag{14}$$

$$\overline{A_G C_G D_G E_L E_R} \tag{15}$$

Board 8 performed only marginally until active ground planes were removed. There are also two 1's in this case as shown in (16) and (17).

$$\overline{A_G B_G C_G D_G E_L E_R} + \overline{A_G B_G C_G} D_G \overline{E_L E_R} \tag{16}$$

$$\overline{A_G B_G C_G E_L E_R} \tag{17}$$

Board 9 was the poorest performer until E_{LEFT} was removed. There is only one Boolean expression for this circuit to work effectively, and that is shown in (18).

$$\overline{E_L E_R} \tag{18}$$

6.2.6 Explanation of 0-Vectors

To again explain the 0-vectors, Tables 43 and 44 list the minterms for Boards 1 and 2. The highlighted areas change to non-zero vectors with lower tolerances.

Table 43: 0-Vector Explanation for Board 1

$A_G B_G C_G$	
001	C_G is never present without A_G and B_G
010	B_G is never present without A_G
011	B_G and C_G are never present without A_G
101	A_G and C_G are never present without B_G
$D_G E_L E_R$	
000	When D_G and E_L and E_R are all missing, performance is < 5V
001	E_R is never present without E_L
010	E_L is never present without D_G
100	D_G is never present without E_L and E_R
101	D_G and E_R are never present without D_L
110	D_G is never present without E_L and E_R
111	When D_G and E_L and E_R are all present, performance is < 5V

Table 44: 0-Vector Explanation for Board 2

$A_G B_G C_G$	
001	C_G is never present without A_G and B_G
010	B_G is never present without A_G
011	B_G and C_G are never present without A_G
100	A_G is never present without B_G
101	A_G and C_G are never present without B_G
$D_G E_L E_R$	
001	E_R is never present without E_L
010	E_L is never present without D_G
100	D_G is never present without E_L and E_R
101	E_R is never present without E_L
110	When E_L is present without E_R, performance is < 5V

6.3 ANALYSIS

Table 45 summarizes the Boolean expressions. When all 9 boards are considered, some common terms stand out. First, section E must be included in its entirety, or not at all. Sections C and D also hinder performance when present.

Boards 1 and 2 share common terms. Performance is best only with all grounds and Section E either completely included or excluded. If C_G and D_G are not present and E_L and E_R are present, performance is adequate. Board 4 works best when all inactive grounds and section E are completely removed. Boards 7 and 8 also require the removal all grounds and section E to perform well. Boards that resembled other boards when modified, such as 5 without B_{ANT} or 6 without B_{CKT}, all performed competitively despite the imperfect nature of the testing facility.

Table 45: Summary of Boolean Expressions

Board(s)	Tolerance	Boolean Expression
All	Low	$\overline{B_C C D E_L E_R} + B_A B_C \overline{C D}(\overline{E_L \oplus E_R})$
All	High	$\overline{C D E_L E_R} + B_A B_C \overline{C D}(\overline{E_L \oplus E_R}) + B_A B_C \overline{C D} \overline{E_L E_R}$
1	Low	$\overline{D_G E_L E_R}(\overline{B_G C_G} + A_G B_G)$
1	High	$A_G B_G C_G D_G E_L E_R + \overline{A_G B_G C_G D_G E_L E_R} + \overline{D_G} E_L E_R(\overline{B_G C_G} + A_G B_G)$
2	Low	$A_G B_G C_G D_G E_L E_R + A_G B_G \overline{C_G D_G} E_L E_R + \overline{A_G B_G C_G D_G E_L E_R}$
2	High	$A_G \overline{C_G D_G} E_L E_R + \overline{A_G B_G C_G D_G}(\overline{E_L \oplus E_R}) + A_G B_G C_G D_G E_L E_R$
4	n/a	$\overline{B_G C_G D_G E_L E_R}$
7	n/a	$\overline{A_G C_G D_G E_L E_R}$
8	n/a	$\overline{A_G B_G C_G E_L E_R}$

7 .0 CONCLUSIONS AND FUTURE RESEARCH

7.1 CONCLUSIONS

7.1.1 General Conclusions

In conclusion, proximate elements in RF circuits do impact performance. The procedure to isolate these influences is to fabricate a specific number of variations of the PCB or IC in question based upon the maximum number of potential variable sections of the circuit. Once fabrication is complete, the circuits should be tested, and then sections of the circuit should be removed and the resulting circuit re-tested. The intent is to derive data from which a Boolean table could be defined, for purposes of analyzing the performance-value of each circuit variation. Then the final circuit design should incorporate the circuits with the greatest performance-value, as dictated by the Boolean tables.

Engineers can use this method to design circuits with variations unique to their own circuit as a part of the design process. Design rules for a specific circuit can be extracted from Boolean data. If this technique is integrated into the design process, all interferences are documented, and any constructive interference can be used to harvest more energy if desired.

7.1.2 ARS Conclusions

In the specific circuits used for this research, the E section had the most influence on the ability to harvest RF energy. The commonly occurring expression in (19)

$$\overline{E_L}\,\overline{E_R} \tag{19}$$

is included by (20).

$$\overline{(E_L \oplus E_R)} \tag{20}$$

(19) or (20) show up in every expression in one form or another. If E_{LEFT} is present without E_{RIGHT}, performance suffers dramatically. E_{LEFT} contains a long trace that was originally intended to be an antenna for a signal transmission. This trace is shortened when E_{RIGHT} is not included, raising its resonant frequency closer to 915 MHz (refer to appendix C for details).

In the cases of all boards being compared with no modifications, a common term (21) appeared in both the low and high tolerance tests.

$$B_A B_C \overline{C}\,\overline{D}\,\overline{(E_L \oplus E_R)} \tag{21}$$

The other term in the low tolerance test (22) is included in a similar term in the high tolerance test (23).

$$\overline{B_C}\,\overline{C}\,\overline{D}\,\overline{E_L}\,\overline{E_R} \tag{22}$$

$$\overline{C}\,\overline{D}\,\overline{E_L}\,\overline{E_R} \tag{23}$$

After the boards were modified (and all essentially became boards 1, 2, 4, 7 and 8), boards 1, 2, 4, 7 and 8 all gained a common term (24)

$$\overline{A_G}\,\overline{B_G}\,\overline{C_G}\,\overline{D_G}\,\overline{(E_L \oplus E_R)} \tag{24}$$

which is inclusive of (25), as seen in all boards (specifically boards that never included E).

$$\overline{A_G}\,\overline{B_G}\,\overline{C_G}\,\overline{D_G}\,\overline{E_L}\,\overline{E_R} \tag{25}$$

With the two boards that contained three antennas/doublers (Boards 7 and 8), removing the ground planes of the active (in-use) antennas improved performance. Conversely, the boards with only one antenna/doubler improved when all *inactive* ground planes were removed.

With all of these terms in mind, a combination of terms from the two different sets of tests is shown in (26). (27) is a reduced form.

$$B_A B_C \overline{C}\,\overline{D}(\overline{E_L \oplus E_R}) + \overline{A_G}\,\overline{B_G}\,\overline{C_G}\,\overline{D_G}(\overline{E_L \oplus E_R}) \tag{26}$$

$$(B_A B_C \overline{C}\,\overline{D} + \overline{A_G}\,\overline{B_G}\,\overline{C_G}\,\overline{D_G})(\overline{E_L \oplus E_R}) \tag{27}$$

The pieces of this expression can be broken down as follows. (28) indicates that no more than two antenna/doubler combinations should be used in that area. (29) indicates that antenna grounds should not be included. (30) indicates that long traces should not be included in the proximity of the antennas unless tested thoroughly for interference.

$$B_A B_C \overline{C}\,\overline{D} \tag{28}$$

$$\overline{A_G}\,\overline{B_G}\,\overline{C_G}\,\overline{D_G} \tag{29}$$

$$\overline{E_L \oplus E_R} \tag{30}$$

The best performers overall were the boards with only one antenna/doubler. In the cases with two antennas/doublers, performance is best when E_{LEFT} and E_{RIGHT} are both included or omitted. Boards 3, 4, 5, and 6 fall into this category. Ground plane removal enhanced performance of these boards. The worst performers overall were boards with more than two antennas/doublers. Intact ground planes also inhibited performance as well as the presence of E_{LEFT} without E_{RIGHT}. These boards can be modified for comparable performance.

The major factors in energy harvesting, in order of magnitude of interference, are:

1. Long PCB traces oriented perpendicularly and/or parallel to spiral PCB antenna traces that resonant near the frequency used for energy harvesting.
2. The number of antennas/doublers
3. The presence of Antenna Grounds

The minor determinates, having little or no effect in energy harvesting, are the soldered components. This is not to say these components appear to never seriously interfere with energy harvesting, in this case any effect of soldered components was not manifested.

The conclusions are supported by the fact that thorough research was conducted. Several sessions in addition to those mentioned in the thesis have been conducted. A large amount of measurements were conducted in order to have a large sample of data to work from. The concept of verification was in mind during the research. All results are repeatable in the given conditions. For instance, the original anomaly, board 9, is a prime example of how consistency and repeatable results were achieved. Three of the original ARS boards contained the thermal circuitry. When modified, circuit performance was reduced. When modified again, performance had increased.

7.1.3 Extracted Design Rules

With all of this in mind, a set of design guidelines and rules can be formed for the Device Under Test (DUT). In this case, there are three major rules based on the factors unique to this circuit:

1. Avoid long traces parallel and perpendicular to the antennas that are close to ½ λ or ¼ λ.
2. Do not use more than two antenna/doubler pairs.
3. Do not lay out ground planes below antennas.

7.2 FUTURE RESEARCH

7.2.1 ARS PCB

Because E was a major influence on performance, a set of experiments could be done on section E alone. The entire circuit could be redesigned, moved or reoriented to alter performance. More analysis would be done to determine the sensitive areas of the circuit.

Another good follow-up would be to remove the ground planes in different orders for each board. If conducted as thoroughly as the last suggested experiment, this will require $2^4 = 16$ separate populated PCBs.

With these two tests combined, a board should be fabricated using combinations of ground planes and segments of E that are determined by the results. If this board's performance is in the top 5-10%, it would be clear how much the proximate elements contribute to interference. Re-orienting antennas and moving components systematically to monitor variations would be an area of interest.

7.2.2 IC Experiment

Using the same technique, repeat the process for an IC version of the ARS. Since there is no way to generate infrared signals on an IC, other methods of measurement must be used, such as a VCO, which has been proven as an effective method of measuring harvested DC energy [4].

A problem will manifest itself as the actual VCO circuitry cannot be measured for interference itself, due to the inability to transmit the measured voltage. Relocating the VCO may change circuit performance, in which case, a best case scenario would be to place the VCO where it least hinders performance. Testing with IC variants is much more costly than doing testing with PCB variants, so abundant funding or a cheap process will be required.

APPENDIX A

Background Information

A.1.1 RFID Overview

Radio Frequency Identification (RFID) technology provides a mechanism to replace barcodes, tracking systems, security systems, and other portable identification devices. The concept of a 'radio' barcode is analogous to an RFID device. The common scenario of device usage involves an RFID device that enters a designated spatial location and transmits a sequence of data to a specific receiving device.

The benefits of using an RFID system over traditional identification mechanisms are numerous. The most important is the ability to identify the RFID transponders without having line of site. In retail environments, today's methods of dealing with identifying products involve barcodes. These barcodes need to be presented to a laser scanner in an almost perpendicular fashion at close ranges in order to be read correctly. More importantly, only one object may be scanned at a time. In practical terms, this reduces the efficiency of 'checking out' in a retail environment. RFID systems do not require line of site. In fact, the item being 'scanned' may even be behind other items, and still respond to the 'scanning' signal, or interrogating signal, as it is commonly referred to in RFID terminology.

The devices used in this research are referred to as RFID transponders. A transponder transmits and responds information. Most currently RFID transponders in use are in the form of stickers, thin metal sheets or even plastic tags with small amounts of circuitry inside. These have been sufficient for current applications until now. Future demand for the technology will require more compact systems in order to cut costs of fabrication and implementation. Also, the smaller the transponder, the harder it will be to find and tamper with. These devices must become more portable, so the size constraints are limiting. The goal is to be able to embed these transponders

into anything so they can be taken and used anywhere at anytime. Some applications will involve a transponder enclosed in product packaging that will activate when interrogated by a cashier, and others will involve a transponder contained within key-ring sized packaging that is used by the consumer themselves when purchasing gasoline, or some other automated RFID service.

A.1.2 Active RFID versus Passive RFID

Active transponders make use of an on-board power supply (typically a battery) as well as an active transmitter. The use of localized power source makes it possible to utilize more power when transmitting. This results in a greater range of use for the transponder, as well as a way to compensate for a low signal to noise ratio (SNR). Active transponders may be configured to take advantage of more complex encoding schemes, as well as decoding any data signals from the interrogator.

There are two different kinds of passive transponders, semi-passive and passive. Semi-passive transponders use an on-board power source, but no active transmitter. Passive transponders use no on-board power source, meaning they are remotely powered, and no active transmitter. By referring to an active transmitter, the use of discrete components to modulate a new signal is implied. The alternative is to use a concept known as modulated backscatter, which is the process of modulating the reflected waves by shunting a load and changing impedances, resulting in an amplitude modulated (AM) carrier.

A.1.3 Energy Harvesting

In passive RFID implementations, the lack of a battery implies the need for another source of power. Current research involves a concept known as energy harvesting. Energy harvesting is achieved by rectifying the received signal. Rectification can be achieved with many different circuit topologies. Three common textbook rectifiers are the half-wave, full-wave and voltage doubler. These essentially eliminate or invert negative peaks of a carrier wave, and use a filter capacitor to maintain the output voltage at a steady positive DC value. This DC voltage is used to supply power to other parts of the transponder.

APPENDIX B

PCB Photographs

Figure 48: ARS PCB Variation 1

Figure 49: ARS PCB Variation 2

Figure 50: ARS PCB Variation 3

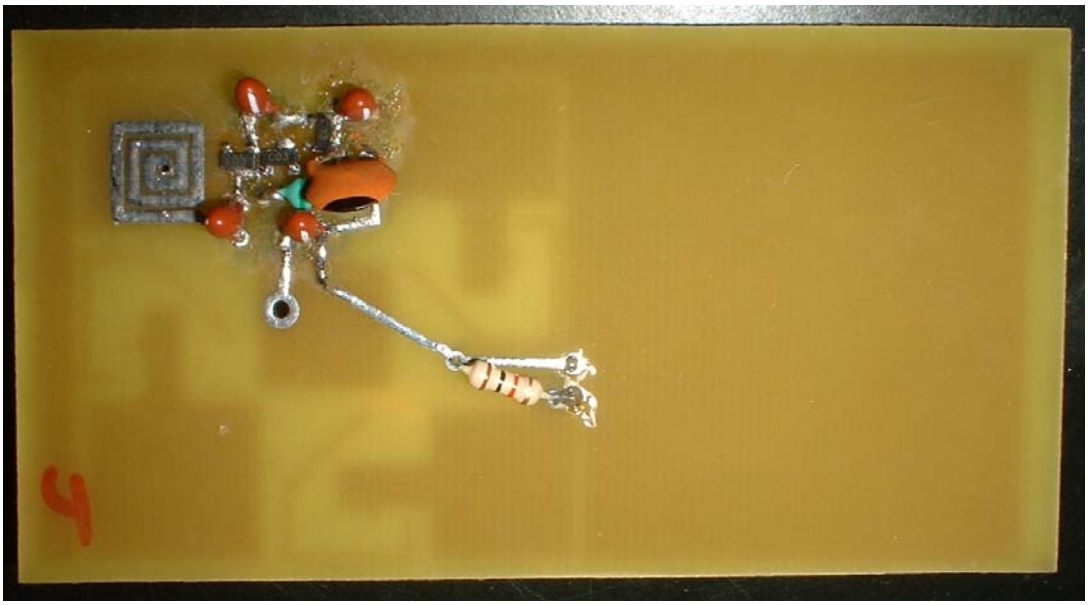

Figure 51: ARS PCB Variation 4

Figure 52: ARS PCB Variation 5

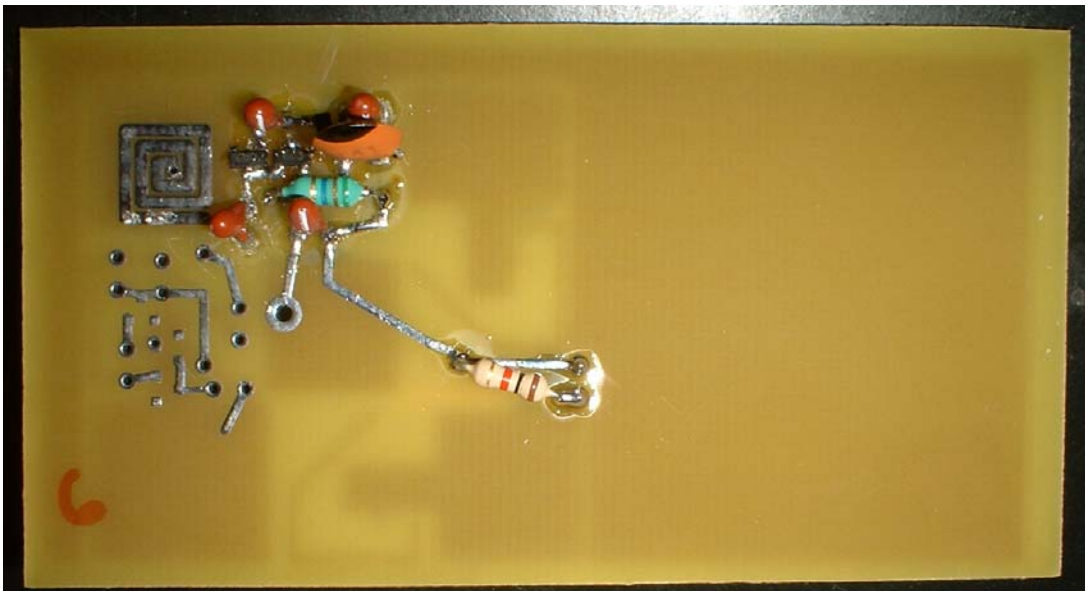

Figure 53: ARS PCB Variation 6

Figure 54: ARS PCB Variation 7

Figure 55: ARS PCB Variation 8

Figure 56: ARS PCB Variation 9

APPENDIX C

Center Frequency Calculations of long E-Region trace

Assumptions [5]:

1. $F = c/\lambda$
2. $c = 3x10^8$ m/s

Unmodified E-region
Vertical segment = 1.125
Horizontal segment = 2.725
Total length = 3.85 inches = 0.09779 meters (1/4 λ)
Resonant frequency = 766,949,585 Hz ~ 766 MHz

Modified E-region
Vertical segment = 1.125
Horizontal segment = 2.475
Total length = 3.6 inches = 0.09144 meters (1/4 λ)
Resonant frequency = 820,209,973 Hz ~ 820 MHz

Shift in center frequency ~ 53 MHz

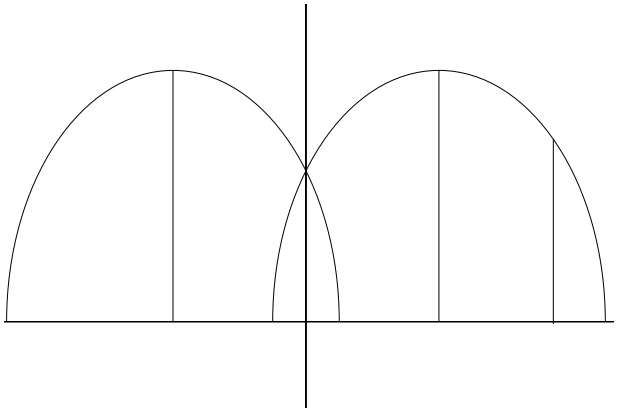

Figure 57: Bandwidth Coverage

This is significant due to the common orientation of the antennas and the long trace. Field lines of each reception element are commonly oriented, causing a significant amount of the fields to interfere with one another.

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