INVESTIGATION INTO VAPOR-LIQUID-SOLID GROWTH OF BETA-GALLIUM OXIDE NANOWIRES AND METHODS FOR DEVICE IMPLEMENTATION

by

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INVESTIGATION INTO VAPOR-LIQUID-SOLID GROWTH OF BETA-GALLIUM OXIDE NANOWIRES AND METHODS FOR DEVICE IMPLEMENTATION

John R. Erickson, M.S.

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Gallium oxide (Ga_2O_3) has recently gained interest in the scientific community due to its large semiconductor energy bandgap and other advantageous electronic material properties. With the rise of cost effective manufacturing capabilities for single crystal native substrates, along with improved capabilities for producing low-dimensional structures, Ga_2O_3 has the potential to offer significant advantages in select facets of the electronics industry. High quality, single crystal Ga_2O_3 nanowires can easily be grown through a simple vapor-liquid-solid (VLS) mechanism. Since it was first proposed, the VLS growth mechanism has been extensively used for any unidirectional growth with a liquid mediating phase and precursors supplied from a vapor phase. This work investigates the VLS growth of Ga_2O_3 nanowires at varying temperatures and pressures and categorizes the resulting nanowires. In addition, a method for selectively patterned deposition and alignment of nanowires called combing is demonstrated for the as-grown Ga_2O_3 nanowires. Traditional methods for nanowire deposition use arrays of pre-patterned electrodes and disperse the nanowires among them, resulting in a few working devices. Nanowire combing can pre-pattern selected areas for nanowire deposition, increasing the reliability and yield of the fabrication process and is readily adaptable to existing semiconductor fabrication technologies.

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PREFACE

This work could not have been done without the help of several people. First and foremost, I would like to thank Dr. William Stanchina for advising me throughout my time in graduate school here at PITT and helping me with everything that comes along in life and work. I also want to thank the other members of my committee Dr. Feng Xiong and Dr. Minhee Yun for their time and understanding of the delays that came along in the completion of this project. I would also like to especially thank Dr. Susheng Tan for his help in the initial imaging of our nanowires when this project was just getting started, as well as his efforts in imaging all of the TEM images seen in chapter 4, as well as the FIB and sample analysis done in Fig. 4.9. Dr. Jun Chen as well as Pei Liu helped me better understand the lithographical processes used in this work as well, and this would not be possible without them.

Finally, a huge thank you to all of my friends and family who put up with me and helped me make it through this thesis, I couldn't possibly list you all here. However, I would like to give a special thank you to my labmate Joseph Kozak for helping me edit this work. I would also like to express my heartfelt thanks to my girlfriend, editor, and academic role model, Erica Stevens. I wouldn't have made it through any of this without you.

1.0 INTRODUCTION

Gallium oxide (Ga_2O_3) has recently gained interest in the scientific community due to its large bandgap and advantageous electronic material properties. With the rise of cost effective manufacturing capabilities for single crystal native substrates, along with improved capabilities for producing low-dimensional structures, Ga_2O_3 has the potential to offer significant advantages in select facets of the electronics industry. This chapter discusses some basic material properties of Ga_2O_3 along with some devices already being pursued.

1.1 GALLIUM OXIDE MATERIAL BASICS AND APPLICATIONS

There are five known phases of gallium oxide (Ga_2O_3): α, β, γ, δ, and ε. The β phase is the most stable, both chemically and thermally, and is the subject of this work. The other phases are metastable and will revert back to β-phase at temperatures above 600 ^oC [1]. β-Ga_2O_3 belongs to the C2/m space group and has a base centered monoclinic crystal structure with the crystallographic lattice constants listed below in Fig 1.1. In a 20-atom unit cell there are four Ga_2O_3 formula units, with two nonequivalent Ga atoms, Ga(I) and Ga(II), and three nonequivalent O ions, O(I), O(II), and O(III). Ga(I) is tetrahedrally coordinated while Ga(II) is octahedrally coordinated, and the oxygen ions are arranged in a distorted cubic close-packed array, with O(I) and O(II) being threefold coordinated and O(III) is fourfold coordinated [2].

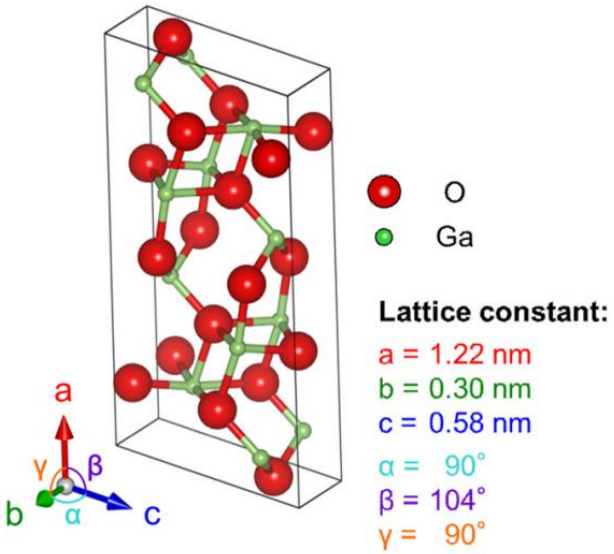


Figure 1.1 Crystal structure of β-Ga_2O_3. Reproduced from [3], with the permission of John Wiley and Sons.

β-Ga_2O_3 has a bandgap typically listed between 4.7 and 4.9 eV. The detailed band structure of β-Ga_2O_3 was calculated by Varley et al., using Vienna Ab initio Simulation Package (VASP) code [2]. They based their calculations on traditional density functional theory (DFT), but used novel hybrid functionals which account for the bandgap problem that affects traditional DFT.

Density Functional Theory (DFT) is an analytical method used to accurately calculate band structures. DFT takes advantage of the Hohenberg-Kohn theorem, which states that for any system, the total many-body electron energy is a unique functional of the local charge density [4]. By guessing a form for the electron density function, the total energy for that system can be computed. By then varying the form of the electron density function and comparing the total energy, the form that minimizes the total energy can be found.

Using DFT, Varley found an indirect bandgap of 4.83 eV near the *M* point, and a direct bandgap of 4.87 eV at the Γ point. Analysis of the dipole matrix elements showed that while vertical transitions are dipole-allowed at the Γ point, the transition probability rapidly decreases to

0 at the *M* point, making β-Ga_2O_3 a direct-gap material. This conclusion is supported by the observed sharp optical absorption peak at 4.9 eV.

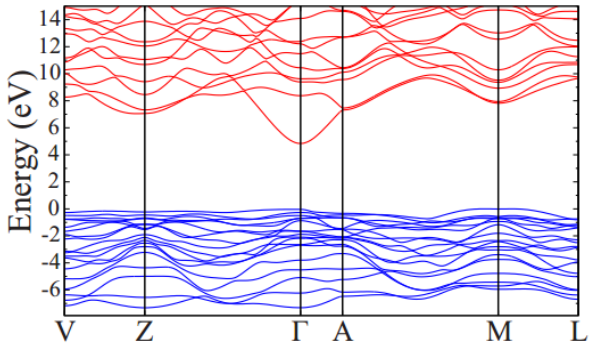


Figure 1.2 Calculated band structure of β-Ga_2O_3 Reproduced from [2] , with the permission of AIP Publishing.

Varley et al. also calculated electron and hole effective masses from this modeling. They found that the electron effective mass, m_e^*, is almost isotropic with a value of 0.281 +/- 0.005 m_e. However, the effective hole mass is vastly directionally dependent with a value of ~40 m_e along the *Γ-Z* direction, but ~0.40 m_e along the *Γ-A* direction [2]. This is confirmed by other groups' observations of very low hole conduction in intrinsic β-Ga_2O_3 systems [2, 5–7].

After finding that undoped Ga_2O_3 lacked useful conductivity, Villora et al. investigated the effects of Si doping on β-Ga_2O_3 [8]. They found that not only is Si an effective *n*-type dopant, it can change the conduction and free-carrier concentration by up to three orders of magnitude. Further investigation revealed that Si is the main impurity present in commercial Ga_2O_3 powders, such as those often used in growth of bulk crystals. It was also confirmed by Varley et al. that Si, Ge, Sn, F, and Cl all behave as shallow donors, confirming the source of unintentional doping [2]. Varley's group also confirmed the calculations for the ionization energy of oxygen vacancies. Originally, it was thought that β-Ga_2O_3 was intrinsically *n*-type due to shallow donor oxygen

vacancies but Varley's work showed that they are in fact deep donors and thus not significant contributors to conduction.

Along with its electrical characteristics, the relatively simple growth methods for mass production make β-Ga_2O_3 an attractive replacement for SiC and GaN. SiC and GaN bulk wafers are grown from diluted vapor sources, which can be expensive and wasteful of materials. β-Ga_2O_3, however, can be grown from atmospheric melt sources which is the current standard in electronics industries, due to their high growth rates and relatively low cost.

There have been several different methods developed to grow single crystal β-Ga_2O_3 wafers from a melt. These include floating zone technique [9], Verneuil technique [10], Czochralski method [7], flux method [11] and chemical vapor transport [12]. However, the most common by far is the edge-defined film-fed growth (EFG) first designed by LaBelle and Mlavsky in 1971 [13]. One of the main advantages of the EFG method is the ability to precisely control the cross-sectional shape and size of the grown crystals.

A typical EFG process is illustrated below in Fig. 1.3a. Ga_2O_3 powder is used as the source material and placed in the crucible. Upon melting, the Ga_2O_3 is forced upwards through the die slit through capillary action. Once the melt reaches the top of the die, a seed crystal is placed in contact and drawn out as illustrated below in Fig. 1.3b.

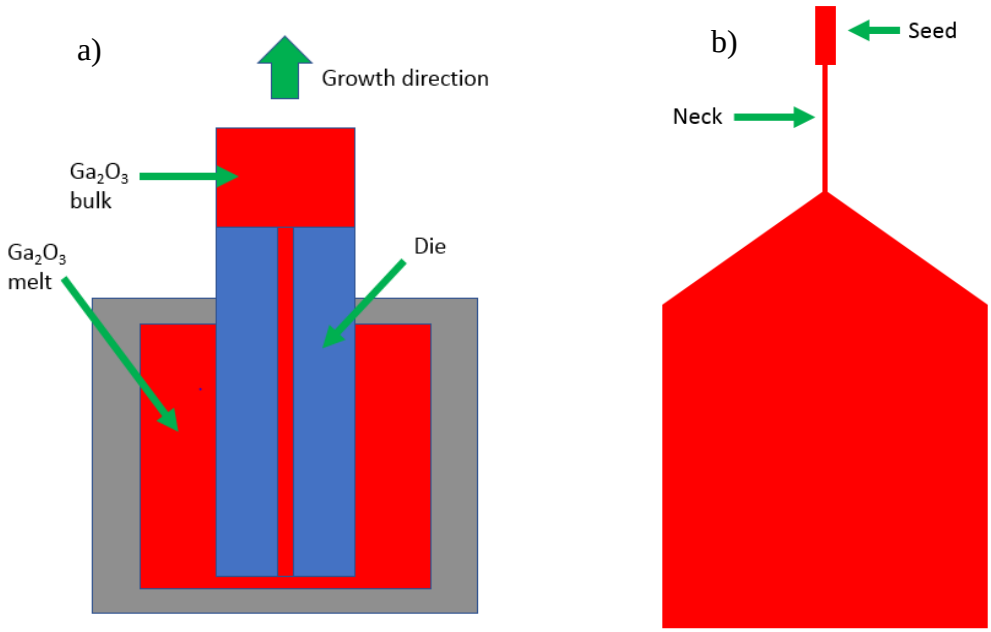


Figure 1.3 Example of typical edge-defined film-fed growth set up. Fig. 1.3a depicts a typical growth furnace with melted material moving up the die-slit to form bulk material. Fig 1.3b depicts an example of a fabricated crystal.

Shinamura et al. were the first group to apply the growth techniques developed for other oxides to β-Ga_2O_3. However, their initial crystals were cracked and had several polycrystalline inclusions [13]. By increasing the seeding temperature and decreasing the neck cross section, Aida's group was able to improve upon the previous processes and reduce the number of dislocations, leading to larger single crystal growth [13].

In addition to the bulk growth methods mentioned previously, significant progress in thin film growth has been made. Ga_2O_3 thin films have been readily produced through metal-organic chemical vapor deposition [14], mist chemical vapor deposition [15], molecular beam epitaxy, halide vapor phase epitaxy and atomic layer depositions [5].

Molecular beam epitaxy (MBE) is a very established technique for growing thin films of various semiconducting materials. It was first developed early in the 1970s to grow high-purity epitaxial layers of compound semiconductors. It can produce abrupt interfaces of high-quality

materials with very fine control over the thicknesses, doping levels and composition of the grown materials. For Ga_2O_3 thin films, there are two main set ups, dependent on the oxygen source. One uses oxygen radicals that are generated through a radio-frequency plasma cell, and the other uses ozone. Sasaki et al. were able to produce Sn-doped Ga_2O_3 films on β-Ga_2O_3 (010) substrates with extremely low surface roughness [16].

Halide vapor phase epitaxy (HVPE) is a very attractive production method for β-Ga_2O_3, as it can be done at atmospheric pressures, as opposed to MBE which requires ultra-high-vacuum environments. However, HVPE for β-Ga_2O_3 specifically, is still in its infancy, despite advances made by Higashiwaki et al. [5]. HVPE relies on forming and then reducing chloride gasses, in this case GaCl. A separate inlet for the Cl_2/N_2 gas and pure Ga source are kept at 850 ^oC, which forms GaCl. After leaving this inlet, the $GaCl/N_2$ gasses mix with the O_2/N_2 gasses and travel to the substrates, which are (001) β-Ga_2O_3 grown with EFG. The Ga atoms dissociates from the Cl at the elevated temperature and form with the O_2, forming Ga_2O_3 on the substrate. If *n*-type films are desired, $SiCl_4$ can be simultaneously supplied for Si doping, which has been demonstrated for densities of $10^{15} – 10^{18}$ cm^{-3} [5]. Using this method, growth of high-quality materials has been demonstrated with speeds up to 20 μm/hr.

Due to the asymmetry of its crystal structure, the thermal conductivity of β-Ga_2O_3 is extremely directionally dependent as found by Guo et al. [17], who used time domain thermoreflectance (TDTR) to investigate the thermal conductivity along the [001], [100], [010], and [$\bar{2}$01] directions at various temperatures. TDTR is a method which uses a pulsed laser to heat up thin films, whose reflectance is temperature dependent. By measuring the change of reflectance along the surface, an idea of how the heat from the pulsed laser moves along the surface can then be used to infer the thermal conductivity.

They found that at room temperature the [100] direction had the smallest thermal conductivity of 10.9 ± 1.0 W/mK, while the [010] direction had a value of 27.0 ± 2.0 W/mK [17]. These values are roughly an order of magnitude lower than those for GaN [18]. Furthermore, the thermal conductivity in all directions displays a 1/T relationship, shown below. This is an indication of phonon-dominant thermal transport.

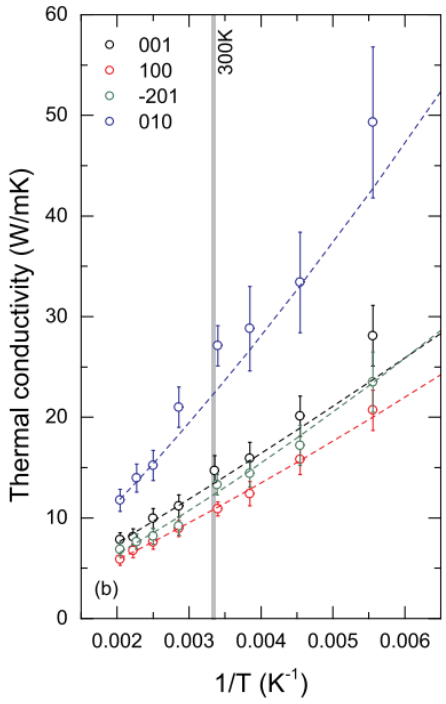


Figure 1.4 1/T vs Thermal Conductivity for β-Ga_2O_3 thin films along different crystallographic directions. Reproduced from [17] , with the permission of AIP Publishing.

1.1.1 High Voltage Power Devices

Use of β-Ga_2O_3 as a native substrate for GaN-based devices is a very appealing application. It would combine the transparency of sapphire with the electrical conductivity of SiC, the two primary substrates currently used [2]. After some investigation, β-Ga_2O_3 on its own also has some

favorable material properties for high voltage power devices. Grown, unintentionally doped, single crystals of β-Ga_2O_3 have been observed to have *n*-type conductivity with electron concentrations between 6 x 10^{16} and 8 x 10^{17} cm^{-3} [7]. Intentional doping of β-Ga_2O_3 can produce concentrations from 10^{15} to 10^{19} cm^{-3} [5]. Single crystals with intentional Si doping had maximum conductivity of 50 Ω^{-1} cm^{-1} and estimated electron mobility of 300 cm^2 Vs^{-1} [2, 7]. In addition, the breakdown electric field is estimated to be around 8 MV cm^{-1}, much higher than other semiconductors [5].

In 1983, Baliga derived a figure of merit (BFOM) that describes material parameters to minimize the conduction losses in power field effect transistors (FETs), given by Equation 1.1,

$$BFOM = \varepsilon \mu E_b^3 \quad (1.1)$$

where ε is the relative dielectric constant, μ is the electron mobility and E_b is the breakdown field [19]. BFOM has since turned into a metric by which to compare materials in any power devices, not just FETs. Typical BFOMs are given relative to Si, the electronic standard. Even though β-Ga_2O_3 has a much smaller electron mobility than Si, since its breakdown field is an order of magnitude higher, its relative BFOM is typically listed as 3444 [3]. A comparison of β-Ga_2O_3 and other materials commonly used are given below in Table 1.1.

Table 1.1 Electronic material propertires of semiconductors. Reproduced from [3], with the permission of John Wiley and Sons.

	Si	GaAs	4H-SiC	GaN	Diamond	β-Ga_2O_3
Bandgap E_g (eV)	1.1	1.4	3.3	3.4	5.5	4.5–4.9
Electron mobility μ (cm^2 Vs^{-1})	1,400	8,000	1,000	1,200	2,000	300
Breakdown field E_{br} (MV cm^{-1})	0.3	0.4	2.5	3.3	10	8
Relative dielectric constant ϵ	11.8	12.9	9.7	9.0	5.5	10
Baliga's FOM $\epsilon \mu E_{br}^3$	1	15	340	870	24,664	3,444
Thermal conductivity (W (cm K)$^{-1}$)	1.5	0.55	2.7	2.1	10	0.27 [010] 0.11 [100]

A power device's on-resistance (R_{on}) is indicative of the amount of conduction loss in a device. This is also based on the break down field of the material and can determine the required semiconductor surface [20]. Ideally, devices should maximize breakdown voltage, while keeping R_{on} at a minimum. Theoretical limits of on-resistances as a function of V_{br} were calculated by Higashiwaki et al. in 2012, and are shown in Fig 1.5 [3]. These calculations show that β-Ga_2O_3 has consistently lower R_{on} than other semiconducting materials currently being used.

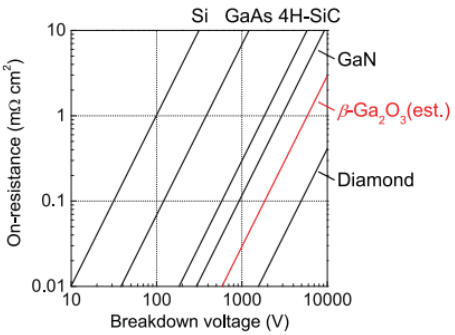


Figure 1.5 Breakdown voltage vs On-resistance of some semiconductor materials. Reproduced from [21], with the permission of AIP Publishing

Several single crystal microelectronic devices have been fabricated from β-Ga_2O_3 thin films on native substrates. These include; metal-semiconductor field effect transistors (MESFETs), depletion-mode MOSFETs, and Schottky barrier diodes (SBDs), represented below in Fig. 1.6.

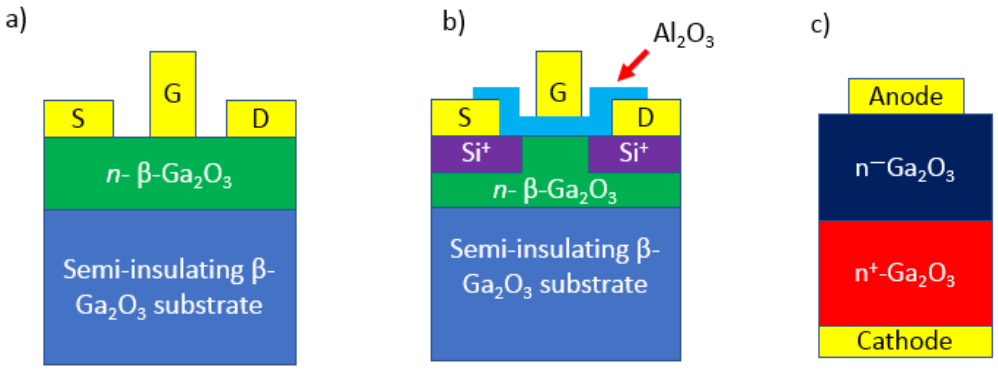


Figure 1.6 Schematic of fabricated microelectronic devices. 1.6a shows the MESFET, 1.6b shows the MOSFETand 1.6c shows the SBDs.

The first demonstration of transistor action for crystalline β-Ga_2O_3 was in 2012 by Higashiwaki et al. [21]. A Sn-doped *n*-type Ga_2O_3 layer was grown on a semi-insulating Mg-doped Ga_2O_3 (010) substrate. The area designated for Ti/Au ohmic contacts was prepped with reactive ion etching (RIE), which significantly increased ohmic properties, as shown below in Fig. 1.7a. Finally, Schottky gates of Pt/Ti/Au were fabricated for the gate. This device exhibited excellent characteristics as a first demonstration, as seen in Fig. 1.7b. Drain current was effectively modulated by the gate voltage and exhibited pinch off at relatively large negative gate bias. The maximum transconductance was 2.3 mS mm^{-1} at V_d = 40 V. The off-state drain leakage current was as small as 5 μA mm^{-1}, with an on/off ratio of four orders of magnitude. However, the device had other issues, including the high contact resistance of the source/drain electrodes and the on/off ratio being limited by the small leakage current. In addition, at a V_d of over 250 V the device had a catastrophic breakdown, permanently damaging the gate electrode.

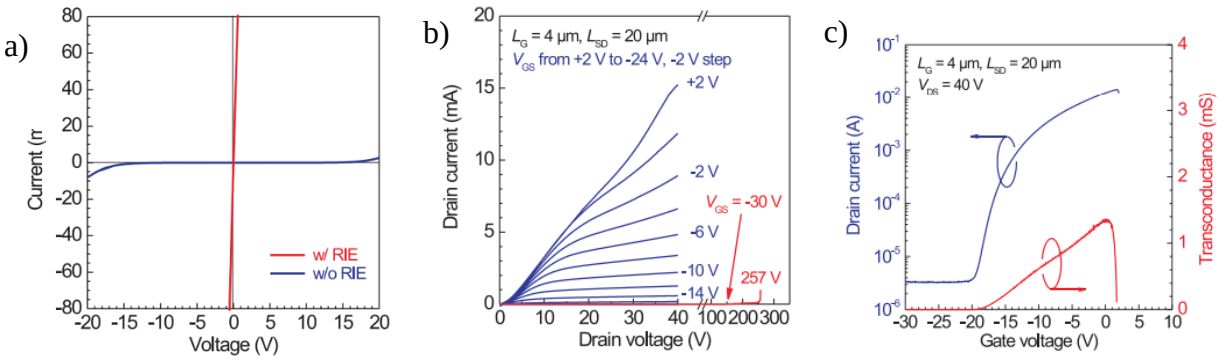


Figure 1.7 Electrical characteristics of fabricated MESFETs. Reproduced from [21], with the permission of AIP Publishing.

As a solution to the problems involved with the MESFETs described here, depletion-mode MOSFETs were also developed by Higashiwaki's group [5]. The first version relied on a Sn-doped channel; however this led to problems reproducing the doping profile, so the group switched to Si^+ implantation. This device has the same cross sectional schematic as shown in Fig. 1.6b, but with Si doping instead of Sn. All the device characteristics were the same or slightly improved with the switch to Si. The maximum I_d was 65 mA mm^{-1} at V_g = – 6 V, with a three-terminal off-state V_{br} was 415 V at V_g = -30 V. The I_d on-off ratio was about ten orders of magnitude at V_d = 30 V, with a maximum transconductance of 3.6 mS mm^{-1}. In addition, the device was capable of stable operation at temperatures of up to 250 °C.

With the work done to establish HVPE processes for β-Ga_2O_3, work on industry scalable Ga_2O_3 Schottky barrier diodes (SBDs) was able to move forward [5]. A thin layer of Si-doped n^--Ga_2O_3 was grown through HVPE on n^+-Ga_2O_3 (001) substrates. By simultanesously suppyling $SiCl_4$ as a *n*-type dopant gas during the HVPE process, the effective dopant concentration was able to be controlled. The two devices fabricated had $N_d - N_a$ of 1.4 x 10^{16} cm^{-3} and 2.0 x 10^{16} cm^{-3}, and a R_{on} estimated to be 3.0 mΩ*cm^2 and 2.4 mΩ*cm^2, respectively. These devices had ideality factors very close to 1, and had a high V_{br} of around -500 V [5].

1.2 GALLIUM OXIDE NANOWIRE PROPERTIES AND DEVICES

An attractive feature of nanowire-based devices is the electron transport properties. Since nanowires are considered quasi-one dimensional structures, electrons behave very differently than traditional planar MOS devices and bulk systems. There are several approaches to calculating this phenomena, but a general model has yet to be developed. Granzer et al. worked to develop an empirical model based off the available literature for Si nanowires, but as they mention, "While qualitatively, the majority of methods delivers the same general trend of carrier mobility versus [Si nanowire] diameter, quantitatively the calculated mobility values can differ considerably between the individual approaches, even if the considered [nanowire] structures are comparable [22]." They then point out that not only do the calculated mobility values greatly differ from the measured values, but there is little data for Si nanowires with diameters below 10 nm. In addition, as the diameter increases the experimental data spreads, further muddying the picture. They conclude that a clear picture of how electron mobility is affected by the geometry of a Si nanowire is not available [22].

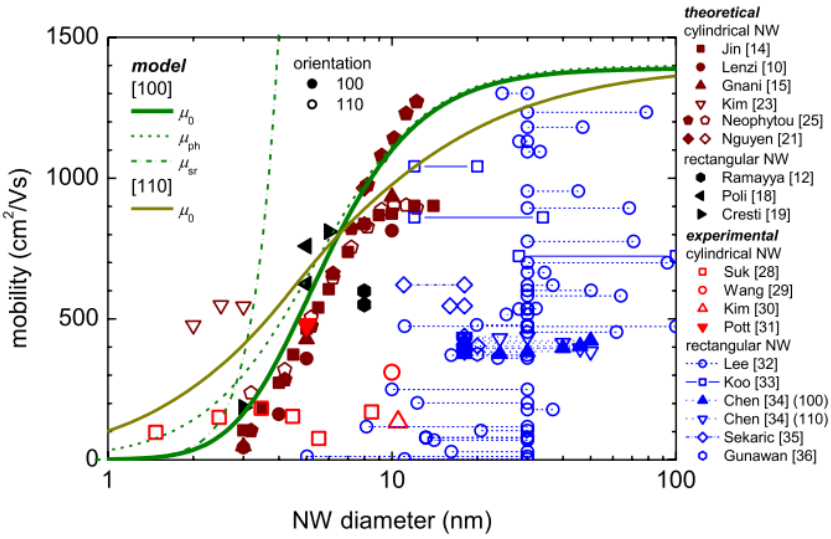


Figure 1.8 Nanowire diameter vs electron mobility theoretical and experimental results. 2014 IEEE. Reprinted, with permission, from R. Granzner, V. M. Polyakov, C. Schippel, F. Schwierz, and S. Member, "Empirical Model for the Effective Electron Mobility in Silicon Nanowires," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 1–7, 2014.

While this data is derived specifically for Si nanowires, it can readily be applied to other materials as a first order approximation. Bulk mobility in Si is listed in Table 1.1 as 1,400 cm^2/Vs, and as can be seen from Fig. 1.8, the models suggest that the values approach bulk mobility as the diameters approach 100 nm. This shows that nanowire based devices should not have any loss of conduction with proper preparation and diameter control.

β-Ga_2O_3 nanowires have been produced through several methods. These include: physical evaporation [23], laser ablation [24], carbothermal reduction processes [25], microwave plasma assisted [26] and traditional CVD processes [27–29], among others. Although these are all viable methods for research, the focus of this work will be on CVD, specifically VLS mechanisms, due to its ease of scaling up for industry.

Successful FETs have been fabricated by Chang et al. in 2005 and Li et al. in 2008. Chang's group grew Ga_2O_3 through a traditional vapor-liquid-solid mechanism, which will be discussed later in this work. They used pure Ga metals as their source material, with Au catalysts with an O_2/ 2% Ar flow at 920 ^oC [6]. The as-grown wires exhibited almost no current (below 1 pA) at room temperature and at bias voltages up to 30 V. Since β-Ga_2O_3 is intrinsically *n*-type, they elected to use Zn as a *p*-type dopant. Zn ions are very similar in size to Ga ions, 0.074 nm for Zn^{2+} and 0.062 nm for Ga^{3+}. Doping took place by placing the Zn source adjacent to the substrates with grown wires in a furnace at 450 °C for one hour with an inert Ar atmosphere.

After doping, the wires were then dispersed into isopropyl alcohol and deposited onto a *p*++ silicon chip with a 200 nm SiO_2 layer on top. Electrodes of 20 nm Ni and 300 nm Au were then fabricated onto the chip with traditional photolithography techniques to probe individual nanowires. These FETs exhibited *p*-type semiconducting characteristics, proving that the Zn dopants had been incorporated into the β-Ga_2O_3 lattice. Their FET measurements are shown below in Fig. 1.9.

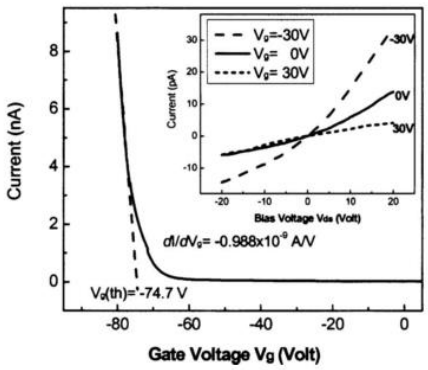


Figure 1.9 Gate voltage vs drain-source current for fabricated FET. Reproduced from [6], with the permission of AIP Publishing.

Characterization revealed these FETs had a threshold voltage $V_g(th)$ = -74.7 V and a transconductance of -0.988 nA/V [6]. Martel et al. developed estimations for carrier concentration and carrier mobility in *p*-type quasi-one dimensional systems on SiO_2 in 1998, given below in Equations 1.2 and 1.3:

$$p = \frac{V_g(th)}{e} . \frac{2\pi\varepsilon\varepsilon_o}{\ln(\frac{2h}{r})} \quad (1.2)$$

$$\mu_h = \frac{dI}{dV_g} . L \frac{ln\left(\frac{2h}{r}\right)}{2\pi\varepsilon\varepsilon_o} \quad (1.3)$$

Where *h* is the height of the insulating layer, *r* is the radius of the nanowire, *L* is the length of the nanowire channel and ε is the permittivity of the SiO_2 [30]. Although their work was initially on single-wall carbon nanotubes, it still serves as a good first order estimation for β-Ga_2O_3 devices. Chang et al. estimated their FETs to have p = 5.3 x 10^8 cm^{-1} and μ_h = 3.5 x 10^{-2} cm^2/Vs. This mobility is much lower than reported mobility for GaN devices, but is consistent with previous calculations of hole effective weights in β-Ga_2O_3 [2].

Li et al. fabricated *n*-type β-Ga_2O_3 nanowire FETs through a novel high-frequency inductive heating method [31]. Their growth substrate was prepared by mixing Ga_2O_3 and graphite powders in ethanol and then mixing and drying. Once dried, the powder was dispersed over their silicon substrates and placed in a quartz tube furnace. The furnace was then heated at an applied frequency of 11.7 MHz. Growth was carried out at 600 ^oC and a pressure of ~ 0.01 Torr for 3-5 min. They found this process resulted in randomly distributed nanowire growth over the substrate, with diameters ranging from 20-40 nm and lengths on the order of microns.

Their as grown nanowires were then sonicated into ethanol and dispersed onto a substrate with pre-patterned Au electrode pairs (separating distance 2 μm) to form FETs. After annealing in an Ar environment at 700 ^oC for 5 min, they electrically characterized these devices. They applied

gate voltages from 0 to 7.5 V with drain voltages from – 0.5 to 0.5 V as shown below in Fig. 1.10. It was abundantly clear that increasing the gate voltage increased the conductance, indicating the wire was *n*-type. In addition, the on-off current ratio was more than 10^5 at V_G from 0 to 7.5 V at V_{DS} = -0.2 V. Finally, the mobility of the channel was found to be 65.4 cm^2/Vs, which is comparable to previously reported GaN nanowire based devices.

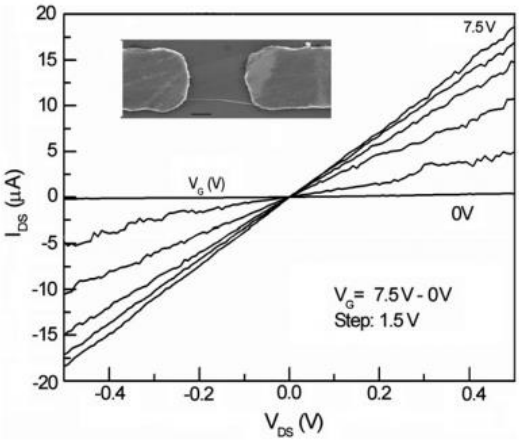


Figure 1.10 Voltage vs Current for fabricated FET. Reproduced from [31], with the permission of John Wiley and Sons.

Another application that is benefiting from nanowire incorporation are high sensitivity gas sensors. Nanowires' extremely high surface/volume atomic ratios make them extremely sensitive to surface effects, which is ideal for high-sensitivity gas sensors**.** β-Ga_2O_3 nanowires are attractive candidates for gas sensors for their ability to sense oxygen at high temperatures in addition to their sensitivity to reducing gases. One example of these sensors are the devices fabricated by Arnold et al. in 2009 [32].

Interdigital capacitor (IDC) gas sensors sense gasses through changes in capacitance of interdigital electrodes. Arnold et al. fabricated simple IDC sensors that function at room

temperature and have reversible responses to acetone and methanol, with limited responses to some hydrocarbons [32]. They fabricated platinum interdigital electrodes through traditional photolithography techniques, followed by a deposition of Au thin film. They then grew a mesh of β-Ga_2O_3 through basic VLS techniques. This resulted in a dielectric mesh on top of the platinum electrodes. By applying a voltage to these electrodes, the mesh of nanowires is polarized. A gas is then passed over the device which may physisorb onto oxygen defect sites on the nanowires. This directly affects the dielectric of the mesh, which changes the capacitance of the platinum electrodes, as seen below in Fig. 1.11. These are a fine example of simple, easy to operate devices that are grown via VLS. These gas sensors have a very fast cycling time and operate at room temperature.

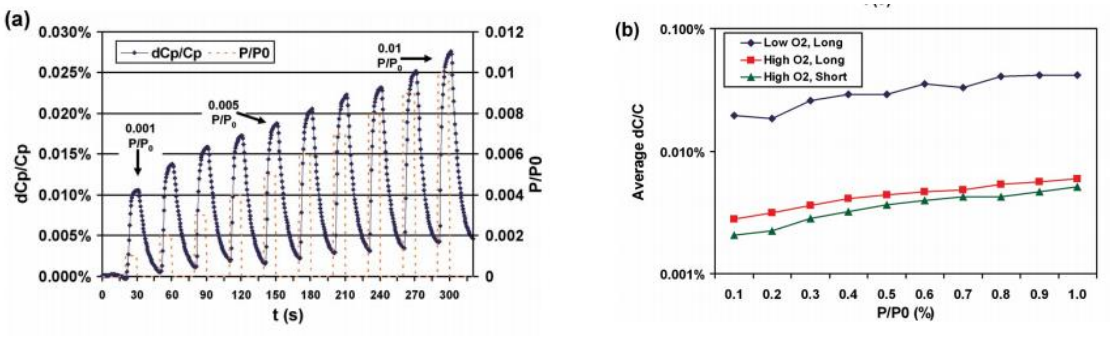


Figure 1.11 Electrical Characteristic of fabricated nanowire gas detector. 1.11a shows the change in capacitance vs time. 1.11b shows the average change in capacitance vs the gas concentration. Reproduced from [32], with the permission of AIP Publishing.

Due to its extremely large bandgap β-Ga_2O_3 has also attracted a lot of attention as a possible material for solar-blind photodetectors. Earth's stratospheric ozone absorbs light with wavelengths below 290 nm. Any device that can detect signals of wavelengths in that range can be used for a multitude of communications applications along with several military endeavors. β-Ga_2O_3 strongly

absorbs light at 254 nm making it an ideal candidate, as demonstrated by Feng et al. in 2006 [33]. They grew β-Ga_2O_3 nanowires through a typical VLS process and then placed individual wires on top of pre-patterned Au electrodes on a 500 nm SiO_2 layer. These devices were then tested at 10^{-4} Torr at room temperature, with promising results. The dark current of these devices were on the order of pA, with illumination currents jumping up to several nA very quickly. They measured the response time to be less than 0.22 s, and the slowest recovery time to be 0.09 s. These measurements are given below in Fig. 1.12.

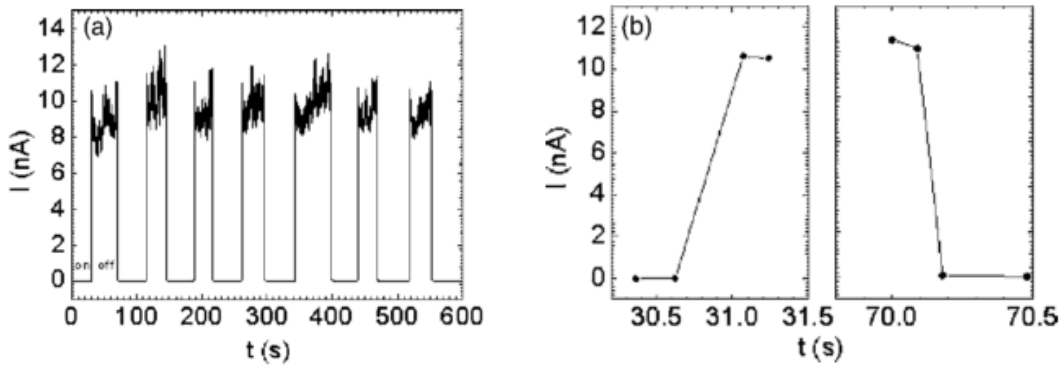


Figure 1.12 Current vs time for nanowire photodetector. 1.12a shows the on/off states exposed to 254 nm light, 1.12b shows an enlarged "on" rise (right) and enlarged "off" decay (left) Reproduced from [33] with the permission of AIP Publishing.

Typically, photodetectors of this nature usually suffer from large dark current and long recovery times. Other metal oxide nanowire devices (ZnO, In_2O_3) have been measured with response times > 10 s and recovery times of >200 s. These β-Ga_2O_3 nanowire based devices have excellent response and recovery times, and the only issues reported so far are attributed to the poor contacts between the wires and electrodes, indicating a large potential for manufacturability with the right electrode materials.

1.3 CONCLUSIONS

Gallium oxide has a multitude of potential applications across multiple fields. It's large bandgap and large breakdown field make it an exciting candidate for high voltage power devices. Gallium oxide nanowires have also been implemented in several devices, and are the focus of this work. However, a lack of consistent fabrication techniques has extremely limited device production and testing. Discovering how to best grow the nanowires as well as establishing new techniques for fabricating nanowire based devices is paramount to further maturing the technology.

2.0 VAPOR-LIQUID-SOLID NANOWIRE GROWTH MECHANISM

2.1 INTRODUCTION

The first evidence of the vapor-liquid-solid (VLS) growth mechanism was put forward in 1964 by Wagner and Ellis as an explanation for silicon whisker growth [34]. Since then it has been extensively used for any unidirectional growth with a liquid mediating phase and precursors supplied from a vapor phase. In addition, it has been used as a basis to develop other growth mechanisms such as; vapor-solid-solid, vapor-adsorption layer-solid, solid-liquid-solid, among many others. Recently, VLS has been used as a quick and easy method for large scale growth of nanowires of various materials [35–37].

The basis of VLS is as follows, from Wagner's book *Whisker Technology*. "The surface of the liquid has a large accommodation coefficient and is therefore a preferred site for deposition. The liquid becomes supersaturated with material supplied from the vapor, and crystal growth occurs by precipitation at the solid-liquid interface. Unidirectional growth is the consequence of an anisotropy in sold-liquid interfacial energy [38]." The following sections explore some of the driving forces of VLS mechanisms in more detail.

2.2 BASIC SET UP

In a basic VLS set up, the target substrate is coated with a thin layer of a catalyst material. These catalysts are typically metals such as Au, Ni, Co and Fe that can form low temperature eutectic

systems with the growth materials [1]. Source materials are loaded into a furnace along with the prepared substrates. The furnace is then brought up to the desired growth temperature, melting the thin catalyst layer and evaporating the source material. The melted catalyst material beads up into small liquid droplets, and the evaporated source materials are then incorporated into the liquid. Once the liquid is supersaturated with the desired source material, the excess is deposited onto the liquid-solid interface, resulting in pillar like growth.

Wacaser et al. introduced clarifying terminology in their work on VLS mechanisms, which will be used henceforth in this paper [39]: The liquid phase is referred to as the *collector*, the vapor phase is the *supply*, the solid phase is the *crystal*, the atomic building blocks of the nanowire is the *growth species*, and the chemical complexes used to supply the growth species are the *precursors*. In addition, the one-dimensional growth is denoted as the *wire*, regardless of final geometry.

2.3 CHEMICAL THERMODYNAMICS OF NANOWIRE GROWTH

The defining characteristic of growth from a VLS mechanism is the collector remaining at the tip of the grown wires, as shown below in Fig. 2.1. To better understand the VLS mechanism then, the main questions to ask are: why does material get deposited below the collector, and what makes the wires grow in one direction? As Wacaser et al. point out, the bulk shape of these crystals do not have one dimensional symmetry, so unidirectional crystal growth must be due to something in the nanowire growth breaking the natural symmetry of the crystal [39]. The following sections will answer these questions while also shedding some light onto how the growth environment influences properties of the wires.

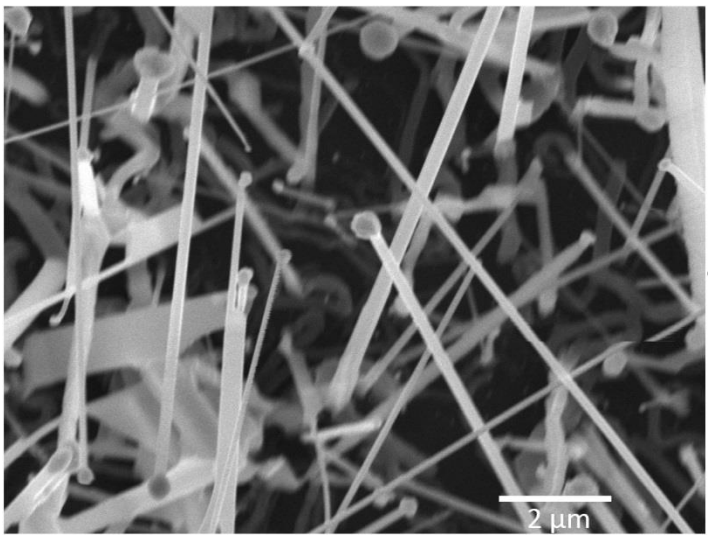


Figure 2.1 SEM image of as-grown β-Ga_2O_3 wires on a Si substrate, note the spherical Au collector tips on the wires. Scale bar reads 2 µm.

2.3.1 Accommodation into the collector

To understand what makes the collector such an integral part of this mechanism, an understanding of how incoming growth species interact with the phases already present is needed. This is quantified by the accommodation coefficient, which is defined as the fraction of the growth species that is actually incorporated into the phase in question. In the most basic case of mono-atomic three-phase systems, the liquid collector surface stays ideally rough even at low supersaturations, allowing for faster accommodation**.** A liquid surface is very different from a crystal surface and can be thought of as ideally rough, as Wagner wrote [38]. The liquid can be considered to be composed of ledges and steps that are perfect accommodation sites which are only atomic distances apart. At these low supersaturations, any growth species that land on the crystal will not be incorporated but will diffuse away, as is the case with atomic layer depositions, or desorb back into the vapor phase.

In VLS systems, however, the catalyst is not the same material as the growth species, and the growth species can be more than one material. The above arguments must now be adapted for accommodation into solutions, rather than homogenous liquids. In this case, the accommodation coefficient is now a function of the concentration of the growth species in the collector. If the collector becomes supersaturated with respect to the supply, then the steps of the collector will act as ideal desorption sites, rather than incorporating more material into the collector/crystal system. This leads to the thought that there is an upper limit to how high the concentration of growth materials can be in the collector while growth is still occurring. This is expressed by the inequality:

$$\mu_s \geq \mu_c \qquad (2.1)$$

where μ_s is the chemical potential of the supply, and μ_c is the chemical potential of the collector. If material is then transported from the collector to the crystal, then the total potentials of the system can be expressed as:

$$\mu_s \geq \mu_c \geq \mu_k \qquad (2.2)$$

where μ_k is the chemical potential of the crystal.

While this inequality holds true, the system is either in equilibrium, the potentials are equal, or growth species will be driven from the supply on to the collector. Supersaturation between two phases, i and j, can be expressed as:

$$\Delta\mu_{ij} = \mu_i - \mu_j \qquad (2.3)$$

If $\Delta\mu_{ij}$ is positive, then the i phase is supersaturated with respect to the j phase. Therefore, for accommodation into the collector to take place, then the difference $\Delta\mu_{sc}$ must be positive. If we examine this definition and apply it to the inequalities stated above, we arrive at the conclusion made by Wacaser [39] that:

$$\Delta\mu_{sk} \geq \Delta\mu_{sc} \qquad (2.4)$$

$$\Delta\mu_{sk} \geq \Delta\mu_{ck} \qquad (2.5).$$

This shows that the driving force for growth at the supply/crystal interface is larger than that for growth at the supply/collector interface and the collector/crystal interface, for ideal thermodynamic systems. To answer the question of what role the collector plays in VLS systems then, the fact that the growth species themselves need to form and are not directly supplied needs to be taken into account.

As discussed, typically during VLS growth the chemical potential of the growth species is higher in the supply phase, and lowest in the crystal phase, with the collector phase being between the two, as expressed by Equation 2.2. However, in systems where the growth species are either supplied via precursors that are chemical complexes or higher energy molecules, these precursors need to form the growth species. The incoming precursors see the collector as a lower chemical potential and thus begin to concentrate there. Once on the collector/supply interface the precursors favorably form the growth species. The growth species can then see the collector as a local maximum of concentration and chemical potential, and tend to move to the area of the lowest free energy to nucleate. In these cases, the collector acts as a catalyst. The collector is then shown to be integral for nanowire formation, as the growth species will not favorably form on the bare substrate. This catalysis process has been investigated by Wacaser et al. in their work on the VLS mechanism and has been put forward as a candidate for the explanation of nanowire growth [39]. Now that the collector's role has been explored, the question that remains is why wire growth takes place exclusively on the collector/crystal interface.

2.3.2 Nucleation

There are four important boundaries in a VLS system: supply/collector; supply/crystal; collector/crystal; and supply/collector/crystal, the three phase boundary (TPB) where the supply, collector and crystal all meet. From an overarching view, it can be stated that wire growth is achieved through suppressing nucleation at the supply/crystal and supply/collector interfaces, and encouraging nucleation at the collector/crystal and TPB. These two possible nucleation models are shown below in Fig. 2.2.

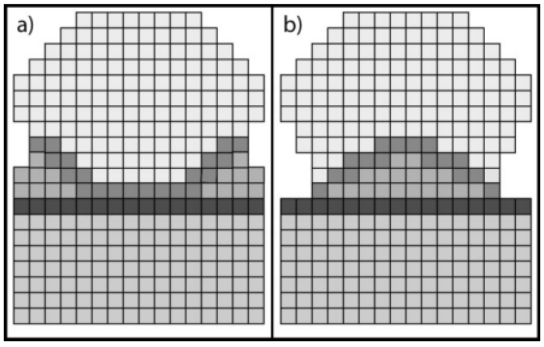


Figure 2.2 Schematic of two possible nucleation methods. 2.2a shows nucleation at the three phase boundary. 2.2b shows nucleation at the collector-crystal interface. Reproduced from [39], with the permission of John Wiley and Sons.

Wacaser's work derived expressions for the Gibbs free energy of nucleation at different interfaces:

$$\Delta G_{sk} = -n\Delta\mu_{sk} + Ph\sigma_{sk} \quad (2.6)$$

$$\Delta G_{ck} = -n\Delta\mu_{ck} + Ph\sigma_{ck} \quad (2.7)$$

$$\Delta G_{TPB} = -n\Delta\mu_{sk} + P_{ck}h\sigma_{ck} + P_{sk}h\sigma_{sk} \quad (2.8)$$

where n is the number of atoms at the interface, P is the perimeter length of the specific interface, h is the height of the initial nucleus and σ is the surface energy of the interface [39]. Since a lower Gibbs free energy corresponds to the preferential nucleation site, to initiate wire growth maximizing ΔG_{sk} while minimizing ΔG_{ck} and ΔG_{TPB} is necessary.

Since the supersaturations of the phases are more or less constant for given growth parameters, the surface energies are what need to be investigated. These surface energies are heavily influenced by the wetting angle of the collector, as explained by the Gibbs-Thomson effect. If there are strong interactions between the collector and the crystal, then the wetting angle is small and the supply/crystal energy will be higher than the collector/crystal, favoring nucleation at the collector/crystal interface. If there are weak interactions, then the wetting angle is large and the supply/crystal energy will be higher than the collector/crystal, making wire growth less favorable.

As discussed above, the wetting angle of the collector heavily influences wire growth. As the Gibbs-Thomson relationship implies, an increase of curvature of a liquid increases the chemical potential of the liquid. This heavily suggests a minimum collector radius that allows wire growth. Wagner and Ellis were the first to observe this phenomenon and they empirically derived Equation 2.9:

$$R_{min} = \frac{2\Omega_l \gamma_{lv}}{k_B T \, ln(\Phi+1)} \qquad (2.9)$$

where Ω_l is an elementary volume in a liquid drop; γ_{lv} is the surface energy on the collector-supply interface; Φ is the supply supersaturation and $k_B T$ is the average thermal energy [40]. This has since been derived theoretically by Dubrovskii in 2012 [40].

For nucleation at the TPB, required conditions are a bit simpler. The supersaturation of the growth species is at its highest at the TPB because it is in contact with a constant source of growth species, the supply. Nucleation will not be favorable until this condition is met, otherwise any

growth species at the TPB will be incorporated into the collector. Wacaser et al. suggested the TPB in VLS systems could be the preferred nucleation site for growth species. They claimed that the nucleus shape and position will adjust to minimize ΔG, minimizing Equation 2.8 and making the TPB the most preferential nucleation site [39]. This was corroborated by other groups for the case of nucleation and growth of water crystals from water and water vapor, but as Wacaser points out, the collector phase was inert, and as such more research is required to confirm this for the more dynamic nanowire system.

This all leads directly to an answer to the second question: what makes the wires grow in one direction? For nucleation and growth steps as described above, growth of the wire will proceed perpendicular to the collector/crystal interface. This interface will orient itself such that the interfacial energy is minimized, resulting in unidirectional growth. However, during growth the collector/crystal interface is usually mobile, which will result in aligned wires. This mobility can be a candidate for the cause behind some observations of thin layers of amorphous growth species before crystallization [41]. However, there are factors which can limit the mobility of this interface as Wacaser et al. write: "These exceptions can be grouped into four different groups depending on why the nanowires do not grow perpendicularly to the lowest energy facet. i) There is a lack of mobility of the collector. The nanowire then grows in the direction of the original interface. ii) Multiple facets are present at the collector crystal interface; the interface is not flat. iii) The side facets of the nanowires are not always perpendicular to the collector/wire interface, so that as the nanowire grows the collector/wire interface progresses in both the growth direction and a lateral direction. iv) The relative surface free energies are not what might be conventionally expected due to interactions between the materials, or even the small size of the interfaces [39]."

2.4 CONCLUSIONS

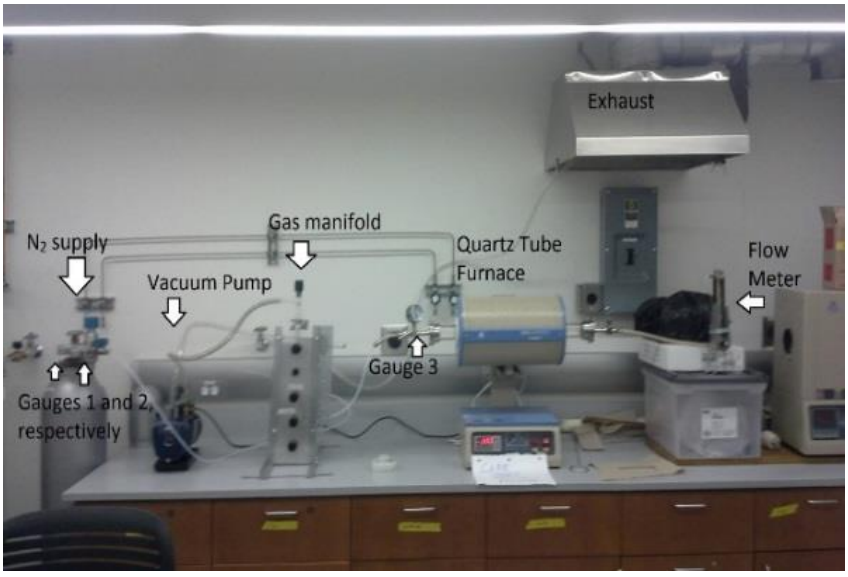
Vapor-liquid-solid (VLS) growth of nanowires is a simple and reliable fabrication method. However, the underlying mechanisms are still being investigated. Gaining a better understanding of how to better control the formation of the grown wires is essential for developing producible electronic devices. As seen, the growth of nanowires via VLS is highly dependent on several factors: movement of the growth materials from the source to the growth substrate, the growth environment, the reaction kinetics and thermodynamic behavior of all three phases, and finally the pressure and temperature of this system. In order to better understand the formation of β-Ga_2O_3 nanowires via VLS, this work investigates the effects of the most easily controlled of the above factors, the pressure and temperature.

3.0 EXPERIMENTAL NANOWIREGROWTH

3.1 EXPERIMENTAL SET UP

This research uses a typical quartz tube furnace to implement VLS growth of β-Ga_2O_3 nanowires. The crystal is a (100) silicon wafer with an adhesion layer of 2 nm of Ti followed by a 10 nm of Au for the collector, deposited onto the wafer by electron beam evaporation. The precursors are elemental gallium (99.99% Arcos Organics) and background oxygen. The growth is carried out in a nitrogen environment to ensure the cleanest conditions possible. The entire growth apparatus is shown below in Fig. 3.1a with the temperature profile of the furnace at 900 ^oC growth temperature shown in 3.1b. This profile clearly shows a flat temperature level near the center of the tube. In Fig. 3.1c, a schematic of the quartz substrate holder is shown. Cut substrates are placed in the first and third rows of the holder, with the gallium precursor in the second.

a)



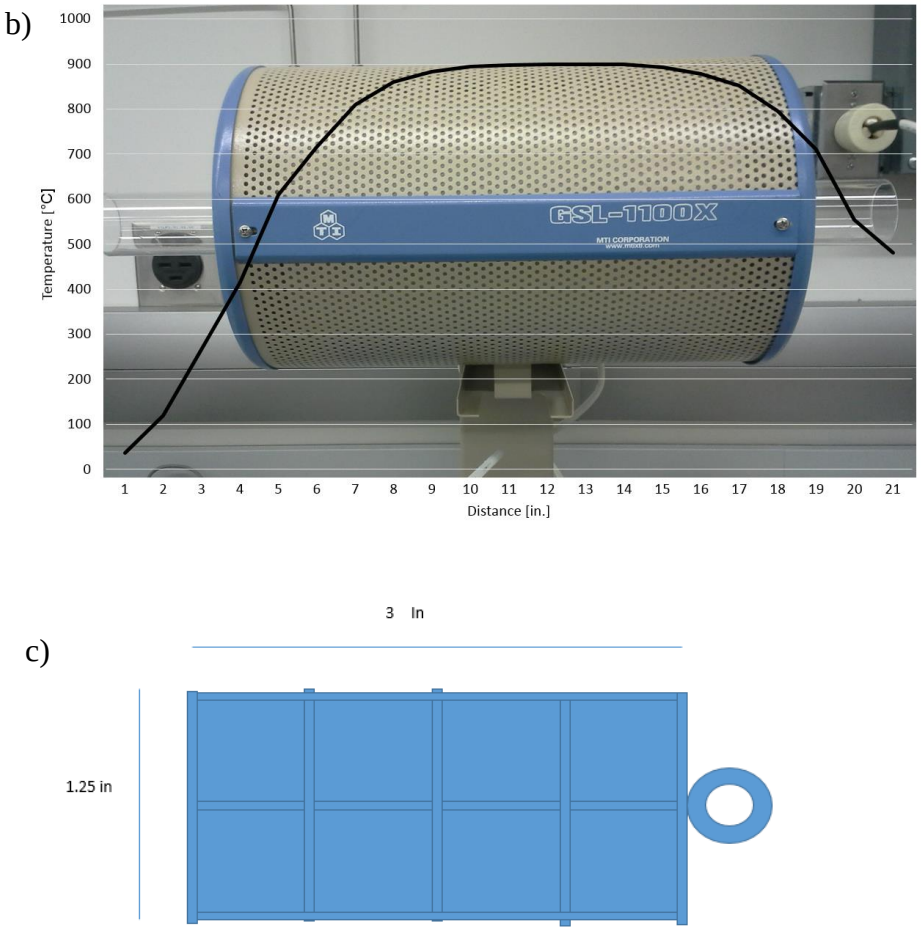


Figure 3.1 3.1a shows the entire growth apparatus. 3.1b shows the temperature profile of the used tube furnace at T = 900 ºC. 3.1c shows a schematic of the quartz substrate holder used in this work.

3.2 PROCEDURE

After loading the cut substrates and precursors, the holder is placed in the furnace in the constant temperature area. Once in place, a flow of ultra-high purity nitrogen is established through the furnace at a flow of 0.5 s.l/min and a pressure of 0.11 MPa for 10 min. Then the furnace is purged and refilled to atmospheric pressure with nitrogen, and then this cycle is repeated. Finally, another flow of nitrogen is established at a flow of 0.5 s.l/min and a pressure of 0.11 MPa for 10

min. Once this cleaning procedure has finished, the furnace is evacuated to the desired pre-growth pressure level and sealed, and then the temperature cycle begins. The oxygen precursors are supplied through the remnants of ambient air. Very small amounts of oxygen left over in the reaction will result in oxidizing of the wires, forming Ga_2O_3 [42, 43].

The temperature cycle at the furnace center is shown in Fig. 3.2. The furnace first ramps up to 105 ^oC over 35 minutes and is held there for 15 min. This is intended to drive any residual water vapor from the system. The temperature is then raised to 500 ^oC over 20 min and held there for 10 min. This is to stabilize the entire system just below the growth conditions. Finally, the temperature is raised to the desired growth temperature over 25 minutes and held there for an hour. After the growth is finished, the furnace is allowed to cool to ambient.

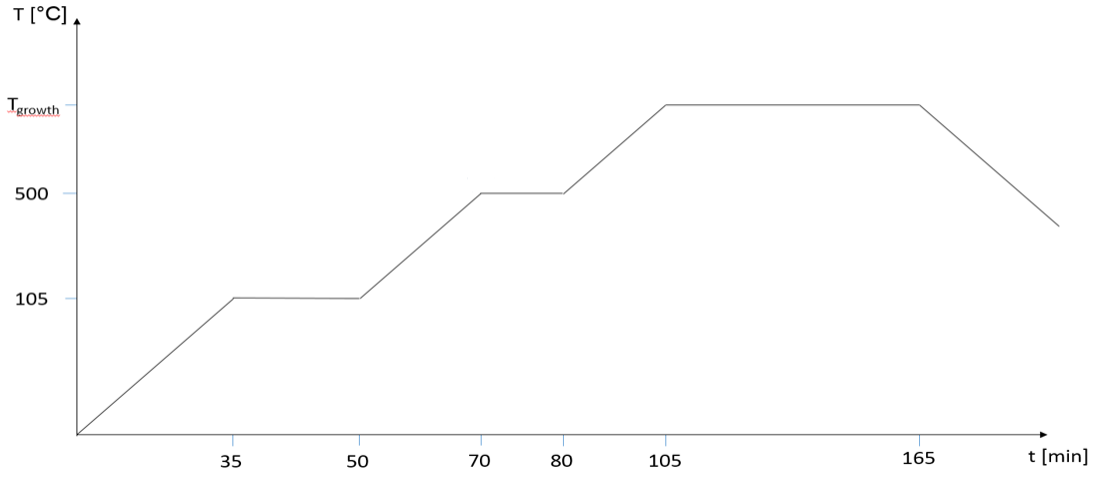


Figure 3.2. Temperature cycle used for nanowire growth in the furnace.

Due to the nature of our experimental set up, growth parameters are classified by the initial evacuation pressure rather than the growth pressure. The final growth pressures for different growth temperatures and initial evacuation levels are given below in Table 3.1. This work investigates five different growth temperatures and five different initial pressures.

Table 3.1 Approximate growth pressures in MPa achieved for given growth pressure and initial evacuation pressure.

	0.01 MPa	0.02 MPa	0.03 MPa	0.04 MPa	0.05 MPa
650 ºC	0.017	0.038	0.063	0.083	0.110
700 ºC	0.020	0.040	0.065	0.088	0.115
750 ºC	0.021	0.043	0.067	0.095	0.118
800 ºC	0.022	0.045	0.070	0.100	0.124
850 ºC	0.023	0.049	0.077	0.105	0.130

4.0 GROWTH RESULTS AND ANALYSIS

4.1 INTRODUCTION

Using the procedure discussed in Chapter 3, nanowires have been grown at several different pressure and temperature combinations. This chapter examines the result of these growths and categorizes the conditions based on the resulting wires. In addition, the wire materials are analyzed and confirmed, as well as the crystallographic constants to confirm the phase of the grown material. Finally, insight into the possible nucleation methods of the wire growth are discussed.

4.2 RESULTS

Samples of substrates grown at the relevant temperature/pressure combinations are shown in Fig. 4.1. For ease of reference, the temperature/pressure combinations are labeled 1 through 25, as seen in the upper left corner of each image. Of the 25 investigated temperature/pressure combinations, some degree of wire growth was achieved for all of them except three: samples 3, 4 and 5. All of these growth results are extremely consistent and exhibit the same growth characteristics throughout several different runs. The samples of grown nanowires are separated into two categories: short wires with lengths on the order of 1 μm, Type I; and longer wires with lengths on the order of several tens of μm, Type II. Substrates with no wire growth are outlined in

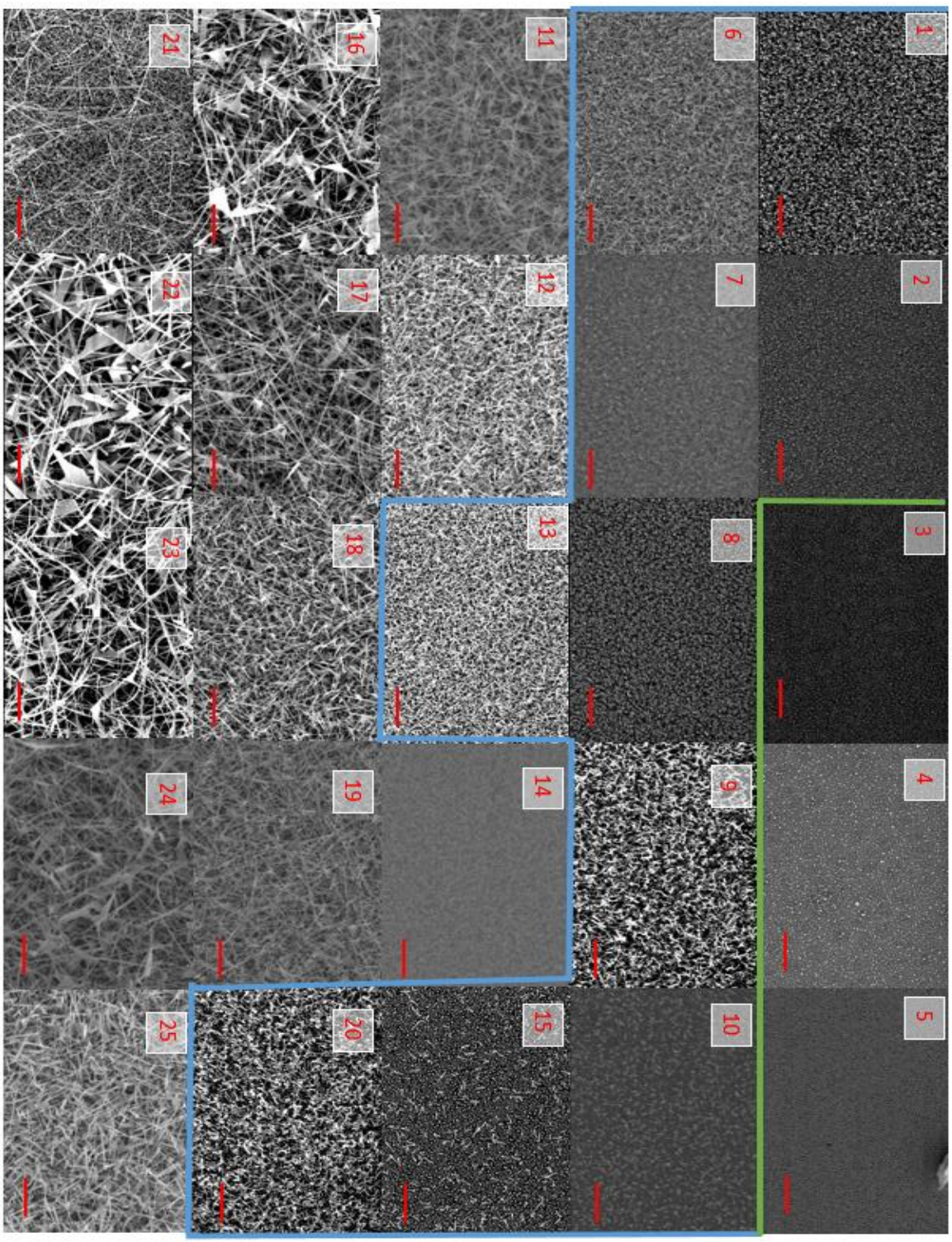
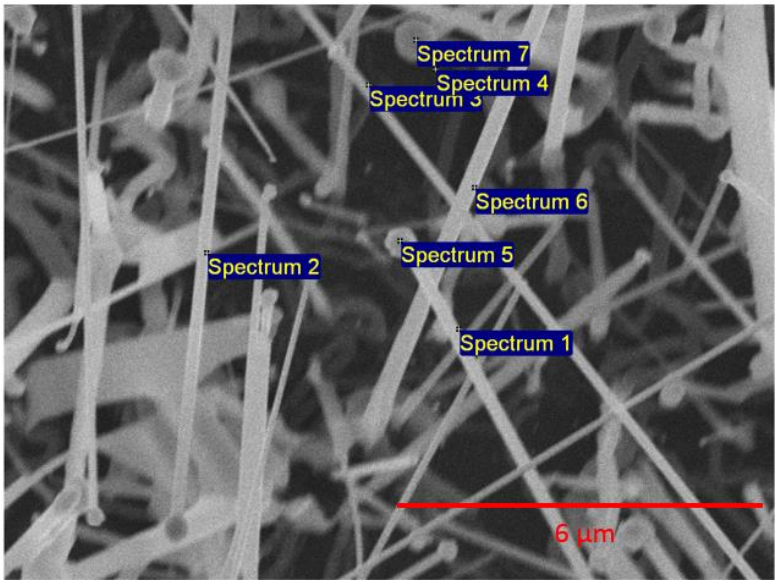


Figure 4.1 Examples of substrates grown at each growth condition. Scale bars all indicate 10 μm

green (upper right corner of Fig. 4.1). Type I wires are those in Fig. 4.1 that are separated on the upper side by the green line and by the blue line on the lower side, with the rest of the substrates being Type II wires.

Both Type I and II wires have diameters on the order of 200 nm. This similarity is directly due to the influence of the collector on the diameter of the wire. Regardless of whether nucleation takes place at the three phase boundary or the collector/crystal interface, the collector defines these interfaces and will determine the diameter of the wire. Furthermore, what influences the diameter of the collector is the amount of material present in each collector. Since the collectors in question are formed through the melting of a thin film, the diameter size distribution is based on how thick these films are. However, of the substrates analyzed, Type I wires have a larger average size. This disparity is likely due to the fact that the Type II wires that can be imaged are the longer, thinner wires that make it to the top of the substrate.

All Si substrates used in this work are prepared as described in Chapter 3, with a collector layer of 2 nm of Ti and 10 nm of Au. Since all substrates have the same film thickness, they will all exhibit wire growths with similar diameters. Grown wires were confirmed to be Ga_2O_3 through energy-dispersive X-ray spectroscopy (EDX) analysis, and were further confirmed to be β-phase through TEM analysis.



Spectrum	O	Si	Ga	Au	Total
Spectrum 1	25.34	45.57	29.09	0.00	100.00
Spectrum 2	29.05	29.96	40.99	0.00	100.00
Spectrum 3	19.94	59.01	21.05	0.00	100.00
Spectrum 4	20.81	79.19	0.00	0.00	100.00
Spectrum 5	0.00	0.00	19.82	80.18	100.00
Spectrum 6	22.43	38.17	39.40	0.00	100.00
Spectrum 7	0.00	0.00	100.00	0.00	100.00

Figure 4.2 Energy-dispersive X-ray Spectroscopy results of grown wires. Scale bar reads 6 µm.

As EDX analysis shows in Fig. 4.2, the high amounts of Ga and O confirms that the wires grown are Ga_2O_3. The ratio of measured Ga:O is not exactly 2:3 due to the thin native oxide layer of the Si crystal as well as remaining collectors that collected Ga without growing wires, that are present underneath the grown wires. The high amount of Si comes from the crystal background and the small amounts of Au present account for the collectors present in the substrate.

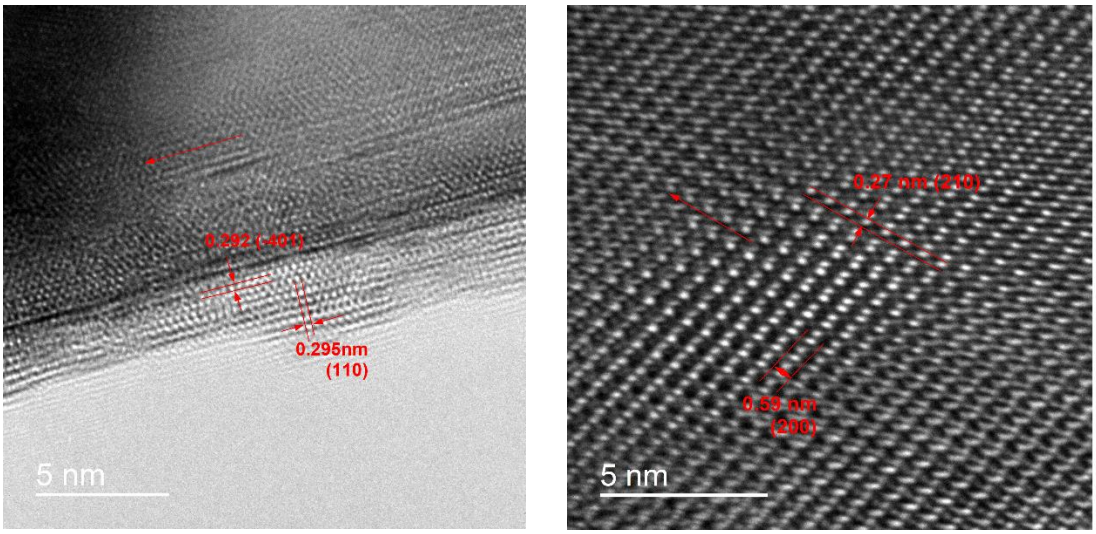


Figure 4.3 Transmission electron microscopy images of a grown Type II wire, showing crystallographic spacings of the (-401), (110), (210) and (200) planes. Scale bars both read 5 nm.

A grown wire sample was imaged and characterized via TEM, shown above. The growth directions of the wires are indicated by the red arrows, along with various plane spacings. Planes indicated are ($\bar{4}$01), (110), (210) and (200) with spacings of 0.292, 0.295, 0.27, and 0.59 nm, respectively. These results confirm the single crystal nature and β-phase of theses Ga_2O_3 nanowires.

4.2.1 Type I wires

Type I wires were observed for all growths at 650 and 700 °C, as well as for growths 13, 15 and 20. Most growths exhibited extremely dense wire growth, with the exception of growth 15. Growth 15 shows a lot of potential wire sites with a few isolated wires grown, and serves as clear image of individual wires. Using this image, it was determined that for wires of this type the average length was 2.025 ± 0.360 μm, with an average diameter of 210 ± 46 nm.

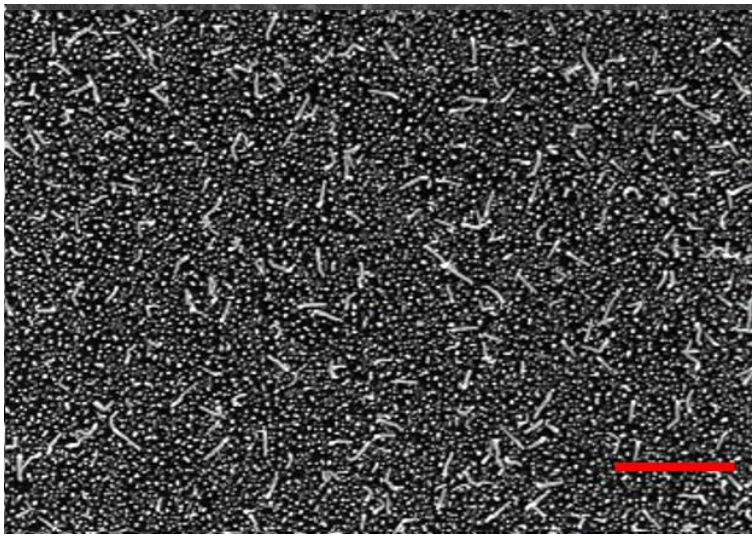


Figure 4.4. Beginning of wire growth, sample was grown at T_g = 750 °C, P_{evac} = 0.05 MPa. Scale bar shows 10 μm

An illuminating example of how the growth pressure of the system affects wire growth is seen by comparing growths 1 and 2. Both of these samples were grown at 650 °C, but from Table 3.1, growth 1 was grown at 0.017 MPa, while growth 2 was grown at 0.038 MPa. Growth 2 has minimal wire growth, and the wires that are present have extremely small lengths. Growth 1 on the other hand has much denser wire growth, in addition to a much higher average length. There are two different factors that the growth pressure effects. The higher pressure of growth 2 makes the liquid collector have a smaller radius of curvature [44] which makes the needed chemical concentration for successful growth to be higher. In addition, the higher pressure greatly reduces the amount of Ga that makes it to the growth substrate. Ga has an extremely low vapor pressure, so this higher environmental pressure will drastically reduce the amount of vapor Ga in the growth system.

This pressure influence is also clearly represented by growths 6 through 10, reshown below in higher resolution. All of these take place at the same growth temperature, 700 °C, but get less and less dense as the growth pressure increases. In addition, lower growth pressures seem to allow

for longer wire growths, which is consistent with the amount of Ga precursors that will make it to the collector.

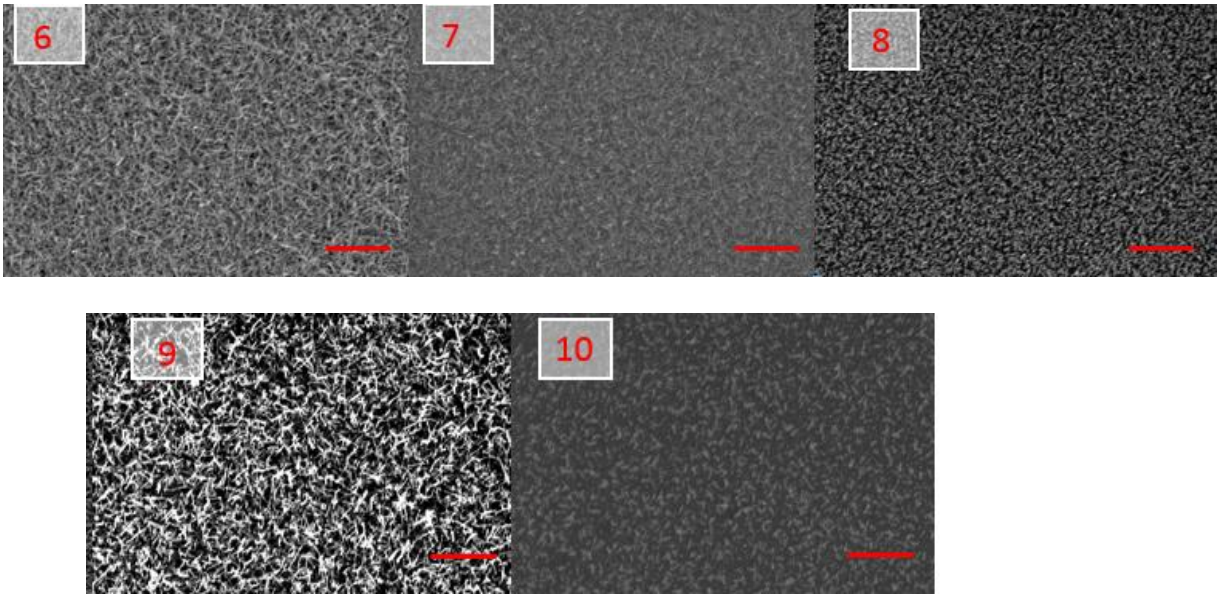


Figure 4.5. Growths 6 – 10, reprinted for convenience. All scale bars indicate 10 μm.

To test the influence of the gas flow on wire growth, two separate growths were conducted. One kept a flow of N_2 at 0.105 MPa throughout, and the other kept the N_2 flow only until 500 °C, at which point the flow was stopped and the furnace was evacuated to a pressure of 0.07 MPa, which was previously known to raise the growth pressure to the required 0.105 MPa at the growth temperature of 850 °C. Samples of both of these growths as well as a sample from growth 24 are shown in Fig 4.6. As is evident that are little to no discernable differences between the samples, confirming that the sealed tube method used here produces identical wires to more traditional VLS growths with much less gasses used.

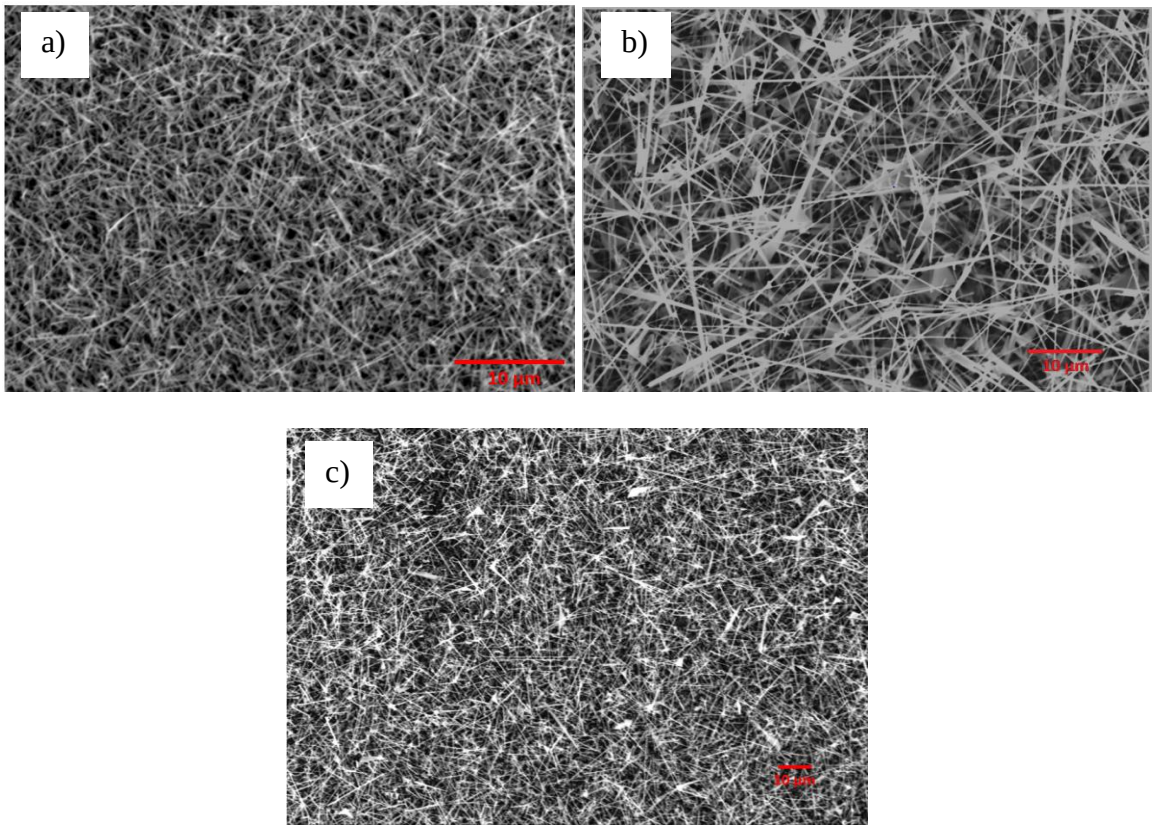


Figure 4.6. Examples of substrates grown with different flow conditions at the same growth temperature and pressures. 4.6a shows growth done with a flow throughout. 4.6b shows growth with a paused flow midway through. 4.6c shows standard sealed tube growth. All scale bars indicate 10 μm

4.2.2 Type II wires

Type II wires were grown at all conditions for 850 °C, growths 16-19 for 800 °C as well as growths 11 and 12 for 750 °C. As discussed previously, these wires tend to have diameters on the same order as Type I, although several times longer. Type II wires were measured to have diameters of 242 ± 62 nm. The high standard deviation in the measured diameter are due to the large number of possible diameters, seen below for a sample grown at growth condition 24. In addition, due to the number of layers of wires, the only wires able to be imaged are the longest wires, limiting the sample size.

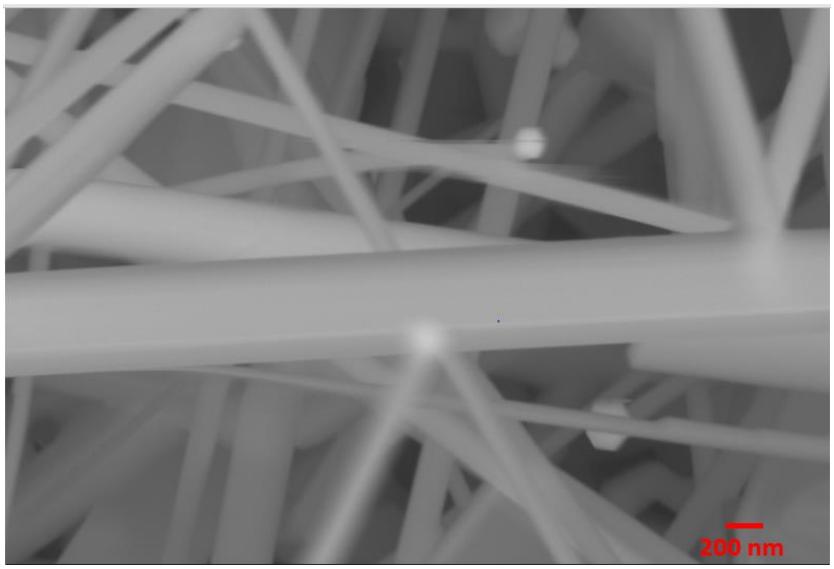
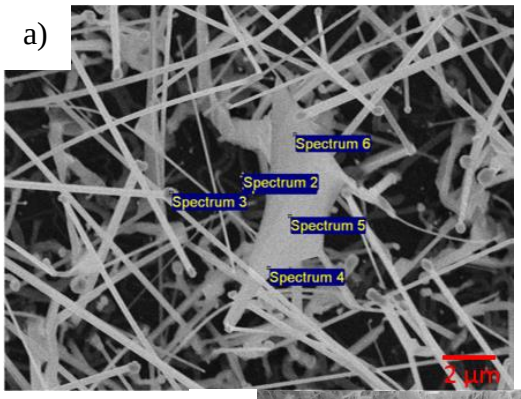


Figure 4.7 High resolution SEM of grown Type II wires, showing an assortment of possible nanowire diameters. Scale bar reads 200 nm.

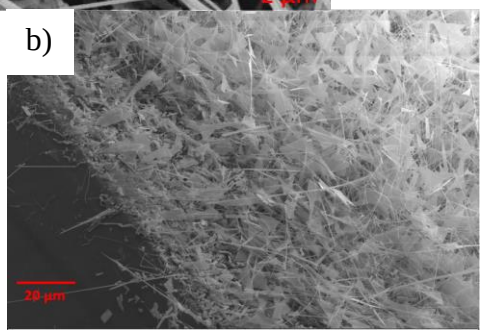
For type II wires, changes in temperature and pressure did not affect the apparent densities or lengths, but as temperatures increased and pressures decreased, more substrates exhibited sheets of material between wires. These sheets are highly concentrated near edges of substrates, and less so in the middle, as shown in Fig. 4.8. Initial EDX of these sheets show that they have a much higher concentration of carbon near their edges than surrounding areas, indicating that these might be Ga_2O_3 growths on a carbon matrix. However, more work is needed to characterize exactly what these sheets are. Since substrates are stored in the same environment and put through identical preparation and growth processes, in addition to the fact that sheets are observed in multiple different growth runs at the same growth conditions, individual contaminations seem a highly unlikely source of formation.

a)



Spectrum	C	O	Si	Ga	Au	Total
Spectrum 2	0.00	19.22	65.15	15.62	0.00	00.00
Spectrum 3	0.00	6.75	0.00	14.19	79.06	00.00
Spectrum 4	34.23	25.15	8.98	31.64	0.00	00.00
Spectrum 5	0.00	27.90	18.09	54.02	0.00	00.00
Spectrum 6	31.84	23.60	13.16	31.40	0.00	00.00

b)



c)

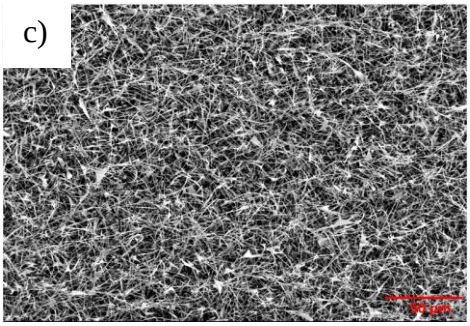


Figure 4.8. Examples of sheets observed for Type II wire growth. 4.8a shows EDX results, with noticeably higher C concentrations near the edges of the sheet, scale bar reads 2 µm. 4.8b shows examples of the higher concentrations of sheets near the edges of grown substrates, scale bar reads 20 µm. 4.8c shows examples of lower concentrations of sheets near the center of grown substrates, scale bar indicates 50 µm.

This trend of high temperatures and lower pressures increasing the concentration of sheets holds until the most extreme case of this work, growth 21. Growth 21 has a large amount of Type I wires, with a few extremely long Type II wires. In addition, it seems that there are no sheets present. This raises the possibility of these sheets forming through the joining of growth defects in adjacent wires. For substrates with much higher density growths of Type II wires, the sheets are commonplace, for growth 21 which has a much lower density of Type II wires, the sheets are not present.

4.3 NUCLEATION SITES

Further investigation into substrates with no wire growth revealed an interesting look at the possible nucleation process of these wires. A substrate was encapsulated into a carbon protection layer and then cut via focused ion-beam (FIB) milling to obtain a cross section of the solidified collector. This cross section was then imaged via high-resolution transmission electron microscopy (HRTEM), shown below in Fig. 4.9. The HRTEM image revealed the presence of Ga_2O_3 surrounding the now solid Au collector.

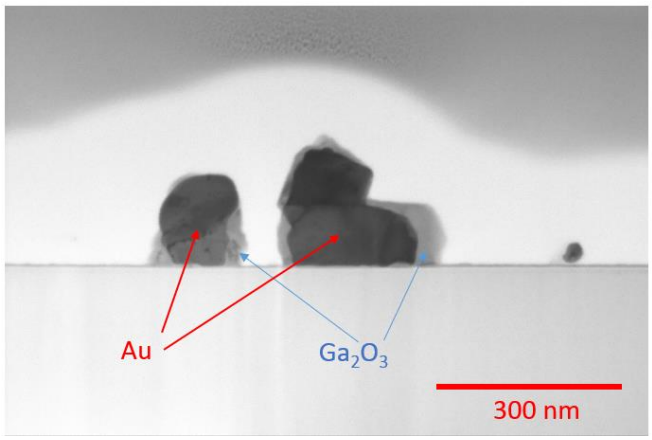


Figure 4.9 High-resolution transmission electron microscopy image of nucleated Ga_2O_3 on a collector with no wire growth. Scale bar reads 300 nm.

This result initially seems to suggest that wire nucleation takes place at the three phase boundary, however upon further inspection it seems to indicate the opposite. This substrate is one that exhibited no nanowire growth so it is just as viable that nucleation at the three phase boundary indicates no growth while nucleation at the collector/crystal interface results in wires.

The solidified collectors at the tips of wires are measured to be hundreds of nm in diameter, while the collectors shown here have an average diameter of 13.65 ± 4.07 nm. This disparity in size is a result of the collector formation process. A thin film initially melts into liquid droplets, and these are then allowed to solidify as the reactor ambiently cools. Au contracts when it transforms from liquid to solid, so as these liquid collector dots on the substrate start to solidify they shrink. As they shrink, they begin to fracture and form smaller and smaller solid gold particles until they are fully solid. Au at the tip of wires has nowhere else to solidify so they are stuck there, forming the catalyst tip that is the signature of VLS growths.

With this in mind, the HRTEM image seems to imply that as the reactor is cooling, material is still being incorporated into the collector. Since Au expands as it melts, the two main Au particles shown in Fig 4.9 would have been one liquid particle. If material was not being accommodated into the collector as it was solidifying, the 'inner' sides wouldn't have any Ga_2O_3 as they were the middle of the liquid particle, and not a suitable nucleation site. Looking at the larger collector particle on the right side of Fig 4.9, the side adjacent to the smaller particle seems to have less material than on the outside, indicating that the inner sides were plausible nucleation sites for less time than the outer sides. This most likely took place during cooling, after the one liquid particle fractured into two separately solidifying particles. This seems to further vindicate that nucleation at the three phase boundary is not the method for wire growth.

Observation of another HRTEM image taken of a grown wire, shown below, offers another look at the possible nucleation sequence. Fig. 4.10 clearly shows areas of gold trapped inside the formed wire, the darker areas near the end. This shows the changing conditions that results in the termination of wire growth. While it is unclear what exactly is happening, an easy explanation can be extrapolated from this image.

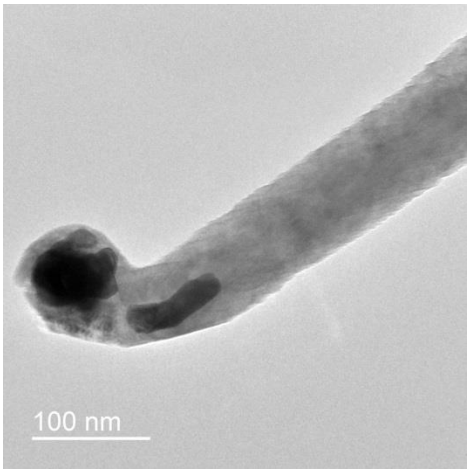


Figure 4.10 High-resolution transmission electron microscopy image of a grown Type II wire with trapped Au material near the tip (darker). Scale bar reads 100 nm.

As nucleation starts to take place at the three phase boundary as well as at the collector/crystal interface, the approximately spherical collector tip starts to elongate more and more until finally, material bridges the gap between the two and cuts off the elongated portion from the rest of the collector. Once this occurs, the curvature of the collector increases to account for the loss of material, changing the necessary conditions for wire growth. Once growth ceases, material still being incorporated into the collector continues to nucleate at the three phase boundary, which is making its way further and further up the collector until finally, the collector is completely encapsulated by Ga_2O_3, which is easily seen in Fig. 4.10. A representation of this possible nucleation sequence is shown below in Fig. 4.11.

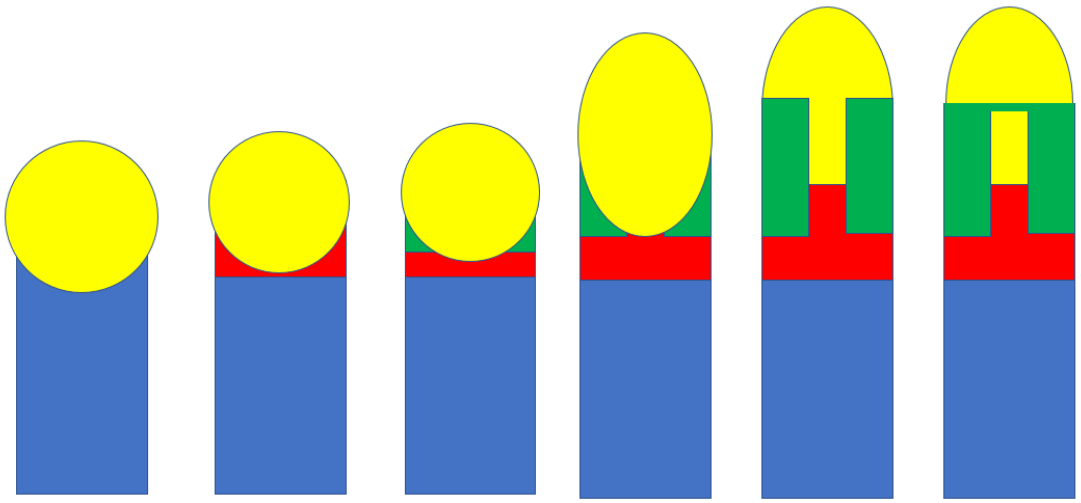


Figure 4.11. Possible Nucleation sequence resulting in the trapped Au shown in Fig. 4.10. The collector is the yellow material shown, and the already grown wire is blue. Material nucleated at the collector-wire interface is colored red and material nucleated at the three phase boundary is green.

4.4 CONCLUSIONS

This chapter described the results of 25 different temperature and pressure combinations for the growth of gallium oxide nanowires through a vapor-liquid-solid (VLS) mechanism. The grown wires were first confirmed to be gallium oxide and then further confirmed to be β-phase. The growths were separated into two types based on the type of wires grown. Type I wires were shorter and tended to have wider diameters, and Type II wires were much longer, with smaller average diameters although both diameters were on similar scales. These experimental findings suggest that VLS growth of β-Ga_2O_3 nanowires is a robust process with a broad range of acceptable conditions. Finally, high-resolution transmission electron microscopy images were offered as evidence that wire nucleation likely takes place along the collector-crystal interface.

5.0 SELECTED AREA DEPOSITION

5.1 INTRODUCTION

As discussed in previous chapters, fabrication methods for single-nanowire based devices lack consistency. Current methods rely on dispersing the grown nanowires into a solution, and then distributing the solution onto the desired substrate. These substrates either have prepatterned electrodes on them [31] or then have electrodes fabricated around the wire [6]. With either approach, there is usually a high degree of randomness with regard to the nanowire orientation making it difficult to fabricate significant numbers of similar working devices. While these methods are fine for a first generation of lab based devices, they are not sustainable for scaling up to commercial applications. This chapter discusses a new method for selected area deposition and alignment for reproducible device fabrication.

5.2 NANOWIRE COMBING

In 2013 Yao et al. demonstrated a method for depositing and aligning Si nanowires, called combing [45]. They fabricated a substrate with alternating areas of high and low adhesion to the nanowires. By then passing the growth substrate over the patterned substrate, nanowires were able to be deposited and straightened. Yao et al. used SiO_2 as the anchoring material, high adhesion area, and PMMA as the combing material, low adhesion area.

As shown below in Fig. 5.1, the pre-patterned substrate, blue, is brought into contact with the growth substrate, green, with a small amount of high viscosity mineral oil as lubricant, not shown. The substrates are then unilaterally translated with respect to each other. The areas of high adhesion to the wires 'catch' the wire being passed over, orange, and the surrounding areas of low adhesion, black, allow the wire to be straightened out. These wires were extremely well aligned within ±1º [45]. Yao was then able to show that by patterning smaller areas, selected deposition areas were able to be determined, making this a powerful tool for future nanowire-based devices.

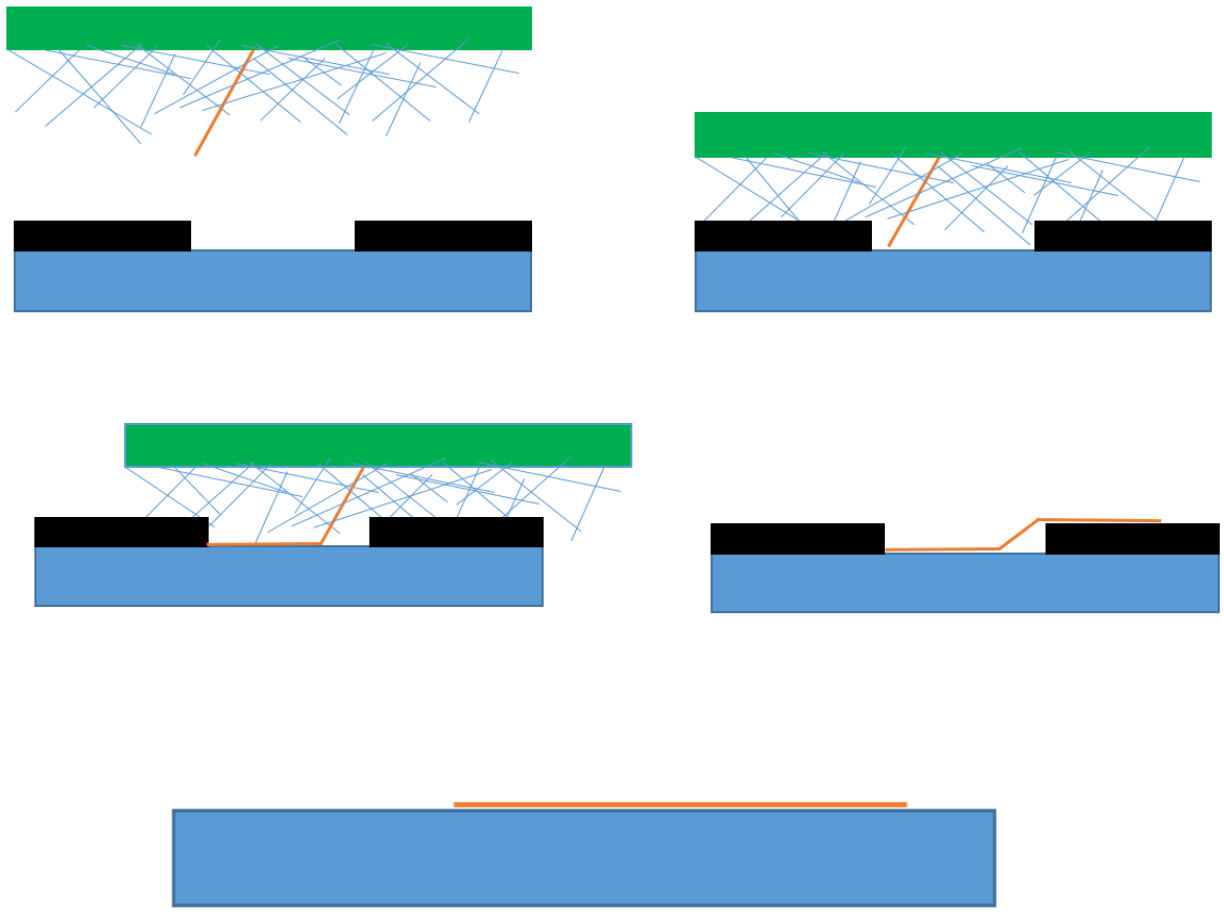


Figure 5.1. Example of a nanowire combing process. Growth substrate is colored green with the wire of focus in orange. The anchoring material substrate is colored blue and the combing material is black.

5.2.1 Combing for β-Ga_2O_3 nanowires

With this work [45] as a basis, a method for the combing of β-Ga_2O_3 nanowires was developed. Using methods for thin film growth, it was determined that materials that have good adhesion to β-Ga_2O_3 include SiO_2 and sapphire, among others [2,10]. SiO_2 was chosen as the material for this work due to its cost efficiency and well documented properties. In order to confirm that SiO_2 was a viable material, rudimentary combing was performed by hand on bare SiO_2 substrates. Large numbers of nanowire transfer was achieved as shown in Fig. 5.2. Although overall alignment was very poor, there is an observable long-range order. The poor initial alignment was attributed to the sizeable number of potential deposition sites and wire orientation.

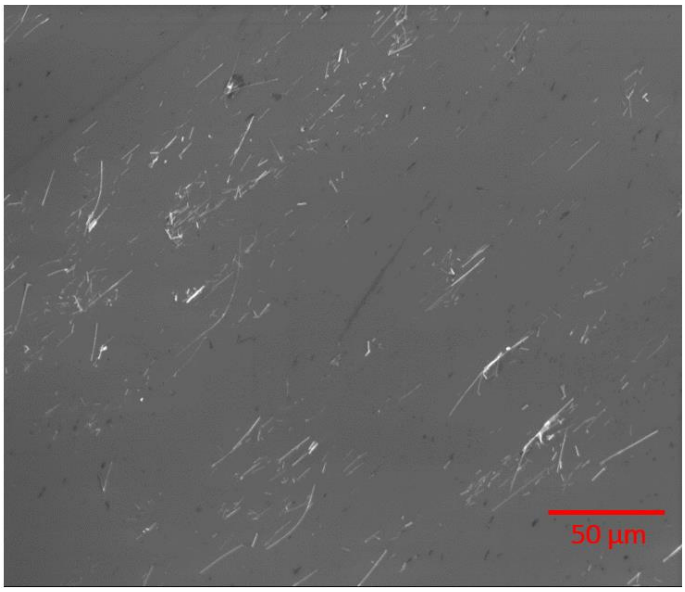


Figure 5.2 Example of initial hand-combing results. While overall alignment is poor, the original combing direction is clearly evident. Scale bar reads 50 µm.

Choosing a material that has poor adhesion to β-Ga_2O_3 required experimental testing due to the lack of available literature. An ideal material was thought to be photoresist of some sort, allowing for ease of removal after combing. In this vein, testing began with the available Electron Beam Lithography (EBL) resists. It was determined that Microchem 495 PMMA A4 was a good candidate. Fig 5.3 shows the clear difference in adhesion, post combing and stripping of the PMMA. During EBL patterning of the anchors, the lower right corner of the "cross" alignment marker was an area of focus, which exposed the rectangular area around it, represented by the white box. During combing, the area that was lithographically exposed and subsequently developed caught wires while the surrounding unexposed/undeveloped areas did not.

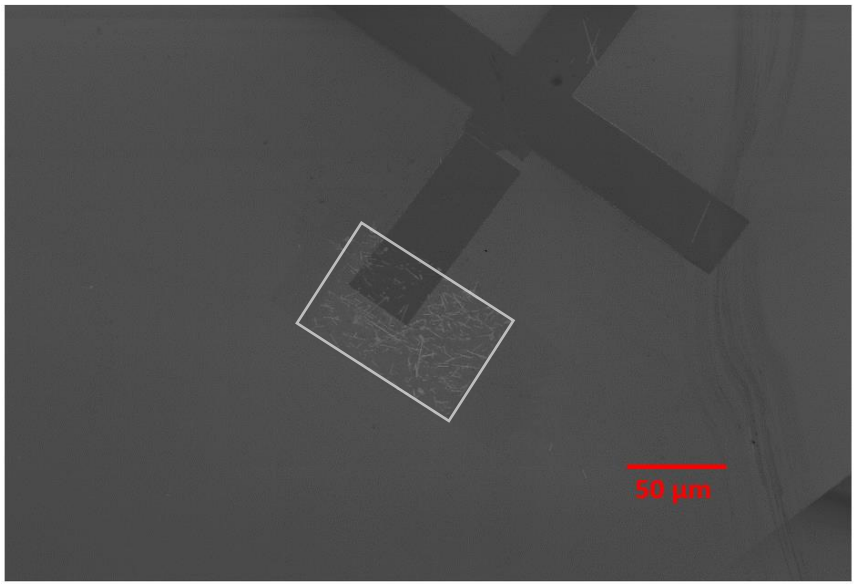


Figure 5.3. Depicting the clear difference in adhesion between the SiO_2 and PMMA. White box represents the focused area during EBL alignment. Scale bar reads 50 µm.

5.3 MACHINE COMBING

After the materials for both the anchoring and combing regions were chosen, a method for obtaining consistent combing was needed. A device was constructed to facilitate unilateral translation of two substrates, shown below. The track was constructed out of a used printer arm, with a new stepper motor which is controlled via an Arduino. The motor is capable of moving the substrate holders at speeds ranging from 5 to 50 mm/min. The top substrate holder was made to attach to the printer belt, and the bottom one is attached to a microscope stage mounted to the base via a block. The microscope stage allows consistent vertical contact positions of the substrates. Both of the holder blocks are made with a hole through them allowing a vacuum line to hold the substrates in place.

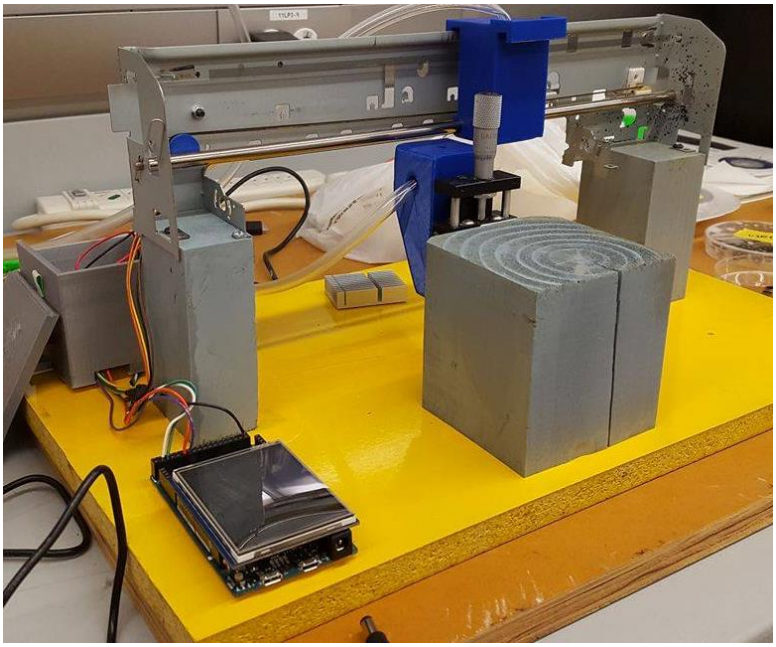


Figure 5.4. Mechanical Comber developed for consistent test conditions. Blue blocks are the vacuum holders for the two substrates. The top block moves left-to-right with respect to the stationary lower block. Vernier caliper adjusts the substrate-to-substrate spacing.

5.3.1 Wet combing

Using this machine, initial combing tests were performed on bare substrates with excellent results. Wires grown at growth condition 24 (T_g = 850 °C, P_{evac} = 0.04 MPa) were chosen as the grown nanowire substrates to use, with approximately 0.018 mL of light white mineral oil (Fisher Scientific) as the lubricant. Excellent transfer was observed with acceptable alignment, as shown below. However, as evident below, the mineral oil stays present on the substrate, even after drying. This presents many problems with making good electrical contact to the wires, and as such a cleaning process was investigated.

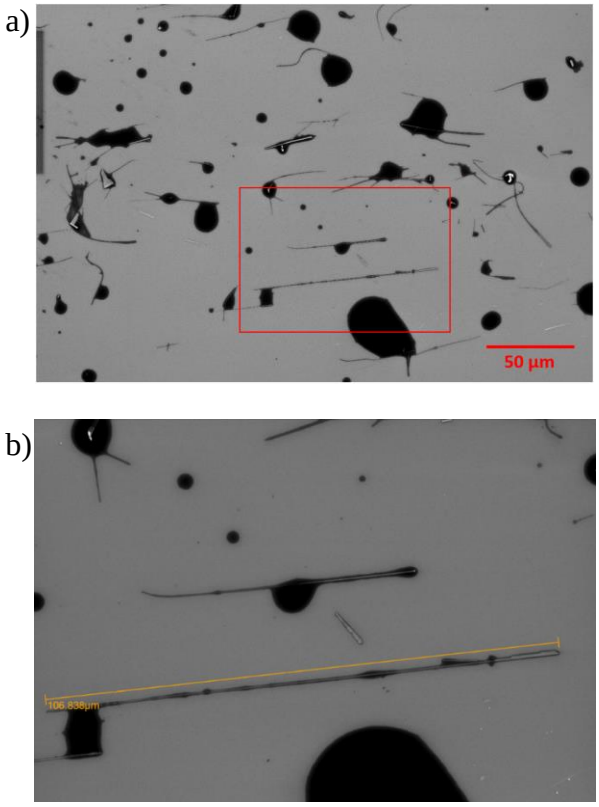


Figure 5.5 Initial wet combing results. Lower image is an enlarged image of the red box in 5.5a, wire measured is 106.838 µm. Scale bar reads 50 µm.

Three different cleaning methods were tested, deionized (DI) water rinse; isopropyl alcohol (IPA) rinse followed by a DI water rinse; and acetone, IPA then DI water rinse. An example of each cleaning method is shown in Fig 5.6. A pure DI water rinse had little effect on the oil residue, as expected. Rinsing with IPA and then DI water seems to slightly remove the oil but not enough. Rinsing with acetone, IPA and then DI water seems to remove all of the oil and was thus chosen to be the cleaning method used for any wet combing. This rinse order has the added benefit of stripping any PMMA on the substrate while cleaning the oil.

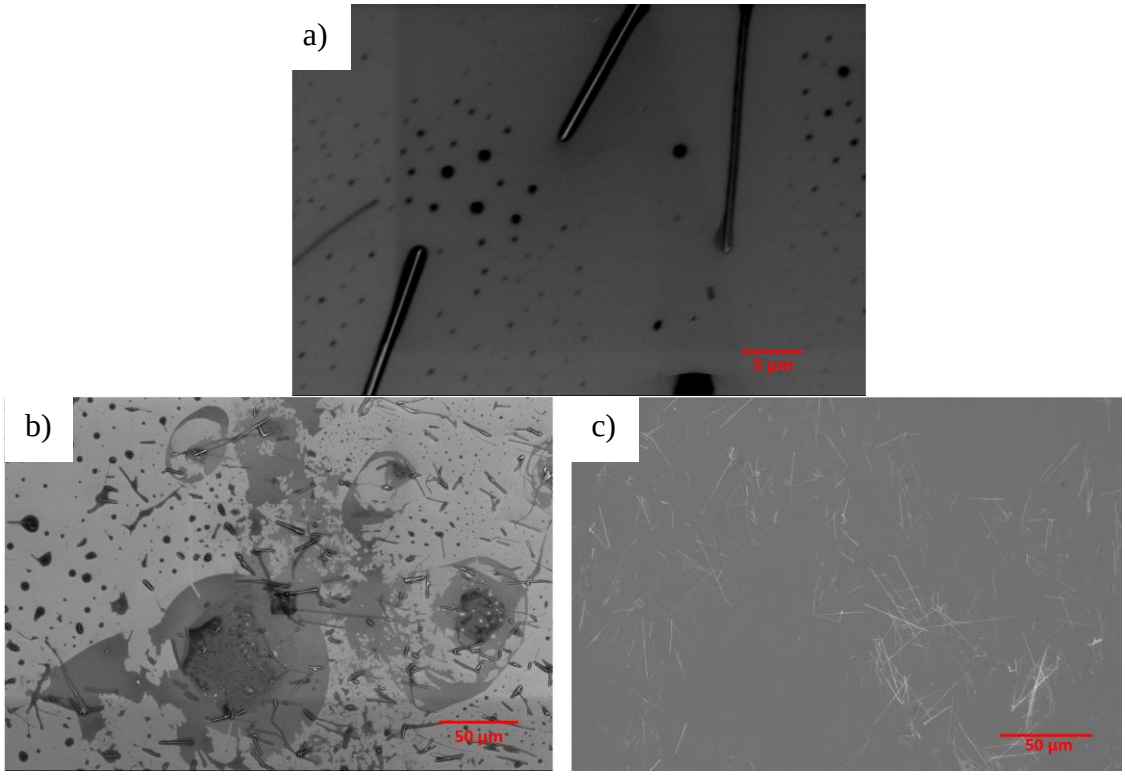


Figure 5.6 Cleaning tests for wet combing. 5.6 a shows wires after a deionized water rinse, scale bar reads 5 µm. 5.6b shows an isopropyl alcohol rinse followed by deionized water, scale bar reads 50 µm. 5.6c shows acetone followed by isopropyl alcohol followed by deionized water rinses, scale bar reads 50 µm.

5.3.2 Dry combing

Another method, called dry combing, was also investigated. This method was developed in response to the cleaning requirements for wet combing. By bringing the substrates close together without actually being in contact, the anchoring regions should only be in contact with the longest wires, ensuring a bottom limit on transferred wire length. Initial results are shown in Fig 5.7. Note the overall alignment of the wires.

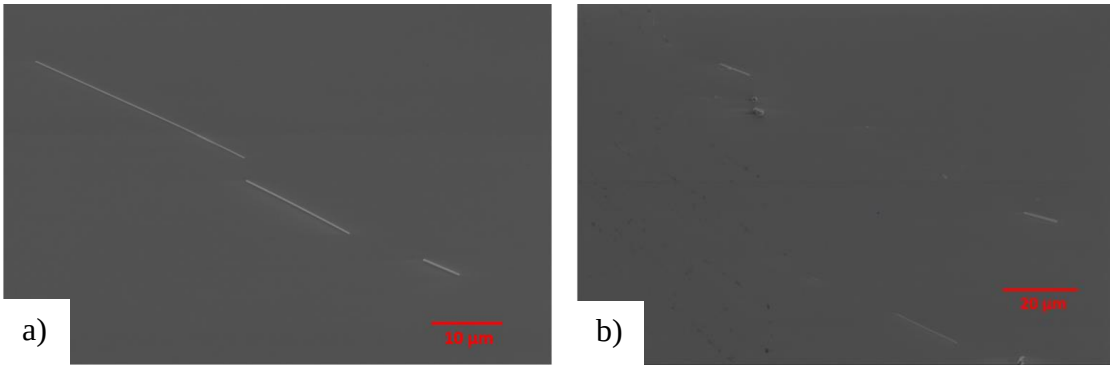


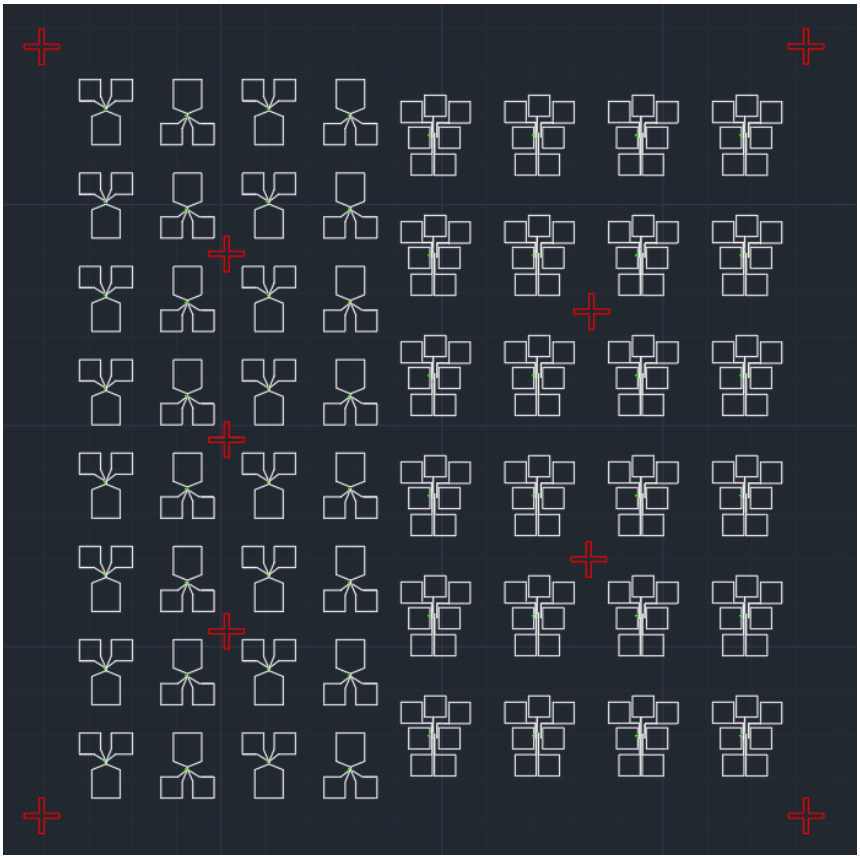
Figure 5.7. Initial dry combing results. 5.7a shows 3 aligned wires in a row, scale bar reads 10 µm. 5.7b shows aligned wires laterally, scale bar reads 20 µm.

However, this method also seems to have a few draw backs. While the oil imposes a need for post combing cleaning, the oil seems to not only increase alignment but it seems to get more consistent transfer densities. This increase in number of wires transferred is accounted to the capillary forces of the oil pulling the wire to the substrate. In addition, the lack of lubrication in dry combing tend to result in some shearing of the photoresist, resulting in more wire transfer than desired.

5.4 FABRICATION OF TESTING ARRAYS

Once the two methods were developed, work began on fabricating testing arrays. Fig. 5.8a below shows the overall pattern used. The left side of the chip is an array of simple electrodes with a bottom gate, shown in Fig. 5.8b. The two main pads form what would serve as a field-effect transistor (FET) source and drain contacts, with the bottom pad forming a gate contact. They are 150 μm x 150 μm and the bottom gate pad measures 200 μm x 200 μm. The electrode fingers come down to 2 μm prongs, with a gap of 2 μm between them. The right side is an array of transmission line model (TLM) arrays, shown in Fig. 5.8c. This pattern is intended to serve as a test pattern for measuring metal specific contact resistivity to the nanowires for ohmic and Schottky contacts and for assessing the resistivity of the nanowire. TLM measurements work by measuring voltage between several different combinations of the patterned fingers. The total resistance for different spacings can then be used to calculate the resistivity and contact resistance of the fabricated pattern [46]. The designed pads are all 150 μm x 150 μm, and the spacings between the TLM fingers are 2 μm, 4 μm, 8 μm, and 16 μm. The green areas shown in Fig. 5.8b and 5.8c are the anchoring regions, measuring 15 μm x 0.5 μm. The alignment markers and anchoring regions are fabricated via electron beam lithography (EBL), while the electrodes and TLM patterns are fabricated via traditional optical lithography methods.

a)



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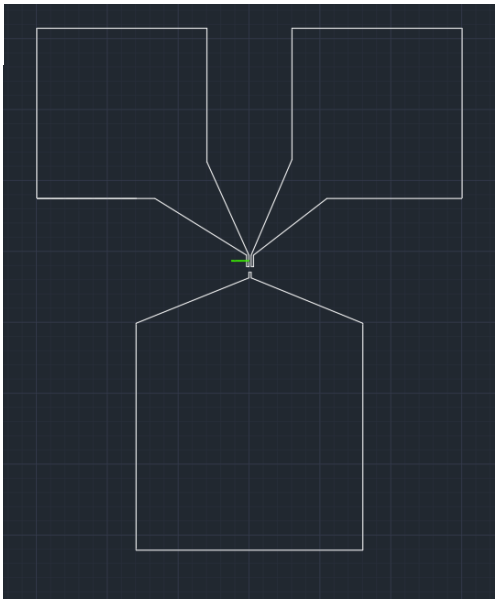

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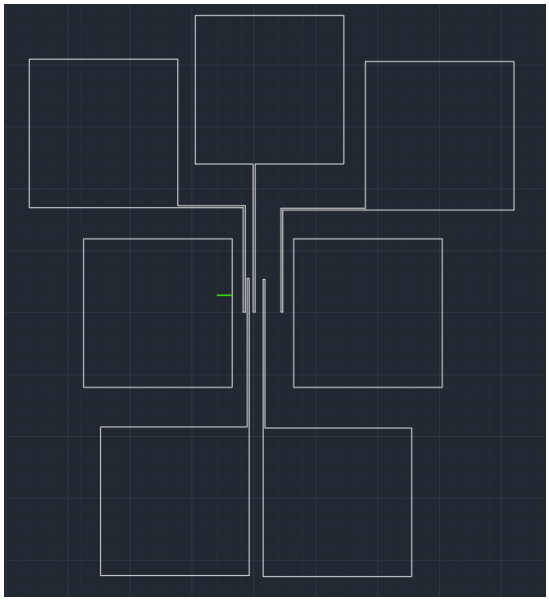

Figure 5.8 Overall testing array pattern. 5.8a shows the overall patterned electrodes in white, with alignment markers in red. 5.8b shows a close-up of the two-pronged electrodes on the left side of 5.8a. 5.8c shows the TLM patterns on the right side of 5.8a. The green areas in both 5.8b and 5.8c represent the anchoring areas.

The overall fabrication process is illustrated below in Fig. 5.9. First, ~200 nm of 495 PMMA A4 is spun onto the SiO_2 substrate at 4000 rpm, and then prebaked for 90 seconds at 180 °C. The alignment markers are then exposed with a Raith e-line EBL and developed in a 1:3 MIBK:IPA developer for 1 minute, followed by a 30 second rinse in isopropyl alcohol (IPA) and postbaked at 90 °C for 1 minute. With the pattern open, 50 nm of Ti capped with 10 nm of Au are deposited via Thermionics electron beam (e-beam) evaporator. Overnight lift off is then performed in an acetone bath, leaving Ti/Au markers on the wafer.

Once the alignment markers are fabricated, the anchoring regions can be formed. Again, ~200 nm of the same resist is spun on the substrate with the same process as above, and exposed via EBL. The substrate is developed via the same process and the anchoring regions are opened. Combing is performed on the prepared substrates, and the remaining EBL resist is stripped with an acetone bath, followed by an IPA rinse, a DI water rinse and then blow dried with N_2.

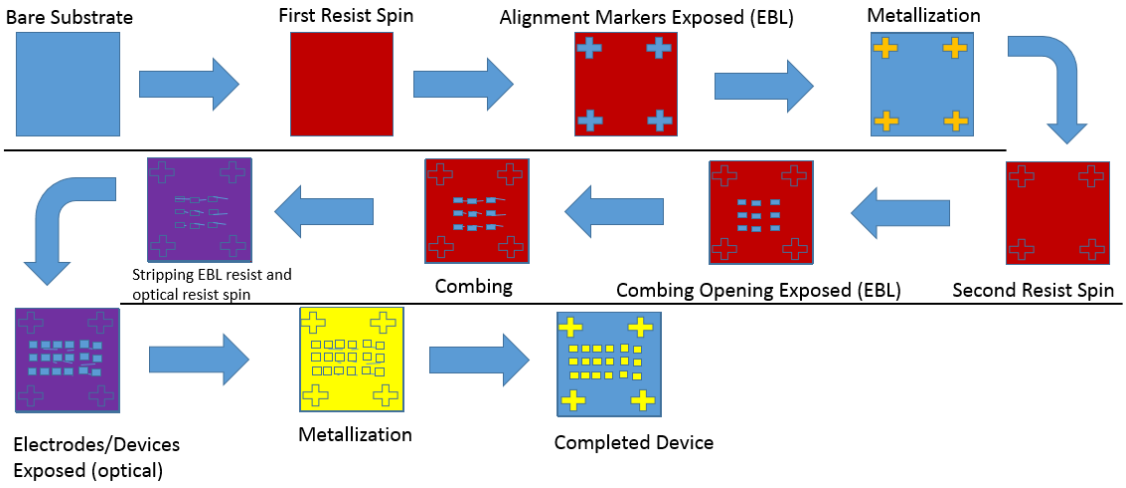

Figure 5.9. Diagram of testing array fabrication process beginning with the bare substrate in the top left, progressing through marker fabrication, combing, and electrode fabrication before the device is completed (bottom right).

At this point the substrate now has alignment markers and aligned wires, and the only thing left to form are the metallic electrodes. First, ~1.75 μm of Microposit SC1827 is spun onto the substrate at 7000 rpm, and prebaked at 115 °C for 2 minutes. The resist is then exposed with a Quintel mask aligner. The substrates are developed for 40 seconds with Microposit 351 developer, diluted such that 1:4 with DI water, followed by a 30 second rinse of pure DI water, and blow dried with N_2. The electrodes are then deposited via electron beam evaporator. The ideal metals to use for ohmic contacts for β-Ga_2O_3 nanowires is still an ongoing investigation and will be discussed in section 6.3, but for this work the electrodes are formed with 10 nm of Ti and 140 nm of Au.

Shown below in Fig. 5.10 are two sets of fabricated devices, with combing directions indicated by the arrows. Fig 5.10a and 5.10b are from the same run and have slightly misaligned electrodes. The optical mask was aligned via the lower right hand corner alignment marker, due to damage to the other markers during fabrication. This accounts for the TLM pattern being more closely aligned than the FET electrode, which has its wire further away from the designated anchoring region. Fig 5.10c was aligned with all the alignment markers, and as such the wire is in an ideal location. However, the electrodes were shorted during fabrication making this a proof of concept for nanowire combing, but less than ideal for electrical characterization.

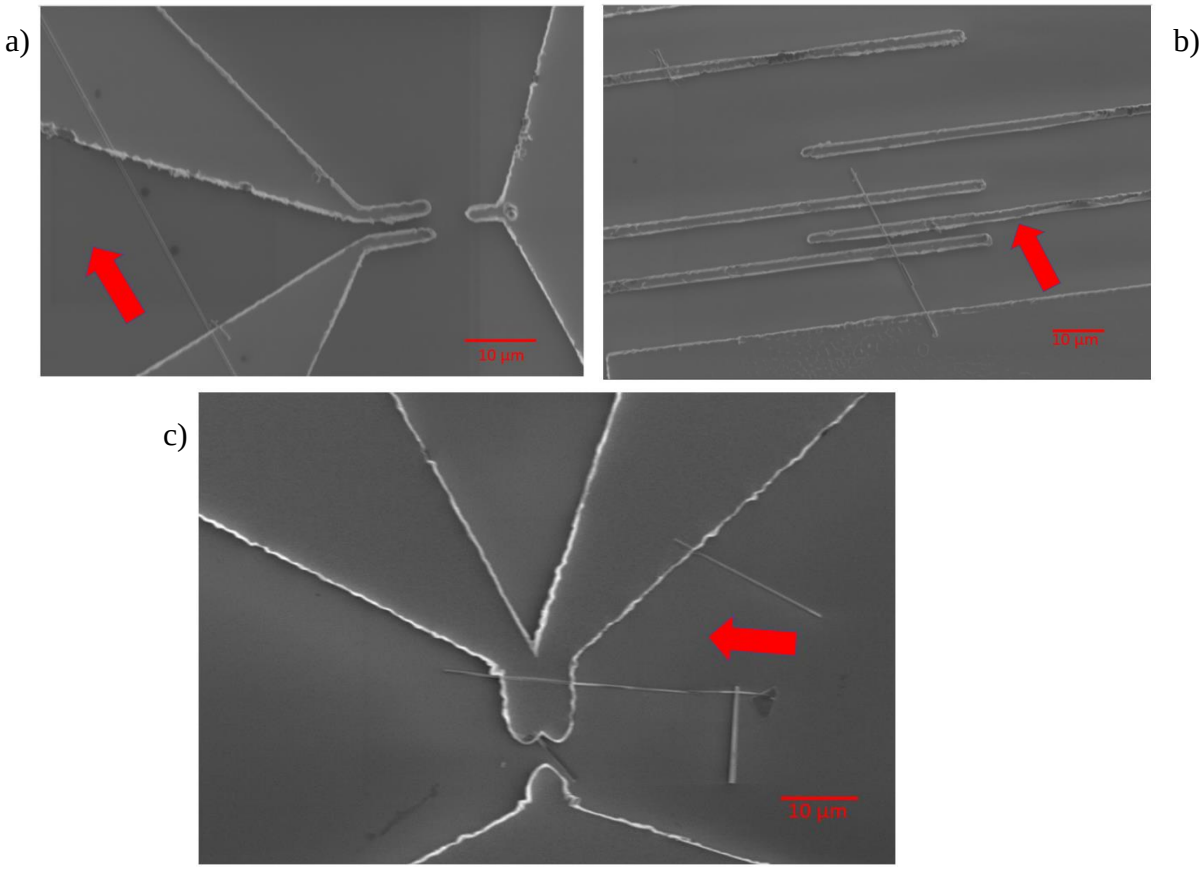

Figure 5.10 Fabricated testing devices, combing direction is indicated on all by red arrow. 5.10a and 5.10b shows a misaligned device but the overall combing direction is the same. 5.10c shows a well-aligned device, however the electrodes were shorted together during fabrication. All scale bars read 10 µm.

Nanowire combing is an incredibly powerful tool for future nanowire based devices. It takes full advantage of the material flexibilities offered at that length scale while allowing precise positioning of the wires. Shown below are two images of wires captured during development. Fig. 5.11a shows the extreme bending that this normally brittle material can go through in this form. Fig. 5.11b shows a wire that is bent around a piece of debris, demonstrating the ability to wrap these wires around objects. These offer exciting new possibilities for nanowire based devices.

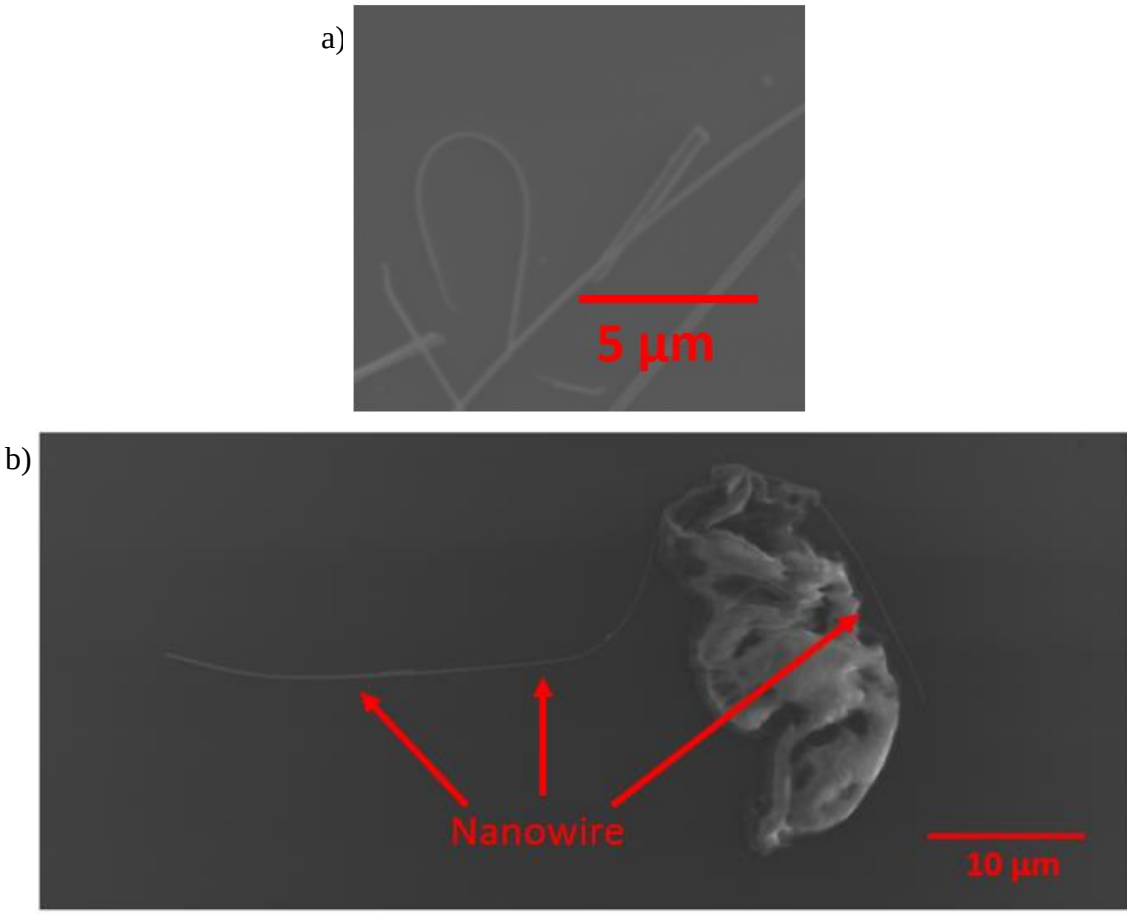

Figure 5.11 Flexibility of nanowires. 5.11a shows a nanowire bent to an extreme curvature, scale bar reads 5 µm. 5.11b shows a nanowire wrapped around a piece of debris during combing, scale bar reads 10 µm

5.5 CONCLUSIONS

Nanowire combing has the potential to open up the ability to implement nanowires into more reproducible devices. Having the capability to choose exactly where to place the nanowire as well as its directionality is an invaluable tool for device and integrated circuit fabrication. With the right set of optimized material selection, nanowire transfer can be a repeatable and efficient method.

6.0 FUTURE WORK

6.1 INTRODUCTION

This work presented an investigation into the vapor-liquid-solid (VLS) growth of β-Ga_2O_3 nanowires, as well as demonstrating a method for simple device manufacturing. Basic thermodynamic parameters of VLS were discussed, and the two nucleation processes were put forward. Influences of growth pressure and temperature were shown for 25 different growth conditions, with two main types of nanowires formed. Finally, a method for reliably depositing and aligning nanowires was demonstrated. For β-Ga_2O_3 nanowires to continue to move forward into the realm of electronic device research and development, there is more work that needs to be done in both characterization as well as optimization of the fabrication processes.

6.2 GROWTH OPTIMIZATION

While the vapor-liquid-solid (VLS) equations have been studied by different groups, [27, 28] these are all aimed at the nano or micro scale characteristics of the growth. These microscale characteristics need to be related to the macro scale controls (reactor gas partial pressures, temperature, substrate/collector optimization, etc) that can be easily influenced to control size and orientation of the grown nanowires.

Another parameter that deserves more investigation is the thickness of the collector film. The melting of thin metal films into nanoscale droplets is a subject of ongoing research [47, 48],

and the size distribution of the grown wires from films of different thicknesses could offer valuable insight into this problem. By fabricating a growth substrate with different growth areas of varying thicknesses and then characterizing the grown wires, what the average size of liquid drops are could be discovered, as well as optimal growth parameters for wire fabrication.

6.3 METAL-SEMICONDUCTOR CONTACTS

Although several different sources have reported ohmic contact to β-Ga_2O_3 devices, getting reliable low specific contact resistivity contacts to nanowires specifically remains a challenge [1]. There are two main methods for fabrication of nanowire devices. One takes nanowires sonicated in a solution and disperses them over an array of pre-patterned electrodes. The other also takes a solution of sonicated nanowires and disperses them on a substrate, and then fabricates electrodes based on the location of the wires. The first of these has extremely low reliability, and the second is extremely time consuming and inefficient and not applicable for integrated circuit fabrication. Both methods lead to poor contact between electrodes and wires, which along with the low number of devices made per run makes testing difficult. Through investigations into patterns like the previously mentioned transmission line measurement (TLM) arrays, characterization of different metal-semiconductor junctions for nanowires can be investigated.

6.4 SINGLE WIRE CHARACTERISTICS

Semiconductor nanowires still have a wide distribution of measured characteristics. To improve this fact, the ability to consistently fabricate large arrays of highly aligned nanowires is necessary. Single-nanowire based devices have been fabricated, but with low consistency and reliability [6, 31]. Once single wire measurements have been completed, establishing working physics-based and equivalent circuit models for the nanowire devices will be the next step. As seen previously in Fig 1.8 for Si nanowires, reshown in Fig 6.1 for convenience, there is a large disparity between most current nanowire models and measured values. Reliable device fabrications for testing will go a long way towards improving these results, although the different possible growth planes of the wires will also need to be considered.

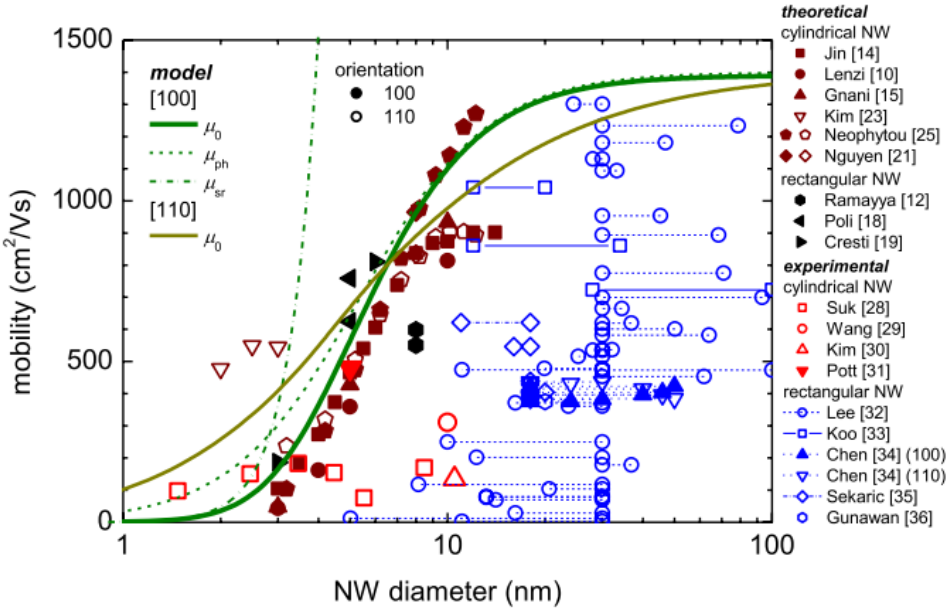

Figure 6.1 Nanowire diameter vs electron mobility theoretical and experimental results. 2014 IEEE. Reprinted, with permission, from R. Granzner, V. M. Polyakov, C. Schippel, F. Schwierz, and S. Member, "Empirical Model for the Effective Electron Mobility in Silicon Nanowires," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 1–7, 2014.

6.5 IMPROVING COMBING YEILD

In order to better facilitate not only the single wire characteristics, but also the metal-semiconductor contacts, improving the combing yields will be extremely useful. Better characterization of the contact force between the nanowire and both the anchoring material and the growth substrate will yield a better understanding of the process, as well as more efficient transfer.

For devices requiring single wire connections, a minimum anchoring area would be needed to ensure only one wire transfer per site. There are two surface interactions that need to be understood, the nanowire-anchor force and then nanowire-growth substrate. Initially, nanoscale friction measurements are performed via atomic force microscopy (AFM) manipulation [49]. By pushing the nanowire on its supporting substrate and measuring the resulting effect on the AFM cantilever, the static friction could be measured. However, this technique is extremely limited due to the nature of the contact between AFM tip, nanowire, and substrate.

In response, several new techniques have been put forth to try to better understand this problem. One group developed a technique called ‘most-bent state’ method. This method revolves around bending a nanowire to the minimum curvature, and applying traditional elastic beam theory to its profile. By bending the wire as shown in Fig 6.2, and assuming that the wire follows the radius of curvature fully around to form a circle of radius, R, the friction force can be calculated through basic mechanics equations.

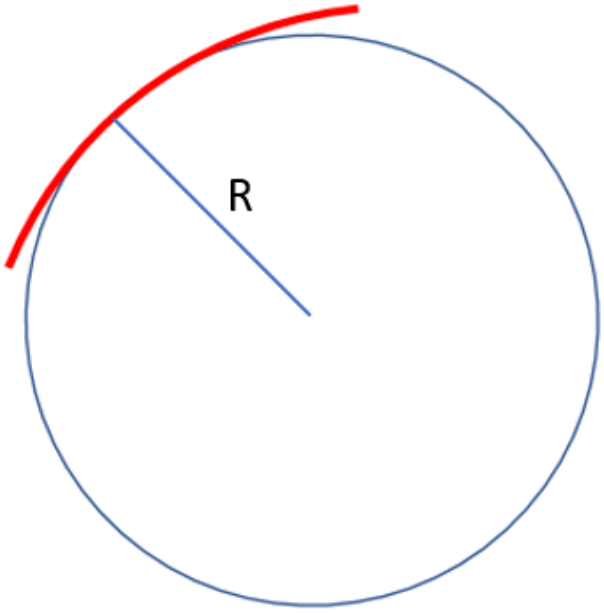

Figure 6.2. Illustration of a bent nanowire as well as its radius of curvature, R, for most-bent-method analysis.

Once surface interactions with the nanowires are better understood, more efficient materials can be chosen for the anchoring and combing surfaces. While it is possible to choose a more efficient material for the growth surface, it is a more limited choice due to the growth needs as discussed in Chapter 2.

6.6 ROLL TO ROLL MANUFACTURING

The flexibility of the nanowires and the planar nature of the combed devices lends itself easily to modern semiconductor fabrication techniques. One of the most exciting applications this method could be used for is roll-to-roll (R2R) manufacturing methods for flexible electronics. R2R manufacturing consists of a continuous sheet of material being passed through several inline processes, as illustrated in Fig 6.3. Combing can be applied to nanowires of any material, as long

as the anchoring and combing surfaces are chosen correctly. This leads to the possibility of not only combing of semiconductor nanowires for devices themselves, but also combing metal nanowires for flexible interconnects between devices.

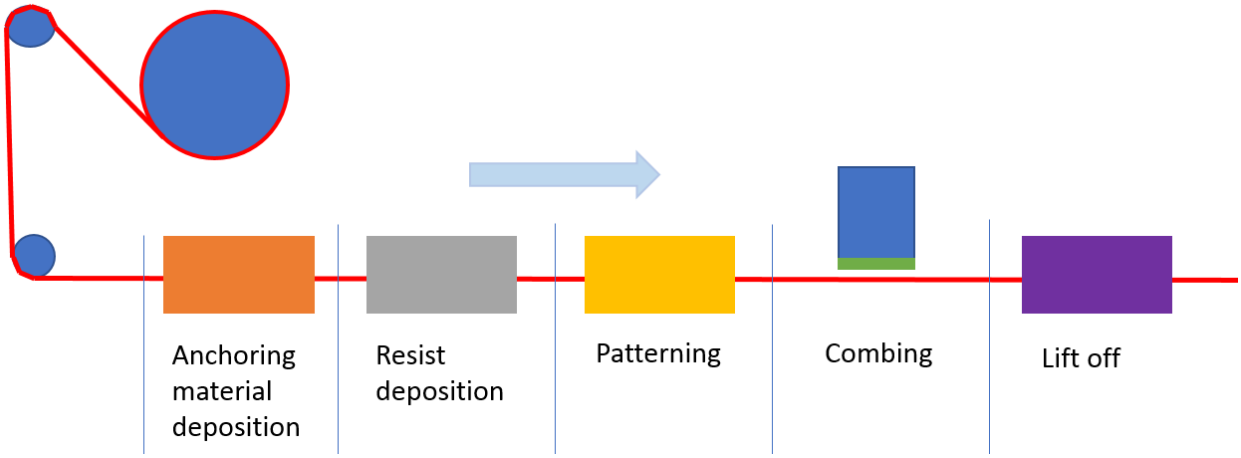

Figure 6.3. Schematic of a possible roll to roll combing process.

To efficiently integrate R2R manufacturing, exploring the effect of combing velocity will be needed. Yao initially found that the wire transfer density and alignment ratio were roughly independent of combing velocity [45], but it seems there should be a maximum combing velocity allowed. If a wire were moving too fast, the forward momentum of the substrate will overpower the weak nanowire-anchor interaction and pull it free. By finding the sticking force per unit area between the grown nanowire and the growth substrate, σ_{ws}, and the sticking force per unit area between the nanowire and the anchoring region, σ_{wa}, a maximum combing velocity, v can be approximated.

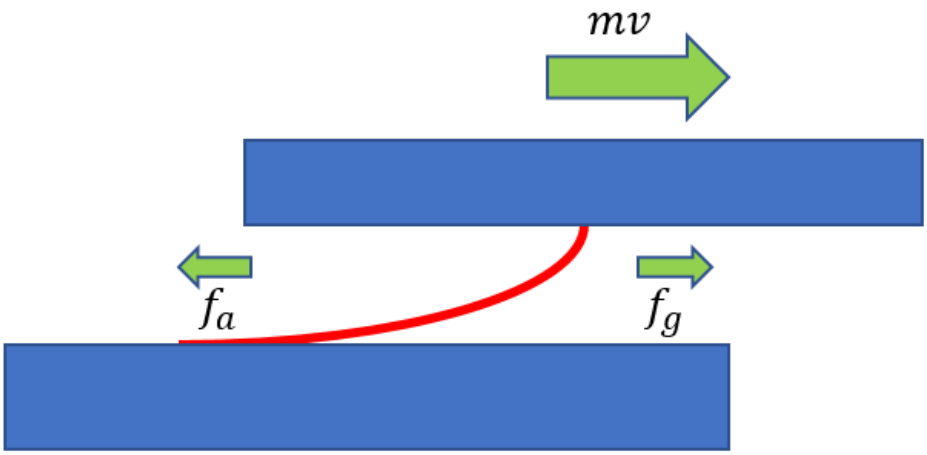

Figure 6.4 Basic forces acting on wires during combing. Upper substrates represents a growth substrate while the bottom represents the patterned combing substrate.

Using the model pictured in Fig 6.4 for an ideal nanowire with perfect contact to the entire anchoring area, A_a and approximately circular contact to the growth substrate, A_g a basic force balance equation can be set for the anchoring friction force, f_a, and the growth substrate friction, f_g. For combing to take place, the anchoring force needs to be greater than the momentum imparted to the wire and the growth sticking force such that:

$$f_a > f_g + mv \qquad (6.1)$$

By approximating the growth area contact to be a circular with the radius of the nanowire, r_w and assuming that the mass of the substrate holder is much bigger than both the wire mass and growth substrate mass, m_s, equation 6.1 can be rewritten as:

$$v < \frac{A_a\sigma_{wa} - \pi r_w^2 \sigma_{wg}}{m_s} \qquad (6.2).$$

It is important to note that the mass indicated here is a sum of the nanowire mass, growth substrate mass and substrate holder. Equation 6.2 is for the transfer of a singular wire onto an anchoring region. For the fabrication of a device consisting of n combed wires, Equation 6.2 takes the form:

$$v < \frac{n(A_a\sigma_{wa} - \pi r_w^2\sigma_{wg})}{m_s} \qquad (6.3).$$

In order to maximize the velocity for a given nanowire material with set anchoring and growth substrate materials, the total number of nanowires can be increased, or the mass of the substrate holder can be decreased. This maximum combing velocity will likely be the limiting factor for R2R applications.

6.7 CONCLUSIONS

Finally, it's clear that considerable opportunities exist for continued research in order to assess and develop the full range of capabilities potentially offered by Ga_2O_3 nanowires for electronic and optoelectronic device applications. Toward this end we have investigated the vapor-liquid-solid (VLS) growth of β-Ga_2O_3 nanowires, as well as demonstrated a method for simple device manufacturing. Basic thermodynamic parameters of VLS were discussed, and the two nucleation processes were put forward. Influences of growth pressure and temperature were shown for 25 different growth conditions, with two main types of nanowires formed. Finally, a method for reliably depositing and aligning nanowires was demonstrated.

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