ELECTRICAL PROPERTIES OF JUNCTION STRUCTURE IN SILICON DEVICES

by

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Semiconductor devices commonly employ junction structures that control carrier transport in various different mechanisms. The resulting junction properties are accessed via Ohmic contacts, and the transport process completes through this contact. It is no exaggeration to say that overall device characteristics are governed by junction properties. In this thesis we have investigated two different aspects of p-n junction structures in silicon devices and their effects on device performances: Ohmic metallization and junction formation. Specifically, we have successfully developed 1) low-loss Ohmic metallization on Si n+-p junction solar cells and 2) a spin-on dopant diffusion process for metal-oxide-semiconductor field-effect transistor (MOSFET) fabrication. In Si solar cells, junction/contact properties can be characterized by shunt and series resistance. By employing silver/graphene paste for Ohmic metallization on nanostructured emitter surface (n+-doped) we have investigated the effects of series/shunt resistances on solar cell efficiencies. In a MOSFET structure, source and drain regions are doped p-n junctions and are commonly formed by gas-phase diffusion of dopant sources. Spin-on dopant (SOD) is an alternative method of forming diffused junctions, offering certain advantages (such as safety and process simplicity). By employing phosphorous SOD we have formed n+-p junctions on p-Si substrate for source and drain regions. The resulting junction properties were characterized by transfer-length method

(TLM). By fabricating n-MOS structure we also demonstrated excellent FET characteristics as measured by device transconductance and carrier mobility.

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1.0 INTRODUCTION

1.1 OHMIC CONTACT ON SILICON

The Ohmic contact is a non-rectifying contact. The Ohmic contact on silicon is an important component of the modern IC industry which is critical for the performance of the device. The Ohmic contact on silicon has a linear I-V curve (current and voltage) following Ohm's law. Low resistance Ohmic contact can reduce the power consumption when current flows through the contact. There are two cases for metal-semiconductor contact to form Ohmic contact as shown in Figure 1. One case is $E_{FM}>E_F$ such that the energy bands of n-type silicon are bent downwards near the interface of contact. This band bending and its extension into the semiconductor are quite small. Due to this result, no potential barrier exists between the metal and silicon, and the charge can easily go through the contact obeying Ohm's law. Thus, this type of contact is Ohmic. Another case is $E_{FM}<E_F$ such that the contact between metal and silicon would prefer to form a Schottky diode rather than a Ohmic contact. It's easy to convert a Schottky contact to an Ohmic contact if the impurity concentration in silicon is high (e.g. $N_d = 10^{20}$ cm^{-3}). The width of the depletion region in silicon is defined as

$$W = \sqrt{\frac{2\varepsilon_{SC}}{qN_d}(V_i - V_a)} \quad (1)$$

In which V_i is the built-in potential and V_a is the applied voltage. In terms of highly doped silicon, the depletion region is very narrow, and electrons can easily tunnel through the barrier leading to a low-resistance Ohmic contact between metal and silicon.[1]

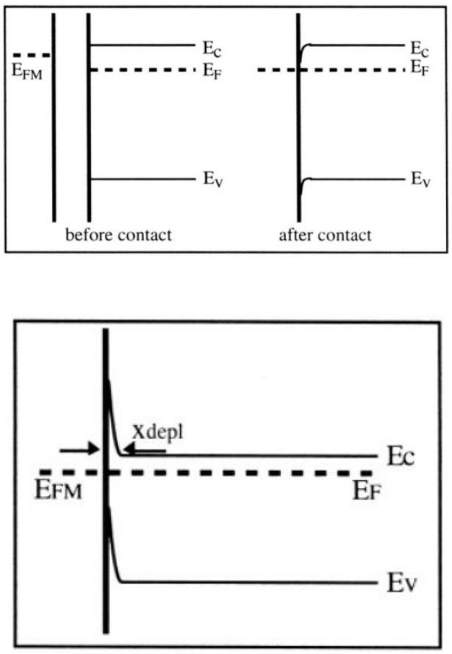


Figure 1. Energy bands of an Ohmic contact.[1]

1.2 SOLAR CELL OPERATION

The solar cell is a device that converts photovoltaic energy into electrical power. Two essential steps are contained in the conversion process. First, the absorbed light generates electron-hole pairs. Then, the electron-hole pairs are separated by an electrical field which is formed by the p-n junction. The electrons are collected by the negative terminal and holes are collected by the positive terminal. Electrical power is generated through this way. The I-V characteristic of an ideal solar cell can be described by the equation [2]

$$I = I_{ph} - I_0\left(e^{\frac{qV}{k_BT}} - 1\right) \tag{2}$$

or in current density

$$J = J_{ph} - J_0\left(e^{\frac{qV}{k_BT}} - 1\right) \tag{3}$$

Where k_B is the Boltzmann constant, T (K) is the absolute temperature, q (>0) is the absolute value of electron charge, and V is the terminal voltage. I_0 is the saturation current. The I_{ph}, photo current, depends on the incident photon flux on the solar cell and the quantum efficiency of the solar cell. In the ideal solar cell, the short-circuit current I_{SC} is equal to I_{ph}, and another important parameter for solar cell, open-circuit voltage V_{OC} is written as

$$V_{OC} = \frac{k_BT}{q}\ln\left(1 + \frac{I_{sc}}{I_0}\right) \tag{4}$$

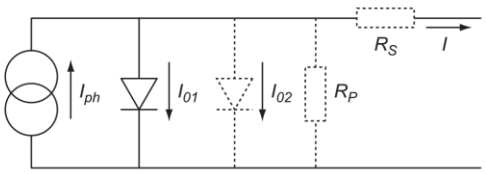


Figure 2. The equivalent circuit of a solar cell. Dotted lines correspond to the practical component.[2]

The maximum power P_{max} of solar cell is reached at certain voltage V_m and current I_m. And the fill factor is defined by

$$FF = \frac{I_m V_m}{I_{sc} V_{oc}} = \frac{P_{max}}{I_{sc} V_{oc}} \tag{5}$$

There is a superposition principle fort the I-V characteristics of an ideal solar cell. The photo current curve can be obtained by shifting the dark curve which is demonstrated in Figure 3. [2]

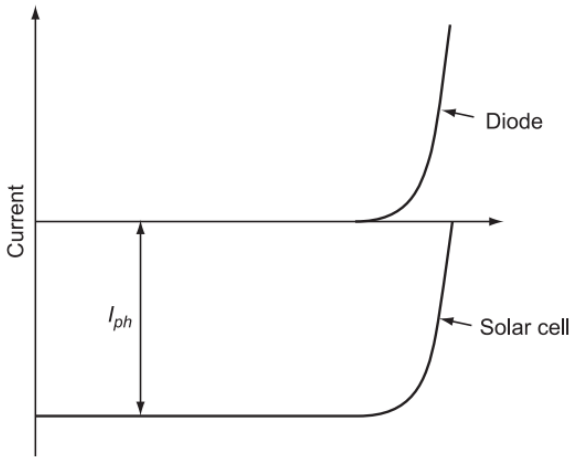


Figure 3. The schematic demonstration of the superposition principle for solar cells.

For a practical solar cell, the I-V characteristic normally differs from the ideal case. The parasitic resistance degrades the efficiency of the solar cell. A part of the parasitic resistance is the series resistance which originates from the contact resistance of the solar cell. Another part is the parallel resistance or shunt resistance which arises from the leakage part of the solar cell. Figure 4 shows

how the parasitic resistance affects the efficiency of the solar cell. The ratio of output power and input power defines the efficiency of the solar cell. The efficiency η can be described by

$$\eta = \frac{V_{oc} \cdot I_{SC} \cdot FF}{P_{in}} \tag{6}$$

Thus, to increase the efficiency of the solar cell, V_{oc}, I_{SC}, FF should be as large as possible to get very high efficiency in practical use.

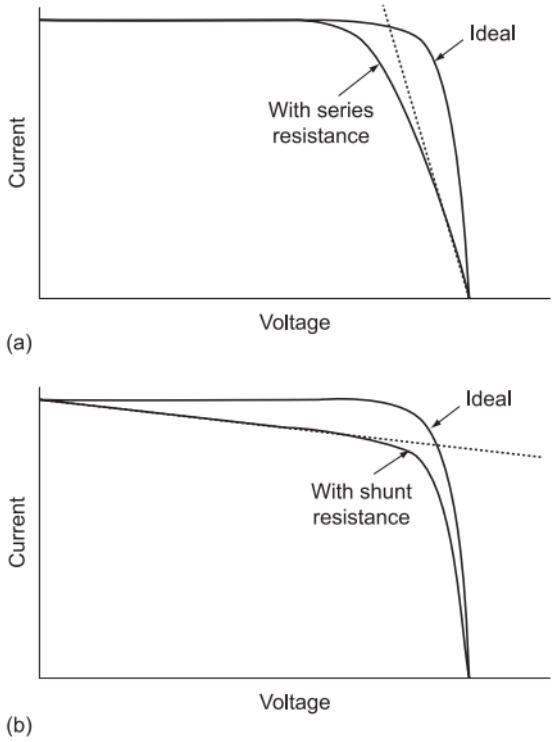


Figure 4. The I-V characteristic of solar cells with large series resistance and with small shunt resistance.[2]

1.3 MOSFET FABRICATION

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the fundamental unit in modern integrated circuits. A standard MOSFET structure is shown in Figure 5, which is the goal of this section. To fabricate a desirable MOSFET, the process flow involves silicon cleaning technology, diffusion, oxidation, photolithography and metallization. The diffusion process is one of critical steps to fabricate a MOSFET. The spin-on dopant (P509 purchased from Filmtronics) is used for n-type diffusion. The advantages of spin-on dopant contain easy lab operation, nontoxic gas, and shallow junction.

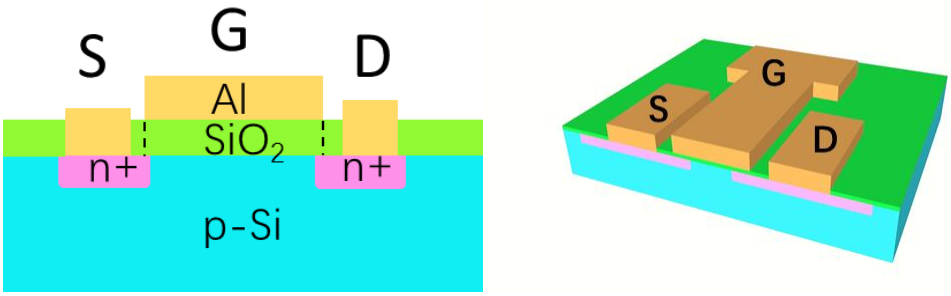


Figure 5. Schematic diagram of n-MOSFET structure.

2.0 OHMIC CONTACT ON SILICON

Semiconductor devices commonly employ metal-semiconductor junction structures that control carrier transport in various mechanisms. The non-rectifying junctions is called Ohmic contacts. The resulting junction properties are accessed via Ohmic contacts, and the transport process completes through this contact. It is no exaggeration to say that overall device characteristics strongly depend on the property of Ohmic contacts. Thus, it's critical to figure out how to prepare a good, reproducible Ohmic contact on silicon. Aluminum is widely used as the metallization material in the IC industry. It has many advantages like low resistivity, ease of deposition, excellent adhesion to dielectrics, dry etching, and Ohmic contact to Si. The problem is that the shallow junction might be short-circuited when aluminum is used to form Ohmic contact.

2.1 OHMIC CONTACT BETWEEN ALUMINUM AND P-TYPE SILICON

In this section, the Ohmic contact between aluminum and p-Si is tested experimentally. Aluminum is well-known as a kind of p-type dopant for silicon. To form a good Ohmic contact between metal and semiconductor, a well-cleaned silicon surface and a proper annealing process are necessary.

2.1.1 Experimental Procedure

The p-Si wafers were single side polished (100) with ρ=1-10 Ω·cm. The silicon surface was prepared by a standard RCA clean process followed by etching in Buffered Hydrofluoric acid (BHF) before metallization. Buffered Hydrofluoric acid (BHF) solution comprises a 6:1 volume ratio of 40% NH_4F in water to 49% HF in water. Detailed procedures of the cleaning process are shown in Table 1. The hydrofluoric acid (ACS reagent, 48-51% solution in water) is used in the experiment. The aluminum is thermally evaporated from a tungsten boat. The silicon surface is covered by a shadow mask to create separate aluminum dots or lines. The base pressure of chamber is ~10^{-6} torr. When aluminum is evaporating, the pressure rises up to ~10^{-5} torr. The freshly prepared samples were annealed at 350ºC, 430ºC, 480ºC with nitrogen for 30min. Figure 6 shows the schematic diagram of the measured sample. The tungsten probes are put on the surface of different Al dots.

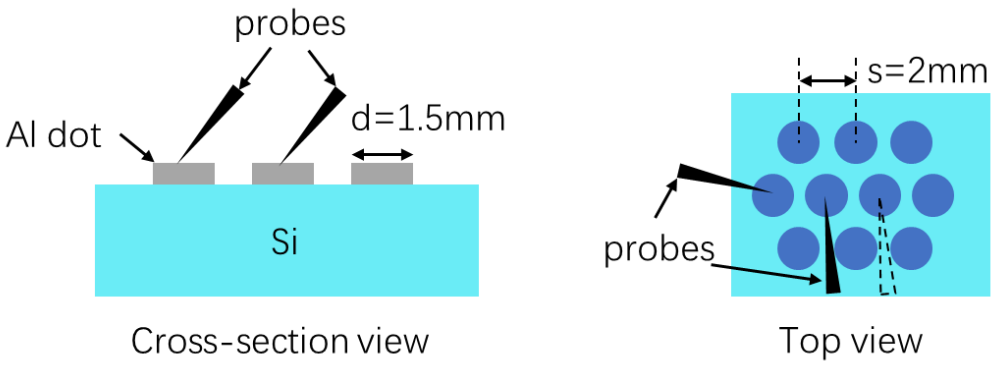


Figure 6. Schematic diagram of Al dots pattern and setup of measurement.

Table 1. Detailed procedure of cleaning method

1	Rinsing in deionized water (DI water)	5min
2	Ultrasonic cleaning in acetone	5min
3	Ultrasonic cleaning in methanol	5min
4	Rinsing in DI water	5min
5	SC-1: Soaking in mixture of 5:1:1=DI water: NH_4OH: H_2O_2	10min @70ºC
6	Rinsing in DI water	1min
7	1:50=HF: DI water	15sec
8	Rinsing in DI water	1min
9	SC-2: Soaking in mixture of 6:1:1=DI water: HCl: H_2O_2	10min @70ºC
10	Rinsing in DI water	5min
11	Etching in BHF	4min
12	Rinsing in DI water	5min

2.1.2 Result and Discussion

The freshly prepared samples were annealed at 350ºC,430ºC, 480ºC separately for 30min with nitrogen ambient. Samples were naturally cooled down in pure nitrogen ambient. Good Ohmic contact didn't obtain at 350ºC. The samples annealed at 430ºC and 480ºC, however, show a good Ohmic contact which corresponded to a linear line in I-V graph, as shown in Figure 7. The formation of Ohmic contact between p-type silicon and aluminum is based on the decrease of

Schottky-barrier height after the proper annealing process. [3] Silicon was found to diffuse very fast in evaporated Al under heating. When samples were annealed, silicon at the interface would diffuse into Al and reach the maximum solubility allowed at that temperature. [4] After cooling down, the diffused silicon would recrystallize at the Si-Al interface to form an intermediate layer. And this silicon layer contains an amount of Al and becomes a p+-doped silicon. The existence of the Al could reduce the Schottky-barrier height between p-type silicon and Al. This diffusion and recrystallization behavior are not proceeded uniformly at the Si-Al interface. Thus, there were many spikes after annealing. Those spikes may short-circuit shallow p-n junctions. That is the reason why people try to add a barrier layer between Al and silicon, so the final contact system can bear a high temperature process. According to the I-V data, higher temperature gives larger current at the same applied voltage. Therefore, a good Ohmic contact can be formed at relatively high temperature for p-silicon and aluminum. But high temperature annealing for Ohmic contact may affect other components in the device. For good Ohmic contact on p-type silicon substrate, 480ºC is a reasonable temperature. In this part, the experiment results confirm that the Ohmic contact between p-type silicon and aluminum can be obtained with proper annealing conditions.

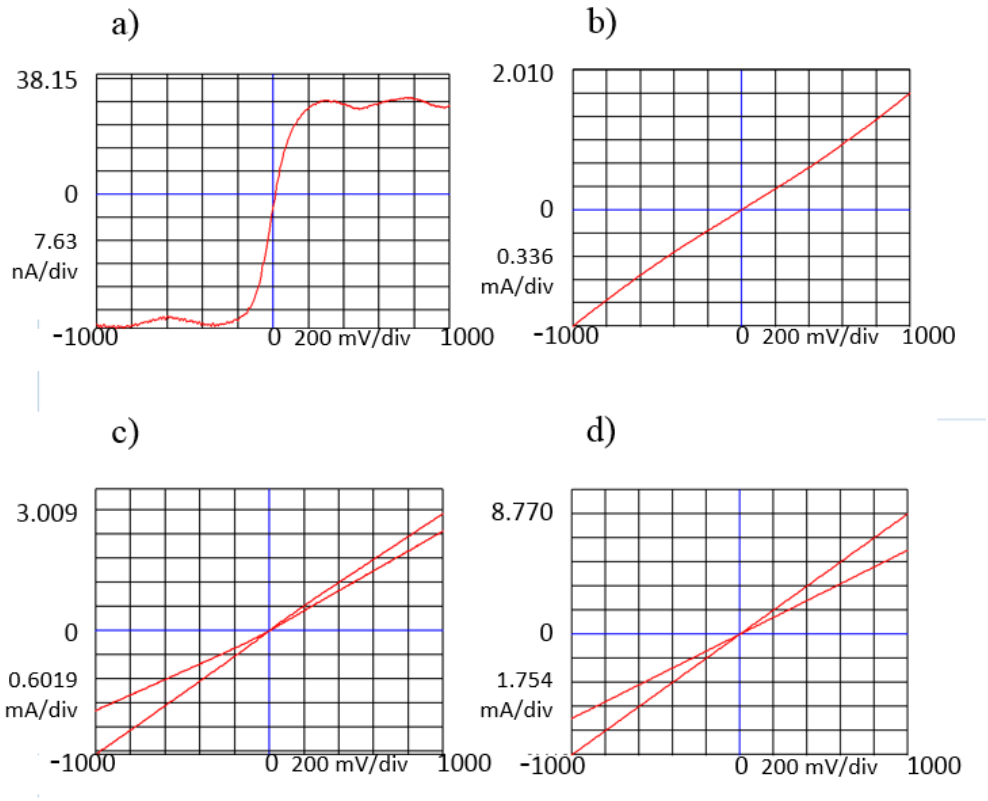


Figure 7. I-V graph of Aluminum and p-type silicon. a) I-V graph before annealing; b) I-V graph after annealing at 350ºC in N_2 ambient; c) I-V graph of two different dot-to-dot spacings after annealing at 430ºC in N_2 ambient; d) I-V graph of two different dot-to-dot spacings after annealing at 480ºC in N_2 ambient.

2.2 OHMIC CONTACT BETWEEN ALUMINUM AND N-TYPE SILICON

2.2.1 Experimental Procedure

The experimental procedure for n-type silicon substrate is same as the p-type silicon substrate. The n-Si wafers were single side polished (100) with ρ=5-30 Ω·cm. In this part, a silver and n-silicon contact system were also investigated.

2.2.2 Result and Discussion

The samples were tested before and after annealing. The annealing was proceeded at 350ºC under nitrogen ambient. As shown in Figure 8, the I-V curve is not a linear line before annealing, which demonstrates the contact between Al and n-Si isn't a good Ohmic contact. However, the annealing process doesn't improve the contact according to the I-V result in Figure 8. Not only the current decreases after annealing, but the curve is even farther from a straight line. To explore a larger temperature range, the annealing temperature was reduced to 200ºC or 300ºC. The Ohmic contact behavior still hadn't been obtain on n-type silicon substrate. The explanation should be the same as the p-type silicon case. Silicon is known to easily diffuse into evaporated Al when annealed at a certain temperature. Silicon recrystallizes at the interface of Al and n-type silicon, which forms a new layer with Al-doped. The contact structure isn't only aluminum and n-Si, instead there is recrystallized p-type silicon between the aluminum and the n-type silicon. This layer somehow benefits the formation of Ohmic contact between Al and p-type silicon.[3] However, it's definitely harmful for the formation of Ohmic contact between Al and n-type silicon. The I-V result after annealing confirms that the height of the Schottky-barrier between Al and n-type silicon is increased. Basically, aluminum is not a good choice to make a good Ohmic contact for the n-type silicon (lightly doped). Although Aluminum still can be used for Ohmic contact material for n+ silicon, the annealing process should be avoided after depositing aluminum on the surface of n+ silicon. Silver is another very common metal used as an electrode on silicon and is also investigated briefly. Silver has the lowest resistivity in natural metal. It is a great electrode material to reduce the series resistance. Silver is also explored at the similar process on n-type silicon. Silver (99.999%) is thermally evaporated to n-type silicon substrate. The samples are annealed at different temperatures. The results show that silver also couldn't achieve Ohmic contact with n-

type silicon. Silver contact deforms after annealing process even in a relatively low temperature like 300ºC, as shown in Figure 9. One important principle to choose proper metal material is that the metal contact shouldn't deform under annealing process. In conclusion, the evaporated pure silver is not suitable to be used as an Ohmic contact for n-type silicon.

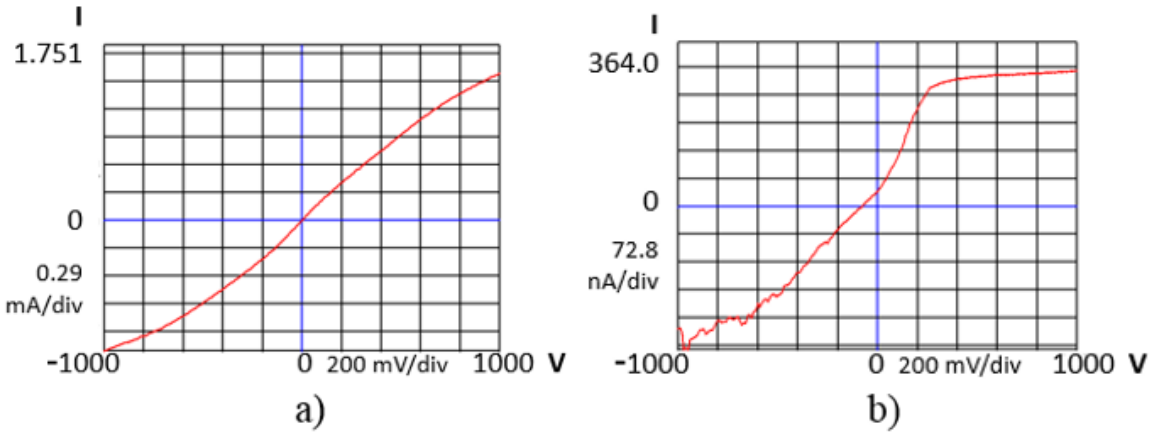


Figure 8. I-V graph of Aluminum and n-type silicon**.** a) I-V graph before annealing at 350ºC in N_2 ambient; b) I-V graph after annealing at 350ºC in N_2 ambient.

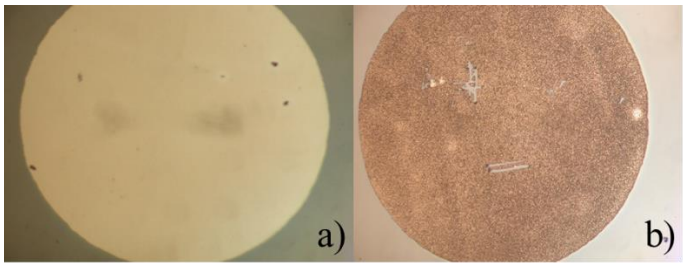


Figure 9. Surfaces of silver dot electrode

a) Before annealing; b) After annealing at 300ºC in forming gas (10% of H_2, 90% of N_2)

3.0 SILICON SOLAR CELL CHARACTERIZATION

3.1 INTRODUCTION

Increasing the efficiency of a solar cell is always an important topic. There are several ways to improve the efficiency of a solar cell. One important and common method is to add an anti-reflective coating on the front-side (face to the light) of solar cell. However, the monolayer of an anti-reflective (AR) coating has an optimal wavelength and incident angle. A multilayer AR coating increases the cost of manufacture and complexity of process but reduces reflectivity over a broad range of wavelengths of light across the solar spectrum. For real application, a monolayer anti-reflective coating normally combines with a texture on the surface to achieve better light absorption or light trapping. The working principle of a textured top surface not only can reduce the reflection of light, but also help to confine the light within the solar cell. Creating this kind of surface structure is an effective way to increase the efficiency of a solar cell. In this section, a solar cell with nanopillar top surface was investigated experimentally. During the experiment, series resistance is reduced by applying silver/graphene paste on the front-side electrode. And the shunt resistance is improved from tens of Ω to thousands of Ω by cleaving the four edges of solar cell.

3.2 EXPERIMENT

3.2.1 Description of solar cell structure

A solar cell is received from Albany. One batch is called a planar solar cell in this thesis. And the planar solar cell is used as the reference solar cell during efficiency measurement and to confirm the process is optimal. The planar solar cell is covered by SiN layer as antireflective coating. (as shown in Figure 10) Another batch is called a nanopillar solar cell. The structure of the tested nanopillar solar cell is shown in Figure 10. First, the solar cell with the flat SiN layer (as depicted in Figure 10.a) was selectively etched through RIE technology. The SiN-nanopillars were created on the top of solar cell. The SiN was fully etched by RIE except for the nanopillar area. Thus, some surface damage was induced here and forms a recombination center for electrons and holes. The effective SiN thickness was too thin causing relatively high reflectance. To get better light absorption, additional SiN layer was deposited by PECVD. The thickness of additional SiN is calculated from the optimal thickness of planar SiN for the solar spectrum. After this process, the nanopillar solar cells were ready for later testing. Figure 11 shows the light propagation in the nanopillar structure and planar structure. The incident light has a greater chance to propagate along the glancing angle and then absorbed into the solar cell. Thus, the solar cell with a proper nanopillar structure as the antireflection layer can absorb more light energy and generate more electron-hole pairs.

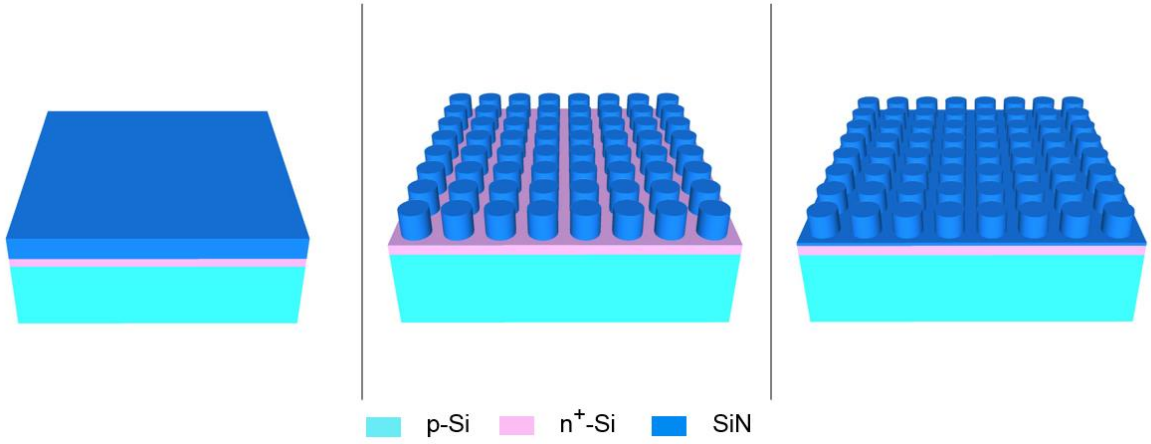


Figure 10. Schematic diagram of solar cell structure.

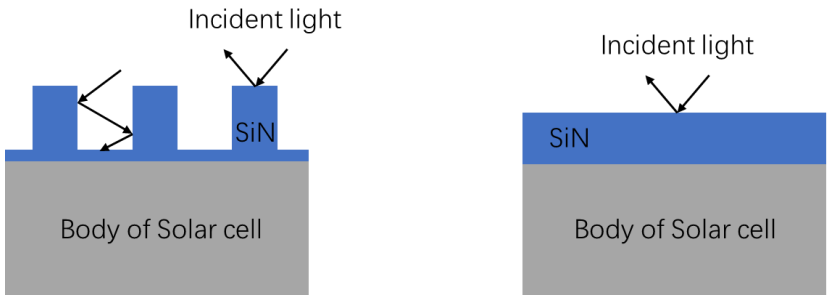


Figure 11. Schematic of the work principle of nanopillar structure.

3.2.2 Backside Ohmic contact

Thin aluminum layer is evaporated to the bake-side of solar at vacuum of 10^{-6} torr. And then samples with aluminum on the back-side were annealed at 350ºC for 30min in forming gas to form the Ohmic contact. The composition of forming gas is H_2 (10%) and N_2 (90%). The aluminum can form a back surface field which benefits the electrical and optical performance of the solar cell.[5] [6]

3.2.3 Front-side Ohmic contact

The front-side electrode can be divided into two sections. The first section is to prepare the three-layer metal contact which consists of titanium, palladium, and silver. In this section, the front-side electrode pattern-1 (as shown in Figure 12.a) is transferred to the solar cell through photolithography. Then BHF etching is used to remove the SiN layer and expose the bare n+ silicon surface for later metallization. Titanium, palladium and silver are deposited by e-beam evaporator in sequence. Figure 12.b shows the photo of the real sample after lift-off process. The contact grid can be seen clearly. The second section is that the silver/graphene paste (Silver/Graphene Conductive Epoxy G6E-SG) purchased from Graphene Supermarket was printed on the top of Ag/Pd/Ti contact. This paste is used to further reduce the series resistance of the front-side electrode on the solar cell. The photolithography combined with a paper tape mask is used to print silver/graphene paste exactly on the top of Ag/Pd/Ti contact. First, the photolithography transfers the front-side electrode pattern-2 (Figure 12.c) to the solar cell which is aligned to the Ag/Pd/Ti contact. Figure12.d shows the front-side electrode pattern-2 after exposing and developing. Then a paper tape mask with the same dimension as the front-side electrode pattern-2 is added on top and print the silver/graphene paste, as shown in Figure 12.e. After printing, the paper tape mask is removed first and the solar cell with fresh paste is heated to 150ºC for 1 hour to cure the paste. After curing, acetone is used to remove the photoresist which can make sure the nanopillar or planar surface is clear. The schematic final structure (cross-section view) of solar cell is shown in Figure 13. According to the data from company, the planar solar cells as received should have an efficiency at around 15%. Thus, to achieve fair comparison between the planar and the nanopillar solar cell, the first step is to reach that efficiency on the planar solar cell by optimizing the contact design and fabrication. The planar solar cell is also the

reference cell during the efficiency measurement. The series resistance and shunt resistance are the major optimized parameters during the experiment process. To obtain low series resistance, silver/graphene paste is added on the top of the front-side contact. The series resistance reduces 1 Ω after applying the silver/graphene paste on the front-side electrode. A short time annealing process in forming gas is also tried to passivate the surface and recover the open-circuit voltage. However, the shunt resistance is still very poor after optimizing the series resistance. The shunt resistance keeps at a small value indicating some parts are leaky. We found that if the four edges of the solar cell were cut, the shunt resistance became very good and the series resistance just slightly increased. Figure 14 displays the photo of the real sample after cleaving the four edges. For now, all processes are acceptable, and the highest efficiency of planar solar cell reaches to 15.20%.

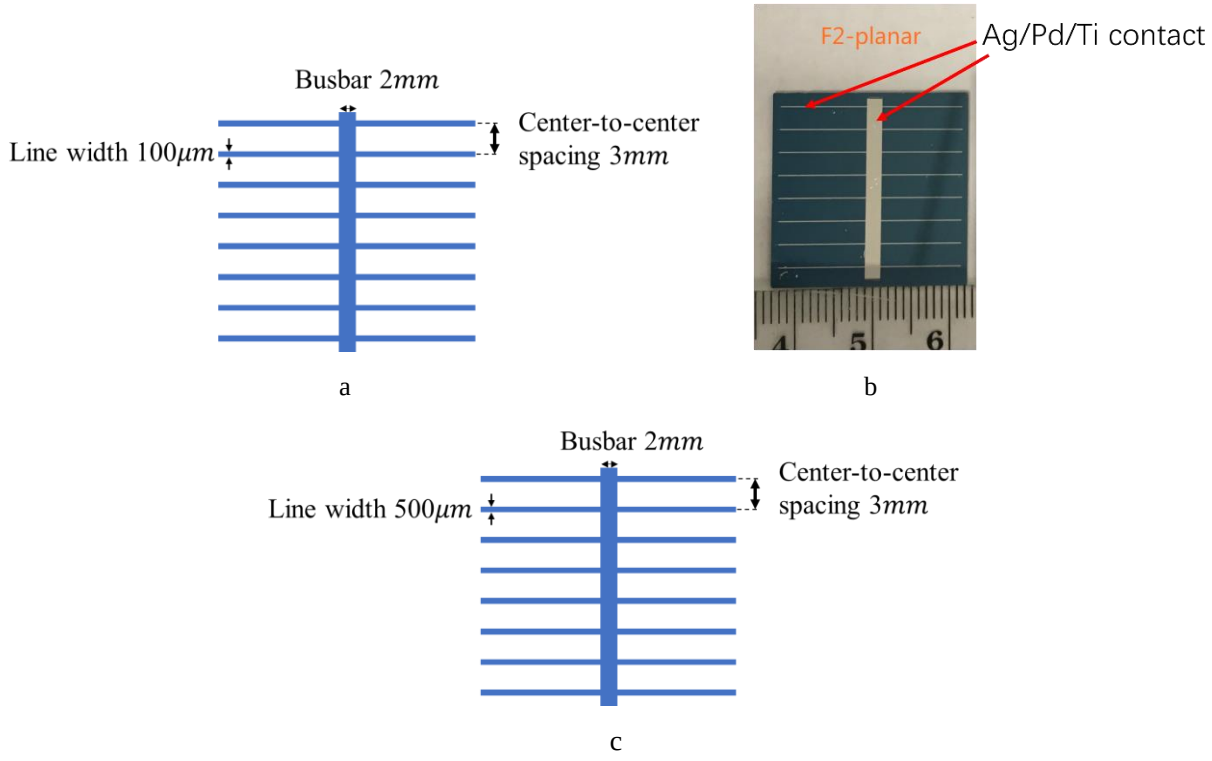
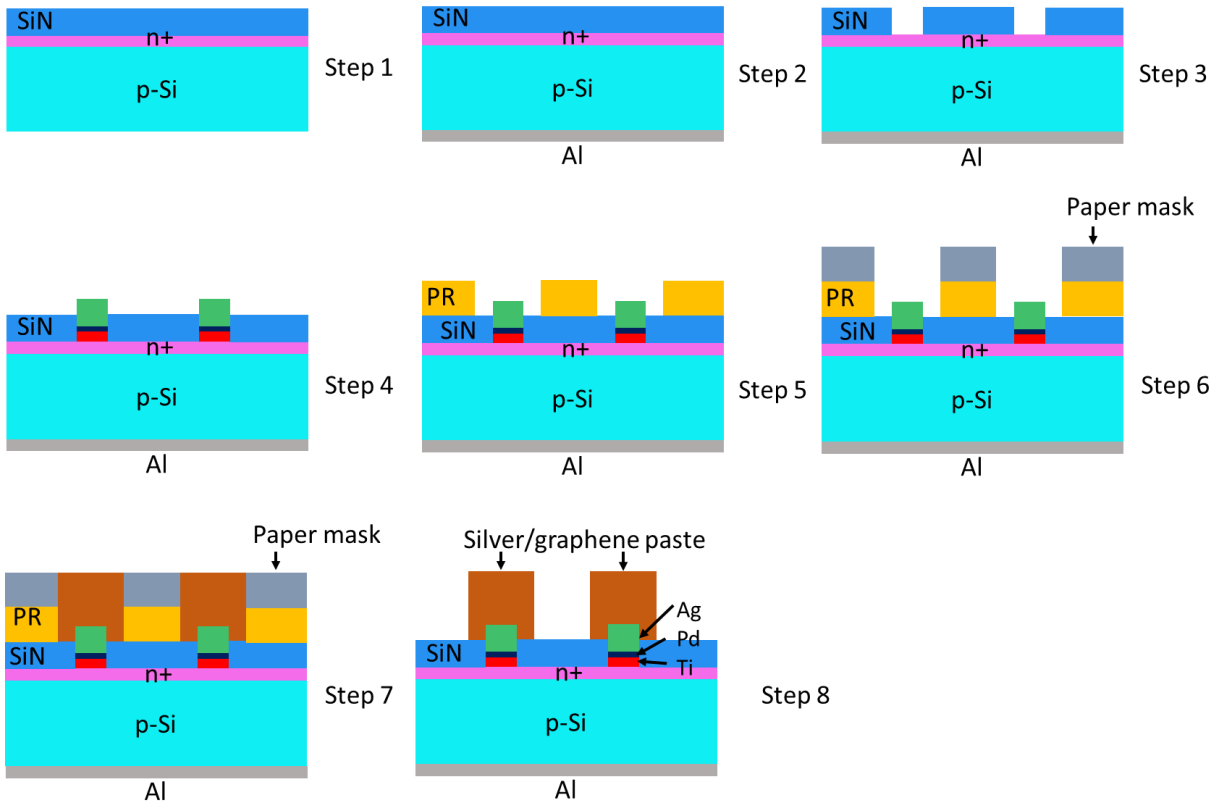
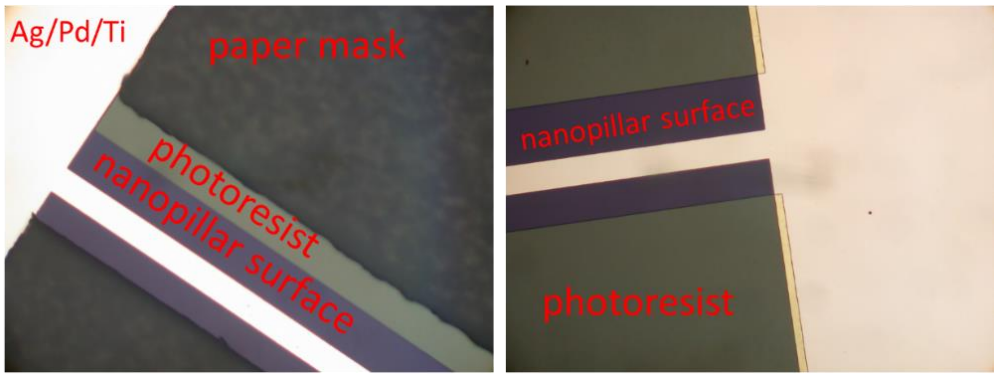


Figure 12. The designed patterns for front-side contact. a) The design of front-side electrode pattern-1 for the Ag/Pd/Ti contact; b) The photo of real sample with Ag/Pd/Ti contact on the top. c) The design of front-side electrode pattern-2 for the printing of silver/graphene paste;



a



b

Figure 13. The fabrication process of solar cells**.** a) Schematic diagram of solar cell contact fabrication process; the thickness of silver (Ag) is ~150nm; the thickness of palladium(Pd) is ~10nm; the thickness of Titanium (Ti) is ~60nm. b) Photos of step 5 & step 6.

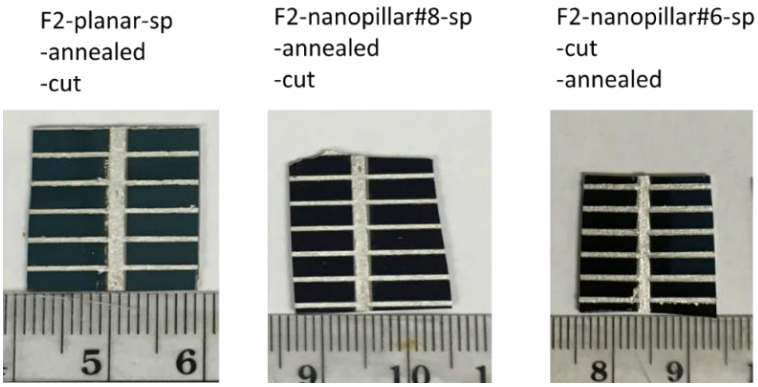


Figure 14. The photos of solar cells after cutting four edges.

3.3 RESULT AND DISCUSSION

In this part, the solar cell with nanopillar structure is referred to as the nanopillar solar cell. The solar cell with flat SiN layer is referred to as the planar solar cell. The planar solar cell is used as a reference cell to confirm the experiment process is optimal and compare the main changes in the parameters of the solar cell. Nanopillar solar cells with different reflectance have been processed in experiments. Table 2 provides the reflectance of different solar cells measured by the He-Ne laser with 633nm wavelength at normal incident angle. Table 3 provides the efficiency measurement results of solar cells including the open-circuit voltage, short-circuit current density, maximum voltage, maximum current, efficiency, fill factor, series resistance, and shunt resistance. The results were measured by the Newport-Oriel Sol3A solar simulator at 1 sun (100 mW/cm^3). Here are some introductions about the rule of sample naming in Table 3. The “F1” and “F2” in the name of sample means Fab1 and Fab2 which stands for the batch number of solar cells. The “-sp” means that the sample has added silver/graphene paste. The “-annealed” in the name of sample means the sample was annealed at 350ºC for 1min in forming gas which was known to passivate

the surface and reduce the surface recombination. Figure 15 shows the effect of annealing in forming gas and support that a proper annealing process benefits the performance of solar cell due to the change of the I-V curve. As shown in Table 3, the open-circuit voltage is slightly improved around 0.002V after annealing process, which should be attributed to the relationship between the open-circuit voltage and recombination. The "-cut" in the name of sample means that sample was cleaved at four edges. The "-sp", "-annealed", "-cut" are ordered by the process sequence in the name of samples. This cutting or cleaving process is demonstrated that it dramatically improves the shunt resistance from tens of Ω to thousands of Ω. As shown in Figure 16 and Figure 17, the I-V curves are improved dramatically after cleaving the four edges.

3.3.1 Open-circuit voltage

According to the efficiency measurement results in Table 3, the open-circuit voltage of nanopillar solar cell (0.577 V) is always lower than the one of the planar cell (0.595 V). And this result consistently appears on different nanopillar solar cells. To understand this phenomenon, two main aspects imposing the limit on the open voltage of solar cell are considered. One aspect is the extrinsic recombination process through the defect levels and at the metal contact region of the solar cell. Another aspect is the intrinsic recombination process like radiative recombination and Auger recombination.[7] The same experiment process and electrode design are proceeded on samples in Table 3. Therefore, the influence of metal contacts should be suppressed. Tested samples were manufactured from the same silicon material and then coated by different thicknesses and structures of SiN layer as AR coating. Thus, the defect levels in bulk silicon substrate should be the same. In short, the extrinsic recombination process should be identical to all samples because of the same fabrication and materials So, the discrepancy of efficiency

between planar and nanopillar solar cells cannot be explained by an extrinsic recombination process. One important fact is that surface damages resulted from RIE which was used to create the nanopillar on the top surface of the solar cell. Although an extra SiN layer was deposited on the top, the surface damages could not be recovered. Those damages may induce a lot of defects which probably accelerates the intrinsic recombination process. This explains why the open-circuit voltage of the nanopillar solar cell is always lower than the planar solar cell.

Table 2. Efficiency table

Sample	Area (cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	V_{max} (cm^2)	J_{max} (mA/cm^2)	FF (%)	**Efficiency (%)**	R_S (Ω)	R_{sh} (Ω)
F2-planar-sp	4.650	0.592	33.66	0.419	26.24	55.23	**11.01**	0.78	39.62
F2-planar-sp -annealed	4.650	0.598	34.41	0.436	27.69	58.63	**12.07**	0.68	60.04
F2-planar-sp -annealed -cut	2.160	0.595	35.40	0.471	32.27	72.20	**15.20**	0.87	2454
F1-nanopillar#6-sp	5.210	0.580	34.03	0.418	28.27	59.97	**11.83**	0.67	83
F1-nanopillar#6-sp -cut	1.890	0.576	36.09	0.459	33.25	73.45	**15.26**	0.95	10598
F1-nanopillar#6-sp -cut -annealed	1.890	0.577	36.73	0.465	33.98	74.58	**15.82**	0.82	4113
F2-nanopillar#8-sp	5.234	0.584	32.19	0.413	24.84	54.60	**10.26**	0.69	54.24
F2-nanopillar#8-sp -annealed	5.234	0.586	33,32	0.413	26.80	56.65	**11.07**	0.71	78.12
F2-nanopillar#8-sp -annealed -cut	2.139	0.585	36.33	0.456	32.98	70.68	**15.03**	0.94	3265

3.3.2 Short-circuit current density

According to the Table 3, the short-circuit current density of the nanopillar solar cell is larger than the one of the planar cell. This enhanced short-circuit current density J_{SC} should be attributed to the SiN-nanopillar structure. First, the SiN-nanopillar solar cell has lower reflectance (<10%) than SiN-planar monolayer (~10%). More electron-hole pairs are generated and collected in SiN-nanopillar solar cell. Second, the nanopillar structure makes the transmission light propagate along a glancing angle in the junction region of the solar cell, providing a better chance for the solar cell to absorb the light. The effective absorption length also increases with glancing propagation of light in junction region. In the ideal case, the short-circuit current density J_{SC} is equal to the photogenerated current density I_{ph} and the open-circuit voltage V_{OC} in equation (4) can be written as

$$V_{OC} = \frac{k_B T}{q} \ln\left(1 + \frac{J_{sc}}{J_0}\right) \tag{7}$$

In the above equation, V_{OC} is proportional to the J_{sc} if the other parameters are the same for different cells. In other words, if one solar cell had high V_{OC}, the J_{sc} should also be high. For our case, the short-circuit current density J_{sc} of nanopillar solar cell is always higher than the planar solar cell. But the open-circuit voltage of the nanopillar solar cell is small compared to the planar solar cell. For now, the nanopillar solar cell can show a similar or a little bit higher efficiency than the planar solar cell. If we assume that an ideal nanopillar solar cell should comply with the equation, a higher efficiency of nanopillar solar cell should be accessible with recovered open-circuit voltage (around 0.6V).

Table 3. Reflectance of solar cells measured by the He-Ne laser with 633nm wavelength at normal incident angle.

Sample	Reflectance
Fab2-planar	10.4%
Fab2-nanopillar#8	7.2%
Fab1-nanopillar#6	4.2%

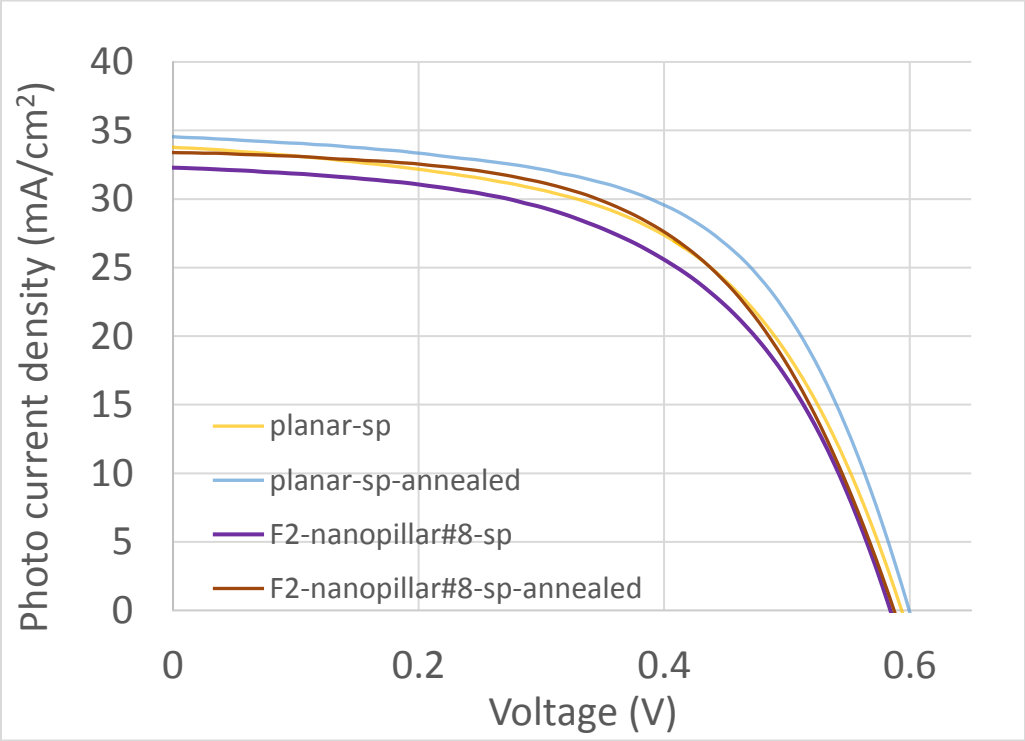


Figure 15. The effect of annealing in forming gas

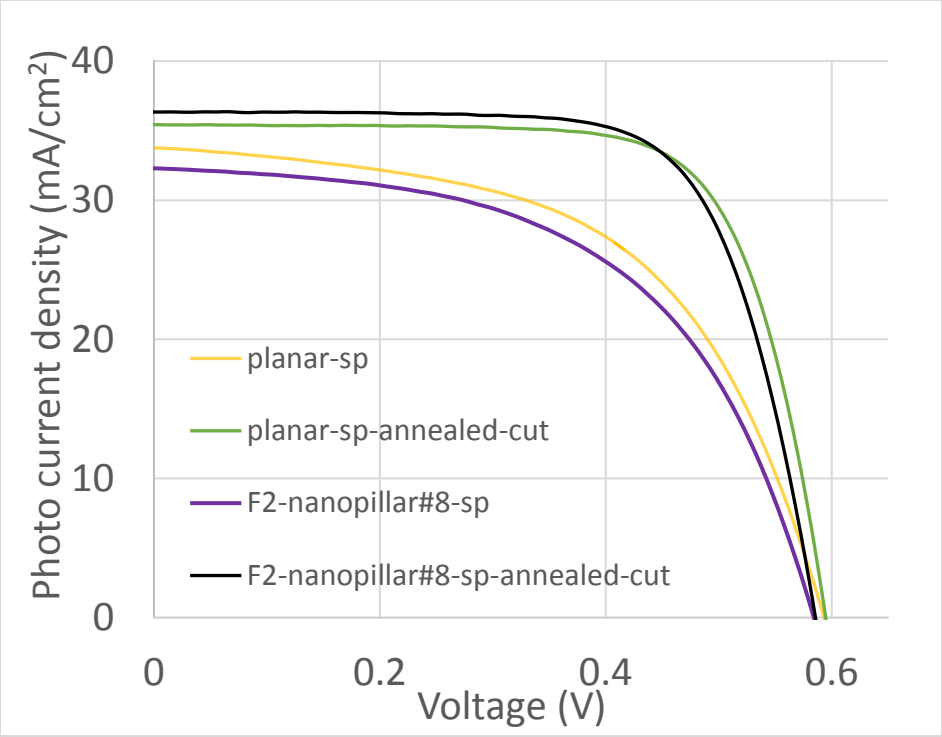


Figure 16. I-V characteristic of F2-nanopillar#8 solar cell and planar solar cell before and after cutting

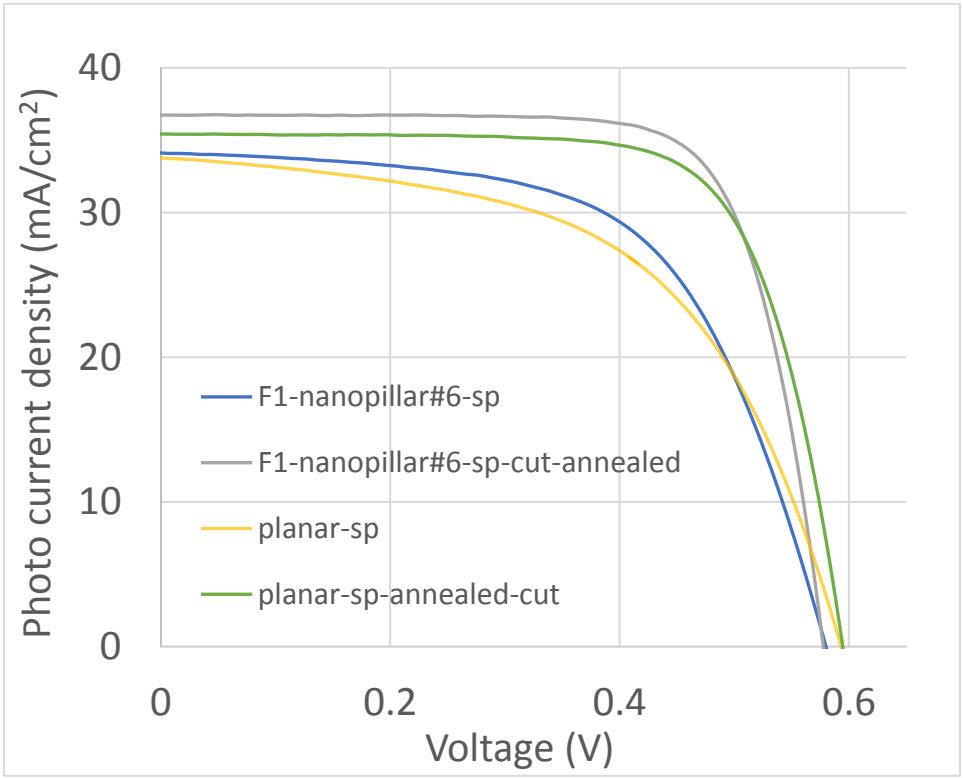


Figure 17. I-V characteristic of F1-nanopillar#6 solar cell and planar solar cell before and after cut

The different SiN-nanopillar structures give different efficiency results. The F2-pillar#5-sp has a 11.6% of reflectance at the wavelength of 633nm. The different SiN nanopillar structures give different efficiency results. Table 4 shows the efficiency of F2-nanopillar#5-sp. The key point is that F2-nanopillar#5 doesn't show a lower reflectance compared to the planar solar cell in Table 3. This indicates the choice of a specific nanopillar structure is critical to achieve the goal of increasing the efficiency. In other words, the surface structure in F1-nanopillar#6 is a better condition compared to F2-nanopillar#8 and F2-nanopillar#8.

Table 4. Efficiency table of nanopillar#5 solar cell

Sample	Area (cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	V_{max} (cm^2)	J_{max} (mA/cm^2)	FF (%)	**Efficiency (%)**	R_S (Ω)	R_{sh} (Ω)
F2-nanopillar#5-sp	5.032	0.582	35,12	0.423	30.00	62.16	**12.70**	0.66	98
F2-nanopillar#5-sp -annealed	5.032	0.586	35.41	0.436	30.29	63.50	**13.19**	0.58	112
F2-nanopillar#5-sp -annealed -cut	1.943	0.581	35.27	0.464	31.76	71.91	**14.74**	0.89	1317

3.3.3 Summary

In this section, we experimentally demonstrate that the efficiency nanopillar solar cells can reach is 15.8% by applying silver/graphene paste on the front-side electrode. The fabrication process is optimal and can give a fair situation for the comparison of planar solar cells and nanopillar solar cells. This indicates the SiN-nanopillar is a promising antireflection layer for a solar cell, which can offer a lower reflectance surface for a broad wavelength window. Furthermore, the performance of solar cells can be improved.

4.0 MOSFET FABRICATION

4.1 INTRODUCTION

In a MOSFET structure, source and drain regions are doped p-n junctions and are commonly formed by gas-phase diffusion of dopant sources. Spin-on dopant (SOD) is an alternative method of forming diffused junctions, offering certain advantages (such as safety and process simplicity). By employing phosphorous SOD we have formed n+-p junctions on p-Si substrate for source and drain regions.

4.2 EXPERIMENT

4.2.1 Diffusion with spin-on dopant

4.2.1.1 Diffusion source

The doping source in this thesis is the spin-on dopant(SOD). Spin-on dopant is chosen as the diffusion technology due to its nontoxic, easy operation, and uniformity in diffusion. SOD P509 is used as the phosphorus dopant source which contained 10.50% dopant compound, 5% SiO_2, water, ethanol, and polymer. The P509 is purchased from Filmtronics and can provide a “N” type

junction with minimum surface damage according to the company's data sheet. The P509 has a shelf life and should be stored at 0 to 5ºC. P509 needs to acclimate to the room temperature prior to use and different bottle sizes need different time. In our case, the 125mL P509 should be placed in room temperature ambient for at least 5 hours to achieve consistent result.

4.2.1.2 Spin-coating and baking

The P509 is spin-coated on the surface of the substrate with patterned mask oxide. The substrate is p-silicon which has 1-10 ohm·cm of resistivity and <100> of orientation with single side polished. The spin speed is 3000rpm for 30 seconds. After spin-coating, the sample is baked at 195ºC for 15min to harden the film. The film looks like a SiO_2 film on substrate after baking. The film thickness is around 485nm according to alpha-step measurement. Table 5 has listed the detail data of alpha-step.

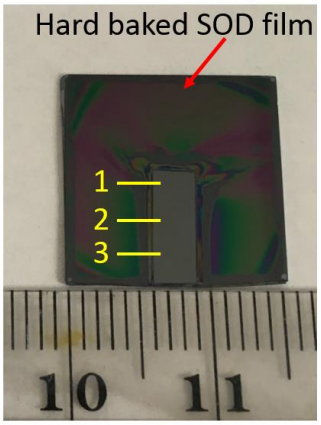


Figure 18. The picture of hard baked SOD film. "1,2,3" in picture stands for different scanning position.

Table 5. Results of Alpha-step

Position	Thickness (nm)
1	654
2	402
3	380
Average	485

4.2.1.3 Diffusion

The diffused samples can be divided into two different type in term of diffusion area. The broad diffused sample means that the whole top surface (polished side) is diffused by SOD and it is designed to do the TLM normally. The patterned diffusion sample means that only the opened window on thick mask oxide is diffused. The different diffusion conditions are listed in Table 6. Samples are heated to desired temperature for 15min in air ambient and are cooled down in air ambient. After diffusion, the SOD layer won't vanish and proper cleaning is needed to remove those remains.

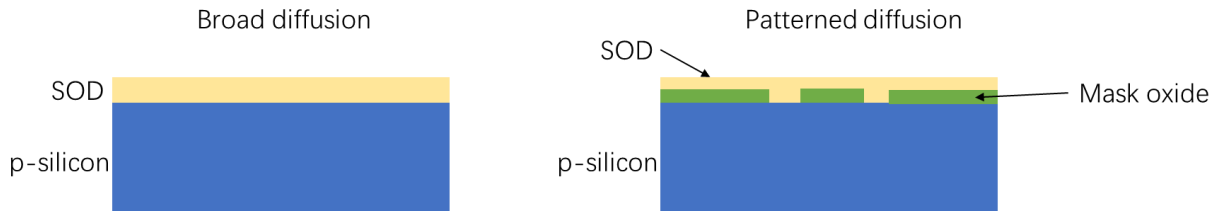


Figure 19. Schematic diagram of the difference of broad diffusion and patterned diffusion.

Table 6. Diffusion condition

Diffusion temperature (°C)	Diffusion time (min)	Ambient
900	15	air
950	15	air
1000	15	air

4.2.1.4 Post-diffusion cleaning

Post-diffusion cleaning is a necessary step for the diffusion by spin-on dopant. The dilute HF is recommended by the Filmtronics. HF solution is well-known to etch away SiO_2. The SOD layer and mask oxide will be removed after soaking HF solution. However, the exposed silicon surface after diluted HF etching is still not ready for metallization. The later experimental results show that the aluminum and n+ diffusion area after diluted HF etching cannot form good Ohmic contact which should be quite easy for aluminum and n+ diffused surface. Because there is a thin unknown layer affecting the formation of Ohmic contact between aluminum and n+ diffused surface. Thus, a proper cleaning step is essential after diluted HF etching. Through the experiment, SC-1 or RCA clean is suitable to make the diffused silicon surface ready for metallization or oxidation. After SC-2 treatment, a thin oxide is chemically grown on the surface of silicon substrate as a protection layer. Table 7 summarizes the detailed steps for post-diffusion cleaning.

Table 7. Post-diffusion cleaning

1	5:1=DI water: HF	5min
2	Rinsing in DI water	5min
3	SC-1: Soaking in mixture of 5:1:1=DI water: NH_4OH: H_2O_2	10min @70ºC
4	Rinsing in DI water	1min
5	SC-2: Soaking in mixture of 6:1:1=DI water: HCl: H_2O_2	10min @70ºC
6	Rinsing in DI water	5min

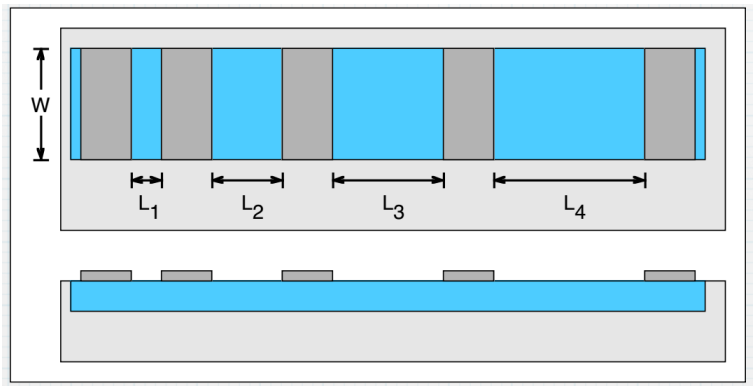
4.2.1.5 Transfer length method (TLM) measurement

Transfer length method (TLM) is used to determine the sheet resistance of diffused samples. The Transfer length method is a well-known method used in semiconductor physics and engineering to evaluate the contact resistance between metal contact and semiconductor, and the sheet resistance of the semiconductor. Figure 20 shows the principle of TLM and schematic diagram of the TLM pattern structure. [8] As shown in Figure 20.b, the measured total resistances between different metal lines are plotted and the fitted curve follows the linear equation below

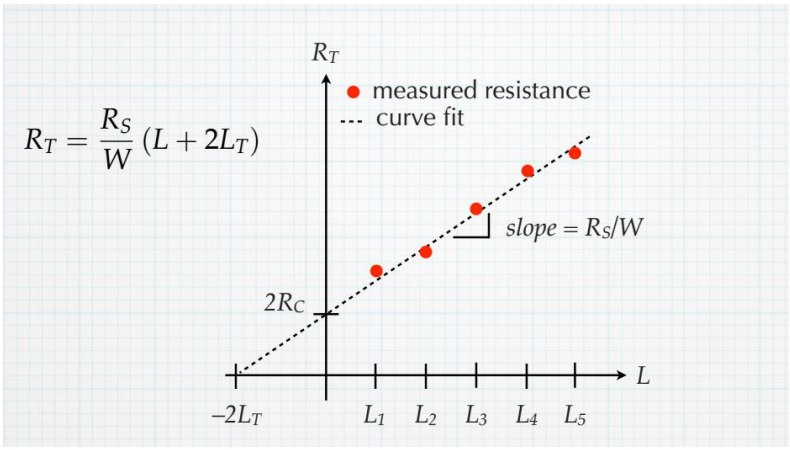
$$R_T = \frac{R_S}{W}(L + 2L_T) \tag{8}$$

where R_T is the total resistance between two nearby metal lines; R_S is the sheet resistance of semiconductor; L is the spacing distance of nearby metal line (the distance between edge and edge like L_1 e.g. in Figure 20.a); W is the width of metal line (as shown in Figure 20.a); L_T is the transfer length which describes the average distance that a carrier can travel beneath the contact before it

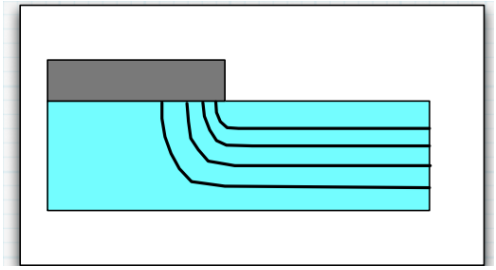
is collected by the contact. This is known as current crowding depicted in Figure 20.c. Thus, $L_T W$ is the effective contact area and the formula for contact resistivity is written as $\rho_C = R_C L_T W$.



a)



b)



c)

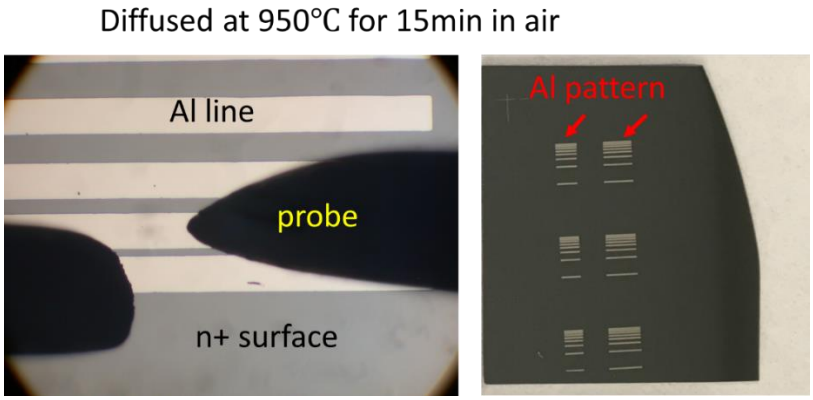
Figure 20. Schematic diagram of principle of TLM. a) W is the length of metal line L is the distance of the metal line. b) R_T is the total measured resistance; R_S is the sheet resistance of semiconductor; L is the spacing; L_T is the transfer length.

Table 8. TLM pattern dimension

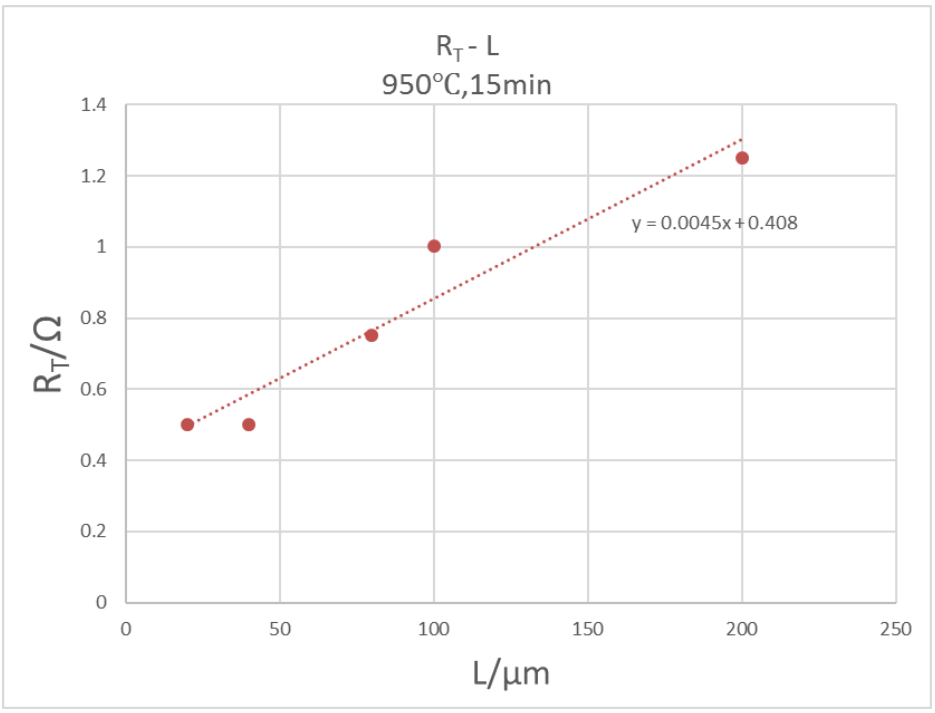
W	L_1, L_2, L_3, L_4, L_5, L_6, L_7
2mm or 1.25mm	20, 40, 80, 100, 200, 400, 1000 (μm)

4.2.1.6 TLM preparation and result

In this part, aluminum is chosen as the metal for TLM. Here is the basic procedure to prepare the TLM pattern for measurement. First, the broad diffusion sample is cleaned by diluted HF solution to remove any residue from SOD and mask oxide. Then, RCA clean is done as listed in Table 6 to remove the residue that cannot be etched by HF solution. Next, the photolithography is done, and the TLM pattern used is same as Figure 21.a. Specific dimension is summarized in Table 8. After developing, the sample is etched by dilute BHF prior to the aluminum lift-off deposition. Aluminum is thermally evaporated from a tungsten boat in 10^{-5} torr of pressure. There is no annealing process after lift-off process. Figure 21 is the TLM result for the sample diffused at 950ºC for 15min in air ambient.



a b



c

Figure 21. The graphs of TLM measurement. a) The photo of measurement. b) The photo of real sample; c) The plotted curve of total resistance and the spacing length (long Al pattern W=2mm).

Calculation:

For long Al pattern: W=2 mm

According to the equation (8)

Sheet resistance: R_S=slope×W= 0.0045×2000 = 9 Ω/□

Contact resistance: R_C= 0.408/2 = 0.204 Ω

L_T=R_C/slope= 0.204/0.0045 =45.3 μm

Contact resistivity: ρ_C= $L_T R_C$W= 0.00453×0.204×0.2 =1.85×10^{-4} Ω·cm^2

In the same way, the calculation results of other diffusion temperature cases can be obtained. Table 9 summarizes the calculation results of different temperature.

Table 9. Results of TLM measurement

T (ºC)	W (mm)	R_S (Ω/□)	L_T (μm)	ρ_C (Ω·cm^2)
900	1.25	26.5	60.6	9.7×10^{-4}
950	2	9	45.3	1.85×10^{-4}
1000	2	7.6	42.1	1.35×10^{-4}

4.2.1.7 Stain etching

To learn more about characteristics of diffused junction, wet-chemical etching of silicon is used to delineate the p-n junction. After reviewing literature[9], 25 mL of nitric acid, 5 mL of hydrofluoric acid and 40 mL of deionized water is chosen as the solution for delineation. The etching time is controlled at around 90 seconds. Figure 22 has shown the SEM images taken at cross-section view. The depth of the delineated junction can be evaluated as ~290nm from the image. Thus, the junction depth of other diffusion conditions should keep in this level or shallower than 290nm.

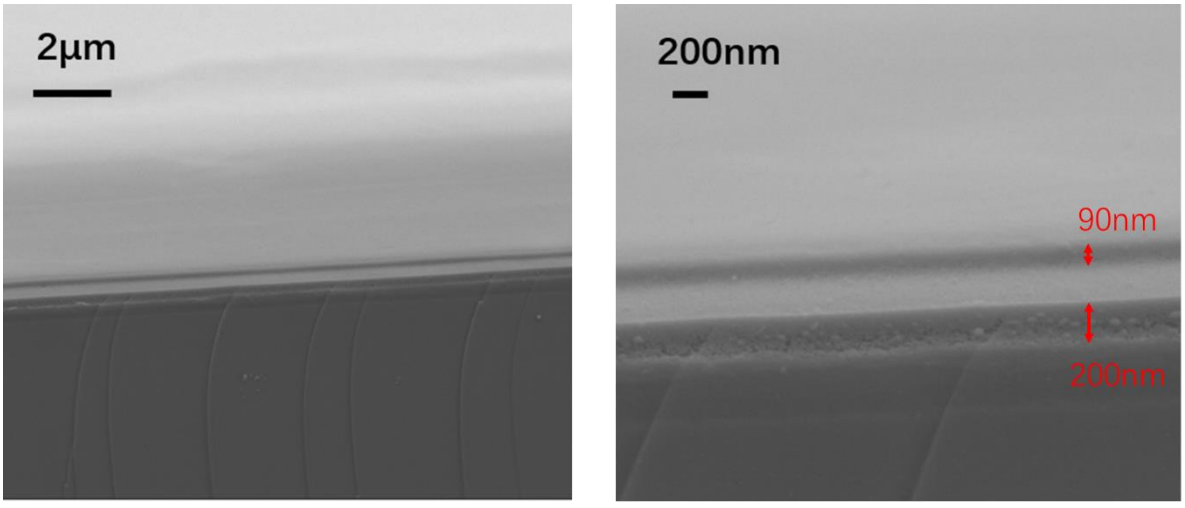
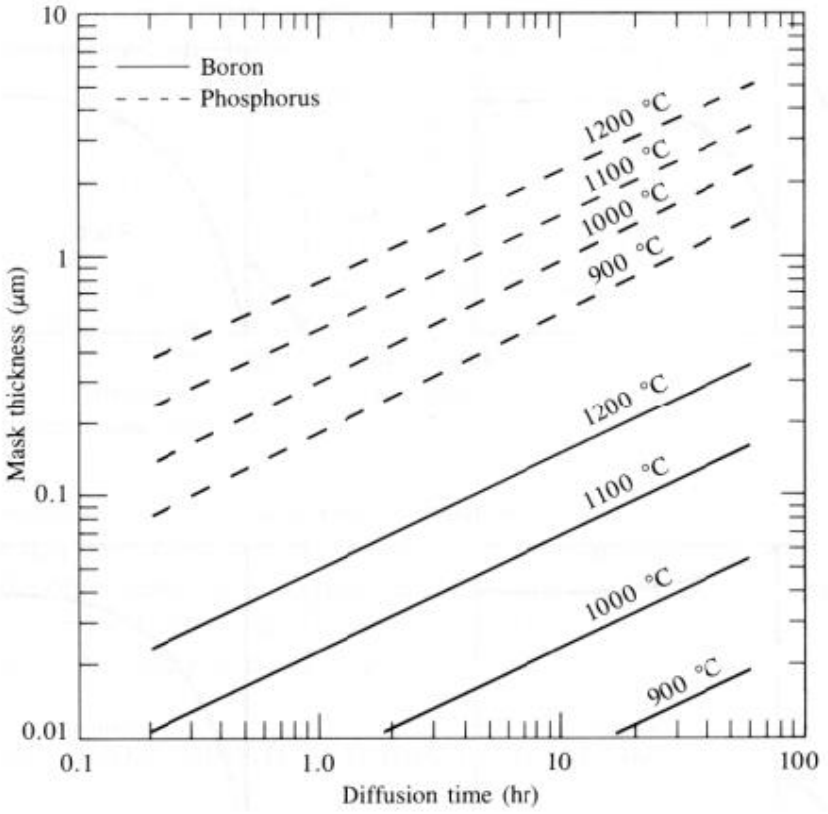


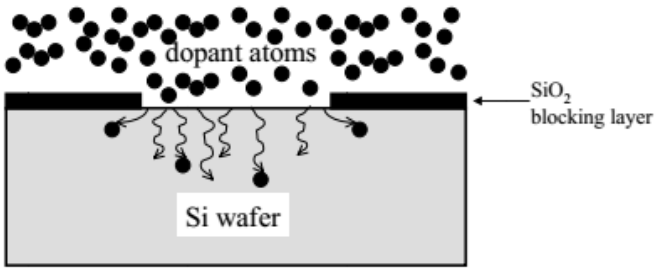
Figure 22. SEM images: cross-section view of p-n junction diffused at 1000ºC for 15min

4.2.2 Diffusion mask

To define the n+ region as drain and source area of MOSFET, the diffusion is commonly blocked at selected areas of substrate with a dielectric mask like SiO_2. According to the reference, the minimum SiO_2 mask thickness for successful diffusion of phosphorus on silicon is determined from the Figure 23.a. [10] According to reference, the minimum oxide thickness for 1000ºC, 15min is around 134nm, which is compatible with the value read from the Figure 23.b. However, it should be safe that the mask oxide thickness reaches up to 200nm or more.



a



b

Figure 23. Mask oxide and diffusion. a) The curve that can be used to determine the essential mask oxide thickness at certain diffusion temperature and time. b) The schematic picture of the function of mask oxide;

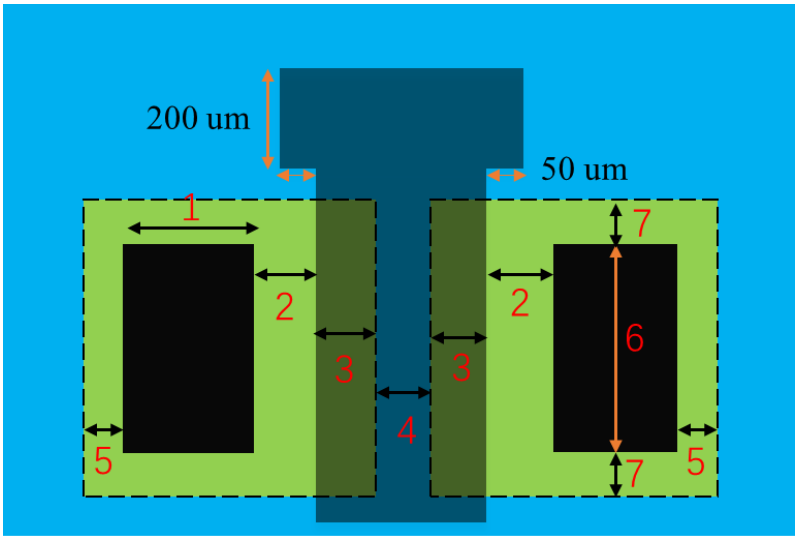
To grow enough thick oxide, the p-silicon substrate is oxidized at 1000ºC for up to 16 hours in total. The p-silicon substrate has 1-10 Ω·cm of resistivity and <100> of orientation with single side polished. Table 1 records the cleaning step before oxidation. The oxidation is done at 1000ºC for 5, 8 and 16 hours in air ambient. The total oxide thickness is measured by alpha-step. The measured step is created by photolithography following a diluted BHF etching. It also helps to calibrate the etching rate of the diluted BHF solution (~20nm thermal grown oxide per minute), which is used as a reference to chemically etch the diffusion window on mask oxide later.

Table 10. Oxide thickness for different time at 1000ºC

T (ºC)	Time (hours)	Measured oxide thickness (nm)
1000	5	138
1000	8	166
1000	16	257

4.2.3 Photo mask design and pattern transfer process

The photo masks used in photolithography are plastic masks ordered from company. The mask for making MOSFET is drawn by AutoCAD, and the main parameter is the channel length which has three different values of 30μm, 50μm, and 70μm. Figure 24.a shows the schematic diagram of top view of the MOSFET. The critical parameter is the channel length which corresponds to the dimension of position 4 in Figure 24.a. The variations of dimension on other positions are designed to give enough space for the alignment of multilevel masks and ensure that there is no dead length in the final channel region caused by the mismatch between gate electrode and channel region. The ratio of channel width and channel length varies from 2.14 to 6.67. The designed patterns are transferred by a combination of photolithography and chemical etching. The chemical etching is done by the diluted BHF (Buffered hydrofluoric acid), which is used as the oxide etchant to open designed windows in oxide layer.



a

Device number

position	4		1	2	3	5	6	7
unit/μm								
	30/50/70	a1	100	20	20	50	50	50
	30/50/70	a2	100	40	20	50	50	50
	30/50/70	a3	100	40	40	50	50	50
	30/50/70	a4	100	20	40	50	50	50
	30/50/70	a5	100	60	60	50	50	50
	30/50/70	b1	100	20	20	50	100	50
	30/50/70	b2	100	40	20	50	100	50
	30/50/70	b3	100	40	40	50	100	50
	30/50/70	b4	100	20	40	50	100	50
	30/50/70	b5	100	60	60	50	100	50
	30/50/70	c1	200	20	20	50	50	50
	30/50/70	c2	200	40	20	50	50	50
	30/50/70	c3	200	40	40	50	50	50
	30/50/70	c4	200	20	40	50	50	50
	30/50/70	c5	200	60	60	50	50	50
	30/50/70	d1	200	20	20	50	100	50
	30/50/70	d2	200	40	20	50	100	50
	30/50/70	d3	200	40	40	50	100	50
	30/50/70	d4	200	20	40	50	100	50
	30/50/70	d5	200	60	60	50	100	50

b

Figure 24. The dimensions of designed MOSFET. a) Schematic diagram of MOSFET; Blue area stands for the thin oxide surface. Green area stands for the n+ regions which are the drain and source region. Black and T type area are the metal electrodes of MOSFET. b) the size table of MOSFET; Position 1-7 correspond to the position number in a).

4.2.4 Fabrication of MOSFET

The fabrication procedure is organized by a photomask sequence.

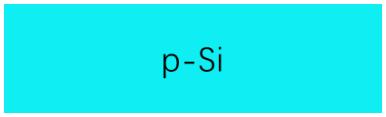
Mask 1: Fabrication is started from cleaning the p-type silicon substrate with mask oxide. This oxide helps to prevent the phosphorus dopant diffusing into the undesired region. After growing the mask oxide, the photolithography is done. First, the photoresist (S1827) is spin-coated on the substrate and exposed by Mask Aligner MJB3. Next, the diluted BHF (Buffered Hydrofluoric acid) is used to etch the mask oxide for defining the rectangular diffused area. Third, SOD P509 is spin-coated on the substrate after removing the PR of previous step. Fourth, a sample with hardened SOD P509 layer is diffused at certain temperature (like 900ºC,950ºC or 1000ºC) for 15min. Fifth,

the diluted HF (1:5 DI water) is used to etch the SOD and mask oxide away following a RCA clean or SC-1 procedure. After this step, the sample is oxidized at 950ºC, 30min in air ambient to grow a thin oxide layer (around 23nm) as gate oxide of MOSFET.

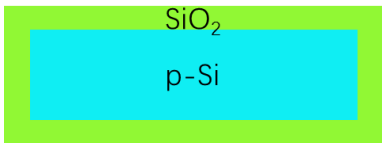
Mask 2: Mask 2 is designed to define the areas for source and drain contacts for the MOSFET. The pattern of Mask 2 is transferred by photolithography. The thin oxide is etched by diluted BHF at a rate of around 20nm/min. After BHF etching, aluminum is thermally evaporated to those areas to form source and drain electrodes following a lift-off process.

Mask 3: Mask 3 is designed to define the window for gate electrode of MOSFET. The pattern of Mask 3is transferred by photolithograph. After developing the photoresist, aluminum is lift-off deposition as the gate electrode.

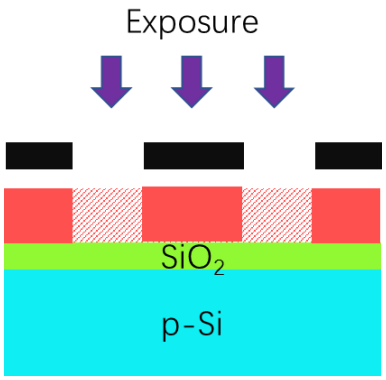
Figure 25 demonstrates the main process flow to fabricate a MOSFET.



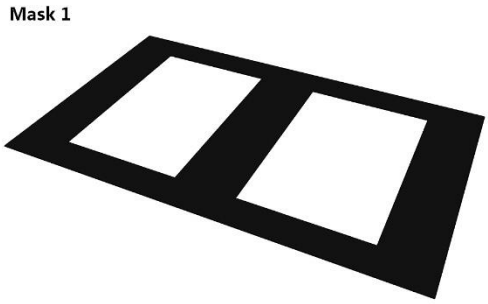
Clean substrate



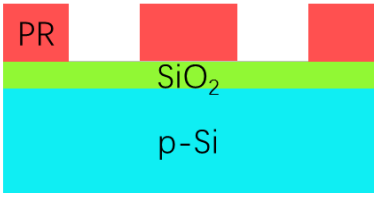
Oxidation for Mask Oxide



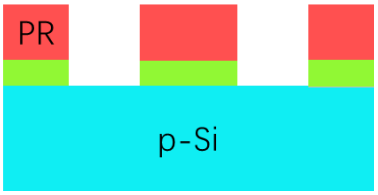
Diffusion window patterned for n+ regions



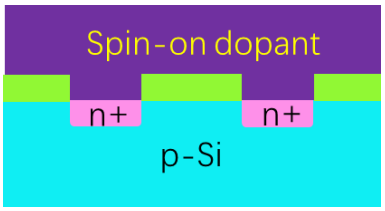
Schematic diagram of Mask 1 for opening diffusion windows



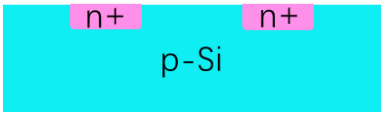
Developing



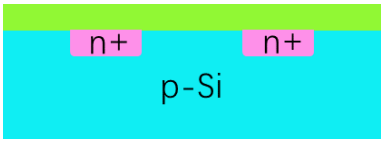
Chemical etching



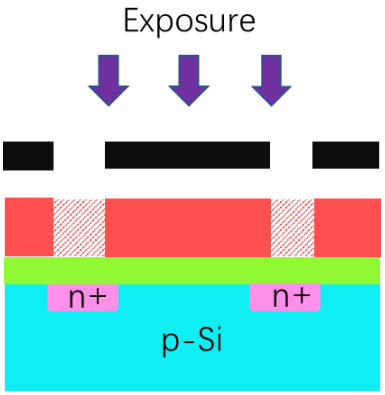
Spin-coating SOD and diffusion



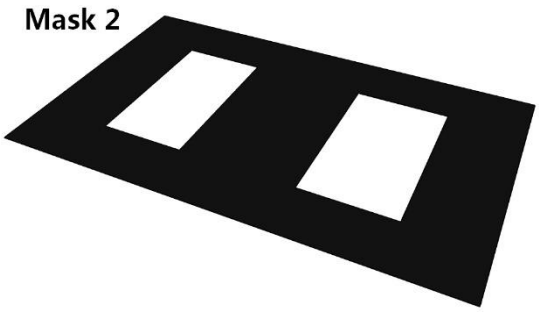
Removing the oxide and SOD and cleaning the silicon surface



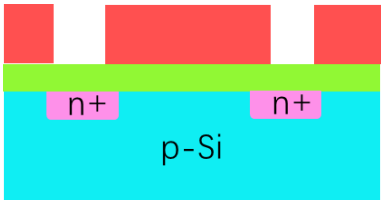
Growing thin oxide as insulating layer



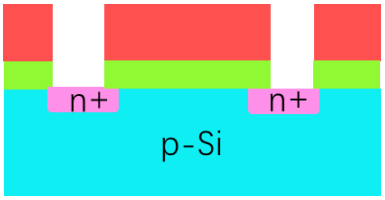
Patterning for drain and source contacts



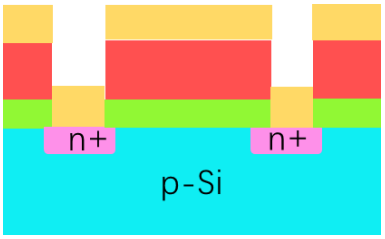
Schematic diagram of Mask 2 for drain and source contacts



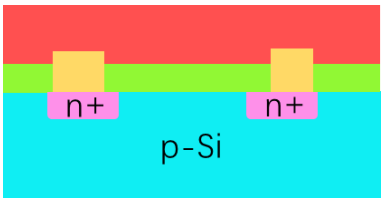
Developing



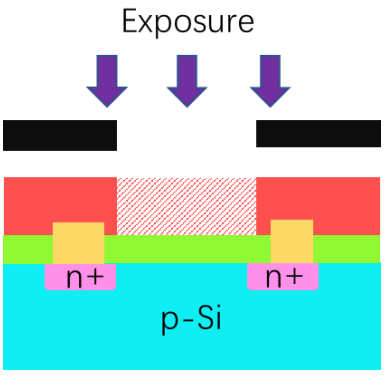
Chemical etching



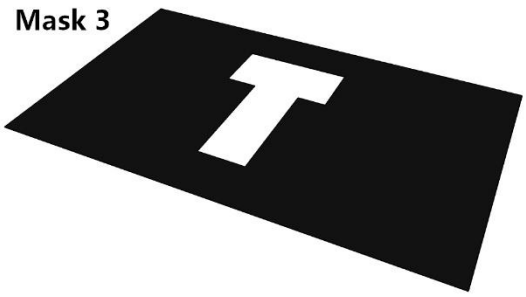
Aluminum deposition



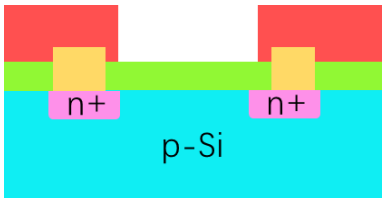
Photoresist spin-coating



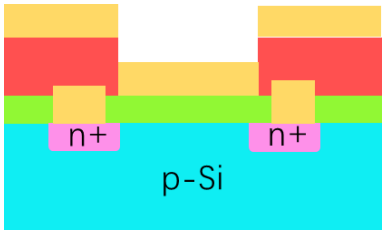
Patterning for the gate electrode



Schematic diagram of Mask 3 for the gate electrode



Developing



Aluminum deposition

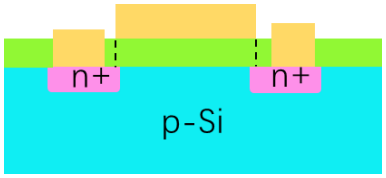


Figure 25. The schematic fabrication process flow of MOSFET

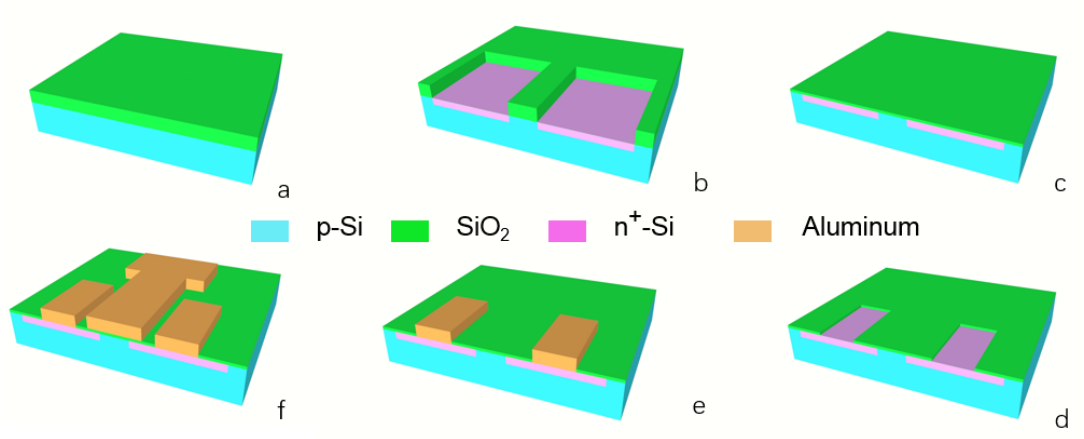


Figure 26. 3D schematic diagram of fabrication process of MOSFET. a) p-silicon substrate with mask oxide. b) n+ regions after diffusion. c) After growing the gate oxide. d) open window for drain and source contacts. e) metallization. f) final structure after depositing the gate electrode.

4.3 CHARACTERIZATION OF MOSFET

4.3.1 Measurement setup

HP 4145B is the I-V machine used to measure the I-V characteristics of FET. Three probes gently touch the drain, source and gate electrode in single MOSFET, as shown in Figure 27. The parameters like V_G, V_{DS} can be programmed in HP4145B.

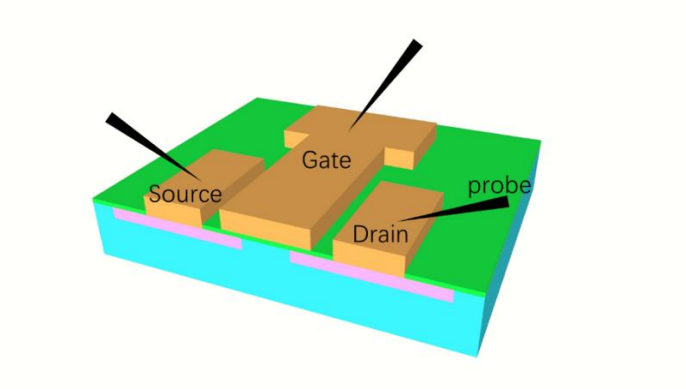


Figure 27. Schematic diagram of the probe setup.

4.3.2 Electrical characterization

Fabrication 3: The substrate is p-Si (1-10 Ω·cm, <100>) with 257nm mask oxide. The Fab3-sample is diffused at 950ºC for 15min in air ambient. The Post-diffusion cleaning is done as shown in Table 7. Then, the sample is immediately oxidized at 950ºC for 30min without removing the thin oxide formed by SC-2. Other processes are the same as the description in Chapter 4.2. Figure 28.a demonstrates the global picture of the sample with a channel length of 50μm. The "a, b, c, d" is used to name and identify the devices, a1 to a5 is from up to down. Figure 28.b shows the photo of the MOSFET (Fab3-a1) microscope with tungsten probes. The channel width W is 150μm, channel length L is 45μm in Figure 28.b. The ratio of channel width and channel length W/L is 3.3.

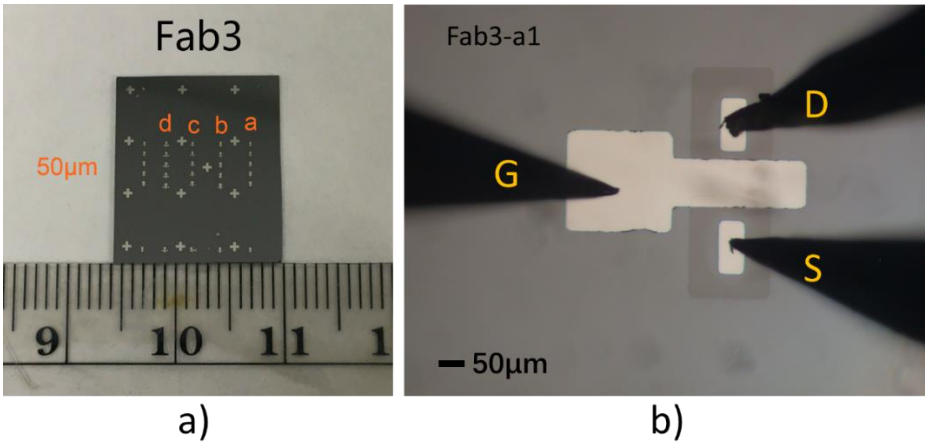


Figure 28. MOSFET photo. a) The photos of MOSFET devices (Fab3); b) The photo of a MOSFET device (Fab3-a1), the ratio of channel width and channel length W/L is 3.3.

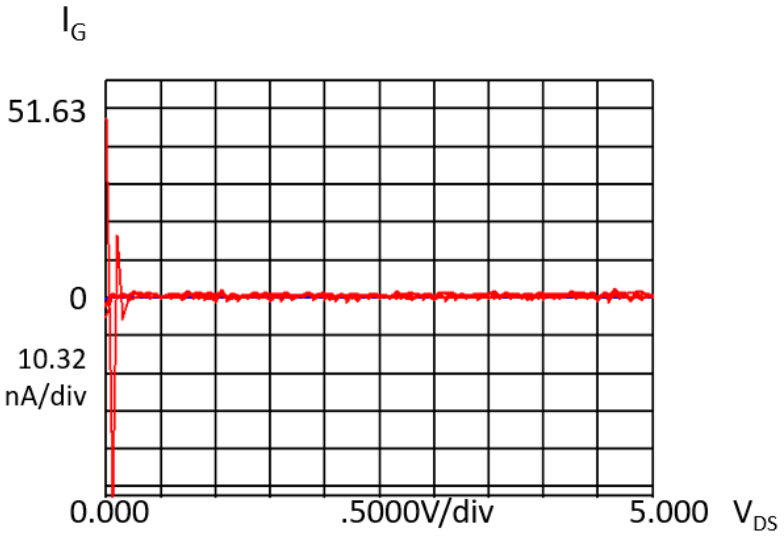


Figure 29. The curve of I_G-V_{DS} demonstrates the gate oxide don't have leakage. V_{DS} starts from 0V to 5V; V_{GS} starts from 0V to 2V; the shown curves are a superposition result of different gate voltages.

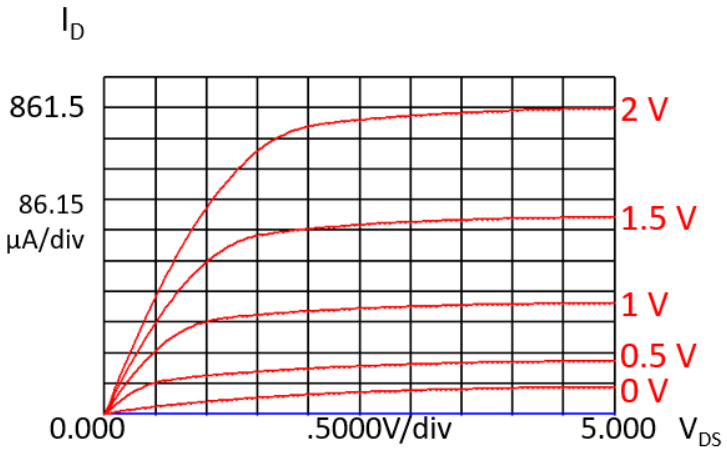


Figure 30. I-V characteristic of the MOSFET(Fab3-a1)

Important parameters can be extracted from I-V characteristic of MOSFET. Figure 29 is the curve of I_G and V_{DS} which demonstrates the gate oxide is not leak. Table 11 is the data read from Figure 30. The formula and equations used to calculate the extrapolated threshold voltage, k_n and μ_n are listed below.

Table 11. Data points at the saturation region of MOSFET

$I_D\ (\mu A)$	$V_{GS}(V)$	$V_{DS}\ (V)$
861.5	2	5
551.4	1.5	5
311	1	5
147.3	0.5	5

$$k_n = \mu_n C_{ox}\left(\frac{W}{L}\right) \tag{9}$$

$$\sqrt{I_D} = \sqrt{\frac{1}{2}k_n(V_{GS} - V_T)} \tag{10}$$

$$\sqrt{\frac{k_n}{2}} = \frac{\sqrt{I_{D1}} - \sqrt{I_{D2}}}{V_{GS1} - V_{GS2}} = \frac{\sqrt{861.5\ \mu A} - \sqrt{551.4\ \mu A}}{2\ V - 1.5\ V} = 11.7 \times\ 10^{-3}\frac{A^{\frac{1}{2}}}{V} \tag{11}$$

$$k_n = 274\ \mu A/V^2$$

$$V_{T0} = V_{GS} - \sqrt{\frac{2 \cdot I_D}{k_n}} = 2\ V - \sqrt{\frac{2 \cdot 861.5\ \mu A}{k_n}} = -0.57\ V \quad (12)$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}\ \frac{F}{m}}{23 \times 10^{-9} m} = 1.5 * 10^{-3}\ \frac{\mathrm{F}}{m^2} \quad (13)$$

$$k_n = \mu_n C_{ox} \left(\frac{W}{L}\right) \quad (14)$$

Table 12. Summary table

Device	$(k_n/2)^{1/2}$	V_{T0} (V)	W/L	k_n (μA/V^2)	μ_n (cm^2/V·s)
Fab3-a1	11.498	-0.55	3.3	264	533
Fab3-a2	10.944	-0.72	3.1	239.5	515
Fab3-b2	12.192	-0.63	4.2	297.3	472

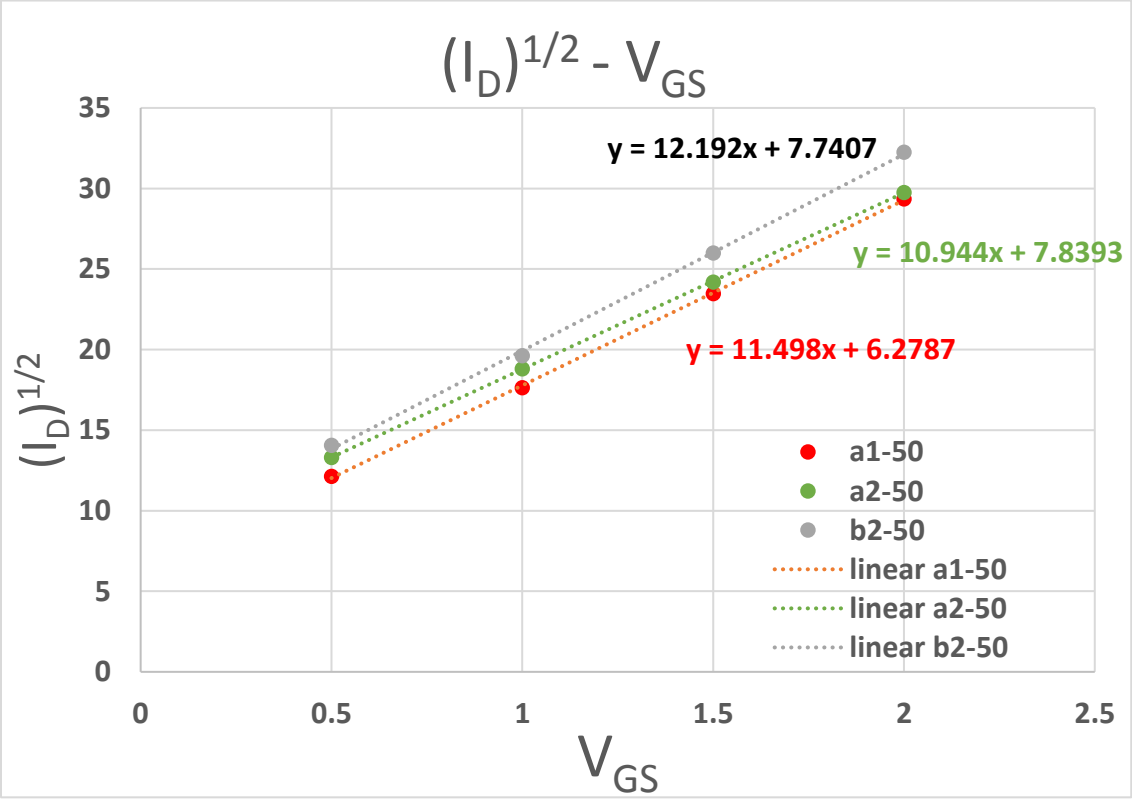


Figure 31. The plotted curve of V_{GS} - $(I_D)^{1/2}$

In Table 12, an important result is that the extrapolated threshold voltage is negative, which means the device fabricated is depletion n-MOSFET. However, in our design, the fabricated MOSFET should be the enhancement n-MOSFET. It's better to refer to it as subthreshold leakage. Fabrication 1 and Fabrication 2 also have similar negative extrapolated threshold voltage or subthreshold leakage. In fabrication 1, the thickness of mask oxide is 166 nm and the Fab1-sample is diffused at the same condition as fabrication 3, 950ºC for 15min in air ambient. In fabrication 2, the thickness of mask oxide is 257 nm and the sample also is diffused at same condition as fabrication 3, 950ºC for 15min in air ambient. Comparing the results of fabrication 1 and fabrication 2, the thickness of mask oxide is not the factor that results in this negative extrapolated threshold voltage. In fact, it demonstrates that 257 nm or 166 nm of mask oxide for phosphorus diffusion at 950ºC for 15min in air ambient is more than sufficient. Thus, the negative extrapolated threshold voltage doesn't result from the n-type channel beneath the gate oxide created during diffusion process. Thus, the reason causing negative extrapolated threshold voltage is not the fixed or trapped charges at the interface of gate oxide and p-silicon in the channel region. To solve this unexpected negative extrapolated threshold voltage, the source of fixed charges must be identified. Charge contamination may come from two parts. One possible contamination source might be that the silicon surface is not cleaned well before growing gate oxide or is recontaminated after surface cleaning process. Bare silicon surface is very reactive and easily contaminated immediately. Another possible contamination source might be the ion contamination from the quartz tube and air ambient during the oxidation for gate oxide. Fabrication 3 has modified and optimized the post-diffusion cleaning to avoid the recontamination before growing gate oxide. The main difference is that the diluted BHF etching is cancelled before oxidation, which is believed to be responsible for the recontamination. However, the I-V characterization doesn't show any significant change. The

negative extrapolated threshold voltage of Fab 3 keeps in the similar level as Fab 1&2. Therefore, surface cleaning process is not the dominant factor for this negative extrapolated threshold voltage. The ion contamination should mainly come from the oxidation process. This is the next problem we want to solve.

4.4 SUMMARY

In this section, we have formed n+-p junctions on p-Si substrate by applying phosphorous SOD. The resulting junction properties were characterized by transfer-length method (TLM). By fabricating n-MOS structure we also demonstrated excellent FET characteristics as measured by device transconductance parameter of k_n and carrier mobility of μ_n.

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