Exploring the Surface Interactions of Graphene for Applications in Dual-Sided Field Effect Transistors

by

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Jorge Torres Quiñones, PhD
University of Pittsburgh, 2024

Graphene is a two-dimensional (2D) material with superior electrical properties that make it attractive for electronic applications. These applications often desire higher transistor densities, leading to the formulation of a dual-sided wafer. Its large surface area to volume ratio renders it extremely susceptible to surface effects, necessitating increased understanding to develop higher quality devices. Large-scale incorporation of graphene requires a growth and transfer process that can affect its properties. It is essential to understand how graphene may be transferred cleanly for improved reliability and CMOS compatibility. Additionally, strong adhesion is desired to withstand the stresses a device can undergo during fabrication and operation. How graphene's electrical conduction is modulated by different substrates is crucial to improving the design and reliability of graphene-based devices. Recent advances in graphene transfer and how these improvements can be incorporated will be discussed. Easy to implement solutions include ammonium persulfate etching of copper foil, heated acetic acid, and lower molecular weight PMMA. The adhesion energy of graphene to SiO_2, Si_3N_4, gold, and platinum substrates was investigated using the intercalation of nanoparticles method. A key aspect of the adhesion energy was how polarizable the interface material was, with increasing polarization bringing larger adhesion energies. Gold was found to have the largest adhesion energy at 7687.10 mJ m^{-2}. Interfacial effects on the electrical conduction of single layer graphene (SLG) and multilayer graphene (MLG) were investigated by determining the temperature coefficient of resistance (TCR). The strongest effect without surface modifications was for SLG on Si_3N_4, where the sheet resistance changed 0.393%/K. The modifications strongly affected graphene's properties and offered avenues for improvement, showing a 0.456% change for SLG on SiO_2. The results of these

experiments were used to develop a dual-sided graphene field effect transistor (GFET). GFETs were developed on both sides of the wafer, with electron and hole mobilities measured up to 1259 and 512 cm^2 V^{-1} s^{-1}. The fabrication of these transistors allows for new device architectures to create compact and versatile devices. The devices are CMOS compatible and can offer higher transistor densities than previously possible.

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Preface

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To my girlfriend, Sierra. Thank you for being with me, for sharing my hopes and dreams, for pushing me when I am feeling down, and being a wonderful girlfriend. I hope to continue experiencing the world with you, both in far off places and in the deepest parts of our minds. To share in life is truly sacred, and I am happy to share it with you.

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1.0 Introduction

Graphene, a two-dimensional (2D) carbon-based material with a hexagonal lattice configuration, was a groundbreaking discovery in 2004. The pioneering work of Novoselov et al., who first transferred few layer graphene by repeated peeling of graphite, marked the beginning of a new era in materials science and nanotechnology [1]. Since then, graphene has been extensively studied, with a focus on its growth and transfer processes, and the unique properties and applications that emerge from its 2D confinement. Despite the exploration of other 2D materials, graphene remains a major research area due to its versatile properties.

Graphene has a unique sp3 bond structure that gives rise to its many properties. It has a measured in-plane thermal conductivity of up to 5600 $Wm^{-1}K^{-1}$ and has a high Seebeck coefficient that enables its use for thermally derived power [2, 3]. It has one of the highest mobilities known, reaching over 2E5 cm^2/Vs at room temperature, allowing it to be highly conductive [4]. Graphene has a theoretical conductivity as high as 1E5 S/m [5]. While its absolute optical absorption of ~2% is relatively low, it is astounding that such a thin material can absorb so much light. Additionally, graphene has a Young's modulus of 1TPa, making it about 200 times stronger than steel and several times harder than diamond [6]. As for its chemical properties, it possesses antibacterial properties and can be used as a chemical sieve to allow the passage of some compounds while blocking others [7]. These miraculous properties have given rise to numerous applications.

The exceptional properties of graphene have led to its application in diverse fields such as medicine, chemistry, and electronics, showcasing its potential for transformative impact. In medicine, graphene has been utilized to detect various viruses and bacteria, demonstrating its potential in disease diagnosis [8]. Similarly, graphene has been employed as a gas sensor and a

catalytic support in the chemical field, highlighting its role in environmental monitoring and chemical reactions [9, 10]. In electronics, graphene's high-frequency transistors, memory devices, and improved battery technology can revolutionize the industry [11-13]. The broad spectrum of applications underscores the unique value of graphene.

Despite graphene's numerous excellent properties and practical applications, its full potential is yet to be realized. The road to unlocking this potential has its challenges. The heavy influence of graphene's growth and transfer processes and its surface interactions pose significant hurdles. The processes required to transfer graphene onto various surfaces need to be optimized for the best performance in any given application. Graphene's ultrahigh surface area to volume ratio underscores the importance of external interfacing in determining material behavior and device performance. The adhesion properties of graphene change substantially based on the choice of substrate. Any surface modifications performed can significantly alter graphene's critical electrical properties. Therefore, a better understanding of the substrate's influence on graphene is crucial to maximize the performance of graphene-based devices. This optimization can lead to better integration with existing complementary metal oxide semiconductor (CMOS) technology, but it's a complex task that requires careful consideration and research.

The processes needed to use graphene differ slightly from those of CMOS technology. Conventional CMOS technology involves thin film grown directly on the substrate via chemical vapor deposition (CVD) or electron-beam (e-beam) evaporation processes, which can then be subsequently patterned. One example is CVD-grown polysilicon, which yields a uniform thin film that helps enable CMOS-based devices [14]. Metal contacts are typically fabricated using e-beam evaporation due to the process control available and resulting uniform thin films. However, graphene is difficult to grow or deposit directly on a desired substrate, especially with non-metallic

substrates [15]. Thus, graphene must be grown on a different substrate, followed by the transfer of graphene from the growth substrate to the target substrate. Device performance can be detrimentally affected by these growth and transfer processes. While several methods have been discovered to grow graphene, the most prominent is the CVD growth of graphene on a transition metal substrate. This growth process can be tuned to provide high-quality graphene, though the choice of growth substrate thus requires a transfer process to allow for integration into CMOS devices. The transfer is typically done using a wet process, in which a polymer covers the graphene. The polymer/graphene/metal material is then set in a chemical bath to etch away the metal, and the resulting polymer/graphene material can be transferred onto the target substrate after cleaning. After transfer, the polymer can then be removed via solvent. This transfer process is essential to providing graphene-based devices, though the process often leaves residues and cause mechanical deformations that negatively affect the performance of the transferred graphene. Consequently, careful consideration must be made to the growth and transfer processes to obtain the best graphene performance possible.

Following the successful transfer of graphene to the desired substrate, studies are needed to determine the usability of graphene for various applications. Due to graphene's 2D nature, it is highly affected by the interactions between itself and the material it contacts. These external interfaces can drastically alter graphene's performance characteristics, thus necessitating an understanding of how such interfaces may affect the operation of a graphene device. Adhesion studies will help show the reliability of graphene-based devices, with solid results improving the contact uniformity of graphene. Additionally, such interfaces affect the electrical conduction of graphene, providing the need for information on how one can alleviate any ill effects or use the effects to an advantage. The study of how graphene resistivity responds to temperature increases

as a result of different surface interactions can elucidate the electrical response of graphene to different interfaces. The results of these experiments can inform future design and fabrications processes as to which materials may work best with graphene, diminishing any harmful effects while maximizing any beneficial effects. This will enable the design and fabrication of graphene field effect transistor (GFET) on both sides of a wafer's surface, which we term dual-sided GFETs (DSGFET).

The ability to successfully fabricate DSGFETs will require understanding of transfer processes and the surface interactions of graphene. Thus, it is necessary to set objectives for this work to provide a foundation for success. The current state of transfer technology should be explored to inform best practices in creating ultraflat, ultraclean graphene. While the best graphene transfer requires appropriate growth processes, graphene growth quality is high enough that transfer improvements can provide more significant results. The adhesion energy of graphene will be explored to different substrates, though it will be necessary to limit the number of materials tested. Thus, only commonly used substrates will be tested. The thermal and electrical response of GFETs are important to consider as well, and how graphene's response changes due to surface interactions. This can be investigated by the exploration of the change in graphene's resistivity as a result of temperature changes across different substrates. As before, the number of materials tested will need to be limited. Additionally, we will not be considering other thermoelectric properties of graphene, such as thermal conductivity. The information gathered from these investigations will then be used to inform the design and fabrication of DSGFETs. This process serves as a proof of concept and will not integrate extensive circuit designs or large-scale techniques.

These objectives will provide the contributions necessary to advance graphene device applications. The refinement of graphene transfer techniques offers increased quality of graphene, which includes less defects and undoped graphene. This creates more reliable GFETs with better performance. The study of adhesion factors can improve device reliability and reduce delamination of graphene during processing. The study of the graphene's resistivity response to temperature and surface interactions can elucidate how the choice of substrate material is important in determining GFET performance. The successful completion of a dual-sided graphene device will open up new possibilities in device architecture, potentially leading to new compact and versatile devices. These devices can offer improved integration with CMOS technology and higher transistor densities than previously possible.

This work will demonstrate investigations into graphene electronics, beginning with a discussion on the state of graphene transfer technology in Chapter 2.0. Adhesion studies of graphene on different substrates will follow in Chapter 3.0. The adhesion interactions between graphene and various gate dielectrics and metal electrodes are investigated using the intercalation of nanoparticles method. Chapter 4.0 evaluates the effects of the substrate and other surface modifications on both single-layer graphene (SLG) and multilayer graphene (MLG) temperature coefficient of resistance (TCR) to advance the understanding of how external influences affect the electrical and thermal properties of graphene, which leads to the final part of this research. The final research avenue displayed in Chapter 5.0 was the development of dual-sided graphene Field Effect Transistors (GFETs). The dual sided GFET is a new platform for advanced applications, allowing for more compact and powerful devices to be made. We show a working prototype and explore how improvements can be made. Future work is then discussed in Chapter 6.0, followed by the Conclusion in Chapter 7.0.

2.0 Graphene Transfer Implementations

The work presented in this chapter was published in [16]. Reused in part with permission.

The graphene transfer process is crucial in determining the quality of resulting devices. Graphene has been used in many applications due to its excellent properties. These graphene-based devices have shown an exciting potential to transform many industries. Despite these possibilities, graphene has not consistently yielded devices with the full characteristics of pristine graphene. As a 2D material, graphene is easily changed by the processes used to fabricate devices. For graphene to provide its most significant benefits, high-quality, ultraclean preparation processes must be created. Depositing or growing graphene on desirable substrates is challenging, thus necessitating a transfer method. The growth method used may affect the quality of later transfer processes. Three of the most common methods to grow graphene are 1) SiC-based growth, 2) highly ordered pyrolytic graphite (HOPG), and 3) transition metal CVD-based growth. Each growth method can be followed by diverse transfer methods. Here, they are divided into wet transfer, dry transfer, and other methods. These processes will be discussed in detail later.

The synthesis of graphene usually takes one of three primary methods: 1) SiC-based growth [17, 18]; 2) highly ordered pyrolytic graphite (HOPG) delamination [19, 20]; and 3) transition metal CVD-based growth [21, 22]. Graphene growth on SiC is typically costly, allowing only limited use cases. Graphene created via HOPG tends to provide graphene with remarkable quality, with limited defects and nearly nonexistent doping due to the ability to use solvent-free processes. However, HOPG is similarly costly and has a low yield. With a low cost and a high scaling capability, CVD graphene is a facile method widely used and can provide high-quality samples.

With a CVD growth process, single-layer or multilayer graphene can be produced. One drawback of this method is that growing graphene directly on the desired substrates is onerous, requiring thin transition metal foils. Since copper has low carbon solubility, it is often chosen as the growth substrate. The low solubility allows for a self-limiting process that can provide repeatable, high-quality, and layer-controlled growth [23]. Figure 1 exhibits different examples of the process and the associated outcome. Copper foil that has already gone through the growth process is shown in Figure 1a, while Figure 1b shows the growth of graphene as viewed with SEM. Typical CVD processes include an annealing and polishing that increases the grain size of the copper, thereby increasing the grain size of the graphene grown on top. The defect sites on the copper surface can be controlled, providing further avenues for increased control. These characteristics have enabled CVD growth to become the primary method of growing graphene. However, using transition metal foils is challenging for the semiconductor industry as conductive metals are unsuitable substrates for most applications. The lack of suitable growth substrates has led to the development and advancement of techniques that can transfer as-grown graphene to the desired substrate.

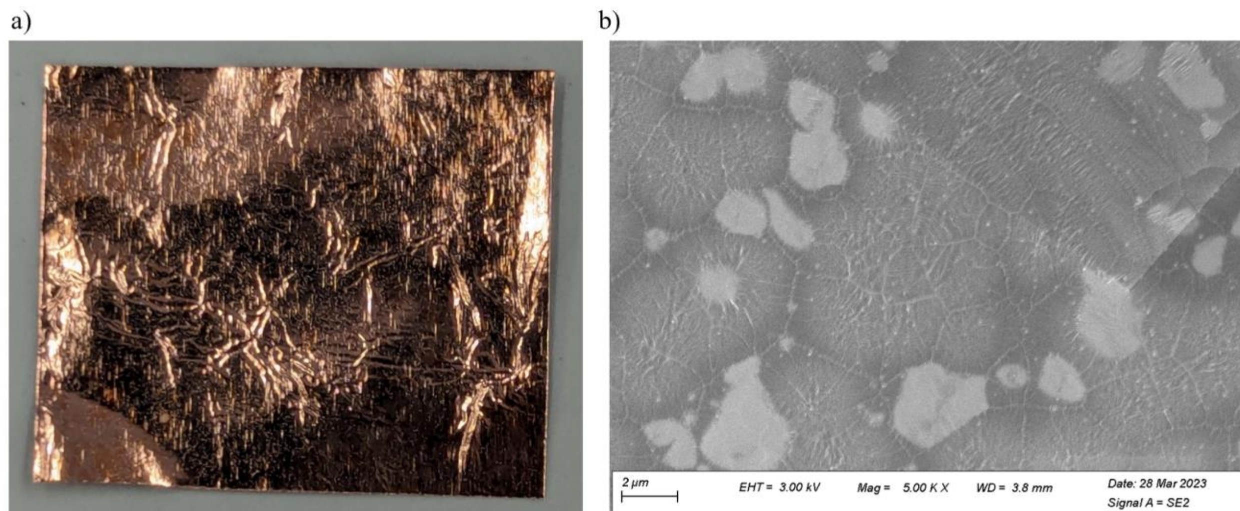

Figure 1. a) Optical image of graphene grown on copper foil; b) SEM image of graphene grown on copper foil

Transfer methods have been developed by the necessity of growing graphene on undesirable substrates and then placing it onto suitable substrates. Graphene transfer from the undesirable growth substrate must fulfill at least two conditions: 1) an intact and complete separation of graphene from the growth material and 2) subsequent intact placement of graphene onto the desired substrate. Many methods have been investigated that fulfill these conditions, with a typical condition being the successful application and removal of an intermediate supporting layer. While previous reviews have detailed many advances, graphene transfer is a subject of intense research, with many new advances being brought to the fore. The pace of experimentation requires a continual update to the state of the art. This chapter focuses on three distinct groups: wet transfer, dry transfer, and other transfer. Wet transfer seeks to use liquid etchants and solvents to separate graphene from its growth material before application onto the target substrate in a liquid environment. Dry transfer removes graphene from the growth material through multiple methods, though the target substrate will receive graphene in an environment without any liquid. Any intermediate supporting layer is typically removed via solvent upon successful lamination. Other methods may use parts of these processes but do not neatly fall into either category. Of the three methods, all are viable paths to a successful transfer. However, due to graphene's high specific surface area, the environment notably affects the resulting properties [24, 25]. If not adequately accounted for, the transfer process may suffer various ill effects. These effects must be considered in any transfer process to deliver ultrahigh-quality graphene.

Transfer processes for graphene can suffer from various issues. These issues can include wrinkles, cracks, and contamination. Wrinkles occur when the graphene sheet overlaps or bunches like a poorly flattened rug. Wrinkles may occur due to differences in topology between the growth

substrate and the target substrate [26], or because the environment causes gaps between graphene and the substrate [27]. The wrinkles cause a deleterious effect on the electrical properties of graphene by creating potential barriers and additional scattering centers [28]. The slender thickness of graphene makes it vulnerable to physical damage and is known as cracking [29]. These physical deformations will also cause undesirable decreases in conduction and poor thermal transfer. Finally, contamination can be caused by the inadequate separation of the growth material or the intermediate support layer [4, 30]. Additional sources of contamination come from the environment, which can cause unwanted doping. Graphene quality and performance are degraded because of these issues, which affect subsequent device performance. Each method achieves different results in its handling of these issues. The etchants and solvents incorporated into the wet transfer process can reduce the level of contamination but may introduce other defects [31]. Dry transfer steps can cause physical damage, and some intermediate support layers can also leave contamination when removed [32, 33]. Various characterization methods have been used to appraise the resulting material properties and defects.

The determination of the quality of graphene may be accomplished through various techniques. SEM imaging, Raman spectroscopy, AFM, and graphene FETs are some accepted instruments used for characterization. SEM imaging may differentiate between single and multilayer graphene samples and determine whether the grain size is monocrystalline or polycrystalline. It can also spot cracks and wrinkles in the graphene structure and potential contaminants [34, 35]. Raman spectroscopy is another method that can determine the number of layers and is also capable of sensing mechanical deformations, strain, and doping [36, 37]. A typical Raman spectrum of graphene will include two peaks, the G peak at ~1580 cm^{-1} and the 2D peak at ~2690cm^{-1}. The ratio of I_{2D}/I_G indicates single layer graphene (SLG) or multilayer

graphene (MLG). A third peak that may show in spectrographic results is the D peak at ~1350cm^{-1}. This peak indicates the existence of mechanical defects in the graphene layer. Note that the position of the D and 2D peaks cited here assume a laser excitation wavelength of 532 nm [38]. AFM can also determine the layers of graphene and spot cracks and wrinkles thanks to its sub-nanometer resolution. The acquisition of the graphene's surface roughness, uniformity, and morphology can determine additional details of its surface quality. More specialized modes of AFM can allow for the gathering of localized material properties, allowing for in-depth analysis of the factors that can influence graphene properties [39, 40]. The creation of GFETs allows for probes into the structure of graphene. The location of the smallest current value for a given drain voltage as a gate voltage is swept is known as the Dirac point. The location of the Dirac point relative to 0 V indicates the doping level present. Additional characteristics, such as mobility and carrier concentration, can be found through this method as well.

The rest of this chapter will focus on graphene transfer and the many methods offered. The wet transfer method is considered in 2.1, the dry transfer method in 2.2, and other transfer methods in 2.3. The overall approach to each method will be discussed, along with benefits, limitations, and possible issues. Section 2.4 will discuss potential avenues of success that may improve graphene transfer quality.

2.1 Wet Transfer Methods

Here, wet transfer is defined as any method in which graphene lies on top of a liquid before being adhered to the target substrate and then dried. Further, only supported transfer processes will be considered here, where a supporting polymer is added to mechanically stabilize the transferred

graphene. As one might expect, the transfer environment is dominated by liquid. Despite graphene's impressive mechanical strength, its thin structure causes it to be a fragile material [41]. The forces involved in a liquid environment can thus damage graphene, requiring a support layer. The removal of graphene from its growth substrate is typically accomplished via an etchant. Figure 2 shows a synopsis of the process. A support layer is deposited after the growth process is complete, as seen in Figure 2a. As stated, the lack of thickness causes graphene to often break without this addition. One common supporting material is PMMA, which can be spin-coated onto the as-grown graphene. As mentioned, this metal is typically copper because of its low carbon solubility and relatively low cost [42]. The combination is then lowered into a suitable etching solution, as Figure 2b shows. Once the metal is etched, the graphene/polymer layer is left floating on top, the graphene side down. The graphene/polymer can then be lifted by another material for additional cleaning, normally by flotation in DI water, as in Figure 2c. After the additional cleaning, the graphene is scooped up by the desired substrate and dehydrated, as in Figure 2d. After drying, the removal of the supporting polymer follows, as in Figure 2e, and another drying round leads us to the finished product in Figure 2f. While this method is simple, each step can cause unwanted contamination and deformation if process control is not maintained. This section will cover further specifics of the wet transfer method and recently introduced technological advancements, as listed in Table 1.

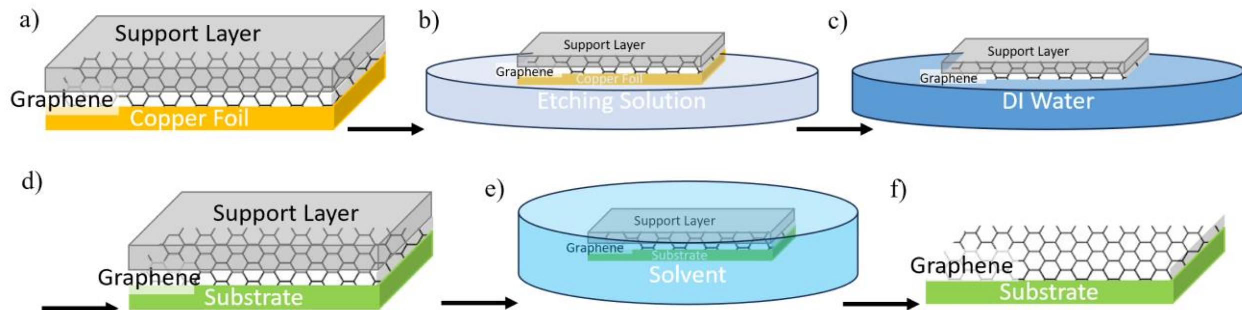

Figure 2. a) Support layer is applied to as grown graphene; b) the combination is lowered into an etching solution to remove the copper foil; c) the remaining support layer and graphene is cleaned via DI water baths; d) the target substrate is used to scoop up the graphene/support layer; e) the support layer is removed by immersion in solution; f) the graphene on substrate is dried and ready for further processing

Table 1. Recent wet transfer method materials

Support Layer	Growth Removal	Support Removal	Ref
PMMA	$FeCl_3$ + HCl	Acetone	[43]
PMMA (different MWs)	$FeCl_3$ + HCl	Acetone/IPA	[44]
PMMA	$FeCl_3$	No removal of PMMA	[45]
PMMA	APS	Acetone	[46]
PMMA	APS	2nd PMMA layer + acetic acid, chloroform, or hot acetone	[47]
Rosin	$FeCl_3$	Acetone/Banana Oil	[48]
Anthracene	APS	Sublimation	[49]
Camphor	APS	Sublimation	[50]
Naphthalene	H_2O_2 + HCl	Sublimation + optional ethanol	[51]
TFB/PMMA	Electrochemical Bubbling	Acetone	[52]

Deformation and contamination problems may occur during the wet transfer process. The problems occur due to the use of liquid etchants and PMMA as its preferred support layer. The etching process may not result in complete removal of the growth substrate, and its particulates are still in solution and may attach themselves to the graphene/polymer stack (Figure 2b and c). The transfer process may also cause the liquid to be stuck between the substrate and graphene, causing the formation of wrinkles as the graphene dries (Figure 2d) [53, 54]. Meanwhile, PMMA-based support layers can bind tightly to graphene thanks to PMMA's functional groups. The strong bonds make PMMA challenging to remove and are a source of p-type doping (Figure 2e and f) [55, 56]. It is not typically practical to remove the support layer, causing the exploration of other materials to be used as a support layer.

Another method attempted is the exploration of different etchants, which may decrease the contamination of metal particles on graphene. These etchants aim to create water-soluble salts that may be eliminated via subsequent DI water-cleaning steps. Initial studies utilized iron chloride ($FeCl_3$) as an etchant. This process left substantial metallic contamination upon completion [47]. A way to improve this situation was to introduce a weak HCl solution, which lowered the remaining metal contaminates [57]. The addition of HCl by Liao et al. was met with success. The added process step removed the excess iron contamination caused by etching copper with $FeCl_3$ [44]. This addition increased the process steps required, which increases the processing time required and may result in mechanical damage. This concern has been removed by other etchants that provide equal or superior results.

Ammonium persulfate (APS) is another etchant that has been examined. This method is used throughout this dissertation due to the inability of FeCl3 to remove metallic contamination

adequately [58, 59]. Other studies have shown that APS is a superior etchant to FeCl3, with much reduced metallic contamination [30]. A comparison of the processes in Ref [43] and Ref [46] shows that the APS process has fewer and smaller residues despite similar cleaning steps. While APS can reduce metallic contamination to an insignificant level, some studies demonstrated that APS may cause increased crosslinking in PMMA polymers, making PMMA more problematic to remove [49]. Additionally, the concentration of APS may cause graphene to crack upon being transferred. The unwanted cracking can be prevented through a lower concentration of APS. The tradeoff comes as a longer etch time [47]. While polymeric residues will occur regardless of etchant, etchants have a role to play in the removal of polymer support layers and thus may necessarily require investigation.

A major problem with wet transfer techniques is polymer residue. Despite its impressive strength-to-size ratio, graphene is easily damaged during the transfer. Thus, the exploration for better support processes has been ongoing for a long time. Improvements to the cleaning process is one method advanced for the reduction of polymer residue. An improved cleaning process can be observed by incorporating the support layer as part of the device and using the properties of the support layer to modulate certain aspects of graphene. Keeping the support layer removes the issue of polymer residue, as the polymer is now a device component. Depending on the application, this may be a preferred method. The polymer may increase the ability to sense certain compounds while restricting the ability to sense others. For example, it is possible to use PMMA to boost the detection and specificity of volatile organic compounds (VOCs) of graphene-based gas sensors. Rattanabut et al. recorded the detection of VOCs using graphene/PMMA and graphene layers [45]. The difference in sensing mechanisms between a PMMA/graphene sensor and a pure graphene sensor enabled different sensitivities and results. The PMMA layer being left on the graphene thus

increased the utility of the graphene sensor. Though PMMA was helpful in this instance, further research is required to determine if support layers can be developed for other applications. The research is required because PMMA is not a universally helpful material. Regardless, this method may be a valuable approach to device fabrication [45]. This approach is unlikely to be universal due to the excellence provided by pristine graphene. However, this approach is suitable for use in various applications and avoids contamination.

Since a change in the support layers cannot meet the needs of all applications, better cleaning solutions are still needed. Many approaches have been attempted, such as annealing in various environments [60, 61], using ion beam treatments [62, 63], plasma treatments [64, 65], or laser exposure [66, 67]. These avenues have the unfortunate drawback of making total removal harder or damaging the transferred graphene [44]. Practical alternatives to these methods are chemical solvents. These chemical solvents can safeguard the mechanical stability of graphene, and thus, this review will explore the different solvents that have been reported and their effectiveness. Park et al. [47] studied the ability of acetone, chloroform, and acetic acid to remove PMMA. Chloroform and acetic acid were used at 25 °C, while acetone was heated to 80 °C. Each chemical performed differently as contrasted to usual acetone-based techniques. AFM images showed that acetic acid resulted in the lowest average surface roughness, achieving a 0.76 nm value. This value was close to the initially recorded value for the substrate before the transfer. In addition, the Dirac voltage of the fabricated GFET moved toward 0V, indicating that the graphene was much cleaner than before. It was accompanied by a gain in electron and hole mobilities. An attempt at annealing was also made, with a 300 °C process showing improvements while a 500 °C process showed detrimental effects. A further benefit of the annealing process was the flattening of graphene on the target substrate. Though higher temperatures work better, the degradation of

graphene at higher temperatures causes a tradeoff between flatness and device performance [47]. This study showed a well-constructed, clean, and flat transfer setup, though enhancements can still be introduced to a thorough transfer process.

Another path toward improved transfer is to investigate how the transfer polymer is manufactured and used. An examination of how the molecular weight (MW) of PMMA affects the remaining residue was conducted by Liao et al. [44]. A simple acetone bath was used to determine how easily the various commercial forms of PMMA could be removed. Lower MW PMMA was found to leave less residue. However, when PMMA of too low a MW was used, it amplified the potential for physical damage due to the diminished mechanical stability of the PMMA. With this data, an improved solution of PMMA was developed that had a low MW and adequate mechanical strength. The solution was made through the mixture of PMMA-15 k and PMMA-550 k in anisole at a 2:1 ratio at 3 wt%. The resulting Raman studies showed a redshift, indicating a reduction of PMMA residues. Low surface roughness and a drop in the quantity of residual particles were recorded with AFM. Specifically, the count of 2.5 um or larger particles in a 650 x 500 um^2 area showed a reduction to <10 particles from a value of ~190 when high MW PMMA was used. The reduction in residue supports the idea that care in the support layer material choice can result in reduced residues [44]. An appropriate chemical solvent and a low MW PMMA support layer can provide ultraclean transfer, though it remains to be seen if such combinations suffice. More improvements can be made, though more thorough cleaning processes may increase the complexity of the wet transfer process. While the additional complexity may achieve the desired ultraclean transfer, simpler processes may achieve such results using a different support layer.

A change in the support layer material provides another approach to reducing residues. PMMA is a strong candidate for transfer due to its low viscosity, high solubility in various organic

solvents, and its nontoxic nature. However, it firmly adheres to graphene and thus necessitates a more involved cleaning approach [47, 48]. Therefore, one method for reducing residues is to find different materials that can serve a similar purpose but are easy to remove. An investigation has been conducted into rosin, camphor, naphthalene, and anthracene [48-51]. The materials listed each provide clean and facile transfer while being simple to remove. Rosin is removed via solvent, while camphor, naphthalene, and anthracene can sublimate at comparatively mild temperatures.

Rosin is a support layer chosen by Zhang et al. [48] for its high solubility in organic solvents, weak adhesion to graphene, and sufficient mechanical strength. Rosin with a MW of 302 was dissolved in ethyl lactate before spin-coating onto a metallic substrate with grown graphene. The metallic substrate was etched with $FeCl_3$. The removal of rosin was achieved using acetone and banana oil. Banana oil was used to ensure the removal of rosin components that were not readily removed via acetone. A surface roughness of 0.66 nm after rosin-based transfer was achieved. Further optical and High-Resolution Transmission Electron Microscopy (HRTEM) images showed remarkably clean graphene surfaces. HRTEM images did show infrequent minute residues, though such results were vastly exceeded the standard PMMA process. The cleanliness was further proved with X-ray photoelectron spectroscopy (XPS), Raman, and GFET studies [48]. The rosin process was used to create organic light-emitting diodes (OLEDs) on a flexible substrate and showed better results than a comparable PMMA or Indium Tin Oxide (ITO) process. Further improvements to the rosin-based transfer process may be possible by using different MW rosin, chemical solvents, or further annealing.

Research into the use of camphor as a support layer was conducted by Wang et al. [50]. The deposition of camphor was done by heating the powder form at 160 °C. The heated camphor was vaporized at this temperature and allowed to deposit on graphene-oxide until it achieved a

thickness of 500 um. The underlying copper growth substrate was removed via APS. After the graphene oxide was transferred, the camphor could be easily removed via sublimation at 60 °C for 24 hours. The sublimation could proceed at room temperature if left for 48 hours. While an etching process was still required to remove the copper layer, the graphene oxide was subjected to reduced stress compared to solvent-based methods. Raman studies performed before and after the removal of camphor indicated complete success, with AFM imaging unable to find traces of camphor residue and providing confirmation. The camphor-based process was replicated for graphene grown on copper. This camphor-based process achieved transfer onto an ultrathin (~100 nm) layer of polycarbonate (PC). The transfer onto an ultrathin layer is a substantial improvement in comparison to the transfer onto 1 um PC thickness that can be achieved without using camphor. Of particular interest is the failure to transfer graphene onto SiO2. However, camphor can be removed effectively, as shown [50]. Materials that can sublimate after transfer are thus still materials worthy of consideration for ultraclean transfer processes.

Another material under consideration is naphthalene. It can also sublimate and was chosen due to the lack of charge transfer to graphene and its low MW. Chen et al. melted naphthalene crystals at 100 °C and drop-cast the solution onto as-grown graphene [51]. A glass slide covered with Kapton tape was then used to press and spread the solution. The glass slide method was favored over spin coating as it did not require a solvent. The growth substrate was removed, and the graphene/Naphthalene combination was transferred. The cleaning process used a vacuum oven at 60 °C for 1 hour, though the process may proceed in air. An optional ethanol step can also reduce or eliminate any remaining residues. Images taken via AFM and SEM displayed minor residues; subsequent Raman spectroscopy corroborated the observations. The fabricated GFET displayed a mobility of 700 cm^2 V^{-1} s^{-1} and little to no doping effect. The satisfactory mobility shows that

naphthalene is a clean process with few drawbacks. As with other materials that can be sublimated, naphthalene can function for transfer onto a flexible substrate. No solvent is required, and it has sufficient mechanical strength to endure the etching and transfer process [51]. This process provides an additional example supporting the use of polymers that can be sublimated for use in the graphene transfer process.

The last material to be discussed is anthracene, which can also be sublimated with elevated process requirements compared to naphthalene and camphor. A study by Yulaev et al. [49] used thermal evaporation in a vacuum oven at -20 °C to deposit the polymer. The copper substrate was removed via APS, and the anthracene was removed by heating it at 120 °C for 40 minutes. SEM and Raman spectroscopy studies confirmed a clean transfer compared to standard PMMA processes. The study determined that an extra process using activated carbon was necessary for ultraclean graphene surfaces. The activated carbon process mandated a Pt thin film deposition onto the target substrate to provide a catalytic effect [49]. The proposed process is effective, though it requires utilization of dedicated equipment. In addition, the practical application of activated carbon may be limited.

The appeal of alternative polymer materials for facile and ultraclean transfer is high. However, these processes could be better investigated and utilized. Each method provides a simple preparation and more straightforward removal, except for anthracene, which requires a low-temperature vacuum oven. A comparison of the SEM images taken for each material will all show remarkably clean substrates. While a direct comparison is unavailable, all studies confirmed little to no left-over contaminants compared to PMMA.

The use of intermediate layers is another avenue for reduced contamination. The intermediate layer can be used to reduce the adhesion of graphene to the support structure, enabling

a cleaner removal process. A conductive polymer known as TFB (poly(9,9-di-n-octylfluorene-alt-(1,4-phenylene-(4-secbutylphenyl)imino)-1,4-phenylene), which was doped with tetrafluorotetracyano-quinodimethane, was shown to adhere to graphene in a work by Liu et al. [52]. This intermediate layer of TFB allowed for a near total removal of PMMA via acetone and was not removed itself. The process culminated in high-quality OLED devices. The researchers showed proof of cleanliness via Raman spectroscopy [52]. Though success was achieved in this instance, further exploration is required to determine if intermediate layers can be used in other applications. One potential drawback is that shaping the material into a device configuration may require etching both the underlying graphene and the intermediate layer that persists post-cleaning. An intermediate layer that can be removed via cleaning may provide more utility. However, this may introduce unwanted complexity and other challenges that must be addressed. Regardless of these challenges, an intermediate layer may be a convenient approach to creating graphene-based devices.

This chapter has shown that the wet transfer process is well-examined, with various advances made thus far. Research continues to provide additional options with varying degrees of success. Changes in the etchants have allowed for more complete metallic substrate removal. Polymer residues have been reduced through changes in solvent, the MW of PMMA, and the use of different polymers altogether. These improvements frequently increase process complexity or time or still need to achieve optimal results. These drawbacks have led to ongoing research efforts to provide wet transfer process improvements.

2.2 Dry Transfer Methods

The definition of a dry transfer method used herein is any method in which the graphene is transferred in a dry environment. The transfer step to the target substrate is how the difference between the dry and wet transfer methods may be illuminated. The use of liquids in the wet transfer method, while no liquids participate in the dry transfer method. The dry transfer method allows no possibility of trapping liquid between graphene and the target substrate. Removing liquid from the process can help reduce the rate of wrinkle formation and the risk of unwanted doping [68, 69]. With this definition, liquids may prepare the target or growth substrate for any subsequent transfer process. Liquids may be used for any requisite cleaning steps. Figure 3shows two general approaches to dry transfer. An indirect approach is shown in Figure 3a. The indirect method starts similarly to a standard wet transfer process. Graphene grown on copper is coated with a support layer. The copper is removed via peeling or chemical etching. Subsequently, the graphene/support layer is laminated onto the target substrate without any liquid involved in the process. The support layer may be removed via peeling, chemical etchant, or solvent. Alternatively, as shown in Figure 3b, the graphene on copper can be directly applied to the target substrate. The copper can then be peeled or etched away. A list of recent studies that used a dry transfer method is shown in Table 2.

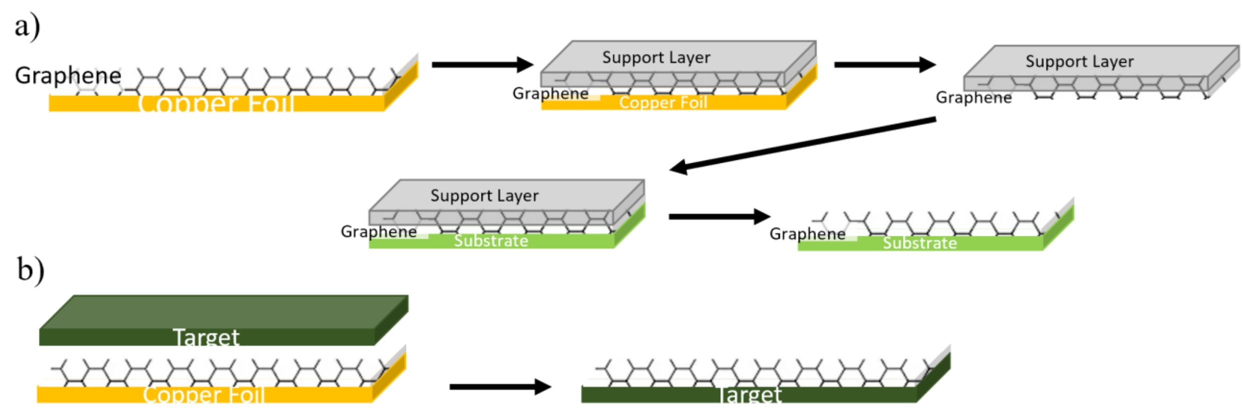

Figure 3. a) indirect dry transfer process; b) direct dry transfer process

Table 2. Dry transfer method papers with a brief description

Grouping	Description	Ref
Mechanical / TRT	Oxidize the copper growth substrate. TRT is used to delaminate and relaminate on a target substrate	[37]
Mechanical / Al_2O_3	Deposit Al_2O_3 on as-grown graphene. Oxidize copper in DI water bath. Use a PVA support layer for delamination and remove PVA after transfer	[70]
Mechanical / Thermal	Deposit ultrahigh MW PE film onto as-grown graphene. Improve adhesion via heat and then peel copper	[71]
Mechanical / Thermal	Spin coat PEI-GA onto the growth substrate. Graphene/copper lamination occurs via a rolling process. Apply heat and pressure to improve adhesion. Peel copper via machine	[72]
Hot Press / R2R	Prepare glass or PET with APTMS+PI. Hot press or R2R onto the target substrate from the growth substrate	[73]
R2R	Hot roll PET/EVA film onto the growth substrate. Peel copper via another set of rollers	[74]

A recent study into the dry transfer process was done by Kim et al. [37]. The direct removal of graphene from the copper growth substrate is difficult due to its high adhesion. The high adhesion causes such attempts to be prone to damaging the graphene. One method to reduce this adhesion is to oxidize the copper surface, which makes delamination of the graphene less prone to damage. Other researchers have employed this method [75, 76]. These earlier attempts suffered from the use of polymers [75], chemical etchants [76], or limited target substrates [77]. In

addressing these drawbacks, Kim et al. explored the use thermal release tape (TRT) as the support layer. TRT was chosen because it was readily removed by the application of heat. After growing graphene on copper, the copper growth substrate was situated in a hot water bath (90-95 °C) for 5 hours. The heated water bath oxidized the copper and reduced the adhesion of graphene to its surface. The substrate was taken out of the water bath and dried after the time elapsed. Then, care was taken to laminate the TRT overtop to avoid creating air bubbles. The copper and the TRT were then delaminated, releasing the graphene from the copper surface. The graphene/TRT was then transferred directly to a target substrate. The TRT was heated at 180 °C for less than a minute, which allowed a gentle lift-off to be performed. The copper foil was lightly etched to remove the copper oxide and could then be recycled for further graphene growth and transfer [37]. While the foil cannot be infinitely reused due to the thinning of the foil after the removal of copper oxide, the ability to reuse the foil helps to lower the cost of graphene growth. This dry transfer process successfully yielded graphene that was then characterized.

The graphene transferred via TRT yields desirable characteristics upon characterization. The process significantly reduced the damage to graphene, as revealed by Raman spectroscopy. The compressive strain that usually accompanies graphene growth, which results from the thermal expansion mismatch, was eased by the formation of copper oxide. The study also determined that the adhesion from this dry transfer process was superior to a typical wet transfer process. A direct comparison could be made by fabricating a GFET device with the dry transfer method and again with a wet transfer method. The GFET created via dry transfer showed an increased symmetry in the results compared to wet transfer, showing that less residue was left on the device. Additional experiments showed this to be the case and confirmed that such a GFET device had reduced contact resistance, increased on/off ratio, and improved mobilities [37]. Thus, the dry transfer method is a

serious contender for a universal ultraclean transfer process, though additional improvements are required.

An analogous experiment was conducted by Shivayogimath et al. [70] using aluminum oxide instead of TRT. This method reduced the difficulty of depositing an atomic layer deposition (ALD) layer of alumina on transferred graphene. Graphene grown on copper was used as the substrate, with the copper foil underneath supplying increased wettability. A DI water bath at room temperature was then used to oxidize the copper/graphene/Al_2O_3 sample. The temperature was kept low to allow time for the water to seep between the graphene and copper layers to ensure better delamination. After the copper is sufficiently oxidized, the sample is removed from water and dried. It is coated with a layer of polyvinyl alcohol (PVA). The delamination can now occur, allowing the copper foil to regenerate as described earlier. The graphene can then be transferred, and the PVA layer can be removed. This process results in a small D peak being observed in Raman spectroscopy results. The presence of the D peak shows that a small amount of damage arises during the process. Additional studies demonstrated that the graphene was lightly doped, displaying a clean transfer process. It was determined that etching methods were unsuitable for this process as they would remove the Al_2O_3 layer. This layer would need to be of an appropriate thickness, as too thin (<10 nm) would allow it to be too easily removed, and too thick (>30 nm) would cause the Al_2O_3 layer to crack [70]. The researchers have shown that this method makes depositing high-performance gate oxides on graphene possible. They noted that other gate oxides could also be suitable and that heating the water bath may decrease the time to transfer.

Heat is a common aspect of dry transfer processes. While previous studies have used various thermal ranges, Li et al. [71] show a process using a single temperature range to transfer graphene to a flexible substrate directly. An ultra-high MW polyethylene (PE) film was used as

the target and transfer substrate, permitting a direct dry transfer process. Ethanol was introduced to the surface of the as-grown graphene to enable the PE film to be applied. The ethanol enabled the removal of air gaps upon drying and altered the adhesion forces at play. The combination film was annealed at 125-145 °C for 10 minutes, causing the PE film to partly melt and improve contact between the PE film and graphene. Afterward, the copper film could be peeled from the PE/graphene layer. The peeling allowed for the copper layer to be reused and for the graphene to be successfully transferred to the PE substrate [71]. The PE/graphene layer could be applied to a target substrate, and the PE layer could be removed if further transfer is desired. After the transfer process, the fabricated device was characterized to ensure quality.

The characterization of the PE/graphene device showed significant benefits. A lack of wrinkles was observed in imaging, highlighting the ability of this process to transfer graphene in an ultra-flat manner. It was shown that the PE/graphene morphology followed that of the copper growth substrate. SEM images showed the presence of second-layer graphene islands. Together, they highlight the need for high-quality growth processes to make subsequent high-quality transfers worthwhile. Raman spectroscopy showed a large $I2_D/I_G$ ratio and no D-band signal, indicating a high-quality transfer. The researchers attribute the high quality to the improved contact area of the PE film gained from the partial melting. The partial melting increased the conformal mapping of the corrugations present on the copper film, thus ensuring that the PE and graphene layers were tightly matched. The fabricated PE/graphene device was connected to copper electrodes to create a piezoresistive strain sensor. The resulting test showed the highest factor obtained from graphene to date, with a gauge factor of 3100 at a breaking strain of 100.6%. The result is enabled by the transfer process allowing for improved use of graphene's capabilities [71].

Thus, this method provides high-quality, clean, flat graphene on flexible substrates and allows for the reuse of copper foil.

PE film is not the only material that can be used to develop a direct transfer process onto a flexible substrate. Seo et al. [72] investigated the use of adhesive gel to increase bonding to a target substrate before peeling the copper foil from graphene. A polyethylenimine (PEI) and glutaraldehyde (GA) liquid mixture (PEI-GA) was spin-coated onto a target substrate. The as-grown graphene was then laminated onto the PEI-GA/substrate via a rolling process. A high-pressure process at 160 °C was used to improve the bonding of graphene to the PEI-GA. This process also cured the PEI-GA into its gel state. The sample was quenched by blowing N2 gas to improve performance further. The copper was delaminated by a machine process, completing the transfer and allowing for the reuse of the copper film for growth.

Characterization of the fabricated graphene device was undertaken to ensure quality. The results of Raman spectroscopy verified that the graphene was wholly detached from the copper surface. The graphene was also shown to be highly n-doped from the PEI-GA, and little to no damage was observed. Despite the doping, sheet resistance results showed a much lower resistance than a standard wet transfer process. The wrinkling of graphene was also reduced, as the average surface roughness was measured to be ~0.26 nm after transfer. This measurement is compared to the ~2.78 nm surface roughness of graphene on the copper growth substrate. It was determined through further testing that the gel's viscoelastic nature helped flatten the graphene. The proof of minor to no structural damage of graphene was obtained via a vapor test. A pristine graphene sample is impermeable to all gases except for H_2 [78]. A standard wet transfer process does not allow for graphene to showcase this trait due to the holes induced during the transfer process [79, 80]. The test identified an increase of 10x to a previously reported lowest value, highlighting the

defect-free nature of the transfer. This defect-free result was further proved by the graphene layer's ability to protect the underlying PEI-GA layer against solvents [72]. Presuming the n-type doping is desired or of little concern, PEI-GA is an effective polymer for dry transfer. Despite this process's high quality and ultra-flat surface, dopant-free transfer remains.

The application of heat and pressure may be performed with a hot press, as in the preceding study, or using rollers. Marchena et al. [73] performed a study that compared these two processes. They used either a glass or a polyethylene terephthalate (PET) substrate. The glass substrate was prepared with a proprietary polyimide (PI) blend, while 3-aminopropyltrimethoxysilane (APTMS) was added to the PET. The samples were dried in a 40-80 °C oven. The transfer process differed at this stage. The hot press processes were performed at 150 °C under 150-300 psi of pressure for 10 minutes. A silicone rubber sheet was used to attain a homogenous pressure distribution. The rolling process, also known as a roll-to-roll (R2R) process, was performed with heated silicon rollers at a prespecified distance. The temperature was set to 140 °C for either the glass or PET case. The distance was set to 1-2 mm for the glass substrates and 38 um-1 mm for the PET. The discrepancy in temperature between the hot press and R2R method was not a concern as these set points signified optimum operating conditions. The copper was peeled away after lamination through the hot press or R2R process. Though each process was individually optimized, the transfer results were shown to differ. The hot press process showed a diminished dependence on the morphology of the copper substrate, as the mobility was high despite the imprinting of the copper surface onto the PI film. However, the R2R method depended on surface morphology, requiring low surface roughness copper film. The R2R method additionally had heightened mechanical damage due to the associated shear and compressive forces, which could also be reduced with low surface roughness copper film [81, 82]. The PI film in this process resulted in n-

type doping, overriding the effect normally present in a glass or PET substrate. The doping was due to the PI layer being the contact layer of graphene instead of glass or PET. The researchers showed that polyamic acid could create different forms of PI, allowing for a broader range of materials for this process [73]. This research reinforces the idea that the choice of graphene contact surface can strongly influence the properties of graphene. Additionally, the quality of the transferred graphene can be improved by optimizing process parameters, highlighting the need for revised processes.

Achieving large-scale graphene transfer and reusing growth substrates significantly benefit an R2R process. However, the R2R process needs to solve the issue of mechanical damage and the decreased quality that results. A study was undertaken by Hong et al. [74] o optimize the R2R process to achieve higher-quality graphene transfer. The researchers chose to optimize the peeling speed and tension. A PET and ethylene vinyl acetate (EVA) film was compressed onto the as-grown graphene with a roller at 150 °C to determine the best parameters. Results showed that low speed had a high variability in quality while high speed was less variable. Regarding the peeling tension, high tension caused increased variability due to increased mechanical damage at the grain boundaries of graphene. The two parameters also displayed a relationship, with higher speeds requiring higher tension for better results. The best results were attained at a peeling speed of 2 m/min and a peeling force of 10 N. While Hong et al. could not achieve a higher performance due to the lack of available speed, regression analysis indicated that a 1.8 m/min speed at 12 N may provide better results. Experiments on the constructed GFET showed a near-zero doping level and a low Dirac point. The researchers showed consistent results across multiple devices, displaying the ability to reproduce their efforts. In their fabrication process, gold was deposited on top of the graphene instead of underneath, which decreased the gate leakage current. A sheet resistance

measurement displayed an increased resistance from this graphene transfer than wet transfer. However, this is likely due to the difference in Dirac points between the two processes. The R2R process has a Dirac point close to 0V, corresponding to the point of highest resistance and the state of the graphene when undergoing a sheet resistance test. Thus, the graphene can be intentionally doped for lower resistance, as the wet transfer process results in unintentional doping [74]. The increased process control shows that the R2R transfer process has potential for effective, large-scale transfer of graphene.

The inherent adhesion mechanics of graphene to the copper film and the target substrate are a constant theme in examining dry transfer methods. Each technique shown shares the ability to manipulate graphene adhesion to the various substrates. The adhesion characteristics of the dry transfer process need to be well understood so that a mechanical, thermal, or chemical manipulation can be more accurately targeted for success. Thus, the exact mechanisms need to be researched to increase process quality. The improved comprehension will grant accurate targeting of efforts into process optimization for numerous techniques. One potential avenue for research is the use of an intermediate adhesive layer that can be tuned for the application or removed entirely to enable graphene's characteristics to be revealed.

2.3 Other Transfer Methods

This chapter provides insight into current wet and dry transfer processes. This section will review other techniques outside those classifications to provide a more comprehensive view. Each previous section had transfer methods cleanly identified as wet or dry processes. This section will have transfer methods that can be completed wet or dry, with no etching of the growth substrate,

with no support structure required, or without using any transfer method. The oldest graphene transfer method used scotch tape to isolate a few layers of graphite pencil lead, which was used in the first graphene-based transistor [1]. Transfer techniques have made many advancements since then. The reuse of the copper foil has been made possible in a wet transfer mode using electrochemical or non-electrochemical bubbling methods [83, 84]. These methods delaminate the graphene from the copper without using destructive chemicals, thus reducing the metallic contamination issue. Each method has also been employed in a wet or dry environment, showing a wide range of utility. Studies have shown the potential for support-free transfer methods to be used, eliminating the issue of polymer residue [85, 86]. Direct growth processes have also been developed that remove the transfer process entirely [87, 88]. Table 3 shows the studies this section will review.

Table 3. A succinct description of other transfer methods

Method	Description	Ref
Electrochemical Bubble Transfer	A graphene/copper cathode in an electrochemical solution with an anode to delaminate graphene via bubbles	[89]
Stamp Method	Stamp graphene onto a target substrate with PDMS	[90]
Support-free Transfer	A wet transfer process sans a supporting polymer layer	[91]
Direct Growth	Graphene directly grown on a silicon substrate	[92]

The bubbling method can be achieved through electrochemical or non-electrochemical means. In either case, the delamination process is achieved through the bubbles created between graphene and copper in an aqueous environment. An electrochemical bubbling method was performed by Lu et al. [89]. A dual supporting layer system was used. The first layer was a standard

PMMA layer, as in a wet transfer process. The second layer was polystyrene (PS), which was termed a selective soluble polymer (SSP). The electrolyte was chosen to be sodium sulfate (Na2SO4). DC voltage was applied using copper as the cathode and platinum as the anode. Since copper was used as the cathode, it allowed for the delamination of the graphene/PMMA/PS layer by generating bubbles between graphene and copper. The graphene/PMMA/PS layer was placed into a DI bath with a top layer of n-hexane. Cyclohexane was gradually added to the top layer to selectively remove the PS, which helped to remove any wrinkles. The graphene/PMMA layer was then transferred onto the target substrate, and the PMMA was removed via acetone and IPA baths. PS was included to strengthen the supporting layers for use in the electrochemical bath. The study also treated the surface of the SiO2 wafer to be more hydrophilic, which enabled the DI water to be removed in a fashion that reduced wrinkling. The low-intensity D peak obtained from Raman spectroscopy confirmed the lack of mechanical damage from this process [89]. The study highlights how choosing appropriate substrates and preparing the substrate for transfer are important considerations.

The stamp method is a more direct method of transfer. Seo et al. [90] use PDMS as a support layer and a target substrate to study this technique. Epitaxially grown copper on SiO_2 substrate was used to grow graphene, which was removed by a wet transfer analog. In this technique, the tape was placed around the edges of the copper/graphene, allowing a flat or curved PDMS substrate to lift the graphene out of the water. The copper was etched via APS solution. The curved PDMS substrate was used as a target substrate to show the capacity to transfer graphene onto non-flat surfaces. The flat surface was used to transfer graphene to other substrates, which required careful peeling of the PDMS to complete. Raman spectroscopy showed a strong monolayer graphene signal. This process demonstrated the ability to pattern graphene before

transferring it to the target substrate and still create usable electronic devices. Consistent with prior research, the study showed that peeling angle and speed were essential considerations when removing the PDMS. This stamp method allows for a polymer-free transfer or transfer to unusually shaped substrates [90].

The support-free transfer method is a process that usually takes place in an aqueous environment. This method avoids the issue of polymer residue by forsaking the use of a support layer. Despite the inadequate absolute mechanical strength, Zhang et al. [91] showed that a genuinely polymer-free process was possible in what was termed a water-transfer-printing process. The growth substrate can be removed by a chosen etchant, and anti-wrinkle agents can be introduced to the solution. These anti-wrinkle agents can be added by soaking cleanroom wipers (made of a blend of cellulose and polyester). It was found that adding a small amount of the fibers helped to remove wrinkles. A convex surface was formed by placing a quartz or glass frame onto the solution's surface. The copper/graphene was then fixed on top, and n-heptane was gradually added as a liquid protection layer to eliminate the adhesion of residues. The elimination occurs due to heptane not being miscible in water. Once the growth substrate is removed, the target substrate can be lowered on top of the graphene instead of from underneath due to the lack of a support layer. Adhering the target substrate to the topside of the graphene helps to lower the influence of the etching solution on the final characteristics of the transferred graphene. The researchers performed this operation without a glass frame on a 10" section of graphene, showcasing the possibility of large-scale transfer. The convex surface was created by slightly overfilling the container. Results showed that the graphene was mainly transferred damage-free, wrinkle-free, and dopant-free [91]. The success of this experiment shows that polymer-free transfer can be a practical option for ultraclean, ultra-flat transfer of graphene.

Direct growth methods seek to grow graphene directly on target substrates. Direct growth is typically prevented by the need to grow metallic films on the target substrate first, preventing proper direct growth [93, 94]. Processes that do not require metal layers to be grown have surfaced in recent years [95, 96]. Further research is required to provide efficient large-scale graphene growth, as these processes are still in their infancy. Through careful process control, a study by Tai et al. [92] helped to advance the state of direct growth on Si. The study used a process similar to typical atmospheric CVD growth of graphene. The nucleation of small graphene domains (~130-160 nm across) was realized after 1 hour of growth. Higher temperatures achieved faster growth rates, though the silicon surface was destroyed at temperatures more than 950 °C due to hydrocarbon radicals. Other process improvements to quicken growth rates are still possible, facilitating more large-scale graphene growth [92]. While direct growth is a possible avenue of graphene use, commercialization of this process will require further optimizations.

Though the processes in this section are underutilized, they show great potential for the future of graphene transfer techniques. The electrochemical bubbling method allows for the reuse of copper, though issues similar to those of standard wet transfer methods remain. The electrochemical bubbling method also necessitates additional equipment, though the non-chemical method may ease this concern. While the support-free method is new, lessons from previous research can be adapted for better results. The direct growth method allows for the removal of the transfer step entirely. This method would allow for improved integration with current CMOS technologies. Challenges remain for direct growth, including a sizable enhancement in the growth rate of graphene films and the ability to grow large-scale monocrystalline graphene on arbitrary substrates.

2.4 Recommendations

Graphene transfer is an increasingly critical research area. The full potential of graphene can only be achieved by placing graphene on suitable substrates in an ultra-high-quality manner. Several research projects have been undertaken to pursue this goal, many of which could not be reviewed here. The general grouping of wet, dry, and other transfers is still applicable. External factors to transfer are also influential in the final device performance. The goal of ultra-high-quality graphene transfer and the implementation of ultra-high-quality graphene devices still requires further research.

The leading process in the literature is the wet transfer method due to its straightforward implementation. The transfer of centimeters or larger sizes of graphene in a time and cost-effective manner is easily achieved with wet transfer methods. Of the many implementations of the wet transfer method, PMMA is one of the most widely used support materials. PMMA is used despite the drawbacks that have yet to be eliminated. Many attempts have been made to remove these drawbacks, including the use of various kinds of etchants, the removal of the need for an etchant, a change in the support layer material, the removal of the support material, or its inclusion in the final device. In these attempts, some changes reduced the metallic contamination issue, while others helped to remove unintentional doping of graphene or with the intentional doping of graphene. Each method needs to account for the presence of liquid in the wet transfer process, as the liquid can become trapped and disturb graphene's mechanical structure, influencing other properties of graphene. While straightforward, many steps can be optimized for the best possible performance. Thus, large-scale, efficient, and high-quality transfer persists as an undecided issue.

Several advantages are offered using dry transfer methods. The most prominent is that liquid cannot be stuck underneath graphene if there is no liquid, preventing any unwanted doping

or mechanical deformations that affect the properties of graphene. With no liquid being used, the range of materials is expanded to include any material that cannot withstand exposure to water or other liquids. The dry transfer method also shows a greater variety of techniques that can successfully transfer to target substrates. No single dry transfer process has emerged as a favorite. An understanding of adhesion is highly desirable for further developing dry transfer processes. A lack of this understanding can cause a decrease in the quality of the graphene transferred due to structural damage. The substrate interaction dynamics between graphene and its growth and target substrates need to be further understood to facilitate the process of transferring graphene. Some dry transfer methods suffer from the polymer residue problem in wet transfer processes. However, an advantage of the dry transfer method is directly transferring graphene without using etchants or solvents that can dope or damage graphene's structure. This benefit can lead to higher-quality graphene and improved processing ability. As with wet transfer, many steps can be individually optimized for the best performance.

This chapter has also reviewed other transfer processes that only fit partially into a wet or dry transfer process. Each offers a viable alternative for advancement despite their underutilization. The lack of a transfer process can enable direct growth methods to provide the highest quality graphene. Large-scale, efficient graphene growth is still challenging, and thus, transfer methods are still needed in the near future. Bubbling techniques allow for the reuse of the growth substrate, potentially lowering the cost of wet transfer methods. Dry transfer methods can also use the bubbling method, allowing for a blend of wet and dry transfer techniques. Blending these techniques can allow for better results than either can achieve separately. The ability of the printing process to transfer graphene to uniquely shaped surfaces is a considerable advantage that may allow the printing process to proliferate. The polymer residue situation may be resolved

through support-free transfer techniques. However, process refinements are nevertheless essential to enable large-scale transfer due to graphene's inherent mechanical weakness as a 2D material. Despite the low popularity of these techniques, they may provide enhancements to transfer processes that traditional processes cannot provide. The beneficial aspects of these unexplored processes can only be uncovered through further research.

As the direct growth of graphene is currently not widely feasible, transfer processes aim to provide high-quality graphene on target substrates. The quality of the transferred graphene depends on the grown graphene's quality, which is an overlooked issue. Over the years, improvements to the quality of grown graphene have been made, though continued improvements will enable higher-quality graphene to be obtained from transfer processes [97, 98]. In the ideal case, grown graphene would come in a monocrystalline, ultra-flat, and ultraclean format with precisely controlled layer formation. Graphene of this quality would allow for the best possible quality after transfer. Many processes create islands of multilayer graphene on otherwise single-layer graphene or create multilayer graphene in its entirety. It is common to grow polycrystalline graphene sheets, causing an increase in resistance and a decrease in device quality due to the effects of grain boundaries. Different substrates for graphene growth can also be investigated, as they may allow for wet and dry transfer methods to work more efficiently. The difference in surface interactions between graphene and substrates like Ge or SiC may provide benefits that growth on copper cannot provide [99]. Thus, graphene growth processes are integral to the success of any graphene transfer process.

Large-scale, ultraclean, ultra flat, and efficient graphene transfer have yet to be fully realized. While much work has been done to improve the state of graphene transfer, the adhesive and mechanical forces at play demand expanded understanding to achieve maximum quality.

While PMMA has allowed for widely successful transfer processes, other support layers may provide a paradigm shift that enables higher-quality graphene devices. Each research discussed has also focused on individual process steps, with little research showing the results of each improvement together. Holistic studies should be performed to determine the effects of individual optimizations on the overall result. Each process has advantages and disadvantages, requiring consideration of which transfer method will produce the best results for a particular application and proving that a universal transfer method is unavailable. Thus, graphene transfer research should continue to investigate the various ways that graphene transfer can be accomplished. The commercial and scientific prospects of graphene will depend on the increased quality that graphene transfer research can provide. The result of improved transfer processes will quickly be known in subsequent research projects.

3.0 Graphene Adhesion to Silicon and Metal Substrates

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The adhesion of graphene to a substrate affects the extrinsic properties of graphene significantly. Since graphene must normally be transferred from its growth medium to its desired substrate, a strong and clean adhesion between the materials is desired and will result in better performance. Due to its 2D nature, the surface interactions between graphene and the substrate have a tangible effect on graphene's properties. Therefore, the adhesion of graphene to a material is of material interest in the design of any application of graphene.

The strength of the adhesion energy between two materials is determined by the surface forces. With an extremely high surface area to volume ratio, graphene is strongly affected by surface interactions. Such interactions have reportedly caused graphene to have reduced electron mobility on SiO_2 [101], the opening of bandgaps [102], and many other effects. Transfer processes may degrade material performance through polymer contamination [15]. To make the best use of graphene, it is essential to understand how it adheres to substrates so that reliable device fabrication processes can be developed. The van der Waals forces are a major component of the adhesion forces, consisting of the Keesom force, the Debye force, and the London dispersion force [103]. The most prominent of these three is the London dispersion force, which is a result of two instantaneously induced dipoles acting on each other. This force increases in magnitude in two ways: (i) an increase in the atomic radius due to the increased polarizability of larger and more dispersed electron clouds; (ii) more molecular interactions from an increase in the contact surface area. Since graphene is highly conformative, a non-planar surface can significantly increase the

actual surface area and have a noticeable effect on the adhesion energy if not taken into account [101]. Since these factors affect the London dispersion force, they also affect the adhesion energy. Graphene device performance can be increased through an increased understanding of the adhesion mechanics between the material and other substrates. This can be done by understanding the surface forces at play, leading to an increase in the understanding of growth mechanisms, transfer processes, and the material properties themselves, with attention given to how they change due to substrate interactions.

Research of the adhesion energy between graphene and substrates is thus influenced by the London dispersion force. Previous research has been made of these properties to various substrates. A double cantilever test was used to measure the adhesion of grown graphene to copper, which obtained an adhesion energy of 0.72 J m^{-2} [104]. A Density Functional Theory model was used to determine the adsorption energy of graphene to copper, which contained the adhesion and binding energies. The adhesion energy was found to be 2.483 J m^{-2} by subtracting the binding energy from the adsorption energy [105]. Another method used was a nanoscratch test that found the adhesion energy from graphene to copper and nickel, which was 12.8 and 72.7 J m^{-2} respectively [106]. A pressurized blister test with graphene sheets on an SiO_2 substrate recorded an adhesion energy of 0.31 J m^{-2} for few layer graphene [107]. Another test for SiO_2 used the intercalation of nanoparticles method to find an adhesion energy of 0.151 J m^{-2} [108]. This overview shows several works into the adhesion energy of graphene, but more work still needs to be done to fully explore this area.

In this section, the van der Waals interactions between graphene and various gate dielectrics and metal electrodes have been investigated. These substrates are SiO_2, Si_3N_4, Au, and Pt. The intercalation of nanoparticles method, using Au nanoparticles as the supports, was chosen

as the framework. Nanoparticles are dropped onto the surface of the substrate before transfer of graphene, allowing nanoparticles to function as supports. These supports cause a blister to be created in graphene. The blister is an area where graphene does not touch the surface of the substrate and can be easily measured by AFM. The blister height, the blister radius, and the graphene thickness were measured to calculate the adhesion energy. This method was chosen due to its relatively low cost, ease of use, and is not influenced by edge effects [108]. This work helps to fill a gap of understanding in the adhesion characteristics of graphene to various substrates.

3.1 Experimental Methods

The sample creation process began with graphene grown via CVD. This was followed by wet transfer onto a prepared substrate. The substrate was prepared by coating the surface with nanoparticles before graphene transfer. The summary of this process is illustrated by Figure 4.

Graphene growth was achieved using copper foil (0.025mm thick, 99.8% pure on a metals basis, Alfa Aesar) as a growth substrate. The Cu foil was cleaned with acetone and isopropyl alcohol (IPA) and dried via hot plate (Figure 4a). The foil was then placed in a quartz boat and subsequently placed into a CVD oven. The chamber of the oven was purged of the ambient atmosphere by running Ar and H_2 gas. The temperature of the chamber was then raised to 1000 °C over 30 minutes, after which the temperature was maintained for an additional 30 minutes to anneal the Cu foil. Graphene was grown by flowing CH_4 through the chamber for 10 minutes, after which the chamber was allowed to cool to ambient. This process produced few layer graphene, as determined by AFM measurements of the graphene thickness on SiO_2, on top of the copper surface (Figure 4b). After the graphene was grown, it was transferred to various substrates. The process

was followed by spin coating polymethyl methacrylate (PMMA) 495 A2 onto the graphene side of the Cu foil (Figure 4c). The backside of the Cu foil was cleaned by oxygen plasma for 10 seconds. These Cu/graphene/PMMA pieces were cut to size to fit onto the prepared substrates. The underlying substrate was etched by an ammonium persulfate (APS) solution overnight (Figure 4d). The remaining graphene/PMMA pieces were then transferred to DI water three times for 10 minutes to reduce contamination (Figure 4e). Afterwards, the graphene was transferred onto the substrate and left to dry in ambient conditions overnight. Finally, the PMMA was removed by soaking the pieces in acetone for 30 minutes, followed by IPA for 5 minutes, and then left to dry in ambient.

The substrates were prepared in parallel to the graphene growth process. Samples were prepared on SiO_2 and Si_3N_4 wafers. The SiO_2 wafers were grown using thermal wet oxidation while the Si_3N_4 wafers were grown using a low stress LPCVD method. The thickness of the SiO_2 layer was 100 nm while the thickness of the nitride layer was 1 um. The wafers were cut into rectangular pieces measuring a few centimeters a side. The pieces were cleaned via acetone and IPA and dried via hot plate. An electron-beam (e-beam) evaporator was used to create the Au and Pt layers. The Au layers were 30 nm thick, while the Pt layers were 11 nm thick (Figure 4f). After the substrates were prepared, a nanoparticle solution was prepared. The solution had Au nanoparticles with 50 nm nominal diameters, supplied in a sodium citrate solution (Alfa Aesar). This solution was then diluted at a ratio of 9:2 DI:nanoparticle in a separate beaker to reduce clustering of nanoparticles, though such clustering was unavoidable. The diluted solution was dropped onto the prepared substrate and left to dry overnight in ambient conditions (Figure 4g). Once the samples had dried, graphene transfer was performed. This allowed for the 2D layer to lie on top of the nanoparticles (Figure 4h).

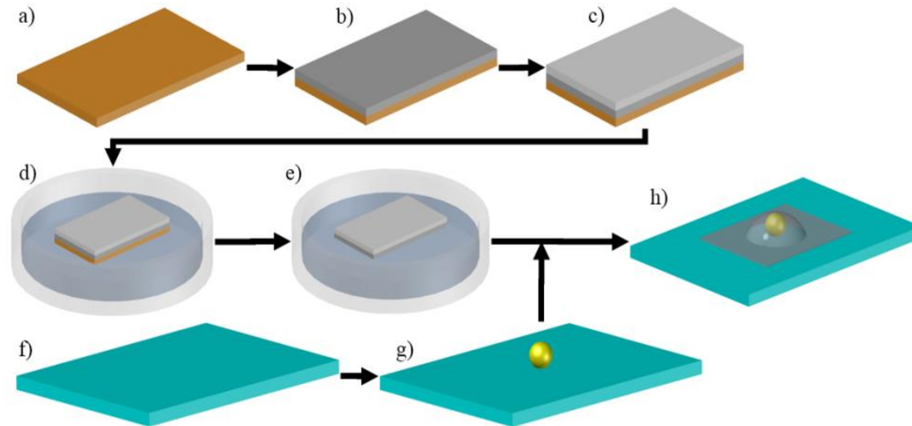

Figure 4. The sample creation process. a) Copper foil is cleaned and annealed. b) Graphene is grown on the Cu foil using a CVD method. c) PMMA is spun on top of the grown graphene and the backside of the Cu foil is cleaned of any excess graphene growth. d) The Cu/graphene/PMMA is put into an etchant bath, Cu side down. e) The Cu is etched away and the remaining graphene/PMMA hybrid is cleaned in DI water baths. f) A substrate is chosen to deposit nanoparticles onto. g) Gold nanoparticles are deposited onto the substrate. h) Graphene is transferred onto the prepared substrate, sandwiching the nanoparticle between the substrate and graphene, resulting in a blister [59].

Samples created by the above process resulted in graphene bound to the substrates by surface forces, such as van der Waals forces, but had nanoparticles acting as supports. This created a blister in the graphene layer. The blister is an area where graphene is not in contact with the substrate. The area of the blister depends on the size of the nanoparticle, with larger nanoparticles causing a larger blister. The size of the resulting blister can then be used to determine the adhesion energy between graphene and the substrate.

The adhesion energy was characterized by using a scanning electron microscope (SEM) (Zeiss Sigma 500VP) and an atomic force microscope (AFM) in tapping mode. The SEM was used to find areas where a single nanoparticle was the support of a circular blister. This blister was measured with AFM. The AFM was also used to find the thickness, and therefore the number of layers, of the 2D material. The AFM scans were made in a 5 um by 5 um area and a 400x400 pixel

resolution using tapping mode. The thickness measurements were made on SiO_2. The adhesion energy could then be extracted by inputting the thickness of the graphene and the radius of the blister into a model.

The blister was modeled by first considering a thin plate with an external load (P) produced by a central shaft of radius (R) as in Wan et al. This leads to the formation of a blister with radius, a (where a >> R), and central deflection $w_0 = \frac{3(1-v^2)Pa^2}{4\pi}$, with υ as the Poisson's ratio of the membrane. Under load, the mechanical energy release rate of the blister can be found. However, this formulation is insufficient for three reasons: (i) the model accounts for only the bending mode, which doesn't account for the dominant stretching mode in thin membranes, (ii) the point contact at the center of the blister has an unphysical stress singularity, (iii) the area near the blister does not account for plastic yielding [109].

To correct these issues, a thin flexible membrane that is under the same loading conditions as a thin plate must be considered. The assumption that a>>R still holds. The authors considered the elastic response by defining the tangential and radial strains and stresses, allowing the researchers to obtain [109]

$$\frac{d}{dr}(\nabla^2 f) + \frac{Eh}{r}\left(\frac{dw}{dr}\right)^2 = 0 \tag{3-1}$$

Where f is the stress function that defines the radial and tangential stresses, E is the Young's modulus, and h is the thickness of the thin plate. If one uses the principle of virtual work, a load function can then be established. Linear elastic fracture mechanics can then be used to establish an energy balance by considering the blister profile. The interfacial energy of the membrane adhered to the substrate (W) under equilibrium conditions becomes [109]

$$W \approx \frac{Eh}{32k_{el}}\left(\frac{w_0}{a}\right)^4 \tag{3-2}$$

where k_{el} is a slowly varying function of a for small debonding angles (<25°). The equation is valid if the yield strength is higher than the effective stress, allowing the blister to remain elastic. The stress approximations are not valid inside the contact circle ($r<a$), though the contact zone contribution is negligible when P is small [109].

Another consideration comes in the form of the nanoparticle that takes the place of the central shaft in the experiment. For small debonding angles, $k_{el} \approx ½$, which allows the equation to be written as [108, 109]

$$\gamma = \lambda Eh\left(\frac{w}{a}\right)^4 \tag{3-3}$$

Where λ is a geometrical factor = 1/16 for a circular blister and comes from $1/(32\ k_{el})$ and w takes the place of w_o. Therefore, Eq. (3-3) is a simplified version of Eq. (3-2). Some other assumptions have been made in the creation process. First, it has been assumed that the 2D layer behaves as a flexible membrane with negligible flexural rigidity because w and a are much greater than h. The substrate and support particle are taken to be rigid with negligible deformation forms the second assumption. The justification for this lies with the fact that 2D layers are ultrathin and so long as the wedge can support the load and does not collapse, the correction to the equation is negligible [108]. The parameters in Eq. (3-3) are shown in Figure 5. Figure 5a shows the diameter of the blister, 2a, in a top-down view, while Figure 5b shows a cross-sectional view. Additionally, Figure 5b shows the height of the 2D material, h, and the height of the blister, w. The gold sphere represents the nanoparticle, while the gray layer is the 2D material, which in this case is graphene.

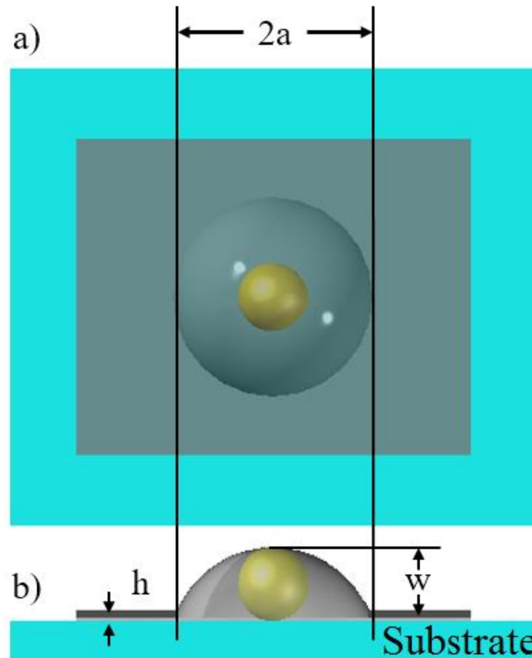

Figure 5. The visualization of the parameters in Eq. (3). h is the thickness of the 2D material, a is the radius of the blister, w is the height of the blister. a) top view, b) cross sectional view [59].

3.2 Results and Discussion

SEM images were captured first to determine how the AFM images may appear. An example image is shown in Figure 6 of graphene on Si_3N_4 with intercalated Au nanoparticles. Regions of single nanoparticles, position A, and multiple nanoparticles, position B, can be seen in the image. Position B is a complex blister that does not fit the underlying assumptions of the mathematical model and thus is not suitable for analysis. Additionally, a region of a single nanoparticle with a wrinkle in the graphene layer can be seen at position C. Since the wrinkle provides extra forces that do not align with the assumptions made, these positions cannot be used for analyses. Thus, only AFM measurements that showed a blister like in position A were used to determine the adhesion energy.

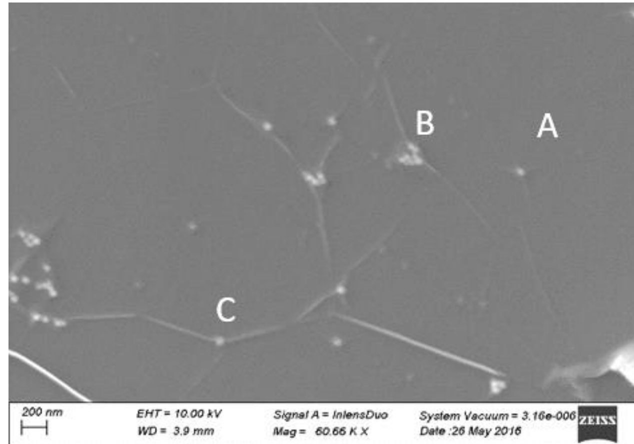

Figure 6. Graphene on Si_3N_4 with Au nanoparticles SEM image with working distance 3.9mm and magnification 60.66kx. The electron beam voltage was 10kV. A regular blister with a single nanoparticle is shown at position A. A complex blister with many nanoparticles is shown at position B. A single nanoparticle blister with a wrinkle in the graphene layer is shown in position C [59].

Tapping mode AFM was performed to obtain the graphene blister profiles. The thickness of graphene was measured to be 3.4 nm, showing that multiple layers of graphene were present. The scanning size was 5x5 um^2 with a resolution of 400x400 pixels. The blister height (w) and the blister diameter (2a) were measured accurately using the AFM software. This was done by taking the contact point between the graphene and the substrate to be the lowest points of the line profile. Graphene AFM images were taken for SiO_2, Si_3N_4, Au, and Pt substrates. Figure 7 shows sample AFM images of graphene on (a) a SiO_2 substrate and (b) a Pt substrate with the line profiles of each shown beneath the AFM image. The lighter regions provide a rough approximation of the height recorded by the AFM. The blisters are taken to be light circular regions, and the line going through them shows the position of the line profile. The height of the blister in Figure 7a was found to be 24 nm while its width was found to be 260 nm. The height and width of Figure 7b was found to be 31 nm and 190 nm, respectively. This led to an adhesion energy of 739.2 mJ m^{-2} for Figure 7a, and an adhesion energy of 2409.41 mJ m^{-2} for Figure 7b.

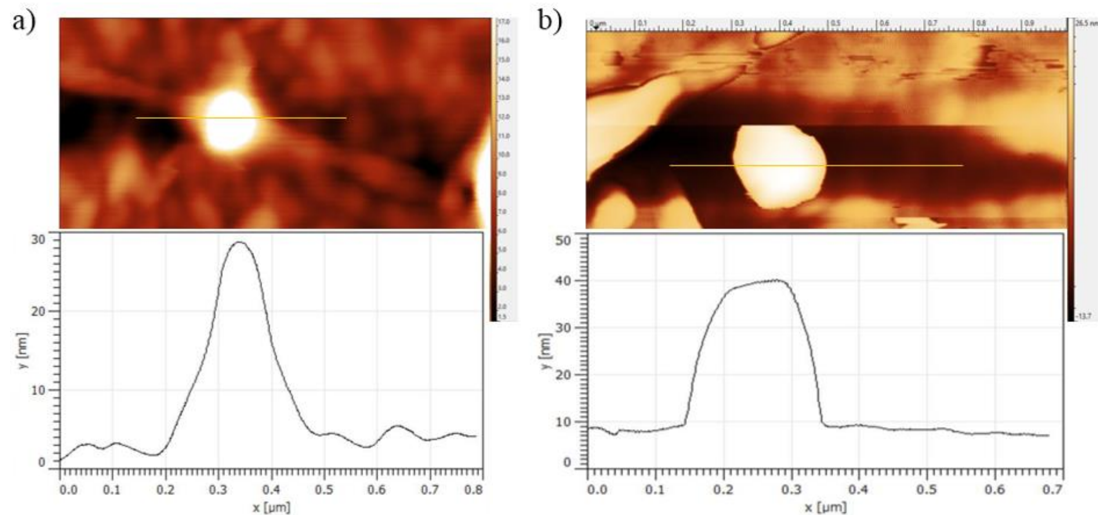

Figure 7. Representative AFM images of graphene covering an Au nanoparticle with a) a SiO_2 substrate, b) a Pt substrate. Taller structures are represented by lighter regions. The line profiles of each blister are also shown. The line profiles have an x-direction unit of um, and a y-direction unit of nm [59].

The AFM images were gathered and analyzed to find the blister heights (w) and blister diameters (2a) for each substrate. The range of these two data points for each substrate are shown in Figure 8. The red boxes on the left for each substrate indicate the blister height and the blue boxes on the right indicate the blister diameter. The min and max values for each box are shown by the extended bars, while the boxes show the middle 50% of the data. As expected, the heights of the data points are uniform due to the use of 50 nm diameter nanoparticles. However, the expected height of 50 nm is not achieved, and the height variation is still larger than expected. Two explanations for this are possible: (i) the 50 nm figure is only the average nanoparticle size and the actual sizes of the nanoparticles vary; (ii) the size of the nanoparticles was impacted due to the transfer process causing a collapse or distortion of the nanoparticles. Since Eq. (**3-3**) does not expect a particular height or diameter, the varied sizes recorded will not affect the resulting measurements. Furthermore, the profile of each measurement was similar, allowing the cases with

small nanoparticles to be considered as good data. This data can then be used to determine on a rough basis which material has stronger adhesion. The adhesion energy is proportional to $(w/a)^4$, which means that substrates that show smaller diameters should have higher adhesion energies. This can be easily seen on the graph, with Au having the smallest diameter and thus can be expected to have the highest adhesion energy. The results show this to be true.

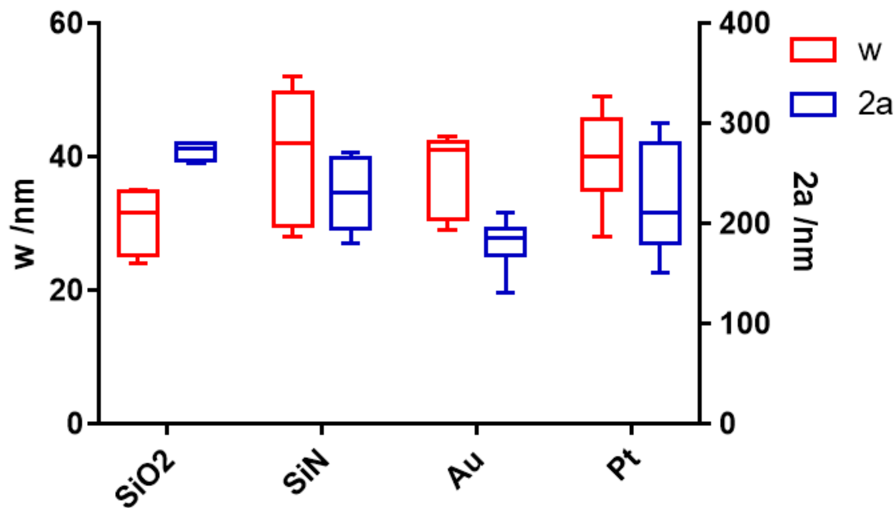

Figure 8. Range of blister data for graphene on various substrates. The red data on the left for each substrate is the blister height, w, while the blue data on the right is the blister diameter, "2a" [59].

The data collated and shown in Figure 8 was put into Eq. (3-3) to determine the average adhesion energy for each substrate. The Young's modulus was reported to be 1 TPa and is the value used for calculation of the adhesion energy [110]. The average adhesion energy results are shown in Table 4. As can be seen, Au shows the strongest adhesion energy. Additionally, the result for SiO_2 aligns well with prior experiments once thickness differences are accounted for [108, 111]. There are a few plausible causes for any differences: (i) a vacuum state was not used; (ii) liquid from the transfer process may remain between the graphene layer and the substrate which

would result in a larger blister radius. However, since the adhesion energy was similar to prior experiments, the process used here can be considered to achieve a sufficient level of dryness.

Table 4. Graphene adhesion energy for recorded substrates

Substrate	Graphene Adhesion Energy [mJ m^{-2}]
SiO_2	567.14
Si_3N_4	3281.64
Au thin film	7687.10
Pt thin film	4021.47

An inspection of Eq. (3-3) shows us that the Young's modulus is an important indicator of adhesion. While adhesion energies can vary due to different van der Waals interactions, materials that interact similarly, and thus create similar blister height to diameter ratios, must then only differ by the Young's modulus and thickness. Thus, if one measures several different thin film materials and finds similar energies after accounting for thickness and the Young's modulus, it can be expected that the materials interact with the same substrate in similar ways. Since 2D materials will typically have similar thicknesses, the Young's modulus of each material will likely have a stronger effect. However, if differences remain in the blister height and diameter ratios even after accounting for the Young's modulus and thickness, then it must be that the materials are interacting with each other in substantively separate ways. Since graphene has an intrinsic Young's modulus and the thickness of each sample was the same, the remaining difference must be in how graphene interacts with each substrate.

The specific forces acting on graphene are not explicitly expressed by Eq. (**3-3**) and thus it must be determined why graphene interacts with each material differently. An explanation can be pursued by noting that Au has the strongest adhesion energy to graphene. It is well known that van der Waals forces act on all materials, and thus provide a major influence on the adhesion energy.

The strongest of these forces is typically the London dispersion force, with a strength that is proportional to the polarizability of the materials involved [112]. Gold has a much larger polarizability than SiO_2 or Si_3N_4. Thus, the London dispersion force will be much greater for Au than for other substrates, causing the adhesion energy to be larger. This is manifested in the larger w/a ratio as the larger adhesion energy results in a small blister radius for a particular blister height. The stronger adhesion energy for Au as compared to SiO_2 and Si_3N_4 can be explained by this mechanism.

An inspection of Eq. (**3**-**3**) shows that the Young's modulus has a significant impact on the adhesion energy of 2D materials. Since the thickness of a 2D material should not vary dramatically, then a material with a higher Young's modulus should be expected to have a stronger adhesion than a material with a lower Young's modulus. However, the blister ratio also plays a key role in the adhesion energy. Once differences in the Young's modulus are accounted for, differences in the blister ratio can point to differences in interaction forces between a 2D material and any particular substrate. With graphene, the polarizability of a particular substrate can cause a major difference in the resulting adhesion energy, with larger polarizability resulting in higher adhesion energies.

4.0 External Modulation of Graphene TCR via Substrate Choice and NP Deposition

The work presented in this chapter was published in [113]. Reused in part with permission.

As stated before, graphene can be greatly impacted by different substrates and surface modifications. These differences can drastically alter important properties, such as electrical conduction pathing. Graphene has a theoretical limit of 200,000 $cm^2 V^{-1} s^{-1}$ to its electrical mobility, though practical experiments have only observed ~185,000 $cm^2 V^{-1} s^{-1}$ in optimized conditions [114]. Graphene's lattice configuration has each carbon atom covalently bonded to three others, leaving a fourth valence electron to form pi and pi-star bands that are responsible for its high carrier concentration and carrier mobility. For SLG, only two channels exist for carrier conduction, which are the top and bottoms surfaces of the single layer. These channels would ideally have an equal carrier distribution. This would allow for uniform motion when placed into an external electric field. Since these electrons almost never interact with carbon, electron-electron scattering is the dominant source of carrier interactions in these surface channels [115]. MLG has additional layers, with each additional layer adding an interlayer channel. Though the top and bottom surfaces of MLG act similarly to the SLG case, the interlayer channels differ. These interlayer channels operate under zero electric field, which is provided by the equal interference generated by surrounding carbon ions. This leaves the interlayer carriers to undergo entropic thermal motion. However, the electrons in the interlayers are affected primarily by phonon and electronic scattering when under the influence of an external electric field. This creates a distinguishing property between SLG and MLG forms.

Whether a carrier is in the surface channel or an interlayer channel will determine how strongly it is affected by temperature. In SLG, temperature has a negligible effect on electron-electron scattering and thus leads to a small temperature coefficient of resistance (TCR). However, the interlayer channels in MLG are much more susceptible to temperature differences due to the electric screening effect. In MLG, the resistance is so strongly linked to temperature that the resistance can decrease with increasing temperature, resulting in a negative TCR value. As the number of layers increases, the strength of the interlayer channels increases, leading to larger TCRs for graphene with more layers. Thus, the thickness of graphene can rapidly change its electrical conductivity levels [115].

The mobility temperature dependence in SLG and MLG can be affected by different material interfaces. This can be different substrates or surface modifications. It has been well observed that the conductive properties of suspended graphene are altered when it is adhered to a substrate. However, little research has been performed into how different specific substrates interact with graphene. This work investigates the interface effects between graphene and amorphous SiO_2 (glass), crystalline SiO_2, and Si_3N_4 through TCR measurements. These interactions help to study bottom channel effects. The top channel effects are studied by the incorporation of silver shell, silica-core metal nanoparticles (MNPs). The production of higher quality graphene devices can be achieved through this work, which seeks to advance the understanding of how external influences can affect graphene conduction paths.

4.1 Experimental Methods

The process of sample preparation and electrical characterization can be seen in Figure 9. MNPs were prepared and examined, followed by multiple TCR characterization tests.

Commercial SLG grown by CVD on copper foil process was acquired from Cheap Tubes Inc. A standard high-temperature atmospheric pressure CVD (APCVD) process was used to grow multilayer graphene (MLG) in-house using cleaned copper foil from Alfa Aesar. The top side of the graphene was spin-coated with PMMA495 A2, after which the backside of the copper was cleaned by soft abrasion to remove any backside graphene. The samples were used to inform the size of the graphene/copper that needed to be cut before being placed in aqueous APS. This removed the copper from the samples and left behind graphene/PMMA layers. The layers were then transferred to a DI water bath for 10 min, repeating this process three times to remove any remaining contaminants. The samples were then transferred to the target substrate and dried via hot plate to remove any water remaining between the graphene layer and the substrate. Acetone was then used to dissolve the PMMA layer, which was followed by a soak in IPA and dried using a hot plate.

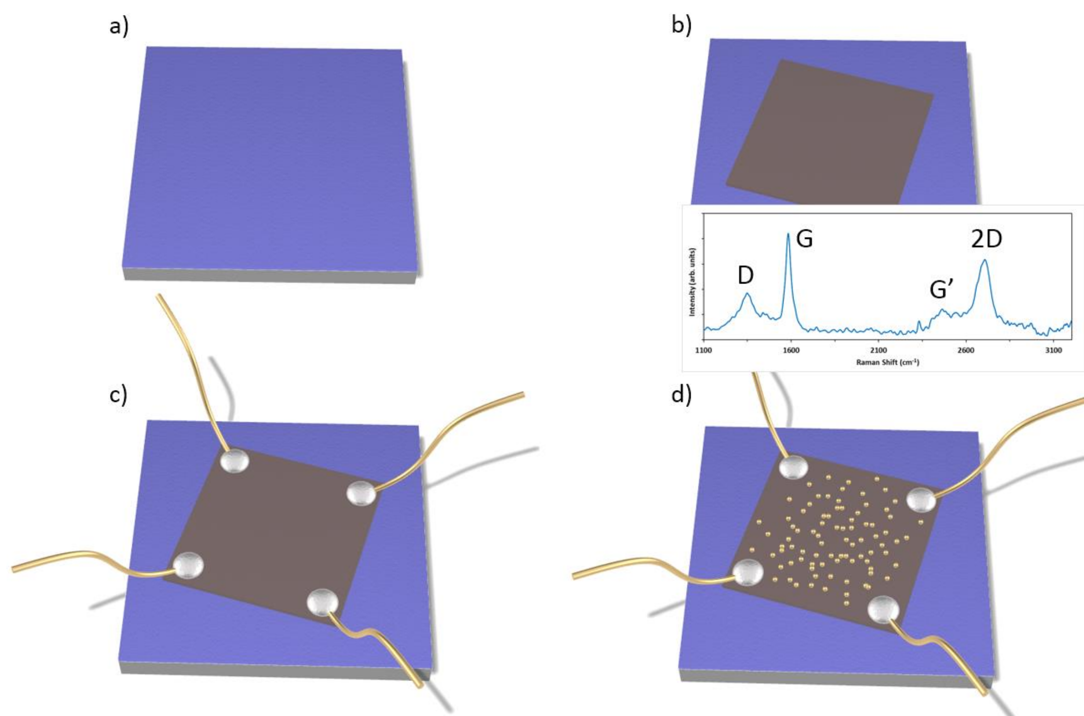

Figure 9. Representation of the sample preparation process. (a) The substrate is cleaned before graphene transfer; (b) a wet transfer process applies graphene to the substrate; (c) soldering/wire-bonding is used to bond contacts to graphene; (d) nanoparticles are drop cast on top of graphene. Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

SLG and MLG samples were transferred onto each of three acetone and IPA cleaned target substrates: glass, SiO_2, and Si_3N_4. Once transferred, the presence and quality of MLG was confirmed via Raman spectra analysis. Sample Raman data (532nm wavelength laser) is shown in the inset of Figure 9b, confirming the presence of MLG by the proper relation of D, G, G', and 2D peaks. The thickness was found to be ~8nm via AFM, which is consistent with Raman results.

A chemical process was used to create silver shell, silica-core nanoparticles with a diameter of 330 nm. This size was chosen because it will easily attach to the graphene surface. Silicon oxide nanoparticle cores with a diameter of 300 nm from Sigma-Aldrich were modified in an APTES solution for subsequent shell deposition. A $HAuCl_4$ solution from Sigma-Aldrich was reduced to

form gold seeds in parallel. This was then mixed with the modified silica cores to create the initial silica/gold nanoparticles. A solution of $AgNO_3$ was added to the nanoparticles to grow a silver nanoshell. The process was stopped once the shell grew 15nm, ensuring a total diameter of 330nm. The density of the nanoparticle solution was 10^8 MNPs/mL. The nanoparticle surface density was then controlled to be ~$3x10^7$ MNPs/cm^2.

Indium-tin was soldered onto the SLG samples for electrical contacts while gold was wire-bonded to the MLG samples. Both SLG and MLG contacts were made in a van der Pau configuration. The resistivity, charge concentration, and mobility results for SLG samples were obtained from a Hall Effect machine (Ecopia HMS-5000) over a temperature range of 310-350K with a 10K step. The results for MLG samples were obtained from a vacuum cryostat from over a temperature range of 200-320K with a 10K step. At each step, 15 data points were collected and averaged together. After each sample was observed without nanoparticles, the tests were redone after MNPs were coated. This allowed the determination of how nanoparticles on the surface of graphene affected its electrical properties.

4.2 Results and Discussion

The data for SLG on glass is shown in Figure 10. The sheet resistance (Ω/sq) can be seen in Figure 10a, while Figure 10b shows the mobility (cm^2/Vs) on the left axis (blue diamond markers) and the sheet concentration (cm^{-2}) on the right axis (orange circle markers). Each figure is shown as a function of temperature with data from 300K to 350K. The linear fit and % change of the data are shown in Table 5. SLG without nanoparticles on glass is shown to experience a resistance increase as the temperature increases. At the same time, the sheet concentration is seen

to increase as the mobility decreases. As resistivity is inversely proportional to the sheet concentration and mobility, mobility shows itself to be the dominant mechanism in this case. This is expected by theoretical results [115]. Additionally, the % change in the mobility and the sheet concentration can be combined to show a similar % change in the sheet concentration, showing the contribution of each towards the resulting resistance increase. The mobility decrease can be attributed to interfacial electron-phonon scattering between the graphene and the glass substrate [115]. The sheet concentration increase occurs from the increased absorption of ambient molecules [116].

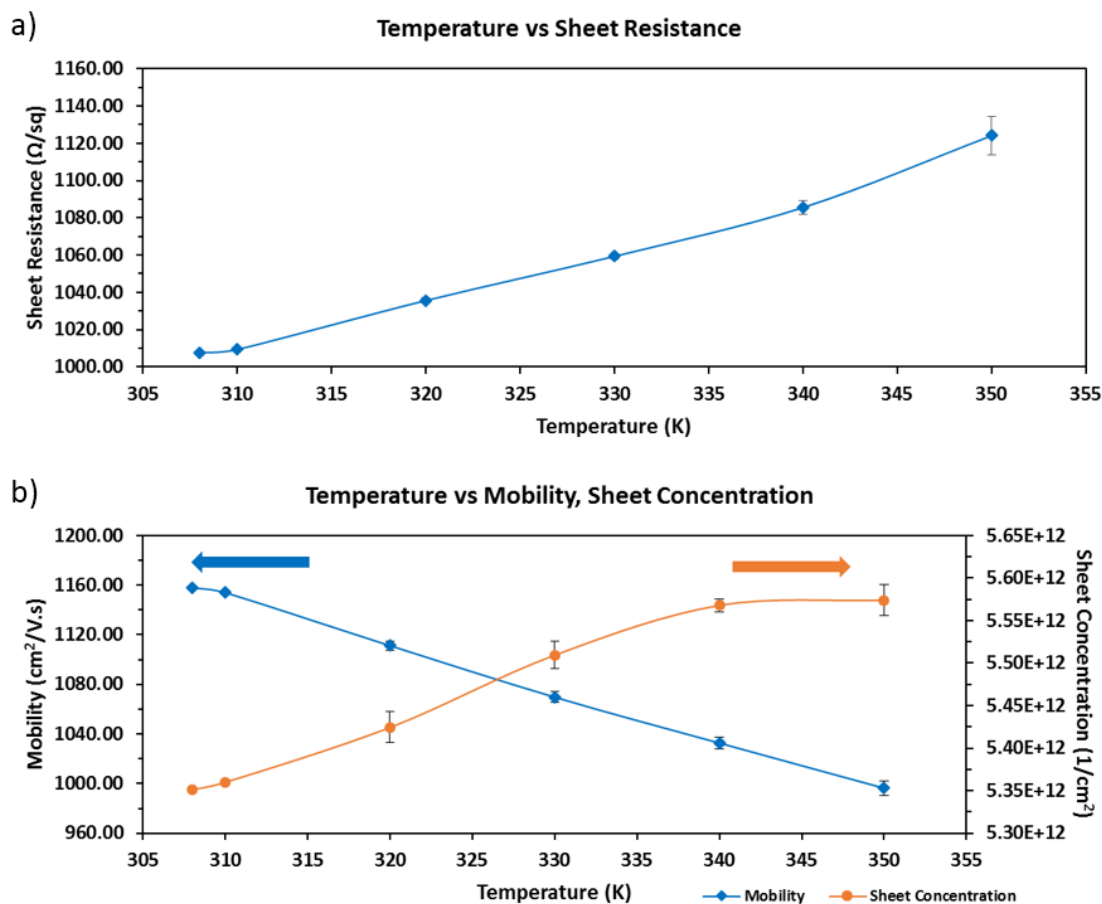

Figure 10. SLG without nanoparticles on glass for (a) sheet resistance, (b) mobility (blue diamond markers, left axis), and sheet concentration (orange circle markers, right axis) over the temperature range 300-350K Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

Table 5. SLG without nanoparticles on glass data using Linear fit slope, 310 K value, and % change of data shown in Figure 10.

	Slope	310 K Value	% Change per K (310-350 K)
Sheet Resistance	2.712 Ω/sq/K	1009.304 Ω/sq	0.284
Mobility	-3.914 $cm^2/Vs/K$	1150.810 cm^2/Vs	-0.341
Sheet Concentration	5.847E+09 $1/cm^2/K$	5.369E+12 $1/cm^2$	0.100

The data for the SLG sample on glass modified by MNPs is shown in Figure 11. The sheet resistance (Ω/sq) can be seen in Figure 11a, while Figure 11b shows the mobility (cm^2/Vs) on the left axis (blue diamond markers) and the sheet concentration (cm^{-2}) on the right axis (orange circle markers). Each figure is shown as a function of temperature with data from 300K to 350K. The linear fit and % change of the data are shown in Table 6. The R^2 value for the linear fit of the sheet resistance is about 90%. It is easily seen that the MNPs have a significant impact on the observed properties of graphene. An increase of 100 Ω/sq in the sheet resistance is caused by the MNPs acting as scattering centers. The temperature coefficient of resistance (TCR) can be seen to decrease as well. The change comes about due to the switch of the dominant mechanism for the resistance to mobility from sheet concentration. Since the MNPs have a silver shell, a charge transfer is likely taking place. The carrier absorption that occurs from the MNPs disrupt the surface channel in such a way as to influence the charge carriers ability to flow inside graphene with the increased thermal motion [117, 118].

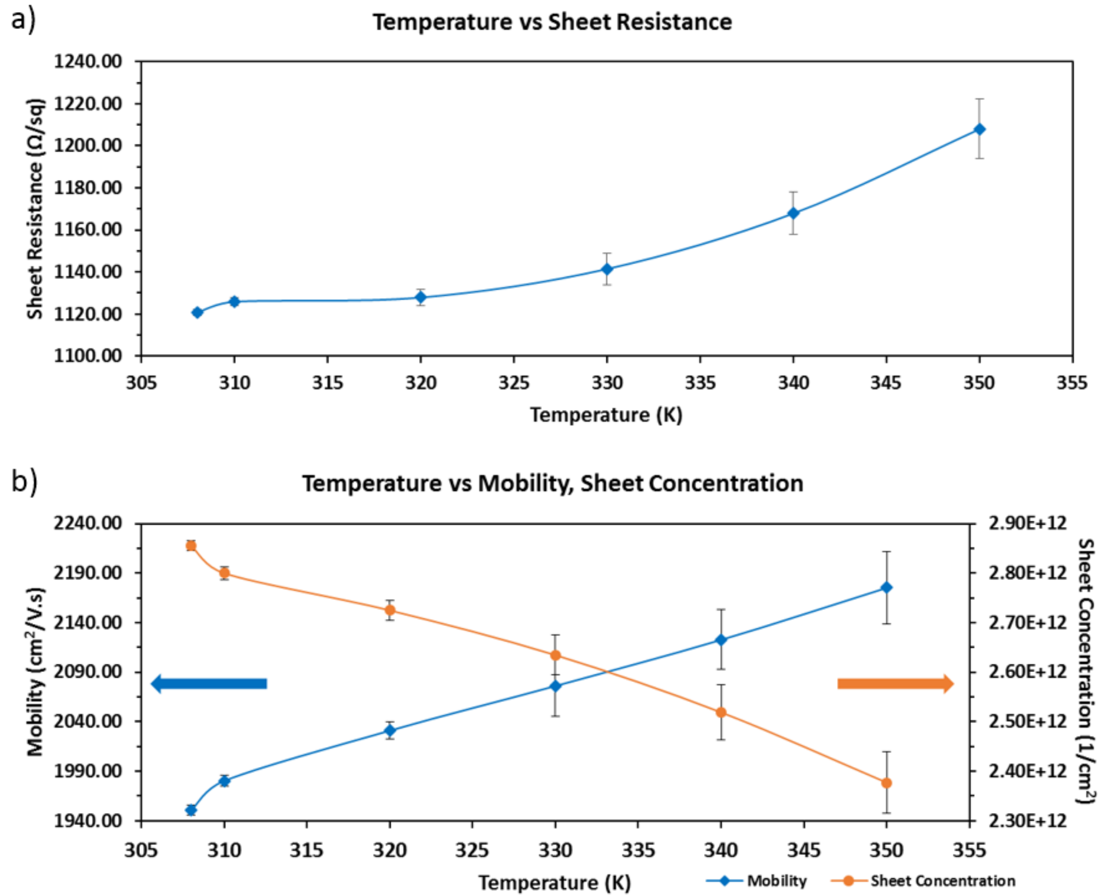

Figure 11. SLG with nanoparticles on glass for (a) sheet resistance, (b) mobility (blue diamond markers, left axis), and sheet concentration (orange circle markers, right axis) over the temperature range 300-350K. Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

Table 6. SLG with nanoparticles on glass data using Linear fit slope, 310 K value, and % change of data shown in Figure 11

	Slope	310 K Value	% Change per K (310-350 K)
Sheet Resistance	1.893 Ω/sq/K	1117.715 Ω/sq	0.182
Mobility	5.082 $cm^2/Vs/K$	1972.971 cm^2/Vs	0.246
Sheet Concentration	-1.068E+10 $1/cm^2/K$	2.826E+12 $1/cm^2$	-0.377

The data for SLG on SiO_2 is shown in Figure 12. The sheet resistance (Ω/sq) can be seen in Figure 12a, while Figure 12b shows the mobility (cm^2/Vs) on the left axis (blue diamond markers) and the sheet concentration (cm^{-2}) on the right axis (orange circle markers). Each figure is shown as a function of temperature with data from 300K to 350K. The linear fit and % change of the data are shown in Table 7. The sheet resistance increases as with the glass substrate, though the mobility in this case is much lower. The ordered lattice of the SiO_2 substrate likely presents a greater scattering source than the amorphous lattice of glass. Additionally, the sheet concentration is increased over the glass substrate. Oxygen is the probable cause of both effects. It is known that oxygen interacts with graphene in a much stronger form than Si, and it can induce a p-type doping effect in graphene [119]. Thus, O atoms are the likely scattering centers. However, the increasing temperature is accompanied by an increase in mobility, while the sheet concentration decreases. This is unlike the glass substrate. This difference results in a % change in the resistance that is slightly lower, but still similar to the glass substrate case.

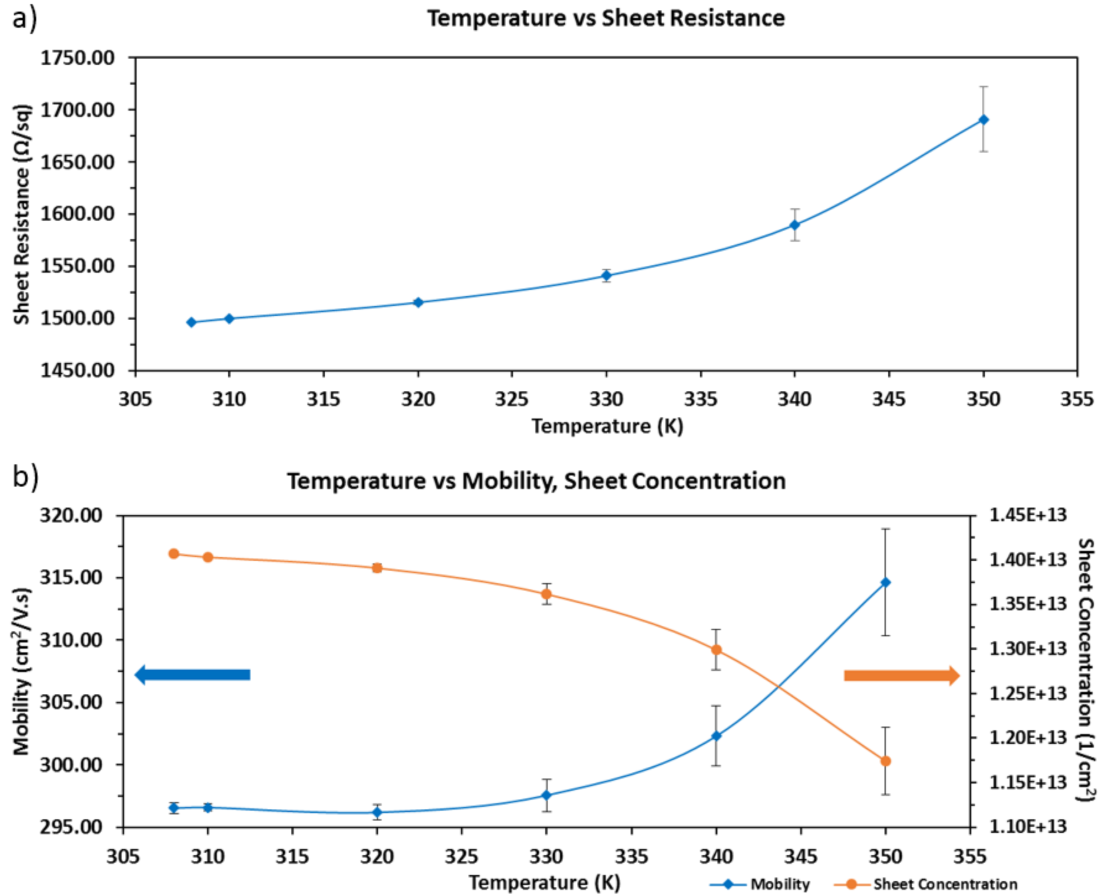

Figure 12. SLG without nanoparticles on SiO_2 for (a) sheet resistance, (b) mobility (blue diamond markers, left axis), and sheet concentration (orange circle markers, right axis) over the temperature range 300-350K. Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

Table 7. SLG without nanoparticles on SiO_2 data using Linear fit slope, 310 K value, and % change of data shown in Figure 12 [59].

	Slope	**310 K Value**	**% Change per K (310-350 K)**
Sheet Resistance	4.183 Ω/sq/K	1487.182 Ω/sq	0.281
Mobility	0.365 cm^2/Vs/K	294.671 cm^2/Vs	0.124
Sheet Concentration	-4.975E+10 1/cm^2/K	1.421E+13 1/cm^2	-0.350

The data for the sheet resistance of SLG on SiO_2 with MNPs is shown in Figure 13a while the mobility and sheet concentration are shown in Figure 13b. The format is unchanged from the previous graphs. As before, Table 8 shows the accompanying linear fit results. In comparison to the case without MNPs, the mobility has increased while the sheet concentration has decreased. The MNPs are again responsible for an overall increase in sheet resistance due to their roles as carrier scattering centers. In this case, the decrease of the concentration allows for the possibility of less electron-electron scattering. The mobility can then increase enough to provide a small offset to the decrease in carrier concentration.

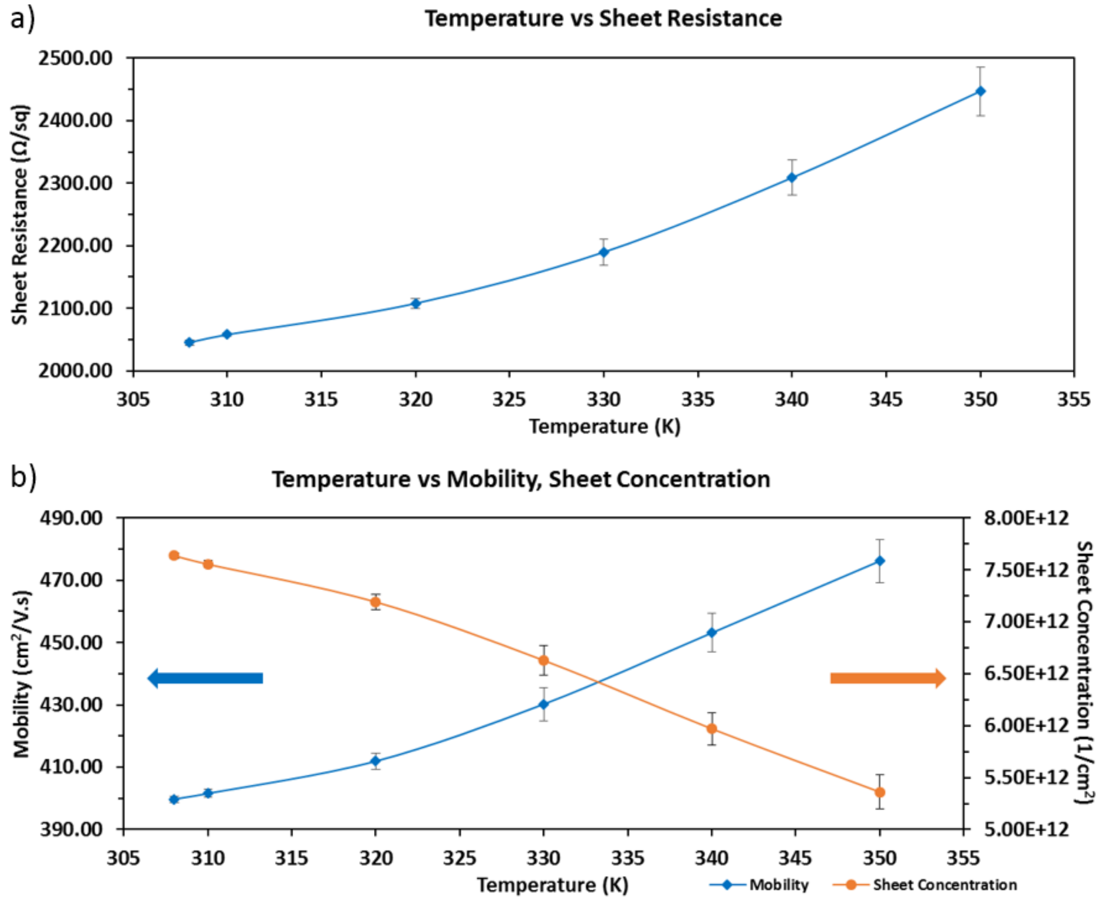

Figure 13. SLG with nanoparticles on SiO_2 for (a) sheet resistance, (b) mobility (blue diamond markers, left axis), and sheet concentration (orange circle markers, right axis) over the temperature range 300-350K. Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

Table 8. SLG with nanoparticles on SiO_2 data using Linear fit slope, 310 K value, and % change of data shown in Figure 13

	Slope	**310 K Value**	**% Change per K (310-350 K)**
Sheet Resistance	9.297 Ω/sq/K	2040.913 Ω/sq	0.456
Mobility	1.812 cm^2/Vs/K	399.203 cm^2/Vs	0.454
Sheet Concentration	-5.426E+10 1/cm^2/K	7.609E+12 1/cm^2	-0.713

The sheet resistance of SLG without MNPs on the final substrate, Si_3N_4, is shown in Figure 14a. The same format previously discussed for the mobility and sheet concentration data is kept for Figure 14b. The linear fit data is shown in Table 9. The sheet resistance increases as with other substrates, while the mobility increases, and the sheet concentration decreases. This is similar to the SiO_2 case. However, Si_3N_4 has the highest resistance and most sensitivity of any tested substrate without nanoparticles. A previous study indicated that Si_3N_4 should have weak interactions with graphene [120]. This study was using β- Si_3N_4 (0001) which has the capability to have graphene lie completely flat. It is unlikely that the wet transfer process used in this study allowed for a completely flat piece of graphene. This uneven surface causes a resistance increase, though it is comparable to other studies [121]. The increase in sensitivity may be explained by the thermal conductivity of Si_3N_4 over SiO_2. The higher thermal response is likely influenced by the increased heat transfer from the substrate to the graphene, allowing the graphene to react accordingly.

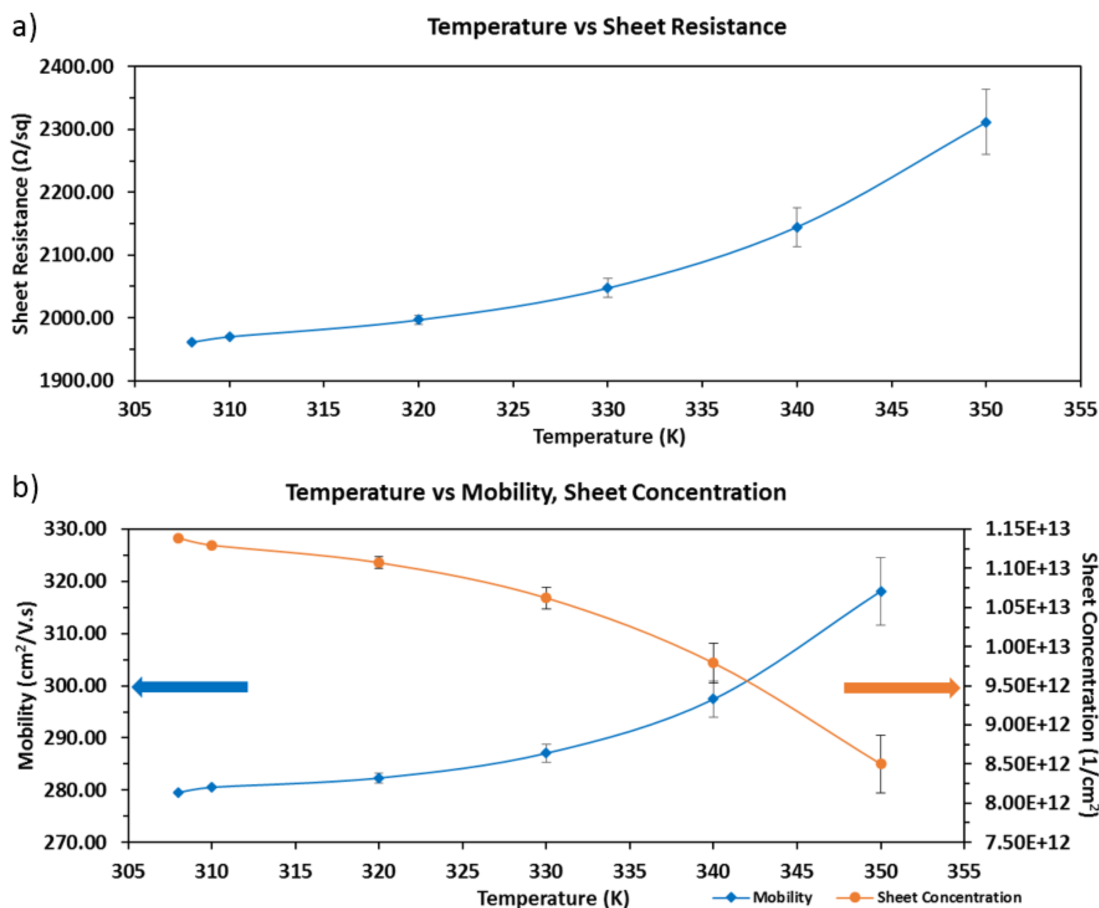

Figure 14. SLG without nanoparticles on Si_3N_4 for (a) sheet resistance, (b) mobility (blue diamond markers, left axis), and sheet concentration (orange circle markers, right axis) over the temperature range 300-350K. Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

Table 9. SLG without nanoparticles on Si_3N_4 data using Linear fit slope, 310 K value, and % change of data shown in Figure 14

	Slope	**310 K Value**	**% Change per K (310-350 K)**
Sheet Resistance	7.659 Ω/sq/K	1946.703 Ω/sq	0.393
Mobility	0.820 $cm^2/Vs/K$	277.450 cm^2/Vs	0.296
Sheet Concentration	-6.373E+10 $1/cm^2/K$	1.149E+13 $1/cm^2$	-0.555

The final test for SLG was performed on Si_3N_4 with MNPs on the sample. As before Figure 15a shows the sheet resistance while Figure 15b shows the mobility and sheet concentration using the previous format. The linear fit results are shown in Table 10. While the sheet resistance increases, a decrease in the % change is observed as compared to without MNPs. The introduction of the MNPs results in less significant thermal coupling than before. The gain in mobility is offset by the decrease in sheet concentration. Together, these effects result in a weaker temperature connection to the resistance value. Here, charge transfer results in less carriers affected by thermal motion [117, 118].

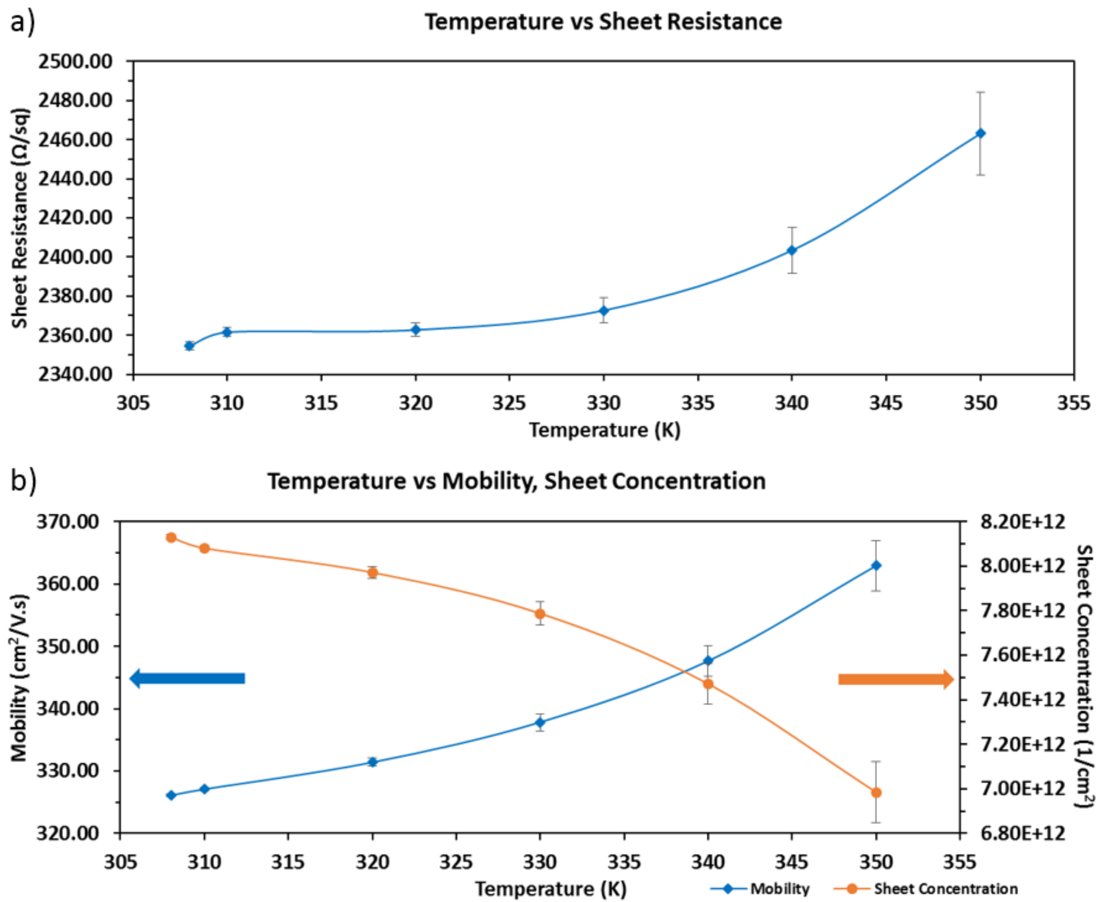

Figure 15. SLG with nanoparticles on Si_3N_4 for (a) sheet resistance, (b) mobility (blue diamond markers, left axis), and sheet concentration (orange circle markers, right axis) over the temperature range 300-350K. Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

Table 10. SLG with nanoparticles on Si_3N_4 data using Linear fit slope, 310 K value, and % change of data shown in Figure 15

	Slope	310 K Value	% Change per K (310-350 K)
Sheet Resistance	2.238 Ω/sq/K	2349.740 Ω/sq	0.095
Mobility	0.826 cm^2/Vs/K	325.342 cm^2/Vs	0.254
Sheet Concentration	-2.533E+10 1/cm^2/K	8.152E+12 1/cm^2	-0.311

MLG was also evaluated on glass, SiO_2, and Si_3N_4 substrates to observe how the resistivity and TCR was affected by the introduction of more layers of graphene. Figure 16 shows the sheet resistance results for MLG on glass, providing a direct comparison to the SLG samples. The blue diamonds mark MLG without nanoparticles on glass, while the orange circles show MLG with nanoparticles on glass. The resistance goes down with increasing temperature, as expected from theory [115]. The thermally driven carrier activity is amplified by the increase in temperature, resulting in less resistance. This contrasts with the SLG behavior that increases in resistance as the temperature increases. The MNP caused a sharp increase in the resistance, again acting as scattering centers. Table 11 shows the linear fit data. The MLG % change is smaller than the SLG case, as the increasing thickness of graphene lessens the substrate effect. The difference in testing protocol plays a role in the difference in measured resistances. The SLG samples were subject to external scattering sources due to ambient absorption, while the MLG samples had a vacuum environment to minimize such disruption. The contact resistance likely does not play a significant role in the results. Both SLG and MLG are semimetals, allowing for a small ohmic contact resistance. The samples were both tested in van der Pau configuration, which allows the low contact resistance to be ignored.

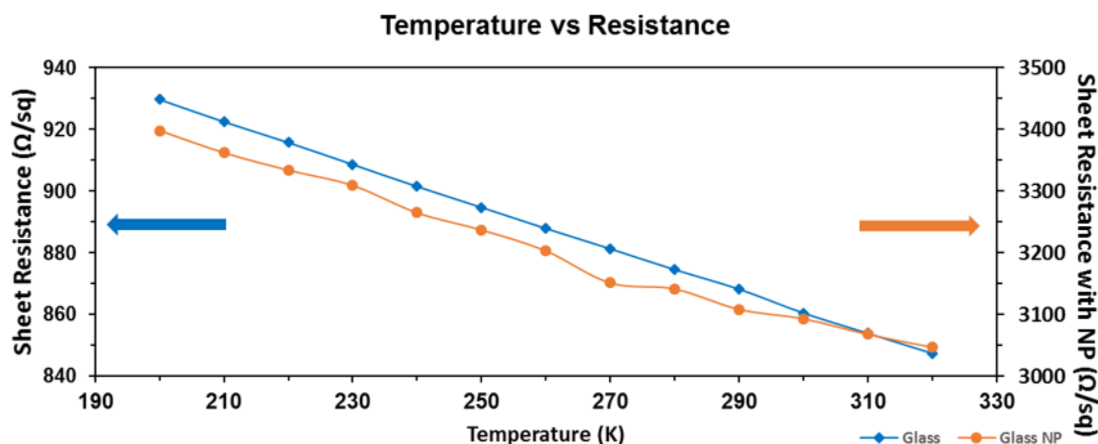

Figure 16. MLG without nanoparticles (blue diamond) and with nanoparticles (orange circle) on glass over the temperature range 200-320K. Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

Table 11. MLG with and without nanoparticles on glass data using Linear fit slope, 300 K value, and % change of data shown in Figure 16

	Slope	300 K Value	% Change per K (200-320 K)
Glass	-0.685	860.833	-0.0737
Glass (nanoparticles)	-3.010	3088.748	-0.0861

The data for MLG on SiO_2 is shown in Figure 17 and is formatted as above. As before, the ordered SiO_2 increases the interfacial scattering between the graphene and the substrate layers as compared to the amorphous glass case. Table 12 shows the linear fit data. The magnitude of the % change per Kelvin of the sheet resistance is lowered by the interfacial scattering. Specifically, the electron-phonon scattering reduces the mobility of the graphene layers closest to the substrate [115]. Similarly to the SLG case, the ordered O atoms interact more strongly with graphene and are the major cause of carrier scattering [119].

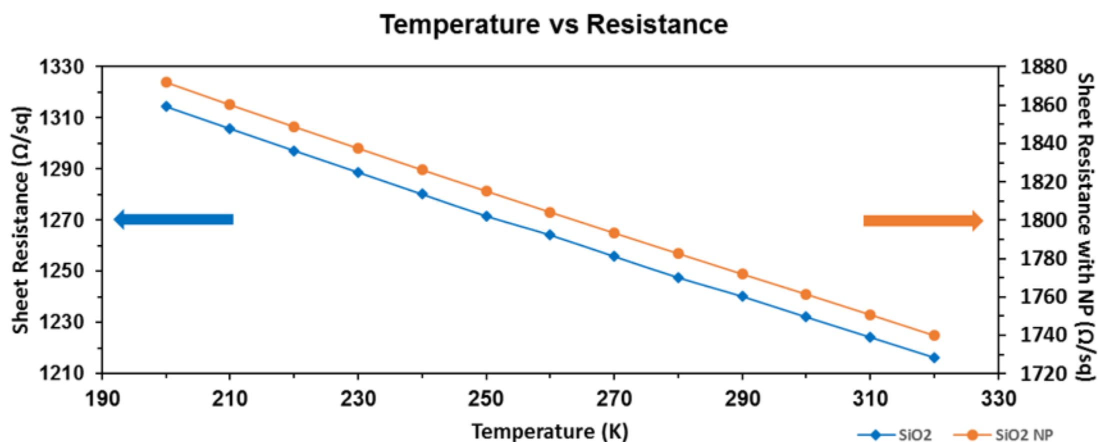

Figure 17. MLG without nanoparticles (blue diamond) and with nanoparticles (orange circle) on SiO_2 over the temperature range 200-320K. Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

Table 12. MLG with and without nanoparticles on SiO_2 data using Linear fit slope, 300 K value, and % change of data shown in Figure 17

	Slope	300 K Value	% Change per K (200-320 K)
SiO_2	-0.815	1231.879	-0.0622
SiO_2 (nanoparticles)	-1.096	1761.078	-0.0587

The final MLG test case was performed on a Si_3N_4 substrate. The results are shown in Figure 18 following the previous format. As before, Table 13 shows the linear fit data. The graph shows that MLG on Si_3N_4 provides the lowest resistance of the three interfaces. The data is in agreement with data from Davaji et al. [122]. This is due to the decreased influence of N atoms on interfacial scattering as compared to O atoms [120]. Here, the MNPs did not provide a significant increase to the resistance, but still provided additional scattering centers. While the resistance was not shifted significantly, the TCR was revealed to have the strongest temperature dependence of any sample combination. It is posited that the electric field from the graphene/substrate interface

is reduced within the interlayers of MLG, allowing a more significant thermal motion of the carriers to arise.

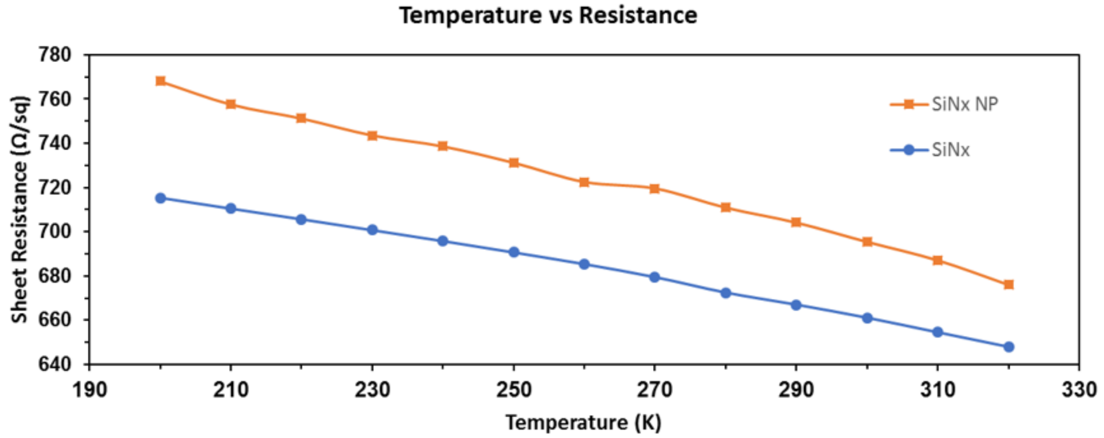

Figure 18. MLG without nanoparticles (blue circle) and with nanoparticles (orange square) on Si_3N_4 over the temperature range 200-320K. Reprinted with permission from [113]. Copyright [2020] American Chemical Society.

Table 13. MLG with and without nanoparticles on Si_3N_4 data using Linear fit slope, 300 K value, and % change of data shown in Figure 18.

	Slope	**300 K Value**	**% Change per K (200-320 K)**
Si_3N_4	-0.561	661.163	-0.0785
Si_3N_4 **(nanoparticles)**	-0.721	694.652	-0.0998

5.0 Dual-Sided Wafer of Graphene Field Effect Transistors

Research into the properties of graphene has enabled better integration into CMOS-based devices. The advent of CMOS technology led to a surge in information processing capabilities and has become an integral part of everyday life, thus requiring graphene research to provide integration methods. Typical CMOS research has continued miniaturizing transistor sizes in previous decades to increase speed and efficiency. These investigations have reduced FET gate sizes to a few nanometers, approaching the size of single atoms [123]. The smaller FETs have allowed integrated circuits (ICs) to go from thousands to billions of FETs on a single chip. The success of this miniaturization has driven technology to the limits of human knowledge, with further efforts to scale down the transistor becoming increasingly unlikely. Though physical limits are being reached, the demand for increased information processing abilities has continued to rise due to the advent of artificial intelligence, big data, and deep learning [124, 125]. However, there is hope on the horizon. Researchers have been exploring new paradigms of advancement, and one such method that has seen promising results is the transition from planar integrated circuits to three-dimensional integrated circuits (3D ICs).

The concept of 3D ICs is not new, with its earliest demonstration dating back to the 1980s [126]. However, at that time, it was more convenient to scale down the planar size of the FET structure, leading to limited research into 3D ICs. The interest in utilizing the third dimension remained low until recent years when the theoretical physical limits started to loom. The potential of 3D IC technology lies in its ability to increase the available computing area. The increased computing area comes from stacking different layers on top of each other. A 3D IC is fabricated as a series of layers, each requiring the ability to communicate with the other layers. The lack of

suitable communication methods limited 3D IC technology until the advent of through silicon vias (TSVs). TSVs are vertical electrical connections that pass through the silicon substrate of a wafer. TSVs are created through an etching process, which creates holes in the wafer that can be filled with conductive material. The TSVs allow for different layers to pass information between each other and can allow for shorter pathways, allowing for 3D IC performance to rise in comparison with mainstream 2D techniques. The research into this paradigm has been steady, with various academic and commercial enterprises showcasing technological advancements and the potential benefits of rigorous study into the technique. Recently, system-in-package chips, with different wafers bonded vertically, have been making their way into commercial products, along with 3D memory technology and 3D gate structures [127-129]. However, widespread use of 3D ICs has yet to be achieved. With the steady increase in technology and the added pressure of planar technology reaching its limits, 3D ICs are poised to make significant strides in the semiconductor industry due to their numerous benefits.

The rise of 3D ICs has necessitated research into fabrication methods. There are two main methods of 3D manufacturing: monolithic integration (Figure 19a) and wafer bonding (Figure 19b). In the wafer bonding method, each layer of the 3D IC is fabricated in parallel. Once fabricated, the layers are aligned and bonded together. Depending on process flow, TSVs can be fabricated before or after bonding and are used to connect the different device layers. The wafers are bonded either front-to-front, front-to-back, or back-to-back, presenting different advantages and disadvantages. On the other hand, the monolithic method sequentially fabricates a 3D IC. Each layer is built on the layer before it. This method does not require alignment or bonding of different wafers and can allow for much smaller metal interlayer vias (MIVs) to be used and, thus, higher circuit densities. The method allows the first layer to use the high-temperature processes necessary

to achieve gate sizes of a few nm. The method then transfers a thin (10-100s nanometers) dielectric layer on top that can be recrystallized and placed on top of the active circuitry. This dielectric layer makes the monolithic method thinner than the wafer bonding method. Since subsequent high-temperature processes cause unwanted dopant diffusion, all following layers are constrained to using low-temperature processes. These two methods offer different advantages and challenges, and the choice between them depends on the specific requirements of the 3D IC being fabricated.

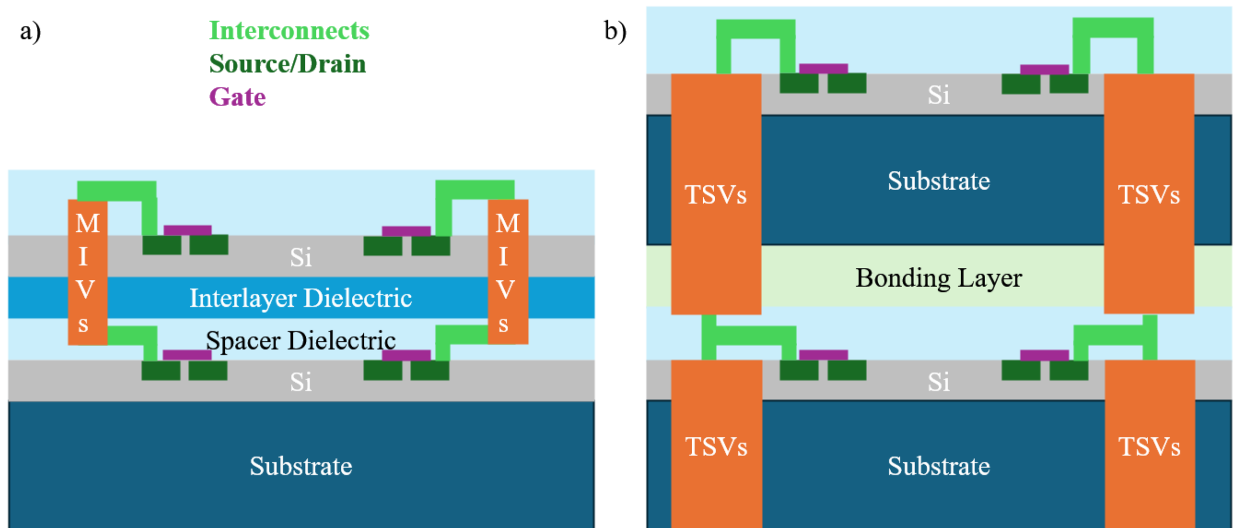

Figure 19. Different 3D IC fabrication methods. a) Monolithic Method; b) Wafer Bonding Method.

The 3D IC paradigm offers several unique advantages in advancing computer processing power. Unlike planar technology, which has limited ability to scale down the size of a transistor or the size and speed of the interconnects, 3D ICs use an additional dimension to address this scaling problem and enhance the communication speed between active units. These benefits include smaller footprints, potentially reduced cost, heterogeneous integration, shorter interconnects, reduced power consumption, increased connectivity, innovative design possibilities, increased circuit security, and increased bandwidth. It is important to note that these benefits are

accompanied by potential challenges that require consideration. The challenges include cost increases, yield reductions, heat buildup, design complexity, size of TSVs, testing difficulty, lack of standards, supply chain integration difficulty, and ownership of the final product.

3D ICs bring many potential advantages over planar techniques. The use of the z direction enables reduced distances in multiple ways. Both fabrication techniques can provide smaller area footprints. These footprints can be achieved by layering different active designs on top of one another, allowing powerful devices to fit into smaller spaces. Splitting the chip into smaller layers can also decrease the distance between various parts of the chip, potentially decreasing circuit delay if the capacitance of the 3D wire can be kept down. The capacitance and distance will affect power consumption, with lower capacitance and shorter distances resulting in less power loss due to parasitic capacitance. The lower power consumption reduces heat generation and can lead to extended battery life and lower operating costs. The increased density of components allows for higher performance and functionality. This effect is more prominent for monolithic integration due to the ability to use smaller vias. The cost of the chip can be reduced by improving yield if a large chip can be partitioned and stacked, with the individual partitions being evaluated separately. Due to the different fabrication processes available, a 3D IC can incorporate many different processes into its creation by using wafer bonding techniques, allowing for a broader range of components to be integrated into a single device. Altogether, these possibilities allow for more complex designs with increased connectivity while improving security. 3D integration can allow for the obscuration of the function of each layer and allow for the implementation of hardware-level monitoring that can protect components from malicious code. Finally, the chip's bandwidth can be increased due to the ability of many vias to be placed between layers. This increase in bandwidth can alleviate the difficulty encountered by processing units that stand idle while waiting for communication

from memory units [130, 131]. The benefits of 3D ICs are numerous and exciting, and they hold the potential to revolutionize the semiconductor industry.

While 3D IC technology offers numerous benefits, the ability to reduce the area footprint of IC chips presents its own set of challenges. Commercialization has been challenging due to the complex process involved, leading to companies being unaware of the cost drivers and, thus, unable to implement cost reductions. Additionally, fabrication techniques need to ensure appropriately high yields. These yields can only be achieved with careful process control, including accurate alignment, controlled etching, deposition, and other processes. This level of process control will also reduce via deformations. High yields can only be achieved by testing 3D ICs and identifying where defects occur. The ability for 3D IC technology to reach mainstream adoption will require the capability to repair or reduce defects and identify when such defects occur. Testing these different layers has been difficult, especially when different sections of the same planar circuit are divided into different layers, preventing independent testing by conventional techniques. New design techniques and tools are needed to leverage the benefits of 3D integration fully. These tools need to consider the localized heating that can occur and allow the management of thermal hotspots. The heating can cause thermal mismatches, which can spoil the device. These design tools are also needed to ensure efficient routing [130, 131].

Another challenge is that the designs need to account for the size differences between TSVs and FET structures, as well as the landing zones, and keep out areas required for TSV structures to avoid generating defects. Such considerations will have an impact on wire length, as well as cause placement and routing issues. Finally, there needs to be more standards in the industry, issues with integrating different supply chains for each device layer, and the need for ownership for 3D

IC integration and assembly. Research has been done to alleviate these issues, with academic investigations focusing on the technical aspects of 3D ICs and the integration of 2D materials.

Another avenue of research into 3D ICs has been the incorporation of 2D materials. As explained before, the unique electrical and thermal properties of 2D materials, such as graphene, provide an appealing avenue of advancement for ICs. They can be integrated into 3D ICs, where they can be stacked to create compact, high-performance devices or utilized in conjunction with existing CMOS technology to improve performance and functionality. Using 2D materials provides an exciting opportunity with plenty of advantages and challenges to overcome.

The incorporation of 2D materials into 3D processing offers several advantages. The first is improved performance. The properties of 2D materials can enhance electrical speed, power consumption, and thermal management performance if appropriately implemented. 2D materials provide increased functionality by their size, allowing for smaller devices. This increase in functionality is provided by the ability to incorporate several types of circuits with traditional CMOS technology. These materials can be used with current manufacturing processes, requiring minor changes to existing infrastructure for their processing. However, a challenge unique to 2D materials is growing or transferring a 2D material onto a CMOS wafer that has yet to scale commercially and accounting for the changes in material properties when integrating 2D materials onto traditional substrates. The remaining challenges for 2D to 3D IC integration are similar to those faced by traditional 3D IC implementations.

Most areas of research in 3D IC technology are conducted in the fabrication or layout of a particular device. Hu and Chen developed a low-temperature Cu-Cu bonding process for 3D ICs [132]. Ding et al. created a way to better manage the thermal issues that develop while running a 3D IC [133], and Thuries et al. developed a way to lay out the circuits to take advantage of the

extra spatial dimension and reduce the power and area needed [134]. However, more research needs to be done on creating transistors on both sides of a wafer. Lai et al. [135] established a process for using ultrathin silicon wafers to create FETs on both sides, and we are not aware of any other examples of such a device.

We propose the creation of a dual-sided GFET wafer, as seen in Figure 20. A dual-sided GFET wafer can address some of the limitations created using only wafer bonding or monolithic techniques. In this structure, a wafer's front and back sides are used as active regions, as seen in Figure 20a, creating patterns on each side that can connect with TSVs or MIVs when using thinner wafers. Each side can be processed to have the full capability of single-sided wafers, doubling the available surface area. The IC will have further component density through the vias as the two sides can communicate directly, as seen in Figure 20b. The increased density from the vias will allow for some of the benefits of monolithic fabrication. Each face of the wafer can additionally be bonded to other similarly processed wafers, thus allowing for wafer stacking. The ability to stack the wafers while using the vias usually reserved for monolithic integration allows for the strengths of each process to be utilized and to compensate for the weaknesses of the other.

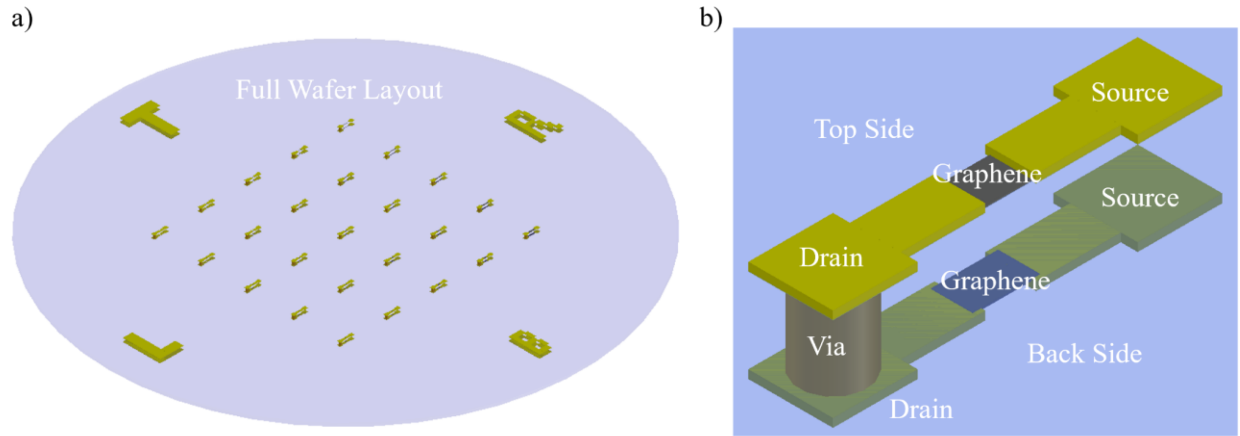

Figure 20. 3D Model of a dual-sided graphene FET. a) Whole wafer; b) Close-up of a single device structured as an inverter

A dual-sided wafer holds many advantages over traditional circuit and 3D IC designs. A dual-sided wafer effectively doubles the usable surface area available for circuit fabrication, increasing the number of transistors on a chip and enhancing functionality. The increased surface area allows for more compact and powerful semiconductor devices. Compact, potent devices are critical to ensuring that mobile devices and the Internet of Things (IoT) continue providing the computational and sensing power demanded [136, 137]. Fitting more transistors into the same space makes achieving better performance in these areas possible. Additionally, the potential doubling of transistors may lead to cost reductions in the future once the fabrication process matures.

An additional advantage to dual-sided wafer processing is the ability to use a dual-sided wafer as a layer in 3D fabrication. In a typical layer fabrication process, the layer must be bonded back-to-front, front-to-front, or back-to-back. Each layering type has its advantages, but front-to-front contact allows for the shortest propagation paths, enhancing performance by reducing delays. This technique can create many front-to-front connections and use internal connections between

faces to reduce propagation delays, thereby providing the highest performance possible. It enables the fabrication process to utilize the best aspects of layering and monolithic fabrication processes and minimize the drawbacks associated with each process.

Our investigations into the transfer and adhesion characteristics of graphene make the ability to create DSGFETs possible. The improved transfer process will minimize graphene defects, allowing more devices to be fabricated successfully. A clean transfer process is essential to minimize contamination that degrades graphene's electrical properties while enabling integration with existing CMOS fabrication processes. The transfer process provides the starting point for GFET fabrication, requiring a well optimized process for best results. For the best transfer possible, it is necessary to ensure good adhesion. A strong adhesion will allow the graphene to survive the processing required to fabricate on both sides of the device and ensure device stability. As we have discovered with our adhesion and TCR studies, oxygen atoms strongly influence graphene's properties. Additionally, the polarizability of the atom plays a role in the adhesion characteristics of graphene. Since it is desirable to use high-k dielectrics for improved FET performance, we choose Al_2O_3 as our gate oxide for increased adhesion. This increased adhesion allows us to be certain that the graphene will survive a dual-sided process. Additionally, Al_2O_3 can passivate and eventually encapsulate graphene surfaces and provide enhanced dielectric capabilities [138, 139].

To display the viability of our idea, we have created a wafer with GFETs on both the front and back sides. We use a global back-gate to simplify the initial prototype and reduce the considerations we need to make for fabrication. Backside alignment through the infrared camera was not attempted as such capabilities are well-established and unnecessary for this initial foray into dual-sided processing [140]. We examine the properties of GFETs on both sides of the wafer

to determine the feasibility of fabrication and quality of the resulting devices. These devices can be interconnected and otherwise improved upon in future experiments to showcase additional functionality.

5.1 Experimental Methods

Figure 21 shows a broad overview of the process of fabricating dual-sided devices. After fabrication, each device on either side was tested to determine suitable candidates for use as an inverter.

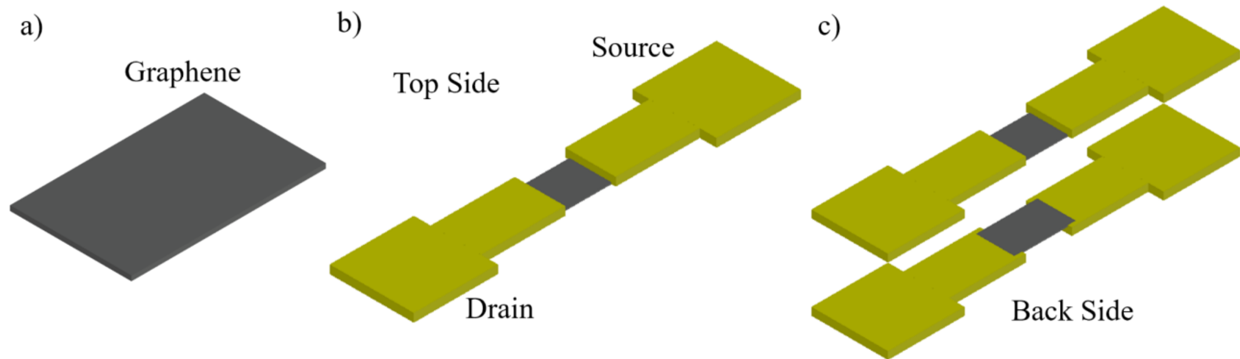

Figure 21. Fabrication process overview. a) Graphene transfer and etching; b) Source and drain contact deposition; c) repeat steps a and b on the backside

The fabrication process began with a Si p-type wafer with 500 um overall thickness. The wafer was cleaned using acetone and IPA. A plasma ALD process was used to grow 30nm of Al_2O_3 on both sides to make the back gate oxide. The ALD temperature was set to 150 °C during the growth process. SLG was obtained commercially (Grolltex) and transferred using a standard wet transfer procedure. In the wet transfer, 495A4 PMMA was used as the support layer. A mixture

of 6 g of APS and 133 mL of DI water was used to etch the copper growth layer. The graphene/PMMA was then scooped onto a clean wafer and transferred into a fresh DI water bath. The graphene was left for 10 minutes to clean any extra particulates from the graphene and then transferred to another fresh DI water bath. The water bath was repeated for a total of 3 water baths. After the graphene/PMMA was cleaned, it was scooped onto the wafer, where excess DI water was removed via kimwipe. The remaining moisture was heated via a hot plate to allow evaporation to remove the rest. The transferred graphene was patterned using photolithography. The SC1827 photoresist was dropped onto the wafer and spun at 3000 rpm for 45 seconds, followed by a 110 °C bake for 2 minutes. It was exposed for 172 mJ underneath a photomask and developed in a Developer 351:DI water bath with a 1:4 ratio of liquids. Once the photoresist was developed, the wafer was placed into an RIE chamber and exposed to oxygen plasma for 2 minutes. The plasma used 50 sccm of oxygen at 100 W and 100 mT to remove unwanted graphene. The photoresist was removed with acetone and IPA and dried via hotplate to avoid damaging the graphene.

Another photolithography step was completed using the same photoresist process as before. This time, the photomask allowed for the e-beam deposition of 4 nm Ti and 150 nm Au source and drain contacts. Liftoff was completed by leaving the deposited wafer in 1165 remover heated to 80 °C for 45 minutes. The extra metal was removed entirely using a pipette to blow off extraneous metal deposits. The front side was then protected with photoresist before starting backside fabrication. After the front side was protected, the graphene for the backside was transferred and patterned, followed by backside contact deposition. The photoresist was reapplied to the front side as needed to maintain protection. Upon completion, each side of the wafer had 25 devices, with increasing channel length from left to right and increasing channel width from top to bottom.

The testing phase was performed with a probe station to make initial contact with the devices. The silicon core was contacted by scratching the thin Al_2O_3 surface and used as a global back gate contact. The measurement device used to obtain the electrical testing information was a Keysight B1500A. Each GFET was tested for a back gate voltage between -10 V and 10 V and a VDS between -1 V and 1 V, which was in line with testing protocols used in other works [139, 141]. Tests were also performed for hysteresis and dual sided connection. The analytical software program GraphPad Prism was used to analyze the results.

5.2 Results and Discussion

Device characterization commenced with simple resistance tests. Notably, on the front side, 14 out of the 25 devices survived the process, while the backside saw 17 devices survive, leading to a success rate of 62%. The resistance values exhibited a wide range, from ~500 Ω to ~75,000 Ω, with 10 devices showing resistances higher than 10,000 Ω. These devices underwent further testing to ascertain FET operation. The FET testing was conducted within a range of ±10 V for the gate voltage and ±1 V for the drain voltage. This range was chosen to prevent the current from causing joule heating to the device. All testing was conducted in atmosphere, further avoiding any undesired heating of the devices under test. Tests were performed well after fabrication was completed to ensure repeatable results. Additionally, testing was done one side at a time, eliminating any crosstalk issues between the two sides.

Comprehensive device evaluation requires a sound understanding of GFETs. In this work, we rely on the traditional field-effect model to extract mobility. This model tends to underestimate the mobility of the given device due to the unknown variable of contact resistance. This

underestimation is lessened by using long channels [142]. Given that the shortest channel length of the devices is 100 um, it is possible to obtain accurate mobility information. The mobility can be obtained from Equation (5-1) below.

$$u = \frac{g_m L}{W V_D C_{ox}} \tag{5-1}$$

Equation (5-1) includes the transconductance, $g_m = dI_D / dV_G$, the channel length, L, channel width, W, drain voltage, V_D, and the gate oxide capacitance, C_{ox}. As the back gate capacitance is the capacitance of the Al_2O_3 layer, $C_{ox} = \varepsilon_r * \varepsilon_0 / t$, where ε_r is the relative permittivity, ε_0 is the vacuum permittivity, and t is the thickness. In the case of Al_2O_3, the relative permittivity is ~9, and the thickness is 30 nm. The result is a C_{ox} of 2.66 mF m^{-2}. The quantum capacitance of graphene is much larger than that of the back gate capacitance and thus can be safely neglected.

Other vital parameters of GFETs include the Dirac point and the residual carrier concentration. The Dirac point, V_{Dirac}, is where the drain current is at its lowest as the gate voltage is swept. This point indicates the doping type of the GFET, where a positive V_{Dirac} indicates p-type doping and a negative V_{Dirac} indicates n-type doping. Obtaining V_{Dirac} allows for the carrier concentration, n, to be obtained using Equation (5-2).

$$\mathbf{n} = \frac{C_{ox}}{q}(V_G - V_{Dirac}) \tag{5-2}$$

In Equation (5-2), q is the electron charge. The residual carrier concentration, n_0, is defined as the carrier concentration at $V_G = 0$ V. The residual carrier concentration, n_0, is generated by the charge impurities on graphene and the dielectric. A large n_0 means more scattering sites that can shift the Dirac point and partially explain suppressed currents [138].

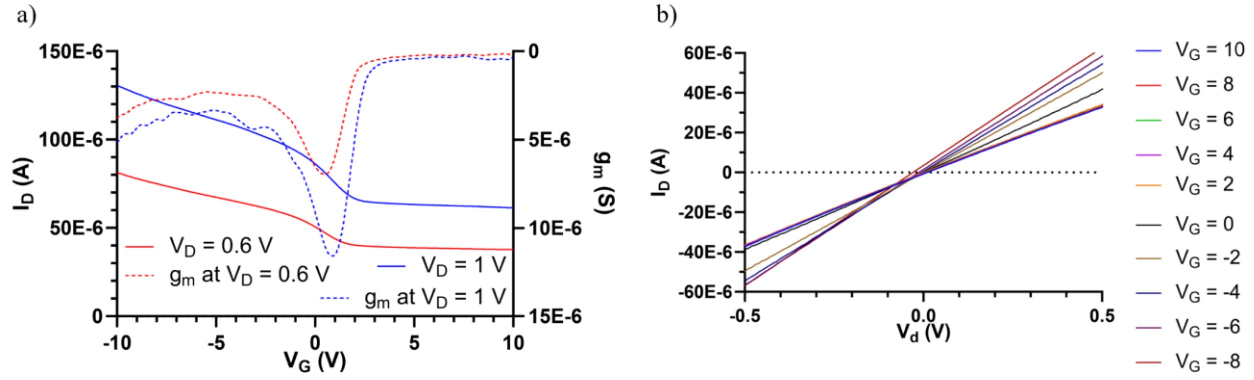

Figure 22. Electrical characterization result of a device on the front side of the wafer. a) V_G vs I_D, g_m graph at different V_D values. The red lines correspond to V_D = 0.6 V, while the blue lines correspond to V_D = 1 V. The straight lines are I_D curves with Y values on the left axis, while the dashed lines are g_m and have Y values on the right axis; b) V_D vs I_D graph at different V_G values.

A front side GFET result is shown in Figure 22. The V_G vs I_D test is given in Figure 22a. We observe a robust hole response for the given voltage, with a maximum hole transconductance value of $g_{m,p}$ = 11.585E-6 S at V_G = 0.87 V. The channel length was 100 um, and the width was 200 um. The hole mobility is calculated with Equation (5-1) as u_p = 21.8 cm^2 V^{-1} s^{-1}. The electron transconductance cannot be determined, as the transconductance never reaches a positive value. The max transconductance is -264 nS at V_G = 7.5V, which indicates that hole conductance is still dominant. As can be seen, electron mobility is significantly suppressed compared to hole mobility. This suppression could be due to moisture or the p-type doping of residual PMMA [138, 143]. Additionally, while the contacting Ti should result in n-type doping based on work function differences, several studies have shown that p-type doping can occur beneath such Ti/Au contacts, typically as a result of oxide formation. This creates a p-n junction that inhibits electron current at positive V_G [144-146]. Results shown later in this work demonstrate that the contact resistance for electron conduction is higher than for hole conduction, providing further proof. Since the GFETs

have a long channel length and are exposed to air, it is likely that atmospheric contaminants and PMMA residue are to blame for the p-type doping seen across devices [147]. The doping is seen in the positive V_{Dirac} value, which lies beyond the 10 V maximum gate voltage used. The resulting minimum value for n_0 is ~10^{13} cm^{-2}, indicating a very high residual carrier concentration.

The result of a V_D vs I_D test is given in Figure 22b. The intersection point of the lines was calculated to be -0.09 V. The two lines are highly linear, but the slope changes between negative and positive V_D. As V_D increases, the slope eventually changes to a smaller magnitude, mirroring the decreased electron mobility in the gate voltage test. The linearity of the lines shows that the device was not operating in the saturation region, which is partially caused by the high sheet carrier density.

These results were obtained for 14 devices on the front side. The hole mobility ranged from 10-50 cm^2 V^{-1} s^{-1}, showing a significantly suppressed result. The suppression is attributed to the fabrication process leaving some amount of residue, as well as the adsorption of environmental contaminants. Often, the Dirac voltage affirmed this, as it was outside the range of the gate voltage used here. The channel lengths and widths of each GFET provided little change to the overall mobility, as no size used provided a constraint to graphene's inherent properties as in a graphene nanoribbon [148]. The front-side results show that the current double fabrication process needs to account for the increased chances of impurities. Fewer impurities and adsorbates can be accomplished with more stringent cleaning protocols during transfer and fabrication and the implementation of encapsulation.

The V_G vs I_D results for a GFET on the back side are displayed in Figure 23 below. This device had a length of 100 um and a width of 150 um. The device showed a hole mobility of u_p = 768 cm^2 V^{-1} s^{-1} at V_G = 1.41 V and V_D = 0.5 V. The electron mobility was suppressed by

comparison, though we obtained a significantly positive transconductance. The device is one of two which show significant electron mobility. The electron mobility has a value of u_n = 312 cm^2 V^{-1} s^{-1} at V_G = 6.52 V and V_D = 0.5 V. Most other devices tested on this side did not have electron mobilities at this level. For V_D = 0.5V, the Dirac point is at V_{Dirac} = 4.27 V, indicating a moderately p-doped GFET. The Dirac voltage lowered to 4.13 V at V_D = 0.1 V. The change in the Dirac voltage is due to the change in charge concentrations at different voltages [149]. This result is close to the point where other devices show depressed conduction. The resulting n_0 of 7.07E12 cm^{-2} shows significant p-type doping compared to pristine graphene's n_0 of 0. This result shows that improved processing techniques can result in suitable GFET devices.

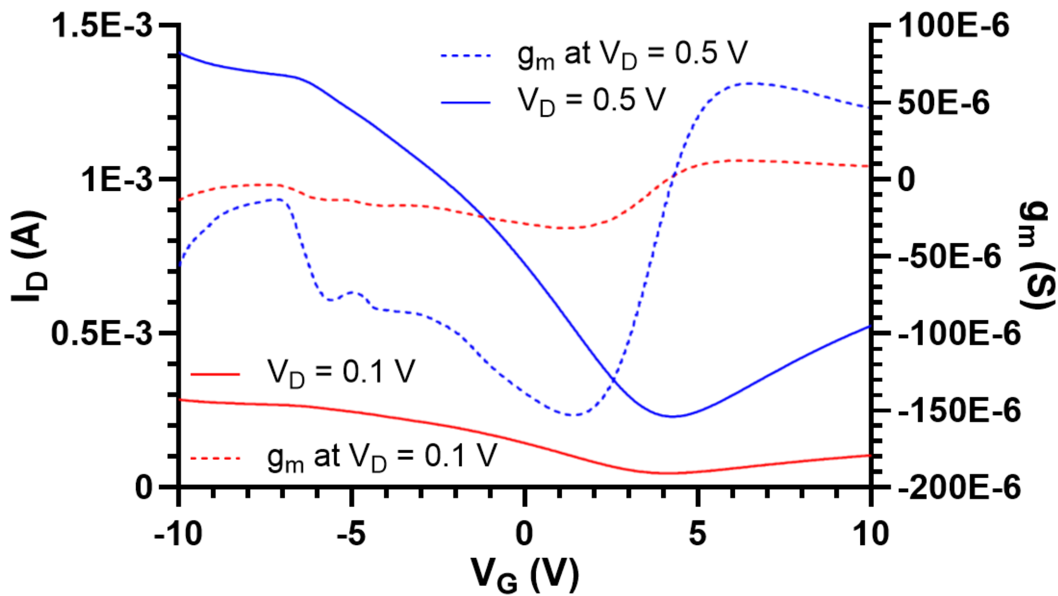

Figure 23. Electrical characterization result of a device on the back side of the wafer. V_G vs I_D and g_m graph at different V_D values. The red lines correspond to V_D = 0.1 V, while the blue lines correspond to V_D = 0.5 V. The straight lines are I_D curves with Y values on the left axis, while the dashed lines are g_m and have Y values on the right axis.

Further testing of the 17 back side devices demonstrated hole mobilities between 200 cm^2 V^{-1} s^{-1} and 900 cm^2 V^{-1} s^{-1}, showing a wide range of mobilities. Despite the differences in lengths and widths, there was no clear correlation with size. The Dirac voltage range stayed within 4-6V, though the slope of many devices did not fully cross over into electron conduction, indicating that the device was much more heavily doped than the testing protocol could observe. As with the front side, electron mobilities were often suppressed, only achieving up to 20 cm^2 V^{-1} s^{-1}. Only two devices showed mobilities over 100 cm^2 V^{-1} s^{-1}. As stated before, the low number of devices with suitable electron mobilities is likely due to the transfer process requiring further improvements, and alterations to the fabrication process to avoid unintended doping. Techniques to avoid unintended doping during fabrication will be discussed in future work. Regarding the transfer process, the residues left behind during the cleaning process need to be better accounted for, which can help lower the Dirac voltage towards 0 V. This can be seen in the high doping concentrations in many of the suppressed devices, which are over 1E13 cm^{-2}.

With the two devices that show significant electron mobility, it was possible to utilize the Y function method to extract further information from our devices. The Y-function method allows for the extraction of mobility without the influence of the contact resistance, R_C, which can also be extracted from the model [142, 150]. The model includes the contact resistance in the expression for $I_{ds} = A*V_D*(V_G-V_{Dirac}) / [1+A*R_C*(V_G-V_{Dirac})]$, where $A = (W/L)*u*C_{ox}$ which can be used to derive the new function for g_m. Here, $g_m = A*V_D / [1+A*R_C*(V_G-V_{Dirac})]^2$ and a function Y can be created such that $Y = I_D * g_m^{-1/2} = ([W/L]*u*C_{ox}*V_D)^{1/2} * (V_G-V_{Dirac})$, which allows the mobility to be extracted from the slope of (V_G-V_{Dirac}) vs $I_D*g_m^{-1/2}$. The extracted mobility can then be used in a plot of $g_m^{-1/2}$ vs (V_G-V_{Dirac}) to extract R_C. For the backside device, a hole and electron mobility of 1259 cm^2 V^{-1} s^{-1} and 512 cm^2 V^{-1} s^{-1} respectively, showing a considerable 60% improvement in

mobility. The extracted hole side R_C was 206 Ω, while the electron side was 289 Ω, which are favorable absolute results. However, once the resistance is normalized for width, the contact resistance is shown to be a major drawback of the current transistor design, reaching over 31 kΩ.um. The high contact resistance displayed in this device shows that the contact resistance in other devices likely plays a strong role in device characteristics despite the long channels [151]. Additionally, since the cleanliness of the backside is better than the front side, conditions allowed for better contact to arise with these devices and prevent the suppression of the electron branch [146]. Other designs have reached contact resistances of less than 1 kΩ.um [150]. Since the contact resistance plays a substantial role in traditional testing methods, refining future designs to lower the contact resistance should enable stronger results.

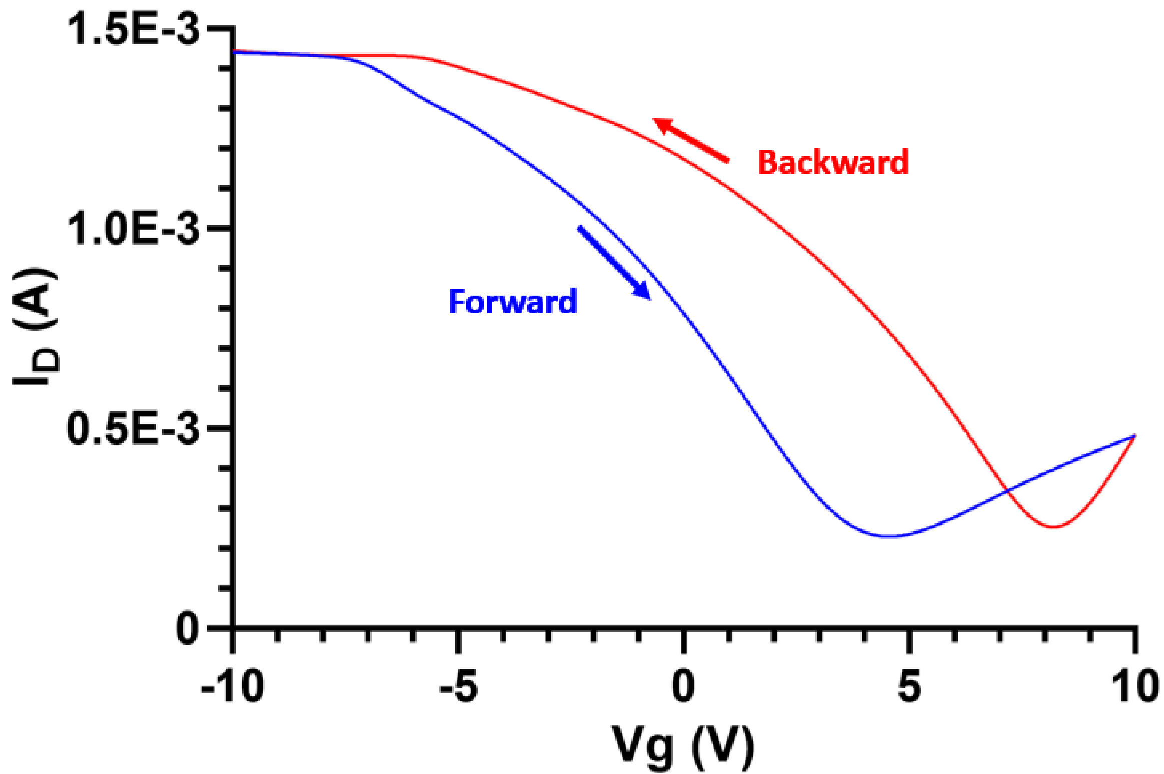

Figure 24. Hysteresis of Back Side Device

The hysteresis characteristics of the GFETs are shown in Figure 24. The gate voltage was swept forward from -10 V to +10 V and back to -10 V. The Dirac voltage on the forward sweep was 4.55V and shifted to 8.20V on the backward sweep, a positive shift of 3.65 V. The differences can be attributed to the charge transfer between graphene and defect sites in the oxide as the voltage is swept forward and back. The charge transfer may also occur between graphene and atmospheric contaminates. The negative voltage at the start of the test attracts the holes in graphene to the trap sites present in Al_2O_3, causing a positive charge to develop. The positive charge causes the graphene to be doped in the negative direction, leading to a smaller p-type doping than in the backward direction. The backward sweep causes holes to be injected from the oxide to graphene, leading to the positive shift of the Dirac voltage. As the doping effect of Al_2O_3 tends to be minor, adsorbates on the surface are likely primarily responsible for the overall p-type doping consistently found across devices. That the Dirac point is positive despite the magnitude of the negative starting voltage, which causes a negative shift in the Dirac point, further emphasizes the presence of atmospheric impurities. The shift in the Dirac point can be attributed to the accumulation of charges from the oxide and the contaminants [152, 153]. This shift shows the need to consider processes that provide encapsulation in future designs. Of additional note is that the electron mobility is far less suppressed when sweeping from the positive direction. The electron mobility shoots up to 976 $cm^2\ V^{-1}\ s^{-1}$ while the hole mobility remains relatively unchanged. Such a shift in mobility characteristics supports the idea that trap charges are becoming scattering centers for electrons, as when fewer holes are present in the oxide or contaminates, the electrons are not as affected [147].

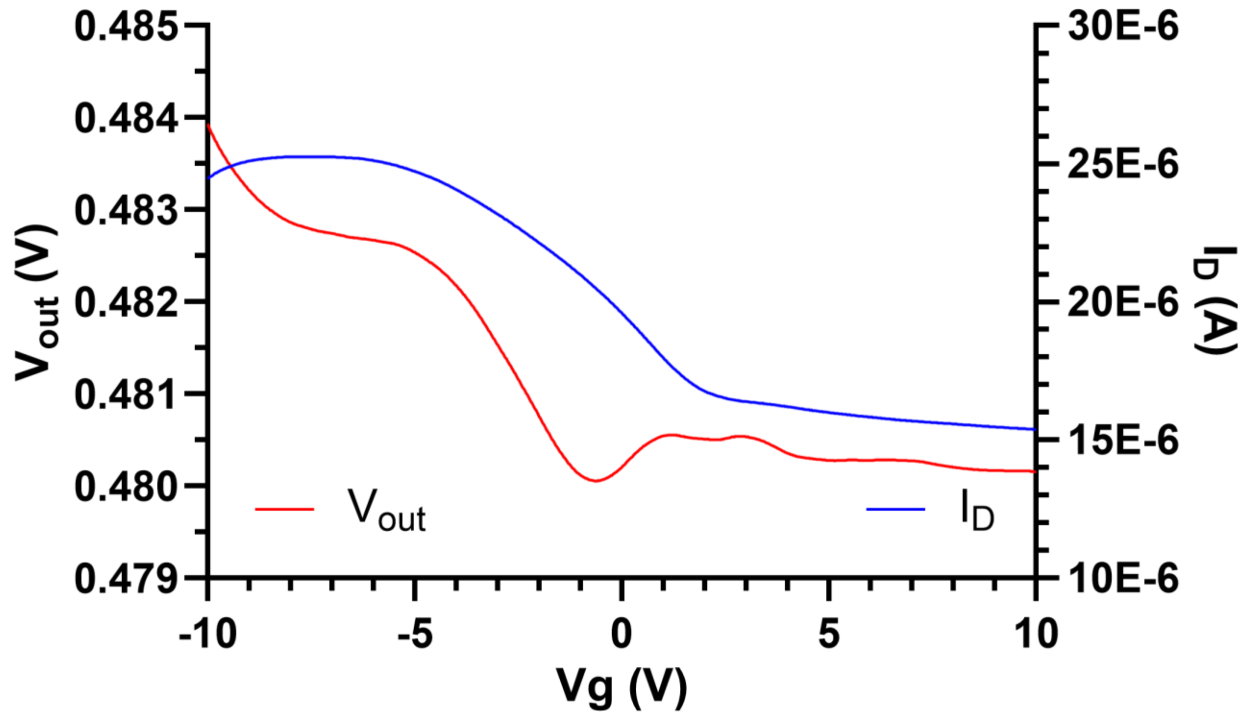

Figure 25. Two GFETs Connected in Inverter Configuration

Shown in Figure 25 is the output voltage of two GFETs connected in series in an inverter configuration. The resulting inverter achieves a voltage swing of 0.8% due to the low quality of the top side devices and both GFETs being p-type. The voltage gain, dV_{out}/dV_{in} was 0.0008 V/V at -2 V. However, the results show that the top and bottom of the wafer may be connected to provide additional functionality. An inverter can change an input to its logical opposite, a fundamental building block of more complex logic circuits. Once the fabrication process is improved and better inverters are shown, more complex designs, such as NAND or NOR gates, can be implemented. In this device, external connections were made between the two sides, the global Si back gate is used as the input voltage, and the output voltage is taken from between the two transistors, as seen on the left axis of Figure 25. The current is measured across both transistors with V_D = 0.5 V and on the right axis of Figure 25.

The results for the device's front and the back sides show that transistor fabrication is possible and thus creates exciting possibilities for future improvements. The increased n_0 on the front side indicates that the fabrication process should be refined to enable a cleaner process, as environmental factors strongly affect graphene. The increased processing the front side undergoes helps to explain the increased residual carrier concentration. A thorough cleaning process should be employed alongside encapsulation of the graphene channel to provide better protection against unwanted doping [154]. The encapsulation would also decrease variation between the top and bottom sides. A thicker oxide layer may be employed to allow a broader range of gate voltages, as the small range was used to prevent the breakdown of the oxide. Additionally, a transmission line structure can provide higher quality mobility results, including calculating the contact resistance [142]. Finally, the lack of TSV structures and individual top and bottom gates prevented a more complete prototype of a dual-sided wafer. Alternatively, an appropriate doping mechanism can allow both n-type and p-type unipolar GFETs to be fabricated.

6.0 Future Work

The investigations that have been undertaken have revealed the potential for graphene to make great strides in technological advancement. They have also shown the need for continued research into improved graphene growth and transfer processes, along with potential studies for clarifying the nature of graphene's interactions with other materials. Ultraclean and ultra-flat graphene transfer can be seen as the holy grail of graphene-based devices, and investigations towards that end will benefit future research. Since direct growth techniques are not always feasible, it falls onto these techniques to provide high-quality graphene for application use. These improvements will enable any application or physics-based research to yield better results, which can be distributed to the community.

Potential improvements to the transfer process can be investigated by combining previous research into a unified process. Many research projects have focused on improving one step of the transfer process. There is still more work to demonstrate how each step can contribute to a holistic process. For instance, PMMA can be modified to have a lower MW and be cleaned more efficiently with heated acetic acid. This modification is expected to yield graphene of higher quality than current processes. The use of APS has already been successfully included in this work. It may also be possible to adapt the methods of the support-free transfer process to improve graphene's flatness by reducing the effect of liquid surface tension. The reduction in surface tension may also enhance the reliability of the wet transfer process. The improved process can be used in application research, such as improving dual-sided GFETs. Such considerations should also be made for the growth process used, as ensuring that the transfer process has consistently high-quality graphene to be transferred is essential to the success of any transfer process. Effects could be directed

towards reducing the inherent wrinkling of graphene on copper sheets or increasing the grain size of grown graphene.

As the quality of transfer can affect any study on graphene's properties, such improvements can allow for retesting to see if improved transfer methods result in significant differences. In terms of studying surface interactions, modeling approaches such as density functional theory or molecular dynamics should be utilized to determine if any retesting of substrates should be undertaken with the improved transfer process. The modeling would enable the verification of results not well represented in the literature, such as the adhesion of graphene to metallic substrates. It would also allow for a baseline to be established for any future applied research projects.

This modeling approach can also be used to inform future research. The effect of a surface on graphene has yet to be completely understood, and thus, further research can be performed in this direction. The use of modeling would provide an idea of what can be expected of applied research. Modeling programs using density functional theory are widely available, including open source programs likes ABINIT and CONQUEST, and academic source programs like CASTEP. Similar programs are available for molecular dynamics studies. Each program would allow for the determination of various properties of graphene under different conditions, allowing the researcher to understand the results at a deeper level. Fonseca et al used a density functional theory model to determine the contact resistance for a metal-graphene interface. By modeling the interface for various metals, Fonseca was able to determine which metal would provide the lowest contact resistance and confirmed the results experimentally, enabling future projects to more efficiently create new devices [155]. Jang et al. used a molecular dynamics modeling approach to determine the adhesion of graphene nanoplatelets to a vinyl ester resin matrix. Their use of modeling allowed

the development of an optimized ratio of graphene to resin for increased strength and a larger operating range [156]. The use of different programs can even allow for the use of different theoretical approaches to determine which is more useful in a given context. The modeling accomplished can then be compared to results from experiments. The modeling can also allow optimized design structures to be developed more quickly.

Experiments that wish to compare to models can use various methods, including those used in this work. Future projects can additionally use conductive AFM (cAFM) and Kelvin Probe Microscopy (KPM) to determine what the underlying causes of graphene's property changes with greater spatial accuracy. Such methods can inform how the different substrates affect graphene on a more nuanced basis or provide clues as to which substrate would provide the best influences on graphene's properties given the desired parameters.

An additional avenue of research is on how to use the top surface of graphene to influence its properties. While the nanoparticles used in Chapter 4.0 showed significant differences, other methods may provide better results. Direct doping of graphene may be preferred as it would not cause a bend in graphene's mechanical structure, or functionalization may be used. If graphene is placed in the middle of two different substrates, as would be done in a top-gated approach, it would be worthwhile to understand how the confluence of different substrates may benefit graphene-based devices.

Continuing the dual-sided GFET project is straightforward, though many design considerations need to be made. A direct TSV integration using locally top-gated graphene transistors needs to be shown. These transistors should be appropriately connected to demonstrate their usability across both sides of the transistor. Such efforts can show true dual-sided processing capability and incorporate more complex logic gates. Further research can explore using one side

as a sensor while the second side is used to process and amplify sensor outputs, as shown in Figure 26. The research could be for various applications such as chemical or photo-sensing. Moreover, energy storage devices could benefit from using both wafer sides. The complicating factor is the need to tighten the fabrication process to reduce contact resistance and residues.

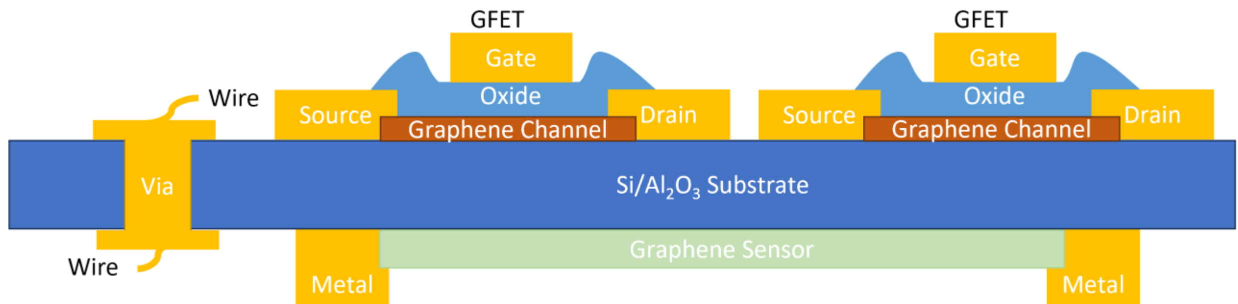

Figure 26. A conceptual example of a dual-sided graphene-based device

Initial attempts at continuing this line of research may benefit from using wafers with pre-established TSVs, which are available from companies such as IceMOS Technology. Alternatively, TSVs can be fabricated using the nanofabrication facilities at the University of Pittsburgh or Carnegie Mellon University. Such TSV-first approaches should prove more straightforward to design, allowing front and backside masks to use the TSVs as initial alignment markers. The formation of TSVs follows a five-step process: 1) etch, 2) oxide, 3) barrier/seed formation, 4) plating, and 5) chemical mechanical polishing. While there are several different ways to order the TSV formation, it is suggested to use a via-first approach, as the dual-sided wafer concept will need access to both sides of the layer. By creating the via first, the TSV process steps do not interfere with the fabrication of the GFETs. The TSV first approach should enable more GFET devices to survive the fabrication process than the TSV last approach.

The creation of TSVs is an understood process. The TSV fabrication process should begin by preparing a thin silicon wafer (300 um) for etching. After cleaning the wafer, a thick photoresist can be deposited in preparation for etching. The mask for this process should allow for the creation of TSVs that are at least 30 um in diameter, allowing for a less than 10:1 aspect ratio to be formed. A complete through etch can be performed by adhering the back of the wafer to a dummy wafer with a crystal bond wax. A Bosch process should be used to allow for directional etching. The process will involve using a deep RIE machine with alternating etching (SF_6 gas) and depositing a polymer passivation layer (C_4F_8 gas) [157]. This process forms the via that has a scalloped sidewall profile. The via can be smoothed by following a plasma treatment and solvent routine. A 20 minute NF_3 plasma treatment, followed by a 20 minute O_2 plasma treatment, can be performed. The plasma treatments are followed by using N-Methyl-2-pyrrolidone at 55 °C for 30 minutes. This process will successfully remove the polymer layer that was built up during the Bosch process [158]. Finally, a wet oxidation at 1000 °C can be performed. This oxide layer can be etched away using buffered oxide etchant.

After forming the via, an oxide needs to be formed to prevent electrical leakage. An ALD process can be used from both sides to create a layer of Al_2O_3. The creation of the oxide layer can be followed by the deposition of a nickel seed layer in preparation for electroplating to fill the TSV. Electroplating can be done with copper or nickel, which is necessary due to the thickness of metallization required. A wet etching process must be used to remove the excess metal, as a liftoff process cannot be performed. The etching process can consist of a combination of nitric acid and hydrochloric acid or a 30% solution of $FeCl_3$. These etchants will remove the excess nickel from both sides of the wafer. Care should be taken to avoid over-etching. The process will leave exposed TSVs on both sides of the wafer that can be used for further processing.

Once the TSVs are established, local top gates for each GFET should be created to allow individual control and provide protection from contamination. The literature displays various local top and back gate GFET designs, and designs for a more integrated dual-sided GFET should consider these. The gate inputs and outputs will need to be connected appropriately, a task that can be made simpler by appropriate utilization of the TSVs that were made. The creation of top gates is preferred as it ensures that graphene is encapsulated and thus protected from the environment.

The creation of a top gate structure for GFETs is also understood, though care needs to be taken to avoid damaging the graphene channel. One promising method is depositing a seed layer of Al_2O_3 at low temperatures (100 °C) followed by a high-temperature deposition to obtain a higher-quality Al_2O_3 layer. This method does not rely on seeding a layer of aluminum metal and thus will provide better electrical isolation to the gate contact from the drain and source contacts. The gate contact can be deposited using a Ti/Au process, and the Al_2O_3 can be etched through to allow contact with the buried source and drain contacts. The silicon core of the wafer can be employed as a back gate to control the doping level. However, a buried gate structure can allow each GFET to be tuned as a p-type or an n-type. This structure would involve putting a gate contact layer down as the first step and depositing a gate oxide layer on top. This bottom gate can be used to set the carrier type of the graphene FET. The graphene channel can then be created with drain and source contacts. Another top gate oxide and a gate contact can be deposited for the logic inputs. This structure would allow a fully featured IC design to be implemented. The data and power paths of the devices may be connected through TSVs depending on design requirements.

The fabrication of the new device should also ascertain whether different contact structures are necessary for better performance. It has been shown that different geometries of contacts can have a considerable effect on GFET mobility. Implementing a contact geometry that maximizes

the perimeter of graphene under the contact may increase mobility measurements. Additionally, the fabrication process needs to be altered to better remove residue. A potential avenue of success is using heated acetic acid to improve PMMA residue removal and vacuum annealing for extended periods before metal deposition to remove environmental adsorbates. A properly executed annealing process can also improve contact resistance. With an improved cleaning process and a top gate oxide protecting from additional processing, the unintended doping level can be substantially reduced.

Testing of the fabricated device can proceed as before. Any wired connections that need to be made outside the wafer can be made using solder or wire bonding processes. Probes can be used to make initial contact, and a wafer clamp can provide access to both the front and back of the wafer to allow for more precise testing. Due to the number of probes required, it would be beneficial to obtain more probe positioning units for ease of testing. Additionally, XPS testing can be performed to verify that oxygen vacancies are indeed a cause of the doping seen in the GFETs tested. As previously mentioned, the use of cAFM and KPM can provide more detailed analysis of graphene transistor characteristics. Tests performed inside a vacuum chamber can determine the effect of exposure to the atmosphere due to the elimination of the potential for redox reactions. A laser scan of the graphene channel may also provide detail about operating conditions. Furthermore, the fabrication of a transmission line structure can ensure that contact resistance has been decreased by a chosen method, such as annealing. An improvement to the analysis can come from the introduction of a new model. The models used in this work do not account for the changing carrier concentrations due to changing gate voltage. Updating the model to account for this variation should enable higher-quality investigations.

A final consideration should be made for the insulating layer used for the gate. In the research, oxygen atoms consistently appeared as major factors in graphene's apparent characteristics. The adhesion study determined that SiO_2 does not present graphene with a strong adhesion, but that a more polar material could better adhere to graphene. Hence, in the fabrication of the DSGFET, we choose Al_2O_3 due to its polar nature and excellent dielectric capabilities. In the TCR studies, we determined that oxygen atoms have a noticeable doping effect on graphene's carbon atoms, inducing a p-type doping effect. We noticed that this doping effect was reduced compared to Si_3N_4 atoms despite being a polar molecule and thus having a larger adhesion energy. The reduced doping effect was attributed to nitrogen atoms having a reduced interaction with graphene. Therefore, Si_3N_4 may be a better choice for graphene gate layers. Another polar material that should be investigated is AlN, another high-k dielectric material (~9). This material has already shown improved mobility and reduced p-type doping compared to using a SiO_2 layer [159]. A higher mobility at room temperature has also been shown for AlN compared to SiO_2 [147]. However, SiO_2 has an inferior dielectric constant to Si_3N_4, AlN, and Al_2O_3, and thus, a more direct comparison should be made to determine which material is better for GFET production. Aside from AlN, each material has shown the ability to be used for graphene encapsulation as well [160, 161]. Since oxygen atoms tend to interact strongly with graphene, seeking out non-oxide materials as the insulating layer for GFETs may be beneficial. Thus, an -in-depth comparison of these non-oxide materials, such as chalcogenides or nitrides, should be performed to elucidate if oxide or non-oxide insulators can provide higher-quality results. Based on our results and current capabilities, Si_3N_4 is a natural starting point for comparison. It can also prove beneficial to further understanding graphene's interactions and thus obtain the highest quality GFETs possible.

7.0 Conclusion

Understanding the substantial role of graphene surface interactions in device performance is crucial to maximize graphene's potential. In our research, an avenue for advancement in graphene transfer quality was discussed. We investigated surface interactions through adhesion energy and TCR testing. The adhesion energy was examined using the intercalation of nanoparticles method, which aided in gauging device reliability and design. The TCR was tested by placing SLG and MLG in a van der Pau configuration and subjected to temperature variations. These findings paved the way for future research directions.

As interfacial effects play a significant role in graphene behavior, improved growth and transfer processes are necessary to ensure the best performance. Accordingly, future work should enhance the growth and transfer processes available and communicate such results to the greater scientific community. Any research into the growth and transfer process needs to acknowledge that each process depends on the other. The highest quality graphene layer possible to be grown is the limit of the best possible transfer process, and any improvements to the growth process are constrained by the inadequacies of the transfer. Various methods have yet to be tested against each other, and some potential process improvements have yet to be reported. The possible impact of these improvements is significant, as they can be used to establish an ultraclean transfer method for improved graphene devices. Additionally, care should be chosen to choose the best transfer process for the desired application. Until a universal transfer method is found, modifying a process for increased compatibility per application may lead to improved results. The improved devices can inspire further advancements in the field by allowing graphene's exceptional properties to be unencumbered by defects.

The adhesion energy results showed that Young's modulus could be used to estimate the adhesion energy of graphene to a substrate, though additional surface interactions can strongly affect the outcome. These interactions can come in many varieties, such as the effect of charge interactions between materials, and can significantly affect the adhesion energy. Furthermore, the thickness of a 2D material will influence the results as well, though this only applies to thin films. The highest adhesion energy for graphene was observed with gold, measuring 7687.10 mJ m^{-2}.

The TCR testing described in Chapter 4.0 showed that substrate-induced scattering could affect graphene. The scattering breaks the symmetry of the top and bottom surfaces and introduces another scattering mode. The O atoms in SiO_2 functioned as such scattering sources. In SLG, the temperature increases resulted in increased mobility and decreased sheet concentration. Without the additional surface modifications made by MNPs, the highest effect was from Si_3N_4, with a 0.393% change per K. Crystalline SiO_2 provides the largest overall sheet resistance change of 0.456% per K when paired with MNPs. For MLG, the substrate effect is reduced by the bottom layer and is influenced by graphene thickness [162]. This reduction occurs because of the electric field provided by the bottom surface carriers and the decreasing field strength at a distance, even at these scales. Therefore, MLG has a reduced substrate effect compared to SLG, which was confirmed by the data.

The introduction of MNPs allowed the exploration of top surface channel modulation. MNP samples had higher resistances in all cases for two reasons: (i) structural deformations that are known to increase graphene resistivity were caused by strong surface binding [163]; (ii) charge transfer wells were created by the MNPs, reducing carrier efficiency. The MNPs affect the resistivity's response to temperature changes, differentiating SLG and MLG samples. SLG shows a decrease in the magnitude of the TCR due to the decreased efficiency. MLG shows an increase

in the TCR as the effect is reduced by the top layer and cannot outweigh the increased thermal motion. The situation is reversed in crystalline SiO_2, likely due to the influence of ordered O atoms.

The process improvements in the transfer techniques can be shown in a double-sided wafer application setting. The potential improvement of 3D ICs using a wafer coated with graphene on both sides is an exciting research opportunity. We have demonstrated a dual-sided graphene wafer concept, achieving a hole mobility of 1259 $cm^2\ V^{-1}\ s^{-1}$. The demonstration included single and connected FETs, though further research is needed to show a complete design. TSVs should be implemented to connect the front and back sides directly, and a complex system should be demonstrated. The fabrication process should be refined for better contact resistance and reduction in impurities. The results from this research provide a next-step platform for advanced graphene electronic devices, instilling confidence in the potential of our findings.

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